EFFECT OF GATE-OXIDE DEGRADATION ON ELECTRICAL PARAMETERS OF SILICON AND SILICON CARBIDE POWER MOSFETS

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ABSTRACT

EFFECT OF GATE-OXIDE DEGRADATION ON ELECTRICAL PARAMETERS OF SILICON AND SILICON CARBIDE POWER MOSFETS

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The power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is recognized as a crucial component of many power-electronic systems. The physical structure of both Silicon and Silicon Carbide power MOSFETs require an oxide layer as a dielectric material between their gate terminal and the semiconductor surface. The gate-oxide material, which is predominantly silicon dioxide, slowly degrades under the presence of an electric field. Over time, the degradation process significantly alters the electrical parameters of power MOSFETs, causing a negative impact on performance, reliability, and efficiency of power converters they are used in. In order to monitor this, the electrical parameters are utilized as precursors (or failure indicators) of gate-oxide degradation.

Despite extensive investigation of gate-oxide degradation in Silicon (Si) power MOSFETs, the research literature has not attributed a consistent variation pattern to its gate-oxide degradation precursors. This dissertation investigates the variation pattern of existing precursors: a) threshold voltage, b) gate-plateau voltage, and c) on-resistance. While confirming the previously reported dip-and-rebound variation pattern of the threshold voltage and the gate-plateau voltage, a similar dip-and-rebound variation pattern is also identified in the on-resistance of Si power MOSFETs. Furthermore, a new online precursor of gate-oxide degradation— the gate-plateau time, is proposed and demonstrated to exhibit a similar dip-and-rebound variation pattern. The gate-plateau time is also shown to be the most sensitive online precursor for observing the rebound phenomenon. In addition, the analytical expressions are derived to correlate the effect of gate-oxide degradation

with simultaneous dip-and-rebound variation pattern in all four precursors. The dip-and-rebound variation pattern is experimentally confirmed by inducing accelerated gate-oxide degradation in two different commercial Si power MOSFETs.

While multiple electrical parameters have been identified as precursors for monitoring the gate-oxide degradation in Si MOSFETs, very few precursors have been proposed for Silicon Carbide (SiC) power MOSFETs. This dissertation proposes that in addition to the threshold voltage, the other online precursors identified for Si power MOSFETs: the gate-plateau voltage and the gate-plateau time, are also effective for monitoring the effect of gate-oxide degradation process in SiC power MOSFETs. Though the gate-oxide material is the same in both Si and SiC power MOSFETs, the effect of gate-oxide degradation on the variation pattern of electrical parameters is different. In contrast to the dip-and-rebound variation pattern of precursors in Si MOSFETs, the research literature has attributed a consistent linear-with-log-stress-time variation pattern to the threshold-voltage shift in SiC power MOSFETs. It is shown that both the gate-plateau voltage and the gate-plateau time increase in a linear-with-log-stress-time manner similar to the threshold voltage. The analytical expressions are derived to correlate the effect of gate-oxide degradation with simultaneous linear-with-log-stress-time variation pattern in all three online precursors. The increasing trend of precursors is experimentally confirmed by inducing accelerated gate-oxide degradation in both planar and trench-gate commercial SiC power MOSFETs under high voltage, high temperature, and hard-switching conditions.

Dedicated to the memory of my beloved parents,
Bharat Man Karki and Minu (Ram Maya) Karki.

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Introduction

1.1 Background

The power MOSFET (Metal Oxide Semiconductor Field Effect Transistor) is recognized as a crucial component of many power-electronic systems. The silicon (Si) power MOSFETs has dominated the low voltage (< 200 V), low power (< 1 kW) and high frequency (> 100 kHz) power-electronic applications for a long time. The development of Silicon Carbide (SiC) MOSFETs has led to adoption of power MOSFETs in high voltage, high frequency and high power-density power-electronic applications, including renewable energy inverters, electric vehicle charging systems and three phase industrial motor drives [1].

The two common device structures for both Si and SiC power MOSFETs are: a) planar structure, and b) trench-gate (or U-MOSFET) structure, as shown in Figure 1.1. The physical structure of power MOSFETs require an oxide layer as a dielectric material between their gate terminal and the semiconductor surface, in the form of a Metal-Oxide-Semiconductor (MOS) sandwich, as shown within dashed rectangles in Figure 1.1. The gate terminal is placed over this insulating gate-oxide layer, which controls the operation of MOSFETs through the electric field across its oxide. When a positive bias is applied to the gate terminal, it attracts electrons at the surface of the semiconductor below the gate-oxide forming a conductive channel between the drain and source terminals. This conductive channel provides a path for the drain-source current when a positive drain voltage is applied.

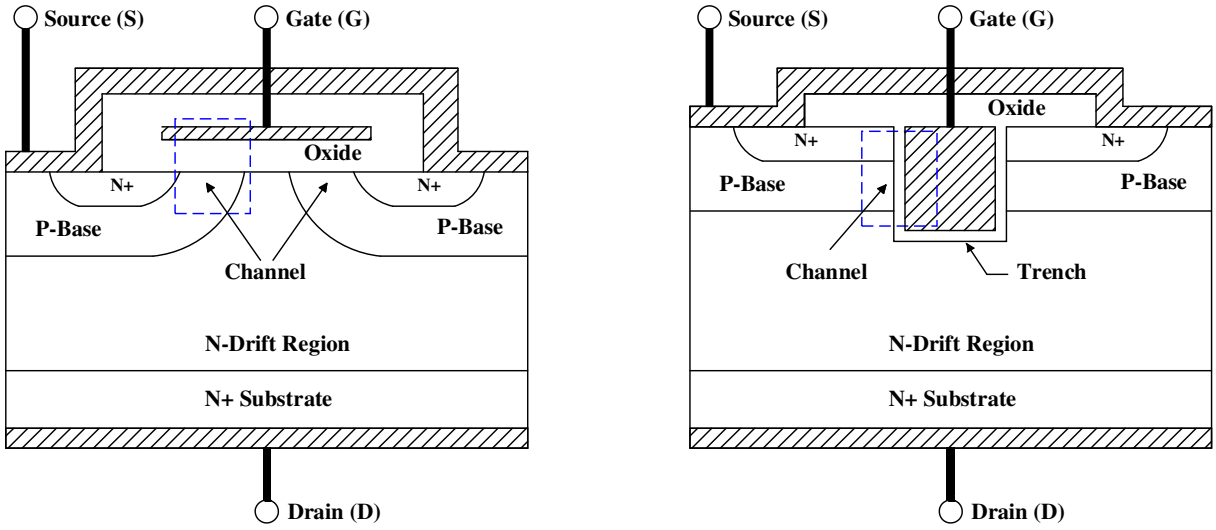


Figure 1.1: The elementary cell cross-section of (a) planar MOSFET, and (b) Trench-gate MOSFET.

1.2 Gate-Oxide Degradation in Power MOSFETs

The Si power MOSFET has a relatively thick gate-oxide layer (approximately 100 nm in 100 V, 5.6 A, IRF510, Si MOSFET [2]) as a dielectric material between its gate terminal and semiconductor surface. The gate-oxide material, which is predominantly silicon dioxide (SiO_2), slowly degrades over time. The degradation of gate oxide in Si power MOSFETs (also referred to as Si MOSFETs in this dissertation) under an electric field has been a subject of extensive investigation for nearly two decades [2]–[8]. These studies have established that the gate-oxide degradation in Si MOSFETs generates two primary types of charges: i) Oxide-trapped charge (Q_{ot}) within gate oxide, and ii) Interface-trapped charge (Q_{it}) at the oxide-silicon interface. These two

types of trapped charges significantly alter the electrical parameters of Si MOSFETs, which could shift the parameters out of their specifications over time, and in the worst case, lead to catastrophic failures in the power converters they are used in.

The gate-oxide material in both Si and SiC power MOSFETs degrades over time. However, the degradation process is more critical in SiC power MOSFETs (also referred to as SiC MOSFETs in this dissertation) than in their Si counterparts. This is because the gate oxide is designed to be thinner in SiC MOSFETs (approximately 50 nm in 1200 V, 36 A, CREE C2M0080120D SiC MOSFET [9]) to achieve a desirable threshold voltage [10]–[12]. Therefore, for the same gate-bias magnitude, a higher electric field appears across the gate oxide in SiC MOSFETs than in Si MOSFETs. Furthermore, if the devices were subjected to their respective maximum electric field, the internal electric field developed in the gate oxide in SiC MOSFETs (which is nearly 2.5 times the breakdown strength of SiC i.e., 2.5 x 3 MV/cm) could be approximately ten times larger than the electric field in the gate oxide in Si MOSFET (which is nearly 3 times the breakdown strength of Si i.e., 3 x 0.25 MV/cm) [11]–[14]. As a result, the gate oxide in SiC MOSEFTs could easily reach its reliability limits.

The number of oxygen vacancy related defects in SiO_2 is much larger in SiC-SiO_2 structure than in Si-SiO_2 structure [15]–[17]. As these defects are located near SiC-SiO_2 interface in the oxide, they are referred to as the near-interfacial oxide traps (NIOTs) [18]–[21]. The gate-oxide degradation in SiC MOSFETs has been attributed to charging of these oxide traps via a direct tunneling mechanism [16], [18], [19], [21]. The increase of charge states in oxide traps significantly alters the electrical parameters of SiC MOSFETs, thereby affecting the device performance, reliability and efficiency.

1.3 Precursors of Gate-Oxide Degradation in Power MOSFETs

In order to monitor the gate-oxide degradation process in both Si and SiC power MOSFETs, the electrical parameters are utilized as precursors (or failure indicators) of gate-oxide degradation. Most of the identified electrical parameters for the role of precursors in Si MOSFETs are offline precursors which cannot be directly monitored from the operating power-electronic system. Such electrical parameters are monitored using offline methods, in which the MOSFETs are physically removed from the power-electronic system/test setup and inserted into a device analyzer to obtain the electrical parameters of interest. On the other hand, online precursors enable monitoring of electrical parameters without physical removal of devices from operating power-electronic systems. Therefore, such precursors are extremely helpful in achieving real-time condition monitoring of gate-oxide degradation in power MOSFETs. In this dissertation, special emphasis has been given to the identification of new online precursors of gate-oxide degradation for power MOSFETs.

The threshold voltage is the most commonly studied precursor of gate-oxide degradation in Si power MOSFETs [2], [4], [6]–[8], [22]–[24]. The on-resistance, though a well-known precursor, has mostly been studied for assessing package-related failures during thermal or power cycling of power MOSFETs [25]–[28] and thus, very few studies have assessed its role as a precursor of oxide degradation [29], [30]. Recently, the gate-plateau (or miller) voltage was proposed as an online precursor of gate-oxide degradation for Si power MOSFETs [31]. In this dissertation, the gate-plateau time is proposed as a new online precursor of gate-oxide degradation for Si MOSFETs.

While multiple electrical parameters have been identified as precursors for monitoring the gate-oxide degradation in Si MOSFETs, very few precursors have been proposed for SiC MOSFETs. The Si and SiC MOSFETs might be different in terms of their substrate material, device characteristics and switching performances, but both belong to the same MOSFET family and have the same electrical parameter definitions. Following this reasoning, it is demonstrated in this dissertation that the precursors used for monitoring the gate-oxide degradation process in Si MOSFETs can also be extended to SiC MOSFETs.

1.4 Research Objectives and Contributions

The main objective of this research is to: i) investigate the effect of gate-oxide degradation on multiple electrical parameters of Si and SiC power MOSFETs, ii) identify new gate-oxide degradation precursors in both Si and SiC power MOSFETs, iii) identify the variation pattern of precursors unique to Si and SiC power MOSFETs, and iv) compare the sensitivity of precursors in both Si and SiC power MOSFETs.

The key contributions of this research investigating the effect of gate-oxide degradation mechanism on electrical parameters of Si power MOSFETs are summarized as follows:

- The effect of gate-oxide degradation on four electrical parameters: a) threshold voltage, b) gate-plateau voltage, c) gate-plateau time, and d) on-resistance is investigated both analytically and experimentally. It is confirmed that the above four precursors reflect the gate-oxide degradation process with a simultaneous dip-and-rebound variation pattern.

- The gate-plateau time is proposed as a new online precursor of gate-oxide degradation. The new precursor is demonstrated to exhibit a dip-and-rebound variation pattern over the course of gate-oxide degradation.

- The threshold voltage is determined to be the most sensitive indicator of the negative shift (dip), while the on-resistance and the gate-plateau time are determined to be the most sensitive indicators of the positive shift (rebound).

The key contributions of this research investigating the effect of gate-oxide degradation mechanism on electrical parameters of SiC power MOSFETs are summarized as follows:

- In addition to the threshold voltage, the other online precursors identified for Si MOSFETs: the gate-plateau voltage and the gate-plateau time, are shown to be suitable precursors for monitoring the effect of gate-oxide degradation process in SiC MOSFETs as well.

- The gate-plateau voltage and the gate-plateau time are shown to increase in a linear-with-log-stress-time manner similar to the threshold voltage, both analytically and experimentally.

- The threshold voltage is determined to be the most sensitive precursor of gate-oxide degradation in SiC MOSFETs, followed by the gate-plateau time and the gate-plateau voltage.

1.5 Outline

This dissertation is organized as follows:

Chapter 2 is aimed at providing detailed information about the effects of gate-oxide degradation on multiple electrical parameters: a) threshold voltage, b) gate-plateau voltage, c) gate-plateau time, and d) on-resistance of Si power MOSFETs. The background information regarding the nature of the oxide-trapped charges and the interface-trapped charges, and their effects on electrical parameters of Si MOSFETs are presented first. The analytical expressions derived to correlate the effect of gate-oxide degradation with simultaneous dip-and-rebound variation pattern in all four precursors are presented next. Then, the significance of dip-and-rebound variation pattern in terms of device performance, reliability and efficiency is discussed. Finally, the experiment results confirming the dip-and-rebound variation pattern in two different commercial Si power MOSFETs are presented.

Chapter 3 is aimed at providing detailed information about the effects of gate-oxide degradation on multiple electrical parameters: a) threshold voltage, b) gate-plateau voltage, and c) gate-plateau time of SiC MOSFETs. The background information regarding the direct tunneling process and their effects on electrical parameters in SiC MOSFETs are presented first. The analytical expressions derived to correlate the effect of gate-oxide degradation with linear-with-log-stress-time variation pattern in all three precursors are presented next. Then, the significance of linear-with-log-stress-time variation pattern in terms of device performance, reliability and efficiency is discussed. The high-temperature double-pulse test setup with provisions for inducing accelerated gate-oxide degradation in SiC MOSFETs is described next. Finally, the experimental results confirming the linear-with-log-stress-time variation pattern in both planar and trench-gate

commercial SiC MOSFETs under high voltage, high current, high temperature and hard-switching conditions are presented.

Chapter 4 provides concluding remarks.

Chapter 5 discusses possible future works.

Chapter 2

Effect of Gate-Oxide Degradation on Electrical Parameters of Silicon Power MOSFETs

2.1 Introduction

The degradation of gate oxide in Si MOSFETs under an electric field has been a subject of extensive investigation for nearly two decades [2]–[8]. These studies have established that the degradation of SiO_2 introduces two primary charges that significantly alter the electrical parameters of a power MOSFET: i) Oxide-trapped charge (Q_{ot}) within gate oxide, and 2) Interface-trapped charge (Q_{it}) at the oxide-silicon interface.

The electrical parameters serve as precursors (or failure indicators) of gate oxide degradation in power MOSFETs. However, in terms of observing the effects of gate-oxide degradation, very few precursors have been identified. The threshold voltage (V_{TH}) is the most commonly studied precursor of gate-oxide degradation in power MOSFETs [2], [4], [6]–[8], [22]–[24]. The on-resistance (R_{ON}), though a well-known precursor, has mostly been studied for assessing package-related failures during thermal or power cycling of power MOSFETs [25]–[28] and thus, very few studies have assessed its role as a precursor of oxide degradation [29], [30]. However, it is shown later that R_{ON} varies significantly over the stress period and should therefore be considered an important precursor of gate-oxide degradation. Recently, the gate-plateau (or miller) voltage (V_{GP}) was proposed as an online precursor of gate-oxide degradation for power MOSFETs [31]. In this

chapter, the gate-plateau time (t_{GP}) is proposed as a new online precursor of gate-oxide degradation. In comparison to V_{GP}, this new precursor is shown to be a more sensitive indicator of Q_{it}. It is interesting to note that online precursors, unlike offline precursors, can be extracted without affecting system operation. The extraction of online precursors: V_{TH}, V_{GP} and t_{GP}, can all be done from the same turn-on waveform of a power MOSFET shown in Figure 2.1, without physical removal from operating power-electronic systems.

The precursors exhibit a distinct variation pattern due to accumulation of Q_{ot} and Q_{it} over the course of oxide degradation. In [2], [4], [6], [7], it is reported that the threshold voltage initially decreases (i.e., dips) due to a buildup of positive Q_{ot}, but it rises back to its initial value and beyond (i.e., rebounds) due to an accumulation of negatively charged Q_{it}. This dip-and-rebound variation is also known as the turn-around effect [4], [22], [32], [33]. Recently, a similar dip-and-rebound variation pattern was also observed in gate-plateau (or miller) voltage, although only at certain gate-bias stress magnitude [31]. On the other hand, some literatures have reported that precursors only increase (or rebound) over time. For instance, the threshold voltage and the on-resistance have been reported to only increase due to gate-oxide degradation [23], [24], [30], [34]. While

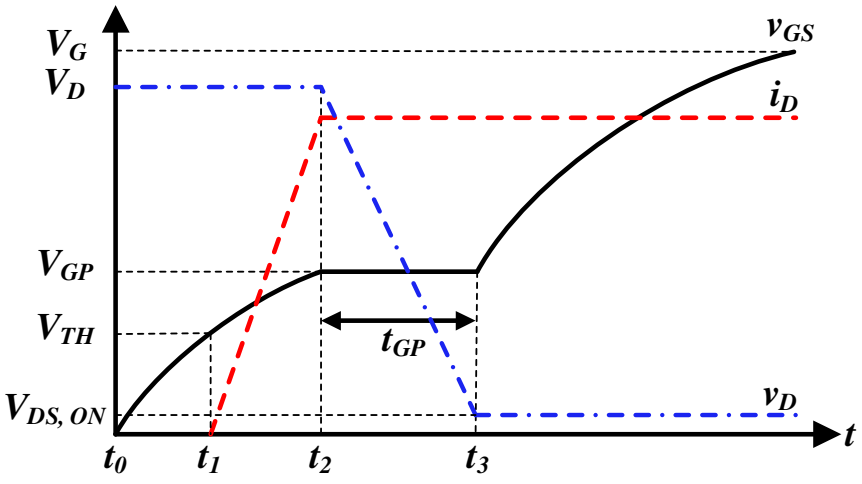


Figure 2.1: Typical turn-on waveform of Power MOSFETs.

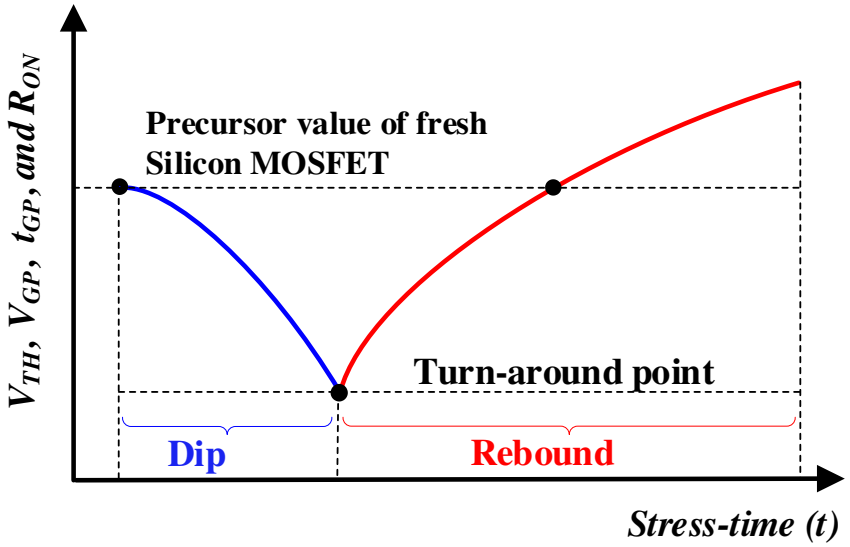


Figure 2.2: Expected dip-and-rebound variation pattern of electrical parameters during gate-oxide degradation in Si MOSFETs.

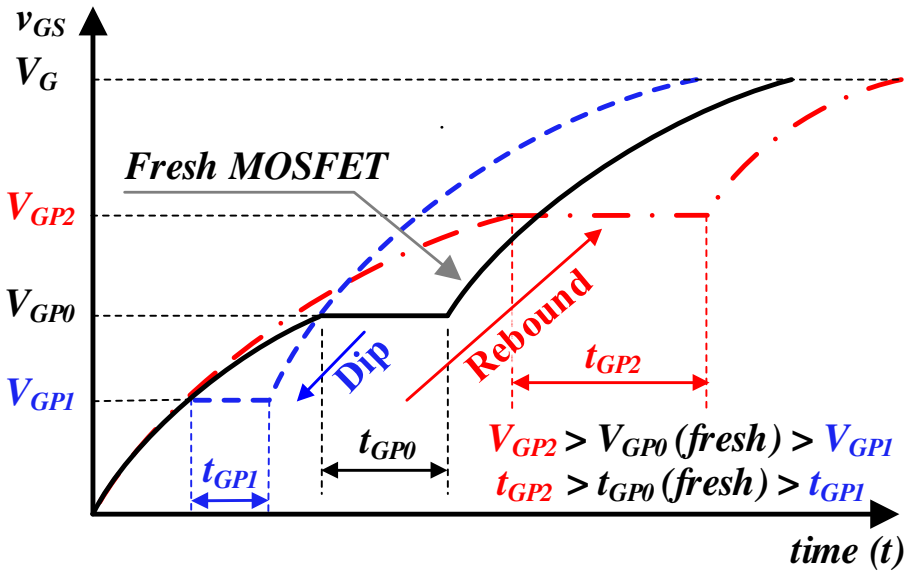


Figure 2.3: Expected degradation trend of precursors as shown in gate-source voltage waveform during turn-on of Si MOSFETs.

confirming the dip-and-rebound variation pattern of precursors, we observed that, if measurements were not taken at brief intervals especially during initial stages of degradation, the initial dip might not be observed at all. This is because the effect of Q_{ot} is dominant during initial stages of degradation [3], [22], [31], [35], and depending upon the electrical stress, its effect may be observable for a relatively short time. It is important to note that all electrical parameters mentioned above: V_{TH}, R_{ON}, V_{GP}, and t_{GP}, bear a strong analytical relationship with Q_{ot} and Q_{it} through the threshold voltage. Therefore, we can expect the variation of other precursors to replicate the dip-and-rebound variation pattern of V_{TH} over the course of gate-oxide degradation as shown in Figure 2.2. The precursors initially dip, reach their minimum values at turn-around point, and then rebound to their initial values and beyond. The expected degradation trend of precursors in Si MOSFETs can be observed in gate-source voltage waveform during turn-on, as shown in Figure 2.3, where V_{GP2} (rebound) > V_{GP0} (fresh MOSFET) > V_{GP1} (dip), and t_{GP2} (rebound) > t_{GP0} (fresh MOSFET) > t_{GP1} (dip).

The purpose of this chapter is three-fold: 1) To propose a new online precursor of gate-oxide degradation — the gate-plateau time; 2) To demonstrate a simultaneous dip-and-rebound variation pattern of all four precursors of gate-oxide degradation (V_{TH}, R_{ON}, V_{GP}, and t_{GP}); and 3) To compare the shift tendencies of each precursor over the course of gate-oxide degradation. It is shown that all four precursors reflect the gate-oxide degradation status with a simultaneous negative and positive shift from their initial values. The threshold voltage was found to be the most suitable precursor for observing the negative shift (dip) while R_{ON} and t_{GP}, were found to be the most suitable precursors for observing the positive shift (rebound). Such an understanding of the nature of variation of these precursors will enable an effective and redundant monitoring of gate-oxide degradation process in power MOSFETs while being used in real power-electronic systems.

The rest of this chapter is organized is as follows. Section 2.2 provides background information about the effect of gate-oxide degradation in power MOSFETs. Section 2.3 investigates the variation of all four precursors with respect to the type of trapped charges. Section 2.3 explains the significance of dip-and-rebound variation pattern. Section 2.4 explains the experimental setup and precursors' measurement methods in detail. The subsequent sections provide experimental verification of variation patterns in two commercially available power MOSFETs (IRF510 and IRF520).

2.2 Gate-Oxide Degradation Mechanism in Silicon MOSFETs

The two well-known vertical structures of power MOSFETs are shown in Figure 1.1. These MOSFETs have a relatively thick gate-oxide layer as a dielectric material between the gate terminal and semiconductor surface. The Metal-Oxide-Semiconductor (MOS) sandwich thus formed is shown within dotted rectangles in Figure 1.1.

The degradation of gate oxide under electric field has been a subject of extensive investigation for nearly two decades. Several researches have been devoted to the theoretical and analytical study of the effects of trapped charges on threshold voltage and mobility [2]–[4], [6]–[8]. Based on these studies, the gate-oxide degradation generates two primary types of charges: i) Oxide-trapped charge (Q_{ot}) within gate oxide, and ii) Interface-trapped charge (Q_{it}) at the oxide-silicon interface. The present understanding of the effect of trapped charges on threshold voltage can be summarized into three stages as shown in Figure 2.4.

Stage I: This represents the MOS structure before the initiation of gate-oxide degradation. It is assumed that there are no Q_{ot} or Q_{it} within gate oxide prior to degradation.

Stage II: During the initial phase of degradation, Q_{ot} begins to build up within gate oxide. These oxide-trapped charges exhibit donor like behavior and are positively charged. The presence of positive Q_{ot} increases effective electric field across the gate oxide and contributes to the inversion of the channel. This leads to a decrease of threshold voltage in power MOSFETs. The threshold voltage may even decrease (dip) to a negative value causing a "normally OFF" (or enhancement type) MOSFET to become a "normally ON" (or depletion type) MOSFET.

Stage III: After a buildup of a certain threshold of Q_{ot}, interface traps begin to form at oxide-silicon interface. Since there is a time delay between the creation of Q_{ot} and the creation of interface traps, the effects of Q_{ot} is observable at early stages of degradation. However, after a certain time, the increase of interface traps become very dominant. Since the interface traps can interact electrically with the charge carriers, they begin to capture electrons and, in the process, become negatively charged in a n-channel MOSFET. Additionally, the build-up of negatively charged Q_{it} compensates the effect of oxide field. Thus, a higher electric field is required across the oxide for channel inversion. This leads to an increase (rebound) of threshold voltage in power MOSFETs. Upon prolonged stress, the threshold voltage rises to back its initial value and beyond, allowing the power MOSFET to regain its "normally-OFF" state.

Based on above discussion, the threshold voltage shift can be represented as a sum of the shifts due to positive oxide-trapped charges (during stage II) and negative interface-trapped charges

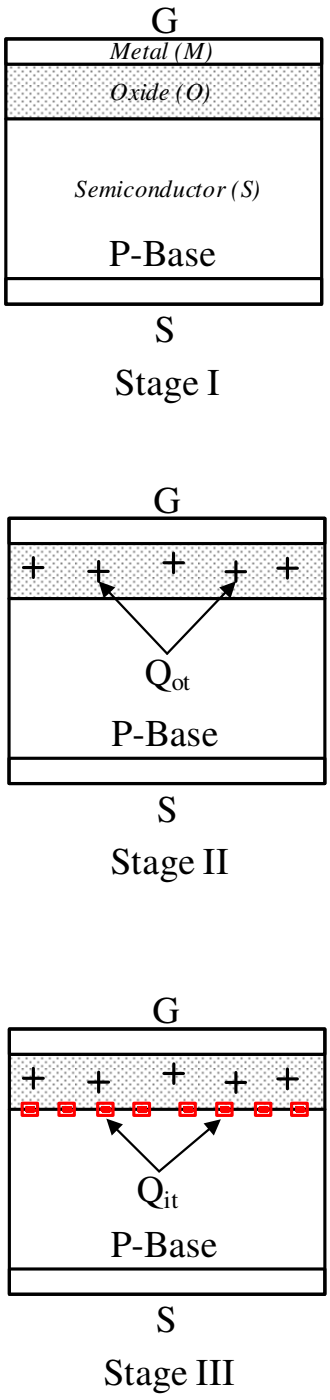


Figure 2.2: Stages of gate-oxide degradation.

(during stage III). The positive oxide-trapped charges have an effect of reducing the threshold voltage while the negative interface-trapped charges have an effect of increasing the threshold voltage. It is also important to mention that both accumulation of Q_{ot} and Q_{it}, reduce channel carrier mobility. However, the mobility reduction is primarily due to scattering from charges in interface traps [36]–[38]. The empirical expression modeling the effect of gate-oxide degradation mechanism on threshold-voltage shift and channel carrier mobility reduction is given by [2], [7]

$$V_{TH} = V_{TH0} - \frac{qN_{ot}}{C_{ox}} + \frac{qN_{it}}{C_{ox}} \text{ , and} \tag{2.1}$$

$$\mu = \frac{\mu_o}{1 + \alpha_{ot} N_{ot} + \alpha_{it} N_{it}} \quad , \tag{2.2}$$

where V_{TH0} and μ_o are the initial values of threshold voltage and mobility respectively, N_{ot} and N_{it} are the stress-induced changes in densities of Q_{ot} and Q_{it} respectively, and α_{ot} and α_{it} are the coefficients describing the effects of Q_{ot} and Q_{it} respectively.

2.3 Investigation of Variation of Precursors

It is important to note that other electrical parameters: V_{GP}, t_{GP}, and R_{ON}, bear a strong analytical relationship with threshold voltage. Therefore, we can expect the variation of these failure precursors to replicate the dip-and-rebound variation pattern of V_{TH} over the course of gate-oxide degradation. In this section, the analytical expressions of four precursors are analyzed to show their respective dip-and-rebound variations.

2.3.1 Variation of Threshold Voltage

The partial derivative of V_{TH} in equation (2.1) with respect to (w.r.t) N_{ot} and N_{it} results in

$$\frac{\partial V_{TH}}{\partial N_{ot}} = -\frac{q}{C_{ox}} < 0 \text{ , and} \tag{2.3}$$

$$\frac{\partial V_{TH}}{\partial N_{it}} = \frac{q}{C_{ox}} > 0 . \tag{2.4}$$

The partial derivative of V_{TH} w.r.t N_{ot} in equation (2.3) is negative. Similarly, the partial derivative of V_{TH} w.r.t N_{it} is positive. This follows our previous discussion that V_{TH} decreases with increase of N_{ot} and increases with increase of N_{it}, indicating a dip-and-rebound variation pattern.

2.3.2 Variation of Gate-plateau Voltage

Recently, V_{GP} was proposed as a precursor of gate-oxide degradation and its analytical relationship with respect to the trapped charges was derived for power MOSFETs in [31]. However, the dip-and-rebound pattern was not observed for all gate bias-stress magnitude. As we pointed out earlier, if measurements were not taken at brief intervals especially during initial stages of degradation, the initial dip might not be observed at all. The gate-plateau voltage of a vertical-diffused (VD) MOSFET is given by [39]

$$V_{GP} = V_{TH} + \sqrt{\frac{I_D L_{CH}}{\mu C_{ox} Z}} , \tag{2.5}$$

where I_D is the drain current, L_{CH} is the channel length, Z is the channel width and C_{ox} is the specific gate-oxide capacitance.

The partial derivative of V_{GP} w.r.t N_{ot} and N_{it} results in

$$\frac{\partial V_{GP}}{\partial N_{ot}} = \frac{\partial V_{TH}}{\partial N_{ot}} - \frac{1}{2\mu_o^{3/2}} \sqrt{\frac{I_D L_{CH}}{C_{ox} Z}} \frac{\partial \mu}{\partial N_{ot}} \quad \text{, and} \tag{2.6}$$

$$\frac{\partial V_{GP}}{\partial N_{it}} = \frac{\partial V_{TH}}{\partial N_{it}} - \frac{1}{2\mu_o^{3/2}} \sqrt{\frac{I_D L_{CH}}{C_{ox} Z}} \frac{\partial \mu}{\partial N_{it}} \quad . \tag{2.7}$$

Since the manufacturing parameters of commercial power MOSFETs are not always provided in the datasheet, an appreciable effort was made to determine the sign of equation (2.6) in [31]. As mentioned before, the presence of both Q_{ot} and Q_{it} reduce the channel carrier mobility. However, since the mobility reduction is primarily due to interface trapped charges [36]–[38], we can assume that the decrease of mobility due to N_{ot} in equation (2.6) is negligible. This assumption simplifies the analytical expressions of (2.6) and (2.7) to

$$\frac{\partial V_{GP}}{\partial N_{ot}} \simeq \frac{\partial V_{TH}}{\partial N_{ot}} \quad < 0 \text{, and} \tag{2.8}$$

$$\frac{\partial V_{GP}}{\partial N_{it}} = \frac{\partial V_{TH}}{\partial N_{it}} - \frac{1}{2\mu_o^{3/2}} \sqrt{\frac{I_D L_{CH}}{C_{ox} Z}} \frac{\partial \mu}{\partial N_{it}} \quad > 0 . \tag{2.9}$$

As the partial derivative of V_{TH} w.r.t N_{ot} is negative, the partial derivative of V_{GP} w.r.t N_{ot} in equation (2.8) is also negative. Also, since V_{TH} increases with respect to N_{it} and μ decreases with respect to N_{it}, the partial derivative of V_{GP} w.r.t N_{it} in equation (2.9) is positive. This means that V_{GP} initially decreases due to accumulation of N_{ot}. As the formation of N_{it} begins to compensate the effect of N_{ot}, V_{GP} rebounds to its initial value and beyond. The shift tendency of V_{GP} due to

trapped charges is illustrated in Figure 2.5, where $V_{GP2} > V_{GP0}$ (Fresh MOSFET) > V_{GP1}. This indicates that V_{GP} dips initially, and then rebounds like V_{TH}.

2.3.3 Variation of Gate-Plateau Time

The gate-plateau time (t_{GP}) is proposed as a new online precursor of gate-oxide degradation. This is the time span where the gate voltage remains constant and equal to V_{GP} [time span (t_3-t_2) in Figure 2.1]. During this time span, the drain voltage (v_D) gradually decreases at a rate given by [39]

$$\frac{dv_D}{dt} = -\frac{V_G - V_{GP}}{R_G C_{GD,av}}\ , \tag{2.10}$$

where R_G is the gate resistance, V_G is the gate voltage and $C_{GD,av}$ is an assumed average value of gate-drain capacitance during the transient.

As seen from equation (2.10), the rate of change of v_D depends on the magnitude of R_G and V_{GP}. For a given R_G, a smaller V_{GP} results in a larger dv_D/dt and vice versa. Furthermore, a larger dv_D/dt corresponds to a smaller t_{GP} and vice versa. The presence of Q_{ot} leads to a smaller V_{GP} and thus, a smaller t_{GP}, while the presence of Q_{it} leads to a larger V_{GP} and thus, a larger t_{GP}. This is illustrated in Figure 2.5, where $t_{GP2} > t_{GP0}$ (Fresh MOSFET) > t_{GP1}. This indicates that t_{GP} dips and rebounds like V_{TH} and V_{GP}.

The variation of t_{GP} can also be explained using quantitative method. The time interval (t_3-t_2) of a power VD MOSFET is given by [39]

$$t_{GP} = t_3 - t_2 = \frac{R_G C_{GD,av}}{V_G - V_{GP}}\left[V_{DS} - v_{D(t3)}\right]. \tag{2.11}$$

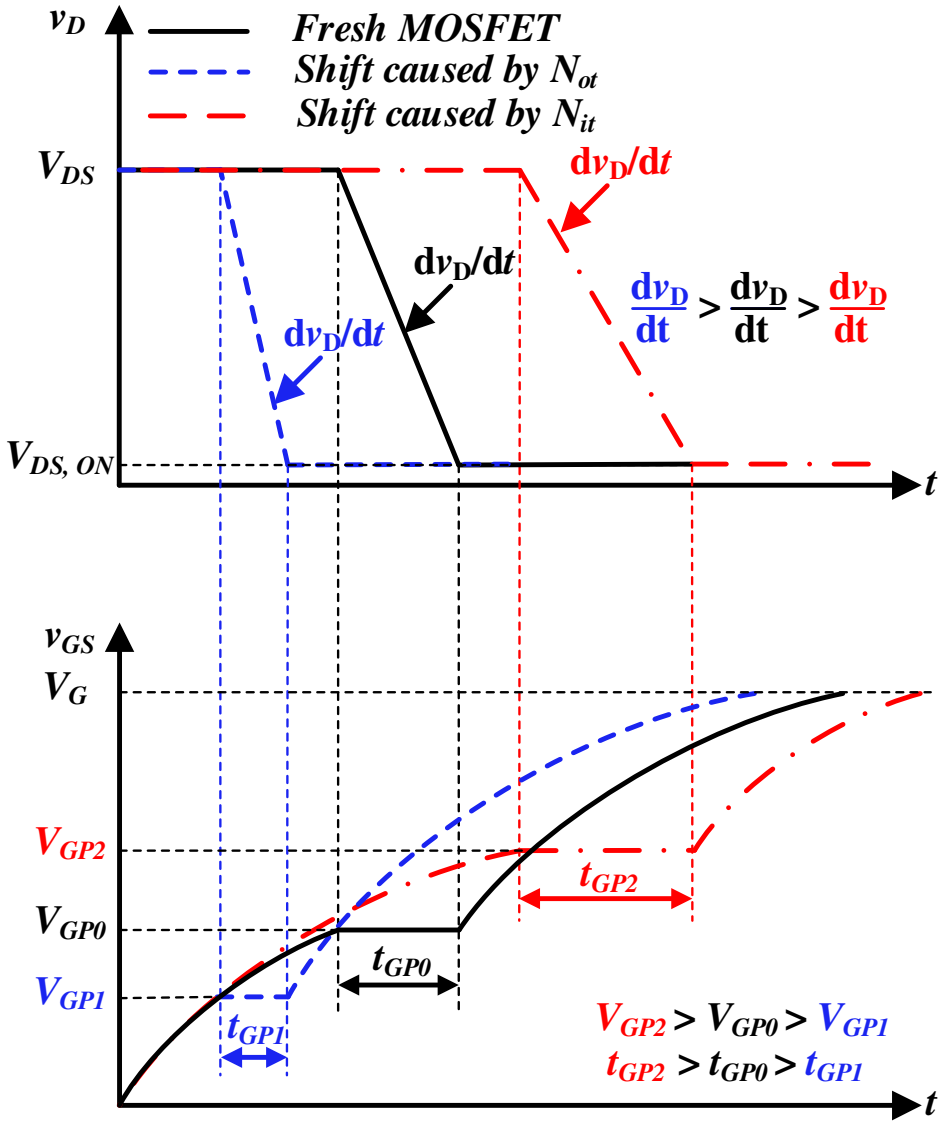


Figure 2.3. Shift tendencies of V_{GP} and t_{GP}.

As shown in the turn-on waveform in Figure 2.1, at the end of time t_3, the drain voltage $v_D(t_3)$ becomes nearly equal to the on-state voltage drop of the power MOSFET. Thus, $v_D(t_3)$ can be considered negligible. Therefore, the expression for t_{GP} in equation (2.11) can be re-written as

$$t_{GP} = t_3 - t_2 = R_G C_{GD,av} \frac{V_{DS}}{V_G - V_{GP}} \ . \tag{2.12}$$

The partial derivative of t_{GP} w.r.t. N_{ot} and N_{it} results in

$$\frac{\partial t_{GP}}{\partial N_{ot}} = R_G C_{GD,av} \ \frac{V_{DS}}{(V_G - V_{GP})^2} \ \frac{\partial V_{GP}}{\partial N_{ot}} \quad < 0 \text{ , and} \tag{2.13}$$

$$\frac{\partial t_{GP}}{\partial N_{it}} = R_G C_{GD,av} \ \frac{V_{DS}}{(V_G - V_{GP})^2} \ \frac{\partial V_{GP}}{\partial N_{it}} \quad > 0 \ . \tag{2.14}$$

respectively. Since the partial derivative of V_{GP} w.r.t N_{ot} is negative in equation (2.8), the partial derivative of t_{GP} w.r.t N_{ot} in equation (2.13) is also negative. This indicates that t_{GP} decreases with increase of N_{ot}. Similarly, since the partial derivative of V_{GP} w.r.t N_{it} is positive in equation (2.9), the partial derivative of t_{GP} w.r.t N_{it} in (2.14) is positive. This indicates that t_{GP} increases with increase of N_{it}. Thus, t_{GP} follows a dip-and-rebound variation pattern like V_{TH} and V_{GP}.

2.3.4 Variation of On-Resistance

The on-resistance of the power MOSFET shown in Figure 1.1 is mainly composed of four resistances: channel resistance R_{CH}, accumulation layer resistance R_A, drift resistance R_D, and contact resistance R_C [30], [39]. The presence of trapped charges due to gate-oxide degradation mainly affects R_C and R_A [30]. Thus, the variation of R_{CH} and R_A reflects the variation of R_{ON} of

power MOSFETs. These resistances are given by [39]

$$R_{CH} = \frac{L_{CH}}{2Z\mu C_{ox}(V_G - V_{TH})} \text{ , and} \tag{2.15}$$

$$R_A = \frac{L_A}{2Z\mu_{nA} C_{ox}(V_G - V_{TH})}, \tag{2.16}$$

where Z is the length of the cell in the orthogonal direction to the cross section shown in Figure 1.1, L_{CH} is the channel length, L_A is the accumulation layer path, μ is the inversion-layer mobility, μ_{nA} is the accumulation-layer mobility and C_{ox} is the specific gate-oxide capacitance.

As mentioned before, the effect of N_{ot} on mobility is assumed to be negligible. Thus, the derivative of R_{CH} w.r.t N_{ot} and N_{it} can be simplified to

$$\frac{\partial R_{CH}}{\partial N_{ot}} = \frac{L_{CH}}{2Z\mu C_{OX}(V_G - V_{TH})^2} \frac{\partial V_{TH}}{\partial N_{ot}} \quad < 0 \text{ , and} \tag{2.17}$$

$$\frac{\partial R_{CH}}{\partial N_{it}} = \frac{L_{CH}}{2Z\mu^2 C_{OX}(V_G - V_{TH})^2} \left[\mu \frac{\partial V_{TH}}{\partial N_{it}} - (V_G - V_{TH}) \frac{\partial \mu}{\partial N_{it}} \right] \quad > 0 . \tag{2.18}$$

The field dependence of the accumulation-layer mobility is very similar to inversion-layer mobility [38]. Thus, the presence of trapped charges can be expected to bring a similar reduction in both μ and μ_{nA}. Therefore, the derivative of R_A w.r.t N_{ot} and N_{it} can be calculated (with similar assumptions made for R_{CH}) as

$$\frac{\partial R_A}{\partial N_{ot}} = \frac{L_A}{2Z\mu_{na} C_{OX}(V_G - V_{TH})^2} \frac{\partial V_{TH}}{\partial N_{ot}} \quad < 0 \text{ , and} \tag{2.19}$$

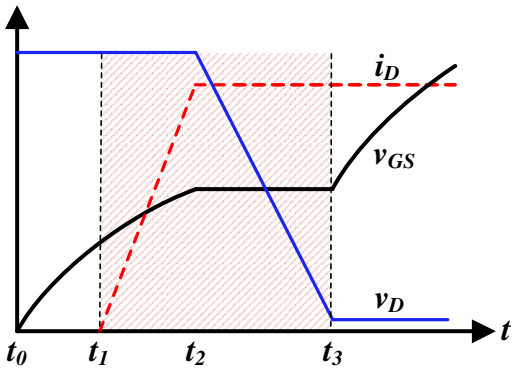
$$\frac{\partial R_A}{\partial N_{it}} = \frac{L_A}{2Z\mu_{na}{}^2 C_{OX}(V_G - V_{TH})^2}\left[\mu_{nA}\frac{\partial V_{TH}}{\partial N_{it}} - (V_G - V_{TH})\frac{\partial \mu_{nA}}{\partial N_{it}}\right] \quad > 0. \quad (2.20)$$

As seen from expression (2.17) and (2.19), the derivative of both R_{CH} and R_A w.r.t N_{OT} are negative, which indicates that R_{ON} decreases with increase of N_{ot}. Similarly, the derivative of both R_{CH} and R_A w.r.t N_{it} in equations (2.18) and (2.20) are positive, which indicates that R_{ON} increases with increase of N_{it}. This means that R_{ON} follows a dip-and-rebound variation pattern like V_{TH}, V_{GP} and t_{GP}.

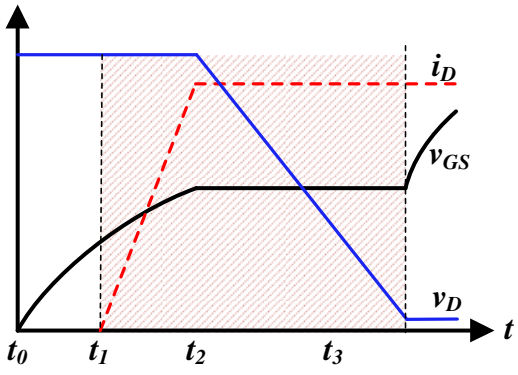
2.4 Significance of Dip-and-Rebound Variation Pattern

The dip-and-rebound variation of electrical parameters due to gate-oxide degradation can be detrimental to device performance, reliability and efficiency. The dip may cause the threshold voltage to shift to negative values (as shown in the experimental results in subsequent sections), which may cause a "normally OFF" (or enhancement type) MOSFET to become a "normally ON" (or depletion type) MOSFET, or may result in a MOSFET with high OFF-state leakage current [2], [36]. This is a very serious problem as it can lead to unintended operation of power-electronic devices. For example, let us consider a single phase-leg of a power inverter, where the top and bottom "normally OFF" MOSFETs are switched in a complimentary manner, so that, when one MOSFET is ON, the other is OFF. If the MOSFET, which is supposed to remain turned OFF while the other MOSFET is conducting, were to suddenly conduct as a result of transition from its "normally-OFF" state to a "normally ON" state, it would cause a shoot-through of the DC voltage source leading to a huge over-current and a catastrophic failure of this power inverter.

In a similar manner, the rebound causes simultaneous increase of R_{ON}, V_{GP}, and t_{GP}, which correspond to an increase in on-state loss, switching loss and switching time of the MOSFET, respectively. The maximum switching loss occurs during the crossover between the drain voltage, v_D and the drain current, i_D as shown by the hatched rectangular area in Figure 2.6(a). The increase in switching losses (due to increase of t_{GP}) can be visualized by the enlargement of cross-over area after the degradation, as shown by an enlarged and hatched rectangular area in Figure 2.6(b). Thus, the rebound effect slows down the power MOSFETs and makes them less efficient; this is contradictory to the desired performances of power MOSFETs. From the point of view of device



(a) Before degradation



(b) After degradation

Figure 2.4: Switching losses in Si MOSFETs before and after the degradation (during rebound).

manufacturers, the rebound effect might increase the values of electrical parameters of Si MOSFETs beyond their specifications.

2.5 Experiment Details

Experiments were performed on two different commercial power MOSFETs: IRF510 (100 V, 5.6 A) and IRF520 (100 V, 9.2 A) [40], [41] in order to validate the analysis made in previous section.

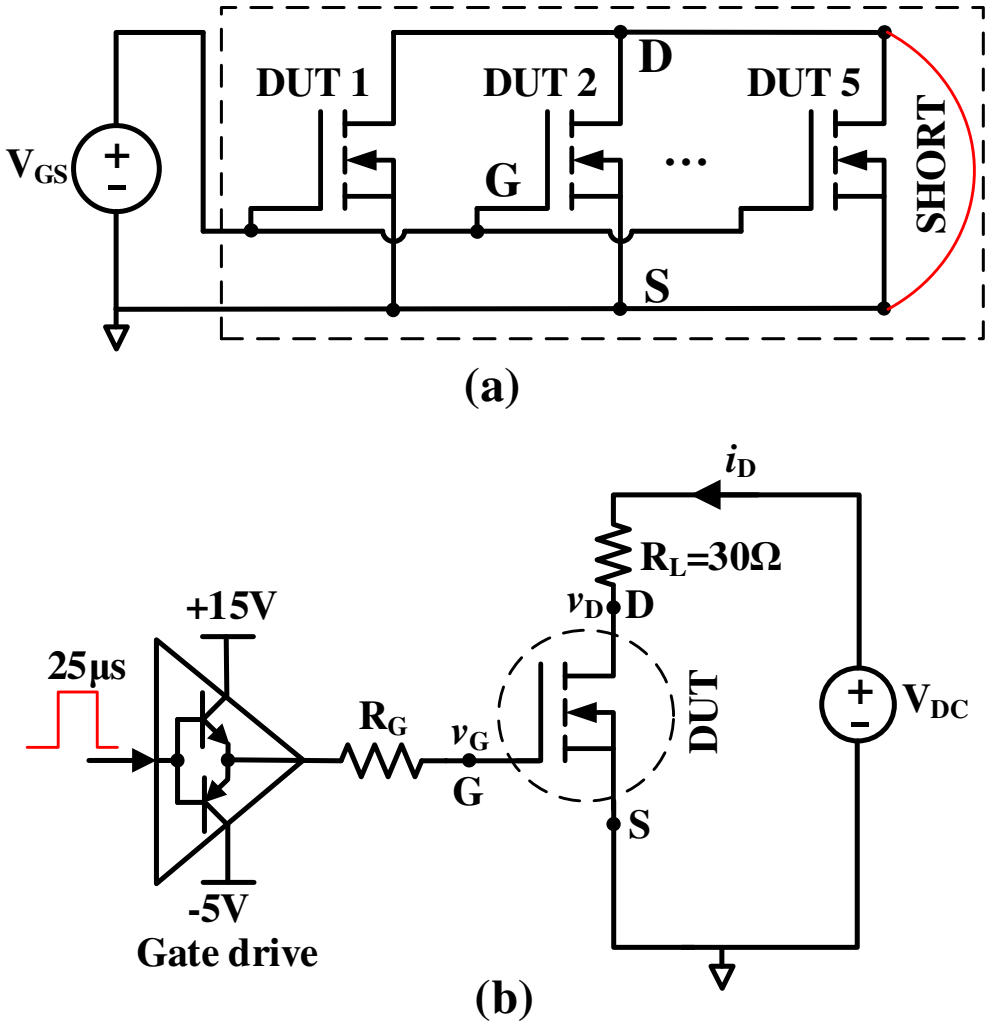


Figure 2.5: Circuit schematic for (a) HEF-stress platform, and (b) Switching-test platform.

2.5.1 Experimental setup

The experimental circuit schematic and overall setup are shown in Figure 2.7 and Figure 2.8 respectively. The setup mainly consists of a High Electric Field (HEF) stress platform [Figure 2.7(a)] to induce accelerated gate-oxide degradation of MOSFETs, a switching-test platform [Figure. 2.7(b)] to obtain the MOSFETs' turn-on waveform, and a B2912A device analyzer to obtain device characteristics.

A total of five MOSFETs [DUT 1 through DUT 5 in Figure 2.7(a)] were inserted into the sockets of the HEF-stress platform for accelerated aging. Electrical stressing was performed by applying positive bias to the gate electrode at ambient temperature (25 ^{O}C) with the drain and source terminals grounded. The gate voltage was chosen (fixed 65 V for both devices) such that it was

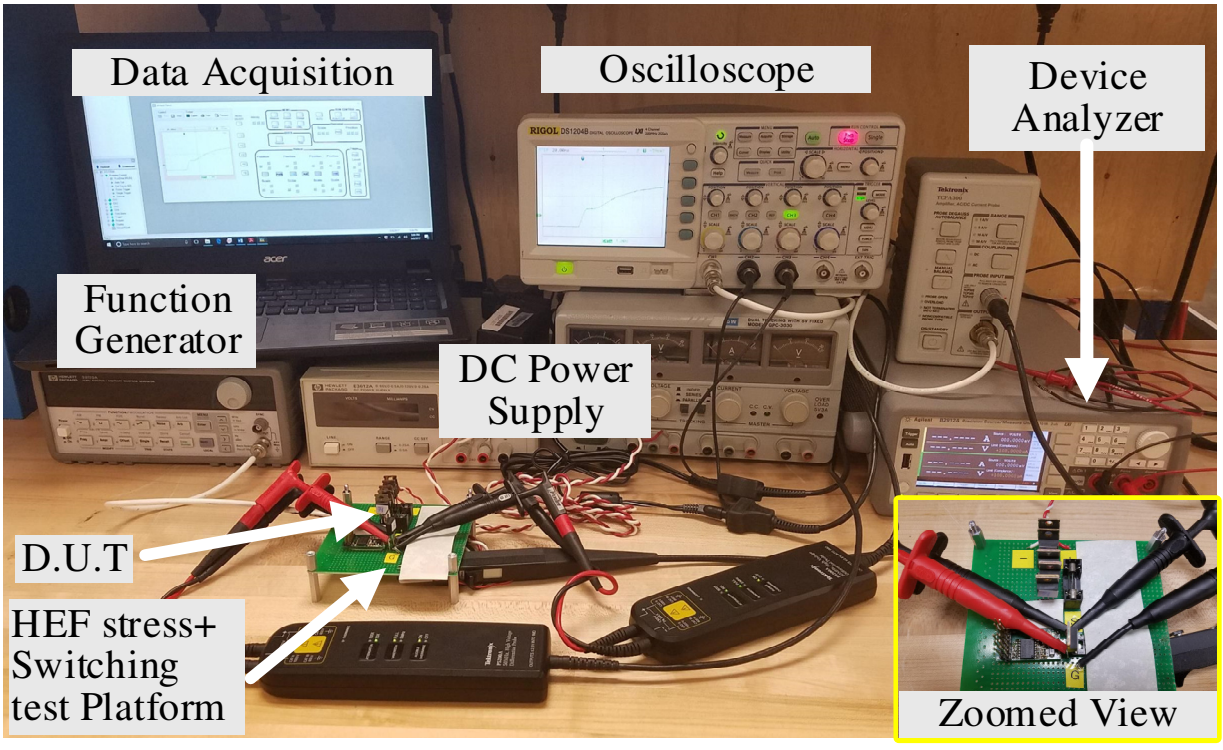


Figure 2.6. Experimental setup.

sufficient to initiate observable gate-oxide degradation, but low enough not to cause gate-oxide breakdown.

To obtain the turn-on waveforms, each MOSFET was driven by a gate driver with a gate bias voltage of -5V/+15 V [see Figure 2.7(b)]. Since, it is easier to observe switching characteristics with a larger gate resistance, an external 100 Ω resistance was inserted between the gate driver and the gate terminal of the MOSFET. To minimize self-heating of the MOSFET during the test, a single 25 μs pulse was provided to the gate driver. A DC voltage of 30 V and a load resistance (R_L) of 30 Ω were used to ensure a drain current of 1 A.

2.5.2 Experimental Procedure

The experimental process mainly comprises the following: 1) the application of HEF stress for accelerated aging of gate oxide, and 2) the measurement of precursors after the stress. The stress-and-measurement of precursors were carried out for variable times represented by the time set, t= {0,2,2,2,2,2,20,40,40,40} for 150 minutes. It is important to mention that a brief stress-and-measurement pattern of 2-minute interval during the initial stages of stress was necessary to observe the 'dip' effect of Q_{ot} on precursors.

Figure 2.9(a) shows the experimental process followed to determine V_{TH} and R_{ON} for the batch of five MOSFETs. The pulsed I_D-V_{GS} transfer characteristics and I_D-V_{DS} characteristics graphs were obtained using a B2912A device analyzer. The threshold voltage was determined from the pulsed I_D-V_{GS} characteristics using linear extrapolation method [42]–[44] , and the on-resistance was determined from the pulsed I_D-V_{DS} characteristics (@ I_D= 1A and V_G= 10 V). Then, the batch of five MOSFETs was transferred into the sockets of HEF-stress platform for accelerated aging for a specific duration listed in the time set above. Upon subsequent aging, the precursors were

measured again. This stress-and-measurement process was carried out for a total duration of 150 minutes.

Figure 2.9(b) shows the experimental process followed to obtain V_{GP} and t_{GP}. The individual MOSFETs were inserted into the socket of switching-test platform. The gate-plateau voltage and gate-plateau time were obtained from the turn-on waveform. Upon subsequent aging, these precursors were measured again. This stress-and-measurement process was carried out for a total duration of 150 minutes.

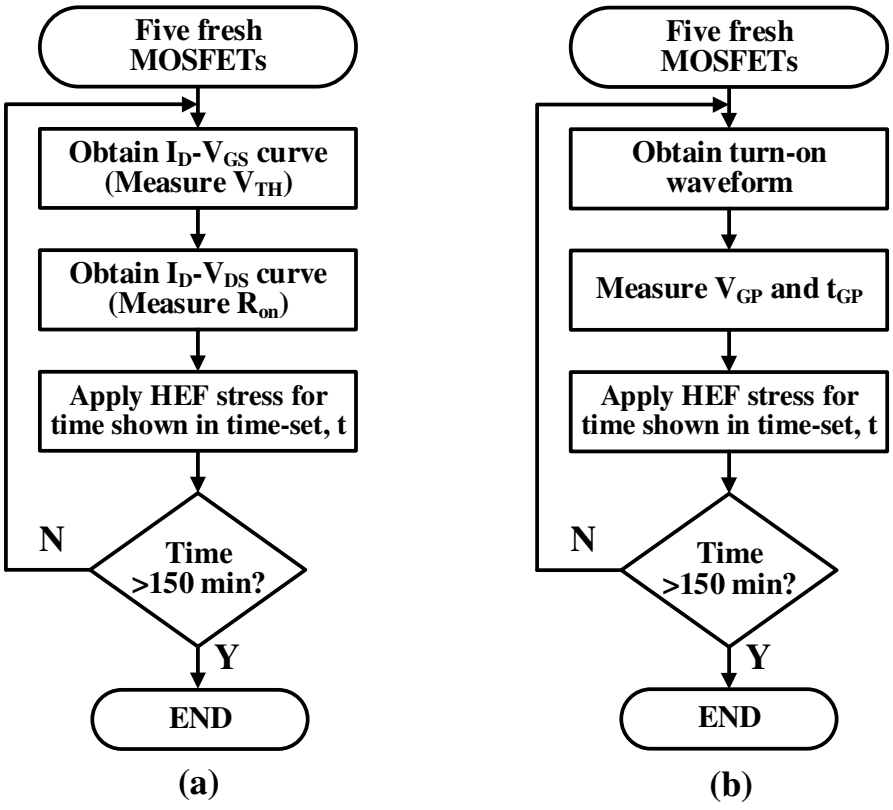


Figure 2.7: Experimental process flowchart for measurement of (a) V_{TH} and R_{ON}, and (b) V_{GP} and t_{GP}.

2.6 Results and Discussion

A total of 20 MOSFETs (ten of each MOSFET type) were tested to confirm the variation pattern of electrical parameters. The names of different samples followed the format: KP-510-xx for IRF510 sample group and KP-520-xx for IRF520 sample group, where xx denoted each sample's number. Figures 2.10 and 2.11 show the variation of precursors with HEF stress for all the samples, where the bottom horizontal axis corresponds to the order of measurement and the top horizontal axis corresponds to the specific time at which each measurement was taken. As aforementioned, an initial dip was predominantly due to a buildup of Q_{ot}, while the rebound in the later stages was predominantly due to an accumulation of Q_{it}.

2.6.1 Variation of Threshold Voltage

Figures 2.10(a) and 2.11(a) show the variation of V_{TH} that occurred in both the IRF510 (KP-510-11 through KP-510-15) and IRF520 (KP-520-51 through KP-520-55) samples when the samples were subjected to HEF stress. Fresh KP-510-xx and KP-520-xx samples had average initial positive V_{TH} of nearly +3.2 V and +3.1 V, respectively. During an initial four minutes of stress, V_{TH} decreased to negative values (nearly -3.1 V for KP-510-xx samples and -3.2 V for KP-520-xx samples). After the turn-around point, V_{TH} returned to and surpassed its initial positive value. The 'positive to negative to positive' transition of V_{TH} indicated 'normally OFF to normally ON to normally OFF' transitions in power MOSFETs over the course of gate-oxide degradation.

2.6.2 Variation of On-Resistance

Figures 2.10(b) and 2.11(b) show the variation of R_{ON} that occurred in both the IRF510 (KP-510-

11 through KP-510-15) and IRF520 (KP-520-51 through KP-520-55) samples. It was observed that R_{ON} decreased very slightly in the initial stage. However, it rebounded significantly in the later stages of degradation (exceeding 4 times for IRF510 samples and 6 times for IRF520 samples). Thus, it was observed that R_{ON} followed the dip-and-rebound variation pattern like V_{TH}.

2.6.3 Variation of Gate-plateau Voltage

Figures 2.10(c) and 2.11(c) show the variation of V_{GP} that occurred in both the IRF510 (KP-510-31 through KP-510-35) and IRF520 (KP-520-71 through KP-520-75) samples. It was observed that V_{GP} dipped and rebounded in a manner similar to V_{TH} and R_{ON}. Figure 2.12 shows gate voltage (V_G) waveforms for samples KP-510-31 and KP-520-74. The solid black arrows point to an initial V_{GP} decrease, which was followed by a V_{GP} increase during later stages. Tabulated V_{GP} values show that V_{GP} @ 150 min > V_{GP} @ 0 min (Fresh MOSFET) > V_{GP} @ 6 min for KP-510-31 sample (or V_{GP} @ 4 min for KP-520-74 sample).

2.6.4 Variation of Gate-plateau Time

Figures 2.10(d) and 2.11(d) show the variation of t_{GP} that occurred in both the IRF510 (KP-510-31 through KP-510-35) and IRF520 (KP-520-71 through KP-520-75) samples. It was observed that t_{GP} dipped and rebounded in a manner similar to other precursors: V_{TH}, R_{ON}, and V_{GP}. Such a variation can also be observed in the waveform in Figure 2.12, in which dotted black lines show t_{GP} at different stress times. Tabulated t_{GP} values show that t_{GP} @ 150 min > t_{GP} @ 0 min (Fresh MOSFET) > t_{GP} @ 6 min for KP-510-31 sample (or t_{GP} @ 4 min for KP-520-74 sample).

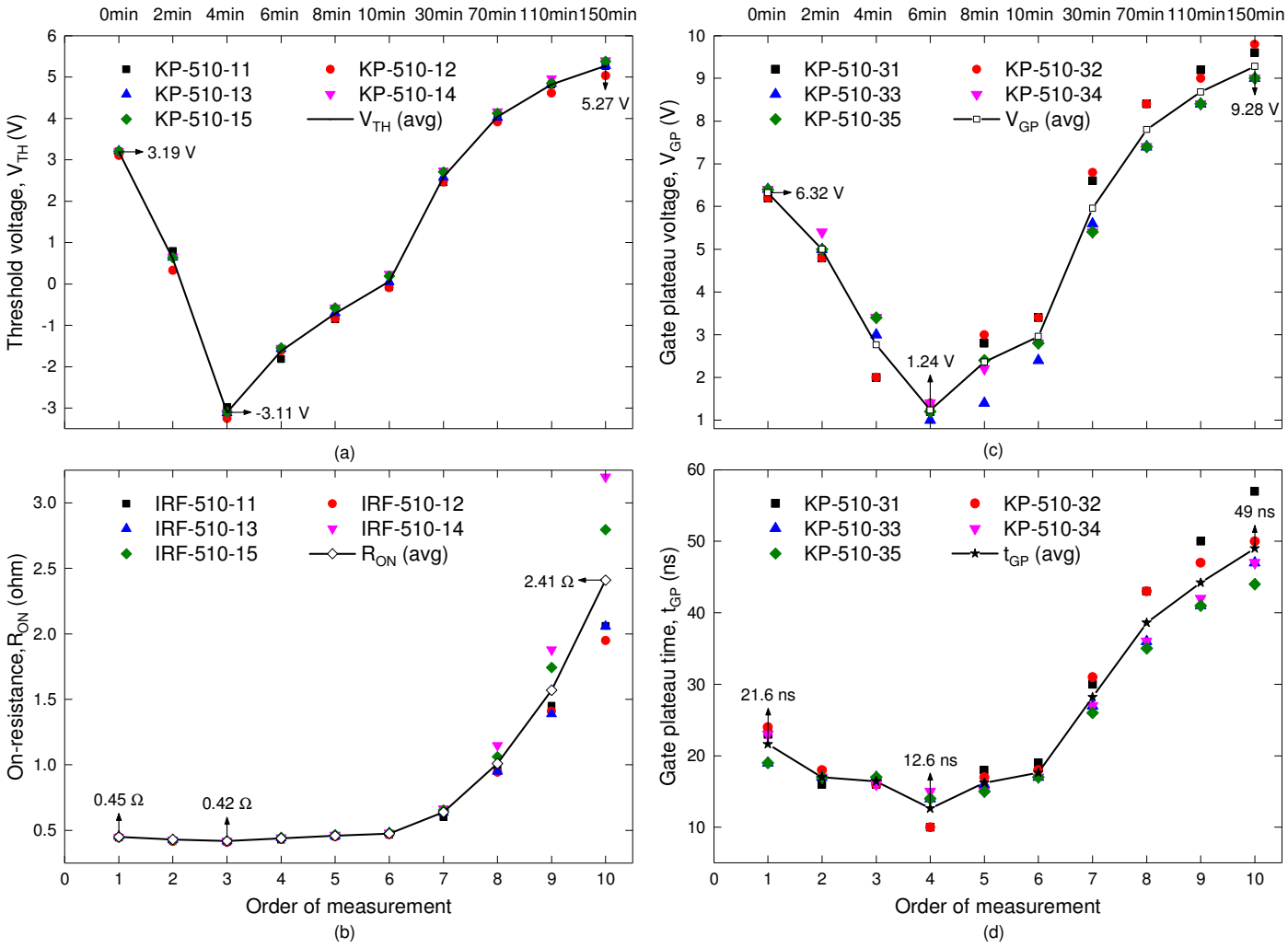


Figure 2.8: Variations of: a) Threshold voltage, b) On-resistance c) Gate-plateau voltage, and d) Gate-plateau time, for five samples of IRF510 over time.

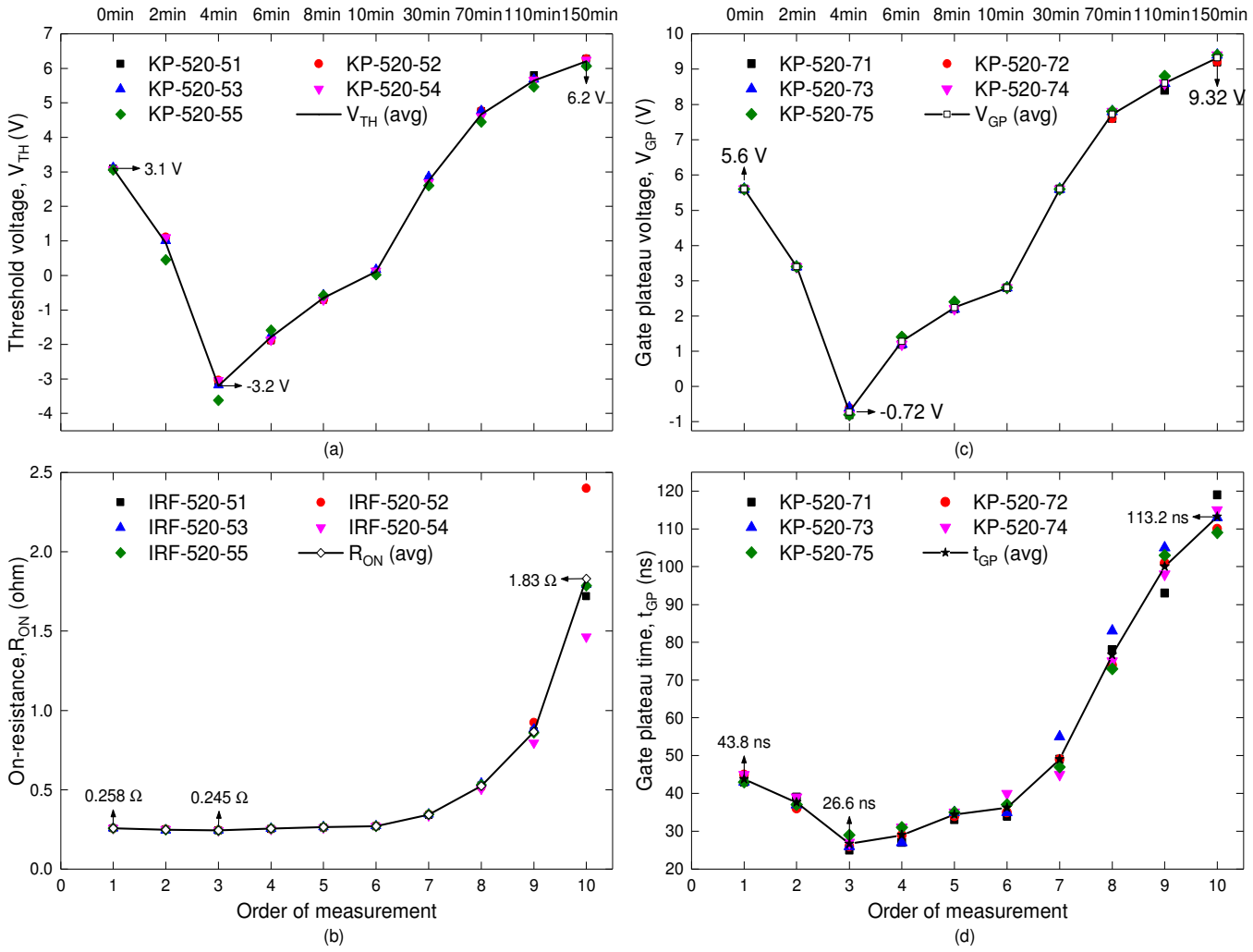
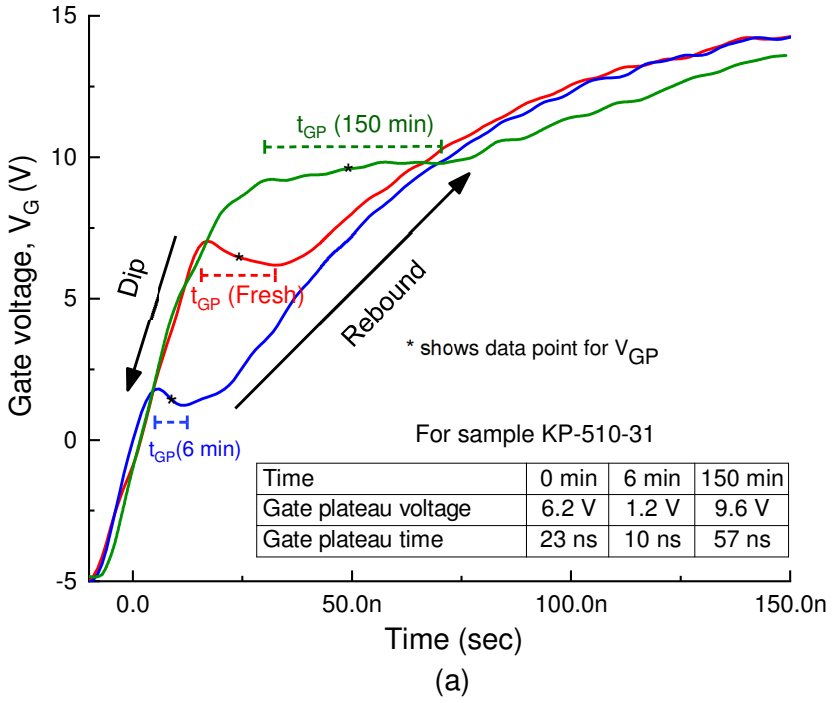


Figure 2.9: Variations of: a) Threshold voltage, b) On-resistance c) Gate-plateau voltage, and d) Gate-plateau time, for five samples of IRF520 over time.



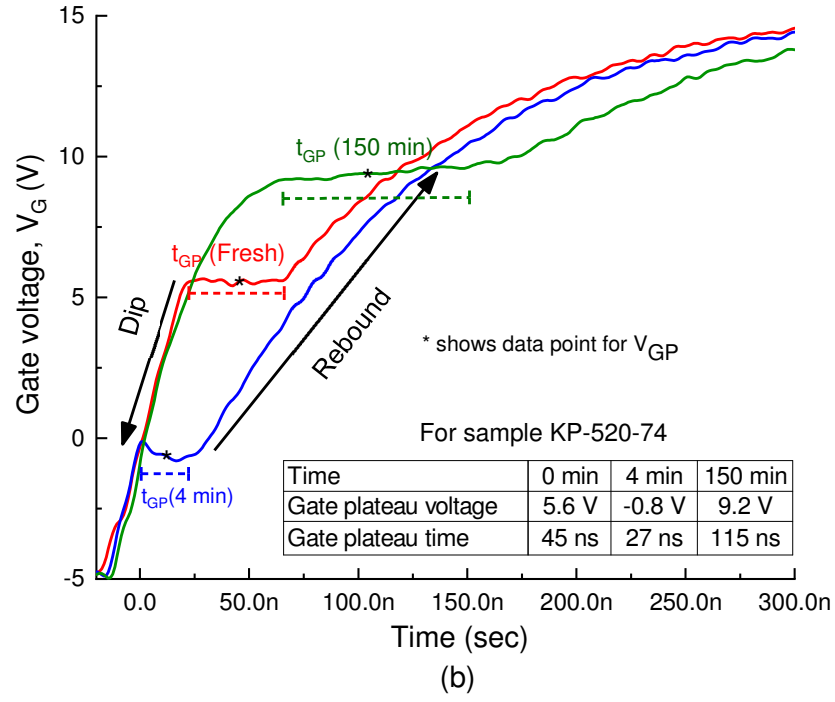


Figure 2.10: Variations of V_{GP} and t_{GP} shown in gate voltage waveform of (a) sample KP-510-31, and (b) sample KP-520-74.

2.6.5 Precursor Comparison

The experiment's results confirmed that all four precursors reflected the gate-oxide degradation status with simultaneous negative and positive shifts from their initial values. The shift tendency of each precursor was different; the average shifts from the respective initial values of the precursors in both sample groups are provided in Table 2.1. The percentage shifts were computed for a stress period of 150 min. For longer stress periods, the percentage positive shifts can be expected to increase. Three observations were noted:

1) In both sample groups, V_{TH} had the highest negative shift at nearly 200% each, while R_{ON} exhibited the least negative shifts at 7% and 5% for the IRF510 and IRF520 samples, respectively. In addition, for both groups, V_{GP} had a higher negative shift than t_{GP}.

2) In both sample groups, R_{ON} had the highest positive shift at nearly 440 and 610% for IRF510 and IRF520 samples, respectively. Moreover, t_{GP} had the highest positive shift (nearly 130% for IRF510 samples and 160% for IRF520 samples) compared to V_{TH} (nearly 65% for IRF510 samples and 100% for IRF520 samples) and V_{GP} (nearly 50% in IRF510 samples and 70% in IRF520 samples). Although it was found that the offline precursor R_{ON} had a maximum positive shift, the

Table 2.1: Percentage shift of precursors in Si MOSFETs.

Precursors	IRF510 samples		IRF520 samples	
	% negative shift	% positive shift	% negative shift	% positive shift
Threshold voltage	200%	65%	200%	100%
On-resistance	7%	440%	5%	610%
Gate-plateau voltage	80%	50%	115%	70%
Gate-plateau time	40%	130%	40%	160%

online precursors (V_{TH}, V_{GP} and t_{GP}) have an additional advantage over R_{ON} (offline precursor) in that they can be extracted without affecting a system's operation.

3) The threshold voltage was the most suitable precursor for observing the negative shift while R_{ON} and t_{GP} were more suitable precursors for observing the positive shift.

2.7 Conclusion

In this chapter, the effect of gate-oxide degradation on four electrical parameters of Si MOSFETs were examined qualitatively and quantitatively. It was demonstrated that the electrical parameters of Si MOSFETs vary with a dip-and-rebound pattern over the course of gate-oxide degradation. The pattern, which results from the presence of oxide-trapped charges and interface-trapped charges, was confirmed by inducing gate-oxide degradation in two different commercial power MOSFETs. The results of all samples were very consistent and repeatable. Furthermore, shift tendencies, which occurred throughout gate-oxide degradation in the online and offline precursors: V_{TH}, $V_{GP,}$ R_{ON} and t_{GP}, were compared. The new online precursor t_{GP} was found to be a competitive precursor of gate-oxide degradation, as it had a higher positive shift than the other online precursors (V_{TH} and V_{GP}). Additionally, V_{TH} was found to be the most sensitive precursor for observing the negative shift, while R_{ON} and t_{GP} were found to be the most sensitive precursors for observing the positive shift.

Chapter 3

Effect of Gate-Oxide Degradation on Electrical Parameters of Silicon Carbide Power MOSFETS

3.1 Introduction

Gate-oxide degradation significantly alters the electrical parameters of power MOSFETs over time. Several electrical parameters have been identified as precursors for monitoring the gate-oxide degradation process in Si MOSFETs. The threshold voltage (V_{TH}) has been identified as the most common precursor for Si MOSFETs [6], [31], [45] . Very recent literature have also reported the gate-plateau (or miller) voltage (V_{GP}) [31] and the gate-plateau time (t_{GP}) [45] as new online precursors of gate-oxide degradation in Si MOSFETs. On the other hand, only the threshold voltage [19], [20], [46], [47] and the gate leakage current [48] have been reported as precursors of gate-oxide degradation in SiC MOSFETs. The Si and SiC MOSFETs might be different in terms of their substrate material, device characteristics and switching performances, but both belong to the same MOSFET family and have the same electrical parameter definitions. Following this reasoning, it is demonstrated in this chapter that the three precursors used for monitoring the gate-oxide degradation process in Si MOSFETs: V_{TH}, V_{GP} and t_{GP}, can also be extended to SiC MOSFETs. The extraction of these three precursors can all be done from the same turn-on

waveform of power MOSFET as shown in Figure 2.1. As these precursors enable monitoring of electrical parameters without physical removal of devices from operating power-electronic systems, they are very suitable for online monitoring of gate-oxide degradation process in practical applications.

Though the gate-oxide material is same in both Si and SiC MOSFETs, the effect of gate-oxide degradation on electrical parameters are different. In Si MOSFETs, the positively charged oxide-trapped charges (Q_{ot}) have been found to accumulate within the gate oxide during the initial stages of degradation while the negatively charged interface-trapped charges (Q_{it}) have been found to form predominantly at the oxide-silicon interface during the later stages of degradation [6], [45] [as discussed in previous chapter]. The accumulation of positive Q_{ot} increases the effective electric field across the gate oxide, which contributes to channel inversion and leads to a simultaneous decrease (or dip) of all three precursors in Si MOSFETs initially. On the other hand, the accumulation of negative Q_{it} at the Si-SiO2 interface compensates the effect of oxide field, which leads to a simultaneous increase (or rebound) of all three precursors in Si MOSFETs in the later stages of degradation. Thus, all three precursors: V_{TH}, V_{GP} and t_{GP}, exhibit a dip-and-rebound variation pattern in Si MOSFETs, as shown in Figure 2.2 [45]. The degradation trend of precursors in Si MOSFETs can be observed in gate-source voltage waveform during turn-on, as shown in Figure 2.3, where V_{GP2} (rebound) > V_{GP0} (fresh MOSFET) > V_{GP1} (dip), and t_{GP2} (rebound) > t_{GP0} (fresh MOSFET) > t_{GP1} (dip).

In SiC MOSFETs, the parameter shift due to gate-oxide degradation has been attributed to the direct tunneling of channel electrons into pre-existing oxide traps near the SiC-SiO_2 interface (also called near-interfacial oxide traps) [18], [19], [49]. The accumulation of electrons (or negative charges) in near-interface oxide traps decreases the effective electric field across the gate oxide,

thereby making it more difficult to form the inversion channel. As a result, upon positive gate bias stress, the electrical parameters in SiC MOSFETs do not exhibit the dip-and-rebound pattern but only increase with stress time (the details of which are discussed in subsequent sections). Furthermore, the tunneling mechanism causes the charge states in oxide traps to increase in a linear-with-log-stress-time manner [18], [19]. This linear-with-log-stress-time increase in density of charge states causes the electrical parameters of SiC MOSFETs to increase in a similar manner. Under the presence of gate-bias stress, the threshold voltage in SiC MOSFETs has been found to increase linearly with logarithm of stress-time [18], [19]. In this chapter, it is demonstrated analytically and experimentally that the other precursors: V_{GP} and t_{GP}, also exhibit a similar linear-with-log-stress-time response, as shown in Figure 3.1. The expected increasing trend of precursors can be observed in gate-source voltage waveform during turn-on of SiC MOSFETs, as shown in Figure 3.2 , where V_{GP0} (at initial transition tunneling time, $t = t_o$) < V_{GP1} (after time, $t = 10t_o$) < V_{GP2} (after time, $t = 100t_o$), and t_{GP0} (at initial tunneling transition time, $t = t_o$) < t_{GP1} (after time, $t = 10t_o$) < t_{GP2} (after time, $t = 100t_o$).

The purpose of this chapter is three-fold: 1) To demonstrate that the three gate-oxide degradation precursors used in Si MOSFETs: V_{TH}, V_{GP} and t_{GP}, can also be used in SiC MOSFETS; 2) To demonstrate that all three precursors increase in a linear-with-log-stress-time manner over the course of gate-oxide degradation in both planar and trench-gate SiC MOSETs; and 3) To compare the positive shift tendencies of each precursor and determine the most sensitive indicator of gate-oxide degradation. It is shown that all three precursors reflect the gate-oxide degradation status with simultaneous positive shift from their initial values.

The chapter is organized as follows. Section 3.2 provides background information about gate-oxide degradation mechanism and associated parameter shift in SiC MOSFETs. Section 3.3

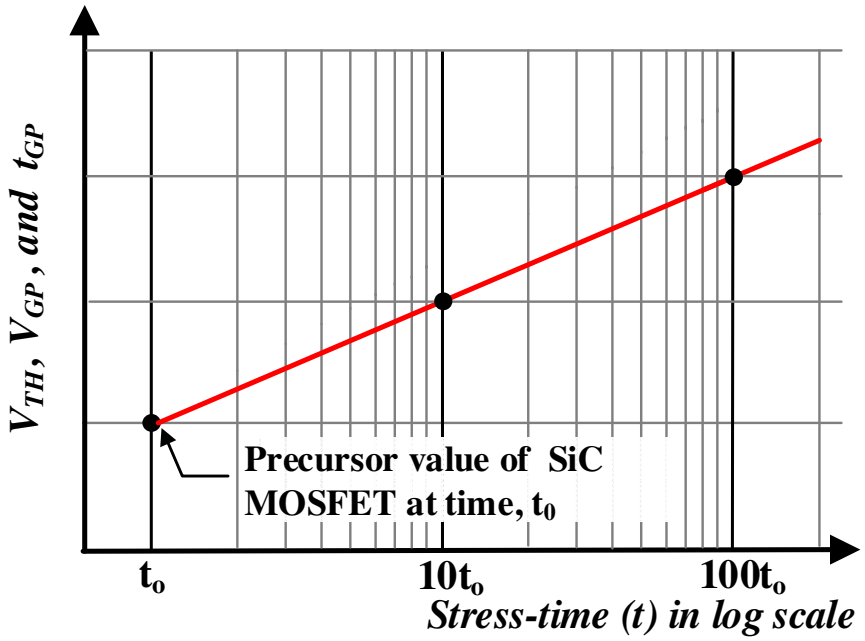


Figure 3.1: Expected Linear-with-log-stress-time variation pattern of electrical parameters during gate-oxide degradation in SiC MOSFETs.

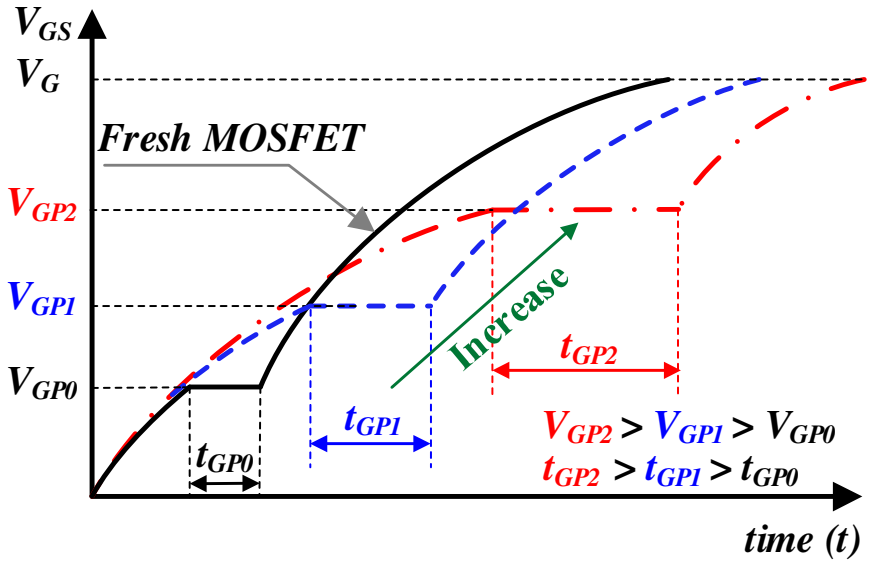


Figure 3.2: Expected degradation trend of precursors as shown in gate-source voltage waveform during turn-on of SiC MOSFETs.

provides analytical expressions demonstrating the linear-with-log-stress-time response of all three precursors. The subsequent sections provide experimental verification of the linear-with-log-stress time responses of precursors in two different types of commercial SiC MOSFETs (650 V, 70 A trench-gate SiC MOSFETs and 1200 V, 19 A planar SiC MOSFETs) under high temperatures of 150 °C and 125 °C, respectively.

3.2 Background

The two common device structures adopted in the fabrication of commercial SiC MOSFETs are: a) planar structure, and b) trench-gate structure. Their respective simplified structures are shown in Figure 3.3. The gate-oxide layer (SiO_2) between the gate terminal and the semiconductor surface in both structures is shown within dashed rectangles.

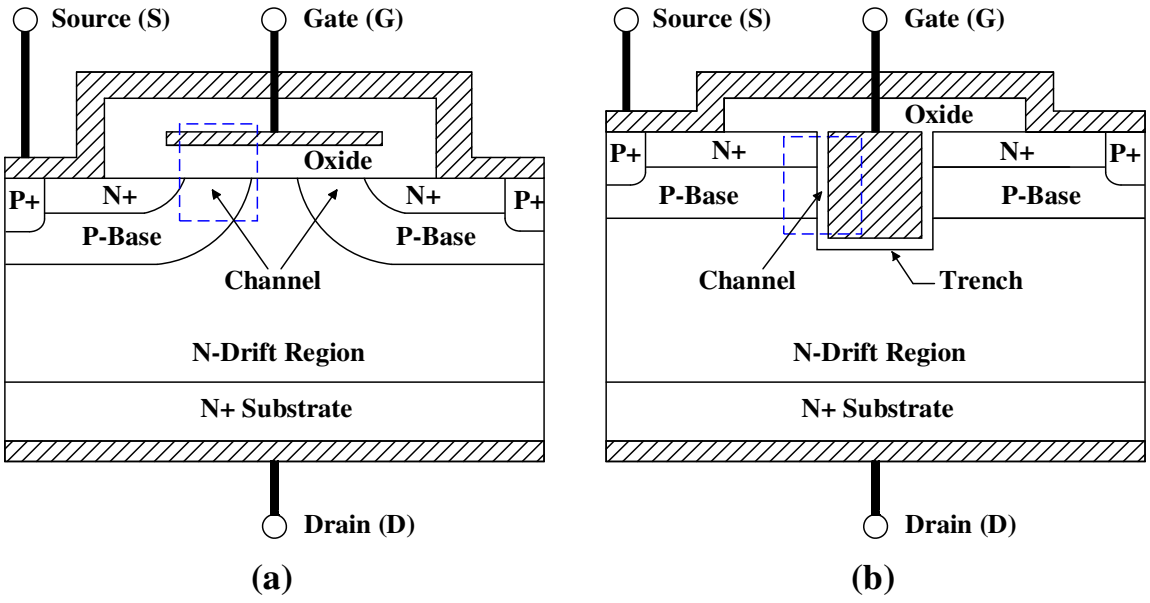


Figure 3.3: Simplified device structure of (a) Planar, and (b) Trench-gate SiC MOSFET.

3.2.1 Gate-Oxide Degradation Mechanism in SiC MOSFETs

The number of oxygen vacancy related defects in SiO_2 is much larger in SiC-SiO_2 structure than in Si-SiO_2 structure [15]–[17]. As these defects are located near SiC-SiO_2 interface in the oxide, they are referred to as the near-interfacial oxide traps (NIOTs) [18]–[21]. The NIOTs are represented as defect energy bands (E_T) near the conduction band edge of SiC, as sketched in Figure 3.4(a) with dashed lines. The gate-oxide degradation in SiC MOSFET has been attributed to charging of these oxide traps via a direct tunneling mechanism [16], [18], [19], [21].

The electron trapping mechanism in NIOTs is explained with the help of energy band diagram. When a positive bias is applied to turn on the MOSFET, the applied electric field causes the fermi level to bend near the SiO_2-SiC barrier. This causes the surface to invert and, as a result, a large

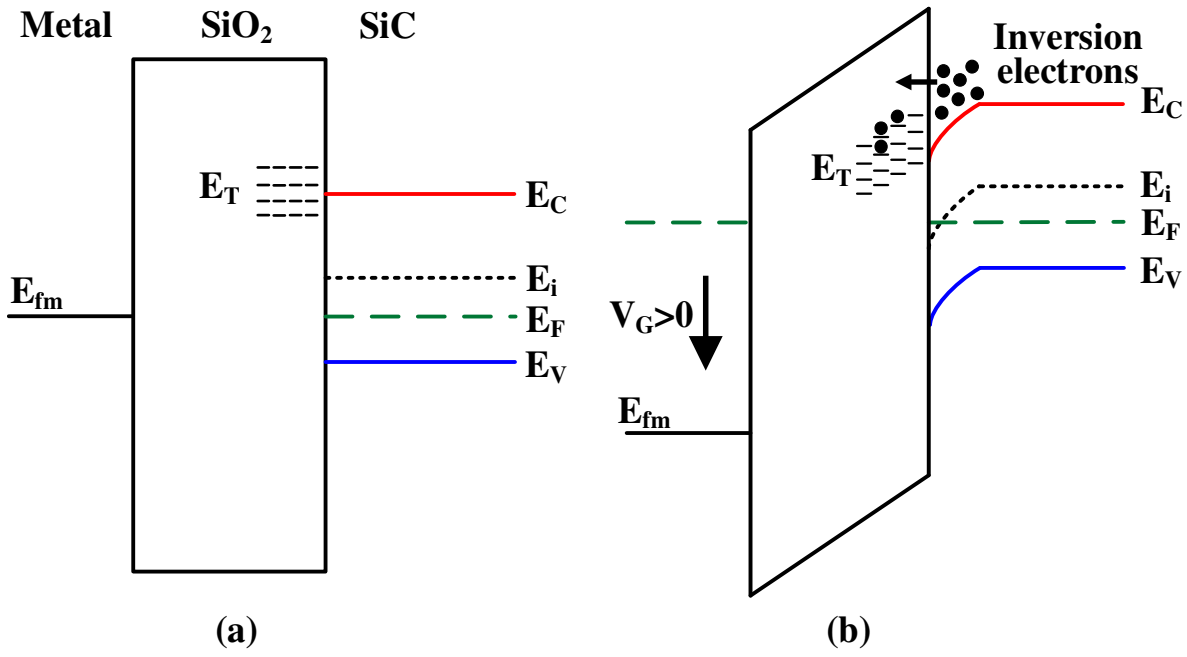


Figure 3.4: Energy band diagram of a SiC/SiO2 structure (a) with a defect energy band, and (b) with electron tunneling into oxide traps under positive gate bias.

number of electrons accumulate near the conduction band edge of SiC. These electrons, which are in excited state, can then tunnel into the defect energy bands (which are lower in energy level compared to the conduction band edge of SiC) and occupy the oxide traps as shown in Figure 3.4(b). The number of electrons tunneling into NIOTs depends upon the duration and magnitude of positive stress; a longer stress duration (or a higher gate bias) causes more electrons to penetrate deeper into the oxide [18], [49]. The electrons that become trapped in oxide traps opposes the effect of applied oxide field. As a result, a higher electric field is required across the oxide for channel inversion and leads to an increase of threshold voltage in SiC MOSFET [18], [19]. It is important to note that both V_{GP} and t_{GP} bear a strong analytical relationship with V_{TH}. Therefore, it is expected that these other precursors will also exhibit a similar increase over the course of degradation.

3.2.2 Linear-with-Log-Time Response of Precursors

During direct tunneling, the electrons flow into the gate oxide in the form of a tunneling front (or wave) at a linear-with-log-time rate [18]–[20]. In other words, in the presence of an electric field, the electrons flow linearly with logarithm of time into the oxide and become trapped in the NIOTs. Based on the direct tunneling model of charge transfer into MOS devices, if N is the arbitrary distribution of oxide traps (or oxide trap density), the total charge transferred into these traps [after applying bias-stress for a time (t) follow a logarithmic time dependence, as given by [50], [51]

$$Q_{NIOT}(t) \cong \frac{eN}{2\beta}\left[\ln\frac{t}{t_0}+\gamma\right], \tag{3.1}$$

where e is the electronic charge, t_o is the initial tunneling transition time (around 0.1 ps), β is the tunneling parameter related to barrier height facing the tunneling electrons, and $\gamma \cong 0.577$ is the Euler's constant. It can be seen from equation (3.1) that the charge states in oxide traps increase in a linear manner with respect to the logarithm of stress-time. This linear-with-log-time change in charge states causes the electrical parameters of MOSFETs to increase in a similar manner. Under the presence of gate-bias stress, the threshold voltage has been found to increase linearly with the log of stress-time in SiC MOSFETs [18]. In this chapter, it is demonstrated that the other precursors: V_{GP} and t_{GP}, also exhibit a similar response.

In order to observe this response, the electrical parameters are plotted on a logarithmic time scale instead of a linear time scale, as shown in Figure 3.1. It is important to note that the increasing trend of precursors in SiC MOSFETs can be observed in a linear time scale as well. However, the increasing trend, by itself, does not provide a meaningful relationship between the parameter shift and the stress-time. On the other hand, the parameter shifts (ΔP), when plotted in a logarithmic time scale, exhibit a linear relationship with the logarithm of stress-time (t) in the form: $\Delta P = k \ln(t/t_o)$, where k is a constant dependent upon manufacturing parameters. This is meaningful because: i) it confirms direct tunneling is the responsible mechanism for parameter shifts observed in SiC MOSFETs, and (ii) it helps to develop a precise gate-oxide degradation model for SiC MOSFETs. Such a model can be extended to predicting the degradation state and forecasting the remaining useful life of gate-oxide.

The increasing trend of precursors is important for SiC MOSFETs. This trend, when plotted in a logarithmic time scale, exhibit a linear relationship with the logarithm of stress-time. This is meaningful because: i) it confirms direct tunneling is the responsible mechanism for parameter shifts observed in SiC MOSFETs [18], [51] , and (ii) it helps to develop a precise gate-oxide

degradation model for SiC MOSFETs. Such a model can be extended to predicting the degradation state and forecasting the remaining useful life of gate-oxide. In addition, the increasing trend of electrical parameters over the course of gate-oxide degradation can be detrimental to device performance, reliability and efficiency. The degradation causes a simultaneous increase of V_{TH}, V_{GP} and t_{GP}, which correspond to an increase in conduction loss, switching loss and switching time of the MOSFET, respectively. A holistic approach inclusive of the variation of all three precursors is, therefore, necessary to understand the overall detrimental effects of gate-oxide degradation in SiC MOSFETs.

3.2.3 Super-Linear Response of Precursors at High Temperature

The reliability of gate dielectric at high temperature is an important concern for SiC MOSFETs as they are intended to operate under this condition. The direct tunneling mechanism is a function of the stress bias and the stress time, but it is not very sensitive to the temperature [16], [21], [46]. However, in the older generation of SiC MOSFETs, the threshold voltage was found to increase significantly in a super-linear manner at higher temperatures (deviating from the expected linear-with-log-stress-time response) [16], [46]. This was attributed to a large number of additional oxide-traps activated at higher temperatures, which would then participate in the direct tunneling mechanism causing a super-linear increase of electrical parameters. As the super-linear increase of precursors could pose a substantial reliability issues for SiC MOSFETs, it was necessary to conduct gate-oxide degradation tests at high temperature to verify if the latest commercial SiC MOSFETs exhibited a similar dramatic increase of precursors. It is important to highlight that no super-linear increase of precursors was observed during our experiments, indicating that the newer gate oxides were more robust against additional oxide-trap activation at elevated temperature. This

is consistent with the observations reported in [46], where the newer devices exhibited a very small oxide-trap activation during elevated temperature. This can be attributed to improvements in the quality of gate-oxide layer in the latest commercial SiC devices.

3.3 Investigation of Variation of Precursors

In this section, the analytical expressions are derived to demonstrate the linear-with-log-stress-time response of precursors during gate-oxide degradation in SiC MOSFETs. It is worth mentioning that the derivations do not have temperature terms because the direct tunneling mechanism is not very sensitive to the temperature [16], [46].

3.3.1 Variation of Threshold Voltage

The gate voltage at which the MOSFET begins to conduct the drain current is referred to as the threshold voltage (occurs at time t_1 as shown in Figure 2.1). The effect of charge-trapping mechanism on threshold-voltage shift is given by the following relationship [18]

$$V_{TH} = V_{TH0} + \frac{Q_{NIOT}(t)}{C_{ox}}, \tag{3.2}$$

where V_{TH0} is the initial value of threshold voltage, $Q_{NIOT}(t)$ is the total charge transferred into the oxide traps after a stress-time (t), and C_{ox} is the specific gate-oxide capacitance.

Upon substituting $Q_{NIOT}(t)$ from equation (3.1) in equation (3.2),

$$V_{TH} \cong V_{TH0} + \frac{eN}{2\beta C_{ox}}\left[\ln\frac{t}{t_0} + \gamma\right]. \tag{3.3}$$

The slope of V_{TH} in logarithmic time axis is given by the partial derivative of V_{TH} in equation (3.3) with respect to (w.r.t) logarithm (log) of stress-time as

$$\frac{\partial V_{TH}}{\partial \ln t} = \frac{eN}{2\beta C_{ox}} \quad > 0. \tag{3.4}$$

Since the slope of V_{TH} w.r.t log of time is a positive constant value, the threshold voltage represents an increasing linear function w.r.t log of stress-time (or time).

3.3.2 Variation of Gate-Plateau Voltage

The constant gate voltage during the time span (t_3-t_2), as shown in Fig 2.1, is referred to as the gate-plateau voltage (or miller voltage), and is given by [39]

$$V_{GP} = V_{TH} + \sqrt{\frac{I_D L_{CH}}{\mu C_{ox} Z}} \ . \tag{3.5}$$

where I_D is the drain current, L_{CH} is the channel length, Z is the channel width, μ is the channel carrier mobility, and C_{ox} is the specific gate-oxide capacitance of MOSFET.

The partial derivative of V_{GP} w.r.t log of time results in

$$\frac{\partial V_{GP}}{\partial \ln t} = \frac{\partial V_{TH}}{\partial \ln t} - \frac{1}{2\mu^{3/2}} \sqrt{\frac{I_D L_{CH}}{C_{ox} Z}} \frac{\partial \mu}{\partial \ln t} \quad > 0. \tag{3.6}$$

The electron trapping in oxide traps reduces channel mobility (μ) by coulombic scattering of the charge carriers in channel [18]. In other words, the effective mobility is a decreasing function of time and can be written as

$$\frac{\partial \mu}{\partial \ln t} < 0. \tag{3.7}$$

Since V_{TH} increases with log of time in equation (3.4) and μ decreases with log of time in equation (3.7), the partial derivative of V_{GP} w.r.t log of time in equation (3.6) is positive, meaning that V_{GP} also increases with log of time. Furthermore, the contribution of the second term of (3.6) to the overall V_{GP} shift can be considered negligible (readers interested can refer to the Appendix for detailed discussion on this), in which case, the slope of V_{GP} w.r.t log of time in equation (3.6) simplifies to

$$\frac{\partial V_{GP}}{\partial \ln t} \simeq \frac{\partial V_{TH}}{\partial \ln t}. \tag{3.8}$$

It can be seen from above expression that the partial derivative of V_{GP} and V_{TH} (w.r.t log of time) are approximately equal. Since the slope of V_{TH} is a constant positive value, it follows that the slope of V_{GP} is also a constant positive value. Thus, the gate-plateau voltage is also an increasing linear function with log of time similar to V_{TH}.

3.3.3 Variation of Gate-Plateau Time

The gate-plateau time is the time span (t_3-t_2) where the gate voltage remains constant and equal to V_{GP}, as shown in Figure 2.1. Alternatively, this is also the time span where the drain voltage gradually decreases during the turn-on process of MOSFET.

The gate-plateau time of a power MOSFET is given by [45]

$$t_{GP} = t_3 - t_2 = R_G C_{GD,av} \frac{V_{DS}}{V_G - V_{GP}} \ , \tag{3.9}$$

where R_G is the gate resistance, V_G is the gate voltage and $C_{GD,av}$ is an assumed average value of gate-drain capacitance during the transient.

The partial derivative of t_{GP} w.r.t. log of time results in

$$\frac{\partial t_{GP}}{\partial \ln t} = R_G C_{GD,av} \ \frac{V_{DS}}{(V_G - V_{GP})^2} \ \frac{\partial V_{GP}}{\partial \ln t} \quad > 0 \ . \tag{3.10}$$

Since the slope of V_{GP} w.r.t log of time in equation (3.6) is a positive constant value and the other parameters in equation (3.10) are also constant terms, the slope of t_{GP} w.r.t log of time in equation (3.10) is also a positive constant value. This indicates that t_{GP} represents an increasing linear function w.r.t log of stress-time, similar to V_{TH} and V_{GP}.

3.4 Preliminary Low voltage, Room temperature Experiments

The preliminary experiments were performed to verify the increasing trend of precursors on a commercial 1200 V/ 36 A planar SiC MOSFET at low voltage, room temperature, resistive load, and low current condition [52].

3.4.1 Preliminary Experiment Details

The experimental setup mainly consists of a High Electric Field (HEF) stress platform [Figure 3.5(a)] to induce accelerated gate-oxide degradation in SiC MOSFETs and a switching-test

platform [Figure 3.5(b)] to obtain the turn-on waveform of SiC MOSFETs.

The accelerated aging of gate oxide was induced by applying positive bias to the gate electrode at room temperature, with the drain and source terminals grounded. A safe stress level of +45 V was chosen such that it was sufficient to initiate observable gate-oxide degradation, but low enough not to cause gate-oxide breakdown during the experiment.

To obtain the turn-on waveform, each MOSFET was driven by a gate driver with a gate bias voltage of 0 V/+15 V [see Figure 3.5(b)]. A gate voltage of 0 V (instead of a negative gate voltage) was used to prevent the oxide traps from discharging the trapped electrons during the off-state. This enabled to observe the full extent of gate-oxide degradation. Since, it is easier to observe

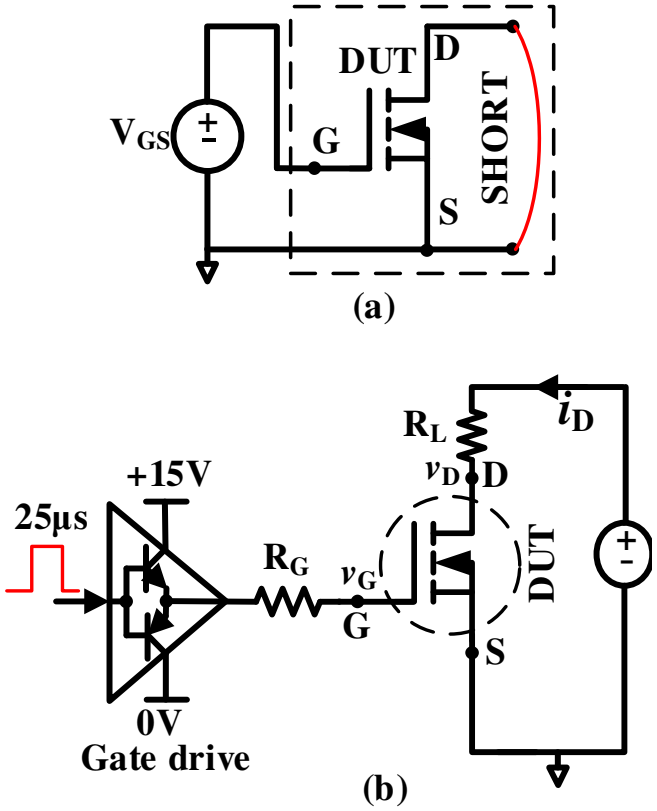


Figure 3.5: Circuit schematic for (a) HEF-stress platform, and (b) Switching-test platform.

switching characteristics with a larger gate resistance, an external 100 Ω resistance was inserted between the gate driver and the gate terminal of the MOSFET. To minimize self-heating of the MOSFET during the test, a single 25 µs pulse was provided to the gate driver. A DC voltage of 30 V and a load resistance (R_L) of 30 Ω were used to ensure a drain current of 1 A.

3.4.2 Preliminary Results

Figure 3.6 shows gate voltage (V_G) waveforms for a 1200 V, 36 A commercial SiC MOSFET sample. It is seen that both V_{GP} and t_{GP} increase over the duration of stress. The solid black arrow indicates an increasing trend of V_{GP} with degradation. Tabulated V_{GP} values show that V_{GP} @ 180 min > V_{GP} @ 120 min > V_{GP} @ 0 min (Fresh MOSFET). Similarly, the dotted black lines show t_{GP} during different stress times. Tabulated t_{GP} values show that t_{GP} @ 180 min > t_{GP} @ 120 min > t_{GP}

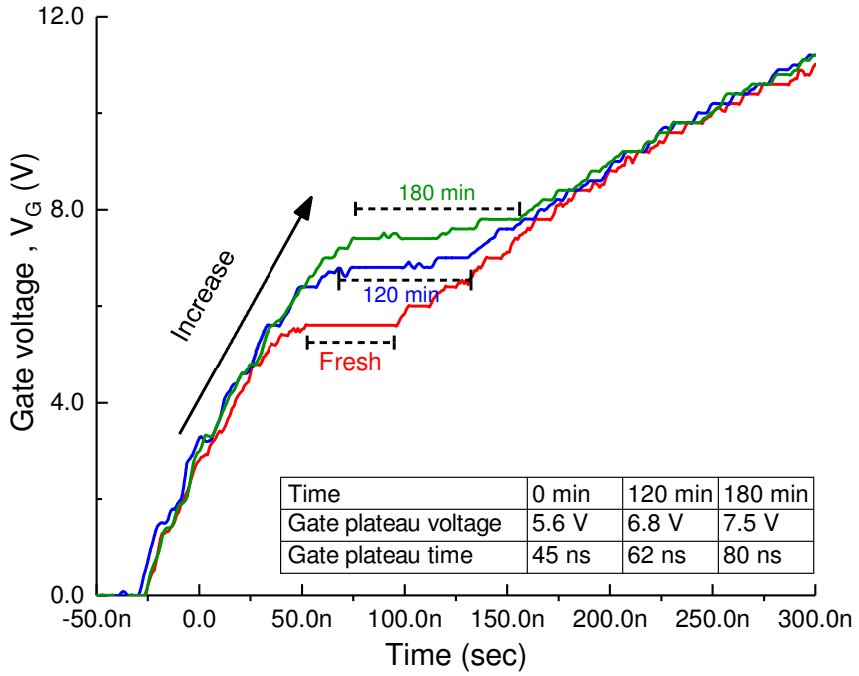


Figure 3.6: Variation of V_{GP} and t_{GP} shown in the gate voltage waveform.

@ 0 min (Fresh MOSFET). The preliminary results confirmed that both V_{GP} and t_{GP} reflected the gate-oxide degradation status with simultaneous positive shifts from their initial values.

3.5 High voltage, High temperature Experiment

3.5.1 Experiment Details

The devices studied in this work came from two leading commercial manufacturers of SiC devices; which prefer to remain anonymous. The first set of devices provided by Manufacturer-1 were 650 V, 70 A trench-gate SiC MOSFETs while the second set of devices provided by Manufacturer-2 were 1200 V, 19 A planar SiC MOSFETs. The devices with both planar and trench-gate structure were chosen for this study because these are the most common structures currently being used in the manufacture of commercial SiC MOSFETs. The experiment has been designed keeping in mind, the practical application scenarios of SiC MOSFETs, which are high voltage, high temperature, inductive load (or hard-switching), and high current conditions.

3.5.2 Experimental Setup

Figure 3.7 shows the circuit schematic of the experimental setup: a high-temperature double-pulse test (DPT) system with an inbuilt provision for applying a high temperature and high electric field (HT-HEF) stress to the gate oxide of SiC MOSFET. Figure 3.8 shows the physical experiment setup.

A double-pulse test is widely used to evaluate switching characteristics of semiconductor devices [53]–[55]. For this, a long turn-on pulse is applied to the device under test (DUT) in Figure 3.7, which causes the inductor current to ramp up to the desired current. The DUT is then turned OFF

making the inductor current, I_L to free-wheel through the diode (as shown with a purple dashed line). After a short time, the DUT is turned ON again with a short second turn-on pulse causing the inductor current to flow through the DUT (as shown with a purple solid line). The MOSFET's turn-on characteristics is obtained at the rising edge of second pulse.

The device under test (DUT) was vertically inserted into the sockets of the DPT board and screw-mounted to an aluminum bar that was bolted to the hot plate (thereby, ensuring a direct mechanical contact between the MOSFET's case and the hot plate). The temperature of the DUT was measured using a thermocouple and regulated within ±5 °C of the desired temperature using a temperature

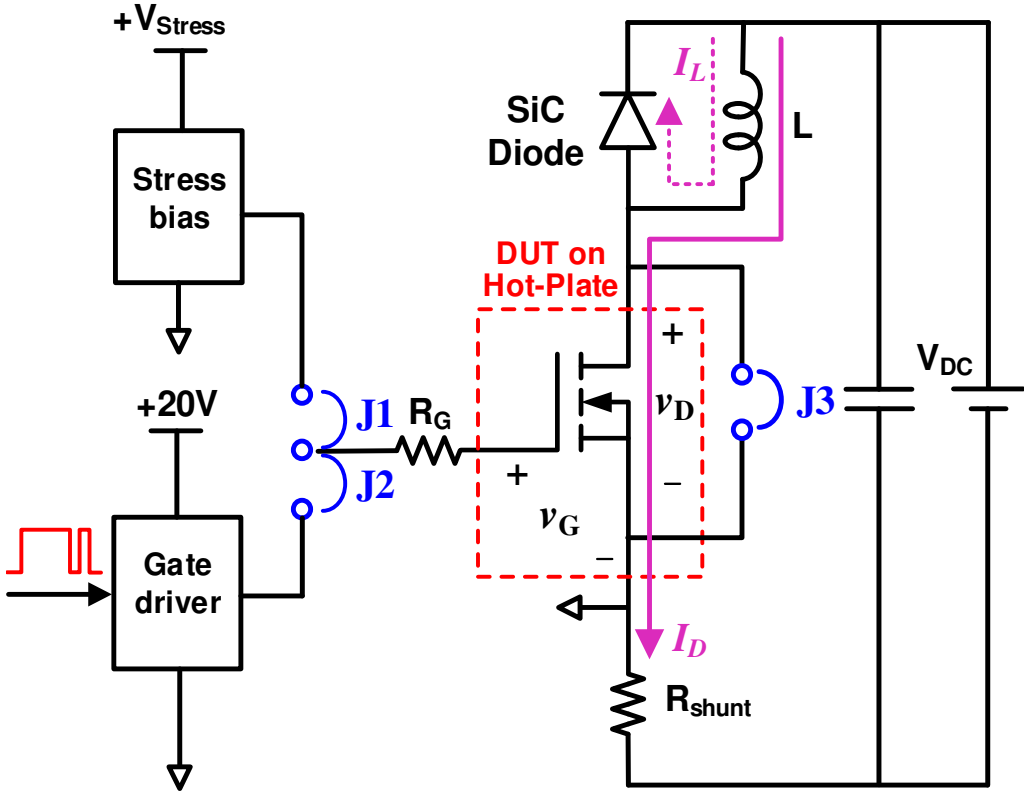


Figure 3.7. High temperature double-pulse test circuit schematic with provision for High Electric field stress (HEF).

controller. All the other components on the test board were kept at a reasonable temperature using an external fan. Each MOSFET was driven by a gate driver with a gate bias voltage of 0 V/+20 V. The gate-source voltage, V_{GS} and drain-source voltage, V_{DS} were measured using single-ended probes to ensure that there was no skewing (or minimum delay) between the waveforms. A 0.1 Ω coaxial current shunt was used to measure the drain current, I_D of MOSFET. A large gate resistance (R_G) of 100 Ω was intentionally inserted to slow down the switching speed of MOSFET and to damp the ringing due to parasitic components, making it clearer to observe the variation of precursors.

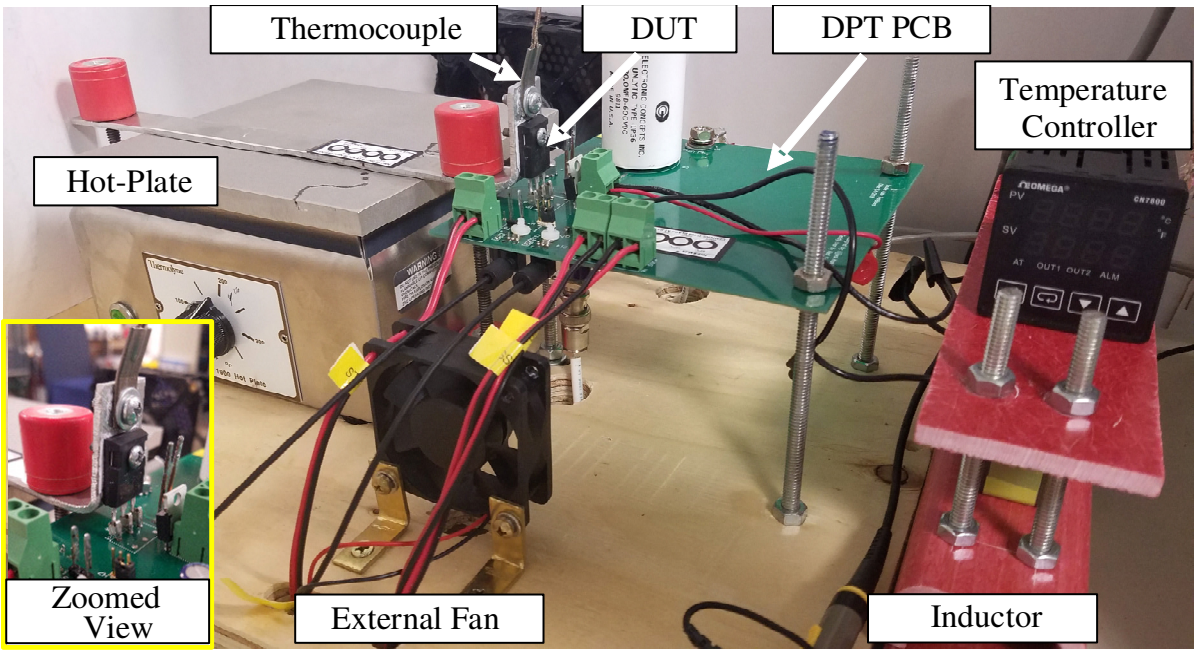


Figure 3.8. Experiment setup.

3.5.3 Test Condition Selection

The selection of following test conditions is explained below:

1) High temperature selection: The test temperature was chosen to be 25 °C lower than the maximum junction temperature specified for these devices in their datasheets. For the devices from Manufacturer-1, the temperature was regulated to 150±5 °C. Similarly, for the devices from Manufacturer-2, the temperature was regulated to 125±5 °C.

2) Accelerated aging stress level selection: The purpose of HEF stress was to induce accelerated aging of gate oxide. This was achieved by applying positive bias to the gate terminal with the drain and source terminals shorted (while being subjected to high temperature). For accelerated aging of gate oxide, a safe gate stress level (+45 V for Manufacturer-1 sample group and +42.5 V for Manufacturer-2 sample group) was determined by performing gate-oxide failure tests on several samples. The stress voltage was chosen such that it was large enough to initiate observable gate-oxide degradation, but low enough not to cause gate-oxide breakdown during the experiment.

3.5.4 Experimental Procedure

The experimental procedure to determine the variation of V_{TH}, V_{GP} and t_{GP} for each SiC MOSFET mainly comprised of three steps: 1) an initial baking (heating) of samples for half an hour, 2) the application of HT-HEF stress for a specific time to induce accelerated aging of gate oxide, and 3) the measurement of electrical parameters before and after the stress. In order to minimize the time between the application of HEF stress and measurement of the precursors (during double pulse tests), the DUT was not moved during the experiment. This was achieved by including provisions for jumpers to interchange between the HEF stress mode (connecting jumpers J1 and J3) and the

regular double pulse test mode (connecting jumper J2), as shown in Figure 3.7.

Figure 3.9 shows a flow chart that summarizes this experimental procedure. To start with, a fresh MOSFET was inserted into the socket of test platform. The sample was initially baked for half an hour without any bias stress (150 °C for Manufacturer-1 samples and 125 °C for Manufacturer-2 samples). Following the baking, the turn-on characteristics of the device were obtained using the double-pulse test method. The electrical parameters of interest: V_{TH}, V_{GP} and t_{GP} were obtained from the turn-on waveforms. While still in the test socket, the device was then subjected to HEF stress (while being subjected to the same temperature). Upon subsequent aging for a specific amount of time, the HEF stress was terminated, and the turn-on characteristics were measured

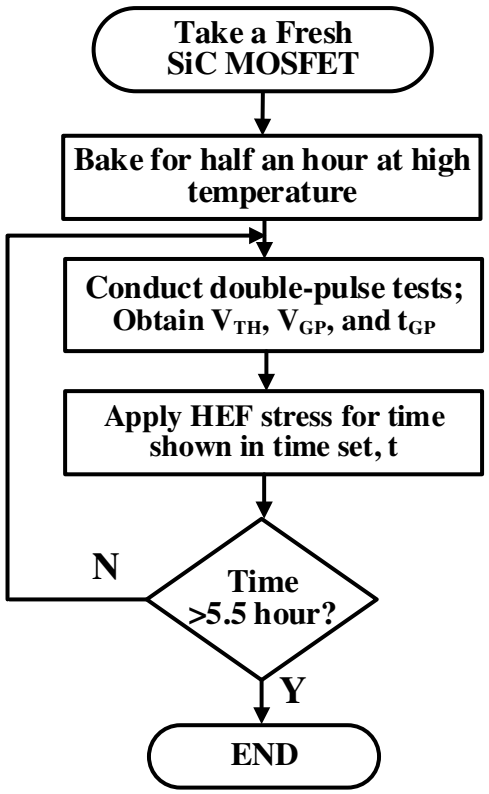


Figure 3.9: Flowchart of experimental procedure.

again. The stress-and-measurement of precursors were carried out for times represented by the time set, t= {0.5,1,1.5,3.5,5.5} hours.

3.6 Results and Discussion

A total of six MOSFETs (three from each Manufacturer) were tested to confirm the linear-with-log-stress-time variation pattern of electrical parameters. The names of different samples follow the format: MN1-xx for Manufacturer-1 sample group and MN2-xx for Manufacturer-2 sample group, where xx denotes each sample's number. Figures 3.10 and 3.11 show the overall variation of precursors (V_{TH}, V_{GP} and t_{GP}) with HT-HEF stress for all the samples, where the horizontal axis corresponds to the specific time (in logarithmic scale) at which each measurement was taken. The samples were baked for an initial half-an-hour without gate-bias stress and the values of precursors measured after this step is henceforth regarded as the precursor values of fresh MOSFETs. The insets on the far-right corner of each figure show the linear-fit to data points for each sample. It is worthy to note that for linear fitting, the first measurements recorded immediately after the baking period has not been included. This is because the HEF stress was applied to MOSFETs only after the baking period; which is a necessary condition for the initiation of tunneling process in gate oxide.

3.6.1 Variations of Threshold Voltage

Figures 3.10(a) and 3.11(a) show the variation of V_{TH} that occurred in both the MN1-xx (MN1-01 through MN1-03) and MN2-xx (MN2-01 through MN2-03) samples when the samples were subjected to HT-HEF stress. Fresh MN1-xx and MN2-xx samples (samples subjected to an initial

half-an-hour baking without gate-bias stress) had average initial V_{TH} of nearly 2.5 V. After half-an-hour of stress, V_{TH} increased to nearly 6.3 V for MN1-xx samples and to 3.7 V for MN2-xx samples. The threshold voltage continued to increase over the stress duration of 5.5 hours, but at a slower rate. This is typical of a linear-to-log-stress-time response; the values increase rapidly at first by a slower rate of increase over time. The insets on the far-right corner of Figures 3.10(a) and 3.11(a) show the linear-fit of V_{TH} for individual samples. The R-square values of individual linear fit were found to be between 0.92-0.97, a statistical measure which quantifies a strong linear relationship between the increase of V_{TH} and the logarithm of stress time.

Figures 3.12(a) and 3.13(a) show the gate-source voltage (V_G) and the drain current (I_D) waveforms for the samples MN1-03 and MN2-03, respectively. From these waveforms, the threshold voltage was determined to be the gate-source voltage at the rising edge of the drain current (as shown by dotted lines). The solid black arrows point to an increase of V_{TH} with stress time. Tabulated V_{TH} values show that V_{TH} @ 5.5 hour > V_{TH} @ 1 hour > V_{TH} @ 0.5 hour (Fresh MOSFET) for both MN1-03 and MN2-03 samples. Thus, the threshold voltage was observed to increase over the course of degradation.

3.6.2 Variations of Gate-Plateau Voltage

Figures 3.10(b) and 3.11(b) show the variation of V_{GP} that occurred in both MN1-xx (MN1-01 through MN1-03) and MN2-xx (MN2-01 through MN2-03) samples. It was observed that V_{GP} increased in a manner similar to V_{TH}. The insets on the far-right corner of Figures 3.10(b) and 3.11(b) show the linear-fit of V_{GP} for individual samples. The R-square values of individual linear fit were found to be between 0.98-0.99, which suggests a strong linear increase of V_{GP} with the log of stress time.

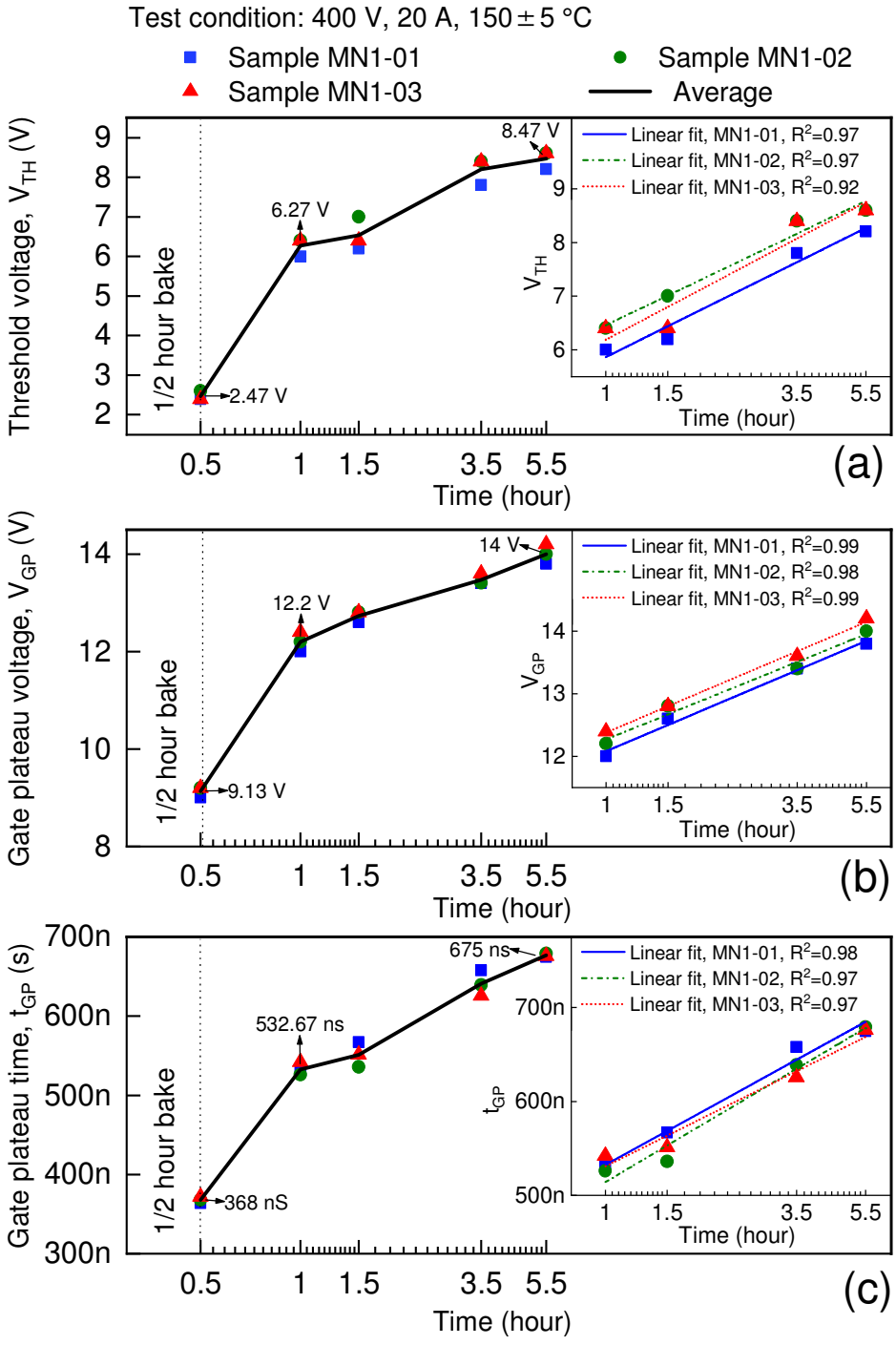


Figure 3.10: Variations of (a) Threshold voltage, (b) Gate-plateau voltage, and (c) Gate-plateau time, for three samples of MN1-xx samples over time. The insets on the far-right corner of each figure show the linear-fit to data points for each sample.

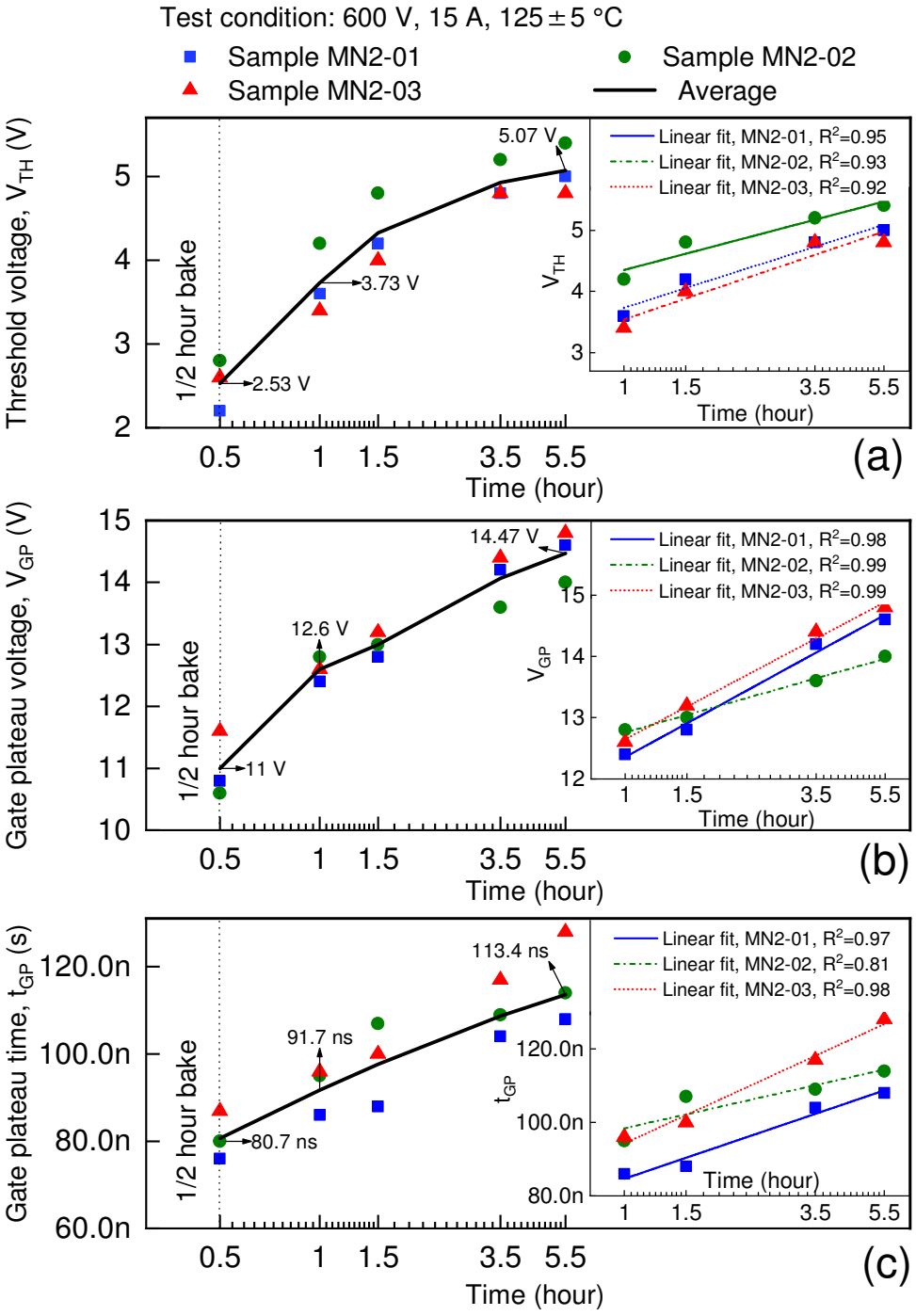


Figure 3.11: Variations of (a) Threshold voltage, (b) Gate-plateau voltage, and (c) Gate-plateau time, for three samples of MN2-xx samples over time. The insets on the far-right corner of each figure show the linear-fit to data points for each sample.

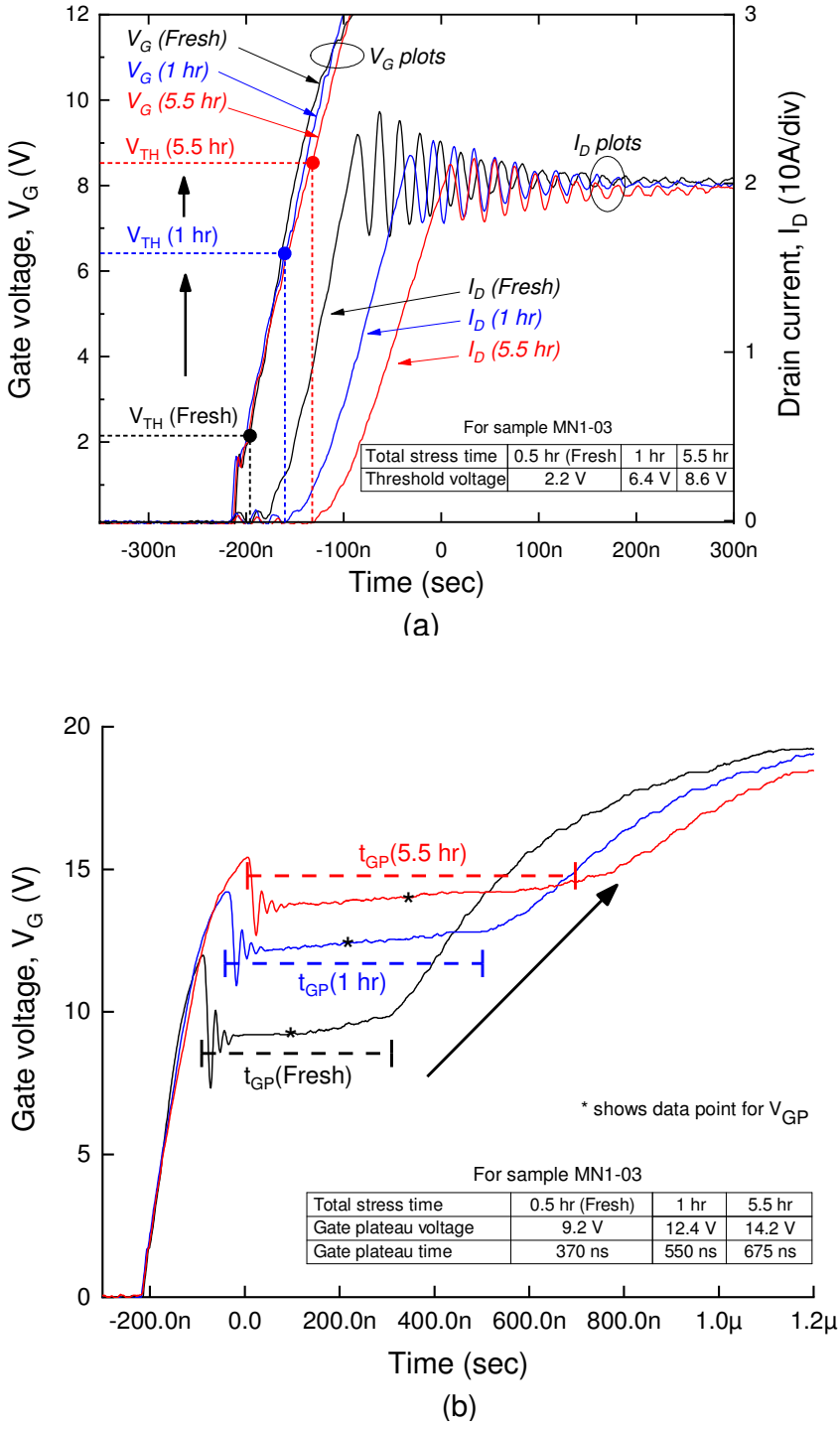
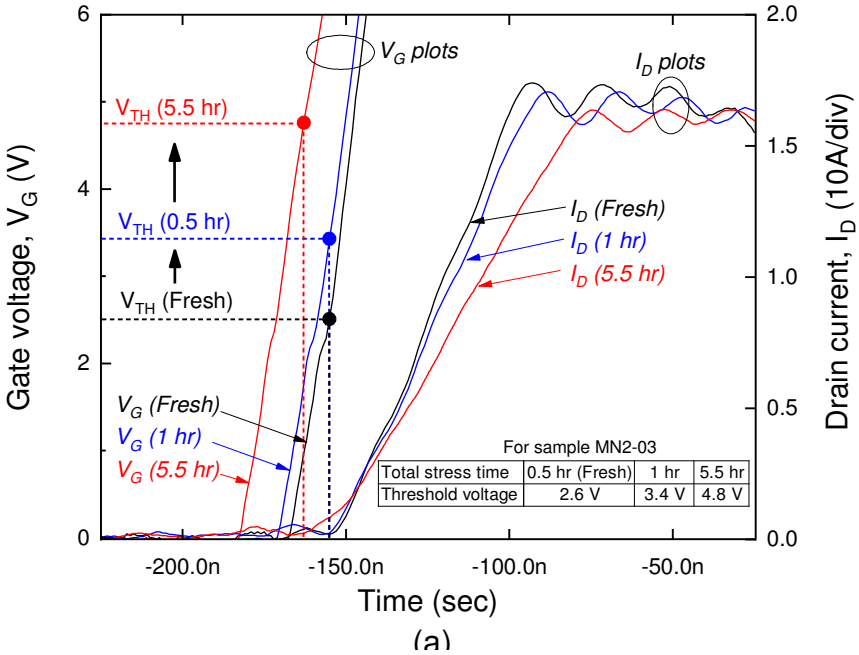


Figure 3.12: (a) Variation of V_{TH}, and (b) Variation of V_{GP} and t_{GP}, shown in gate voltage waveform of sample MN1-03.



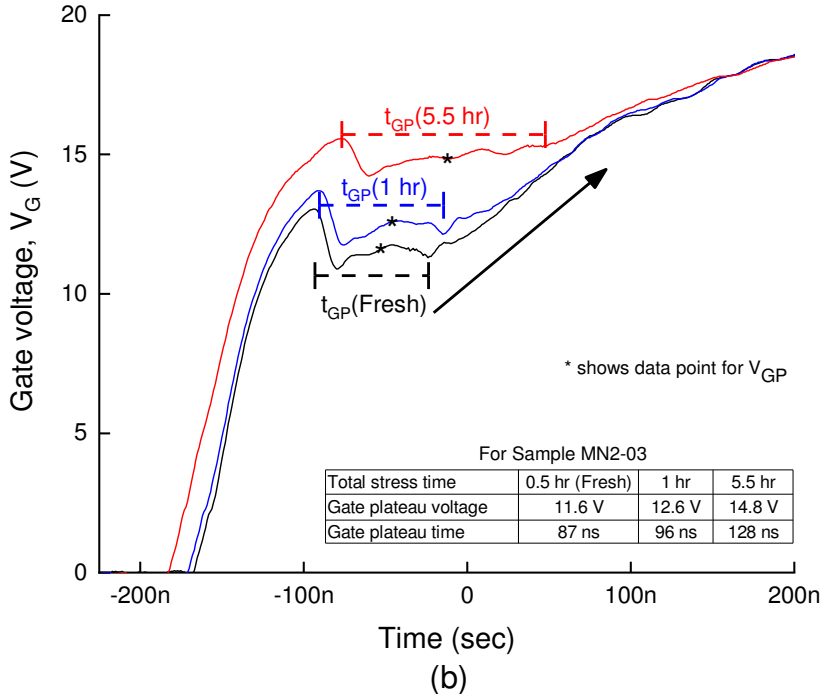


Figure 3.13: (a) Variation of V_{TH}, and (b) Variation of V_{GP} and t_{GP} shown in gate voltage waveform of sample MN2-03.

Figures 3.12(b) and 3.13(b) show gate voltage (V_G) waveforms for the samples MN1-03 and MN2-03, respectively. The asterisk symbol on the waveform indicates the measured data point of V_{GP} and the solid black arrow points to an increase of V_{GP} with stress time. Tabulated V_{GP} values show that V_{GP} @ 5.5 hour > V_{GP} @ 1 hour > V_{GP} @ 0.5 hour (Fresh MOSFET) for both MN1-03 and MN2-03 samples. Thus, the gate-plateau voltage was also observed to increase over the course of degradation.

3.6.3 Variations of Gate-Plateau Time

Figures 3.10(c) and 3.11(c) show the variation of t_{GP} that occurred in both MN1-xx (MN1-01 through MN1-03) and MN2-xx (MN2-01 through MN2-03) samples. It was observed that t_{GP} increased in a manner similar to V_{TH} and V_{GP}. The insets on the far-right corner of Figures 3.10(c) and 3.11(c) show the linear-fit of t_{GP} for individual samples. The R-square values of individual linear fit were found to be between 0.81-0.98, which suggests a strong linear relationship of t_{GP} with the log of stress time.

Figures 3.12(b) and 3.13(b) show gate voltage (V_G) waveforms for the samples MN1-03 and MN2-03, respectively. The dashed lines show t_{GP} at different stress times. Tabulated t_{GP} values show that t_{GP} @ 5.5 hour > t_{GP} @ 1 hour > t_{GP} @ 0.5 hour (Fresh MOSFET) for both MN1-03 and MN2-03 samples. Thus, the gate-plateau time was also observed to increase in a manner similar to other precursors: V_{TH} and V_{GP}.

3.6.4 Precursor Comparison

The experiment's results confirmed that all three precursors reflected the gate-oxide degradation

Table 3.1: Percentage shift of precursors in SiC MOSFETs.

Precursors	Manufacturer-1 MOSFETs (650 V, 70 A)	Manufacturer-2 MOSFETs (1200 V, 19 A)
	% positive shift	% positive shift
Threshold voltage	243%	100%
Gate-plateau time	84%	41%
Gate-plateau voltage	53%	32%

status with simultaneous positive shifts from their initial values. The average percentage increase from the respective initial values of precursors in both sample groups are provided in Table 3.1. The percentage shifts were computed for a total period of 5.5 hours, and for longer stress periods, it can be expected to increase further. Two observations were noted from this table:

1) The threshold voltage was found to be the most sensitive precursor for observing the positive shift, followed by t_{GP} and V_{GP}. In both sample groups, V_{TH} had the highest positive shift at nearly 240% and 100% for MN1-xx and MN2-xx samples respectively, followed by t_{GP} which had a higher positive shift (nearly 85% for MN1-xx samples and 40% for MN2-xx samples) compared to V_{GP} (nearly 55% for MN1-xx samples and 30% for MN2-xx samples).

2) The overall positive shift of all three precursors were much higher in samples from Manufaturer-1. This is because these devices had a higher nominal current rating (70 A) compared to the devices from Manufacturer-2 (19A). A higher current rating of the device represents a larger overall die

size and hence a larger gate-oxide area. Therefore, the effect of gate-oxide degradation can be expected to be more pronounced in SiC MOSFETs with higher current ratings; the application regime of SiC MOSFETs.

3.7 Conclusion

In this chapter, the three electrical parameters: V_{TH}, $V_{GP,}$ and t_{GP}, have been shown to be suitable precursors for monitoring the gate-oxide degradation process in SiC MOSFETs. It was also demonstrated both analytically and experimentally that these precursors increase in a linear-with-log-stress-time manner during gate-oxide degradation. The increasing trend, which results from the tunneling of electrons into oxide traps, was confirmed by inducing gate-oxide degradation preliminarily in commercial planar SiC MOSFETs under low voltage, room temperature conditions, and later on, in both planar and trench-gate commercial SiC MOSFETs under high voltage, high current, high temperature, and inductive load (or hard-switching) condition. In addition, no super-linear increase in precursor values was observed, indicating that the gate oxide in latest commercial SiC MOSFETs was robust against additional oxide-trap activation at high temperature.

Chapter 4

Conclusion

The findings of this research have helped in: i) understanding the effect of gate-oxide degradation on multiple electrical parameters of Si and SiC power MOSFETs, ii) identification of new gate-oxide degradation precursors, and iii) identification of variation pattern of precursors unique to Si and SiC power MOSFETs. The online precursors identified in this research enable monitoring of multiple electrical parameters without physical removal of MOSFETs, a convenience which can contribute to the advancement of condition monitoring, prognostics and health management of complex power-electronic systems. The summary of chapter-wise contributions is presented below:

Chapter 2 investigates the effects of gate-oxide degradation on multiple electrical parameters of Si power MOSFETs. The four precursors of Si power MOSFETs (V_{TH}, R_{ON}, V_{GP}, and t_{GP}) has been shown to vary with an interesting dip-and-rebound pattern over the course of gate-oxide degradation. The new precursor—the gate-plateau time (t_{GP}) has been demonstrated to be an effective precursor. The significance of dip-and-rebound variation pattern in terms of device performance, reliability and efficiency has been discussed. The analytical expressions have been derived to correlate the effect of gate-oxide degradation with simultaneous dip-and-rebound variation pattern in all four precursors. The dip-and-rebound variation pattern, which has been attributed to positive oxide-trapped charges and negative interface-trapped charges, has been

experimentally confirmed by inducing accelerated gate-oxide degradation in two different commercial Si power MOSFETs.

Chapter 3 investigates the effect of gate-oxide degradation on multiple electrical parameters of SiC MOSFETs. It has been shown that the three online precursors (V_{TH}, $V_{GP,}$ and t_{GP}) enable an effective monitoring of the gate-oxide degradation process in SiC MOSFETs. The three precursors have been shown to increase in a linear-with-log-stress-time manner over the course of gate-oxide degradation. The impact of linear-with-log-stress-time variation pattern in terms of device performance, reliability and efficiency has been discussed. The analytical expressions have been derived to correlate the effect of gate-oxide degradation with linear-with-log-stress-time variation pattern in all three precursors. The increasing trend of precursors, which has been attributed to tunneling of electrons into preexisting oxide traps, has been experimentally confirmed by inducing accelerated gate-oxide degradation in both planar and trench-gate commercial SiC MOSFETs, under high voltage, high current, high temperature, and hard-switching condition.

Chapter 5

Future works

The key contributions of this research can help to advance future works in following areas:

Developing a model for parameter shift due to gate-oxide degradation in power MOSFETS for predicting the degradation state and forecasting the remaining useful of gate-oxide

It would be interesting to extend the variation pattern of precursors to develop a model for parameter shift occurring during the gate-oxide degradation process in power MOSFETs. The developed model could then be extended to predicting the degradation state and forecasting the remaining useful life of gate-oxide. For Si MOSFETs, the degradation model could be subdivided into two components: One model describing the negative shift or dip of electrical parameters, and another model describing the positive shift or rebound of electrical parameters. The development of a parameter-shift model for SiC MOSFETs might be simpler in comparison to their Si counterparts since the precursors already exhibit a linear relationship with the logarithm of stress-time.

Observing the parameter shift of precursors in SiC MOSFETs during normal operating conditions

The MOSFETs can be turned ON by applying a positive voltage (typically +20 V) and can be turned OFF by applying a zero gate-voltage or a negative gate-voltage (typically -5 V). In our experiments with SiC MOSFETs, a gate voltage of 0 V was used to turn off the MOSFET to

prevent the oxide traps from discharging the trapped electrons. For many practical applications, a negative gate voltage is generally used to turn off the MOSFET. It would be interesting to observe the parameter shift during the application of a gate voltage of -5V / 20V. In this case, the net parameter shift would also depend upon the duty cycle. This is because the net parameter shift would be a cumulative effect of the charging of oxide traps during the turn-on time (when +20 V is applied) and the simultaneous recovery or discharging of oxide traps during the turn-off time (when -5V is applied).

Developing a gate drive IC with prognostic capabilities

In practical applications, a small gate resistance is preferred in order to reduce the switching loss and expedite the switching speed of MOSFET. However, during intermittent monitoring and measurement of online precursors, it might be necessary to drive the MOSFET with a larger gate resistance. This intentional insertion of large gate resistance slows down the switching speed of MOSFET, damps the ringing due to parasitic components, and makes it clearer to observe the variation of precursors. A smart gate drive IC with prognostic capabilities that can dynamically change the gate resistance between the normal operation mode and the degradation monitoring mode would be an interesting application.

APPENDIX

APPENDIX

Evaluation of the magnitude of second term of expression (3.6)

The gate-plateau voltage can be shown to increase approximately in a linear-with-log-time manner if the magnitude of second term of (3.6) can be shown to be negligible. Please note that this term comprises of manufacturing parameters like L_{CH}, Z and μ, which are not readily available from the datasheet of commercial MOSFETs. Therefore, its magnitude must be indirectly determined from other available parameters from datasheet and test conditions [31]. To begin with, the expression for channel resistance of SiC MOSFETs R is taken into consideration, which is given by [39]

$$R_{CH} = \frac{L_{CH}}{2Z\mu C_{ox}(V_G - V_{TH})}, \tag{A.1}$$

where Z is the length of the cell in the orthogonal direction to the cross section shown in Figure 1.1, L_{CH} is the channel length, μ is the channel carrier mobility, and C_{ox} is the specific gate-oxide capacitance. The relatively low mobility makes the channel resistance dominant component of on-resistance in SiC MOSFETs [12], [56]. For simplicity, we can assume the channel resistance to be nearly 75% of its on-resistance (Ron) [56].

Equation (A.1) can be multiplied with drain current (I_D) on both sides and can be re-written as

$$\frac{I_D L_{CH}}{\mu C_{ox} Z} = 2 I_D R_{CH}(V_G - V_{TH}), \tag{A.2}$$

where values of I_D, R_{CH} ($\approx 0.75\ R_{ON}$), V_G and V_{TH} and are accessible from manufacturer datasheet and test conditions, which are 20 A, 0.75*30 mΩ, 20 V and 2.7 V, respectively for the samples from Manufacturer-1 (denoted by MN-1) and 15 A, 0.75*160 mΩ, 20 V and 2.6 V, respectively for the samples from Manufacturer-2 (denoted by MN-2). Upon substituting these values in equation (A.2),

$$\frac{I_D L_{CH}}{\mu C_{ox} Z} \cong \begin{Bmatrix} 16\text{, for MN-1 samples} \\ 64\text{, for MN-2 samples} \end{Bmatrix}. \tag{A.3}$$

Using equation (A.3), the second term of equation (3.6) can be approximated to

$$\frac{1}{2\mu}\sqrt{\frac{I_D L_{CH}}{\mu C_{ox} Z}}\ \frac{\partial \mu}{\partial \ln t} \cong \begin{Bmatrix} \frac{2}{\mu}\frac{\partial \mu}{\partial \ln t}\text{, for MN-1 samples} \\ \frac{4}{\mu}\frac{\partial \mu}{\partial \ln t}\text{, for MN- 2 samples} \end{Bmatrix}. \tag{A.4}$$

The parameter shifts in SiC MOSFETs has been attributed to the 'slow' NIOTs, which are farther away from the interface and exhibit a long response time to bias-stress [21]. In contrast to the 'fast' NIOTs (which are very close to the interface and respond very quickly to bias-stress), the slow NIOTs change their charge states gradually, leading to a more permanent shift (or drift) of electrical parameters. As mentioned earlier, the presence of trapped charges inside the oxide decreases the mobility of charge carriers in the channel by coulombic scattering. However, the effect of trapped charges on mobility is location dependent [57], [58], i.e., the trapped charges that are located farther from the interface has a much smaller effect on mobility of charge carriers in the channel compared to the trapped charges that are closer to the interface. As a result, the 'slow' NIOTs, which are located farther away from the interface, will have a minor effect on the mobility

of charge carriers in the channel. Also, for a small change in mobility, the magnitude of equation (A.4) is also small. For example, if the mobility decreases by 10%, then $\partial\mu/\partial \ln t = 0.1\mu / dec$; the magnitude of this term is reduced by factor of 10. Similarly, if the mobility decreases by 5% over a decade of stress-time, then $\partial\mu/\partial \ln t = 0.05\mu / dec$; the magnitude of this term is reduced by a factor of 20. Upon considering this term to be negligible, equation (3.6) simplifies to

$$\frac{\partial V_{GP}}{\partial \ln t} \simeq \frac{\partial V_{TH}}{\partial \ln t} \ . \tag{A.5}$$

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