DESIGN, ANALYSIS AND CONTROL OF A SiC BIDIRECTIONAL G2V, V2L AND V2G UNIVERSAL POWER CONVERTER IN NEXT GENERATION ELECTRIC VEHICLE

By

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ABSTRACT

DESIGN, ANALYSIS AND CONTROL OF
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As the electric vehicle (EV) is becoming more and more popular, there exists an increasing need for more efficient charging facilities for both on-board and off-board chargers. High power density on-board charger can help reduce the weight of the vehicle and leading to higher miles per kilo-watt-hour (kwh). What is more, EV with tens of kilo-watt-hour battery is a perfect energy storage unit with mobility. Hence, in the next generation modern home-based microgrid system, EV can play multiple roles beyond transportation. For example, EV can send active power back to the grid, which can help reduce the power grid burden during peak hour. EV can also improve the distribution power grid quality by sending reactive (either inductive or capacitive) power to the grid especially where the heavy unbalanced load is connected. The power flow interaction between the vehicle is often recognized as G2V (Grid to vehicle or charging mode) or V2G (vehicle to grid). Not only does EV can help stabilize the grid, but also it can benefit the home appliance by providing robust AC (single-phase or three-phase) or DC voltage output for various loads whenever the mainline is not available. However, these application scenarios would not be feasible if there is no such universal power converter to facilitate the power flow. A modular and universal power converter is of great need to achieve this goal. Hardware design flexibility and scalability are very important which allows configurations into different ways to accomplish various functions mentioned above.

Hence, in this thesis, a hardware prototype with the mentioned property is built to prove the idea and solve the challenges of integrating all function in a single unit. The wide bandgap power device is used due to their excellence in the reduction of switching and conduction losses. Robust gate drive design with protection feature is explained and verified with experiments results. Galvanic isolation is required in such a converter and implemented by an isolation transformer. The nanocrystalline core material is selected to construct the isolation transformer in this prototype since it has higher saturation flux density and relatively low core losses at high frequency. Optimization algorithm for low conduction loss under variable operating modes is proposed. A generalized transformer design procedure is also discussed and verified with experimental results. To realize these multiple functions, sensors and digital signal processors are used to control this converter. Detailed control strategy for each application scenario has been analyzed and verified with simulation or experimental results.

Dedicated to:

My parents: Haisheng Wang, Xiaoling Zhang

My wife: Ziyou Zhang

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Chapter 1 Introduction

1.1 Research motivation of universal bidirectional converter

Electric vehicle (EV) is gaining more attention from customers due to its ample compelling futures such as environment friendly technology, lower cost per mile, and competitive driving performance. What is more, EV can extend more functionalities besides of being only the transportation facility. Nowadays, EV with a few tens of kWh battery is the perfect candidate for smart and green home system. Hence, there is of great need to equip EV with certain power converters to make it qualified and capable for this important role as the power hub in such system. However, most of the designs are fixed output which increase more component cost whenever additional output or feature are needed. In the next generation modern home-based micro grid system, EV can play multiple roles beyond transportation. For example, EV can send active power back to grid, which can help reduce the power grid burden during peak hour. EV can also improve the distribution power grid quality by sending reactive (either inductive or capacitive) power to the grid especially where heavy unbalanced load is connected. The power flow interaction between the vehicle is often recognized as G2V (Grid to vehicle or charging mode) or V2G (vehicle to grid). Not only does EV can help stabilize the grid, but also it can benefit the home appliance by providing robust AC (single phase or three phase) or DC output for various loads whenever the main line is not available. However, these application scenarios would not be feasible if there is no such universal power converter to facilitate the power flow. A modular and universal power converter is of great need to achieve this goal. Hardware design flexibility and scalability is very important which allows configurations into different ways to accomplish various functions mentioned above. With different combinations of modularized power converter building block (PCBB), various voltage and power rating can be achieved. This

converter can output different types of voltage, such as AC or DC, high voltage or low voltage, single-phase or three-phase.

This converter will be an important piece inside the EV's power conversion unit. Due to its limited space inside the EV, the converter needs to be as compact as possible. The size of the converter is determined by several factors, such as the cold plate, the power devices, the capacitors, and the magnetics components such as common mode chokes, the line inductor, and the transformer. The ideal format of switching is no conduction loss which means that there is no voltage drop and turn on resistance during on state, and no switching loss during on/off transition. However, there is no such ideal device. Fortunately, the appearance of wide band gap device can improve the performance of switching power device and that will lead to faster switching with higher current and voltage while generating less power loss. To explore the potential of the benefit of adopting wide band device in the automotive applications, SiC power module is selected as the switching device of the converter.

1.2 Existing on-board charger review

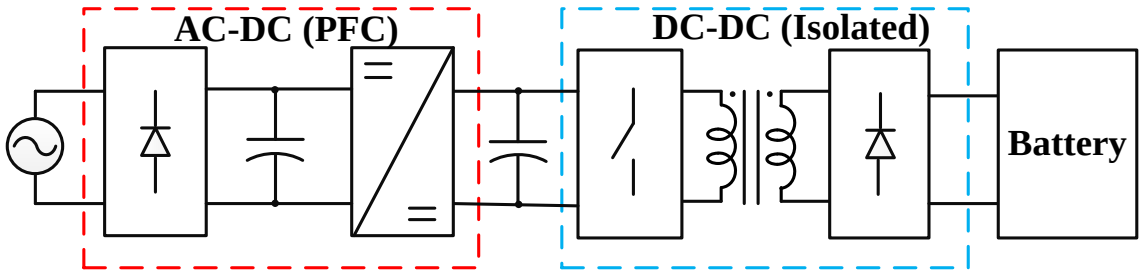


Figure 1- 1 Existing traditional OBC

The most common charger [1] inside EV is a two-stage single phase charger. The first stage is AC-DC which consists of rectifier and DC-DC converter to regulate the current to perform power factor correction function. Extensive reviews of different PFC topologies are summarized in [2] ~ [4].

The second stage is isolated DC-DC converter. Options for isolated are numerous, such as flyback, push-pull, full-bridge, resonant LLC, and dual active bridge converters. Some of them are good for low power applications, while others are more suitable for high power application. Comprehensive reviews of isolated DC-DC converter are summarized in [5] ~ [8].

There also exists single-stage on-board charger [9] ~ [19]. It chops the grid 50/60Hz power into much higher frequency and sends the power through a high frequency transformer whose secondary rectifies the AC power to DC charging the battery shown in Fig 1-2.

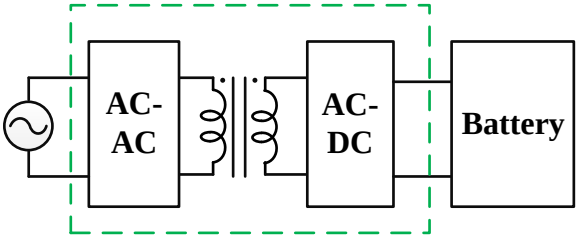


Figure 1- 2 Single stage on OBC

The common charging profiles used in the industry for Li-ion batteries are constant current (CC) and constant voltage (CV) charging. During CC charging, the current is regulated at a constant value until the battery cell voltage reaches a certain voltage level. Then, the charging is switched to CV charging, and the battery is charged with a trickle current applied by a CV.

For OBC, it should be able to provide both CC and CV mode operation capability.

1.3 Proposed SiC bidirectional universal power converter

In this thesis, a unique circuit topology with isolation is proposed to perform various essential functions in single unit such as grid to vehicle on board charging (G2V), vehicle to grid connection (V2G), and vehicle to load (V2L). The proposed circuits in this thesis is composing 8 half bridge legs and it is shown in Fig1-3. P1 to P4 and S1 to S4 along with the transformer in between are known as dual active bridge (DAB). The Q1 ~ Q8 are acting as the grid side

switches or load switches. Q7 and Q8 serves the purpose of neutral connection when working with 3phase 4 wire system.

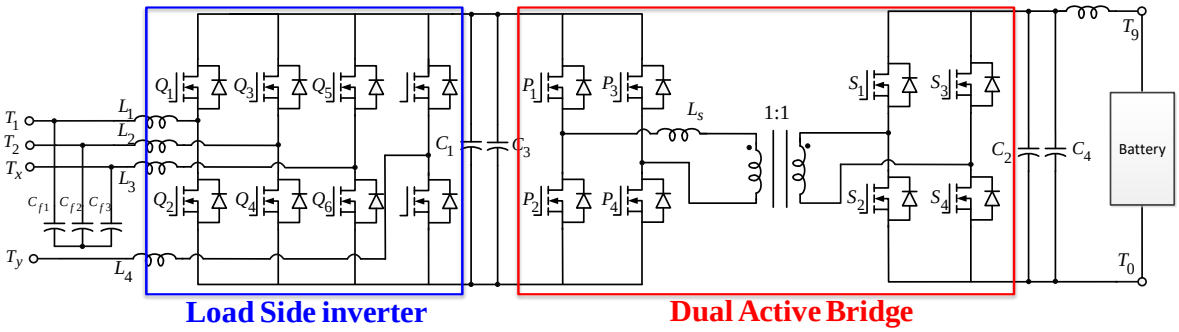


Figure 1- 3 Universal Power Converter Building Block (PCBB) Circuits

The high voltage battery is connected between T9 and T0. The battery has a range of 250V to 450V. The T1, T2, Tx, and Ty are referred as the load or grid terminals. Depending on what is the load, the PCBB will be configured into different ways as shown in Fig. 1-4.

Applications	Connection
Single Phase AC/Load	T1, T2 paralleled as Line Tx, Ty paralleled as Neural
Three Phase AC System/ Load	T1 as line, T2 as line Tx as line, Ty as neutral
48V(Low) DC Load	T1 T2 paralleled as Positive T4 as negative

Table 1- 1 PCBB Rated Power Under Different Applications

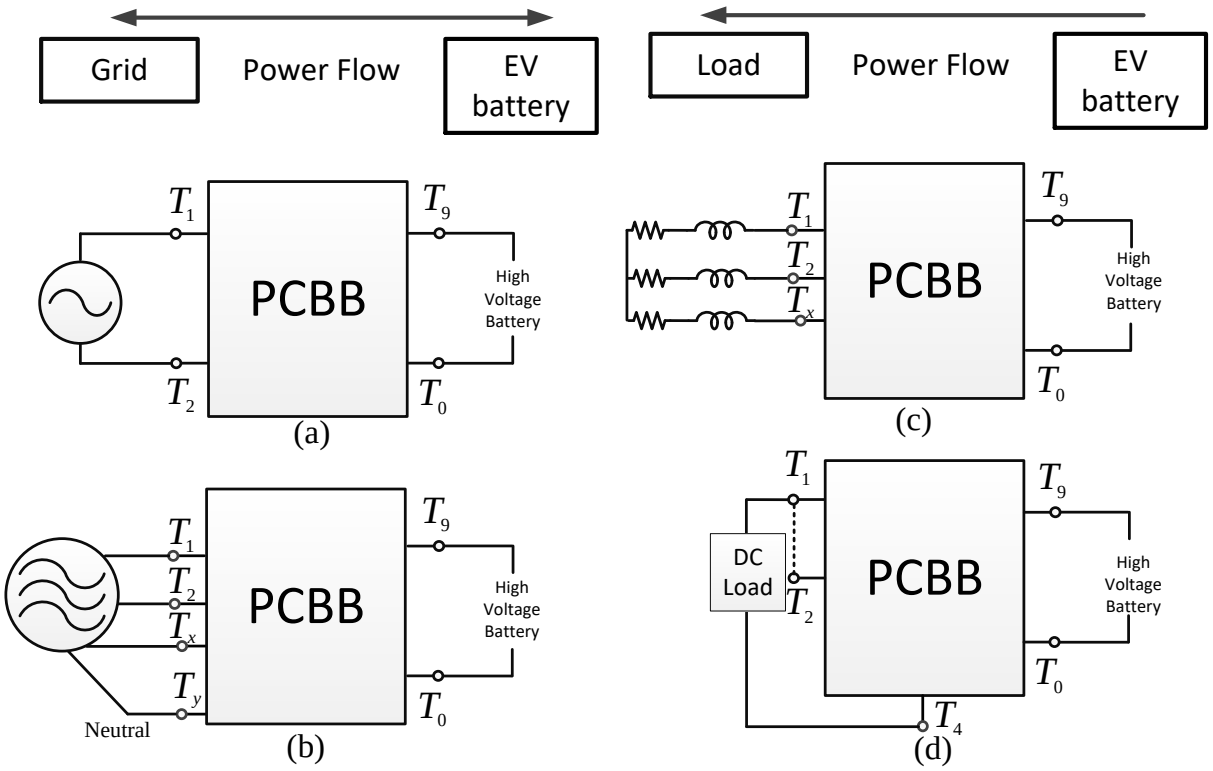


Figure 1- 4 Proposed operation modes

1.4 Scope of the thesis

This thesis is to solve the challenges of integrating all functions into single unit. It covers the hardware design, modeling analysis and control design.

The dissertation is focused on the following subjects to demonstrate the idea of universal power converter.

Chapter 2 describes prototype hardware detail including the gate drive, passive components and the digital control platform.

Chapter 3 explains the control principle and shows simulation and testing results of V2L (AC load or DC load) mode to verify the functionality.

Chapter 4 explains the control principle and shows simulation and testing results of V2G (active power or reactive power) mode to verify the functionality.

Chapter 5 explains the control principle and shows simulation and testing results of G2V (single phase or three phase) charger mode to verify the functionality.

Chapter 6 discusses the conclusion and future work.

Chapter 2 Hardware design of the PCBB

2.1 Selection of Power MOSFET

2.1.1 Wide band gap devices

The advances in WBG power devices [43] enables delivery of dramatic improvements in performance as well as new capabilities, which are not possible with silicon-based devices. Since SiC based semiconductor generally can endure higher voltage and carry larger current, SiC MOSFET is selected as the switching device in this work.

An ideal power switch will possess the following characteristics:

• Able to carry large current with zero voltage drop in the on-state;

• Blocks high voltage with zero leakage in the offstate;

• Induces zero energy loss when switching from off- to on-state and vice versa

With silicon, it is difficult to combine these desirable yet opposed characteristics, especially at high voltage and current. For example, at breakdown voltage 800V or even higher, the channel resistance along with forward voltage drop is very high because of the large drift region required to withstand such voltage. Insulated Gate Bipolar Transistor (IGBT) [43] devices were hence developed to address this problem. For the case of IGBTs, low resistance at high breakdown voltage is achieved at the cost of switching performance. Minority carriers are injected into the drift region to reduce conduction (on-) resistance. Due to SiC's breakdown field strength that is ten times higher than that of silicon, SiC devices can be constructed to withstand the same breakdown with a much smaller drift region.

MOSFETs are majority carrier devices so they have no "tail" current, which is the case with IGBTs when turned off and hence impose the switching speed of IGBT. SiC MOSFETs,

therefore, combine and integrate all three desirable characteristics of power switch, such as low on-resistance, high breakdown voltage, and fast switching speed. SiC MOSFET's smaller die size means smaller parasitic capacitances. The improvement in turn-off is due to absence of tail current in the MOSFET. The improvement in turn-on is due to the much lower recovery loss of the SiC diode.

Unlike silicon MOSFET's, the body diode of a SiC MOSFET presents excellent reverse recovery performance, which is equal to the performance of discrete SiC SBD. Due to the nature of material's larger bandgap, a SiC device can operate at very high temperature. Additionally, SiC's thermal conductivity is three times higher than that of silicon. These properties can help lower cooling needs, making it simpler to cool SiC components. This leads to supporting thermal systems that can be smaller, lighter and lower cost. What is more, the electrical characteristics of SiC MOSFETs do not vary with temperature as much as silicon MOSFET [43]. The difference compared to silicon device can be summarized into Fig 2-1 and Fig 2-2.

In general, low switching losses with SiC MOSFET can bring significant benefits and these are elaborated below:

• Lower losses can incur less heat generation, which leads into smaller, and even lighter cooling systems and ultimately higher power density.

• Reduced switching losses can enable switching frequency to increase to further shrink the sizes of passive components (such as capacitors, inductors and even transformers), reducing system cost, size, and weight (higher power density).

• Less heat allows lower operating temperature under which components do not have to be derated and permits smaller, less expensive components to be used.

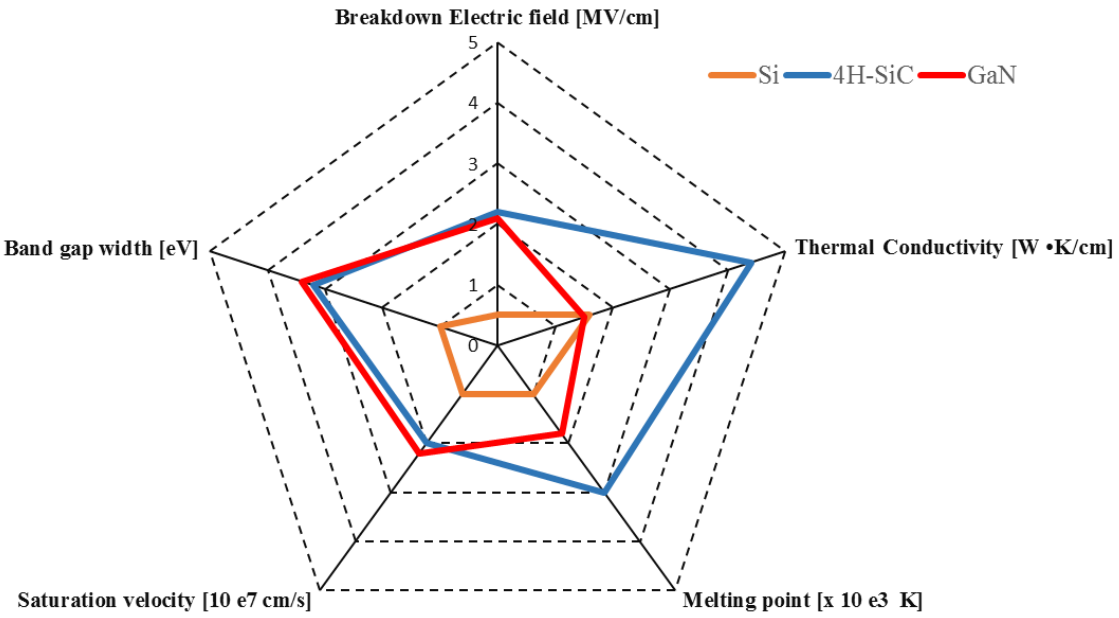


Figure 2- 1 Materials property of Si Vs SiC Vs GaN

Feature	Indication
Breakdown Electric field [MV/cm]	High Voltage Operation
Band gap width [eV]	
Thermal Conductivity [W •K/cm]	High Temperature applications
Melting point [x 10^3 K]	
Saturation velocity [10^7 cm/s]	High frequency operation

Figure 2- 2 Indications of each features

2.1.2 Selected SiC Power MOSFET Key Characteristics

The selected MOSFET BSM120D12P2C005 shown in Fig 2-3 is from Rohm semiconductor [23]. Its key parameters have been summarized into table 2-1.

Figure 2- 3 SiC Half bridge Power module

Parameter	Value
Drain-source voltage	1200V
Drain Current	134A (DC) 240A (Pulsed)
Max Junction Temperature	175 °C
Vgs Threshold Voltage	2.3V
Td(on) turn on time	45 ns
Td(off) turn off time	170 ns
Gate charge	570 nc
Rds ON	15 mOhm
Turn on Loss	3.2 mJ
Turn off Loss	1.5 mJ

Table 2- 1 Maximum rating and electrical characteristics

1200V and 134A SiC half bridge power module is selected since the maximum DC bus voltage is 700V (considering switching transient voltage spike 50% margin is given) and the maximum current under full load is 130A which is only happening for short intervals and will not incur thermal issue per the pulsed current rating.

Vgs is indicating at what voltage level the MOSFET is start being ON which allows current to flow and rise.

Turn on time and turn off time is defined as shown in Fig 2-4 per data sheet [23]. The double pulse result gives the actual switching transient in this setup.

The gate charge is used to calculate the power needed to switch on the device at certain frequency. Associated with that is the input capacitance Ciss which is defined in Fig 2-5. The parasitic capacitance is highly nonlinear regarding the drain-source voltage as shown in Fig 2-6.

On resistance is another important factor when selecting MOSFET because it is indicating the conduction loss $P_{cond} = I_{rms}^2 R_{ds-on}$.

Switching loss data can be calculated from the measurement on the actual prototype. Normally this information can be also found in the data sheet known as Eon and Eoff in Fig 2-7.

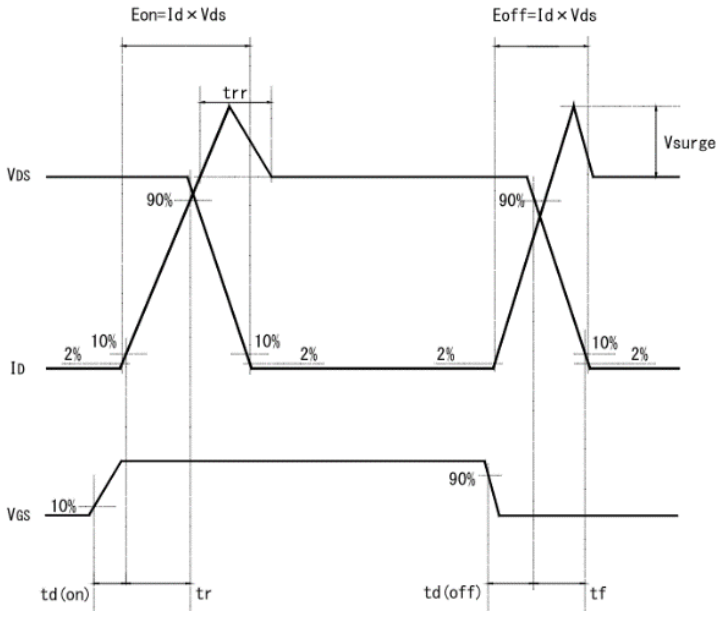
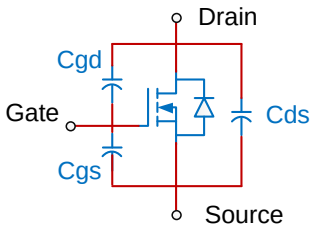


Figure 2- 4 Turn On/Off time



Symbol	Expression	Meaning
Ciss	Cgs+Cgd	Input capacitance
Coss	Cds+Cgd	Output capacitance
Crss	Cgd	Feedback capacitance

Figure 2- 5 MOSFET Parasitic Capacitance

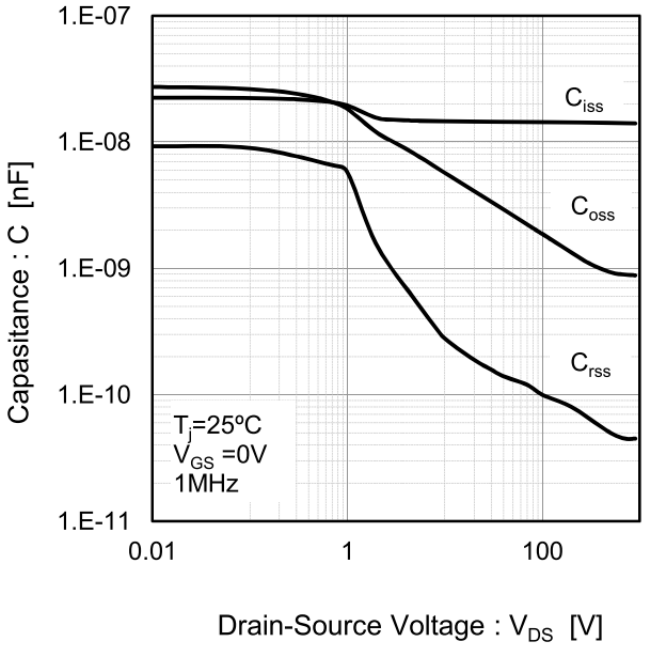


Figure 2- 6 Parasitic capacitance vs VDS

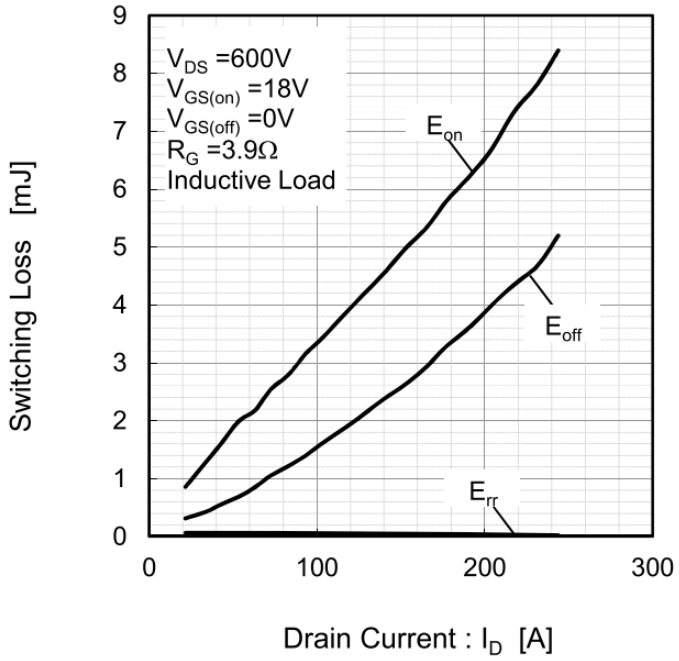


Figure 2- 7 Switching loss vs Drain current

2.2 Design of SiC gate driver

The gate drive serves an important role: turn on/off the power MOSFET with proper protection. The principle is to take the PWM signal (mA level) from the control and then amplify to driving current (A level). The gate drive should be isolated from the digital control system and provide enough protection features to prevent the converter from faulty operation. Detailed design can be found in the following sections.

2.2.1 Gate drive topology

The gate drive normally consists of two parts as shown in Fig 2-8 [47]:

- ✓ isolated power supply to power the gate drive and provide the power needed for switching on/off the device;
- ✓ gate drive IC (sometime with amplifier buffer IC) to amplify the current through an isolated channel (isolated methods can be capacitive or inductive)

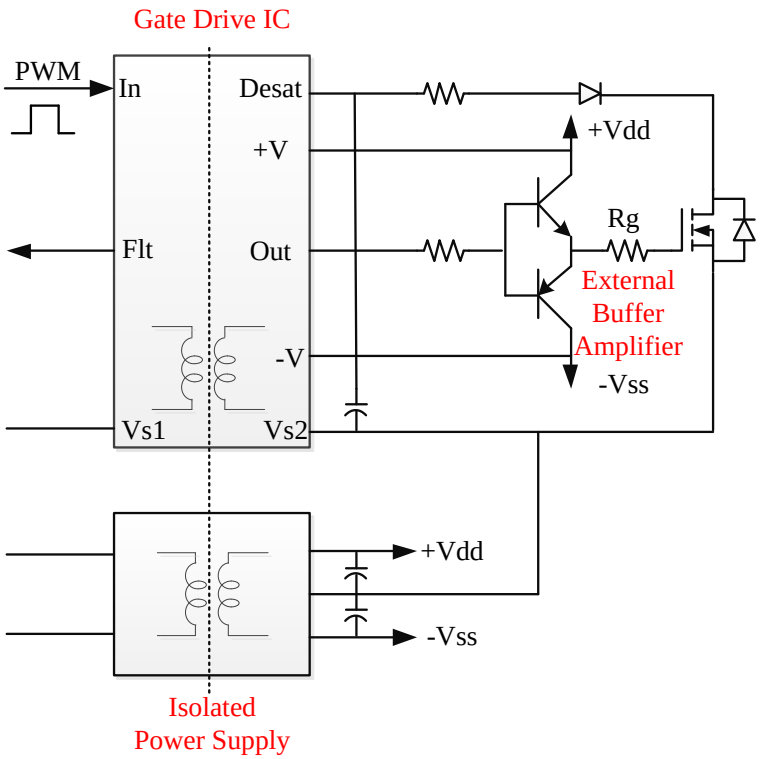


Figure 2- 8 Typical Gate drive structure

For the selected SiC MOSFET, the positive turn ON gate bias voltage is Vdd2 = 19V, and the negative turn OFF gate bias voltage is Vss2 = -5V. Based on the gate charge curve provided in the datasheet in Fig 2-9, the power needed to drive the MOSFET at switching can be found.

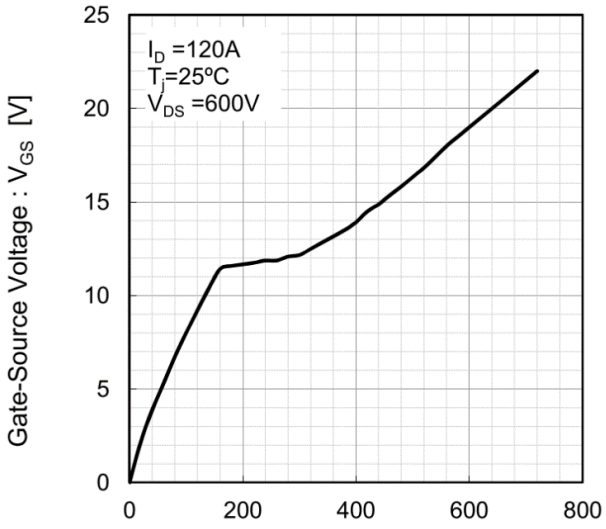


Figure 2- 9 Gate Charge Curve

$$P_{gdsw} = \frac{1}{2}(V_{dd2} - V_{ss2})Q_g f_{sw_{Limit}} = 0.5 * 24V * 570nC * 200kHz = 1.368W \quad (2\text{-}1)$$

$$P_{gdPOWER} = 2P_{gdsw} = 2.7\text{W} \quad (2\text{-}2)$$

Hence, we need an isolated power supply whose power rating is 3W and can generate dual output. Final selection comes down to the PQMC3-D24-D12-S [45].

Gate drive IC is another important piece which takes cares of switching ON/Off dynamics. There are several key factors which needs extra cautions such as isolation type, source/sink current level, propagation delay, common mode transient injection (CMTI), undervoltage lockout protection, active miller clamp, Desat protection and soft shunt down. After detailed comparison, the final selection falls to ADuM4135 [46]. Section 2.2.2 will disclose the gate drive design proposed in this thesis.

2.2.2 Gate drive schematics

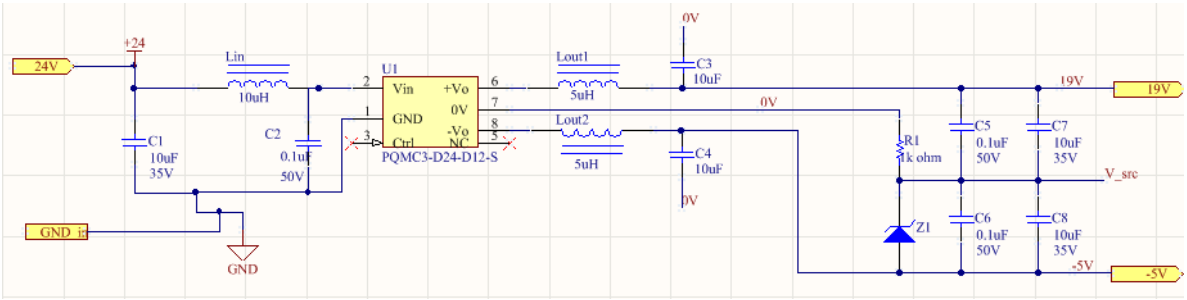


Figure 2- 10 Gate drive isolated power supply

In Fig 2-10, positive 19V and negative 5V is generated from the off-shelf power supply [45]. 5.1V Zener diode is placed between the power supply middle point output and the power supply negative rail output.

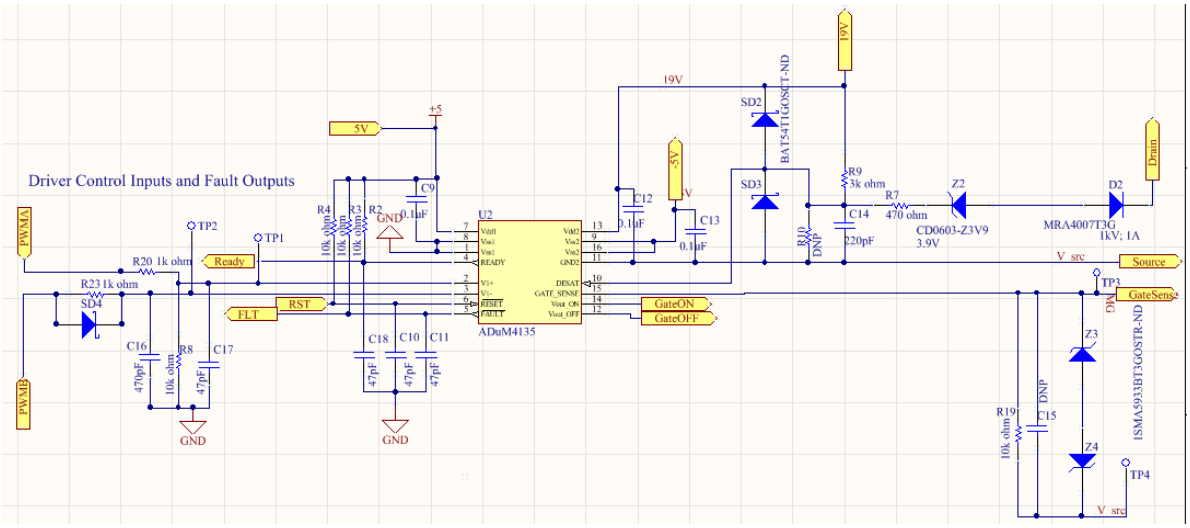


Figure 2- 11 Gate drive IC sections

The gate drive IC Vdd1 is connected to 5V. Ready signal (“HIGH”) is indicating the IC has no UVLO or Desat fault. Ready signal is not latched. It is pulled by R2 (10kohm resistor).

Fault(“LOW”) is indicating that Desat fault is detected. Once detected, the IC will be latched. Reset(“LOW”) can clear the fault. Both fault and reset are pulled by R3 and R4.

The IC protects the circuit with extra caution to avoid shoot through under half-bridge configuration. V1+ is the PWM signal for the MOSFET being driven. V1- is the PWM signal for complimentary MOSFET. When the IC detects both V1+ and V1- are high, it will shut down the gating to prevent shoot through. In this design, extra deadtime compensation has been added to the PWM signal path of V1-. R23, SD4, and C16 will determine the delay.

SD2 and SD3 are Schottky diode which protects the V_{dd2} from voltage spike over the maximum rated voltage.

Z3 and Z4 are Zener diode which functions the same. They clamp the gate-source voltage not exceeding +22V and -6V.

R9, R7, C14, Z2, and D2 are for Desat protection which will be explained later.

Gate_Sense pin is connected to MOSFET's gate pin for Active Miller clamp protection. Detailed explanation is the later section.

In order to provide enough source/sink current for turning ON/OFF the switch, additional buffer is placed on both Upper MOSFET and Lower MOSFET's gate drive. Three 1206 12 Ω resistor are used as gate resistor (effective gate resistance 4 Ω) for thermal concern as shown in Fig 2-12. Final gate drive board with SiC half bridge is shown in Fig. 2-13.

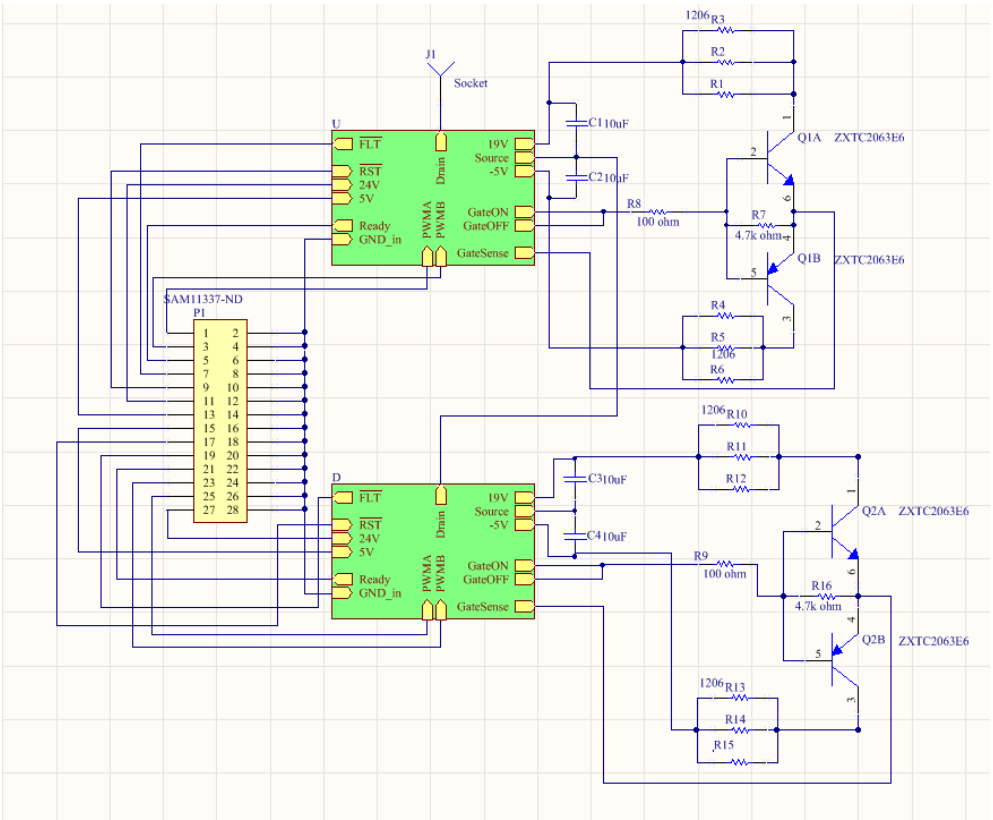


Figure 2- 12 Gate drive amplifier buffer section

Figure 2- 13 Gate drive board with SiC power module

2.2.3 Gate drive test (Double pulse) results

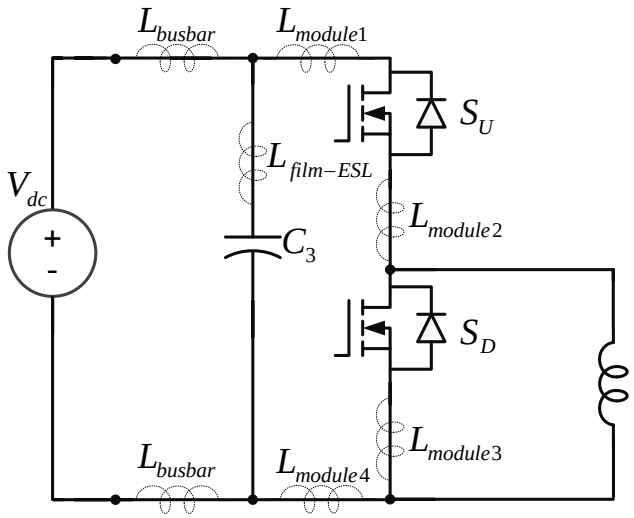
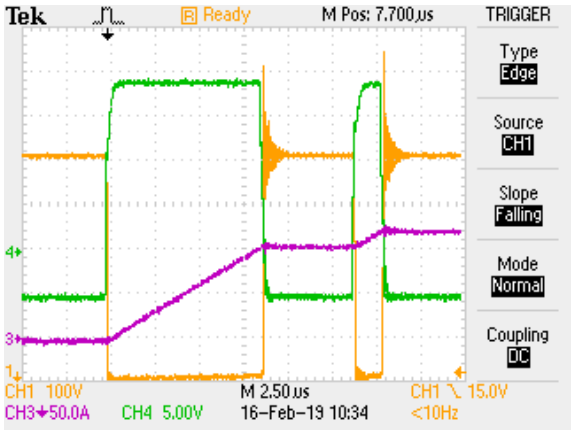


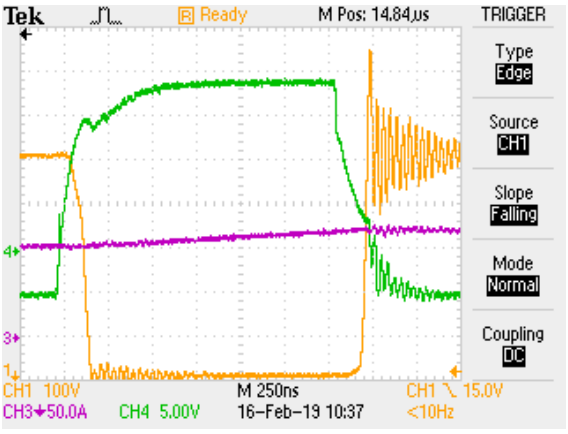
Figure 2- 14 Double pulse test setup

Double pulse test is used to examine the gate drive driving capability, protection features, MOSFET on/off transient details and estimate the bus bar leakage inductance.

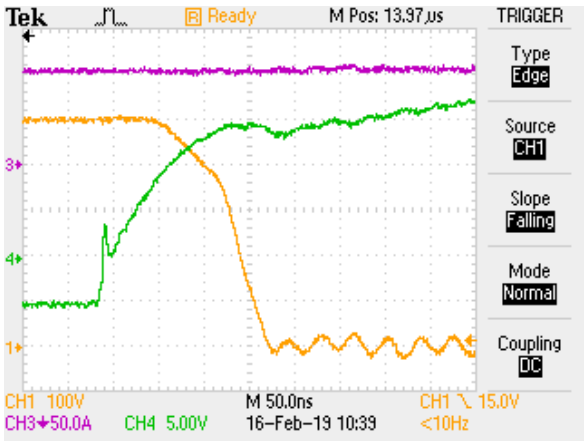
In Fig 2-15, Ch1 is Vds, Ch3 is inductor current, and Ch4 is the Vgs. Fig 2-15 (a) Shows the double pulse results, (b) shows the turn on and the turn off detail. The gate drive can switch at 500V DC bus with 120A in the switch. (c) and (d) extends closer look at the ON/OFF transient, from which the turn on time can be found as 170ns and turn off time as 250ns.



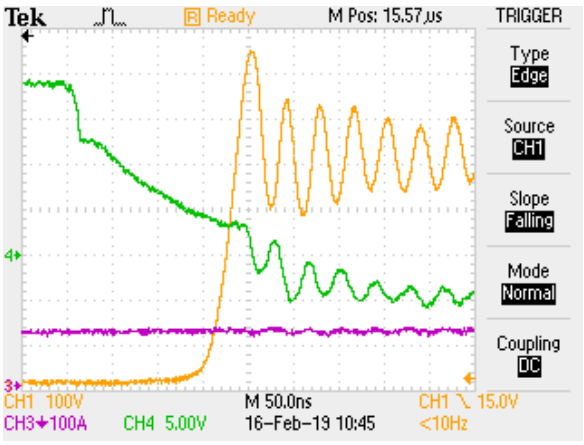
(a)



(b)



(c)



(d)

Figure 2- 15 Lower MOSFET Double pulse test result

In order to examine the bus bar leakage inductance, the drain current from the MOSFET is measured using Rogowski coil. Due to the package limitation of the SiC power module, the double pulse test will be performed on the upper switch as shown in Fig 2-16. To avoid the inductor saturation problem during high current test, air core inductor is adopted.

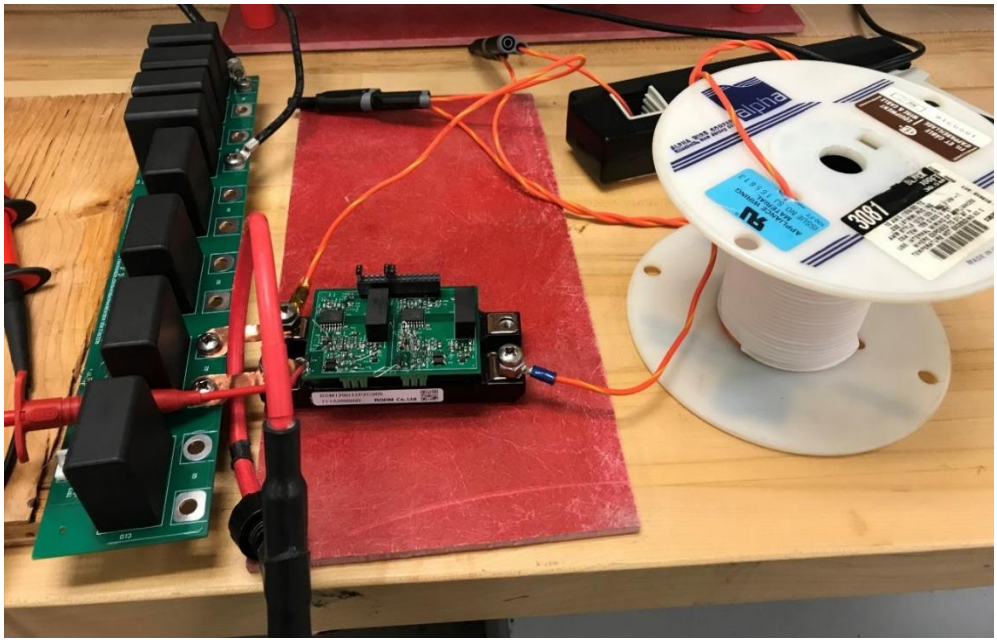
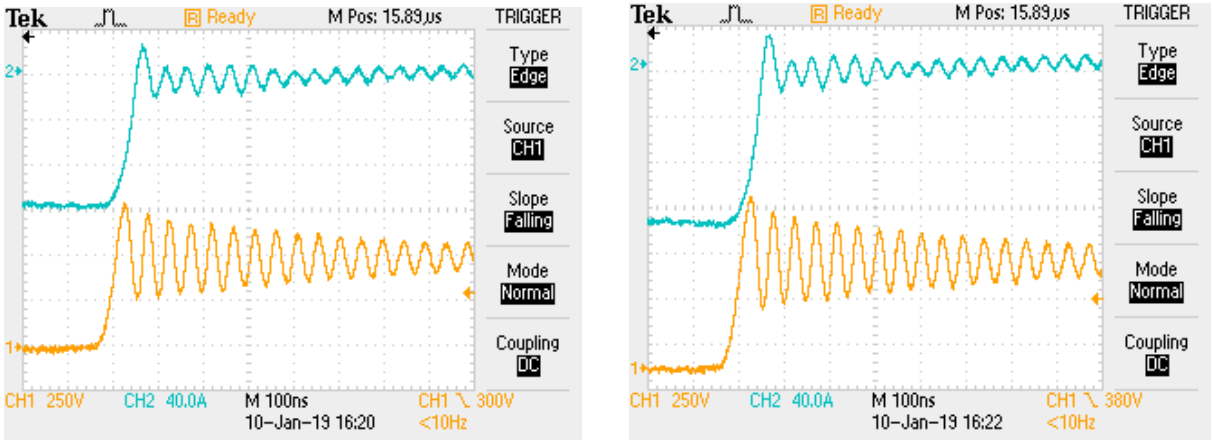


Figure 2- 16 Upper MOSFET Double pulse test setup



(a) **(b)**

Figure 2- 17 Vds and Drain Current

In Fig 2-17, Ch1 is the upper switch Vds, Ch2 is the current (notice the polarity). Loop inductance can be calculated by finding the sharpest di/dt and the corresponding ΔV ($\Delta V = L\frac{di}{dt}$). Estimated loop inductance is 100nH.

2.2.4 Gate drive protection feature

Under voltage lockout (UVLO): When the IC detects the primary side Vdd1 is below 2.3V, the “Ready” pin will be driven to Low. When the IC detects the secondary side Vdd2 is below 11V, the “Ready” pin will be drive to Low. This is not a latched fault, when the voltage is above the threshold level, the IC will be Ready again.

Desat protection: Desat is used to detect the over current fault inside the MOSFET. The principle is that the Vds across the MOSFET when the device is conducting current will show different values depending the current conducting. And this voltage value can be used in the desat protection loop to help indicate and detect whether there is over current happening. This relationship between current and voltage can be found in the I-V curve as shown in Fig 2-18.

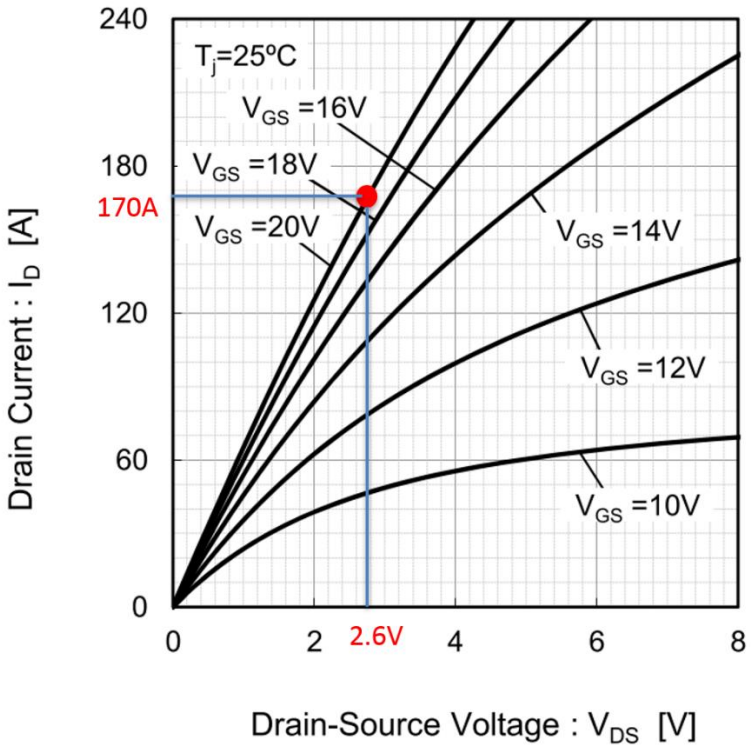


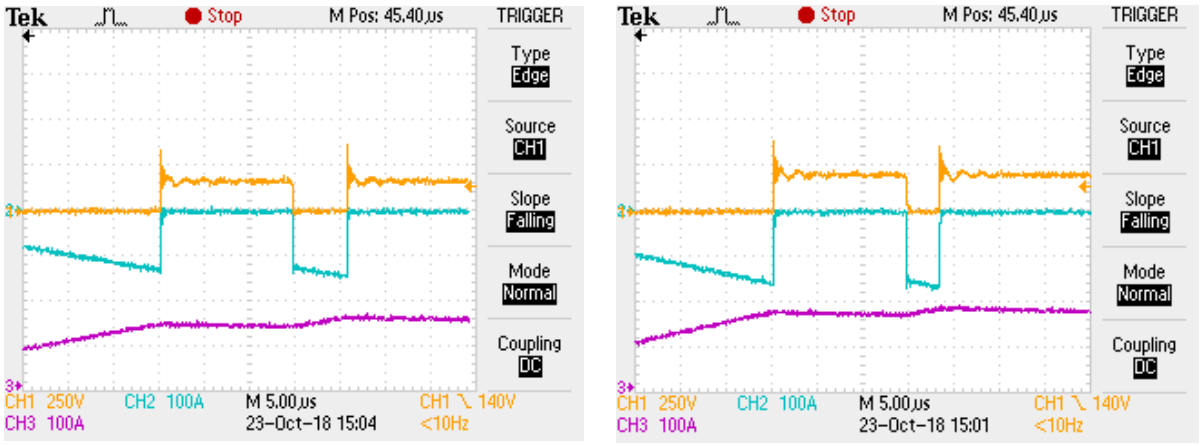
Figure 2- 18 I-V electrical output characteristics

The designed desat trigger level is 170A and the 2.6V Vds can be found correspondingly. When the ON signal is applied to the gate drive, the internal desat comparator is enabled. When the pin "Desat" detects 9.4V(set by the IC), fault will be triggered. However, there is 6.8V difference between the IC threshold value. R9, R7, Z2 and D2 will compensate that difference. Here is how:

$$V_{Z2} + V_{D2} + V_{R9} = 3.9V + 0.6V + \left(\frac{19V-4.5V}{3k\Omega} + 500\mu A\right) * 470\Omega = 7\text{V} \quad (2\text{-}3)$$

(close to 6.8V, considering the components tolerance)

To verify the desat trigger level, double pulse test is performed. The pulse width is designed to incur 170A during the middle of the second pulse. Test results are summarized in Fig 2-19. Fig 2-19 (a) shows that 150A can not trigger the fault and the second pulse runs completely for 5us. Fig 2-20 (b) demonstrates that the during the middle of 2nd pulse, 170A is reached and the 2nd pulse stops the middle which indicates the gate drive shunts down the gating.



(a) **(b)**

Figure 2- 19 Desat trigger level verficiation

Active miller clamping:

With high speed switching used in high voltage/power system, extra caution needs to be placed on the CMTI performance of the gate drive. For example, when the lower switch is off and the upper switch is turning on, there exists high dv/dt which will be imposed upon Cgd. The dv/dt will incur current (Active miller current) through Cgd and effectively generate voltage spike after Rg on Q1's gate reference to Vee. This process is shown in Fig 2-20.

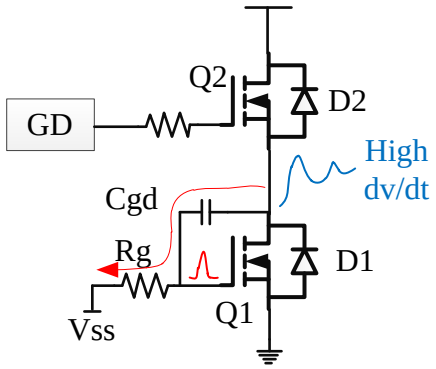


Figure 2- 20 Active miller current injection

Active miller clamping feature will be very important when the voltage spike is above switch threshold voltage. Hence, the IC selected has a 2V trigger level, which means that when Gate_sense gets above 2V when the switch is supposed off. The clamp switch inside IC will clamp the gate voltage to ground preventing false turning on. This protection also helps the elimination of 'cross-talk' shoot-through.

In this design, the peak DC bus voltage will be 700V and the top switching speed will be 200kHz, the effective dv/dt is 3.5kV/us. The gate drive selected has a CMTI up to 100kV/us.

2.3 Controller board and controller interface board

2.3.1 DSP control board

In this project, TI launch pad [62] is used as the DSP control platform, since it can provide 16+ PWM and 10+ ADC channels.

The ADC range is 0~3V and additional sensor feedback signal conditioning is needed to process and do the level shifting before being sent to ADC.

The PWM voltage level is 3V and the gate drive needs 3.5V to be recognized as High. Hence level shifting is required before PWM signal being sending to gate drive.

2.3.2 Sensors in the prototype

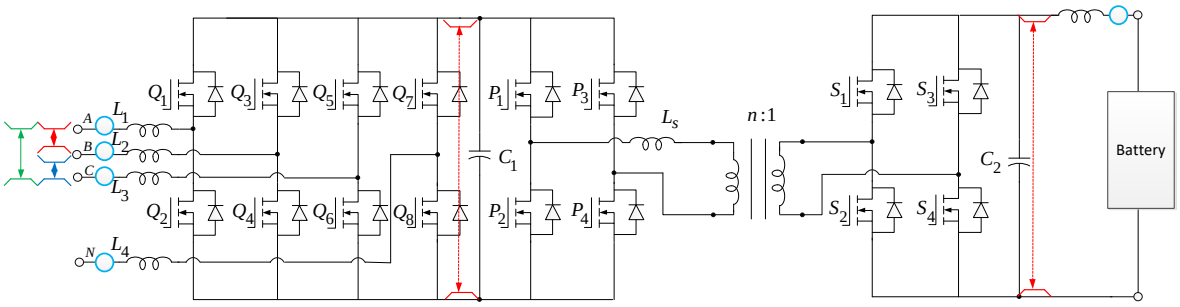


Figure 2- 21 Sensors in the system

To fully control the system, there are 5 current sensors and 5 voltage sensors whose placement are shown in Fig 2-21.

Current sensors: LEM LA205-S is used to sense the current, the sensors output is connected to a signal conditioning circuits shown in Fig 2-22.

The output of the current sensor is also current whose conversion ratio is 1:2000, and the peak sensing current is set to be 150A. After passing through R160 ~ R163, Vac will be imposed on R159. Applying superposition of op-amp:

Assuming 1.5V -> 0:

$$V_3 = V_{ac}\frac{R_{158}}{R_{158}+R_{159}} \tag{2-4}$$

$$V_{o1} = V_3(1+\frac{R_{164}}{R_{165}}) \tag{2-5}$$

Assuming V_{dc} -> 0:

$$V_3 = 1.5\frac{R_{158}}{R_{158}+R_{159}} \tag{2-6}$$

$$V_{o2} = V_3(1+\frac{R_{164}}{R_{165}}) \tag{2-7}$$

In the end, the output voltage being sent to ADC is:

$$V_1 = V_{o1} + V_{o2} = V_{ac} + 1.5 \tag{2-8}$$

Hence, the signal sent to ADC will be a votlage signal whose amplitude is 3V and middle point is 1.5V.

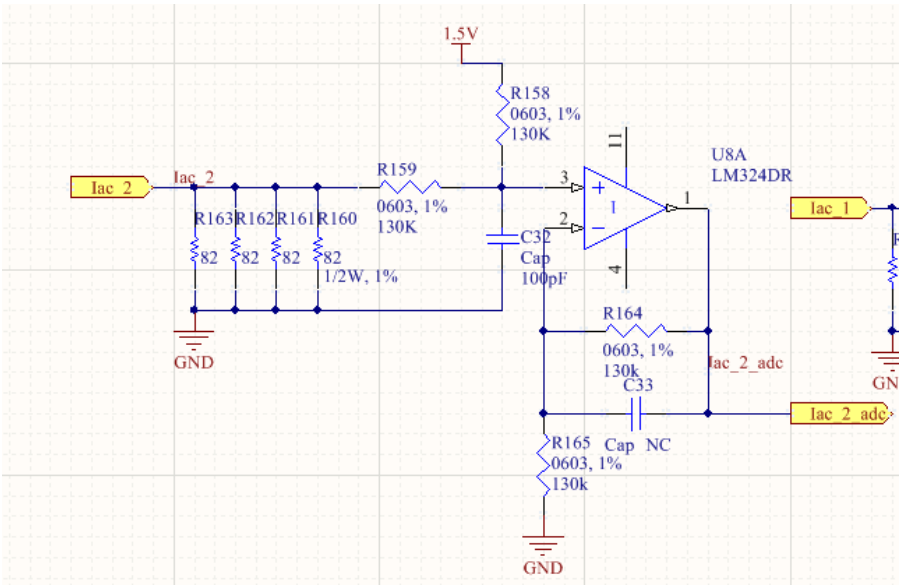


Figure 2- 22 Current sensor signal conditioning circuit

AC Voltage sensors: The high voltage has been converted to a low voltage signal after being divided through a series of resistor.

The signal condition circuit is shown in Fig 2-23.

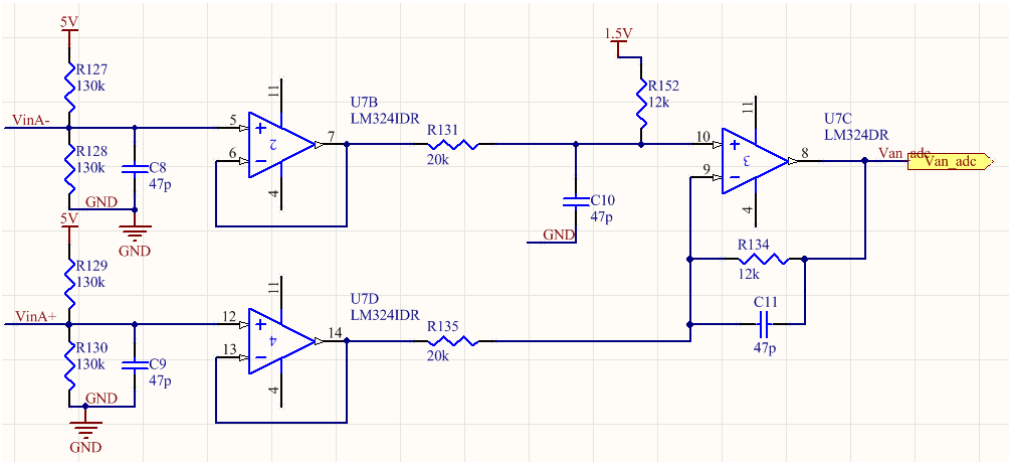


Figure 2- 23 AC Voltage sensor signal conditioning circuit

Applying superposition of op-amp:

$$V_7 = V_{inA-} + 5 * \frac{R_{127}}{R_{127}+R_{128}} = V_{inA-} + 2.5 \quad (2\text{-}9)$$

$$V_{14} = V_{inA+} + 5 * \frac{R_{129}}{R_{129}+R_{130}} = V_{inA+} + 2.5 \quad (2\text{-}10)$$

Assuming V_7 -> 0:

$$V_+ = 1.5\frac{R_{152}}{R_{152}+R_{131}} \quad (2\text{-}11)$$

$$V_{o1} = \frac{1.5*\frac{R_{152}}{R_{152}+R_{131}} - (V_{inA+}+2.5)*\frac{R_{131}}{R_{152}}}{1+\frac{R_{134}}{R_{135}}} \quad (2\text{-}12)$$

Assuming V_{14} -> 0:

$$V_+ = \frac{V_{inA-}+2.5-1.5*\frac{R_{131}}{R_{152}}}{1+\frac{R_{131}}{R_{152}}} \quad (2\text{-}13)$$

$$V_{o2} = \frac{V_{inA-} + 2.5 - 1.5 * \frac{R_{131}}{R_{152}}}{1 + \frac{R_{131}}{R_{152}}} * (1 + \frac{R_{134}}{R_{135}}) \quad (2\text{-}14)$$

In the end, the output voltage being sent to ADC is

$$V_{8-ac} = V_{o1} + V_{o2} \quad (2\text{-}15)$$

DC Voltage sensors: The high voltage has been converted to a low voltage signal after being divided through a series of resistor.

The signal condition circuit is shown in Fig 2-24.

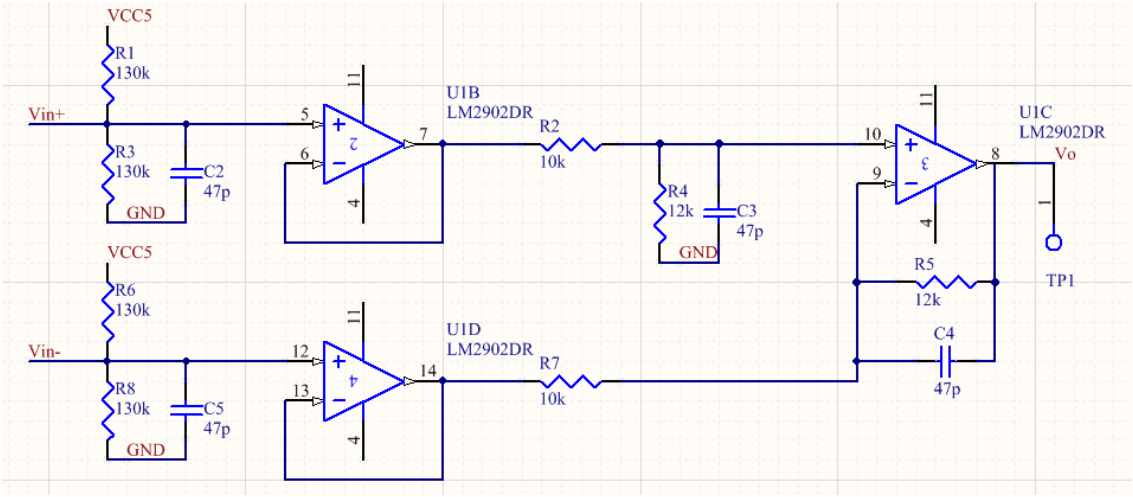


Figure 2- 24 DC Voltage sensor signal conditioning circuit

Applying superposition of op-amp:

$$V_7 = V_{inA-} + 5 * \frac{R_{127}}{R_{127} + R_{128}} = V_{in+} + 2.5 \quad (2\text{-}16)$$

$$V_{14} = V_{inA+} + 5 * \frac{R_{129}}{R_{129} + R_{130}} = V_{in-} + 2.5 \quad (2\text{-}17)$$

Assuming V_7 -> 0:

$$V_+ = 0 \quad (2\text{-}18)$$

$$V_{o1} = -\frac{R_5}{R_7} * (V_{in-} + 2.5) \quad (2\text{-}19)$$

Assuming V_{14} -> 0:

$$V_+ = (V_{in+} + 2.5) * \frac{R_2}{R_2+R_4} \quad (2\text{-}20)$$

$$V_{o2} = [(V_{in+} + 2.5) * \frac{R_2}{R_2+R_4}] * (1 + \frac{R_5}{R_7}) \quad (2\text{-}21)$$

In the end, the output voltage being sent to ADC is

$$V_{8-dc} = V_{o1} + V_{o2} \quad (2\text{-}22)$$

2.3.3 Interface board between DSP and Gate drive boards

This interface board in Fig 2-25 carries other functions such as:

- Signal routing bridge between the control board and the gate drive boards;
- Provide 24V and 5V to the gate drive boards;
    - Off-shelf isolated 5V-12W, 24V-50W and ±15V-6W power supplies are used on this board [63] ~ [65].
- LED indications of gate drive status;
- Power supply for all the auxiliary circuits.

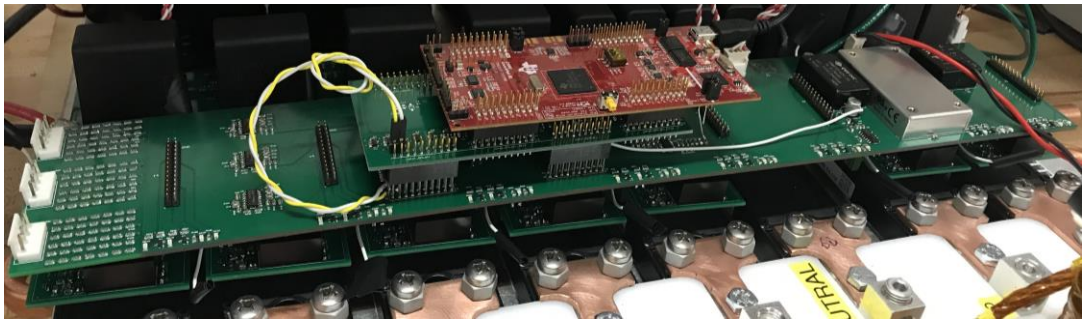


Figure 2- 25 Digital control system: control card and interface board

2.4 DC link capacitors selection

One of the challenges in the universal converter design is that the DC bus should be able to accommodate different working modes such as single-phase AC or three phase AC and handle various level of ripple current such as switching ripple and 2ω ripple. Hence, hybrid bus bar is designed to host all the operation modes as shown and highlighted in Fig 2-27.

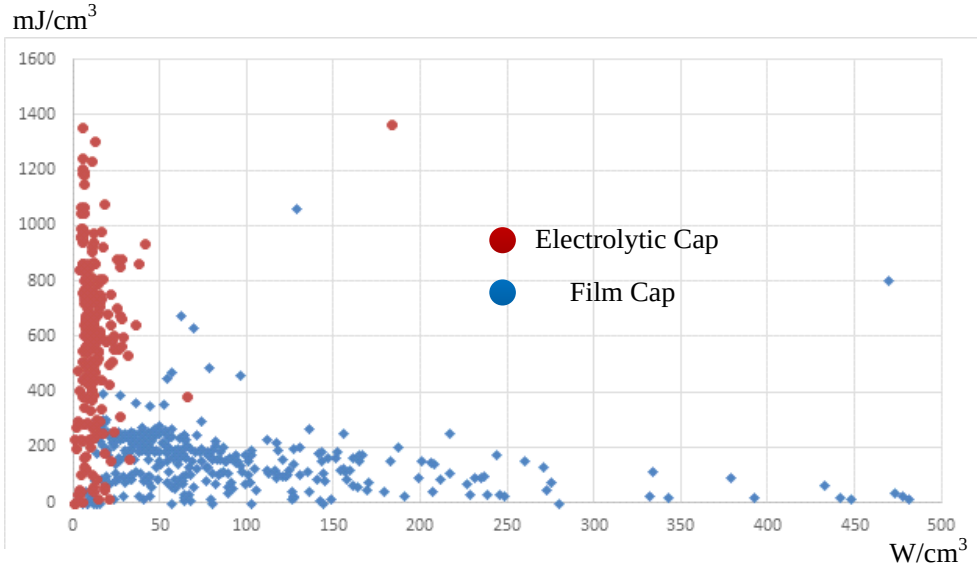


Figure 2- 26 Energy density VS Power density (Electrolytic Cap and Film Cap)

To summarize, electrolytic caps are higher energy density compared to film cap and film caps are higher power density which means have higher ripple current rating as shown in Fig 2-26 which is generated from datasheet of different manufacturer by web crawling script.

Electrolytic caps are better option to absorb the 2ω ripple power, and film caps with low ESL and ESR are considered to absorb the high switching ripple power. From Table 2-2, the DC link caps needs to handle at least 700V.

Another important information for the DC link caps selection is the voltage on the DC bus since the converter needs to work under different operation modes which are summarized in Table 2-2. The power level is defined per the design requirement.

Case	Applications	Power level	DC Bus Voltage Peak
A	120V Single Phase AC	3.2kW (Level 1)	$120 * \sqrt{2} = 170V$
B	240V Single Phase AC	7.8kW (Level 2)	$240 * \sqrt{2} = 339V$
C	208V Three Phase AC	20kW (Level 2)	$208 * \sqrt{2} = 294V$
D	480V Three Phase AC	25kW (Level 2)	$480 * \sqrt{2} = 678V$
E	48V DC	10kW	400V

Table 2- 2 Operation modes

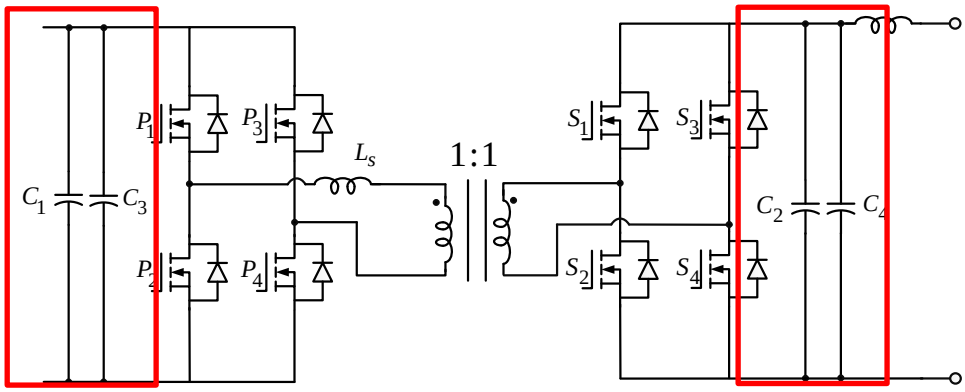
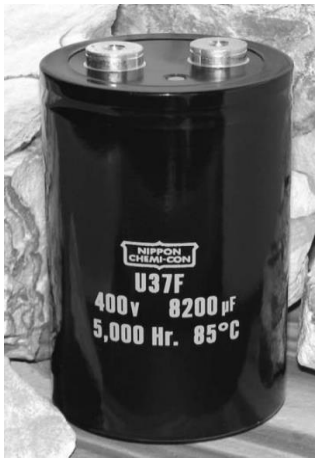


Figure 2- 27 Hybrid DC link capacitors



(a) **(b)**

Figure 2- 28 Electrolytic cap and Film Cap

2.4.1 Electrolytic Capacitors bus bar

2ω capacitance needed can be found in [36], [57] ~ [61].

$$E = \frac{P_{dc}}{2\pi f_{line}} = \frac{1}{2}CV_{max}^2 - \frac{1}{2}CV_{min}^2 = C \times \frac{1}{2}(V_{max} + V_{min}) \times (V_{max} - V_{min}) \quad (2\text{-}23)$$

$$C_1 = \frac{P_{1\emptyset}}{2\pi f_{line} V_{dc} \Delta V_{dc}} = \frac{7.2kW}{2*3.14*60Hz*340V*(5\%*340V)} = 3300uF \quad (2\text{-}24)$$

To leave some margin, two 6800uF caps [50] are put in series as C1. C2 has the same capacitance value while theoretically there will be no 2w ripple and no need for more caps. If the DC bus voltage can be boosted to a higher value, the required capacitance is smaller.

Ripple current:

$$i_{ripple} = \frac{p_{2\omega}}{V_{dc}} = \frac{-V_s I_s \cos(2\omega t)}{V_{dc}} = -17.33\cos(2\omega t)\ \text{A} \quad (2\text{-}25)$$

$$I_{ripple}RMS = \frac{17.33}{\sqrt{2}} = 12.25\ \text{A} \quad (2\text{-}26)$$

The electrolytic caps selected has ripple current of 18.6A which has enough safe margin.

The electrolytic caps are shown in Fig 2-28(a) and electrical characteristics are summarized in Table 2-3.

Parameter	**Value**
Voltage rating	450V
Capacitance value	6800uF
Ripple current	18.6A
ESR	15mΩ

Table 2- 3 DC link electrolytic cap specs

2.4.2 Film Capacitors bus bar

Switching current ripple absorption capacitance needed can be found in:

$$C_{3,\min} = \frac{P_{load}}{\eta f_{sw}\left(2V_{dc}\square v_{dc} + \square v_{dc}^2\right)} = \frac{25\times10^3}{100\%\times50\times10^3\times\left[2\times700\times700\times5\% + \left(700\times5\%\right)^2\right]} = 10\ \mu\text{F} \quad (2\text{-}27)$$

$$C_{4,\min} = \frac{P_{load}}{\eta f_{sw}\left(2V_{dc}\Delta v_{dc} + \Delta v_{dc}^2\right)} = \frac{25\times10^3}{100\%\times100\times10^3\times\left[2\times350\times350\times5\% + \left(350\times5\%\right)^2\right]} = 18\ \mu\text{F} \quad (2\text{-}28)$$

Ripple current:

$$I_{RMS(C3)} = \frac{2S_{load}}{V_{dc}} = \frac{2\times25\times10^3}{700} = 72\ \text{A} \quad (2\text{-}29)$$

$$I_{RMS(C4)} = \frac{2Q_{transformer}}{V_{dc}} = \frac{2\times25\times10^3\times50\%}{350} = 70\ \text{A} \quad (2\text{-}30)$$

The film caps are shown in Fig 2-28(b) and electrical characteristics are summarized in Table 2-4.

Hence, the primary side needs at least 7 of such capacitors in parallel to absorb the total switching ripple.

The secondary side needs 5 of such capacitors to able to absorb the total switching ripple currents.

Parameter	Value
Voltage rating	1000V
Capacitance value	20uF
Ripple current	14A
ESR	7mΩ

Table 2- 4 DC link film capacitor specs

2.5 Transformer design

The transformer in this unit serves several purposes:

(1) galvanic isolation to protect the battery from the load/grid.

(2) use leakage inductance as energy transfer component.

(3) voltage turns ratio to change voltage and power transfer relationship

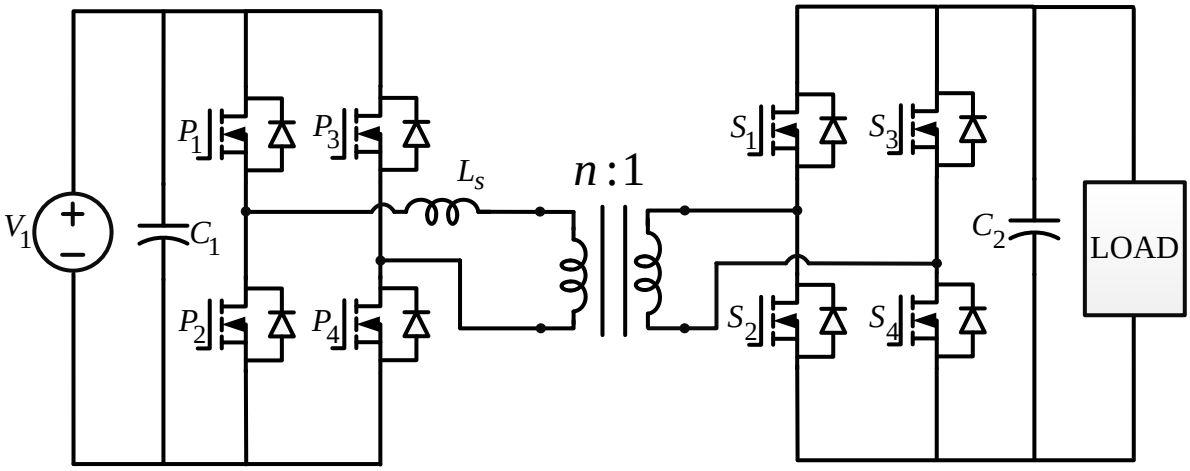


Figure 2- 29 Dual active bridge

The maximum power transfer inside the DAB [27] from V1 to load is given by

$$P = \frac{nV_1V_2}{8L_sf_{DAB}} \tag{2-31}$$

Some observation can be made (1) larger leakage inductance and switching frequency leads to smaller power transfer; (2) larger turns ratio results in higher power transfer.

Hence, transformer design specs need additional efforts which are explained in the following sections.

2.5.1 Single phase shift vs Dual phase shift

Single Phase Shift (SPS)

Single phase shift means that there is a phase shift D ($D = \frac{\emptyset}{\pi}$) between the primary H bridge and secondary H bridge. Both H bridge legs are 50% duty ratio with no inner phase shift between the legs in one H- bridge. And this would lead to two level voltage waveforms across the transformer windings. Fig 2-30 shows the simplified model of DAB.

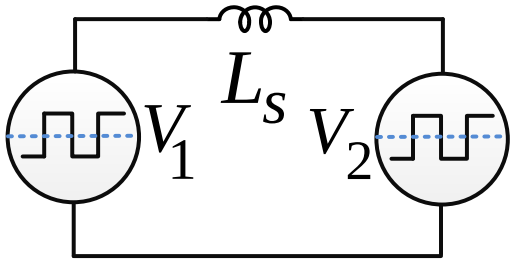


Figure 2- 30 Power Flow Model of SPS

Fig 2-31 presents a typical operating cycle of DAB. V1 is 700V, V2 (battery voltage) is 350V, the leakage inductance Ls is assumed to be 10uH, the switching frequency is 100kHz, and the transmitted active power is 25kW which is the case D in Table 2-2.

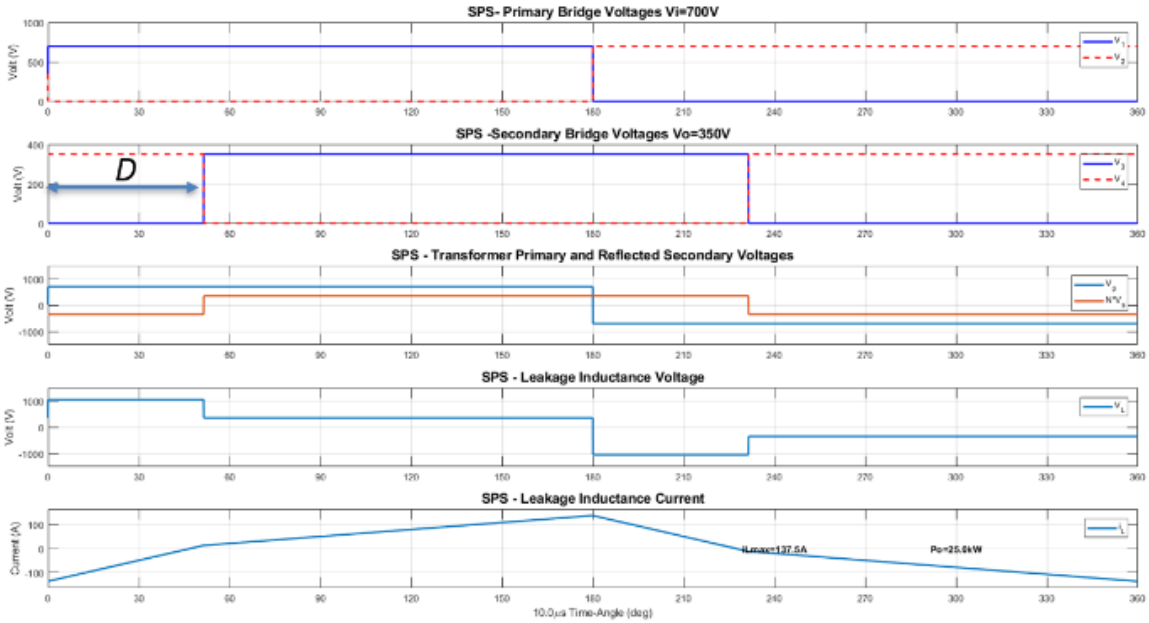


Figure 2- 31 Gating Signals and Voltage/Current Waveforms of SPS

The transmitted power with SPS [27] is summarized in

$$P = \frac{NV_iV_o}{2f_sL_s}D(1-D) \tag{2-32}$$

Dual Phase Shift (DPS)

Dual phase shift means that there is a phase shift D2 between the primary H bridge and secondary H bridge. Both H bridge legs are 50% duty ratio with an inner phase shift D1 between the legs in one H- bridge. And this would lead to three level voltage waveforms across the transformer secondary windings. Fig 2-31 shows the simplified model of DAB. Fig 2-32 presents a typical operating cycle of DAB under DPS.

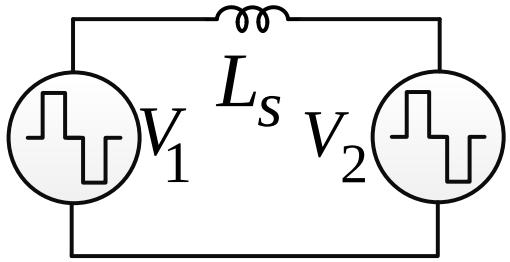


Figure 2- 32 Power Flow Model of DPS

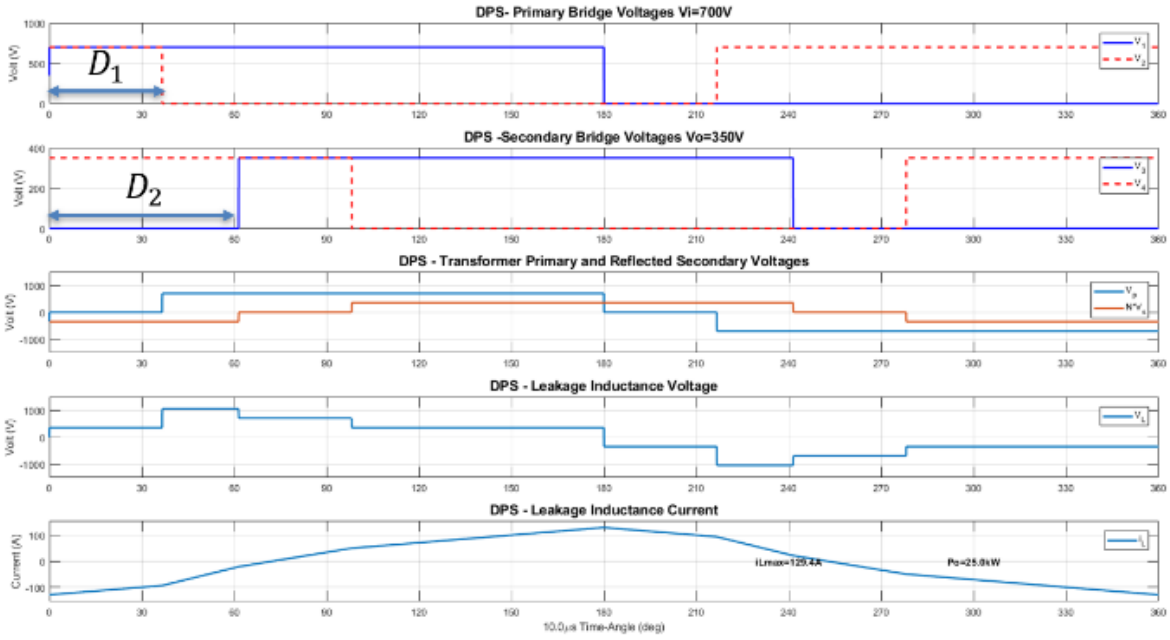


Figure 2- 33 Gating Signals and Voltage/Current Waveforms for DPS

The transmitted power is documented in these two equations

$$P = \frac{NV_iV_o}{2f_sL_s}\left[D_2(1-\mathrm{D}_2) - \frac{1}{2}D_1^2 \right](0 \le \mathrm{D}_1 \le \mathrm{D}_2 \le 1) \quad \text{(2-33-a)}$$

$$P = \frac{NV_iV_o}{2f_sL_s}\left[D_2(1-\mathrm{D}_1 - \frac{1}{2}D_2) \right](0 \le \mathrm{D}_2 \le \mathrm{D}_1 \le 1) \quad \text{(2-33-b)}$$

2.5.2 Turns ratio determination

In this converter, turns ratio is selected based on the minimum current stress under the peak power operating modes. Hence, the primary side voltage will be 700V (480V 3 phase)

Based upon previous sections conclusion, DPS is selected for relatively small current stress. And the maximum current [25] is shown in

$$i_{\max\_sps} = \frac{nV_2}{4f_sL_s}[\frac{V_1}{NV_2} - 1 + 2\mathrm{D}] \quad \text{(2-34)}$$

$$i_{\max\_dps} = \frac{NV_2}{4f_sL_s}[(\frac{V_1}{NV_2} - 1)(1-\mathrm{D}_1) + 2\mathrm{D}_2] \quad \text{(2-35)}$$

This converter needs to deliver the rated power over a wide range of battery voltage for example, 275V ~ 375V. The algorithm for finding optimal turns ration over this range is show in Fig 2-34.

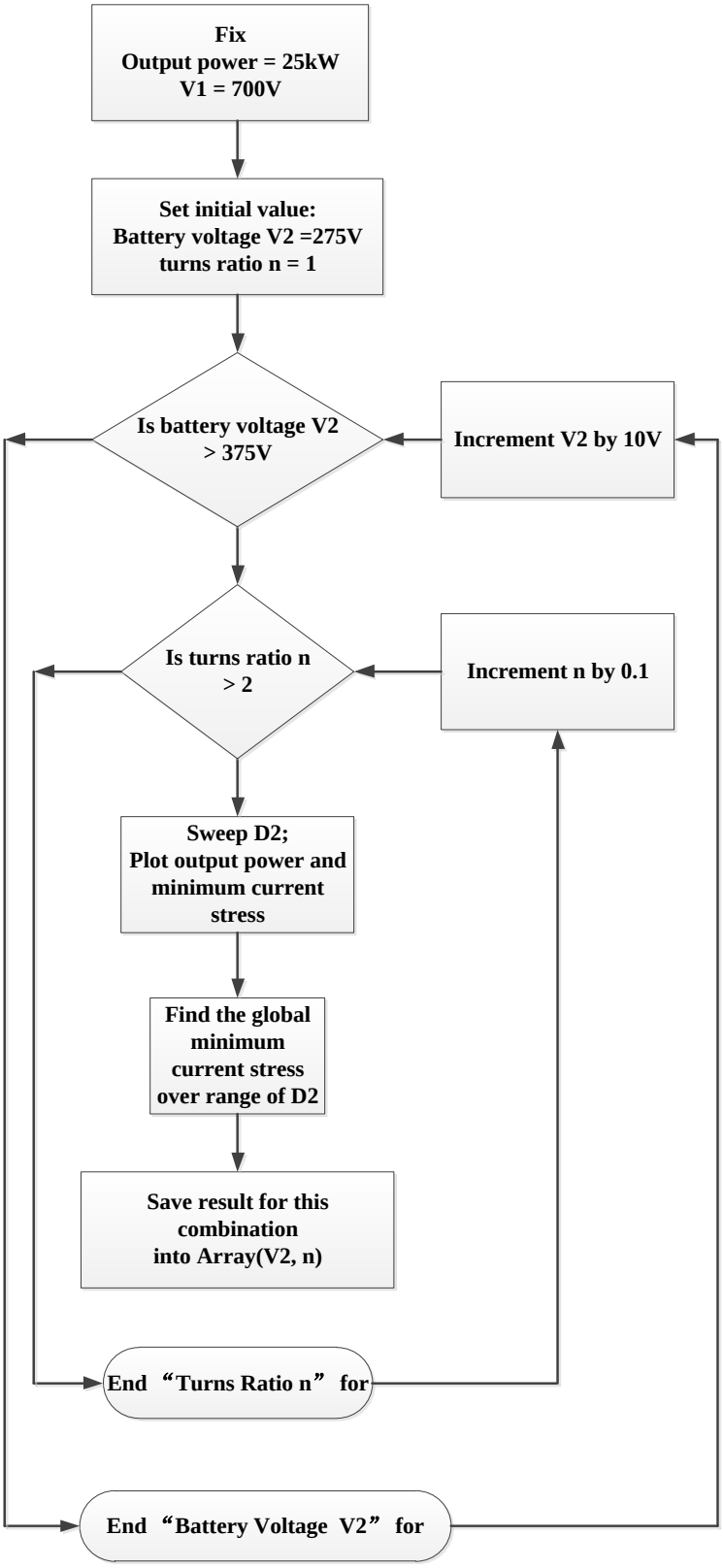


Figure 2- 34 Algorithm flowchart for optimal Turns ratio for minimum current stress

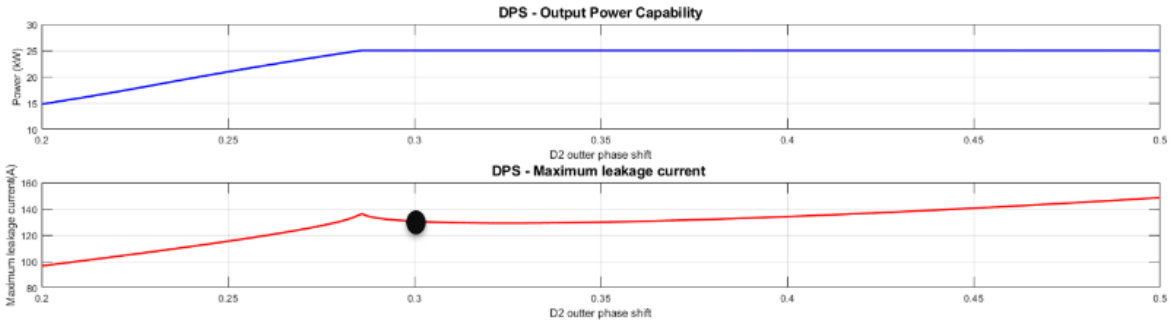


Figure 2- 35 Minimum Current Stress at one operating point.

The black dot in Fig. 2-35 is the minimum current for one operating point (P = 25kW, V2= 300V, n = 1)

Fig 2-36 is the plot for the summary of Array(V2, n) in Figure 2-34. The x-axis is the battery voltage and the y-axis is the current stress. There are total ten curves from n = 1 to n =2.

There is a red line which indicates the current limit of the SiC switch. In this design, 130A is chosen. Only the curves with all data points under the red curve can be valid solutions, and it only leave turns ratio 1 or 1.1 as the options. In order to have equal current stress and switching loss on both sides, N is chosen to be 1.

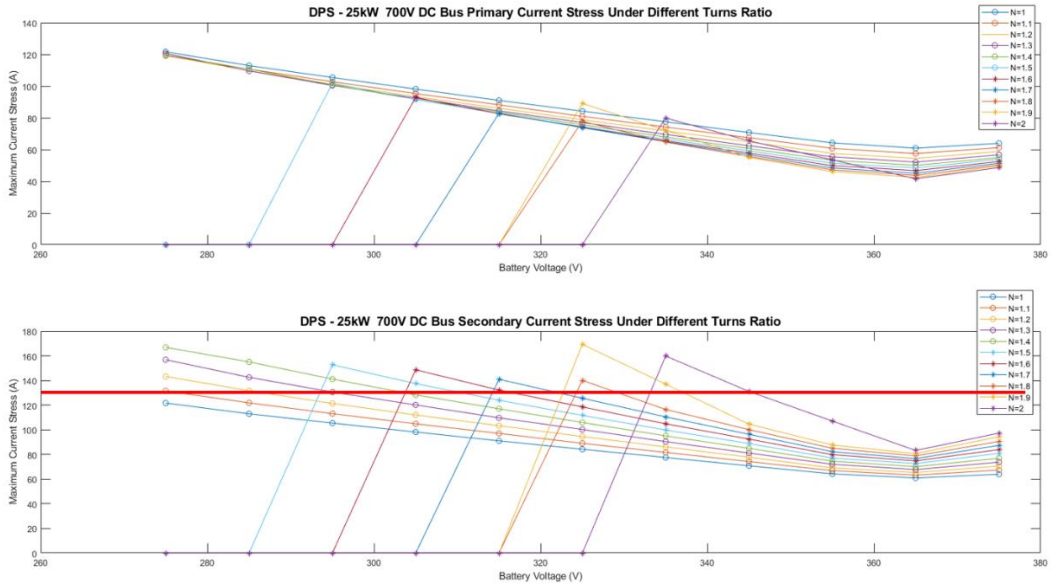


Figure 2- 36 Turns ratio vs Current Stress over Battery Voltage range.

2.5.3 Core Flux waveform

There is one equation (3) known as the transformer equation, where n is the number of turns, A is core are, B is the flux density, K = 4.44 (sine excitation) and K = 4 (square excitation).

$$V = KnBAf_s \tag{2-36}$$

It shows the relationship between core flux density and winding voltage. However, in DAB circuit, the transformer is not seeing either sine excitation or square wave. In this thesis, T-shape transformer model is used for transformer design and analysis as shown in Fig.2-37. Since N =1, total leakage inductance is distributed evenly on both sides. And magnetizing inductance is assumed to be 500uH. When using this T-shape model, design can be more generalized regardless of excitation waveform.

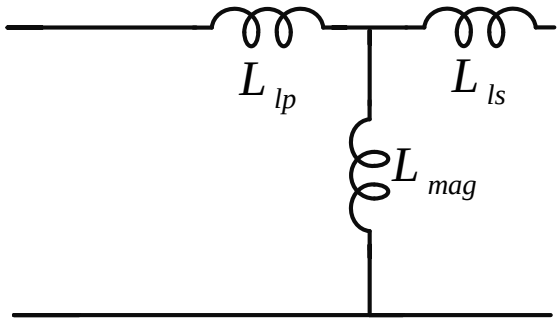


Figure 2- 37 Transformer T-Shape Model

After using the T model in Simulink, the voltage across the magnetizing inductance can be found in Fig. 2-38.

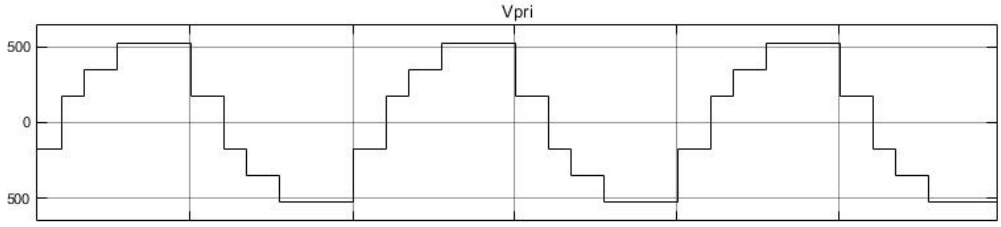


Figure 2- 38 Core Flux Shape Under DPS

With the core flux information, the transformer design process can be started.

2.5.3 Design Steps

The procedure will be summarized below in the flow chart below in Fig 2-39:

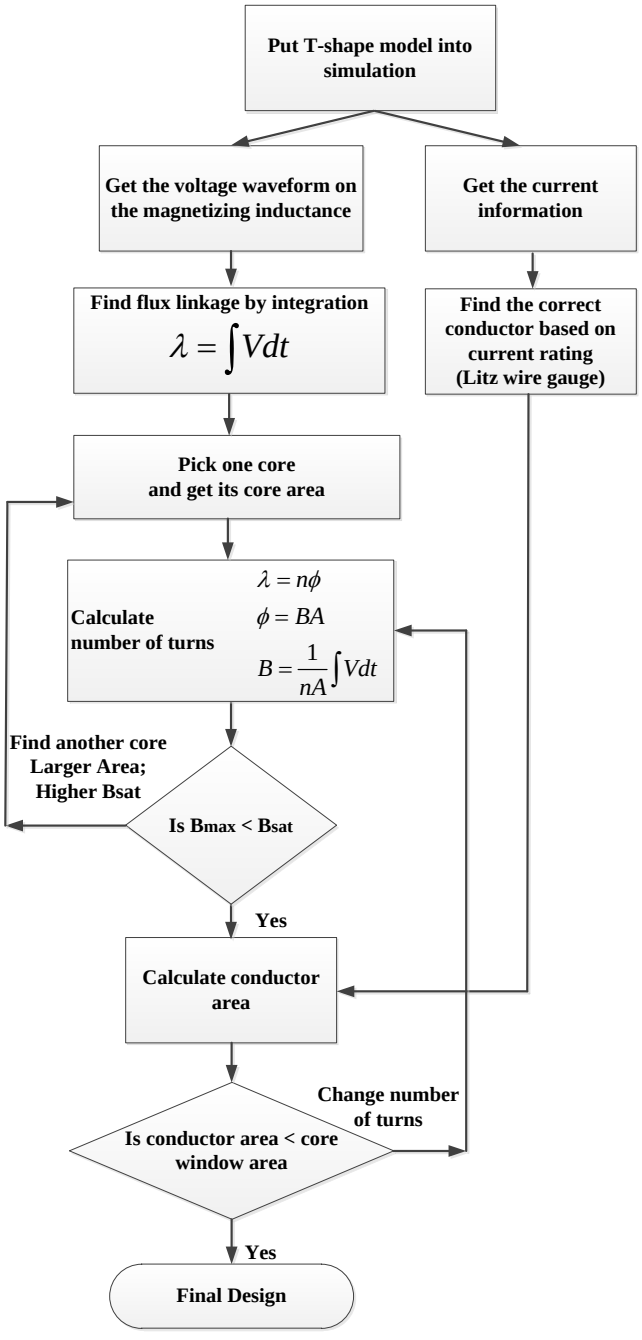


Figure 2- 39 Generalized transformer design flowchart

2.5.4 Design example:

In order to achieve smaller size, higher saturation flux magnetic material is used. Since the DAB is switching at high frequency, low core loss is curial to improve the efficiency. Comparison of different magnetic material is summarized in previous work [61]. The design specs are listed in table 2-5.

Design Specs	Value
Voltage rating	700V
Current rating	130A
Leakage inductance	10uH
Operating frequency	100kHz

Table 2- 5 Transformer design specs

In this design, nanocrystalline material FINEMET F3CC0125 core from Hitachi [47] is used whose Bsat is 1.23T and core loss is lower than silicon-steel commonly used in power transformer. The core area is 545mm^2, and this information can be applied to the algorithm above. The final selection of turns on each side is 10. This results in Bmax is 0.5T which is smaller than Bsat. And the accumulated wire conductor area is less than the window area. This proves a valid design. The final core flux density is shown in Fig 2-40. Litz wire (6*3*45 AWG 38 braid) is adopted for reduction on high frequency proximity loss.

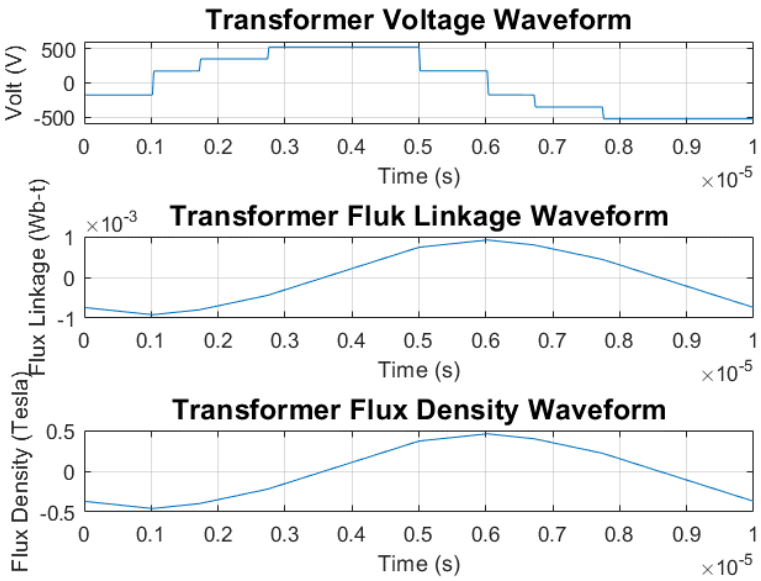


Figure 2- 40 Core flux waveform

2.5.5 Transformer test results

The final transformer assembly result is shown in Fig 2-41.

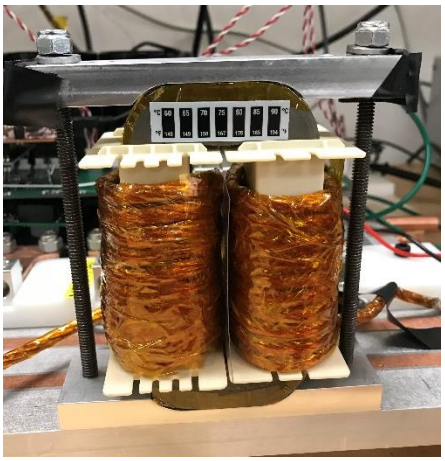


Figure 2- 41 Isolation transformer

The transformer's role is galvanic isolation, and high voltage insulation test between primary and secondary side is performed as shown in Fig 2-42.

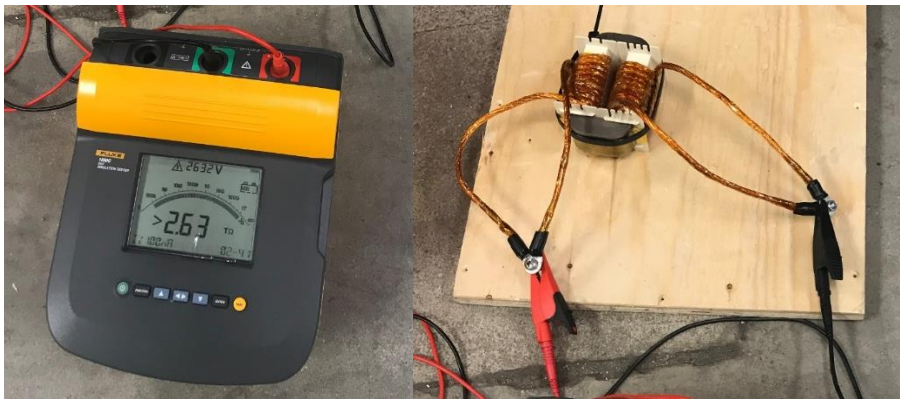
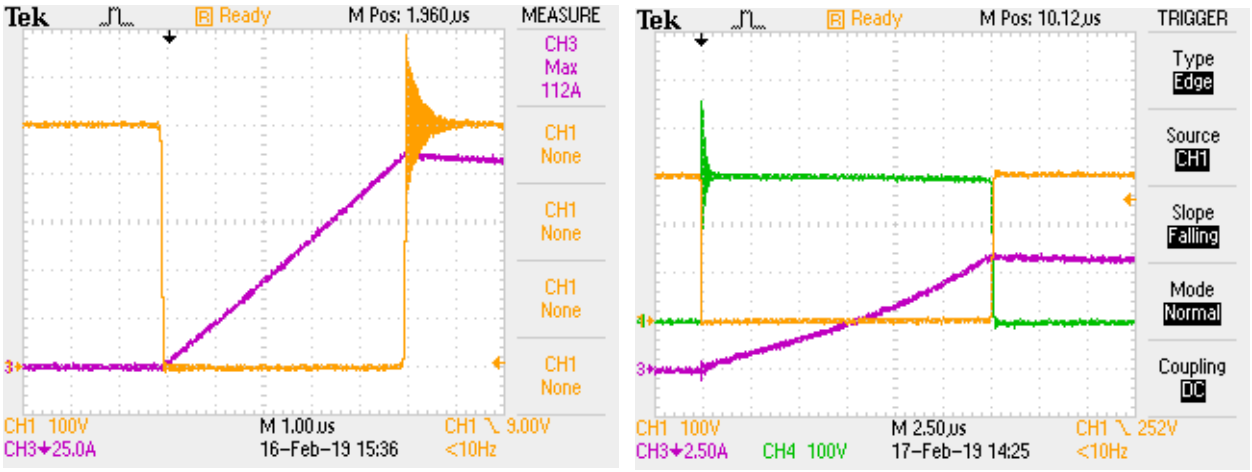


Figure 2- 42 Transformer isolation test

Insulation meter shows minimal leakage current under 2500V which verifies the insulation function.

In order to verify the performance and key parameters, short circuit and open circuit test are conducted whose results are shown in Fig 2-43.



(a) **(b)**

Figure 2- 43 Transformer parameter measurement

Fig 2 -43(a) is the short circuit test whose result indicates leakage inductance value. 22uH is measure result.

Fig 2 -43(b) is the open circuit test whose result indicates magnetizing inductance value and turns ratio. 750uH is measured result and the turns ratio 1:1 is also confirmed.

2.6 Filters design

2.6.1 Filter inductor design

Inductance value is calculated based on work [52] ~ [54]

$$L = \frac{V_{DC}}{6 f_{sw} \Delta i_{pp}} = 10\mu H \tag{37}$$

where f_{sw} is 100kHz * 2 since for 3 phase inverter the inductor is seeing twice the switching frequency;

Δi_{pp} is 10% of the rated current which is 0.1*30 = 3 A;

Vdc = 700V

Using the core selected [55] whose AL is shown in Fig 2-44

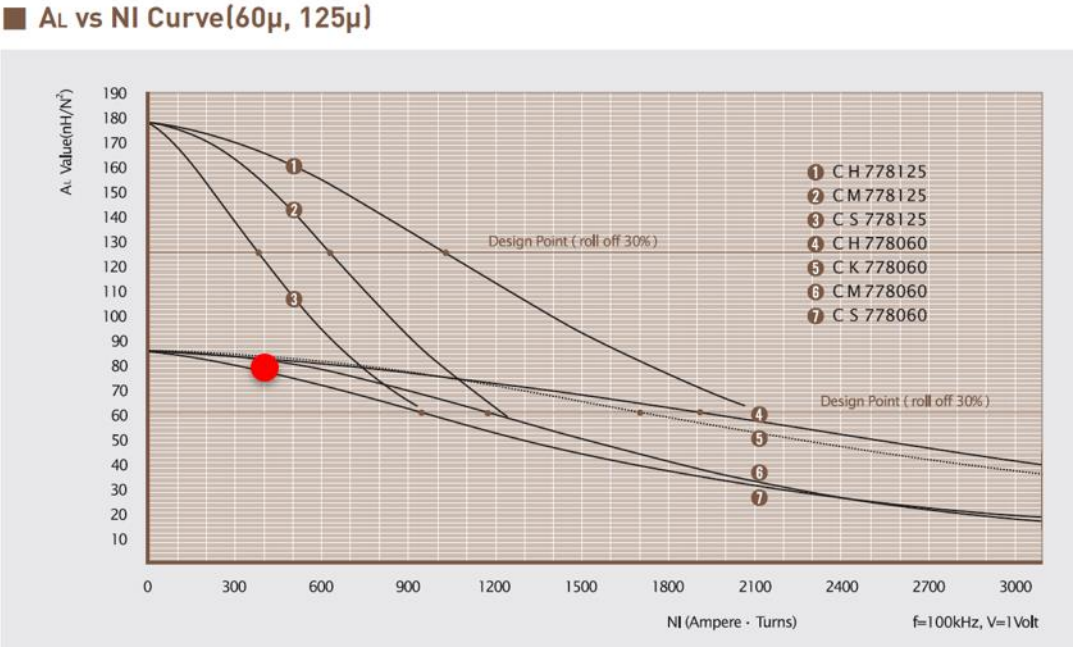


Figure 2- 44 Filtering inductor core AL value

$$L = A_L N^2 \ (@N = 11; I = 30A) = 9.9\mu H \quad (2\text{-}38)$$

2.6.2 Filter capacitor design

The filtering capacitance value is selected based upon the switching frequency f_{sw-inv} of the inverter. The LC filter cutoff frequency should be 1/10 of the f_{inv}.

$$f_{lc} = 0.1 f_{inv} = \frac{1}{2\pi\sqrt{LC}} => = C = \frac{1}{(2\pi f_{lc})^2 L} = 50uF \quad (2\text{-}39)$$

Hence AC film capacitor [56] is selected.

2.7 Complete prototype

The complete prototype is shown in Fig 2- 45

A bench power supply is used to provide auxiliary power needed for the converter. In this setup, a programmable DC source is used to represent the high voltage battery when the converter is operating as V2G and V2L modes. The setup is shown in Fig. 2-45 and Fig 2-46.

Additional caution needs to put when setting up the V2G, since it is equal to connecting two voltage sources together. Current limiting resistors are placed on both grid side and battery side. High voltage diode is inserted before the DC source to prevent current flowing back forward.

A relay is also adopted and will be closed after the phased-lock loop is stable.

Resistor load bank is adopted to simulate the high voltage battery when the converter is operating under G2V mode as shown in Fig. 2-47.

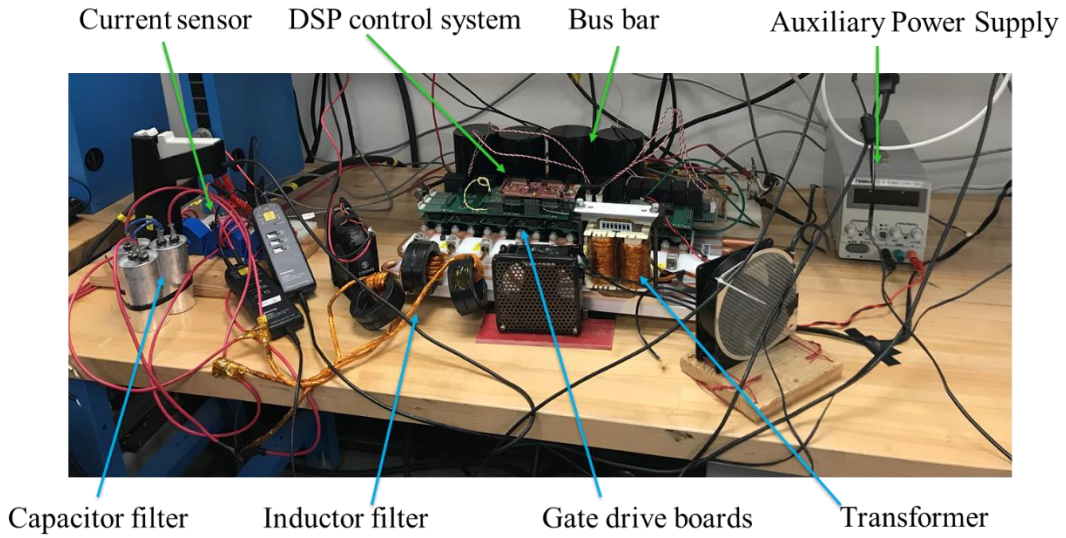


Figure 2- 45 Complete Prototype

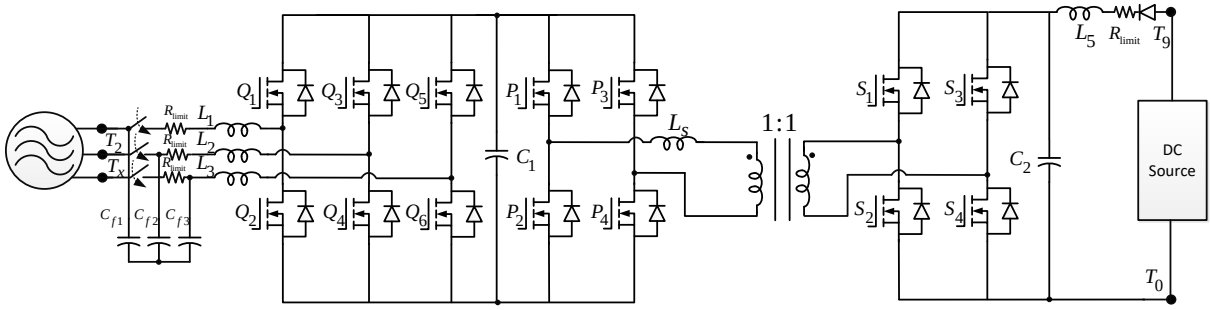


Figure 2- 46 V2G Test setup

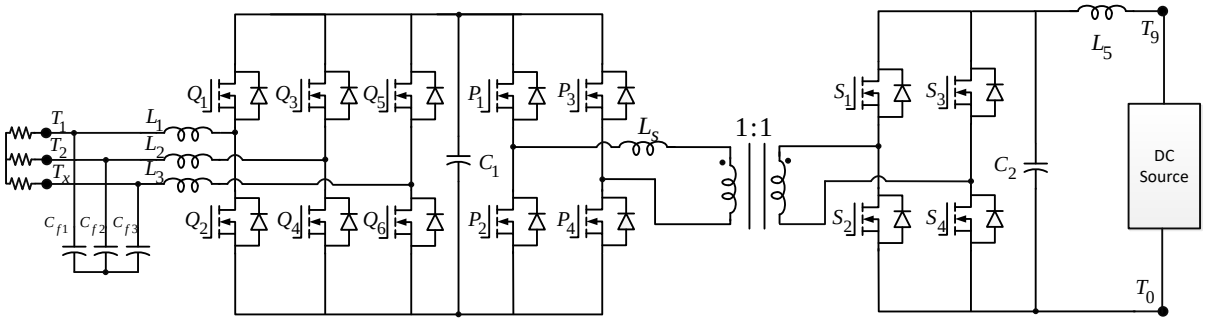


Figure 2- 47 V2L Test setup

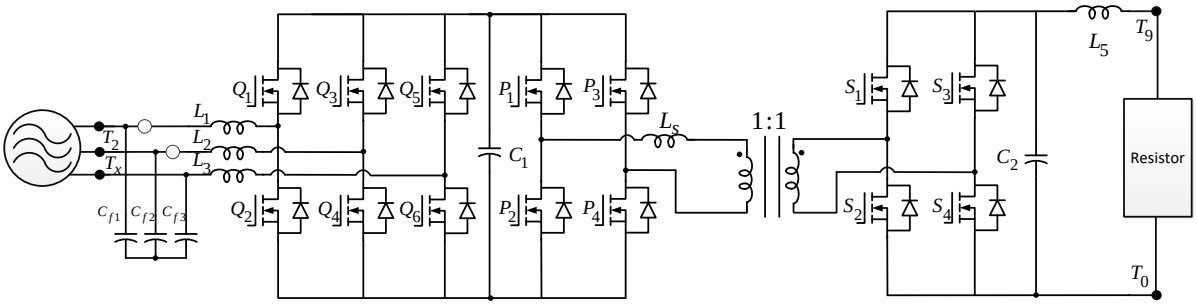


Figure 2- 48 G2V Test setup

Chapter 3 Vehicle to Load (V2L) analysis and control

3.1 Operation principle of V2L mode

In this operating mode, the power is flowing from the battery to the load. In the next generation smart-green home, V2L will be a very typical operating case, such as using the car's battery to power up the home appliance.

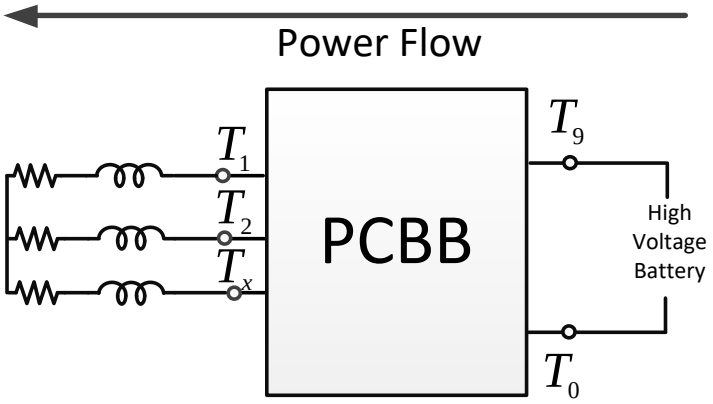


Figure 3- 1 V2L AC load

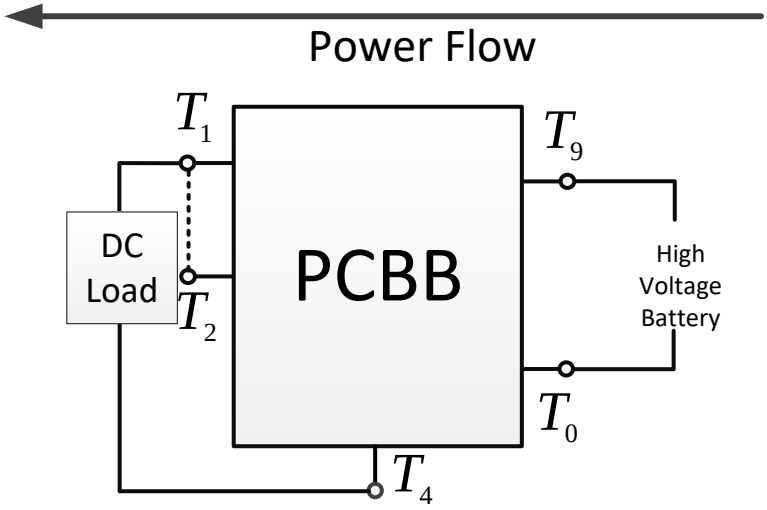


Figure 3- 2 V2L DC load

In this thesis, the AC load is assumed to be in linear nature which means the current will be sinusoidal as well and the current control will not be needed. However, it is common to see non-linear and unbalanced load such as diode rectifier. To regulate the voltage to under such load conditions will need more advanced control techniques and it is not discussed in this thesis. In the chapter 6, some future work and solutions related to this topic will be discussed.

The DC output operation will be able to provide 48V for some on-board appliance to use. Hence, in this thesis, the control will command the converter to generate 48V when the converter is controlled as an interleaved buck mode.

3.2 Control analysis of V2L mode

The converter consists of two stages DAB and inverter, and these two stages are decoupled from each other by the control which will allow separate control.

- DAB is responsible for transferring power from the battery and stabilizing the primary DC bus. Closed loop control on the primary DC bus voltage is needed. Since a 3400uF cap is placed which means a large time constant, a relatively slow control loop whose bandwidth is around 1kHz is high enough to regulate the voltage
- Inverter is providing the AC voltage to the load by doing the PWM on these phase legs. In this thesis. the most classical sine PWM is adopted. However, there exists other carrier based PWM which can perform better in terms of switching loss reduction and common mode voltage reduction which are not covered in this thesis.

AC load control objective:

As shown in Fig 3-3. System control is divided two major loops.

- DAB voltage loop: it works as inner loop whose bandwidth will be higher than the inverter voltage loop. The primary DC bus voltage reference is not an easy decision. For example, it needs to be close enough to the battery voltage to minimize the reactive power and current stress inside the DAB to reduce the conduction loss. However, in this thesis, the dc bus voltage is not optimally selected considering this factor, instead the DC bus voltage reference can be modified by the load voltage reference if the DC bus is not high enough to provide the desired load line-line voltage when under highest modulation index. This idea is also summarized in Fig 3-3 as red "if" loop and green "if" loop. The main goal for this loop is to control the phase shift between primary bridge and secondary bridge to realize the power flow hence regulating the primary DC bus voltage.
- Inverter voltage loop: As mentioned above, the inverter loop may generate a feedforward value to change the DC voltage reference depending on the load voltage requirement. The main goal for this loop is to dynamically change the modulation index to regulate the output voltage and control it as a "stiff" voltage source.

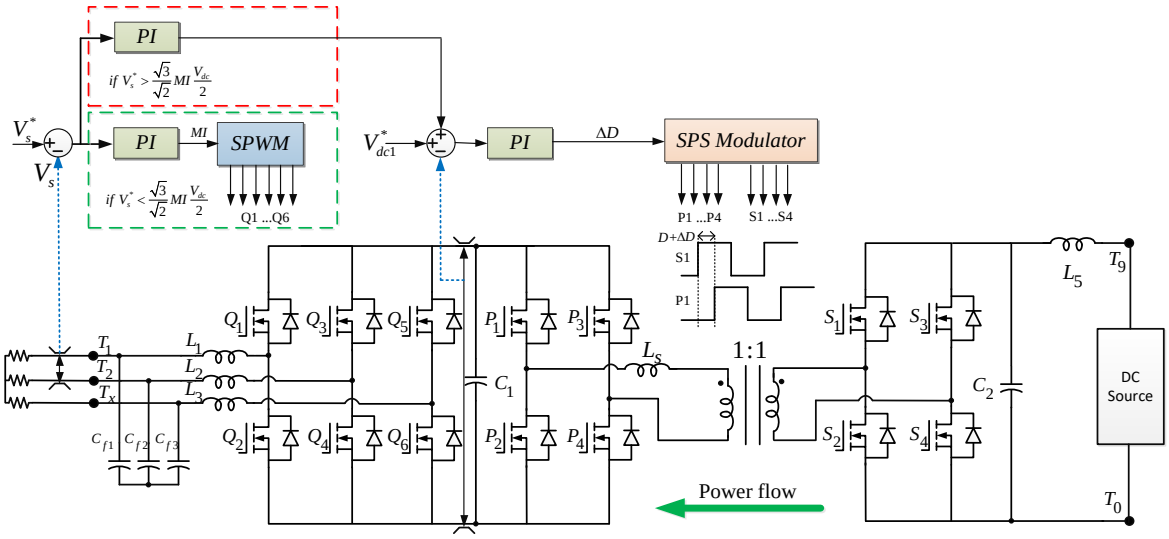


Figure 3- 3 V2L AC Linear Load control diagram

DC load Control objective:

The inverter side switches are working as interleaved buck converter (also known as multiphase buck).

The gating signal is phase shifted between Q1, Q3, and Q5 while they have the same duty ratio based on the relationship of $\frac{V_{in}}{V_{out}}$.

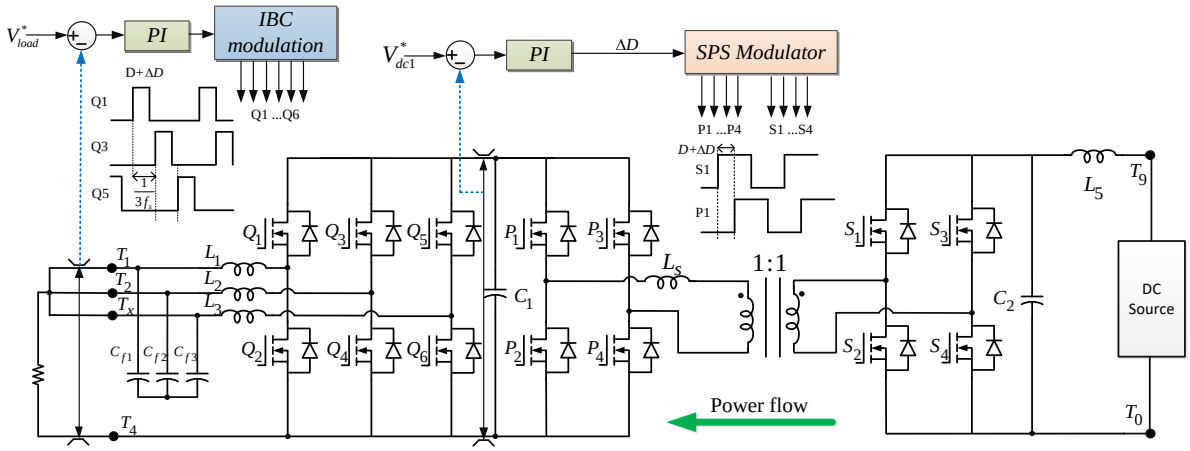


Figure 3- 4 V2L DC Load control diagram

Modeling in power electronics:

There are basically two ways to model the time-discontinuous dynamics of converters.

- One way is to model the converter as a sampled-data system.
- Another way is to apply the averaging theory to transform the converter as a time-continuous system.

The most common averaging approach is to apply the moving average operator, which is also known as the state-space averaging method, to average out the switching dynamics. However, the state-space averaging model can only indicate the information about converter dynamics

below half the switching frequency. To cover and include the switching ripple effect, there are other methods, such as, Krylov–Bogoliubov– Mitropolsky (KBM) and multifrequency averaging (MFA).

The small-signal linearization is working like approximating a non-linear system at a given operating point with small-signal perturbations. The small-signal averaged model is a good tool for controller design, but its accuracy suffers over high frequency range since it eliminates the high-frequency information through the process of the moving averaging.

The small-signal averaged model is the most commonly used when analyzing the controller design. The modeling workflow is also summarized in Fig 3-5.

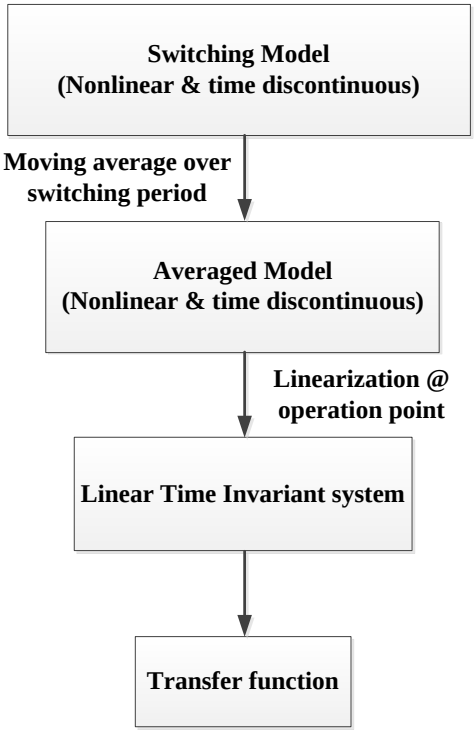


Figure 3- 5 Modeling workflow of power converter

3.2.1 DAB modeling

Perform the state space averaging model analysis on DAB [100].

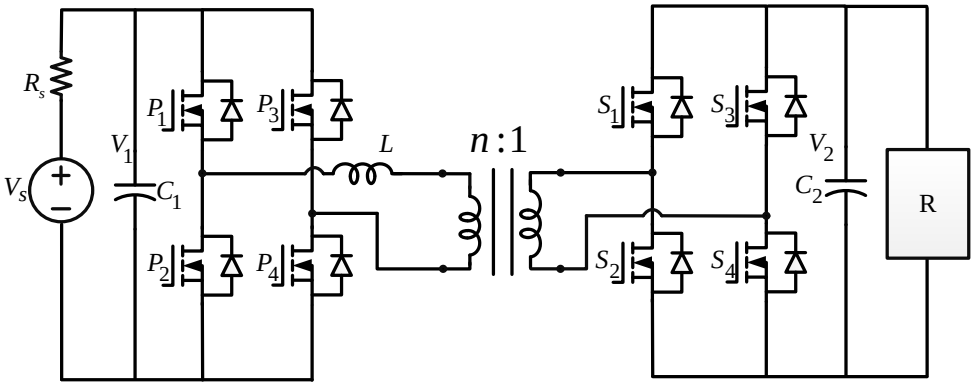


Figure 3- 6 Simplified model of DAB

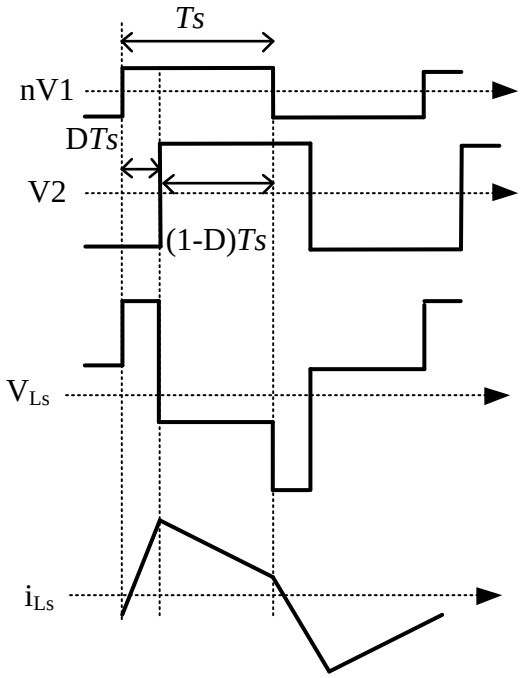


Figure 3- 7 Waveforms of single phase shifted DAB

State space models during four different intervals have been summarized into 3-1 and 3-4.

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} & \frac{1}{L} \\ -\frac{1}{C_1} & -\frac{1}{r_s C_1} & 0 \\ -\frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{r_s C_1} \\ 0 \end{bmatrix} v_s \quad t \in [0\ DT_s] \tag{3-1}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & \frac{1}{L} & -\frac{1}{L} \\ -\frac{1}{C_1} & -\frac{1}{r_s C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{r_s C_1} \\ 0 \end{bmatrix} v_s \quad t \in [DT_s \; T_s] \tag{3-2}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{1}{L} \\ \frac{1}{C_1} & -\frac{1}{r_s C_1} & 0 \\ \frac{1}{C_2} & 0 & -\frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{r_s C_1} \\ 0 \end{bmatrix} v_s \quad t \in [T_s \; (1+\mathrm{D})T_s] \tag{3-3}$$

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dv_1}{dt} \\ \frac{dv_2}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{L} & \frac{1}{L} \\ \frac{1}{C_1} & -\frac{1}{r_s C_1} & 0 \\ -\frac{1}{C_2} & 0 & \frac{1}{RC_2} \end{bmatrix} \begin{bmatrix} i_L \\ v_1 \\ v_2 \end{bmatrix} + \begin{bmatrix} 0 \\ \frac{1}{r_s C_1} \\ 0 \end{bmatrix} v_s \quad t \in [(1+\mathrm{D})T_s \; 2T_s] \tag{3-4}$$

3.2.2 VSI Inverter modeling and Multiphase DC/DC (IBC) modeling

Under V2L operation mode, VSI and the interleaved buck converter (IBC) can be modeled as the voltage amplifier with gain of duty ratio (modulation index).

When the VSI is interacting with the grid, more dynamics detail needs to be modeled which will be covered in the next section.

3.3 Simulation and Experimental results

3.3.1 Three phase resistive load - Experimental and Simulation results

Before the closed loop control is implemented. Open loop test is performed with DAB and inverter together.

Hardware Setup	Value
DAB Switching frequency	100kHz
Inverter switching frequency	100kHz
Load resistance per phase	13 Ω
Filtering inductance	10uH
Filtering capacitance	50uF
DAB leakage inductance	22uH
DC Source voltage	140V
Constant phase shift	90°
Inverter Modulation index	1
Power level	2kW

Table 3- 1 Open loop prototype test setup parameter

Testing conditions: The battery voltage is 140V; the DAB is getting constant 90° phase shift. Since this is V2L operating modes, the secondary phase legs should be leading the primary phase legs.

Without control, the primary voltage is not 140V, it reaches to a stable voltage due to the system power balance with current load setup. The open loop test results are shown in Fig 3-8 and Fig 3-9.

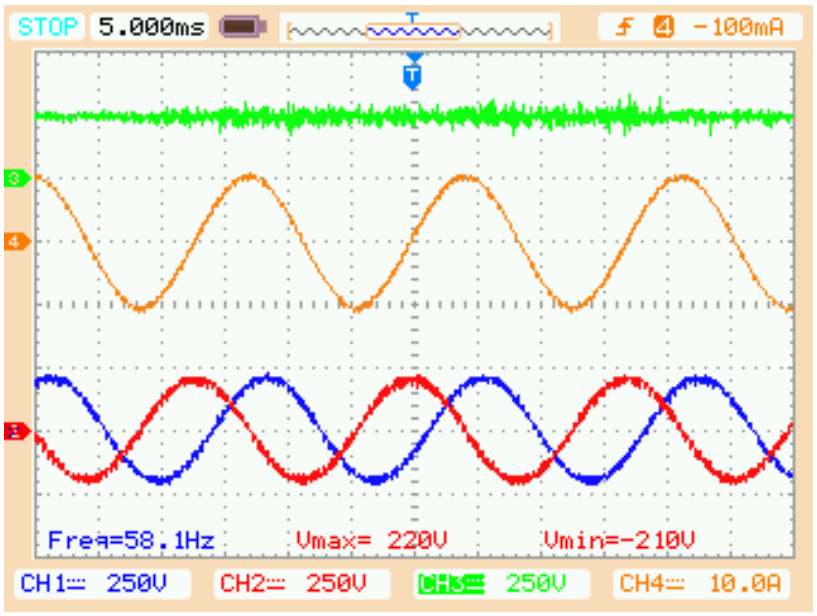


Figure 3- 8 Open loop V2L Inverter's output waveform

Ch1 and Ch2 load line-line voltage; Ch3 DC bus voltage; Ch4 load phase current

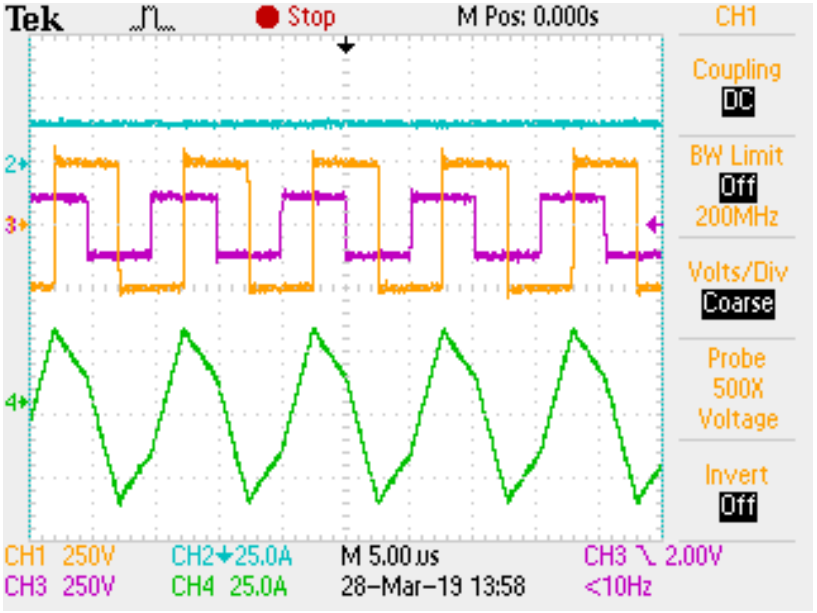


Figure 3- 9 Open loop test DAB waveforms

Ch1 and Ch3 DAB primary and secondary voltage; Ch2 Battery current; Ch4 Leakage current

In order to regulate the primary voltage, a PI controller is implemented. To tune and verify the PI gains, some experiments are performed.

Hardware Setup	Value
Switching frequency	100kHz
Load resistance per phase	13 Ω
Filtering inductance	10uH
Filtering capacitance	50uF
DC Source voltage	120V
Kp	0.001
Ki	0.5
Inverter modulation index	1
Primary voltage reference	80V < --- > 140V

Table 3- 2 Closed loop V2L test setup parameter

Figure 3-10 shows the inverter output during the primary voltage jump up.

Figure 3-11 shows the DAB waveform during the primary voltage jump up.

Figure 3-12 shows the DAB zoomed in version of the dynamic jump-up change. It can clearly show that the phase shift angle is increasing and trying to regulate the voltage following the reference.

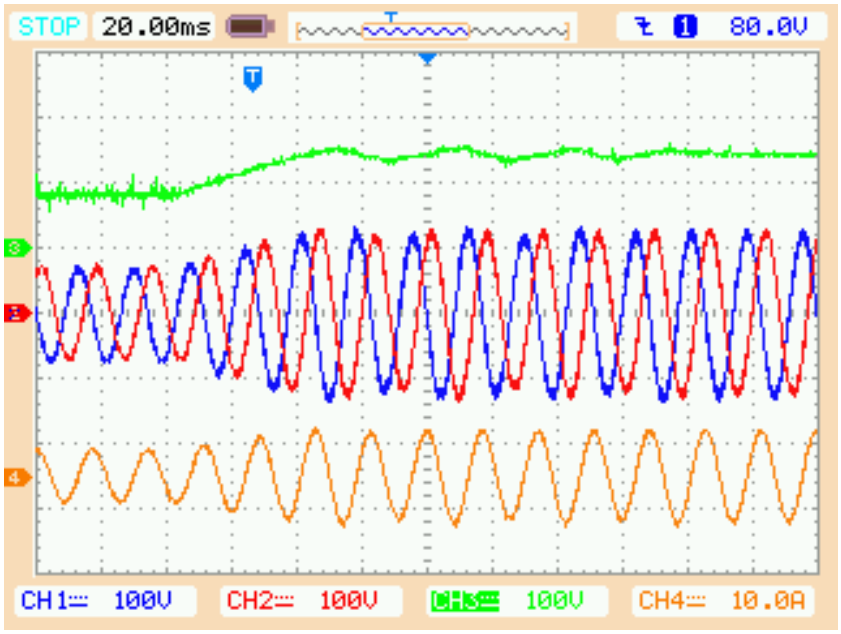


Figure 3- 10 Inverter wavefrom during the change of primary voltage from 80V to 140V

Ch1 and Ch2 load line-line voltage; Ch3 DC bus voltage; Ch4 load phase current

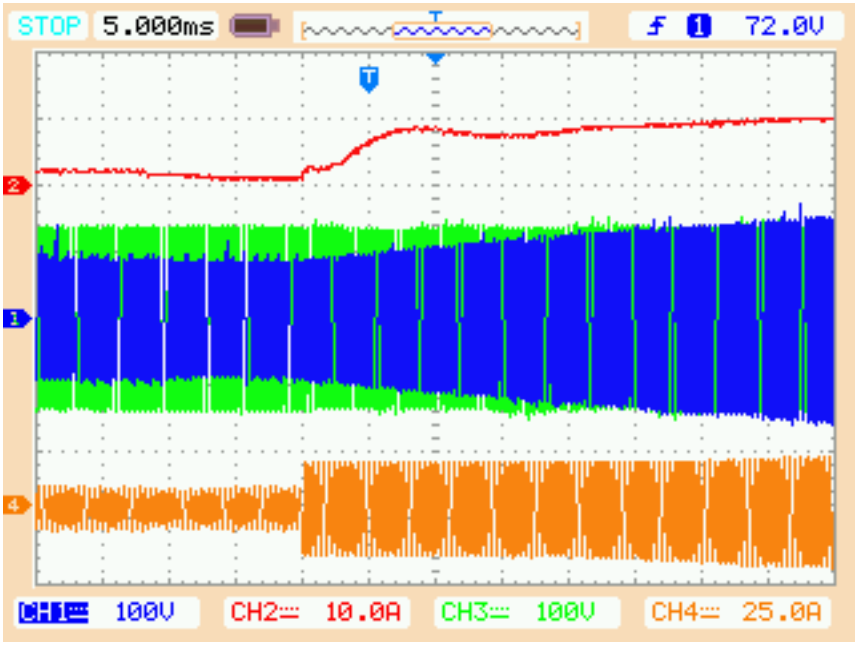


Figure 3- 11 DAB waveform during the change of primary voltage from 80V to 140V

Ch1 and Ch3 DAB primary and secondary voltage; Ch2 Battery current; Ch4 Leakage current

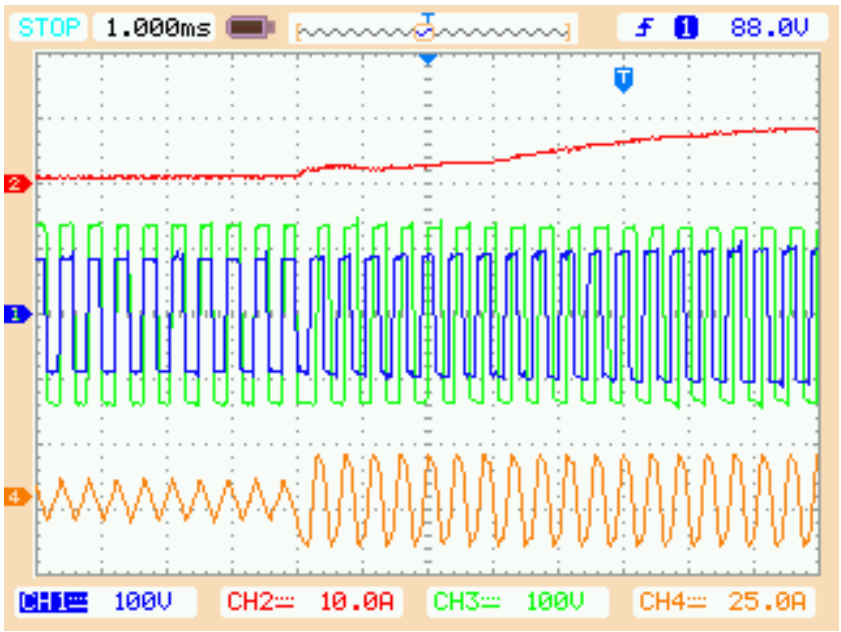


Figure 3- 12 Zoomed in verion of dynamic change during jump up

Ch1 and Ch3 DAB primary and secondary voltage; Ch2 Battery current; Ch4 Leakage current

Figure 3-10 shows the inverter output during the primary voltage jump down.

Figure 3-11 shows the DAB waveform during the primary voltage jump down.

Figure 3-12 shows the DAB zoomed in version of the dynamic jump-up change. It can clearly show that the phase shift angle is gradually decreasing and trying to regulate the voltage following the reference.

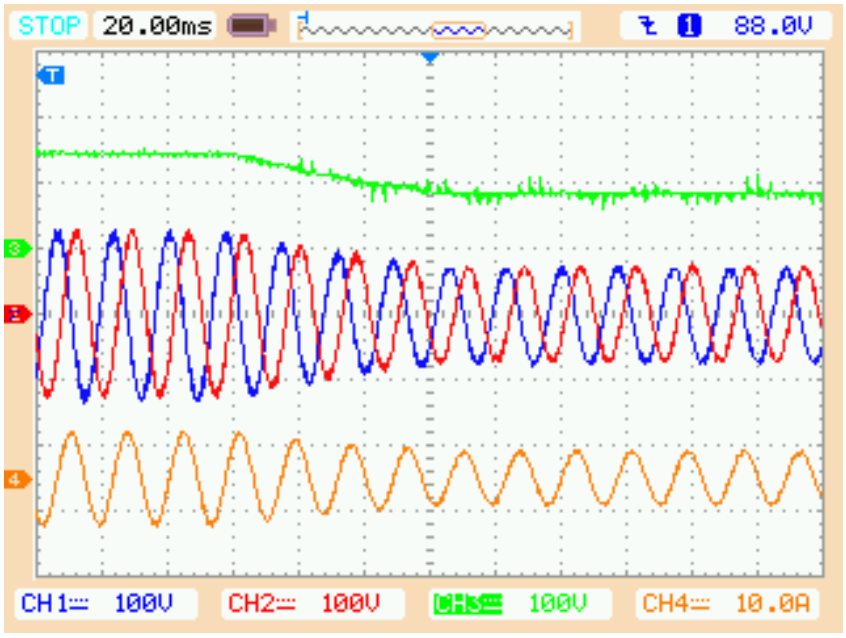


Figure 3- 13 Inverter wavefrom during the change of primary voltage from 140V to 80V

Ch1 and Ch2 load line-line voltage; Ch3 DC bus voltage; Ch4 load phase current

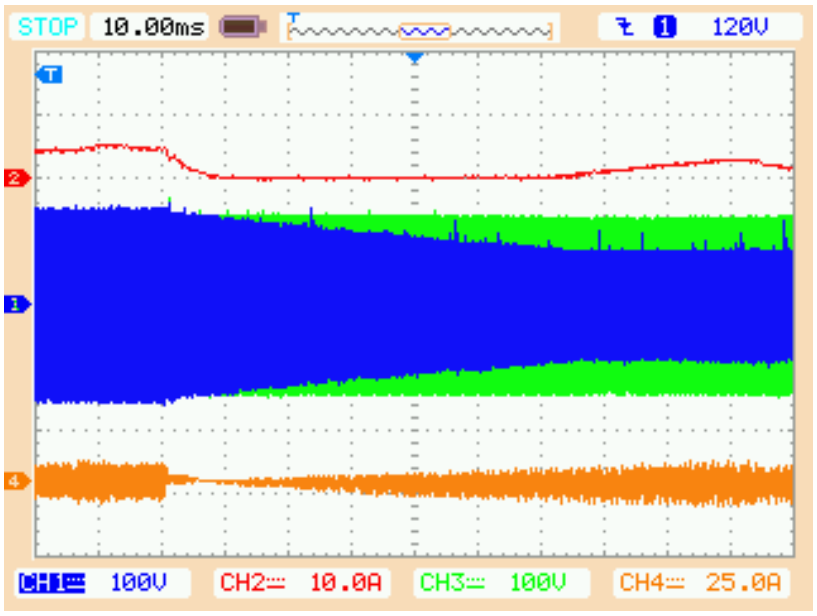


Figure 3- 14 DAB waveform during the change of primary voltage from 140V to 80V

Ch1 and Ch3 DAB primary and secondary voltage; Ch2 Battery current; Ch4 Leakage current

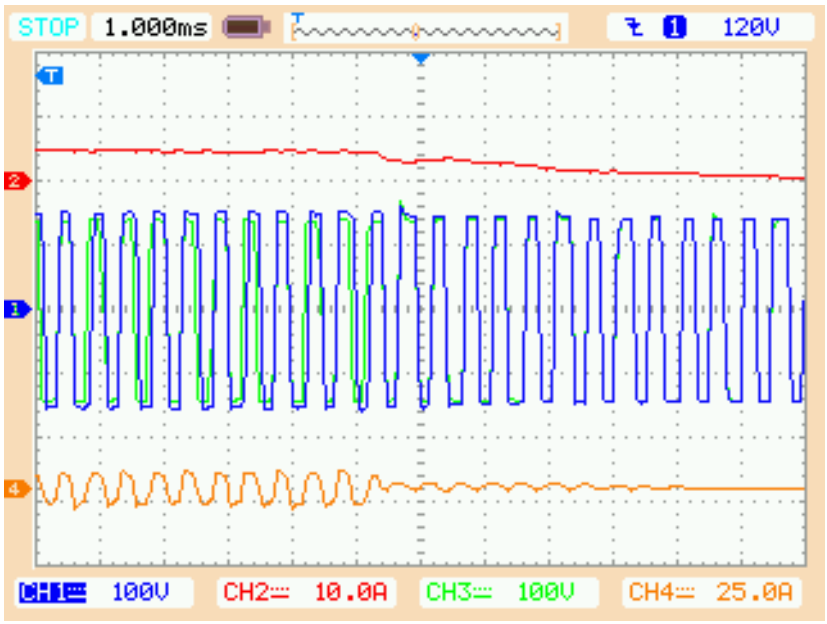


Figure 3- 15 Zoomed in verion of dynamic change during jump down

Ch1 and Ch3 DAB primary and secondary voltage; Ch2 Battery current; Ch4 Leakage current

The above testes verify that the DAB voltage can be regulated.

When the converter operates under V2L modes, it needs to provide "stiff" AC voltage no matter what load is connected. Assuming the primary bus voltage is constant by regulating the DAB, simulation of dynamic load change including linear and non-linear load is carried out to help validate the inverter side control algorithm.

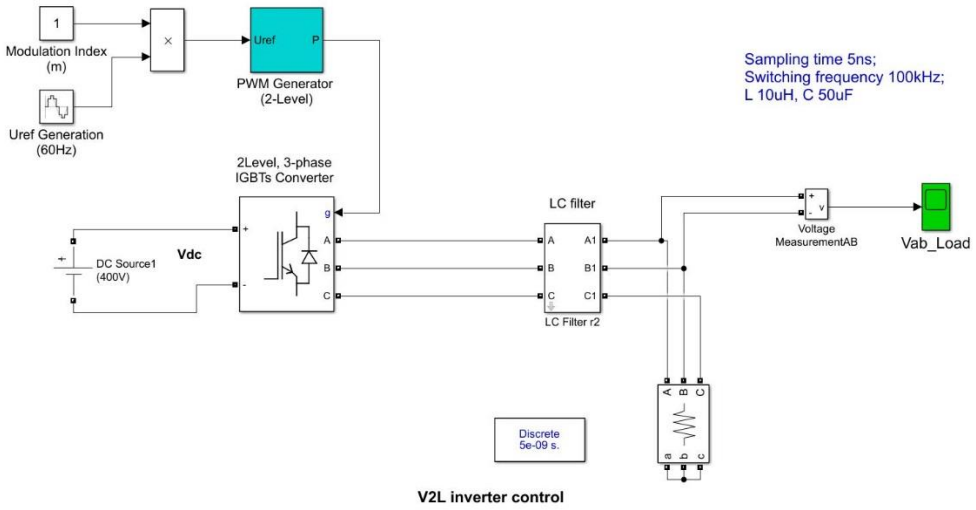


Figure 3- 16 Simulation of Inverter under step linear load change

Fig 3-16 and Fig 3-17 shows that the voltage seen by the load is very stiff even though the load current is larger after a load step change. The reason is that the DC source in the simulation is ideal. However, by regulating the primary DC bus through DAB, "ideal" DC bus can be achieved in the prototype as well.

Simulation Parameter	Value
Switching frequency	100kHz
Load resistance	13 Ω
Filtering inductance	10uH
Filtering capacitance	50uF

Table 3- 3 Linear load step change simulation parameter

Table 3-3 (cont'd)

Inverter modulation index	1
DC source voltage	400V
Load step change	0.05s
Change ratio	3 times

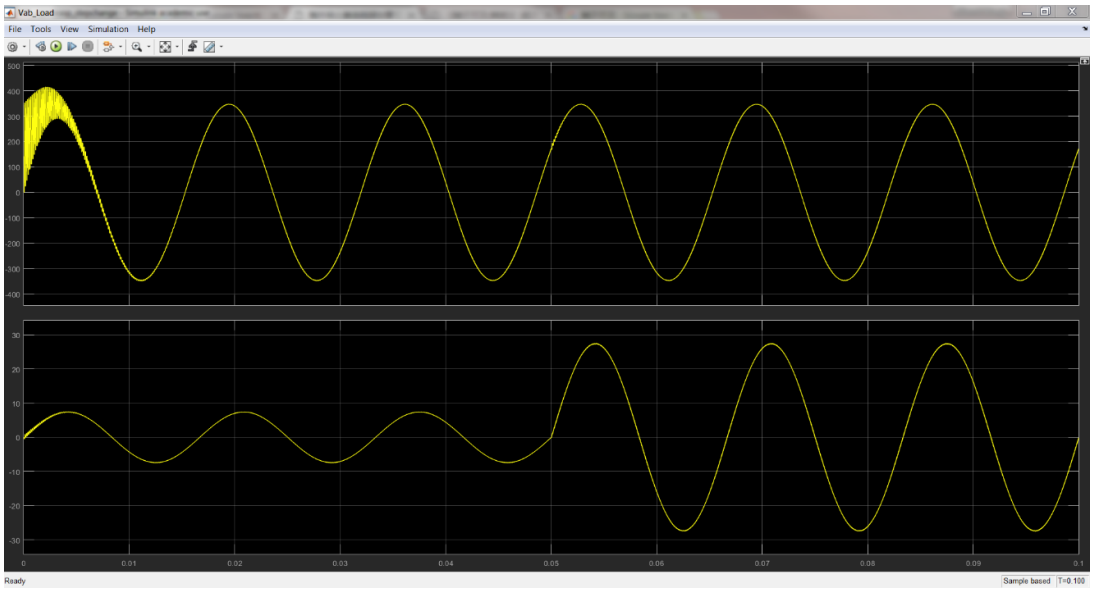


Figure 3- 17 Load voltage(top) and load current(bottom) under step load change

In order to further prove the statement of stiff voltage source, non-linear load (diode bride) is inserted to the system as shown in Fig 3-18. The simulation result in Fig 3-19 shows that even the current is highly distorted, the output voltage seen by the load is still sinusoidal which is the same case as the grid voltage output.

Simulation Parameter	***Value***
Switching frequency	100kHz
Load resistance	13 Ω
Filtering inductance	10 uH
Filtering capacitance	50 uF

Table 3- 4 Non-linear load step change simulation parameter

Table 3-4 (Cont'd)

Inverter modulation index	1
DC source voltage	400V
Load step change	0.05s
Change type	Add diode rectifier

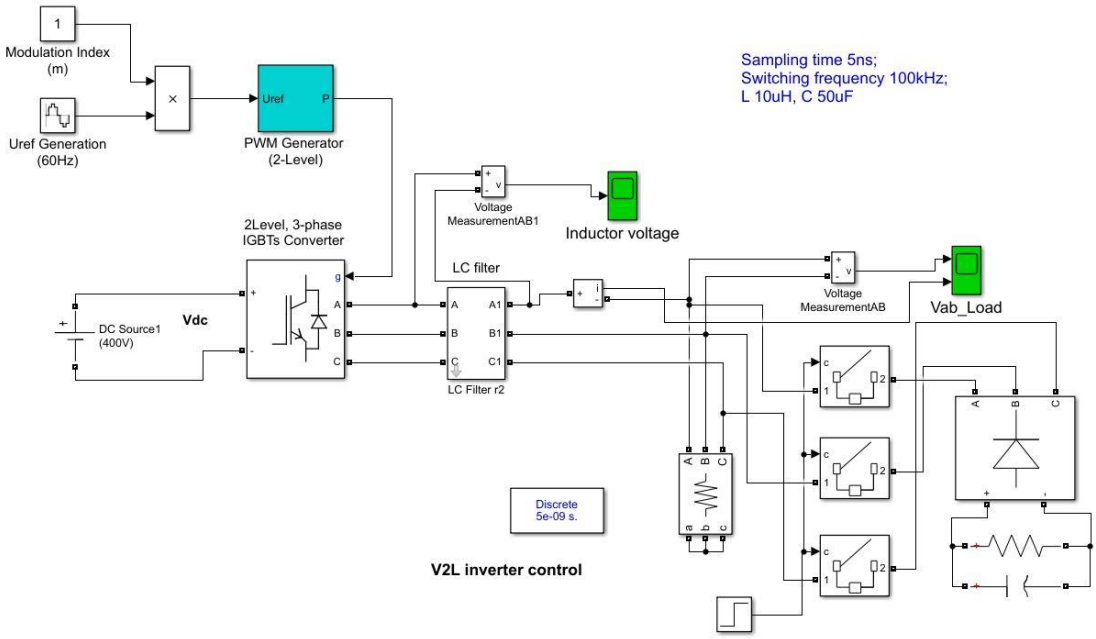


Figure 3- 18 Simulation of Inverter under step non-linear load change

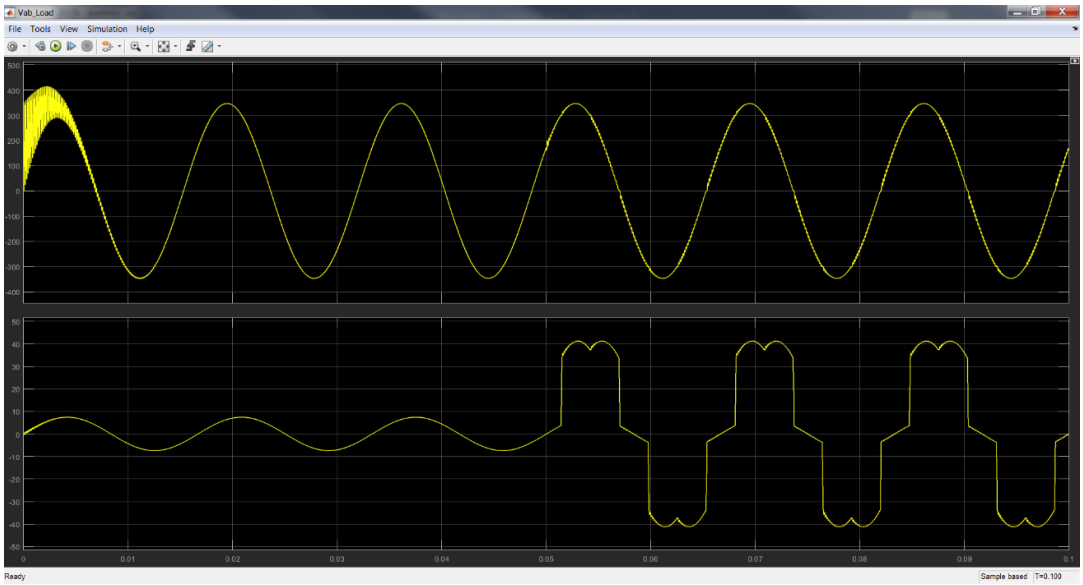


Figure 3- 19 Load voltage(top) and load current(bottom) under step non-linear step load change

Another reason behind the stiffness is the filtering inductance is small, which means the internal impedance of the voltage source is small. If the load impedance is not comparable to internal impedance, the voltage source inverter can be viewed as ideal voltage source. To further verify the idea, filtering inductance is changed to 10mH and with load resistance is 0.1 ohm. Pronounced voltage drop can be observed in Fig. 3-20, since the load and the internal impedance is working as a voltage divider.

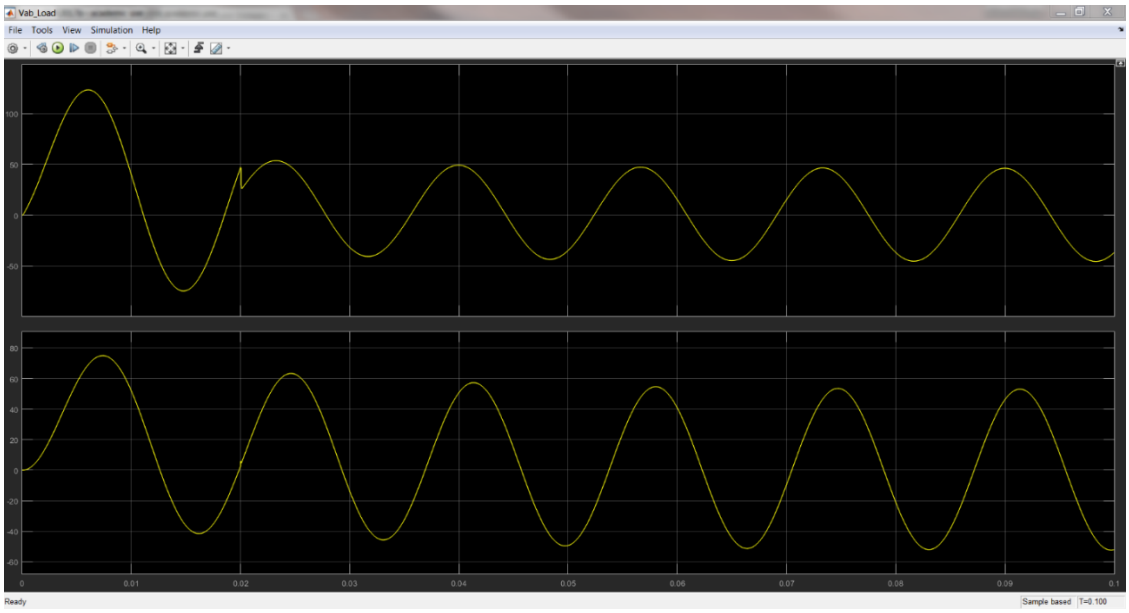


Figure 3- 20 Large filtering inductance and with small resistance load

It is also important to point that low filtering inductance can help to improve the system stability with LC filter and reduce the need for resistive damping.

The Fig 3-21 shows the bode plot of the system LC filter with variable inductance. There is 0.4Ω resistance distributed on the system which works as the damping resistance in this 2^{nd} order system.

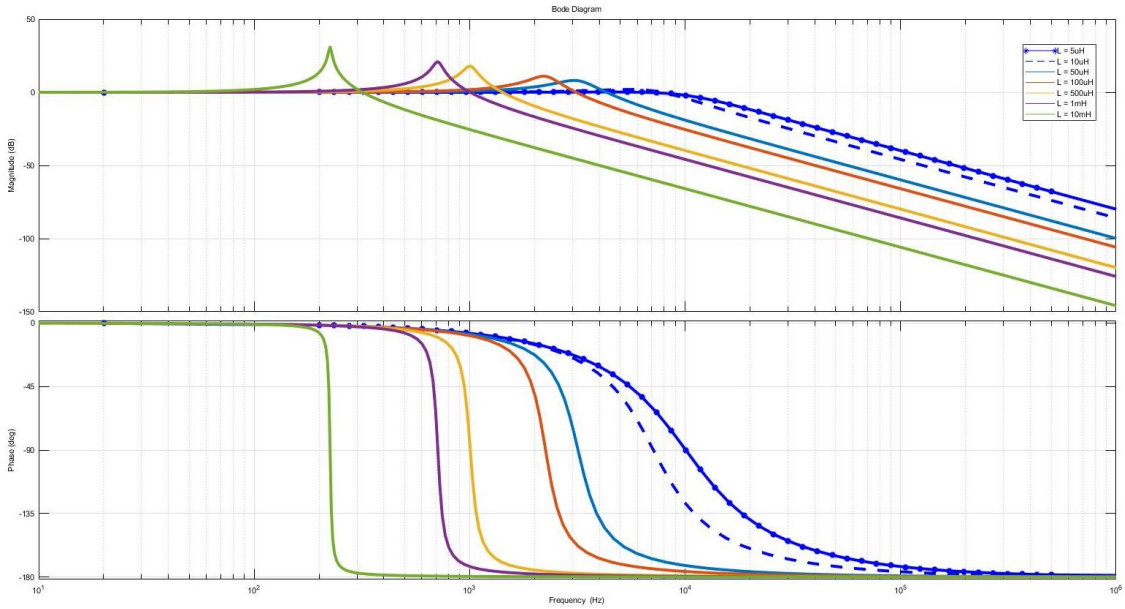


Figure 3- 21 Bode plot of variance of internal filtering inductance

3.3.2 DC load Simulation and Experiment result

In order to verify the multiphase DC-DC operation, simulation is performed first.

Assume the DC bus voltage is 200V, and the load voltage will be regulated to 48V. The inductor and capacitor value are the same as the setup which are 10uH and 50uF. The load is 12ohm. The legs are switching at 100kHz. The simulation setup is shown in Fig 3-22.

Simulation Parameter	Value
Switching frequency	100kHz
Phase shift among each leg	120°
Load resistance	10 Ω
Filtering inductance	10uH
Filtering capacitance	50uF *3
DC source voltage	200V
Output Voltage reference	48V

Table 3- 5 Simulation parameter for V2L DC mode

The legs are having the modulation and carrier signal phase shifted by $\frac{1}{3}T_s$ which is 3.3us. It is also shown in Fig. 3-23.

Fig 3-24 shows each leg's inductor current and the final out put voltage including the start up transient.

Fig 3-21 shows the zoomed in version of the final voltage which shows very minimal voltage ripple.

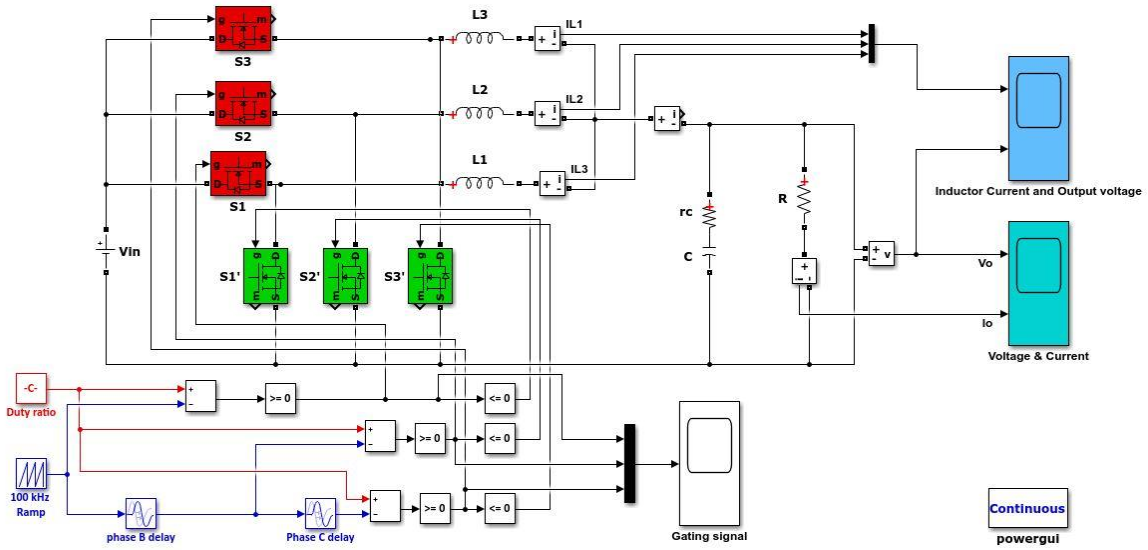


Figure 3- 22 Simulation of Interleaved Buck (Multiphase Buck)

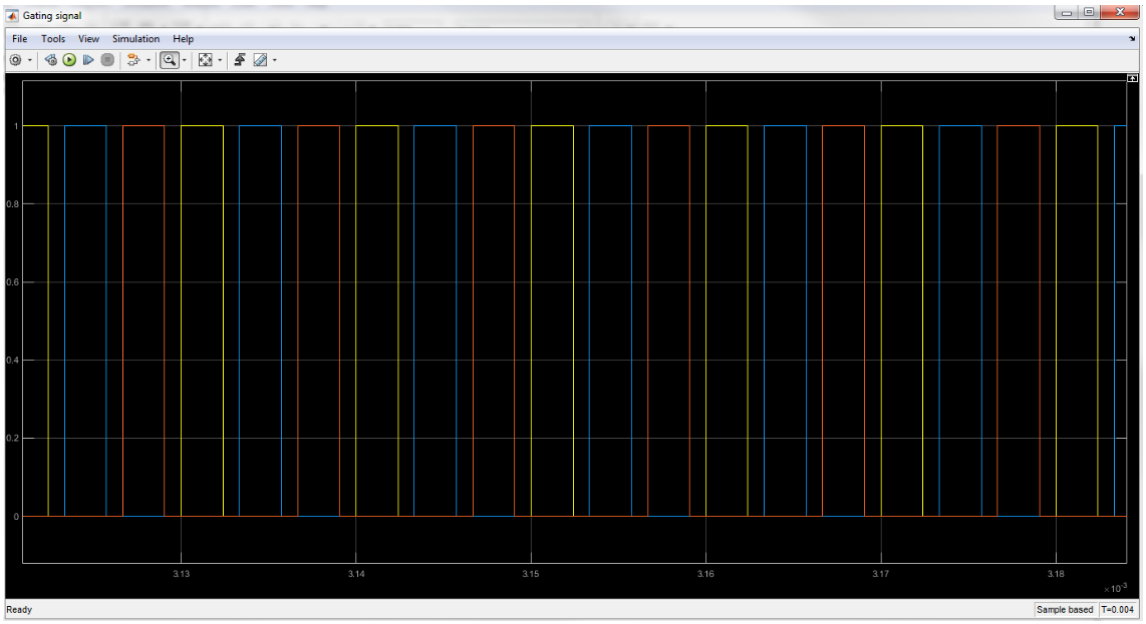


Figure 3- 23 Gating signal of Leg 1, Leg 2 and Leg 3.

The Yellow is leg1's gating signal, the red is leg2's gating signal, and the blue is leg3's gating signal.

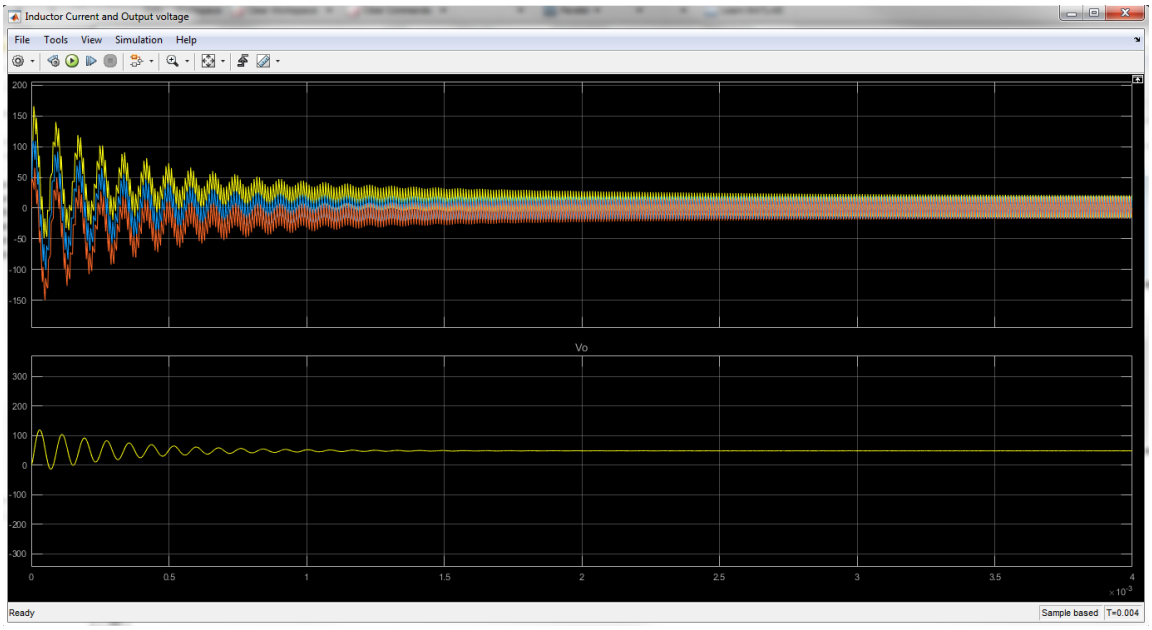


Figure 3- 24 Inductor current of Leg 1, Leg 2, Leg 3 (Top), and output voltage (Bottom)

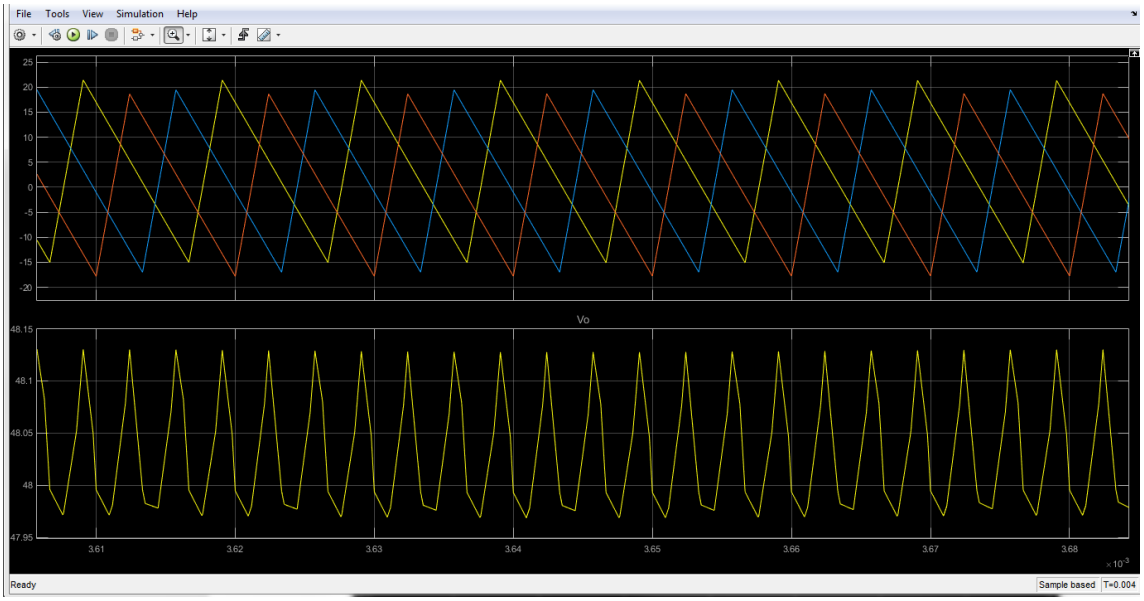


Figure 3- 25 Zoomed in version of inductor current and output voltage

Hardware experiments is carried out to verify the operation principle. The test setup is as follows:

Hardware Setup	Value
Switching frequency	100kHz
Phase shift among each leg	120°
Load resistance	10 Ω
Filtering inductance	10uH
Filtering capacitance	50uF *3
DC source voltage	200V
Output Voltage reference	48V

Table 3- 6 Hardware setup parameter for V2L DC LOAD

The measured output voltage is 48V with phase-shifted modulation signal.

Each modulation signal is phase shifted by 120° and the modulation ratio $D = \frac{48}{200}$ which is shown in Fig 3-26.

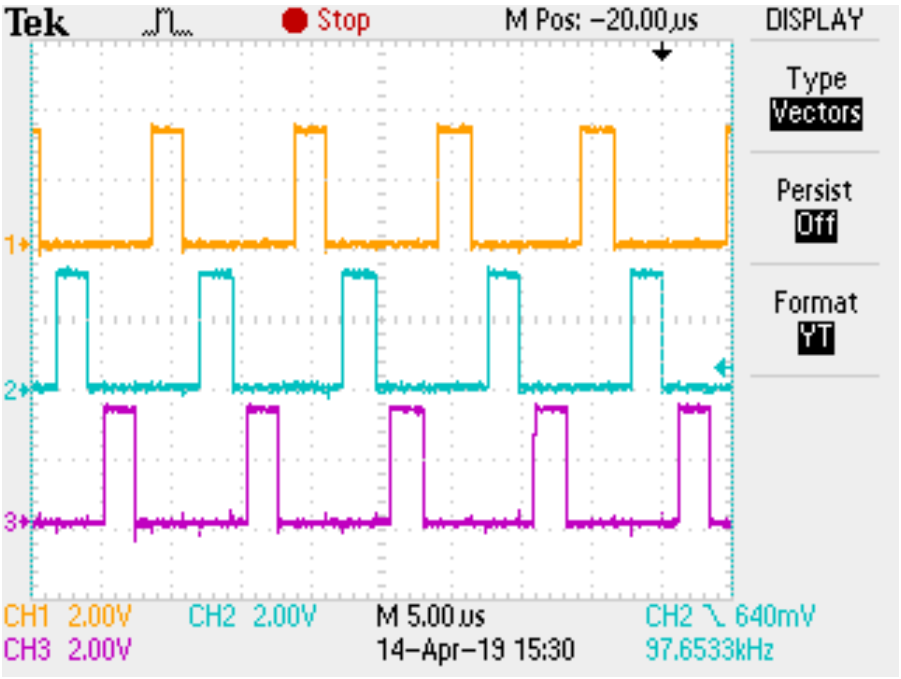


Figure 3- 26 Gating signal of multi-phase step down operation

The output voltage is 48V (blue curve in Fig 3-27), and the notch is due to the gap between each leg's gating signal.

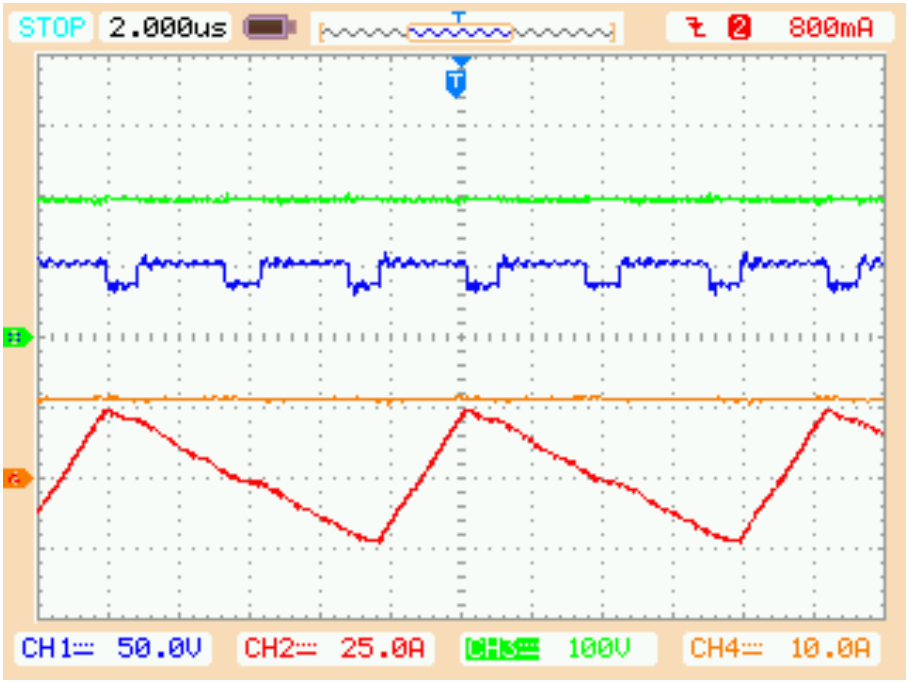


Figure 3- 27 Output voltage and current waveform

Ch1 Output voltage; Ch3 Primary bus voltage; Ch2 Phase leg current; Ch4 Load current

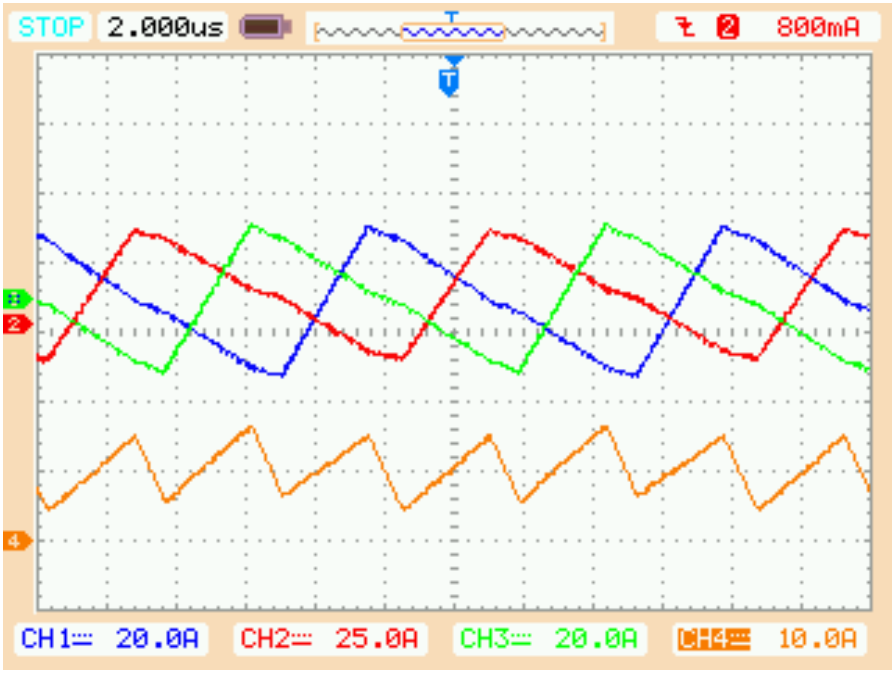


Figure 3- 28 Each phase leg current and resultant current

Ch1 Ch2 Ch3 Phase leg current; Ch4 Resultant current

From the experiment results, the stepped down DC bus voltage is very stable, and the current flowing into the load is not suffering huge current ripple.

By configuring the inverter into multiphase buck converter enables its wide application in other scenarios.

In this section, V2L operation under AC load and DC load are both analyzed and validated with experimental results.

Chapter 4 Vehicle to Grid (V2G) analysis and control

4.1 Operation principle of V2G mode

The power is flowing from the high voltage battery to the grid under V2G. In the home-based microgrid, V2G will be a very useful operating case, such as using the car's battery to perform reactive power compensation which can be used to offset the reactive power drawn by certain highly inductive load such as HVAC to save the utility bill. When providing the reactive power compensation and performing the voltage regulation, the converter loss is converter by the utility grid and the active power of the battery is not drained (state of charge is not adversely affected). What is more, less engagement with the battery can help preserve the battery life.

Another important application or feature is to "sell" or send the active power back to the grid to help the peak hour load shaving, for example at 6pm in the summer.

There are some debates from the automotive company regarding the V2X operation since it will put more stress on the battery and will expediate the battery degrading. However, in this thesis, the adverse effect of V2X to battery will not be discussed.

Three phase and single-phase operation modes are shown in Fig 4-1 and Fig 4-2.

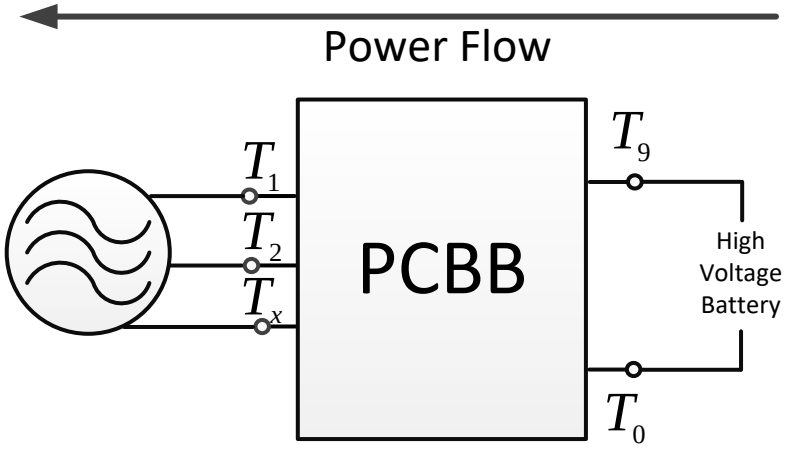


Figure 4- 1 V2G Three phase operation mode

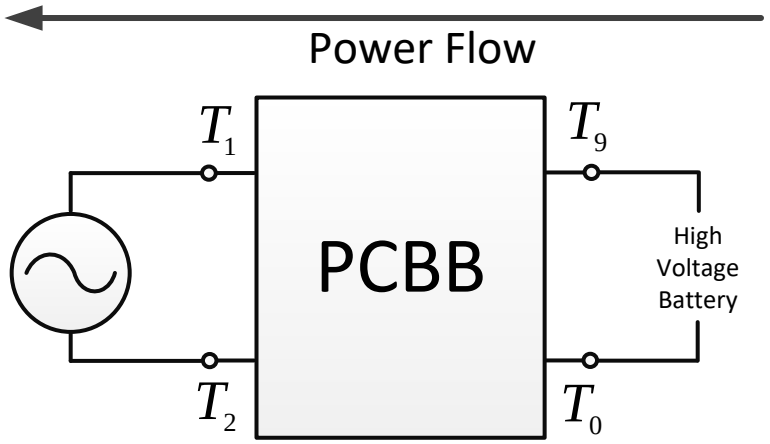


Figure 4- 2 V2G Single phase operation mode

To summarize, EV chargers can provide following services to the grid, that can be offered in V2G: 1) peak shaving, 2) harmonic filtering as APF (active power filter), 3) voltage stabilization and support, 4) power factor correction, and 5) reactive power compensation. Also, if the grid electricity is lost, the charger should be capable for islanded operation to feed emergency power which is often called vehicle-to-home (V2H) or vehicle-to-any load (V2X) and it has covered in section 3.

Under this operation mode, the converter process power through two stages:

Grid-tied inverter: Unlike the inverter in V2L mode, it will need to control the grid current to realize the independent control of active power (P) and reactive power (Q). What is more important, the primary DC bus voltage also needs to be regulated by the inverter control. However, it can also be controlled by DAB and the difference of these two options is not being discussed in this thesis.

Isolated dc-dc converter: Unlike the DAB in V2L mode, the DAB will fall into an open loop mode. It generates the phase shift signal based on the active power command, and voltage value on both sides of the transformer.

In the next section, grid-imposed inverter current controller design and voltage controller design is analyzed thoroughly.

4.2 Grid imposed inverter modeling

There are four typical operation modes for gird-connected voltage source inverter as shown in Fig 4-3. ***V*** is the grid voltage and ***I*** is the gird current (or current out of converter) since VSI is normally operating under current controlled mode.

Mode (a): The voltage and current are in phase and the pf is 1. The active power is flowing into the converter and it is also known as PWM (active) rectifier.

Mode (b): The voltage and current are 180° apart and the pf is -1. The active power is flowing into the grid from the converter.

Mode (c): The current is leading the voltage 90° and the pf is 0. The converter is providing capacitive reactive power to the grid.

Mode (d): The current is lagging the voltage 90° and the pf is 0. The converter is providing inductive reactive power to the grid.

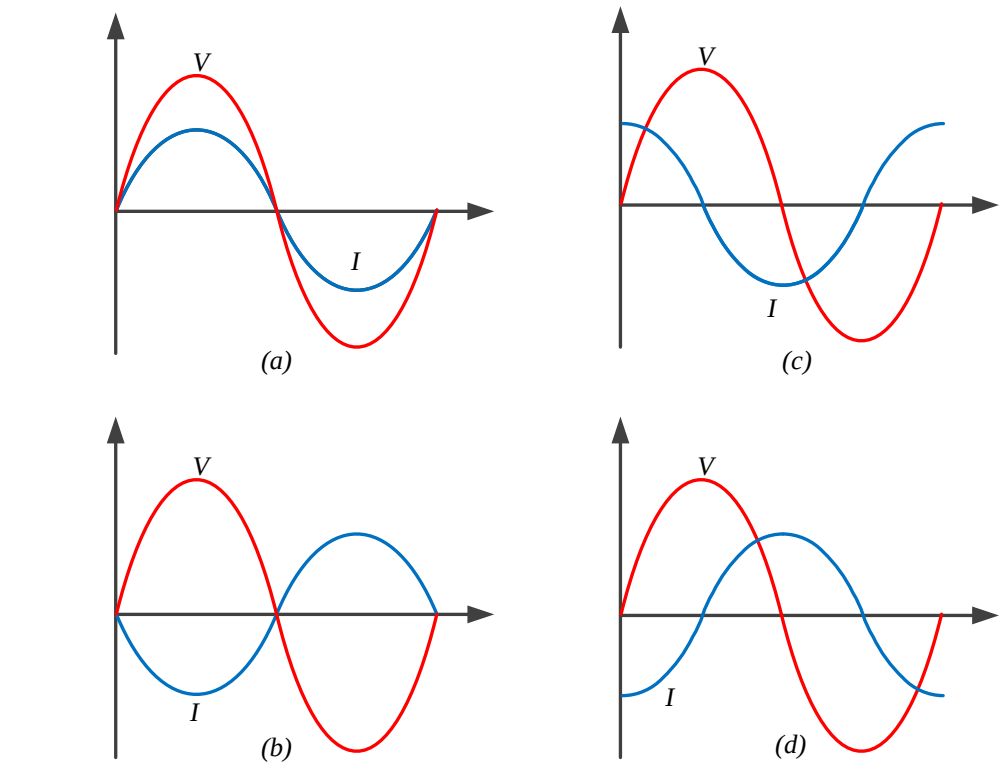


Figure 4- 3 Four operation modes of grid imposed VSI converter

4.2.1 Three phase grid-tied inverter modeling

Assuming the grid is strong which means the voltage sensed before the inductor is strong.

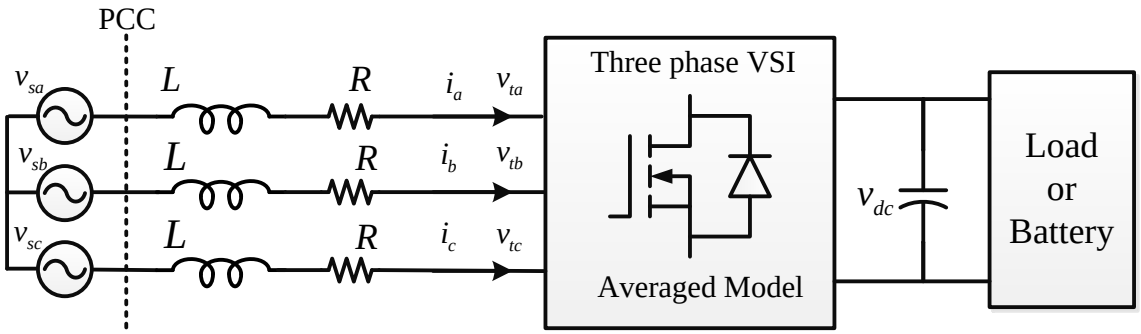


Figure 4- 4 Three phase grid-imposed averaged Model of VSC

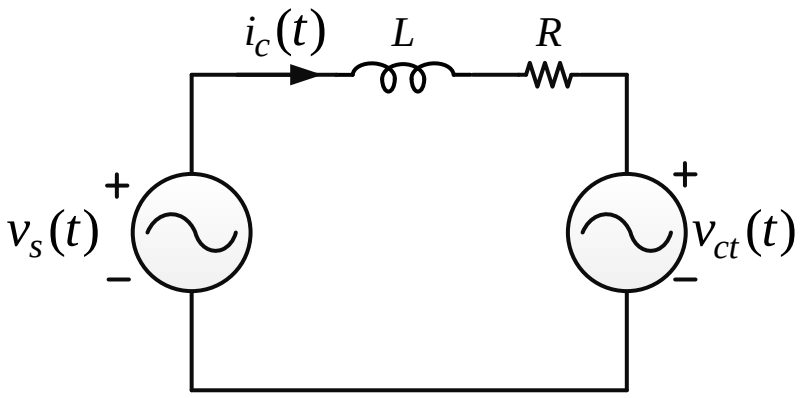


Figure 4- 5 Phasor form of dynamics between VSC and grid

Dynamics of the AC side of the VSI can be described by Eq.4-1

$$L\frac{d\vec{i}}{dt}+R\vec{i}=\overrightarrow{v_s}-\overrightarrow{v_{ct}} \tag{4-1}$$

Where L is the coupling inductor and R is the system resistance (distributed on the line or line).

Replace the rotating phasor expression to d-q frame reference system requires a phase-locked-loop. For 3 phase system, the PLL is structured in this way:

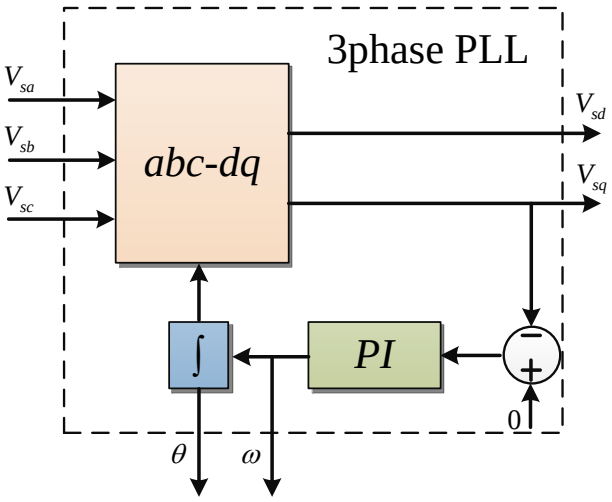


Figure 4- 6 Three phase phased-lock loop

With PLL, the phase angle and frequency can be applied to decompose rotating phasor form of Eq. 4-1.

$$L\frac{di_d}{dt} - \omega L i_q + R i_d = V_{sd} - V_{ctd} \tag{4-2}$$

$$L\frac{di_q}{dt} - \omega L i_d - R i_q = V_{sq} - V_{ctq} \tag{4-3}$$

By using the instantons power theory, the active and reactive power delivered at PCC is

$$P(t) = \frac{3}{2}[V_{sd}(t) \times i_d(t) + V_{sd}(t) \times i_q(t)] \tag{4-4}$$

$$Q(t) = \frac{3}{2}[-V_{sq}(t) \times i_q(t) + V_{sq}(t) \times i_d(t)] \tag{4-5}$$

If PLL is in a steady state and the grid is not unbalanced, Vsq = 0. The active and reactive power equation can be rewritten as

$$i_{dref}(\mathrm{t}) = \frac{2}{3V_{sd}} P_{sref}(\mathrm{t}) \tag{4-6}$$

$$i_{qref}(\mathrm{t}) = \frac{2}{3V_{sd}} Q_{sref}(\mathrm{t}) \tag{4-7}$$

To decouple the cross-dynamics in 4-2 and 4-3, feedforward decouple needs to be designed:

$$V_{ctd} = V_{sd} + \omega L i_q - (L\frac{di_d}{dt} + R i_d) \tag{4-8}$$

$$V_{ctq} = V_{sq} - \omega L i_d - (L\frac{di_q}{dt} + R i_q) \tag{4-9}$$

Hence, the dynamics inside the 4-2 and 4-3 can be simplified into

$$L\frac{di_d}{dt} = -Ri_d + u_d \tag{4-10}$$

$$L\frac{di_q}{dt} = -Ri_q + u_q \tag{4-11}$$

where ud and uq are the output from the current controller.

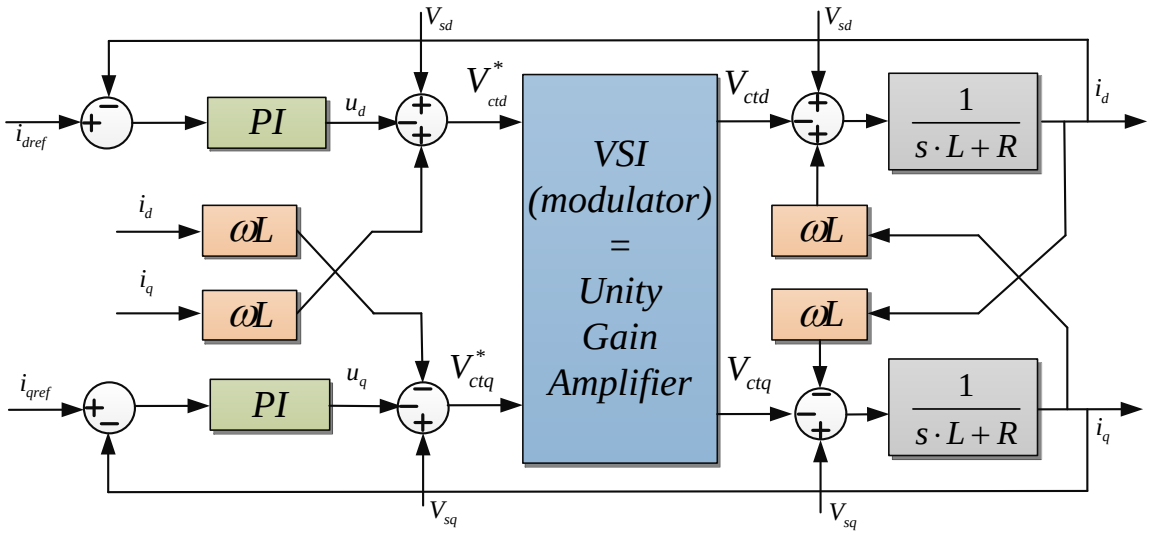


Figure 4- 7 d-q frame grid-tied current controller

The d and q axis current control loop are the same and can be summarized into Fig 4-8

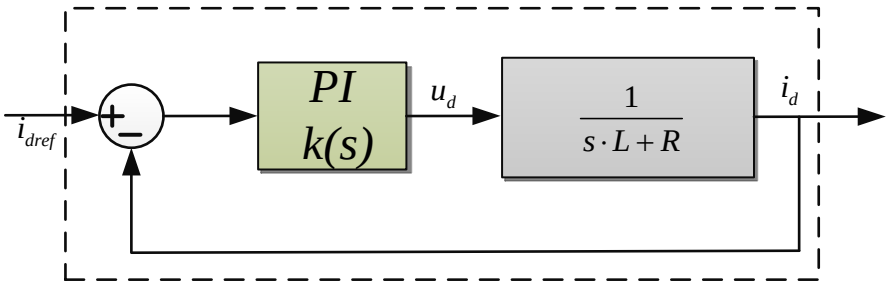


Figure 4- 8 Decoupled d (q) axis current controller

Set

$$k(s) = \frac{k_p s + k_i}{s} \tag{4-12}$$

The open-loop gain is

$$G_o(s) = \frac{k_p s + k_i}{s \cdot (Ls + R)} \tag{4-12}$$

To design the kp and ki to cancel the pole at -R/L. Set kp and ki

$$k_p = \frac{L}{\tau_i} \tag{4-12}$$

$$k_i = \frac{R}{\tau_i} \tag{4-13}$$

where τ_i is the closed loop time constant $G_c(s) = \frac{1}{\tau_i s + 1}$ and needs to be small for a fast current control response but adequately large such that the bandwidth of the closed-loop control is 10 times higher the switching frequency. The switching frequency is 20kHz and the coupling inductor is changed to 1mH for reduced switching frequency. (L = 1mH and R = 0.1 ohm)

τ_i can be set to 1/200kHz which is 20us. kp = 50 and ki = 500. The open-loop bode plot is shown in Fig 4-9.

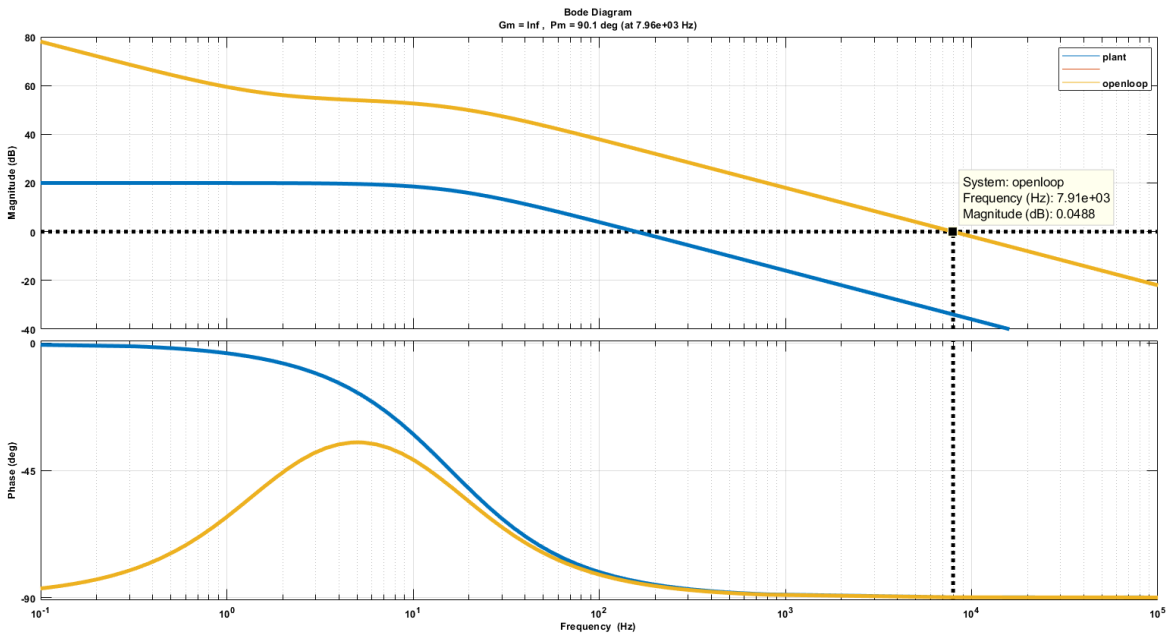


Figure 4- 9 Bode plot of the d (q) axis plant with PI controller

This loop has an 8 kHz open loop bandwidth (closed loop bandwidth will be higher), infinite gain margin and 91° phase margin to insure the fast dynamics response and stability.

(**Note:** Gain and phase margins are common terms to describe how stable a system is. Gain and phase margins are used more because they are simple than because they are ideal measurements of stability. Gain and phase margins are measured from the open loop frequency response of the system. Gain and phase margins cannot be acquired directly from a closed loop frequency response.)

DC Voltage loop:

The current controller *Gid(s)* can be simplified into a constant unity gain since the current loop as much higher bandwidth than the voltage loop (10 times higher).

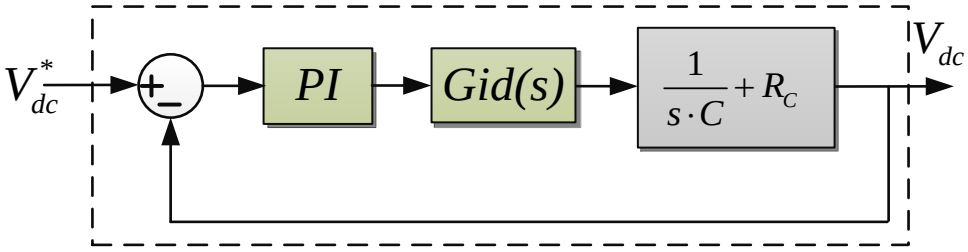


Figure 4- 10 Outer voltage loop with inner current loop

We can adopt similar methods for current controller design to apply on voltage loop controller.

Kp_v = 0.2 and Ki_v = 10.

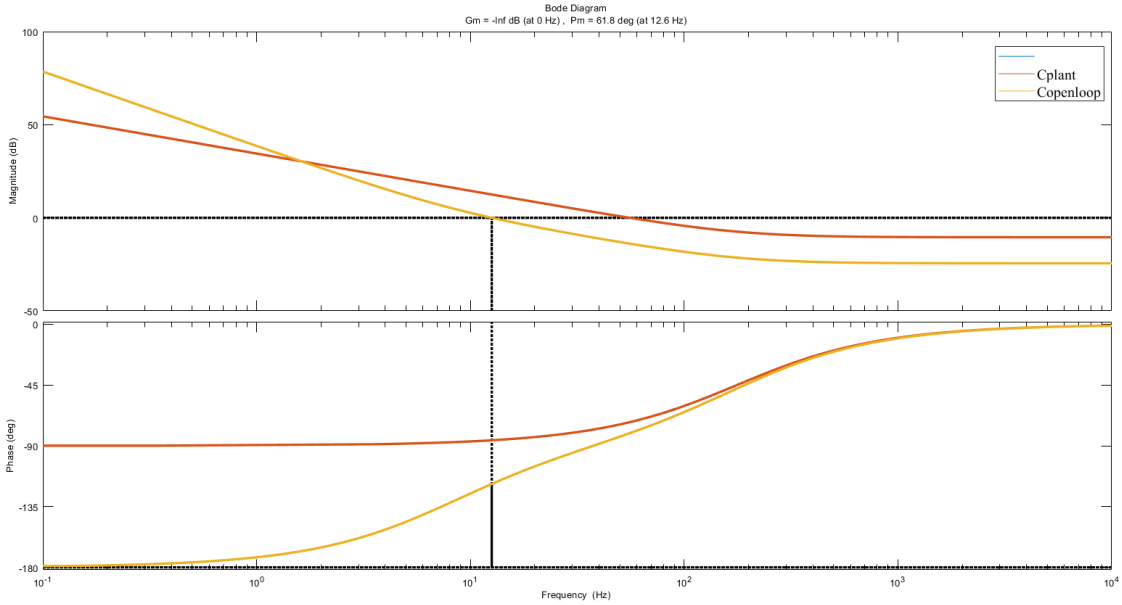


Figure 4- 11 Bode plot of voltage loop controller

4.2.2 Single phase grid-tied inverter modeling

For single phase system, the PLL is structured in a different way with additional orthogonal delay block to generate β axis signal which is shown in Fig 4-12.

The instantons power definition is also different

$$P = \frac{1}{2}(v_\alpha \times i_\alpha + v_\beta \times i_\beta) \tag{4-14}$$

$$Q = -\frac{1}{2}(v_\alpha \times i_\beta + v_\beta \times i_\alpha) \tag{4-15}$$

Despite these differences, the current controller and voltage controller is the same as three phase system since all the AC voltage and current has been transformed d-q frame.

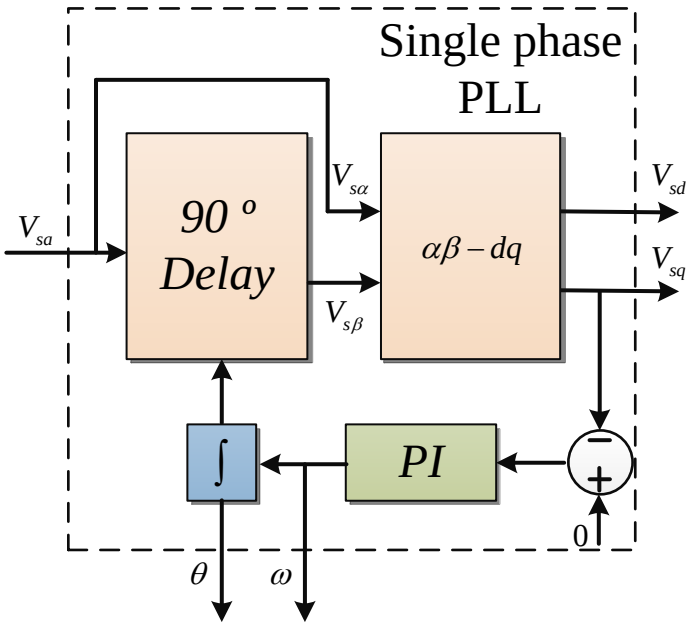


Figure 4- 12 Single phase phased-lock loop

4.3 Control Analysis for V2G mode

From the discussion above, we can find out that independent active power and reactive power control can be achieved by id and iq respectively.

The DAB is sending the phase shift information based on the active power command and the voltage levels sensed on both sides of the transformer which are shown in Fig 4-13 and Fig 4-14.

However, if the primary side DC bus voltage is not stable, power transfer would lose balance and leads to unstable even uncontrollable system.

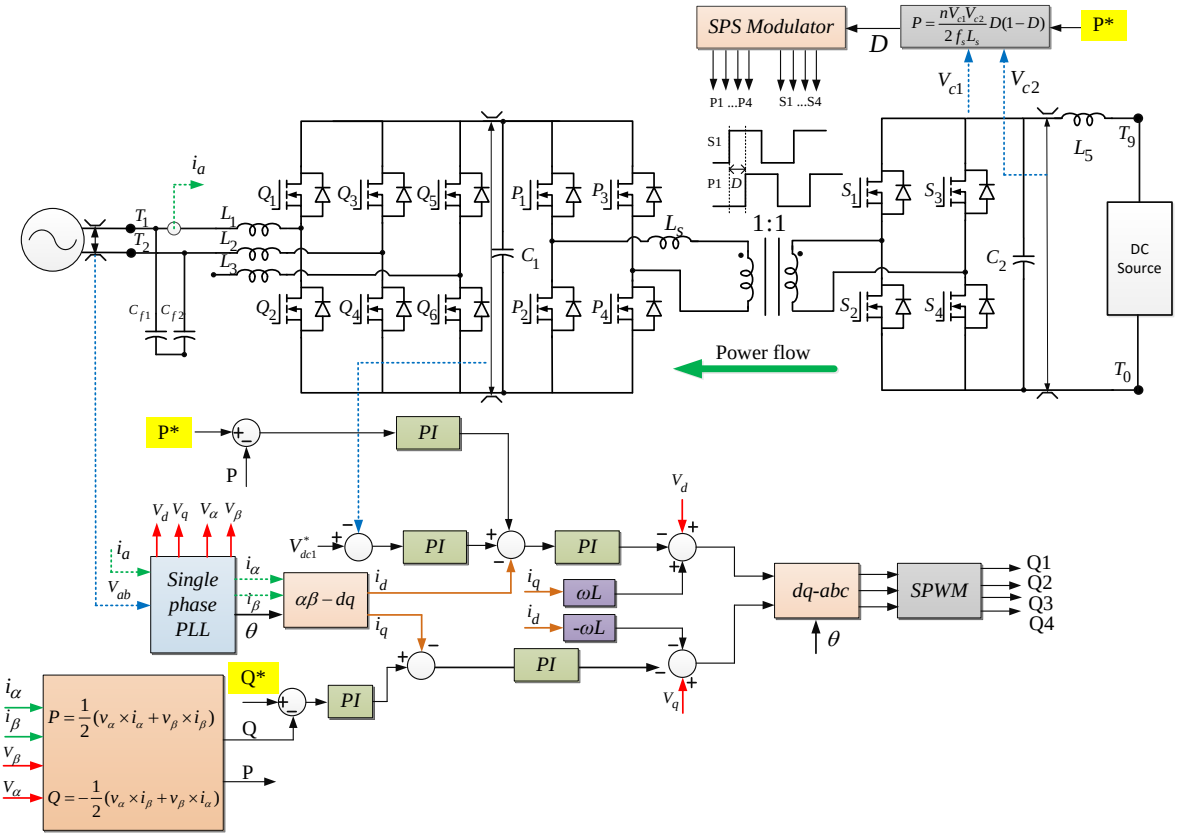


Figure 4- 13 Single phase V2G control diagram

Hence, there is of need to add another loop to regulate the DC link voltage in the inverter control. What is more, there is another option by regulating the DC link voltage through DAB. The difference of these two is not discussed in this thesis.

Another important factor to consider is the DC link voltage. In theory, the DC link voltage cannot be smaller than $\sqrt{2}V_{rms}$, and can be controlled by id. The value of that also matters to the following aspects:

- Current stress in DAB: As shown in Eq (4-16), the less difference between V1 and V2, current stress will be reduced which results in lower conduction.

$$i_{\max\_sps} = \frac{nV_2}{4 f_s L_s}[\frac{V_1}{NV_2} - 1 + 2\mathrm{D}] \tag{4-16}$$

  Hence, DC link voltage reference can be set to track the battery to bring down the conduction loss.

- Switching loss in inverter side: As show in Eq (4-17), the lower of Vds (the DC link voltage), the lower switching loss will be incurred.

$$P_{sw} = V_{ds} \times I_{out} \times f_{sw} \times t_{on} \tag{4-17}$$

  Hence, optimum decision needs to be calculated carefully to balance the switching loss and conduction loss reduction.

Three phase V2G control principle is only different from single phase V2G:

- Phase-locked loop design.
- Instantons power calculation.

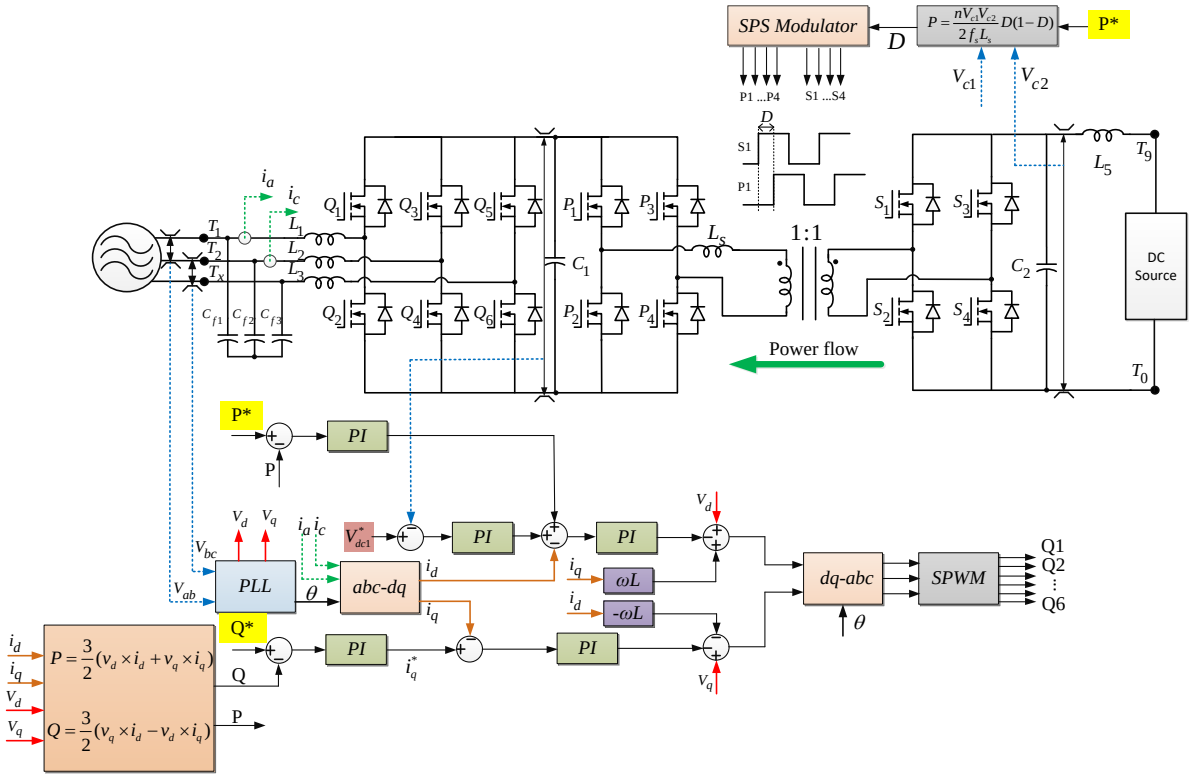


Figure 4- 14 Three phase V2G control diagram

4.4 Simulation and Experiment results

Since V2G is the most complicated scenarios, simulation study is performed first to verify the control algorithm.

4.4.1 Three phase V2G simulation results

Full scale Simulink simulation is constructed to verify the V2G control algorithm. High level 25kW active power command is given.

DC bus voltage is stabilized as shown in Fig 4-16 by additional control loop in the inverter current loop control.

Real power being sent to the grid is calculated based on the grid voltage and current shown in Fig 4-18.

Simulation Parameter	Value
DAB Switching frequency	100kHz
Inverter switching frequency	50kHz
Three phase Grid voltage	480V
Coupling inductor	10uH
DAB leakage inductance	22uH
Battery voltage	350V
Active power reference	25 kW
Reactive power reference	0 kVar
Primary DC bus voltage	700V

Table 4- 1 Three phase V2G simulation parameter

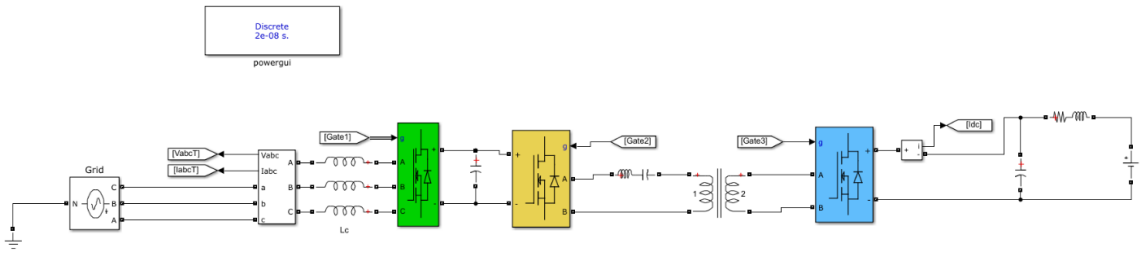
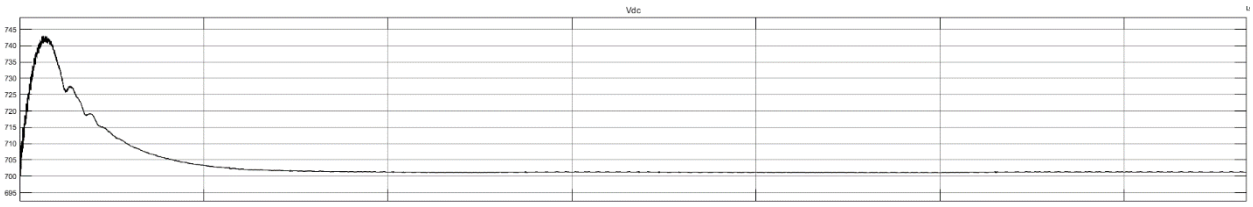
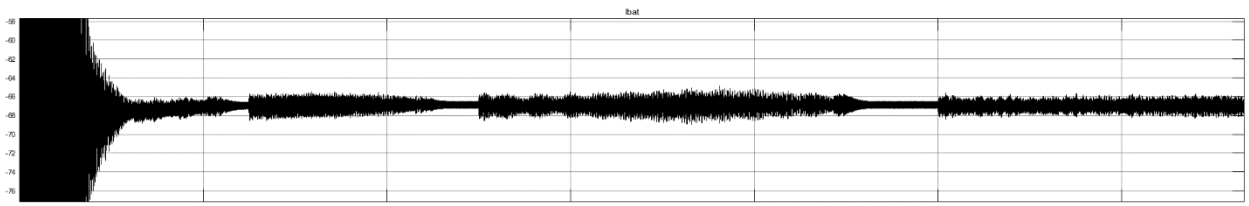


Figure 4- 15 Three phase V2G simulation



(Time is from 0 to 0.33 s)

Figure 4- 16 DC bus voltage during transients



(Time is from 0 to 0.33 s)

Figure 4- 17 Battery current

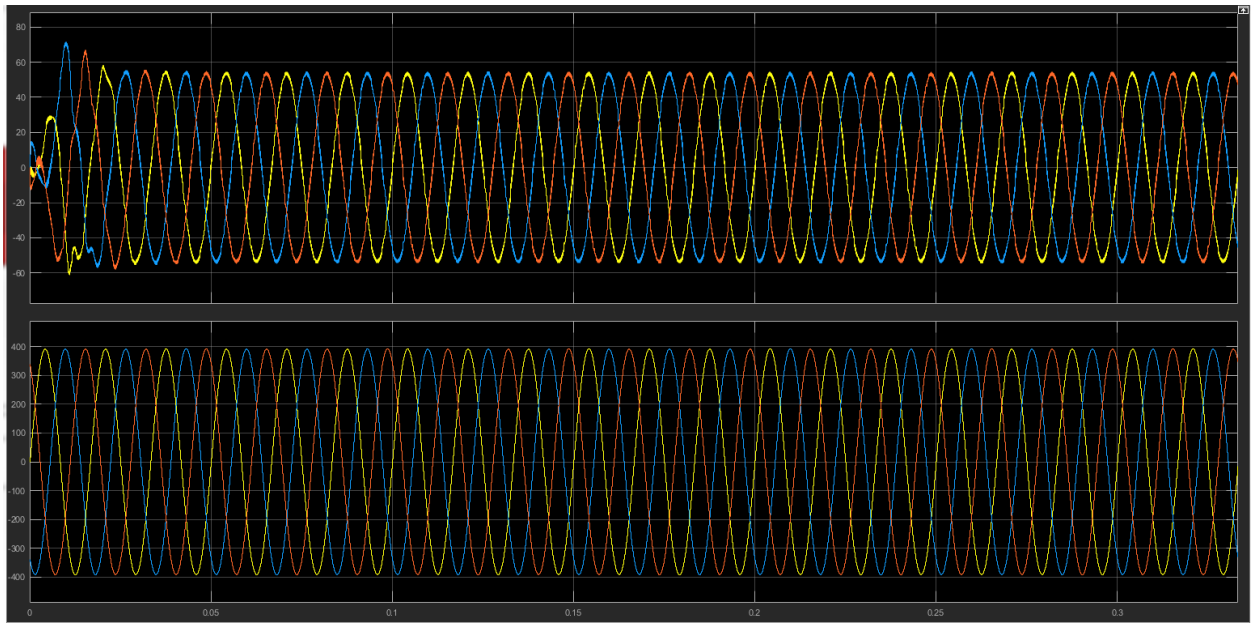


Figure 4- 18 Grid current and voltage

In this section, V2G operation has been analyzed and validated with simulation results.

Chapter 5 Grid to Vehicle (G2V) analysis and control

5.1 Operation principle of G2V charger

The power is flowing from the grid to the high voltage battery in this charging mode.

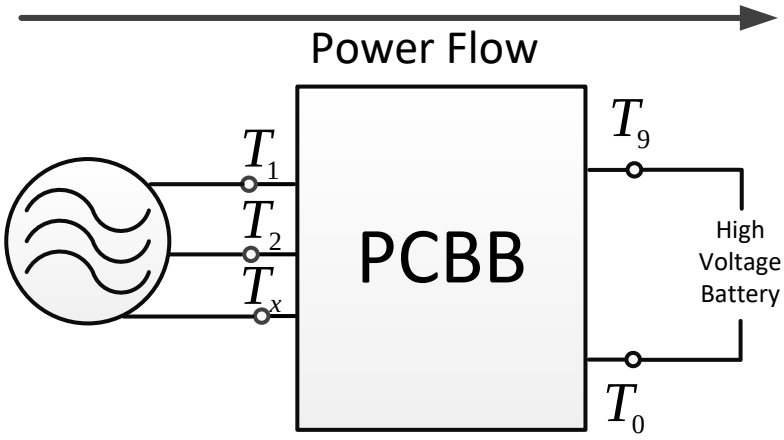


Figure 5- 1 Three phase G2V operation mode

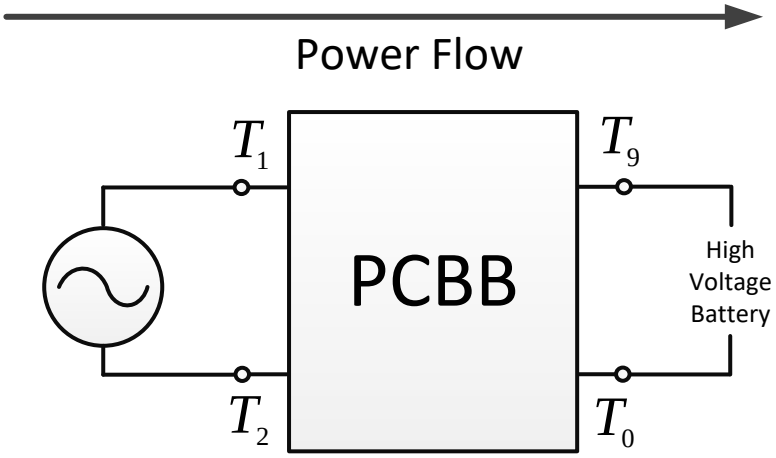


Figure 5- 2 Single phase G2V operation mode

For battery charging operation mode, there are two stages:

- Front end PFC: The job for this PFC is to regulate the current to reduce the line current distortion, and to control the power factor.

- Isolated DC-DC: The role for the DC-DC is to regulate the current (Constant current mode) or the voltage (Constant voltage mode) applied to the battery.

5.2 Control analysis of G2V mode

Control principle: As mentioned above, the two stages are decoupled. The DC bus voltage is controlled by the front-end active rectifier. The DAB is controlling the current or voltage by changing the phase shift (Note that the primary gating signal is leading under this mode).

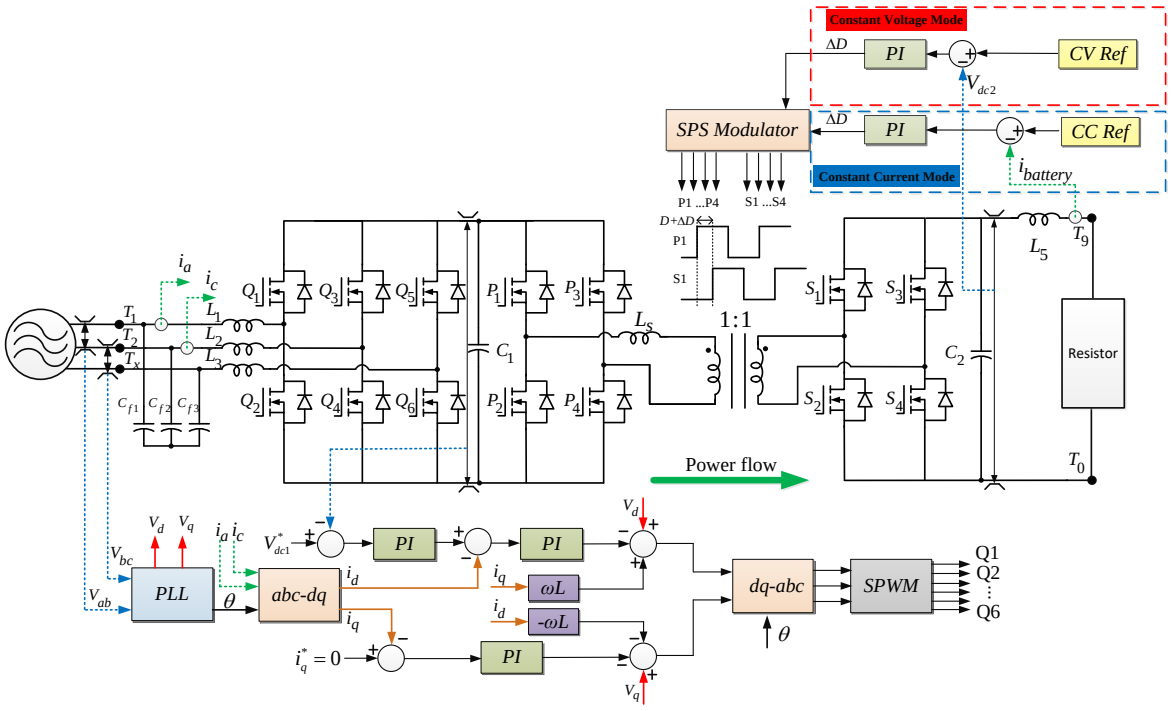


Figure 5- 3 Three phase G2V control diagram

In this section, the active power flow at any moment is flowing in one direction. The operation details of reactive power regeneration to the grid while the battery is being charged is not discussed in this section.

Both three phase and single phase G2V control diagrams are shown in Fig. 5-3 and Fig. 5-4.

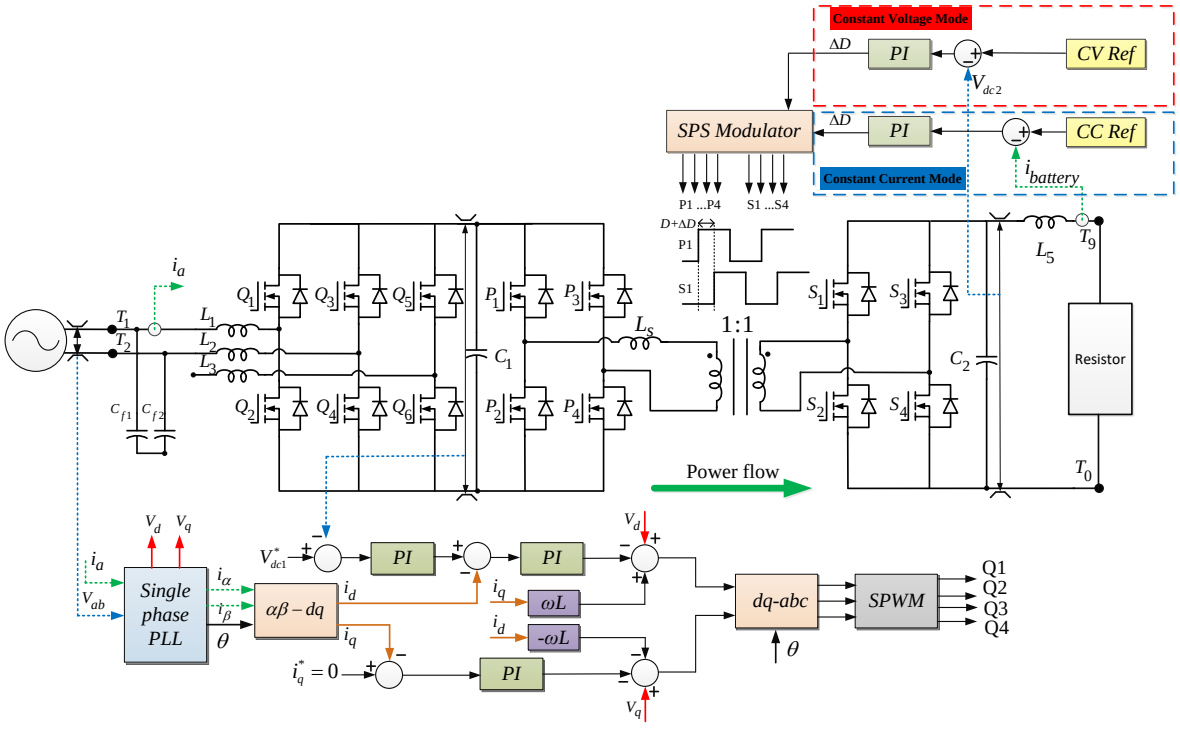


Figure 5- 4 Single phase G2V control diagram

5.3 Simulation and Experimental results

Since the PFC and DAB is decoupled from the aspects of control, testes and simulation are performed separately.

5.3.1 Three phase G2V simulation results

Simulation study is performed first for 3 phase system front end PFC.

Simulation Parameter	Value
Switching frequency	20kHz
Load resistance	10 Ω
Coupling inductance	1mH
Three phase Grid Voltage	240V
Kp	50
Ki	500
Voltage reference	400V

Table 5- 1 Three phase G2V simulation parameters

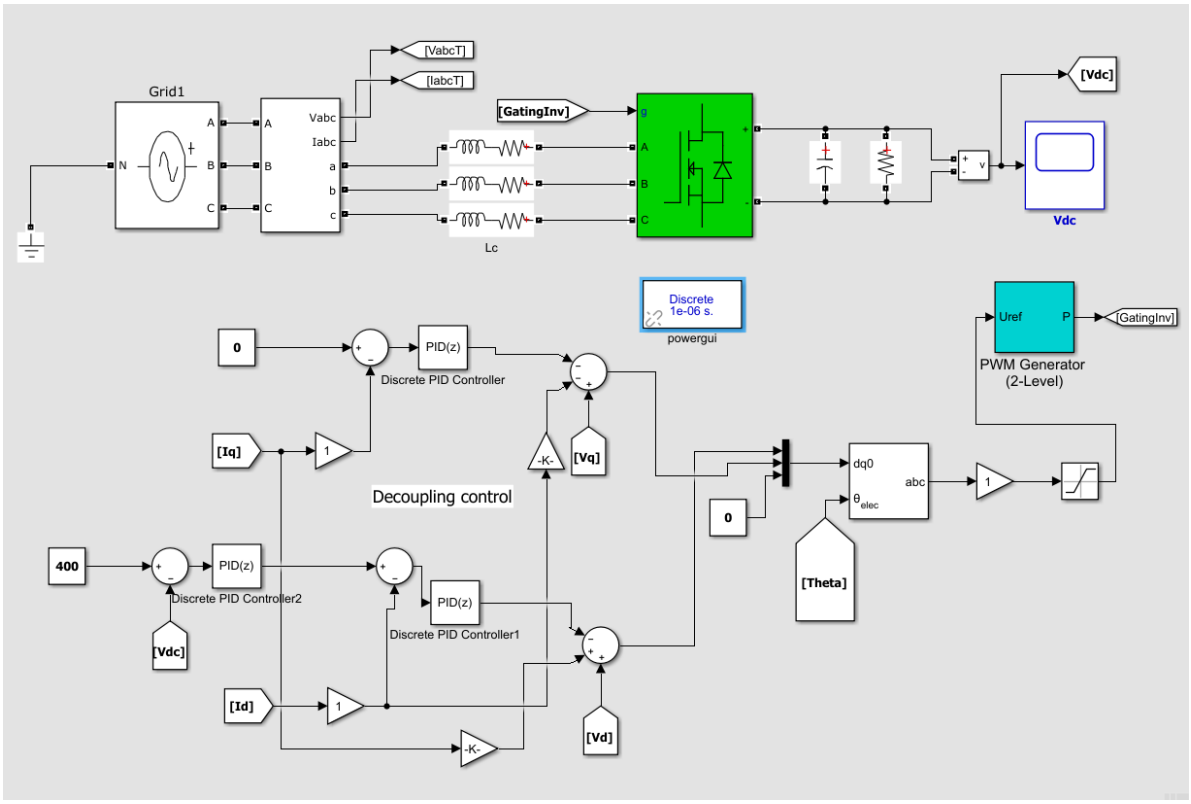


Figure 5- 5 Three phase active PWM rectfier simulation

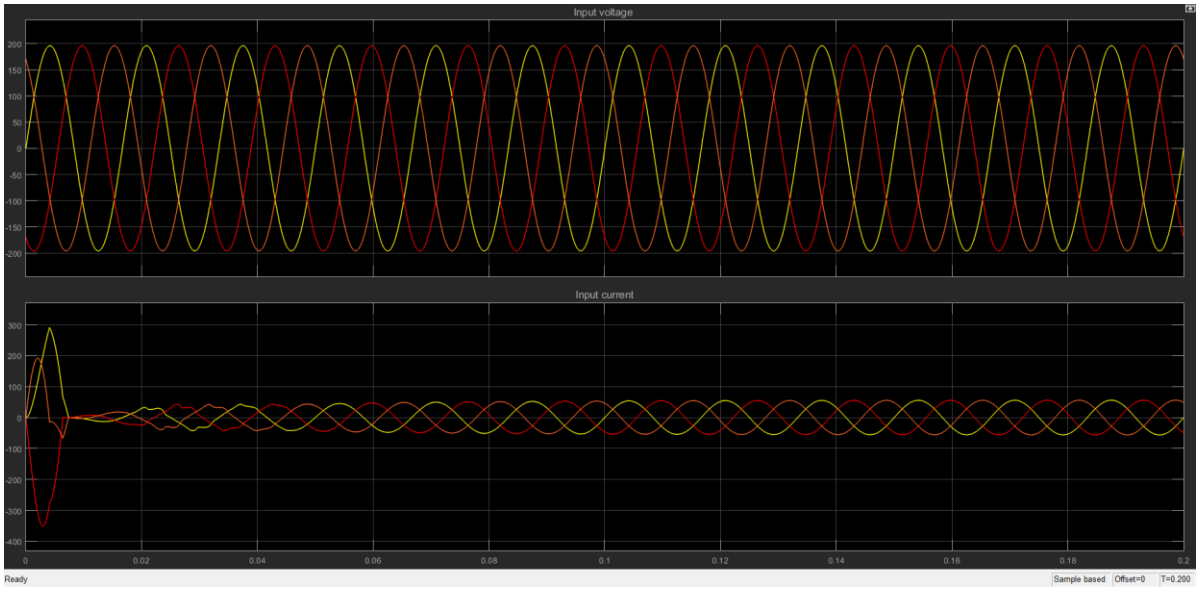


Figure 5- 6 Three phase PFC Grid voltage and current

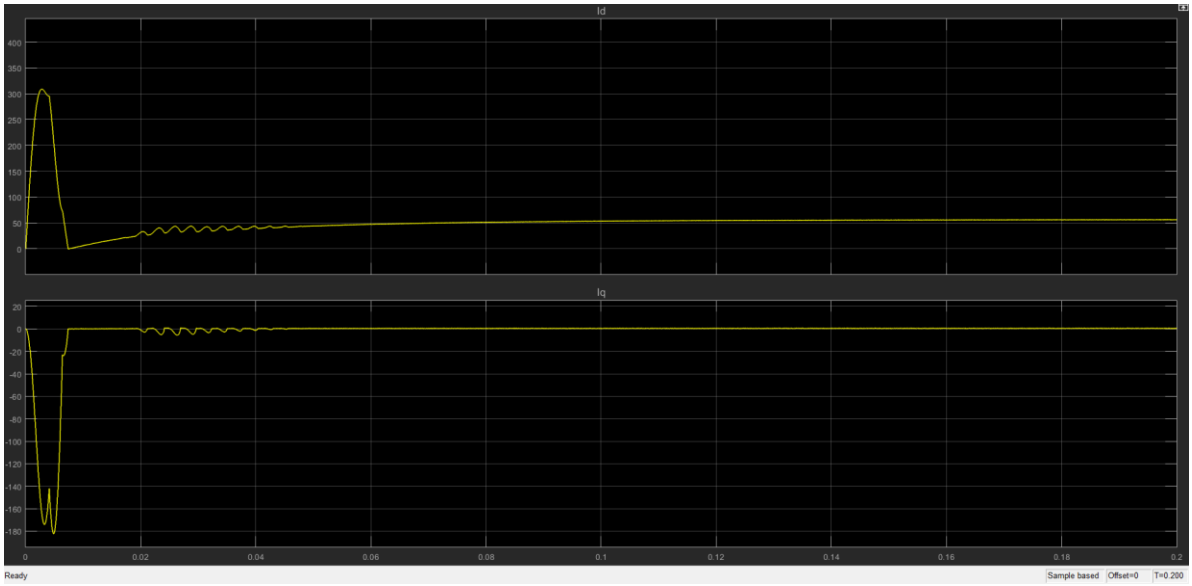


Figure 5- 7 Three phase Id and Iq current controller performance

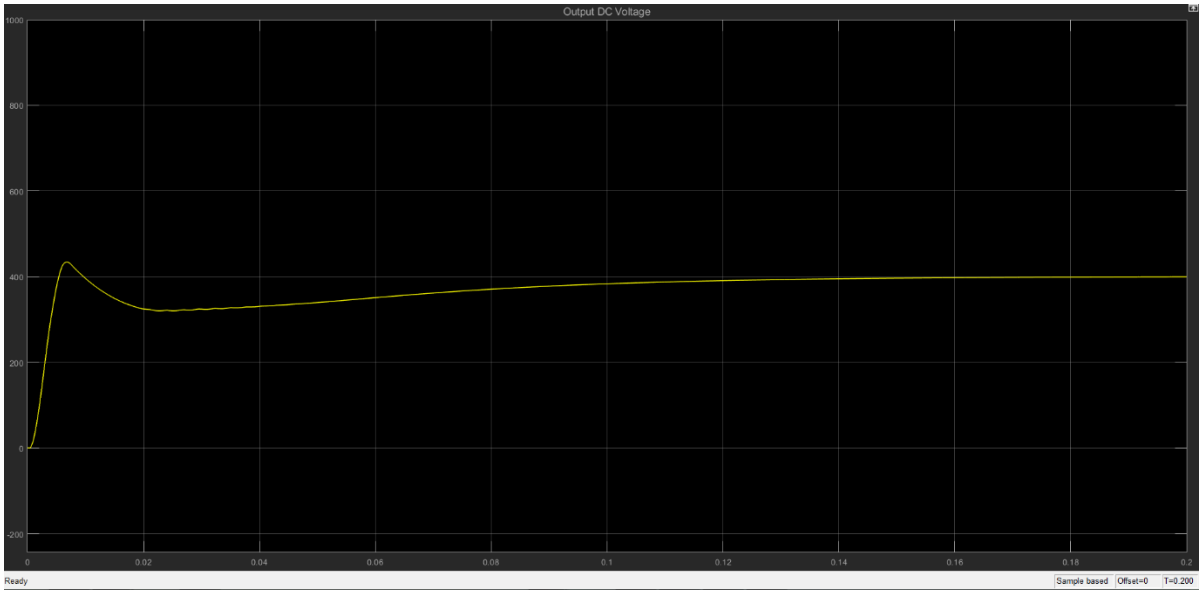


Figure 5- 8 Three phase output voltage

5.3.2 Single phase G2V simulation and experiment results

Before digital control was implemented, Simulink simulation is conducted first.

Simulation Parameter	Value
Switching frequency	20kHz
Load resistance	10 Ω
Coupling inductance	1mH
Single phase Grid Voltage	120V
Kp	50
Ki	500
Voltage reference	400V

Table 5- 2 Single phase G2V simulation parameters

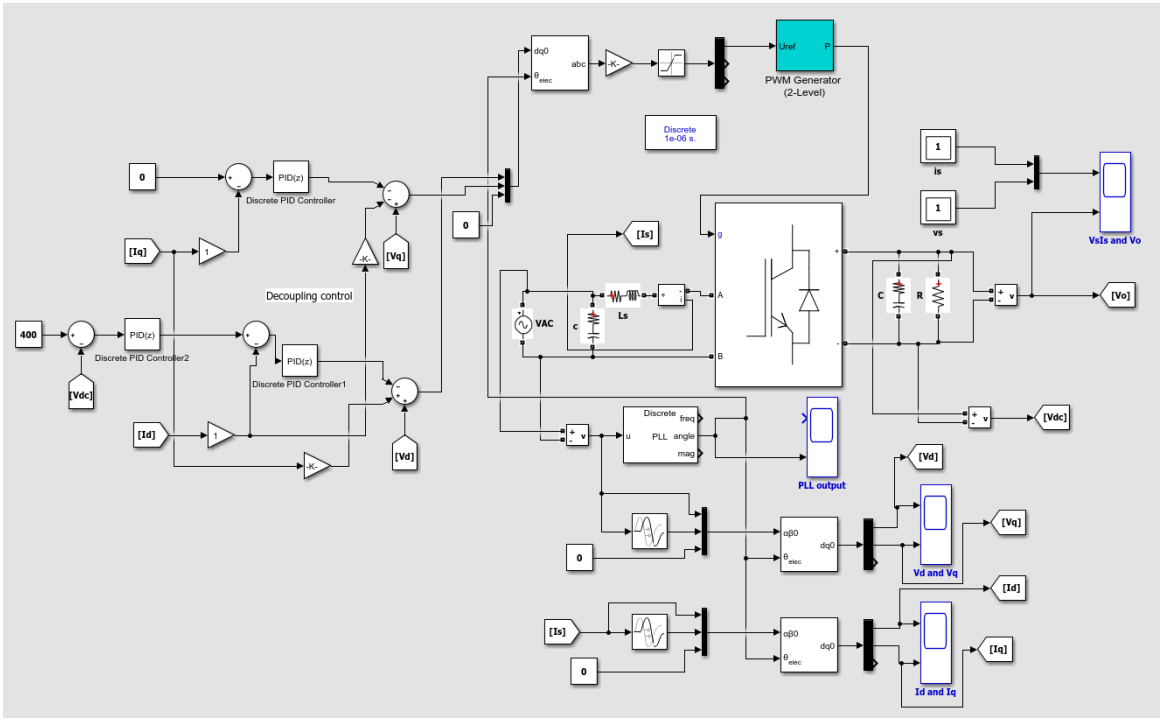


Figure 5- 9 Single phase PWM rectifier simulation

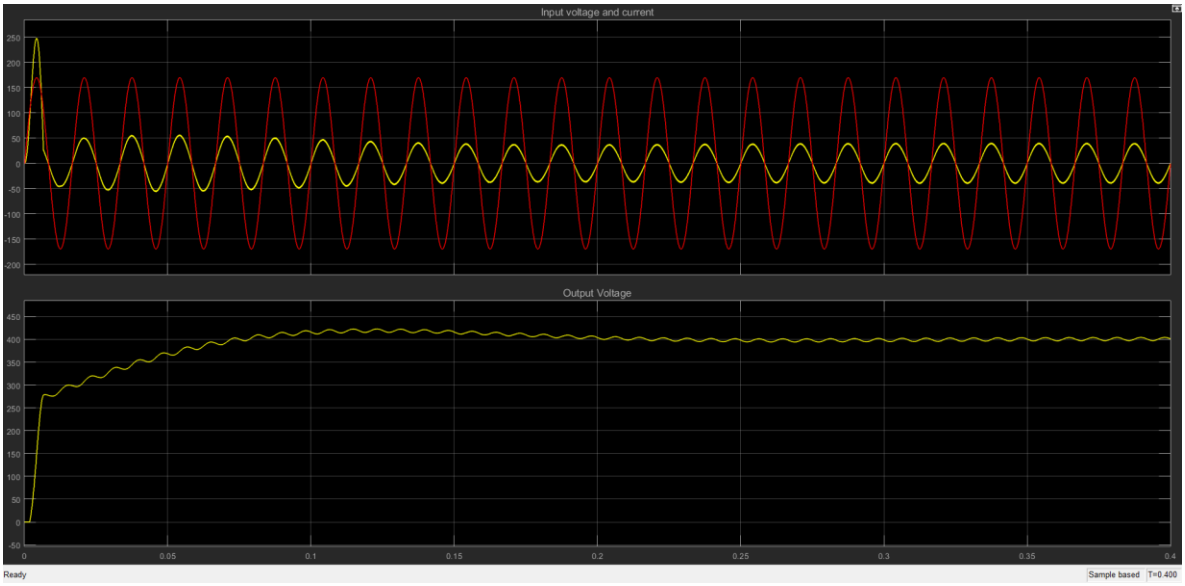


Figure 5- 10 Single phase grid voltage current (top) and output DC voltage (bottom)

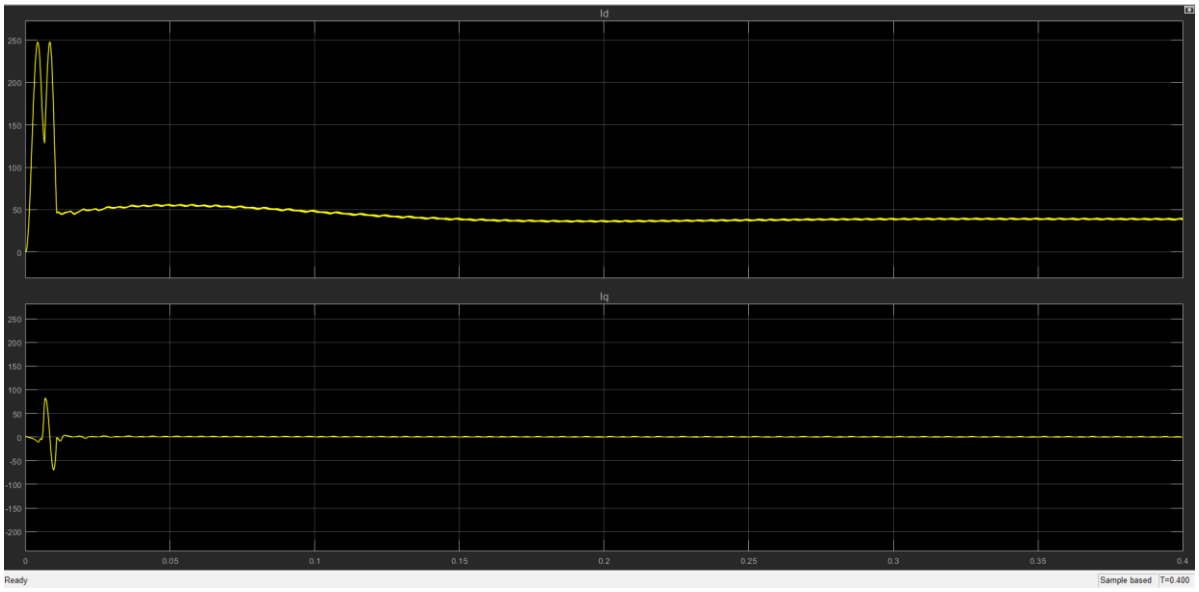


Figure 5- 11 Single phase id and iq current controller performance

Single phase G2V experimental results:

The first step for the PFC is to have a stable PLL. Hence, low voltage open loop test to calibrate the PLL is performed. From Fig 5-12, the inverter output is aligned with the grid voltage which means the PLL is working.

Hardware Setup	Value
Switching frequency	100kHz
Load resistance	27 Ω
Coupling inductance	100uH
Single phase Grid Voltage	120V
Kp	0.1
Ki	15
DC Voltage reference	160V

Table 5- 3 Single phase G2V hardware test parameters

However, the current is adversely distorted. That is why a closed loop current controller is needed as shown in Fig 5-4.

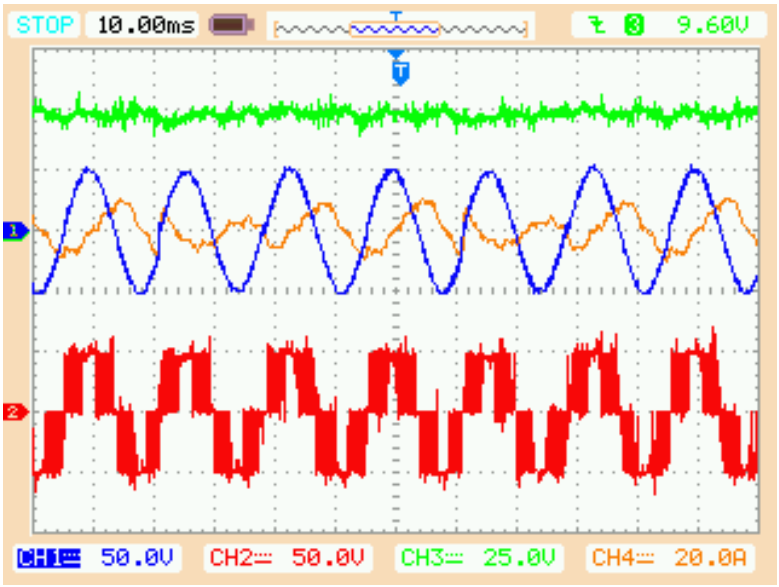


Figure 5- 12 Verification of PLL

Ch1 grid voltage; Ch2 Inverter output; Ch3 grid current; Ch4 DC bus voltage

Fig 5- 13 shows the result after a PI current controller is added into the loop. The current is in phase the grid voltage which is the unity power factor that is desired. However, the high frequency distortion is obvious. Fine tuning for the PI gain is performed and the result is shown in Fig 5-14 which clearly shows less distortion.

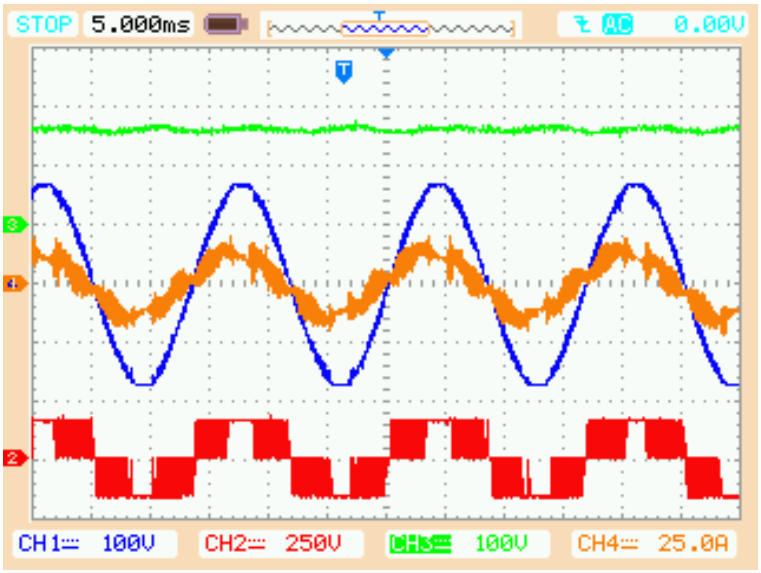


Figure 5- 13 Noisy Current controller

Ch1 grid voltage; Ch2 Inverter output; Ch3 grid current; Ch4 DC bus voltage

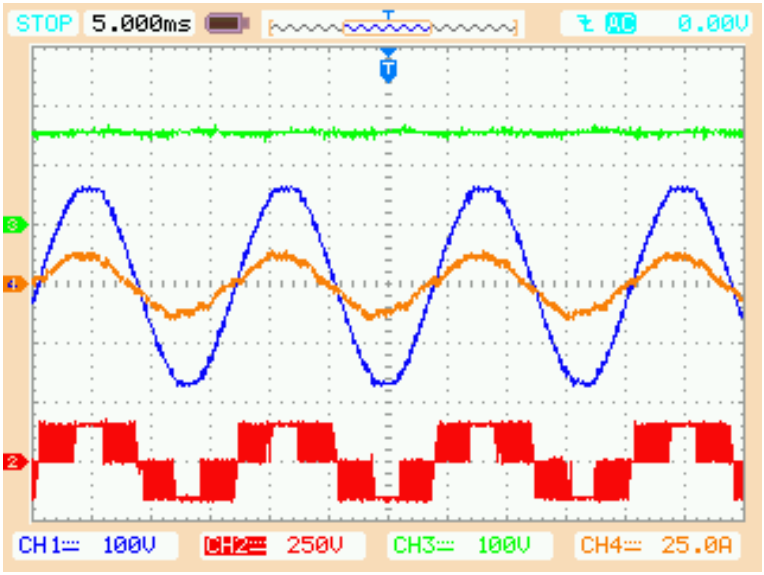


Figure 5- 14 Working current controller

In this section, the operation of single phase and three phase G2V has been analyzed and validated by the experimental results.

Chapter 6 Conclusions, and Future work

6.1 Conclusions

- Robust gate drive with comprehensive protection feature was proposed. Its performance is tested under 600V/130A.
- Proposed optimal parameters design for isolation transformer to cover universal operation modes (3phase or single-phase V2X and G2V).
- Proposed a generalized transformer design method and tested the transformer to verify the design.
- Proposed the closed loop control algorithm for V2L working with both AC and DC load. Verified the control algorithm for AC load under 1kW total system power rating.
- Proposed the closed loop control algorithm for V2G working with both single-phase and three-phase including independent P-Q control (active and reactive power). Verified the control algorithm with Simulink.
- Proposed the closed loop control algorithm for G2V working with both single phase and three-phase. Verified the control algorithm with Simulink.

6.2 Future work

Future work can be made in the following aspects:

- The accurate modeling of leakage inductance in transformer design is very important. Finite element analysis is a good approach for the leakage inductance estimation and modeling.
- Use dual phase shift and other for wider ZVS (zero voltage switching) range is the Dual Active bridge stage to further reduce the switching loss.

- Configure the AC side switches to Totem-pole PFC to be compared with PWM PFC in terms of efficiency and passive components size.
- Design coupled inductor for the LC filtering instead of using three independent inductors to further reduce the passive component size.
- Analyze the influence on DC link voltage ripple by using different modulation methods on the inverter switches such as SPWM and SVPWM.
- Perform small signal analysis for the DAB bridge and design the controller analytically.
- When regulating the primary side DC bus voltage under V2G/G2V operating modes, there are two ways either by controlling the inverter/PFC or controlling the DAB. Study the control difference between using between these two options in terms of system stability.
- When operating under V2L modes, the control methods for providing stiff sinusoidal voltage output with nonlinear load and imbalance load. And there are some suggested approaches such as:
    - ✓ Apply repetitive current or predictive control methods to perform fast tracking of the distorted current to do the dynamic compensation.
    - ✓ Apply the fourth phase leg to absorb the negative sequence current.
- There lacks EMI filter in the system on both grid side filter such as common mode choke and battery side filter for example, Y cap.
- The battery has an operating range not a fixed voltage. To maintain low current stress inside DAB, the primary voltage and secondary voltage needs to be as same as possible. What is more, the primary side voltage also can be determined by the grid

when operating under V2G/G2V. It would be very important to find the optimum DC bus voltage to reduce the switching loss on both stages.

- The transformer's leakage inductance value is a very important factor when it comes to system optimization since it affects the power transfer, ZVS region, and maximum current stress. Besides that, the switching frequency of both inverter and DAB is another factor determining the system optimum operating point. It is necessary to generate an objective function for $PowerDensity = f(f_{inv}, f_{DAB}, V_{dc1}, L_s)$
- V2X operation will put extra stress on the battery pack and some future work should be put into this aspect to quantify the negative effect due to the V2G or V2L operation.

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