

SOLUTIONS TO IMPROVE ELECTRIC VEHICLES' PLUG-IN AND WIRELESS CHARGERS

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ABSTRACT

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With the present trend of reducing carbon emissions to the environment, electric vehicles (EVs) have become a popular topic for the scientific community and automotive-related industries. In order to increase the number of EVs on the road, customers' main concerns: driving range, charging time, and vehicle price need to be addressed. These concerns can be resolved in a variety of manners, ranging from improving the chemistry to the charging units of the EV battery. This dissertation focuses on advancing the two types of charging units: plug-in and wireless, particularly improving the following crucial features: efficiency, reliability, size, and cost.

The first half of the dissertation offers solutions for the plug-in technology, specifically in the power levels of extreme fast chargers (XFC), which will charge EVs within 10 minutes. Current XFC stations have a fixed charging-port configuration (CPC), using a single port to charge any EV type, which requires their power converters to be larger and more expensive than likely necessary. In this dissertation, a 13.8kV, 1.2MW XFC system with a CPC that adapts in response to the types of EVs connected is proposed. Theoretical analysis shows that the proposed CPC allows a station to have a 40%-66.7% smaller power rating compared to one using the conventional CPC, thus achieving a less expensive and smaller system.

For safety reasons, the proposed XFC station as well as conventional plug-in chargers isolate EVs from the power grid with high-frequency transformers (HFTx), which are one of the most heavy, bulky, and inefficient components in the station. Traditional methods to specifically reduce the HFTx's core loss are limited to their design and manufacturing, and typically rely on

complex optimization algorithms. An online-based approach to reduce this loss is proposed in this dissertation, which relative to the conventional methods, is less time consuming to implement and can be easily applied in existing stations. Theoretical analysis and simulation results from ANSOFT Maxwell show a core loss reduction of 50% at light load, and of 80% at full-load.

The second half of the dissertation presents solutions for the wireless technology, which enables EVs to re-charge while driven. Conventional single-phase wireless chargers rely on a two-stage power conversion to perform power factor correction (PFC) and to regulate power flow. To absorb the inherent “ 2ω ” ripple flowing in the system, a large dc-link capacitor is used; which is sized with an equation that relies on a single operating condition. This sizing approach may cause reliability issues, and can inadvertently suggest that the station needs a larger and more expensive capacitor than needed. To overcome this limitation, this dissertation proposes a simulation-validated generalized equation that accounts for system control variables and the whole load range.

The conventional two-stage charger inherently possess the following drawbacks: 1) extra semiconductor devices, as well as their corresponding heat sinks and control circuitry, and 2) any accidental shoot-through in the dc-link can destroy the circuit. To eliminate the size, cost and power loss related to these semiconductors while improve the system reliability, a Z-source-based wireless charger is proposed. Not only does the proposed charger performs PFC and regulate the power to EVs in a single stage, it is also immune to shoot-through states. The system’s operation was experimentally validated, where a 0.987 power factor was achieved at full-load condition.

The ideas presented in this dissertation provide designers with solutions that will ultimately lead to safer chargers and/or benefit the budget of EV owners and automotive-related industries. The solutions for plug-in chargers are helpful to accelerate mass adaptation of EVs, while the ones for wireless are more convenient in the long run.

Dedicated to my beloved wife (Mayra A. Rivas-Rocha) and parents
(Ramón L. González-Pagán and Rosa B. Santini-Pérez), as well as the memory of
Josué López-Alejandro and Ramón L. González-Torres.

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KEY TO ABBREVIATIONS

AC	Alternating current
CMI	Cascaded multilevel inverter
CP	Charging-port
CPC	Charging-port configuration
CS	Charging scenario
DC	Direct current
DAB	Dual-active-bridge
EV	Electric vehicle
HFTx	High-frequency transformer
MV	Medium-voltage
NoP	Number of ports
PE	Power electronics
PEC	Power electronics converter
PF	Power factor
PFC	Power factor correction
RN	Resonant network
THD	Total harmonic distortion
WPT	Wireless power transfer
XFC	Extreme fast-charger

Chapter 1 Introduction

1.1 Why Working on EV Chargers?

With the present trend of reducing carbon emissions to the environment, electric vehicles (EVs) have become a popular topic for the scientific community and the automotive-related industries. The main target is to increase the number of EVs on the road, while decreasing the number of conventional fuel-cars. For this to happen, customers' main concerns need to be addressed, which include: 1) lower vehicle cost, 2) longer driving range, 3) faster charging time, 4) higher number of charging stations. All these need to get to the point where they are similar or better compared to their analogue in conventional fuel-cars, where battery chemistry as well as the EV chargers hold the key for this to happen [1]. Specifically, improving battery chemistry will help with the first three concerns (and indirectly the fourth one), while improving EV chargers—which is the focus of this dissertation—will directly help with the four of them.

1.2 Top-level Description between the Two Types of EV Chargers

There are two types of EV chargers: plug-in, and wireless. In general, the plug-in technology is widely implemented today, thus, helping towards mass adaptation of EVs; while the wireless technology is more convenient in the long run. A top-level comparison between these, and the way they can help address the customers' concerns is provided in the following subsection.

1.2.1 Plug-in

As the word implies, the plug-in technology requires users to manually connect the EV's to the station's charging-port (CP). This not only can represent an electrical hazard in weather such

like rain and snow, but the wires can be: messy, tripping hazards, and too heavy to carry. The latest will be especially cumbersome if the user is using an extreme fast-charging (XFC) station (a type of station that will soon become available to address concern number three in the previous section), which relies on high-power (and current) levels to charge EVs within ten minutes. In addition, if the charger is in a household or parking facility, the possibility always exists of the user forgetting to connect the car. On the other hand, if an off-board-type charger is used (needed to support the power to fast-charge the EV), no weight is added to the car. Also, the technology is well-developed, approaching maturity, and standards (e.g., SAE J1772, SAE J2894) for implementation have been well-defined for a while [2]; these being the main reasons the plug-in technology is the one widely implemented today.

1.2.2 Wireless

In the wireless technology, the user does not need to “plug” the car since a charging coil is on the ground transferring power wirelessly to a “pickup” coil located at the bottom of the EV, as shown in Figure 1.1. This overcomes all drawbacks mentioned for plug-in chargers. Also, because power can be transferred through a large airgap (10cm-25cm), this technology allows the concept of roadway-powered EVs [3], where an EV can be re-charged dynamically, boosting the battery state of charge each time the car goes through a charging coil, thus, extending its driving range. With dynamic charging, a proper energy storage and charging system design could reduce 20% of an EV battery capacity, minimizing the price of this car compared to EVs with plug-in chargers [4]. Therefore, the wireless technology will inherently be able to address the first two customers concerns mentioned in the previous section. However, the infrastructure of the dynamic charging feature is challenging and expensive to implement in an existent road [4], [5]. Another problem with the wireless technology is that the efficiency will drop dramatically if the two coils are not

well-aligned. Also, as opposed to the off-board-type plug-in charger, some power converters as well as a charging coil need to be placed inside the EV. Although benefits of using wireless outweigh the plug-in charger, the technology is still emerging [2]. In addition, its standard (SAE J2954), which came out in 2016, is still incomplete and only considers stationary applications, up to 11kW. These being main reasons why this technology is not presently widely used commercially, but in the long run, it will take over plug-in chargers mainly due to convenience.

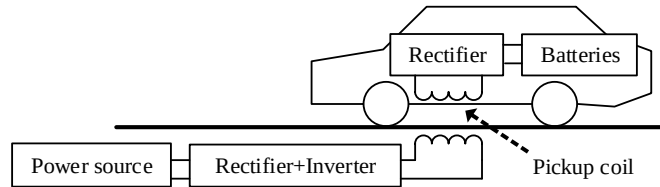


Figure 1.1 EV wireless charger top-level configuration.

1.3 Research Objectives and Contributions to the Field

It can be seen from the descriptions made in the previous section, that while in different timeframes, the two charging technologies are important, which is why both of them are addressed in this dissertation. Specifically, the presented research makes improvements in their following crucial features: efficiency, reliability, size, and cost. Higher efficiencies are needed so as to not have significant power wasted, especially when more EVs on the road means more power demand from charging events that can be very challenging to meet [6]. Reliability always plays an important role so as to keep the customer and electrical equipment safe, as well as a to keep the charger operating without anomalies. Charger size is important, especially if it is to be placed in urban areas where space is limited, as well as if some portion of it is inside the EV. Cost will alleviate the budget of many, including: customers, automotive-related industries, and station owners. The combination of all these have a direct impact in addressing the customers' concerns.

The specific contributions this dissertation makes into the field are as follows:

1. The proposal of a 13.8kV, 1.2MW plug-in XFC system with a charging-port configuration (CPC) that adapts in response to the types of EVs connected to the station. Theoretical analysis shows that the proposed CPC allows a station to have a 40%-66.7% smaller power rating compared to one using the conventional CPC (which is fixed), thus achieving a less expensive and smaller system. Simulation results validate the system's operation, which includes charging multiple types of EVs while keeping balanced utility currents and unity power factor. The exact details and literature review are found in Chapter 2.
2. The proposal of an online-based approach to reduce high-frequency transformer (a component used to provide grid/EV isolation for safety in a plug-in charger) core loss. Relative to the conventional methods (which rely on transformer design, manufacturing, and optimization algorithms), is less time consuming to implement and can be easily applied in existing stations. Theoretical analysis and simulation results show a core loss reduction of 50% at light load, and of 80% at full-load, thus, helping improve the charger's overall efficiency. The exact details and literature review are found in Chapter 3.
3. The proposal of a generalized equation for the dc-link capacitor sizing in conventional two-stage wireless chargers. As opposed to the conventional equation, the proposed one accounts for system control variables, the charger topology, and the whole load range. The simulation-validated equation improves system reliability and avoids oversizing the capacitor. The exact details and literature review are found in Chapter 4.
4. The proposal of a Z-source-based wireless charger which allows for power factor correction and power flow regulation in a single stage. It eliminates the size, cost and

power loss related to the needed semiconductors in the conventional two-stage charger while improve the system's reliability. The system's operation was experimentally validated, where a 0.987 power factor was achieved at full-load condition. The exact details and literature review are found in Chapter 5.

Chapter 2 Plug-in Medium-Voltage Extreme Fast Charger with an Active Charging-Port Configuration that Achieves a Low-Cost System

2.1 Background

Availability of public extreme-fast charging (XFC) stations have been commonly cited to be one of the main ways to reduce driving-range anxiety of EV owners and accelerate mass adaptation of EVs [1]. The station must charge an EV within ten minutes, which according to the definitions of EV types summarized in Table 2.1, it can accomplish it by supplying at least 400kW to a small-sized (S_{EV}) demanding full-load power. Therefore, the station must be rated to at least 1.2MW if three of these EVs are to be charged simultaneously. At this power level, it is not convenient to connect the charger to the low-voltage grid because it will draw large amount of currents which degrades the system's efficiency, and since it requires a bulky step-down distribution transformer which increases the size and cost of the charger. To address these issues, direct connection to the medium-voltage (MV) grid (4.16kV ~ 13.8kV) through multilevel inverters has been the common approach and converters used to design the XFC stations [7]–[10], thus, they are the focus of the following literature review.

Table 2.1 Definition of EV types in this study

EV Type	Battery Capacity
Small (S_{EV})	$\leq 65\text{kWh}$
Medium (M_{EV})	$> 65\text{kWh}$ but $\leq 130\text{kWh}$
Large (L_{EV})	$> 130\text{kWh}$

The authors in [7] proposed a charging station that is composed of three cascaded multilevel inverters (CMIs) (one per phase) with three charging-ports (CPs), one for each CMI. Due to its fixed charging-port configuration (CPC), if a large-sized (L_{EV}) is to be charged, at least one CMI has to handle the power for it. In addition to this, the isolated DC/DC converter in each cell of the CMI is unidirectional (thus there is no vehicle to grid power flow capability); no strategy is addressed for the unbalanced utility currents created by the different charging requirements for the vehicles connected to the CPs; and no strategy is addressed to improve the power factor that will mainly be degraded by the interface inductance. The same authors made improvements to their topology in [8], where bidirectional power flow is possible, and each CMI can equally share the total power demand since they are all connected to a common dc-link; thus, balanced utility currents can be inherently achieved. However, unless the charging station is unpractically designed for a single CP, a redundant DC/DC converter needs to be added at each CP to accommodate for different EV power demand, where at least one of them need to be rated for a L_{EV} . Also, no control strategy is addressed to correct the grid power factor. A very similar topology with the same issues is found in [9].

In [10] an EV charging station consisting of a neutral point clamped (NPC) multilevel converter and with bidirectional power flow capability is proposed. Using such kind of multilevel converter incurs in excessive number of semiconductors for high number of levels [11], which is needed for direct connection to the MV grid. Also, the NPC have to handle the charging station's rated power (at least 1.2MW based on the earlier explanation). Also, as in [8] and [9], this charging station requires each CP to be connected to an individual DC/DC converter, where at least one must handle power for a L_{EV} . These additional converters also increase the size, cost and degrade the system's efficiency.

In [12], a charging station based on a cascaded AC/AC converter, with multiple CPs, common dc-link, and bidirectional power flow capability is proposed. The major drawbacks in this charging station are that the AC/DC converter has to handle the station's rated power, at least one of the redundant DC/DC converters have to handle the power demand of a L_{EV} , and there is a large number of magnetics.

Very recently, the authors in [13] presented an XFC station based on a delta-connected CMI. This topology was introduced by our research group in the past [14] to overcome the wye-connected structure limitation of keeping both balanced utility currents and unity power factor. The advantage of the delta structure compared to wye was further addressed in [15]. Although the XFC station can charge multiple types of EVs while keeping balanced utility currents with unity power factor, it still uses a fixed CPC, thus, at least one of its CMIs have to be rated for a L_{EV} .

The disadvantages mentioned above negatively impact the size, cost, and efficiency of the XFC station, and/or the grid performance. To address the aforementioned drawbacks, a 1.2MW, 13.8kV XFC station based on a delta-connected CMI [14] and an active CPC is proposed in this dissertation. The charging station, shown in Figure 2.1, is controlled so as to supply power to different types of EVs simultaneously while keeping balanced utility currents and unity power factor at the grid. Also, the charger has three ports ($DC_{ab1,2}$, $DC_{bc1,2}$, $DC_{ca1,2}$) that, as opposed to [13], are proposed to be actively re-configured so that it can: 1) charge up to three S_{EV} simultaneously; 2) charge up to one S_{EV} and one medium-sized EV (M_{EV}) simultaneously; 3) charge only a L_{EV} . Due to the proposed CPC, the CMI in each phase can be rated for a S_{EV} even though the XFC unit is able to charge a L_{EV} . This makes the power electronics converter (PEC) in the station to be cheaper, smaller, and lighter compared to the existing XFC stations. The

theoretical validation of these claims as well as tradeoffs are detailed in the next section of this chapter.

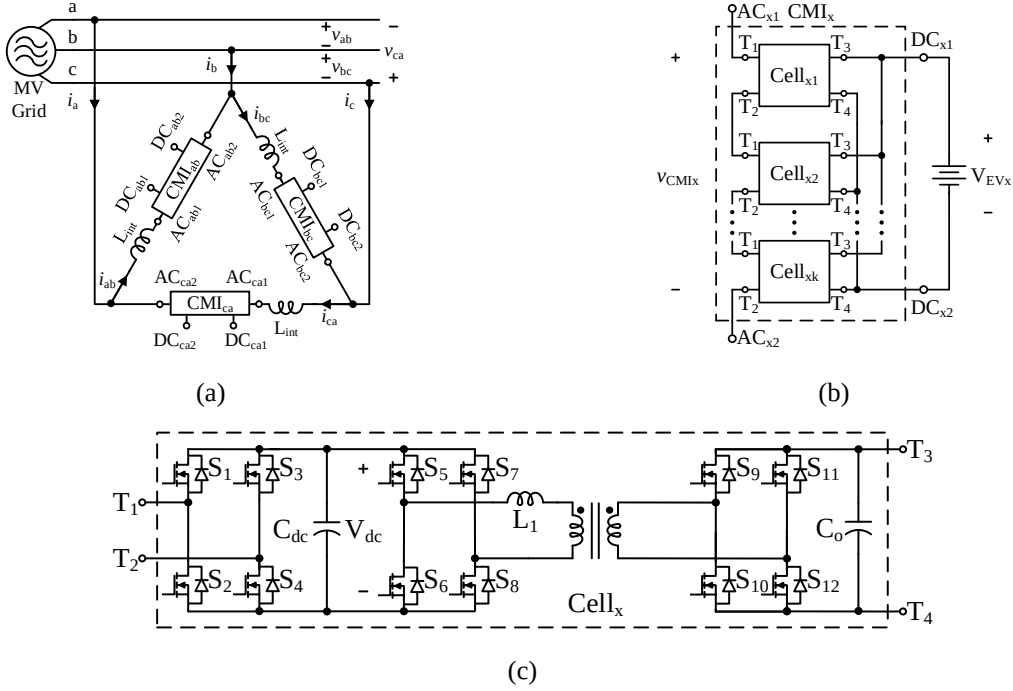


Figure 2.1 Proposed XFC charging station unit: Top-level configuration (a), CMI configuration (b), CMI cell configuration (c), where k is the CMI's total number of cells and $x = ab, bc, ca$.

In addition to the features mentioned above, the proposed XFC unit is able to: 1) withstand direct connection to the MV since each cell in the CMIs is connected in series at the input, 2) supply the high current needed to charge the EVs with low current per cell since each cell in the CMIs is connected in parallel at the output, and 3) support grid-to-vehicle and vehicle-to-grid applications since the CMIs' cell allows bidirectional power flow. Detailed advantages of using CMI in this application can be found in [16], and of using DAB for each cell can be found in [17].

2.2 Theoretical Comparison of the Proposed and Conventional Charging-Port Configurations

Current XFC stations use a fixed CPC (see Figure 2.2 for a general example), so a PEC in direct connection to a CP is forced to take on the full-power flow, and therefore, need to be rated

according to the EV (or maximum power demand) that is allowed in that port. This means that since it is desired to charge any EV type within ten minutes, at least one of the station's PEC need to be rated for a L_{EV} . This will be the case for at least one AC/DC in Figure 2.2a, and at least one DC/DC in Figure 2.2b. This does not hold true for an XFC station using the proposed active CPC since its configuration adapts based on the EV type being charged. Specifically, it utilizes a single CP for a S_{EV} , two in parallel for a M_{EV} , and three in parallel for a L_{EV} . This can be better visualized in Figure 2.3, which shows the proposed CPC being applied to the typical XFC configurations (not using common dc-link (a-c), and using common dc-link(d-f)). Doing this allows the PECs in the XFC station to be rated as for a S_{EV} while being able to charge any EV type, thus, the PECs in the station achieve a lower power rating compared to the ones in a station using the fixed CPC. The main tradeoff to consider is the power rating versus charging scenarios, which is why more detailed comparison regarding these aspects are provided in the next subsections.

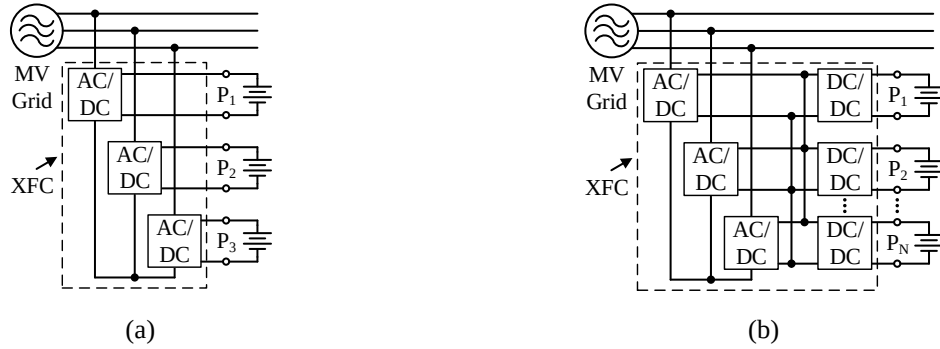


Figure 2.2 Example of XFC unit using conventional CPC: (a) AC/DC in direct contact to CP, and balancing utility currents required (a), DC/DC in direct contact to CP and balancing utility current not required (b). Unit's number of port (N) is assumed to be three.

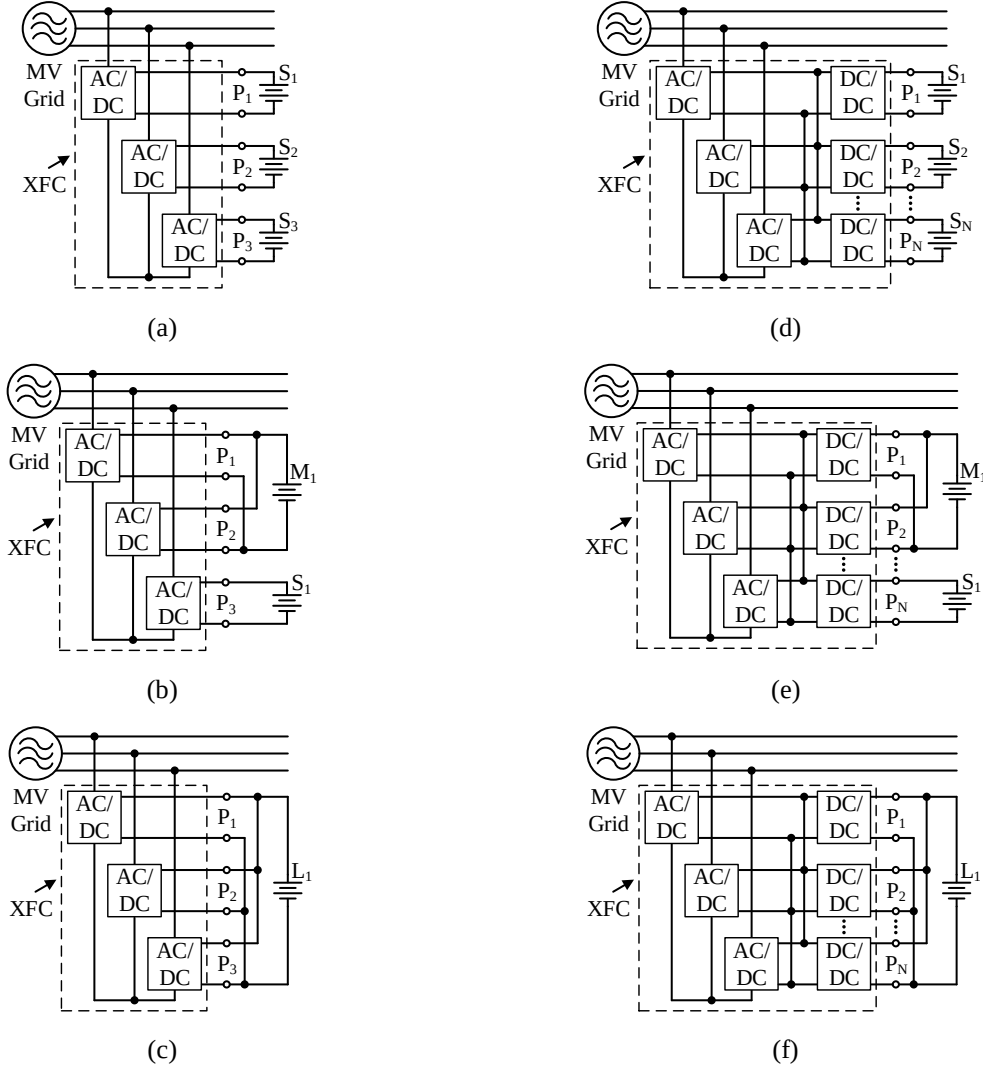


Figure 2.3 XFC unit using the proposed CPC. Requiring balancing utility currents and configured to charge up to: (a) three S_{EV} , (b) one S_{EV} and one M_{EV} , (c) a single L_{EV} . Providing inherent balance utility current and configured to charge up to: (d) three S_{EV} , (e) one S_{EV} and one M_{EV} , (f) a single L_{EV} . N is assumed to be three in this dissertation.

2.2.1 Power Rating

In order to show that the PECs in an XFC station—which can be composed of more than a charging unit—using the proposed active CPC achieve a lower size and cost than the PECs in a station using the fixed CPC, a theoretical comparison among them is provided in this section. The power rating is used as a figure of merit since it is directly related to PEC's size and cost [18]. The following assumptions are made to ensure a fair comparison:

- a) the same PECs are used in the XFC stations;

- b) the same number of ports (NoP) is available in the XFC stations, and all of them are being used simultaneously;
- c) the XFC station is ideal and capable of charging at least one L_{EV} demanding full-load per every three CPs;
- d) the XFC station using fixed CPC need to satisfy *at least* the same scenarios than one using the proposed CPC, which, as shown in Figure 2.3, these are to charge up to: 1) three S_{EV} simultaneously, 2) one S_{EV} and a M_{EV} simultaneously, 3) one L_{EV} , for a station that consists of a single XFC unit (or three CPs);
- e) EVs using the XFC station are drawing full-load power, expecting to be charged within ten minutes, and have the biggest battery capacity in their respective category (see Table 2.1). Therefore, a S_{EV} will draw 400kW, a M_{EV} will draw 800kW, and a L_{EV} will draw 1.2MW (assuming that it is desired to charge EVs with battery capacities up to 200kWh within ten minutes). EVs with battery capacities higher than 200kWh demanding full-load power can still be fully-charged but in more than ten minutes.

2.2.1.1 Conventional charging-port configuration

Without loss of generality, it is assumed for the rest of the dissertation that the NoP per XFC unit (“N” in Figs. 1 and 2) is equal to three. There are different ways an XFC station using the conventional CPC is able to satisfy the charging scenarios (CSs) “1-3” in assumption “d”. The following analysis focuses on the ones requiring absolute minimum and maximum power ratings (termed from now onwards as CPC_A , and CPC_B , respectively), and describes their respective tradeoffs.

Minimum XFC power rating to satisfy scenarios “1-3”

To satisfy the third CS, an XFC station with CPC_A has to have one of its port-connected PECs rated for 1.2MW (i.e., an AC/DC in Figure 2.2a, or a DC/DC in Figure 2.2b). The port connected to this PEC, namely port P_1 , can also be used to charge a S_{EV} or a M_{EV} (since their full-load power demand will be less than 1.2MW), consequently it can be used to satisfy the first or second CS as well. Since to satisfy at least all three CSs with CPC_A the PECs directly connected to the other two ports can be rated at 400kW, the total power rating of this XFC station is 2MW. Following this logic, a general expression for the XFC’s power rating using CPC_A with any NoP is obtained as:

$$P_{XFCA} = N_{LEV} \cdot P_{LEV} + (N_{MEV} - N_{LEV}) \cdot P_{MEV} + (N_{SEV} - N_{MEV})P_{SEV}, \quad (2.1)$$

where $N_{LEV} = \text{floor}(NoP/3)$, $N_{MEV} = \text{floor}(NoP/2)$, $N_{SEV} = NoP$ are the maximum number of L_{EV} , M_{EV} , and S_{EV} that can be individually charged in the XFC station, respectively, and P_{LEV} , P_{MEV} , P_{SEV} are the maximum power demand (P_{demand}) from a L_{EV} , M_{EV} , and S_{EV} , respectively.

An aspect to consider here is that the efficiency of the PEC rated for 1.2MW will be degraded when a S_{EV} or a M_{EV} charges through its port, because PECs usually have higher efficiencies at heavier loads [19]. Also, it is worth noting that in addition to the minimum CSs “1-3” in assumption “d”, a L_{EV} (or a M_{EV}) together with two S_{EV} can also be charged in this case. These additional CSs are tradeoffs to consider when deciding which CPC is best for a specific XFC station.

Maximum XFC power rating to satisfy scenarios “1-3”

Another way to satisfy all three CSs is by sizing each PEC (i.e., each AC/DC in Figure 2.2a, or each AC/DC and DC/DC in Figure 2.2b) for a L_{EV} (i.e., 1.2MW), increasing the station’s power rating to 3.6MW. This will rise the cost and size of the PECs with respect to the one using CPC_A ,

but it also increases the CSs the station can handle; for instance, three L_{EV} or M_{EV} can be charged simultaneously when using CPC_B . However, the station's overall efficiency is expected to be lower most of the time compared to CPC_A , since S_{EV} and M_{EV} will represent light- to mid-load conditions for the PECs. The power rating of an XFC station using CPC_B with any NoP is given as:

$$P_{XFCB} = NoP \cdot P_{LEV}. \quad (2.2)$$

2.2.1.2 Proposed charging-port configuration

To satisfy the third CS, the proposed CPC (termed as CPC_P for the rest of this dissertation) parallels three ports, where each supply equal power, 400kW. To charge a M_{EV} it parallels two ports, each supplying 400kW, the remaining port also supplies 400kW to charge a S_{EV} and satisfy the second CS. Finally, to satisfy the first CS all CPs need to supply 400kW. The aforementioned features mean that all PECs in the XFC station (i.e., all AC/DCs in Figure 2.3(a-c), or all AC/DCs and DC/DCs in Figure 2.3(d-f)) need each to be rated to 400kW. Thus, to satisfy all CSs, a station using CPC_P can be rated for just 1.2MW. Also, as opposed to CPC_A or CPC_B , CPC_P makes better utilization of the PECs, meaning that they will be operating at full-load condition independently of the EV connected to it, and thus, higher efficiency is expected. In general, the power rating of an XFC station using CPC_P with any NoP is given as:

$$P_{XFCP} = NoP \cdot P_{SEV}. \quad (2.3)$$

Based on the above analysis, to satisfy the same minimum CSs, the PECs in a station using CPC_P need less power rating, and therefore, are cheaper and smaller in comparison to the PECs in a station using CPC_A or CPC_B . They are also expected to be more efficient due to better utilization. However, the conventional CPC handle more CSs compared to CPC_P , where CPC_B will handle the most. The aforementioned observations are based on a station that consists of a single charging unit, in order to see if the same conclusions remain in a general fashion, it is necessary to do the analysis with higher NoPs (e.g., when the station is composed of multiple units in parallel).

Figure 2.4 shows the power rating and the power rating ratio (conventional against proposed) for a station consisting of three to eighteen CPs, or in other words, one to six units in parallel. The figure is based on (2.1) – (2.3) and shows that for the same NoP, a station (or the port-connected PECs) using CPC_A or CPC_B needs to have a power rating 1.67 to 3 times higher compared to one using CPC_P . It can also be seen that CPC_P has better advantage compared to CPC_A when it is used with an even NoP, although the advantage becomes similar as the NoP increases. However, as it was mentioned before, using CPC_P sacrifices in the CSs the station can handle. This tradeoff is analyzed in the next subsection.

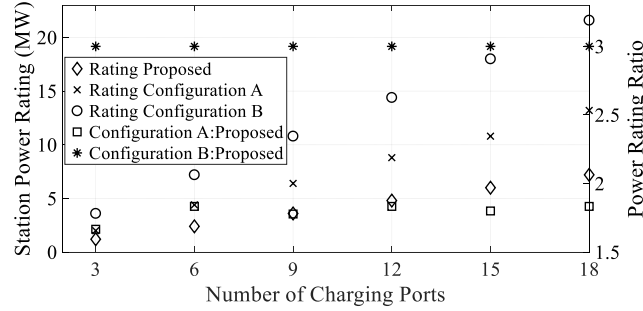


Figure 2.4 Power-rating comparison of an XFC station using the proposed active-port configuration (Figure 2.3) versus using the conventional one (Figure 2.2) for different number of charging ports.

2.2.2 Charging Scenarios

Table 2.2 is used to compare the conventional and proposed CPCs in terms of the CSs they can handle. It provides the number of the specific EV type (S_{EV} , M_{EV} , L_{EV}) in each CS, charging-port configuration (CPC_A , CPC_B , CPC_P) and chosen NoP = {3, 6, 9, 18}, as well as includes the equations used to obtain the entries within the aforementioned NoP. It is worth mentioning that there are many ways this table could have been filled; in this dissertation worst-case condition has been considered by making each entry represent the number of EVs that makes the station supply maximum power within each CS. The first three CSs are the maximum number of S_{EV} , M_{EV} , or L_{EV} that can be charged simultaneously considering that only one of those types is available in the

station, while the rest consider that there may be different EV types in it. In particular, the last row of the table considers when at least a L_{EV} , a M_{EV} , and a S_{EV} are to be charged simultaneously. Just for clarification purposes, a zero in the table means that the station cannot charge the EVs in the specific CS within ten minutes; not that the EVs cannot be connected to the station.

Table 2.2 Charging scenarios and their respective maximum number of EVs demanding full-load power

# of Ports	NoP			3			6			9			...	18		
Configuration	A	B	P	A	B	P	A	B	P	A	B	P	...	A	B	P
S_{EV}	N_{SEV}	NoP	N_{SEV}	3	3	3	6	6	6	9	9	9	...	18	18	18
M_{EV}	N_{MEV}	NoP	N_{MEV}	1	3	1	3	6	3	4	9	4	...	9	18	9
L_{EV}	N_{LEV}	NoP	N_{LEV}	1	3	1	2	6	2	3	9	3	...	6	18	6
$L_{EV},$ M_{EV}	$N_{LEV},$ $N_{MEV} - N_{LEV}$	NoP - 1, 1	$\text{floor}(\text{NoP}/3 - 2/3),$ $\text{floor}(\text{NoP}/2 - 3/2 \cdot L_{EV})$	0	2,	0	2,	5,	1,	3,	8,	2,	...	6,	17,	5,
$L_{EV},$ S_{EV}	$N_{LEV},$ $\text{NoP} - N_{LEV}$	NoP - 1, 1	$\text{floor}(\text{NoP}/3 - 1/3),$ $\text{NoP} - 3 \cdot L_{EV}$	1,	2,	0	2,	5,	1,	3,	8,	2,	...	6,	17,	5,
$M_{EV},$ S_{EV}	$N_{MEV},$ $\text{NoP} - N_{MEV}$	NoP - 1, 1	$\text{floor}(\text{NoP}/2 - 1/2),$ $\text{NoP} - 2 \cdot M_{EV}$	1,	2,	1,	3,	5,	2,	4,	8,	4,	...	9,	17,	8,
$L_{EV},$ $M_{EV},$ S_{EV}	$N_{LEV},$ $N_{MEV} - N_{LEV},$ $\text{NoP} - N_{MEV}$	NoP - 2, 1, 1	$\text{floor}(\text{NoP}/3 - 1),$ $\text{floor}(\text{NoP}/2 - 3/2 \cdot L_{EV} - 1/2),$ $\text{NoP} - 3 \cdot L_{EV} - 2 \cdot M_{EV}$	0	1,	0	2,	4,	1,	3,	7,	2,	...	6,	16,	5,
					1,		1,	1,	1,	1,	1,	1,	...	3,	1,	1,
					1		3	1	1	5	1	1		9	1	1

2.2.2.1 Proposed versus CPC_A

It can be seen from Table 2.2 that when compared under the same NoP, an XFC station with CPC_A is capable of supporting more CSs compared to one with CPC_P . For example: CPC_A can handle up to six L_{EV} and up to twelve S_{EV} simultaneously, while CPC_P can handle up to five L_{EV} and up to three S_{EV} simultaneously when $\text{NoP} = 18$ and the CS is L_{EV}, S_{EV} . If the comparison is made under different NoP, CPC_P can achieve similar or more CSs while require less or similar power rating compared to CPC_A when it uses higher NoP. For instance, when comparing $\text{NoP} = 18$ using CPC_P versus $\text{NoP} = 9$ using CPC_A , CPC_P will handle two more CSs but have 12.5% more power rating compared to CPC_A . On the other hand, when comparing $\text{NoP} = 9$ using CPC_P versus $\text{NoP} = 6$ using CPC_A , CPC_P will handle six less CSs but have 18% less power rating than CPC_A . In both cases CPC_P handles more CSs when the same EV type is connected to the station, but may handle less when different.

2.2.2.2 Proposed versus CPC_B

As shown on Table 2.2, for the same NoP, CPC_B supports more CSs compared to CPC_P while it has three times the power rating (see Figure 2.4). When the comparison is made under different NoP, say under the assumption that both configurations need to charge the same amount of L_{EV} (e.g., using NoP = 3 or 6 with CPC_B, versus using NoP = 9 or 18, respectively, with CPC_P), both stations need to be rated equally while the one using CPC_P can support more CSs. Therefore, if the XFC power rating is a fixed design parameter, CPC_P is the best choice, while if the NoP is fixed then there is a tradeoff between having a cheaper and smaller PECs or more CSs.

The analysis in this section showed the benefits of the proposed CPC on the XFC's PECs size and cost, which is the reason why is adopted in the proposed station. The next section provides the details of the control strategy implemented so as to achieve balanced utility currents and unity power factor while charging multiple types of EVs simultaneously.

2.3 Theoretical Analysis about the Control Strategy in the Proposed XFC Station

The proposed XFC station will naturally cause unbalanced utility currents due to the different power requirement that the station will see in each of its ports—since it was decided not to connect all CMIs through a common dc-link in order to avoid adding size and cost due to the need for redundant DC/DCs. Also, due to its interface impedance, the grid power factor will be degraded. Therefore, a strategy to charge multiple types of EVs while achieving balanced three-phase utility current with unity power factor is needed. The following analysis is mostly based on [20], assumes that the grid is supplying balanced positive-sequence voltage, and neglect losses and the line impedance. For unity power factor, the imaginary part of the grid's positive sequence current (I_1) should be zero, that is,

$$\text{Im}\{\mathbf{I}_1\} = \text{Im}\left\{\frac{1}{\sqrt{3}}(\mathbf{I}_a + \mathbf{h}\mathbf{I}_b + \mathbf{h}^2\mathbf{I}_c)\right\} = \text{Im}\{\sqrt{3}V_{LN}(\mathbf{Y}_{ab} + \mathbf{Y}_{bc} + \mathbf{Y}_{ca})\} = 0 \quad (2.4)$$

where $\mathbf{I}_{a,b,c}$ is the corresponding phasor of the grid currents $i_{a,b,c}$, $\mathbf{h} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$, V_{LN} is the line to neutral RMS value of the grid voltage, $\mathbf{Y}_{ab,bc,ca}$ is the line to line admittance in each phase of the delta, and the “bolded” variables are complex quantities. For balanced three-phase utility current, the grid’s negative sequence current ($\mathbf{I}_2$) should also be zero, that is,

$$\mathbf{I}_2 = \frac{1}{\sqrt{3}}(\mathbf{I}_a + \mathbf{h}^2\mathbf{I}_b + \mathbf{h}\mathbf{I}_c) = -\sqrt{3}V_{LN}(\mathbf{h}^2\mathbf{Y}_{ab} + \mathbf{Y}_{bc} + \mathbf{h}\mathbf{Y}_{ca}) = 0, \quad (2.5)$$

Note that two equations can be obtained from (2.5), $\text{Re}\{\mathbf{I}_2\} = 0$ and $\text{Im}\{\mathbf{I}_2\} = 0$, thus a system of three equations (including (2.4)) and three unknowns ($\mathbf{Y}_{ab,bc,ca}$) can be formed. The reason $\mathbf{Y}_{ab,bc,ca}$ is unknown is due to not knowing its imaginary part, namely, $B_{ab,bc,ca}$; its real part ($G_{ab,bc,ca}$) is known since it depends on the EV power demand and the line to line voltage across the delta. The imaginary part is what the controller needs to identify in order to make the CMI of each phase supply or absorb a specific reactive power so as to make the utility have balanced three phase currents and unity power factor. This system of equation provides the basis of the control strategy implemented in the proposed charging station.

Table 2.3 contains the exact expression of $\mathbf{Y}_{ab,bc,ca}$, obtained after solving the system of equation. The expressions here are general, meaning that the line to line admittances shown in the first scenario are valid for one, two, or three S_{EV} connected to the station; the ones for the second scenario are valid for either a S_{EV} by itself, a M_{EV} by itself, or an S_{EV} and a M_{EV} simultaneously; and the ones included for the third scenario are valid for one L_{EV} occupying the whole charging station (the three ports). Without loss of generality, this table is filled assuming that the EVs are connected to the specific ports identified in the table itself. Also, for the scenarios where some ports are connected in parallel, namely, scenarios “2” and “3”, the conductance G_p equals the

conductance of the phases connected in parallel. For example, in scenario “2”, the ports $DC_{ab1,2}$ and $DC_{bc1,2}$ are connected in parallel for a M_{EV} , therefore, $G_p = G_{ab} = G_{bc}$ since these two phases share the power equally.

It is worth noting that the admittances in each phase are different, meaning that the XFC station will have unbalance currents flowing inside the delta. Furthermore, it can be seen that scenario “3” is inherently balanced in theory since the power is equally shared among the three phases. The actual control implementation of the proposed XFC station is described in the next section.

Table 2.3 Line to line admittance for each possible charging scenario in an XFC station with three ports

#	Scenario	Y_{ab}	Y_{bc}	Y_{ca}
1	Up to three Small-Sized EVs (one per port)	$G_{ab} + j \frac{G_{ca} - G_{bc}}{\sqrt{3}}$	$G_{bc} + j \frac{G_{ab} - G_{ca}}{\sqrt{3}}$	$G_{ca} + j \frac{G_{bc} - G_{ab}}{\sqrt{3}}$
2	Up to one Medium-Sized EV (connected to ports $DC_{ab1,2}$ and $DC_{bc1,2}$) and a Small-Sized EV (connected to $DC_{ca1,2}$)	$G_p + j \frac{G_{ca} - G_p}{\sqrt{3}}$	$G_p + j \frac{G_p - G_{ca}}{\sqrt{3}}$	G_{ca}
3	One Large-Sized EV (connected to ports $DC_{ab1,2}$, $DC_{bc1,2}$, and $DC_{ca1,2}$)	G_p	G_p	G_p

2.4 Control Implementation of the Proposed XFC Station

This section provides the details of the control implementation for the proposed XFC station. This includes the closed-loop system to achieve three-phase balanced utility currents with unity power factor, and how the proposed charging-port reconfiguration is achieved.

2.4.1 Balanced Utility Currents and Unity Power Factor

The control block diagram that provides an overview of how the XFC station charges multiple EVs while achieving balanced three-phase utility currents with unity power factor is shown in Figure 2.5. This is accomplished by injecting a current through each phase of the delta that is generated by the voltage difference between the line to line and CMI voltages, or in other words, the voltage drop in the interface impedance. The CMI voltage that needs to be applied

depends on the charging scenario (“1” – “3” in Table 2.3), and its reference ($v_{CMIab,bc,ca}^*$) is calculated by a PR regulator which is able to track sinusoidal reference signals with zero steady-state errors [21]. The reference signal the regulator is tracking is the phase current ($i_{ab,bc,ca}^*$) which is calculated as follows:

- 1) calculate the line to line conductance: $G_x = \frac{P_{EVx}}{V_{LLx}^2}$, where $x = ab, bc, ca$, P_{EVx} is the EV power demand in the respective phase, which is given by the battery management system, and V_{LLx} is the RMS value of the line to line voltage across the delta (13.8kV in the proposed system);
- 2) calculate Y_x based on the charging scenario (Table 2.3);
- 3) calculate the phase current reference: $I_x^* = Y_x V_x$, where V_{LLx} is the line to line voltage across the delta which needs its phase angle (θ_g) and frequency (ω_g) to be obtained from a phase lock loop (PLL).

The switching functions for the grid-side H-bridges in each cell are generated based on the equal area criteria [22], which will produce a stair-case voltage waveform such as that in Figure 2.6, where V_{dc} is the DAB dc-link voltage, k is the number of levels of the CMI, and the delay angles are given as:

$$\alpha_x = \sin^{-1} \left(\frac{V_{dc}(k-1/2)}{\sqrt{2}V_{CMIx}} \right), \quad (2.6)$$

where V_{CMIx} is the CMI’s voltage RMS value. This modulation strategy achieves low switching losses since it operates the switches at the grid frequency, and due to the high number of levels required for MV grid connection the CMI voltage waveform is close to sinusoidal, thus harmonic elimination [22] is not necessary.

Although not the scope of this dissertation, the voltage balancing in each cell can be accomplished by the switching pattern-swapping technique [23], and the power flow through the

DAB can be controlled by any of the DAB popular control methods: single phase-shift, dual phase-shift, triple phase-shift [24]–[26]. In particular, single phase shift can be used for loads close to full-load, and triple phase shift can be used in light load conditions.

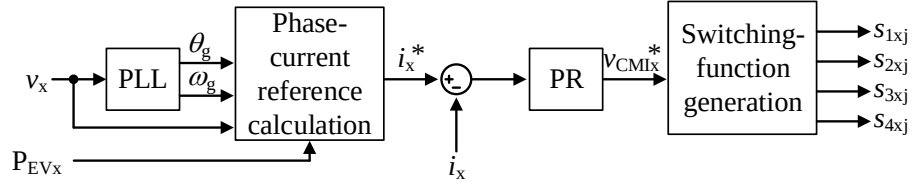


Figure 2.5 Single-phase control block diagram for the grid-side H-bridge of the proposed XFC station, where $j = 1, 2, \dots, k$, k is the CMI's total number of cells, and $x = ab, bc, ca$.

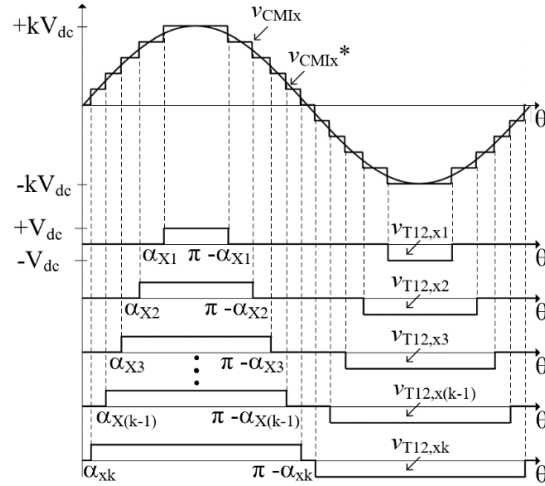


Figure 2.6 CMI actual (v_{CMIx}) and reference (v_{CMIx}^*) voltage waveform, as well as individual cell voltages ($v_{T12,xk}$), where k is the CMIs' total number of cells, V_{dc} is the dc-link voltage in a cell, and $x = ab, bc, ca$.

2.4.2 Charging-Port Reconfiguration

The actual reconfiguration of the charging-ports is achieved with six single-pole-triple-throw (SPTT) switches for an XFC unit with three CPs. This is shown in Figure 2.7, where the exact pole-throw connection is provided in Table 2.4. It can be seen that the main drawback of the proposed CPC is its actual implementation. Not only is more challenging to implement compared to the conventional counterpart (especially as the NoP increases), but it relies on adding extra semiconductor devices to achieve the reconfiguration (where more additional switches are needed if bidirectional power-flow capability is desired).

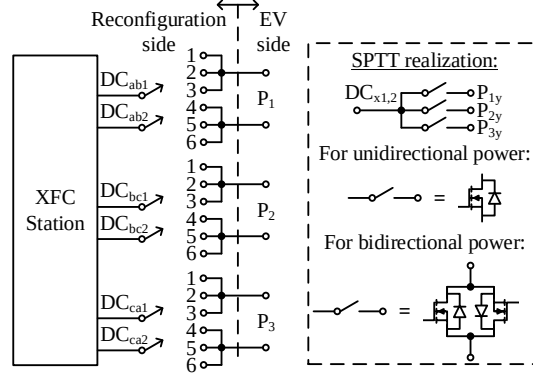


Figure 2.7 Proposed CPC re-configuration diagram for NoP = 3 with its single-pole triple-throw switch realization, where $y = \{1, 2, \dots, 6\}$.

Table 2.4 Single-pole triple-throw switch connection

Pole	Throw
DCab1	P11, P21, P31
DCab2	P14, P24, P34
DCbc1	P12, P22, P32
DCbc2	P15, P25, P35
DCca1	P13, P23, P33
DCca2	P16, P26, P36

The additional semiconductor devices add neglectable size, cost, and loss (less than $\sim 2\%$ expected) compared to the rest of the components in the system. Still, careful selection of these is most be done. Specifically, since conduction loss is the degrading efficiency factor, switches with low parasitic drain-to-source resistance (in the case of MOSFET), or with low collector-to-emitter voltage (in the case of IGBT) are recommended. To help reduce this loss even further, paralleling the switches is suggested, given the high currents (e.g., $>1\text{kA}$ for an EV battery using current industry standard of 400V [1] demanding full-load power) that will be flowing through the SPTT switch. At the moment, the following switches could be some choices so as to keep low cost and conduction loss: AU1RF8739L2TR, IRL40SC228, FDMT80040DC. It is worth mentioning that conduction loss is expected to be lower as semiconductor technology advances, as well as when higher battery voltages (i.e., 800V) are used in EVs [1]. Therefore, the weight in conduction loss

and the extra size and cost incurred in SPTT realization is expected to be even lower as technology evolves compared to at the time of writing.

2.5 Simulation Results

Simulation results are shown in this section in order to validate the XFC station operation. These were carried in MATLAB Simulink using the closed-loop system in Figure 2.5, where the P_{EVx} is given as input while using the proposed CPC, meaning that, for example, if an M_{EV} is connected and demanding say 800kW, its power demand will be split in half, making the reference for the two ports connected in parallel to it be 400kW each. In addition, ideal switches are used to speed-up the simulation time, the line impedance is neglected, and the dc-link capacitor (which, as a reference, can be designed according to [16]) voltages were assumed to be balanced.

The CMI interface inductance is chosen according to [16], where at least 3% was enough for keeping sinusoidal phase currents in a delta-connected CMI; which is what is selected for the proposed XFC. For the CMI cell parameters, the DAB transformer turns ratio was chosen to be equal to unity. Since the current standard for EV batteries is 400V [1], and because it has been found that $V_{dc} = NV_{EV}$ is beneficial for reducing switching, conduction and winding loss in the DAB [27] it was decided to use a 400V dc-link. This in turn means that the number of cells (NoC) should be $NoC \geq \text{ceil}\left(\frac{V_{LL}\sqrt{2}}{V_{dc}}\right) \geq 49$. Choosing 49 is the best alternative for minimum size, cost and loss, but with not much sacrifice in these, 50 will provide a better current total harmonic distortion (THD) for XFC's light load conditions (e.g., charging a single S_{EV}), which is why it is selected. Table 2.5 provides with a summary of the XFC station specifications for the simulations.

Six scenarios were simulated and these are summarized in Table 2.6. The results are shown in Figure 2.8, where in each sub-figure ("a" - "f") the top waveforms are the line voltages and currents, and the bottom ones are the CMI voltages and currents.

Table 2.5 Key specifications of the proposed XFC station

Parameter	Value
Grid voltage (V_{LL})	13.8kV
Grid frequency (f_g)	60Hz
CMIx power rating	400kW
XFC station power rating	1.2MW
CMIx number of cells (k)	50
Interface impedance (L_{int}) and its ESR	37.9mH, 14.3 Ω (3%)
DC-link voltage per cell (V_{dc})	400V
PR constants: k_p , k_r	20, 8

Table 2.6 Simulated scenarios

Scenario	EV type	Power demand
a	One small-sized EV (65kWh)	400kW
b	Two small-sized EVs (65kWh each)	400kW, 200kW
c	Three small-sized EVs (65kWh each)	400kW, 200kW, 200kW
d	One medium-sized EV (130kWh)	800kW
e	One medium-sized EV (130kWh), and a small-sized EV (65kWh)	800kW, 200kW
f	One large-sized EV (200kWh)	1.20MW

Note that for each case the line currents are sinusoidal and in phase with their corresponding voltage, which means that the grid power factor is unity, and have the same amplitude while being 120° apart from each other, meaning they are balanced. The currents within the delta are unbalanced as it is to be expected from the analysis made in section 2.3. These results validate the operation claimed for the proposed XFC station.

Although no actual implementation of the proposed XFC system was made, rough calculations based on charging a L_{EV} indicate that the proposed XFC system can be capable of achieving ~96.1% efficiency at full-load and ~94.5% at half load. These numbers were obtained by assuming that the DABs can be designed to reach an efficiency of 97% at full load and 95% at half load in the power levels of interest [17], resulting in a loss per phase of 12kW, and 10kW, respectively. This is a conservative estimate given that the cited experiments were made in 2005 and were based on Si IGBTs. For the grid-side H-bridge, the switching loss is neglected since it is driven at 60Hz (compared to tens of kHz on the DAB), and operation at 100% duty cycle (i.e., no zero states inserted) is assumed, resulting in a loss per phase of 3.4kW and 0.84kW, respectively,

when using the SiC MOSFET SCT3040KLHR. Finally, the loss per phase due to the SPTT was estimated to be 0.350kW at full load and 0.0875kW at half load (considering two AUIRF8739L2TR switches in parallel), which results the most efficient stage of the system re-confirming that the loss due to the added SPTT can be neglectable.

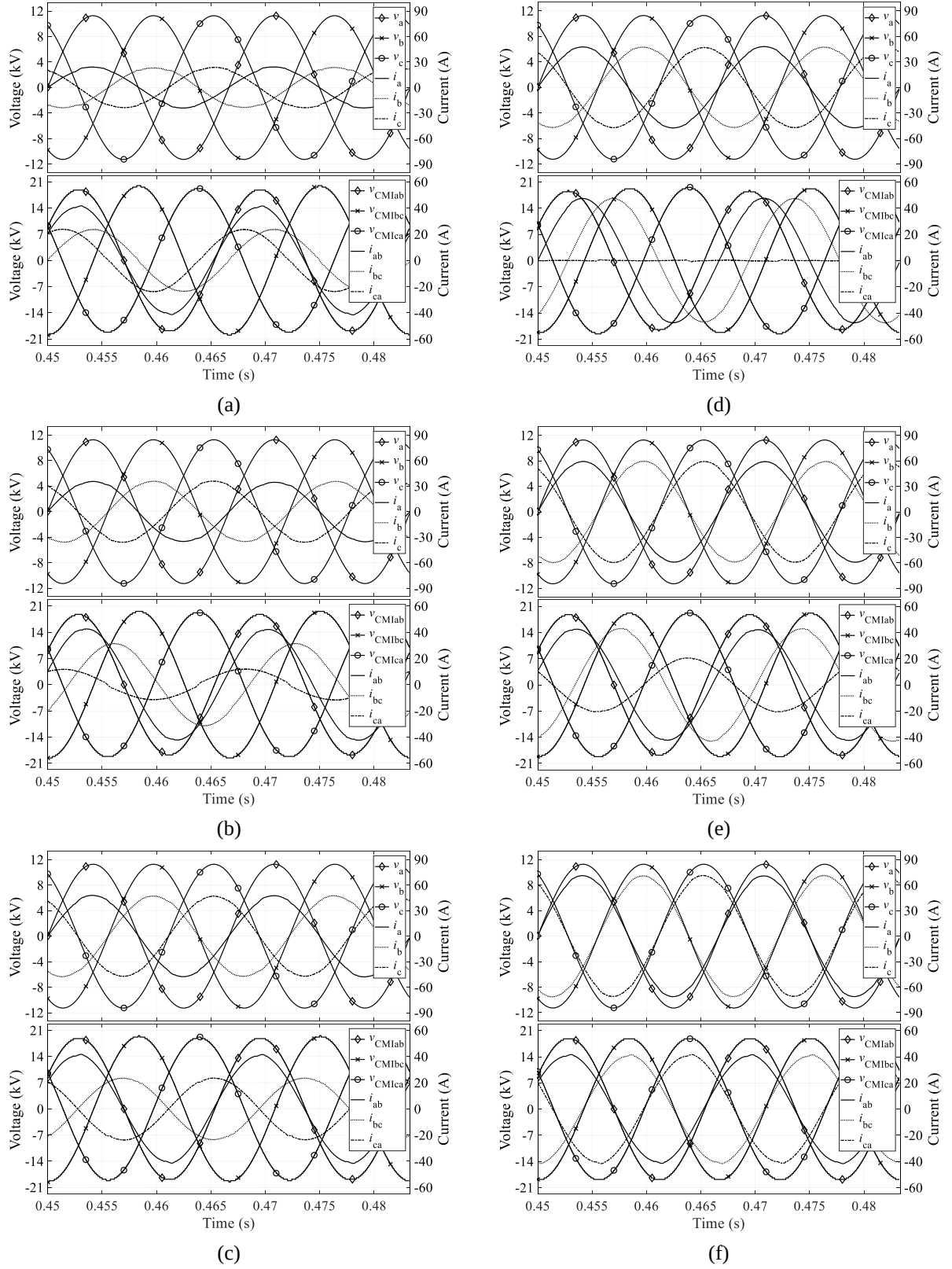


Figure 2.8 Simulated line voltage and current (top), and CMI voltage and current (bottom) for scenarios "a" through "f" on Table 2.6.

2.6 Summary

Extreme fast-charging stations must efficiently process high power ($>1\text{MW}$) to simultaneously charge multiple types of EVs (small, medium, large) within ten minutes. Many chargers have been proposed to accomplish this goal, but they either do not account for the unbalance utility currents, nor the grid power factor, and/or their power converters are larger and more expensive than likely necessary. In this dissertation, a 1.2MW , 13.8kV extreme XFC based on a delta-connected CMI and an active CPC is proposed. The station is able to achieve balanced utility currents and unity power factor while charging multiple types of EVs simultaneously. The control strategy to achieve this was described and validated through simulations. The proposed CPC adapts in response to the types of EVs connected to the charger. Specifically, it allows the XFC to simultaneously charge up to three small-sized EVs, or up to a small- and medium-sized EV, or a large-sized EV, while the CMIs in each phase are rated for just a small-sized EV. As it was theoretically demonstrated, this results in an XFC unit that have 40% - 66.7% less power rating compared to one using the conventional fixed CPC and the same number of charging-ports; thus, reducing the size and cost of the power converters in the system. Tradeoffs of implementing such kind of CPC were also addressed in this chapter.

Chapter 3 Control Strategy for Core-Loss Reduction in High-Frequency Transformer for Plug-in Chargers with Galvanic Isolation

3.1 Background

As it was shown in the previous chapter, the proposed XFC station contains a DC/DC stage in each cell of the CMIs, which consist of a DAB (Figure 3.1). This widely-used power converter utilizes a high-frequency transformer (HFTx) so as to provide isolation between the grid and the EV, while being able to step up/down the voltage in the charger. Since it is typically one of the most inefficient, bulky and heavy components in a PE system [28]–[30], much research has been done in HFTx size and loss optimization. Core loss reduction, which is the focus in this dissertation, traditionally has been done with offline-based methods such as designing different transformer structures or using different core materials, and are typically attached to complex optimization algorithms [30]–[36]. These approaches are effective but: 1) time consuming; 2) inconvenient to implement in a system that is already built; 3) require designers to limit themselves to just the current state of the art in transformer design, manufacturing and/or core materials.

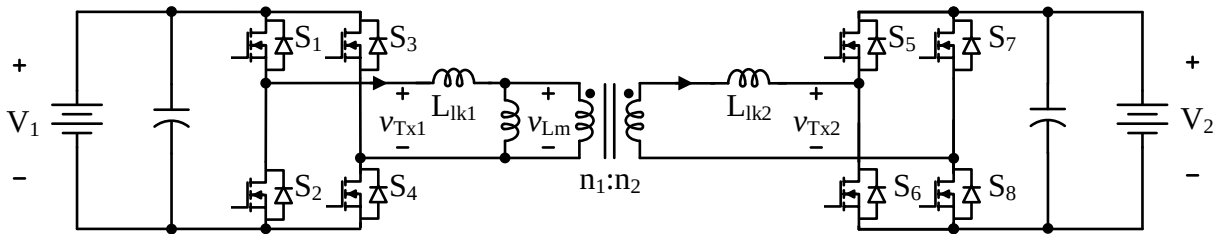


Figure 3.1 Dual active bridge, showing HFTx with its leakages and magnetizing inductances.

In this dissertation, an online-based approach to reduce the HFTx core loss is proposed. It relies on controlling the DAB so as to reduce and/or clamp the transformer's flux linkage while still supplying a desired power to the load. By doing this, the proposed method: 1) is less time consuming to implement; 2) can be easily applied to an existing system by modifying its control strategy; 3) is independent of the transformer design, manufacturing process and/or core material; 4) makes improvements that are additive to any improvement made in the offline-based approaches. This dissertation validates the theoretical analysis using simulation tools that are well-trusted so as to obtain results close to what it will be in an actual setup. Specifically, ANSYS Maxwell is used to simulate the transformer's core loss, and LTspice is used to obtain semiconductor (using its SPICE model provided by the manufacturer) and winding losses. The next section provides the conceptual explanation of the proposed control strategy.

3.2 Conceptual Explanation of the Proposed Control Strategy for Core-Loss Reduction

There are many ways the DAB can be controlled; single phase-shift, dual phase-shift, triple phase-shift are the most popular [24]–[26]. As it will be clear through the discussion, the proposed control strategy to reduce core loss can be applied when using any of them, but to just focus on the concept, only single phase-shift will be discussed in depth. Also, without loss of generality, it is assumed that the power is being transferred from the primary to the secondary side of the DAB (from the source to the EV battery bank), and that the primary side dc voltage, V_1 , is higher than the secondary side dc voltage, V_2 . With the aforementioned assumptions, the voltage across the transformer's primary and secondary terminals, v_{Tx1} and v_{Tx2} , respectively, take the form of that in Figure 3.2a, where θ_{12} is the phase-shift between them. This in turn makes the voltage across

the magnetizing inductance (v_{Lm}) to be a quasi-square wave such as that in Figure 3.2b, which instantaneous value is given as:

$$v_{Lm} = \frac{v_{Tx1} + v_{Tx2}/N}{2}, \quad (3.1)$$

where $N = \frac{n_2}{n_1}$ is the transformer's turns ratio. The instantaneous flux density produced by this voltage is shown in the same figure and can be obtained with:

$$B = \frac{\lambda}{n_1 A_c} = \frac{\int v_{Lm}(t) dt}{n_1 A_c}, \quad (3.2)$$

where A_c is the transformer's core cross-sectional area, and λ is the flux linkage, or volts-seconds, produced by v_{Lm} . The flux density is one of the HFTx's quantities that affect the core loss (P_{core}) as it can be seen from the modified Steinmetz equation (which was proposed to calculate P_{core} from non-sinusoidal excitations) [37]:

$$P_{core} = V_c K f \hat{B}^\beta \left(\frac{1}{2\pi^2 \hat{B}^2} \int \left(\frac{dB}{dt} \right)^2 dt \right)^{\alpha-1}, \quad (3.3)$$

where K , α , and β are the Steinmetz coefficients which depend on the core material and can be extracted from the manufacturer's datasheet by curve fitting, f is the magnetization frequency (equal to the H-bridges switching frequency, f_{sw} , in this case), V_c is the core volume (or mass if this is what the core manufacturer provided in the loss density curves), and $\hat{B}$ is the peak AC flux density.

Notice from (3.3) that for a fixed transformer, it is possible to control the core loss by varying f and/or $\hat{B}$, which can be achieved online by changing the shape of v_{Lm} , as implied in (3.2). Equations (3.2) and (3.3) also show that in order to specifically reduce this loss, the control needs to: 1) reduce the volts-second product so as to reduce $\hat{B}$, and/or 2) “clamp” the flux linkage so $\frac{dB}{dt}$ as well as the instantaneous core loss are zero. The volts-second product can be reduced by decreasing the voltage amplitude across the magnetizing inductance and/or the time intervals with

non-zero voltage, and “clamping” the flux linkage (or density) can be done by inserting “zero states” in v_{Lm} . It can be seen from Figure 3.2a-b and from (3.1) that to insert zero states, a phase shift between v_{Tx1} and v_{Tx2} is needed as well as the following relationship should hold:

$$v_{Tx1} = v_{Tx2}/N , \quad (3.4)$$

meaning that the voltages V_1 and/or V_2 should be controlled (or fixed at the design stage) such that

$$V_1 = V_2/N. \quad (3.5)$$

Figure 3.2c shows the voltage across the magnetizing inductance as well as the flux density when the proposed control strategy is implemented. It can be seen that the greater the θ_{12} the more zero states will be inserted, and thus, the less core loss is to be expected. Some independent observations to be made regarding the above discussion are described below.

- 1) The equation (3.5) has also been found to be beneficial in DABs controlled under single phase-shift, but for reducing switching, conduction, and winding loss [38]–[40]. Also, the equation can be confirmed by equaling the flux density at point “a”, B_a , and the flux density at point “b”, B_b , in Figure 3.2, since these two values will be the same when the flux density is clamped. The analytical expressions for these two points are:

$$B_a = \frac{1}{2\omega_{sw}n_1A_c} \left[\frac{\pi}{2} \left(V_1 + \frac{V_2}{N} \right) - \theta_{12} \frac{V_2}{N} \right], \quad (3.6)$$

$$B_b = \frac{1}{2\omega_{sw}n_1A_c} \left[\frac{\pi}{2} \left(V_1 + \frac{V_2}{N} \right) - \theta_{12} V_1 \right], \quad (3.7)$$

where $\omega_{sw} = 2\pi f_{sw}$ is the angular switching frequency.

- 2) Notice from Figure 3.2c that for a fixed transformer and voltages V_1 and V_2 , the flux linkage (and consequently, $\hat{B} = B_a$) is also be reduced by clamping the flux density (the longer the better as mentioned before and confirmed by the negative in front the “ $\theta_{12} \frac{V_2}{N}$ ” term in (3.6)) since there will be less time for non-zero voltages within a magnetizing period. Increasing

the magnetizing frequency also help (as confirmed by (3.6)), nevertheless, not only there is a tradeoff with increased switching losses in the H-bridges, but the Steinmetz coefficients change and may end up outweighing the reduction in core loss due to lower flux linkage.

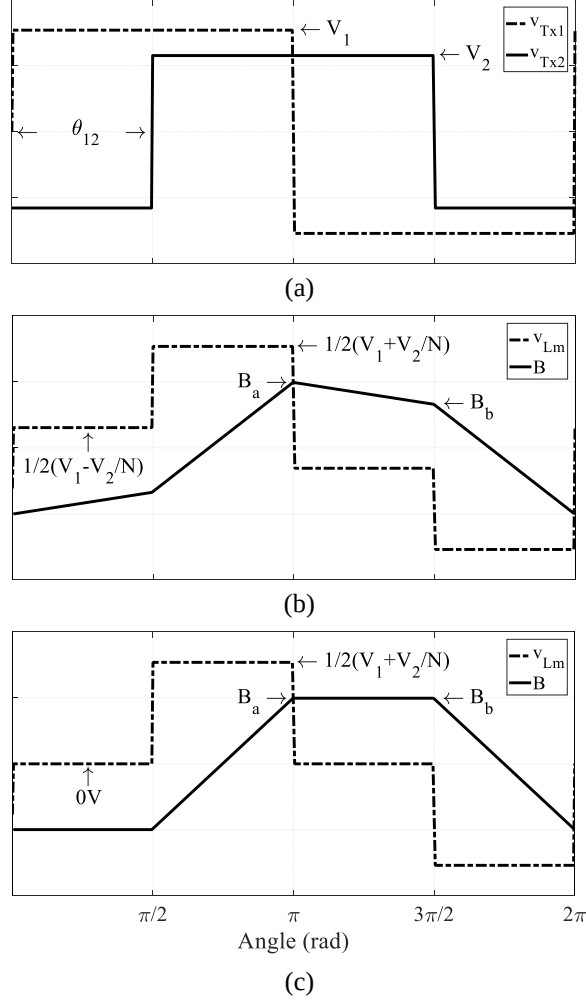


Figure 3.2 DAB key waveforms to implement proposed control strategy for $V_1 > V_2$: a) HFTx primary and secondary voltages, b) Magnetizing inductance voltage and flux density for $V_1 \neq \frac{V_2}{N}$, c) Magnetizing inductance voltage and flux density for $V_1 = \frac{V_2}{N}$. The flux density at point “a”, $B_a = \frac{1}{4\pi f_{sw} n_1 A_c} \left[\frac{\pi}{2} \left(V_1 + \frac{V_2}{N} \right) - \theta_{12} \frac{V_2}{N} \right]$, and at point “b”, $B_b = \frac{1}{4\pi f_{sw} n_1 A_c} \left[\frac{\pi}{2} \left(V_1 + \frac{V_2}{N} \right) - \theta_{12} V_1 \right]$.

3.3 Theoretical Validation of the Proposed Control Strategy for Core-Loss Reduction

The theoretical validation of the proposed control strategy is performed with a case study that compares how much core loss can be reduced when implementing the proposed control strategy versus not doing so (termed as the “nominal” case henceforth). A DAB rated for 8kW (considering that the proposed XFC station in Chapter 2 uses 50 cells per 400kW CMI) with a fixed transformer (designed in accordance to [41]) and V_2 are used for both cases. The DAB parameters are summarized in Table 3.1, and the transformer parameters are summarized in Table 3.2. V_1 is the parameter used to differentiate the proposed from the nominal case, which is chosen to be smaller in the proposed case so as to achieve a lower flux linkage. Since the power flow through the HFTx (P_{Tx}) is given as [42]:

$$P_{Tx} = \frac{V_1 V_2 \theta_{12} (\pi - |\theta_{12}|)}{2\pi^2 f_{sw} N L}, \quad (3.8)$$

θ_{12} will vary accordingly so as to transfer the same power in both cases. In this equation $L = L_1 + \frac{L_2}{N^2}$, where L_1 and L_2 are the primary and secondary side inductances, respectively, which are composed of the HFTx’s leakage inductances (L_{lk1}, L_{lk2}) and any external inductances placed in series to the transformer so as to achieve a desired power transfer. In the given HFTx there is no external inductances and therefore, $L_1 = L_{lk1}, L_2 = L_{lk2}$.

Table 3.1 DAB Parameters/Components

Parameter/Component	Proposed	Nominal
Primary voltage (V_1)	400V	600V
Phase shift (θ_{12})	Variable	Variable
Power rating	8kW	
Secondary voltage (V_2)	300V	
Switching frequency (f_{sw})	100kHz	
SiC MOSFET	SCT3040KL	

Table 3.2 HFTx Parameters

Parameter	Proposed	Nominal
Turns ratio (N)	0.75	
Primary number of turns (n_1)	14	
Secondary number of turns (n_2)	10.5	
Primary leakage inductance (L_{lk1})	12.501 μ H	
Secondary leakage inductance (L_{lk2})	7.0318 μ H	
Magnetizing inductance (L_m)	2.6536mH	
Primary winding resistance (R_{w1})	1.5m Ω	
Secondary winding resistance (R_{w2})	0.83m Ω	
Core material	Ferrite 3C95	
Core size	EE 100-60-28	
Core volume (V_c)	2.0139x10 ⁻⁴ m ³	
Core cross-sectional area (A_c)	0.738 x10 ⁻³ m ²	
Steinmetz coefficient (α)	1.759	
Steinmetz coefficient (β)	2.87	
Steinmetz coefficient (K)	0.0513	

Figure 3.3 shows graphically what results from (3.8) for the proposed and nominal case, where anything above 8kW is not feasible since is greater than the power rating of the DAB. Also, it has been found that operating the DAB for $\theta_{12} > \pi/2$ incurs in higher copper and conduction losses [42]. However, it is hypothesized that when using the proposed control strategy for light load conditions (were transformer currents are low), operating θ_{12} near π compared to near 0 rads could be better since the drastic reduction in core loss could outweigh the increase in copper and conduction loss. This not only follows the discussion in section 3.2, but can be better visualized from the more specific core loss equation (based on (3.3)) for the proposed case (P_{core_Prop}), which is given as follows:

$$P_{core_Prop} = V_c K f_{sw} \hat{B}^\beta \left[\frac{(\pi - \theta_{12})}{\omega_{sw} (2\pi \hat{B} n_1 A_c)^2} \left(V_1 + \frac{V_2}{N} \right)^2 \right]^{\alpha-1}. \quad (3.9)$$

Notice that as θ_{12} approach π , (3.9) approaches zero. For a fair comparison though, this dissertation will focus on $\theta_{12} \leq \pi/2$ for both cases.

The more specific core loss expression for the nominal case is given as:

$$P_{core_Nom} = V_c K f_{sw} \hat{B}^\beta \left\{ \frac{1}{\omega_{sw} (2\pi \hat{B} n_1 A_c)^2} \left[(\pi - \theta_{12}) \left(V_1 + \frac{V_2}{N} \right)^2 + \theta_{12} \left(V_1 - \frac{V_2}{N} \right)^2 \right] \right\}^{\alpha-1}. \quad (3.10)$$

Notice that the difference between (3.9) and (3.10) is that (3.10) has an additional $\theta_{12} \left(V_1 - \frac{V_2}{N} \right)^2$ term which consequently makes the nominal case have higher core loss compared to the proposed case. This equation provides yet another confirmation of (3.5), since choosing $V_1 = \frac{V_2}{N}$ eliminates that additional term, thus reducing the core loss.

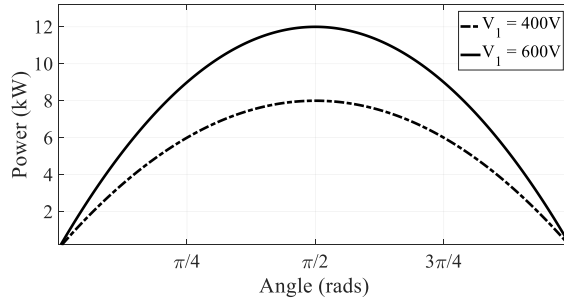


Figure 3.3 Power flow through the HFTx vs phase shift between the HFTx primary and secondary side voltages, θ_{12} , for the proposed ($V_1 = 400V$) and nominal case ($V_1 = 600V$).

To demonstrate the benefit of the proposed control strategy, the ratio between (3.10) and (3.9) is taken for the whole load range using the parameters in Table 3.1 and Table 3.2, and is illustrated in Figure 3.4. This figure also shows the phase shift that was needed to transfer the same amount of power in both, the nominal and proposed cases. Notice that for the specific transformer and DAB design, the nominal case incurs in about five times more core loss at full load condition compared to the proposed case while about two times more at light load. Also, the core loss ratio is higher at heavier loads, which is to be expected mainly because the zero state intervals are longer (i.e. θ_{12} is higher) at heavier loads compared to at lighter loads, where the zero state intervals are reduced significantly.

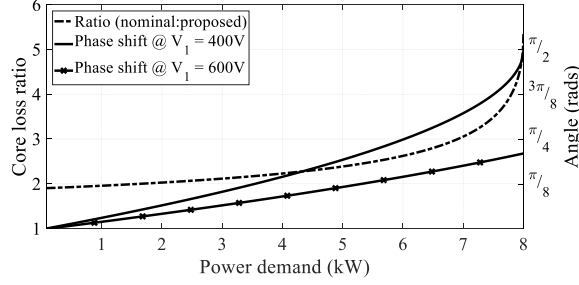


Figure 3.4 Core loss ratio (nominal:proposed) and phase shift between HFTx primary and secondary side voltages, θ_{12} , for the proposed ($V_1 = 400V$) and nominal case ($V_1 = 600V$) versus power demand.

Higher θ_{12} also helped reduce the flux linkage, and thus, $\hat{B}$, which makes the core loss be even smaller when applying the proposed control strategy at this load end. At lighter loads the θ_{12} for both cases become similar and closer to zero which implies that the weight the term $\theta_{12} \left(V_1 - \frac{V_2}{N}\right)^2$ in (3.10) had starts vanishing and thus, (3.10) become approximately equal to (3.9). However, (3.9) and (3.10) will never be exactly equal since not only there is always a small leftover in that term (since $\theta_{12} > 0$ is needed to transfer power), but, V_1 in the nominal case is higher and thus the term $\left(V_1 + \frac{V_2}{N}\right)^2$ will be higher compared to in the proposed case. As it can be visualized in (3.6), V_1 being higher in the nominal case also contributed to make the flux linkage always higher in this case compared to in the proposed one. The whole-load range reduction in volts-second (and thus, $\hat{B}$) when applying the proposed control strategy can be better seen graphically in Figure 3.5.

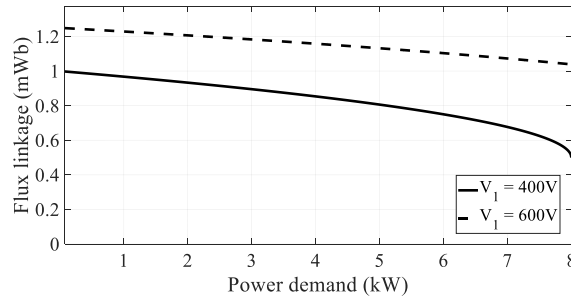


Figure 3.5 Flux linkage versus power demand for the proposed ($V_1 = 400V$) and nominal case ($V_1 = 600V$).

3.4 Simulation Results

3.4.1 Core Loss

To validate the theoretical analysis this section provides with simulation results based on the same parameters and components summarized in Table 3.1 and Table 3.2. ANSOFT Maxwell was used to obtain the core loss, and all simulations were taken for ten EV power demands that ranged from 800W to 8kW. The transformer voltages, magnetizing inductance voltage with its respective flux linkage, and resulting core loss waveforms are provided for both cases in Figure 3.6 and Figure 3.7, under full- and a light-load conditions, respectively. First, by comparing the proposed versus the nominal cases it can be observed that when the proposed control strategy is not implemented, zero instantaneous core loss is not achieved and higher flux linkage as well as peak value of core loss exists; both of these increase the average power loss. It can also be seen that the flux linkage is less in the full-load condition compared to in light-load; and the peak values closely match those theoretically shown in Figure 3.5. Furthermore, the results for the proposed case show that the more θ_{12} (as it is for the full-load condition), the more zero states inserted in the magnetizing inductance voltage, which indeed means longer clamping time in the flux linkage, and thus, more zero instantaneous core loss in this end of the load spectrum.

The 2D model of the transformer simulated in Maxwell along with the flux density distribution for the propose and nominal case at full-load condition is shown in Figure 3.8. This screenshot was taken at the time where peak flux linkage is reached, and, as expected, lower flux density is observed in the proposed case.

Finally, Figure 3.9 shows the theoretical and simulated core loss for the proposed and nominal cases. Although there is a slight error between the theoretical and simulated values, there is good agreement in their trend, as well as in the ratio between the nominal and proposed case. It

is confirmed that the proposed control strategy is indeed able to reduce the core loss for the whole load range. It can also be seen that the core loss reduction is highest (about 80%) at the full load condition as it was predicted in the previous section (see Figure 3.4). In addition, core loss is higher in lighter loads compared to heavier loads since less phase shift is needed, meaning more flux linkage in both cases, and in the proposed case it also means less zero states across the magnetizing inductance. The presented results validate the benefits of the proposed control strategy and confirm the discussions made in the previous sections.

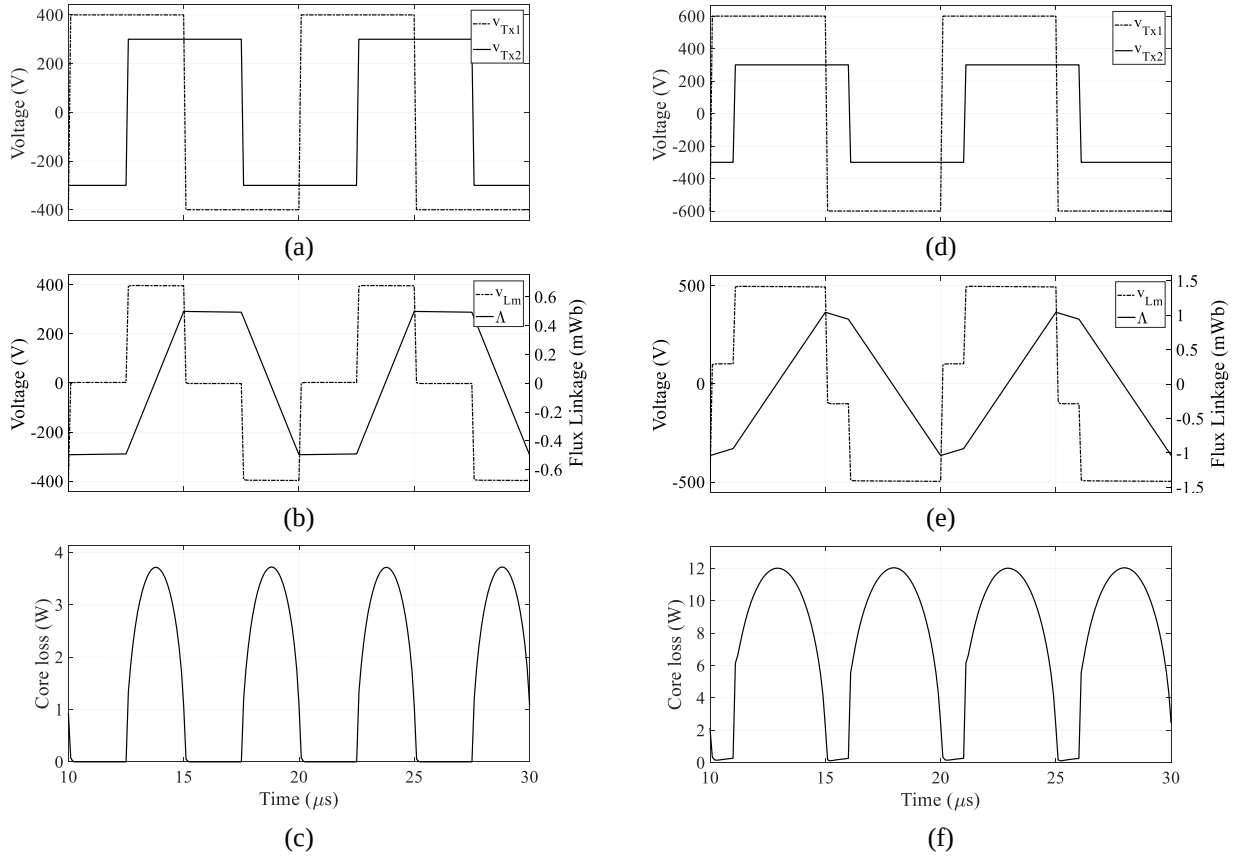


Figure 3.6 Maxwell simulation results under full-load condition (8kW) for the proposed (a-c) and nominal (d-f) cases. For the proposed case $\theta_{12} = 1.571rad$, and for the nominal case $\theta_{12} = 0.664rad$. Results were post-processed in MATLAB for better plot quality.

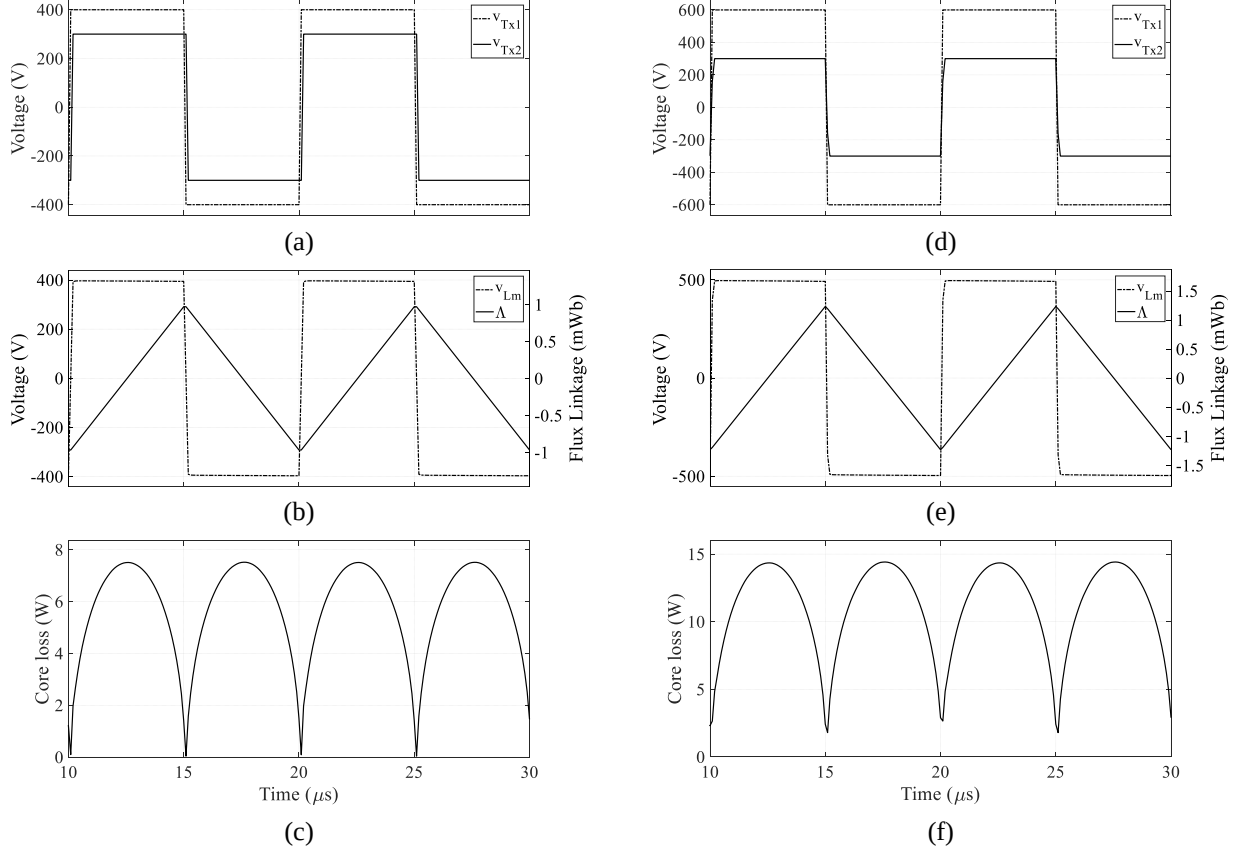


Figure 3.7 Maxwell simulation results under light-load condition (800W) for the proposed (a-c) and nominal (d-f) cases. For the proposed case $\theta_{12} = 0.081rad$, and for the nominal case $\theta_{12} = 0.053rad$. Results were post-processed in MATLAB for better plot quality.

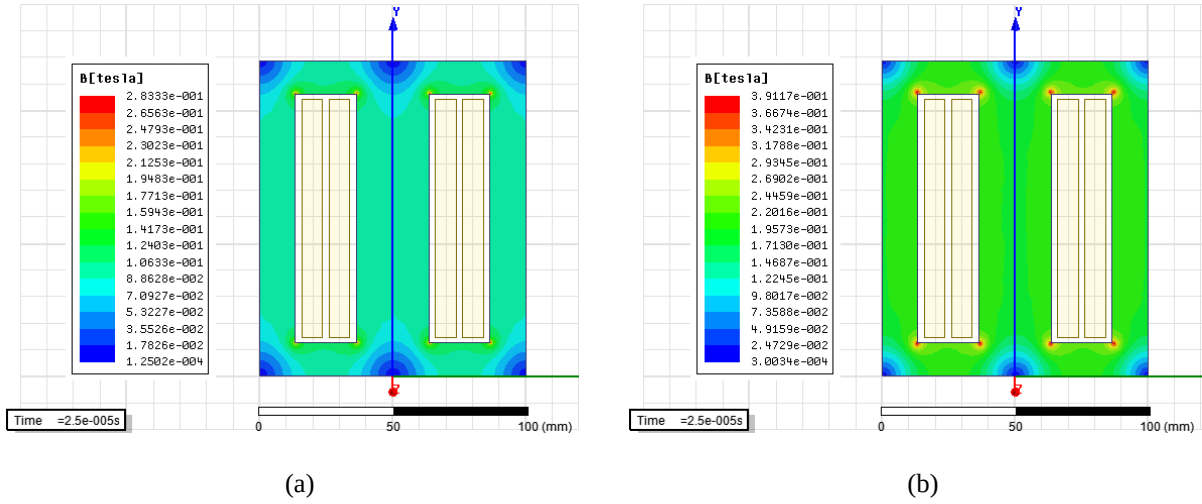


Figure 3.8 Maxwell 2D model of the HFTx with flux density distribution at full load: (a) Proposed, (b) Nominal.

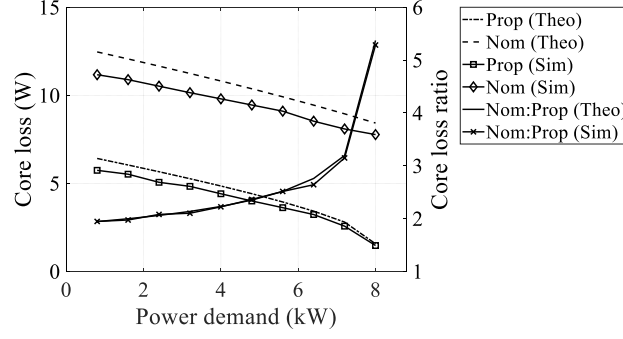


Figure 3.9 Theoretical and simulated value for the core loss vs power demand for the proposed and nominal case.

3.4.2 Overall Charger Efficiency and Loss Distribution

To make sure that the overall losses of the DAB is not negatively impacted by the proposed control strategy for core loss reduction, LTspice is used as the simulation tool to obtain semiconductor losses (using its SPICE model provided by manufacturer), and winding losses. Based on these losses and the core loss obtained from Maxwell, Figure 3.10 shows the simulated and theoretical overall efficiency of the DAB for the whole load range, for both, the proposed and nominal cases. Apart from the good agreement between the simulated and theoretical efficiencies, the proposed case achieve less overall efficiency close to full load conditions, but more for the rest of the load range. In fact, the efficiency improvement is much more at lighter load conditions though the core loss ratio was found to be less at this end of the load spectrum (see Figure 3.4). This is because not only core loss is less in the proposed case for the reasons already discussed, but, as mentioned at the end of section 3.2, using $V_1 = V_2/N$ has also been found to help reducing switching and conduction losses in DAB operated under regular phase shift [38]–[40]. On the other hand, there is a small portion at heavier loads where the nominal case has higher efficiency. The reason is that the proposed voltage was selected less than the nominal so as to achieve less flux linkage, so for the same heavy load, the RMS current in the proposed case is higher compared to in the nominal case. This does not hold true for the whole load range since circulating currents start to take over in the nominal case. The aforementioned discussion can be better visualized in

Figure 3.11 which shows the theoretical loss distribution for the proposed and nominal case versus power demand.

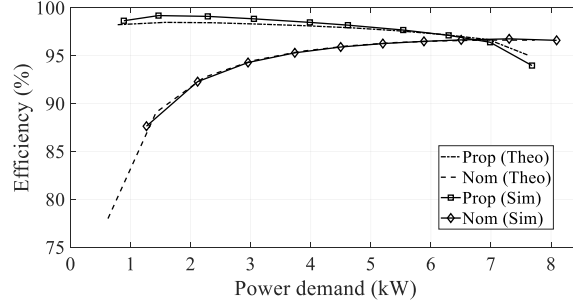


Figure 3.10 Theoretical and simulated efficiency versus power demand for the proposed ($V_1 = 400V$) and nominal case ($V_1 = 600V$).

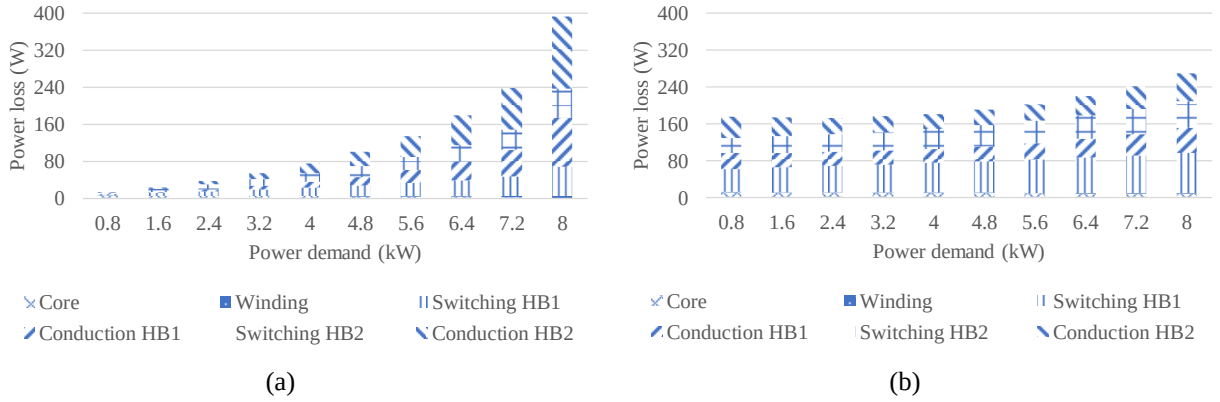


Figure 3.11 Theoretical loss distribution versus power demand for the proposed ($V_1 = 400V$) and nominal case ($V_1 = 600V$): (a) Proposed, (b) Nominal.

An aspect to consider is that the proposed control strategy can be even more impactful in the efficiency improvement of this system if the HFTx had higher core loss, more comparable to other losses in the system. This can happen in the event the transformer is optimized for high power density, which can be more desirable in systems where lower cost, size and weight are more important than higher efficiency.

Finally, the presented overall efficiency results reveal that if this DAB were to be physically implemented in a system with fixed V_1 and V_2 , then it is better to choose the proposed control strategy to operate the converter since it achieves higher efficiency for most of the load

range. However, if at least V_1 is variable, the nominal control strategy can be used for loads close to full-load, and the proposed core loss reduction strategy can be used for the rest of the load range.

3.5 Summary

HFTx are one of the most inefficient, bulky and heavy components in a power electronics system with galvanic isolation (such as EV chargers). For this reason, there has been many literatures in HFTx size and loss optimization; but these are offline-based approaches, limited to the transformer design and manufacturing, and typically rely on complex algorithms. In this chapter, an online-based approach used to specifically reduce the HFTx's core loss was proposed. This is accomplished, with a control strategy that reduces and/or clamps the transformer's flux linkage while still supplying a desired power to the load. The method is independent of the conventional approaches' state of the art, and as opposed to them, it can be implemented with high-degree of simplicity in a system that is already built. An 8-kW DAB controlled under single phase-shift was used to validate the control strategy, though the concept is explained so as to be replicable in other types of DAB control or other types of power converters. Theoretical analysis as well as simulation results from ANSOFT Maxwell showed a core loss reduction of about 50% at light load, and of about 80% at full load, when applying the proposed method compared to not doing so for the given system. Theoretical estimates as well as complementary LTspice simulation results showed that the overall efficiency of the DAB is higher when implementing the proposed control strategy for most of the load range.

Chapter 4 Reliable DC-Link Capacitor Sizing in Wireless Chargers

4.1 Background

Chapters 2 and 3 dealt with solutions to make plug-in XFC stations that are low in cost, small in size and highly-efficient, ultimately advancing this technology so as to help accelerate mass adaptation of EVs. However, for reasons already described in Chapter 1, the wireless technology will be more convenient in the long run, and so is the focus for the second half of this dissertation.

A typical top-level circuit configuration of the wireless charger is shown in Figure 4.1. The first stage consists of an ac/dc converter with power factor correction (PFC) to attenuate the harmonics imposed by the rectification process. Followed by this stage, a dc-link capacitor reduces the twice line-frequency (2ω) ripple flowing through the EV battery bank and provides reactive power. The second stage consists of an H-bridge inverter (which transforms the dc power into high frequency ac), a resonant network (principally used to transfer power from the system's primary (on the ground) to secondary (at the bottom of the EV) side), and an output rectifier used to transform the high frequency ac power into dc to charge the EV battery bank.

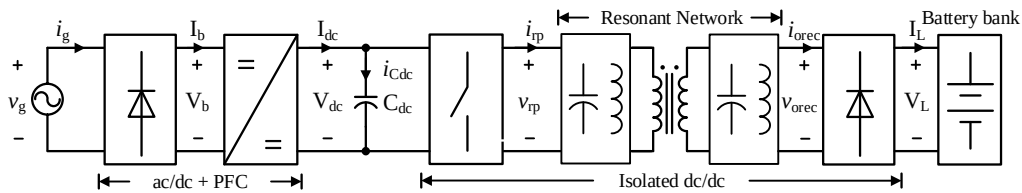


Figure 4.1 Top-level circuit configuration of a conventional wireless charger.

When designing this system, specifically, its dc-link capacitor (C_{dc}), the following well-known equation is used:

$$C_{dc} = \frac{\hat{v}_g \hat{i}_g}{2\Delta\tilde{v}_{Cdc}\omega_g V_{dc}}, \quad (4.1)$$

where $\hat{i}_g$ and $\hat{v}_g$ are the grid current and voltage peak values, respectively, ω_g is the grid fundamental angular frequency, V_{dc} is the average voltage across the capacitor, and $\Delta\tilde{v}_{Cdc}$ is its voltage ripple's peak-to-peak value. As it can be seen, the equation depends on a single operating condition, which it can inadvertently suggest that the station needs a larger and more expensive capacitor than needed, or it can cause reliability issues. Specifically since usually V_{dc} has a range (i.e., $V_{dcMin} \leq V_{dcNom} \leq V_{dcMax}$) the system designers can chose to size the capacitance based on the “worst-case” scenario (e.g., using V_{dcMin}); as it will be shown later in this chapter, this will lead to oversizing—affecting size and cost of the system. If they would have chosen V_{dcMax} , the capacitor would have been under sized, affecting system's reliability since more ripple than expected will flow for certain loads in the system. The aim of this dissertation is to avoid these issues by providing an analytical expression for C_{dc} that provides an insight of how the capacitance needed changes over the whole load range, according to the system control variables as well as the resonant network (RN) topology. Based on this expression, the minimum C_{dc} needed can be obtained to keep the dc-link voltage ripple within a desired limit for the whole load range, either by inspection or by running an optimization algorithm.

4.2 Analysis of the Wireless Charger System

4.2.1 Derivation of the Proposed Equation for DC-Link Capacitor Sizing

The following analysis assumes that the system is ideal, and neglects the high frequency components coming from the PFC and inverter (since their impact on the size of C_{dc} is small compared to the grid frequency). Assuming that the PFC converter is keeping the power factor (PF) at unity, the instantaneous value of the voltage and current at the grid rectifier is given as:

$$V_b = |\hat{v}_g \sin(\omega_g t)|, \quad (4.2)$$

$$I_b = |\hat{i}_g \sin(\omega_g t)|, \quad (4.3)$$

respectively. Then, the instantaneous power at the PFC converter output can be written as:

$$p_{dc} = V_{dc} I_{dc} = V_b I_b = \frac{\hat{v}_g \hat{i}_g}{2} - \frac{\hat{v}_g \hat{i}_g}{2} \cos(2\omega_g t). \quad (4.4)$$

Notice that p_{dc} has two components: a dc term, and a term varying at twice the grid-frequency (commonly referred to as the “ 2ω ripple”). Since it is undesirable to have the 2ω ripple flowing through the battery bank, it must be absorbed by C_{dc} . This means, that the C_{dc} instantaneous power and current can be expressed as:

$$p_{Cdc} = V_{dc} i_{Cdc} = \frac{\hat{v}_g \hat{i}_g}{2} \cos(2\omega_g t), \quad (4.5)$$

$$i_{Cdc} = \frac{\hat{v}_g \hat{i}_g}{2V_{dc}} \cos(2\omega_g t), \quad (4.6)$$

respectively. By using (4.6), the dc-link capacitor voltage ripple and its peak-to-peak value can be obtained as:

$$\tilde{v}_{Cdc} = \frac{1}{C_{dc}} \int i_{Cdc}(\tau) d\tau = \frac{\hat{v}_g \hat{i}_g}{4\omega_g C_{dc} V_{dc}} \sin(2\omega_g t), \quad (4.7)$$

$$\Delta \tilde{v}_{Cdc} = 2 \left(\frac{\hat{v}_g \hat{i}_g}{4\omega_g C_{dc} V_{dc}} \right) = \frac{\hat{v}_g \hat{i}_g}{2\omega_g C_{dc} V_{dc}}. \quad (4.8)$$

Since it is desired to observe the effect of the RN and system’s control variables in C_{dc} , it is necessary to write (4.8) as a function of the RN components and all three control variables (V_{dc} , D_{act} , and f_s). This is done by first calculating the average power flowing out of the H-bridge (P_{rp}) over one switching cycle T_s , with the aid of Figure 4.2. This figure shows a typical voltage and current waveform at the output of the H-bridge inverter of a series-based primary RN topology (such as series-series (SS) and series-parallel (SP)), but the same concept can be applied to any RN.

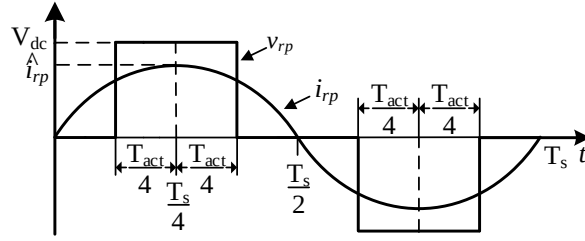


Figure 4.2 H-bridge output voltage and primary side resonant current for a series-primary RN.

Based on these curves,

$$P_{rp} = \frac{1}{T_s} \int_0^{T_s} v_{rp}(\tau) i_{rp}(\tau) d\tau = \frac{2V_{dc} \hat{i}_{rp} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{\pi}, \quad (4.9)$$

where $T_{act} = T_s D_{act}$ is the active state time interval, V_{dc} is the dc-link voltage, $\hat{i}_{rp}$ is the peak value of the current flowing at the resonant network primary side, ω_s is the angular switching frequency, φ_{irp} is the phase angle of i_{rp} with respect to the fundamental component of the H-bridge output voltage v_{rp} , and $\cos(\varphi_{irp})$ is the H-bridge power factor's displacement factor. In an ideal system, this power equals the average power coming from the grid (the dc term in (4.4)).

Therefore, the following equation can be formulated:

$$\frac{\hat{v}_g \hat{i}_g}{2} = \frac{2V_{dc} \hat{i}_{rp} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{\pi}. \quad (4.10)$$

By substituting (4.10) in (4.8), and solving for the dc-link capacitor:

$$C_{dc} = \frac{2\hat{i}_{rp} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{\pi \omega_g \Delta \tilde{v}_{Cdc}}. \quad (4.11)$$

This equation provides a relationship between the dc-link capacitor, the peak-to-peak voltage ripple across the capacitor, the resonant network characteristics, as well as the three conventional control variables used in this system: f_s , D_{act} , and V_{dc} . It is worth mentioning that the RN characteristics, the switching frequency, and the dc-link voltage information are all embedded in $\hat{i}_{rp}$, which can be derived for any of the topologies used as the resonant stage of the WPT system.

An example of this derivation is provided in the next subsection for the SS topology, but a similar process can be applied to any RN.

4.2.2 Derivation of the Current at the Resonant Network Primary Side for the Series-Series Topology

The following derivation is based on the SS-based wireless charger equivalent circuit shown in Figure 4.3, where C_{cp} and C_{cs} are the compensation capacitors in the primary and secondary sides, respectively, L_{lkp} and L_{lks} are the primary and secondary side leakage inductances, L_m is the magnetizing inductance, and $N = N_s/N_p$ is the transformer turns ratio. The excitation applied to this equivalent circuit is the voltage at the H-bridge inverter output, v_{rp} , and the equivalent resistor R_{ac} is commonly obtained by using the fundamental frequency approximation [43], that is, assuming that only the fundamental frequency component is involved in the power transfer. Under this assumption, the fundamental component of the voltage across the output rectifier input (which equals the voltage across R_{ac}) is given as:

$$v_{orec,1}(t) = \frac{4V_L}{\pi} \sin(\omega_s t), \quad (4.12)$$

and the current flowing into this rectifier (which equals the current flowing into R_{ac}) is:

$$i_{rs}(t) = \frac{\pi I_L}{2} \sin(\omega_s t), \quad (4.13)$$

where V_L is the system output voltage and I_L is the system output current. Therefore, R_{ac} can be obtained as:

$$R_{ac} = \frac{v_{orec,1}(t)}{i_{rs}(t)} = \frac{\frac{4V_L}{\pi} \sin(\omega_s t)}{\frac{\pi I_L}{2} \sin(\omega_s t)} = \frac{8V_L}{\pi^2 I_L} = \frac{8}{\pi^2} R_L, \quad (4.14)$$

where R_L is the system resistive load.

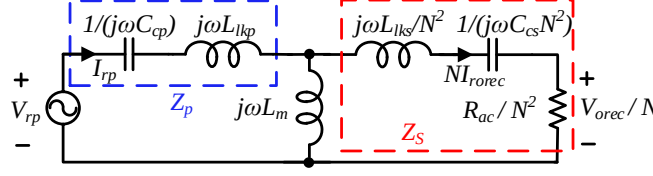


Figure 4.3 Simplified circuit of the wireless charger based on the SS resonant network.

Now that every parameter in the equivalent circuit is known, the current at the resonant network primary side $\hat{i}_{rp}$ can be obtained by a current divider, as follows:

$$\hat{i}_{rp} = \frac{\hat{i}_{rs}}{|k_{ires}(\omega_s)|} = \frac{\pi I_L}{2|k_{ires}(\omega_s)|} = \frac{\pi V_L}{2|k_{ires}(\omega_s)|R_L}, \quad (4.15)$$

where

$$k_{ires}(\omega_s) = \frac{\hat{i}_{rs}}{\hat{i}_{rp}} = \frac{\frac{1}{N}j\omega_s L_m}{j\omega_s L_m + Z_s}. \quad (4.16)$$

Notice the dependency of $\hat{i}_{rp}$ in the RN components, and the switching frequency as it was mentioned in the previous subsection. To show its dependency on V_{dc} , it is assumed that P_{rp} equals the instantaneous power flowing through the resistive load P_L , that is,

$$P_{rp} = \frac{2V_{dc}\hat{i}_{rp} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{\pi} = P_L = \frac{V_L^2}{R_L}. \quad (4.17)$$

By substituting (4.15) in (4.17) and solving for V_L ,

$$V_L = \frac{V_{dc} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{|k_{ires}(\omega_s)|}. \quad (4.18)$$

Then, by substituting (4.18) back into (4.15),

$$\hat{i}_{rp} = \frac{\pi V_{dc} \sin\left(\frac{\pi D_{act}}{2}\right) \cos(\varphi_{irp})}{2|k_{ires}(\omega_s)|^2 R_L}, \quad (4.19)$$

demonstrating the dependency of $\hat{i}_{rp}$ on V_{dc} . Finally, the phase angle of i_{rp} (φ_{irp}) is obtained by:

$$\varphi_{irp} = \arg(Z_{rp}), \quad (4.20)$$

where

$$Z_{rp} = \frac{v_{rp}}{i_{rp}} = Z_p + j\omega_s L_m || Z_s. \quad (4.21)$$

4.3 Case Study: Minimum DC-Link Capacitance for a Desired Voltage Ripple in Series-Primary Resonant Network Topologies

The behavior of (4.11) is analyzed graphically for the two-conventional series-primary topologies, SS and SP, to investigate which of them require a smaller C_{dc} . The analysis is done by using the WPT system shown in Figure 4.4 for the SS and Figure 4.5 for the SP, which parameters under nominal conditions and components values are shown in Table 4.1.

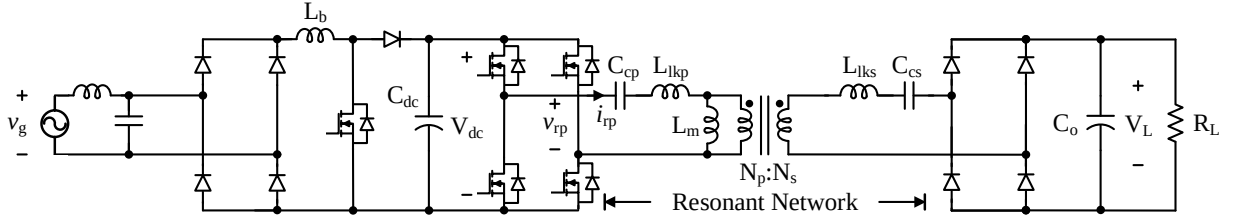


Figure 4.4 Series-Series-based wireless power transfer system for electric vehicle battery charging.

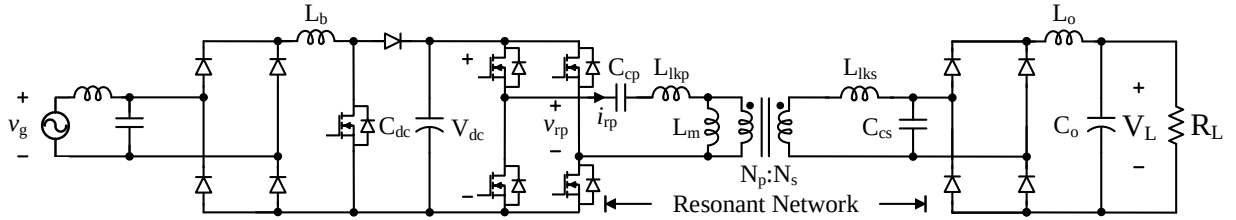


Figure 4.5 Series-Parallel-based wireless power transfer system for electric vehicle battery charging.

Table 4.1 WPT system parameters and components value

Parameter	Value	Component	Value
Grid voltage (v_g)	120VRMS	L_b	1mH
Grid frequency	60Hz	C_{dc}	0.9mF
Resonant frequency	54kHz	C_{cp}	18.21nF
Output voltage (V_L)	200V	L_{lkp}	0.4151mH
Output power (P_L)	1kW	L_m	61.87μH
Transformer turns ratio	15:20	L_{lks}	1.072mH
DC-link voltage (V_{dc})	250V	C_{cs}	7.349nF
V_{dc} peak to peak ripple	5% of V_{dc}	R_L	40Ω
Active state duty cycle	0.5	C_o	1mF
Base value for C_{dc}	0.1842mF	L_o	1mH

The relationship between C_{dc} and P_{rp} , and f_s is shown in Figure 4.6 for different resistive loads (R_L) in the SS topology. These curves are at nominal D_{act} and V_{dc} . Notice that if f_s is kept at resonance (f_r), or between frequencies f_L and f_u , as the load becomes lighter, C_{dc} needs to be increased in order to keep the desired $\Delta\tilde{v}_{Cdc}$. However, at light load operation, either f_s , D_{act} , and/or V_{dc} needs to change in order to meet the power demand (recall that ideally, P_{rp} equals to the power supplied to the load (P_L)). Consider that it was decided to regulate the load power by changing f_s , while keeping D_{act} and V_{dc} at their nominal values. This means that since the full load operation (1kW = 1pu) was designed to be at f_r , f_s needs to be increased or decreased to at least frequencies f_U or f_L , respectively, to meet the power demand. Therefore, irrespective of the load variation, $C_{dc} = 4.9pu$ is large enough to keep the desired $\Delta\tilde{v}_{Cdc}$.

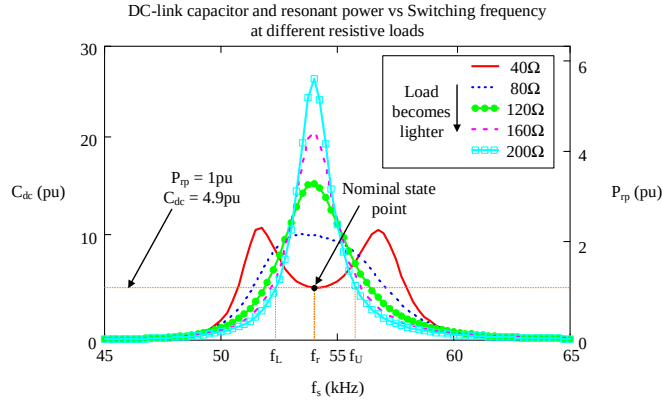


Figure 4.6 DC-link capacitor and resonant power versus H-bridge inverter's switching frequency at different loads for the SS topology.

Figure 4.7 shows the relationship between C_{dc} and f_s for different D_{act} in the SS topology. The curves shown in here are at 40Ω load and nominal V_{dc} . Notice that the effect of decreasing D_{act} from its nominal results in a decrease in the C_{dc} needed to keep the desired $\Delta\tilde{v}_{Cdc}$. Since a decrease in D_{act} must be done to transfer less amount of power when the load goes lighter than full load (assuming that a desired f_s (i.e. f_r) and V_{dc} still provide higher power than the required),

the minimum C_{dc} needed to keep a desired $\Delta\tilde{v}_{Cdc}$ can still be obtained at the nominal state point (4.9pu).

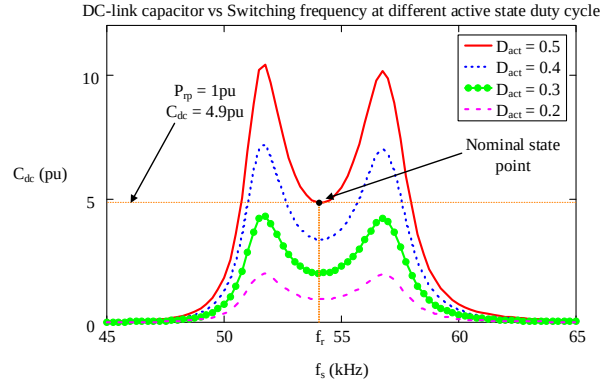


Figure 4.7 DC-link capacitor versus H-bridge inverter's switching frequency at different active state duty cycles for the SS topology.

Finally, the relationship between C_{dc} and f_s for different V_{dc} values is shown in Figure 4.8 for the SS RN. These curves are at 40Ω load and nominal D_{act} . Here, the pattern is similar to the previous case, that is, the smaller the V_{dc} , the smaller the C_{dc} needed to keep the desired amount of $\Delta\tilde{v}_{Cdc}$. Since V_{dc} must be decreased to transfer less amount of power for loads lighter than full load (assuming that a desired f_s and D_{act} still provide higher power than the required), the minimum C_{dc} needed to keep the desired amount of $\Delta\tilde{v}_{Cdc}$ is again at the nominal state point (4.9pu).

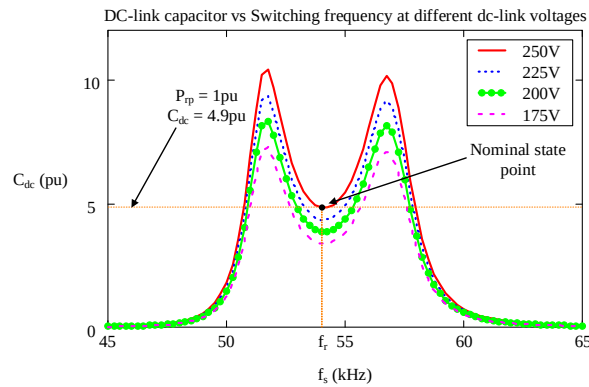


Figure 4.8 DC-link capacitor versus H-bridge inverter's switching frequency at different dc-link voltages for the SS topology.

Based on the previous analysis, it can be concluded that the minimum C_{dc} needed for a desired $\Delta\tilde{v}_{Cdc}$ is found at the nominal state (i.e., nominal V_{dc} , D_{act} , and f_s) for a SS RN topology. For the reasons already explained in section 4.1, a designer using the conventional equation (4.1) could have easily miss this, unless by coincidence it utilized V_{dcNom} in the equation.

Similar analysis can be done for the SP topology, where the C_{dc} vs D_{act} and C_{dc} vs V_{dc} behavior is the same as in the SS RN (Figure 4.7 and Figure 4.8). However, it can be seen from Figure 4.9 that the C_{dc} vs f_s behavior (also at nominal D_{act} and V_{dc} .) for different R_L is different compared to the SS. The operation at resonant frequency of the SP topology will require a huge C_{dc} to keep a desired $\Delta\tilde{v}_{Cdc}$. If $C_{dc} = 4.9pu$ (minimum found for SS) is wanted while keeping nominal D_{act} and V_{dc} , f_s needs to be increased or decreased to at least frequencies f_U or f_L , respectively, to meet the power demand. If this capacitance is desired while keeping operation at f_r , the system will require a drastic decrease in D_{act} (which increases hard switching losses) and/or a smaller V_{dc} . Although the same minimum C_{dc} can be utilized in both topologies, there will be a difference in the control variables selection and limitation to regulate the load power, which will ultimately lead to different system performance.

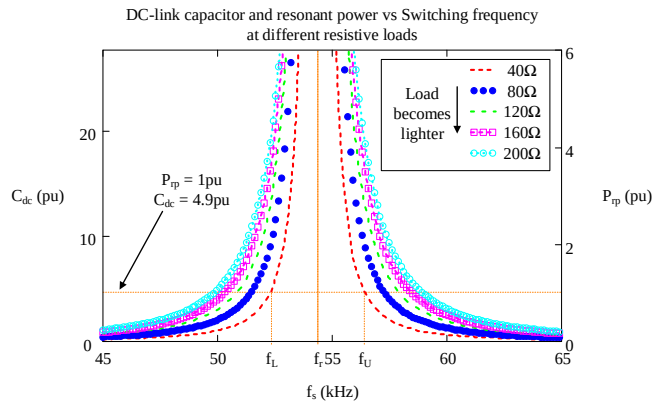


Figure 4.9 DC-link capacitor and resonant power versus H-bridge inverter's switching frequency at different loads for the SP topology.

4.4 Simulation Results

In order to validate the proposed equation, simulations were performed based on the SS topology shown in Figure 4.4, and the components shown in Table 4.1. To support the analysis made in the previous section, every simulation used the optimum dc-link capacitor found by inspection, $C_{dc} = 4.9\mu F$ or $0.9mF$. Five scenarios were evaluated to measure $\Delta\tilde{v}_{Cdc}$, all of which correspond to the analysis made in section 4.3. The parameters used for each scenario are shown in Table 4.2, and the simulation results are shown in Figure 4.10.

Table 4.2 Parameters used for each simulation

Scenario	P_L	V_L	R_L	f_s	D_{act}	V_{dc}
a	1kW	200V	40Ω	54kHz	0.5	250V
b	1kW	200V	40Ω	57.95kHz	0.5	250V
c	500W	200V	80Ω	54kHz	0.225	250V
d	500W	200V	80Ω	58.3kHz	0.5	250V
e	500W	200V	80Ω	54kHz	0.285	200V

A graph showing the theoretical $\Delta\tilde{v}_{Cdc}$ (calculated by using (4.11)), and simulated value for the five cases is shown in Figure 4.11. Notice that for all scenarios the calculated and simulated values of $\Delta\tilde{v}_{Cdc}$ are approximately equal, providing a simulation-based validation of the expression obtained in (4.11). Any difference could be attributed to the fundamental frequency approximation used for the mathematical model. Also notice that at full load the ripple is higher than at half load, but equal or smaller than 12.5V, which is how the system was designed (see Table 4.1). This voltage ripple trend coincides with the analysis made in section 4.3.

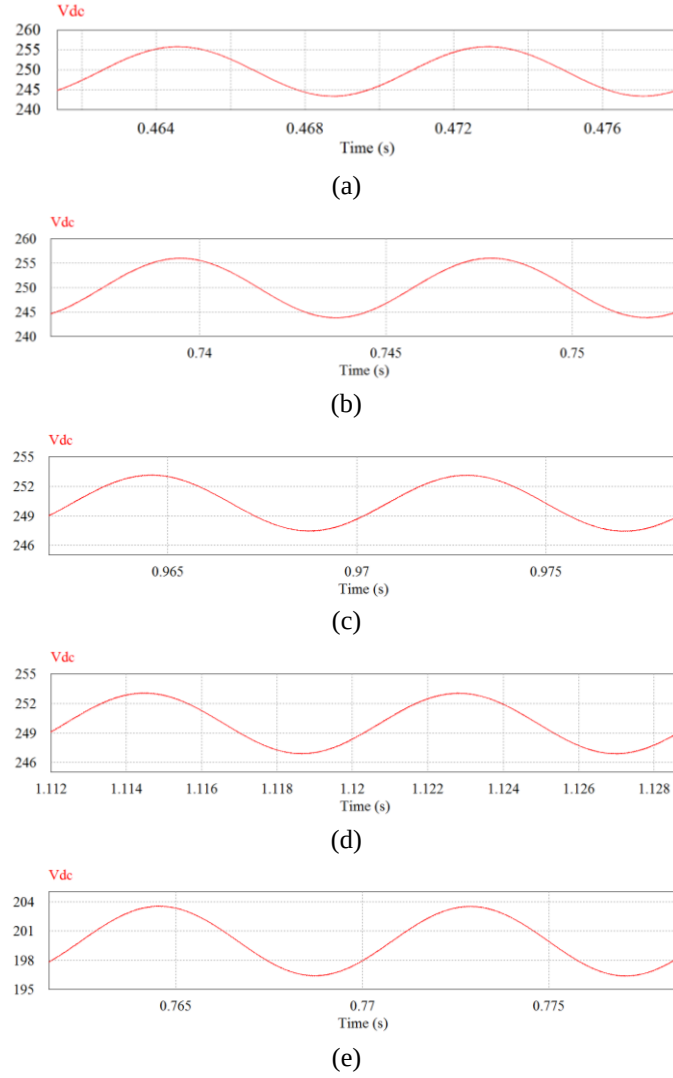


Figure 4.10 Simulation results: DC-link capacitor voltage (V) for the five scenarios.

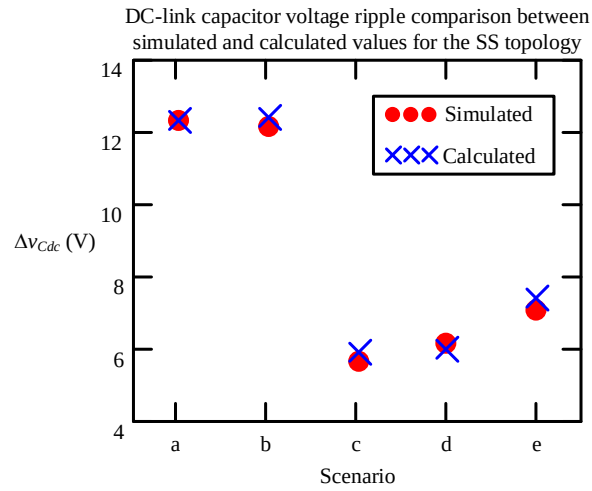


Figure 4.11 Comparison between the theoretical and simulated value of $\Delta \tilde{v}_{dc}$ for the SS RN.

4.5 Summary

In this chapter, a generalized equation to size the dc-link capacitor in conventional wireless charger is proposed and validated through simulations. As it was shown, compared to the conventional equation (which relies on a single operating condition), the proposed one is more reliable and avoids oversizing (directly benefiting size and cost of the system). This is because it provides an insight on how the resonant network characteristic and system's control variables affect the capacitor size. With this equation, the minimum dc-link capacitance needed to keep the dc-link voltage ripple within a desired limit for the whole load range can be obtained. A comparison between the conventional series-primary resonant networks in terms of the dc-link capacitance needs was also presented.

Chapter 5 Z-Source-Based Wireless Charger with Power Factor Correction for a Low-Cost and Highly-Reliable System

5.1 Background

The previous chapter made improvements on size, cost, and reliability on the conventional wireless charger. However, as it was described in it, the conventional wireless charger is typically made of a two-stage (ac/dc + PFC, and isolated dc/dc) converter (Figure 5.1), the design of which follows the standard procedure with mature techniques [44]–[52]. This charger penalizes overall size, cost, and loss due to its inherent need for extra semiconductor devices with associated heat sinks and control circuitry [53]–[55].

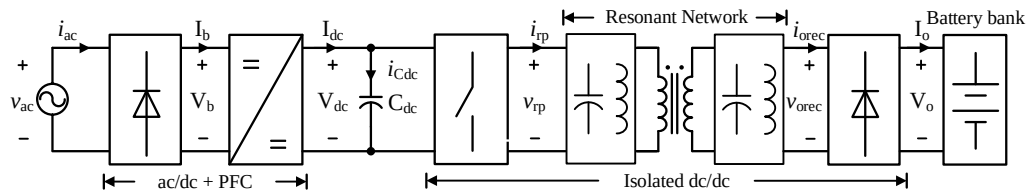


Figure 5.1 Block diagram of a conventional wireless charger.

Single-stage chargers have also been studied. They correct the power factor (PF) while regulating the system output voltage simultaneously. Previous research has been conducted in single phase single stage (S^2PFC) topologies [56]–[60]. Most of them have only one switch, thus achieving low overall cost and simplicity. However, these converters are derived from the flyback and therefore, they all suffer from high stress on the semiconductor switch, leading to the use of a high voltage device, and having a large conduction loss. For this reason, the S^2PFC approach may

only be attractive for low power applications (i.e. less than 100W), where the cost is the major impact on the design [61].

Other topologies have integrated the front-end PFC converter with a resonant converter. An example of this kind of topology is presented in [62], where a boost converter is integrated with a half-bridge LLC converter. Nevertheless, the power rating for this topology is limited, since the boost converter can only operate at the discontinuous conduction mode because the LLC converter duty cycle is fixed at 50%.

A family of single-stage resonant AC/DC converters with inherent PFC was proposed in [63]. It is mainly derived from the LLC converter such that it only has two switches. There is one bulk capacitor maintaining the energy over the whole fundamental period. However, at low line voltage, there might be a surge line current; at high line voltage, power is only drawn from the bulk capacitor, which makes the grid current as discontinuous over a fundamental cycle as a buck-type PFC converter does.

Given that in general, the power rating of single stage chargers is limited to about less than 300W [55], wireless chargers have adopted the two-stage conversion process, where the conventional boost converter is the most commonly used PFC converter in modern EV battery chargers [64]. This is the reason why this converter will be used as a benchmark in this chapter.

5.1.1 Conventional Wireless Charger

The conventional boost-converter-based wireless charger is shown in Figure 5.2, where the DC/DC stage consists of a Series Resonant Converter (SRC), which is the most commonly used converter for wireless charger applications [65].

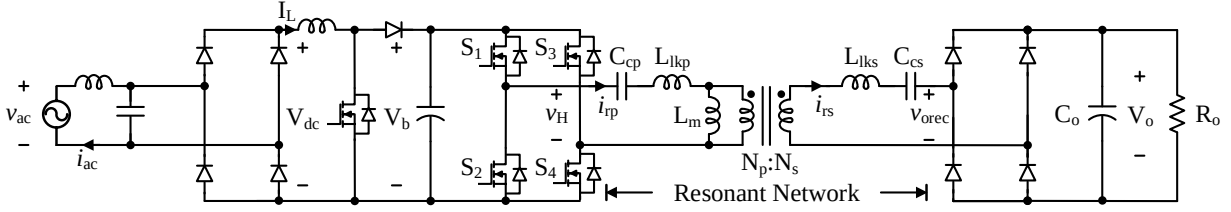


Figure 5.2 Boost-converter-based wireless charger.

In general, the conventional boost PFC converter offers high efficiency, high power factor (PF), high power density, and low cost [66]. Nevertheless, the boost capacitor ripple current is very high [64], [66]. As the power level increases, the system input rectifier losses significantly degrade the efficiency and require efforts to deal with heat dissipation. Because of this, the boost PFC converter is good for low to medium power range, up to approximately 3.5 kW. For power levels above that, designers typically parallel discrete semiconductors, or use expensive diode semiconductor modules, which increases the overall system cost [64], [66]. Additionally, the boost converter switch is operated under hard switching conditions and because of this, the converter has high switching losses, which limit the switching frequency range of the system. Finally, the boost diode reverse recovery produces high electromagnetic interference (EMI), which might cause unexpected shoot-through states that damage the system, or that trigger protection and cause unexpected system shut down [67]–[69]. In order to eliminate the drawbacks related to its inherent semiconductor devices, while improve the system reliability, a new PFC converter is introduced in this dissertation.

5.1.2 Proposed Wireless Charger

This dissertation proposes to use the Z-source Network (ZSN) as a new converter for PFC applications. The ZSN main topology was introduced in [70] and has been widely used mainly for voltage regulation applications. For wireless charger applications, the ZSN can be located at the PFC stage followed by the isolated DC/DC converter, which in this case is the conventional SRC.

The resultant wireless charger proposed topology is named as Z-source resonant converter (ZSRC). The circuit schematic of this converter is shown in Figure 5.3. The core part of this system (everything but AC/DC conversion stage) was first introduced in 2010 by [65] but for DC/DC conversion.

The ZSN in the ZSRC adds the unique feature of inherent PFC without adding extra switches as conventional PFC converters do. It can do this since it provides immunity to the H-bridge inverter shoot-through states, which not only increases the system reliability, but adds a control variable to the system (shoot-through duty cycle (D_{st})) that can be used to shape the input current as a sinusoidal waveform and in phase with the input voltage. This variable also provides a boost feature to the system, which is why it is typically used for voltage regulation [70]. However, to regulate the output voltage, the proposed ZSN-based charger uses the active state duty cycle (D_{act}), which is a conventional control variable used in SRCs. Because both control variables are encrusted in the SRC H-bridge inverter, the ZSRC does not require additional control circuitry to perform the PFC. In other words, because of the ZSN, the ZSRC can perform PFC and DC/DC conversion in one stage. This means that the ZSN can be categorized as a family of the single stage PFC converters, but with the ability of being used in high-power applications. In addition to the aforementioned positive features of the proposed PFC converter, the ZSN offers further advantages over the conventional boost PFC converter. These are described in the following subsection.

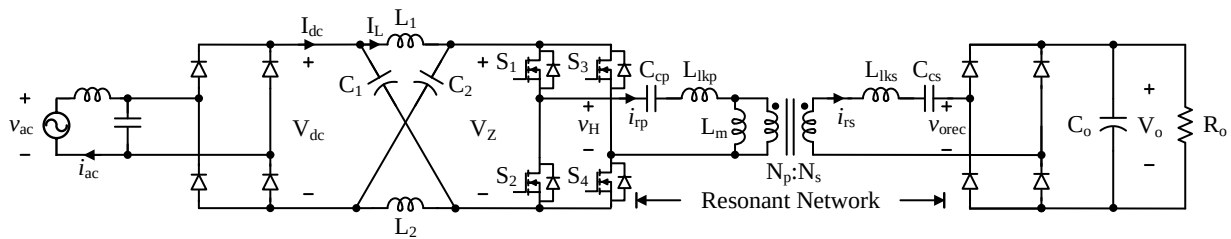


Figure 5.3 Proposed ZSN-based wireless charger: Z-source resonant converter.

5.2 Top-level Comparison between the Proposed and Conventional Wireless Chargers

5.2.1 Reliability Comparison

Adding the ZSN to the wireless charger increases the system reliability since the ZSN is immune to shoot-through states, thus, shoot-through due to mis-gating or EMI noise will not affect the system operation; whereas for conventional PFC converters shoot-through states can destroy the circuit. The ZSN is not only more reliable due to this feature, but, according to [71], the capacitors and semiconductor devices have higher failure and degradation rates (30% and 21%, respectively) among all components in a power electronic system. The 21% failure rate of the semiconductor devices does not even count soldering failure rate which adds another 13% to the overall semiconductor failure rate. This makes the existence of a semiconductor device in a system less reliable compared to that of capacitors. The traditional PFC boost converter has two semiconductor devices and a capacitor, whereas the ZSN has no semiconductor devices and two capacitors. Based on the previous data, the ZSN is expected to have a lower failure and degradation rate compared to the conventional boost PFC converter, thus a better lifetime.

5.2.2 Cost Comparison

Although the ZSN reduces the number of power semiconductors in the system (and so, its associated the size and cost due to the extra heat sinks and control circuitry [72]), it slightly increases the number of passive components compared to the boost PFC converter with one additional capacitor and inductor. However, to minimize the size, weight and cost of the Z-source inductors, they can be coupled together [73]. Furthermore, it can be proven that the proposed control strategy to achieve power factor correction can be applied to the modified versions of the original Z-source [74]. So, if the size, cost and weight need to be reduced even further, a Trans-Z-

source can be used instead of the original Z-source, which gets rid of one capacitor, while using coupled inductors [75], making it even much more competitive compared to the boost-converter-based wireless charger.

5.2.3 Loss Comparison

In order to make a loss comparison between the proposed and conventional PFC converter for the charger, their conduction and switching losses are calculated in this subsection.

5.2.3.1 Conduction losses comparison

To obtain information about the conduction losses, the device current conduction index (DI) is calculated under the same boost ratio (B) for the semiconductors contained in both systems. This index is defined by the following expression:

$$DI = \left[\frac{\sum_{k=1}^n N_k I_k}{I_{base}} \right]_{p.u.}, \quad (5.1)$$

where N_k is the number of semiconductor devices that are simultaneously conducting an average current I_k at any time instant in a sub-system k , and I_{base} is the base current used for the per unit calculation. As shown before, the charger consists of two sub-systems, the AC/DC + PFC stage, and the isolated DC/DC stage. For this comparison, the isolated DC/DC stage will be SRC on both systems. Since the power flow after the H-bridge of the SRC is the same independent of the AC/DC + PFC stage, it will not be considered as part of the analysis.

Boost-converter-based wireless charger

The analysis of the charger with the PFC stage based on the conventional boost converter (Figure 5.2) is done by assuming that the SRC is operating at 50% duty cycle, and at rated power. This means that at any time instant there are two switches in the H-bridge inverter conducting an RMS current of I_{rp} . For the boost converter stage, when the boost switch is either ON or OFF, the boost inductor current I_L will flow through the two diodes in the input rectifier and through the

boost converter diode. By taking I_{rp} as the base value, the DI for the boost-converter-based charger is given as:

$$DI_b = \frac{1}{I_{rp}}[3I_L D + 3I_L(1-D) + 2I_{rp}] = \frac{1}{I_{rp}}[3I_L + 2I_{rp}] p.u. \quad (5.2)$$

where “D” is the boost converter duty cycle. The boost ratio of a boost converter is related to I_L and I_{rp} as follows:

$$B = \frac{1}{1-D} = \frac{I_L}{I_{rp}}. \quad (5.3)$$

By substituting (5.3) in (5.2), the device conduction index expression for the boost-converter-based charger is given as:

$$DI_b = [3B + 2] p.u. \quad (5.4)$$

ZSN-based wireless charger

Now the charger is analyzed with the PFC stage based on the ZSN (Figure 5.3), and at rated power conditions. During the active and conventional zero states’ time intervals, there are always two switches in the H-bridge inverter conducting an RMS current of I_{rp} , and two diodes in the input rectifier conducting a current of $(2I_L - I_{rp})$, where I_L is the ZSN inductor current. During the shoot-through states’ time intervals, the four switches in the H-bridge inverter are conducting; one of the top switches is conducting a current of $(I_L - I_{rp}/2)$ while the other is conducting a current of $(I_L + I_{rp}/2)$, and the same is happening with the bottom switches. During this time interval the voltage across the ZSN input is higher than the grid voltage and therefore the input rectifier is not conducting. By taking I_{rp} as the base value, the DI for the ZSN-based charger is given as:

$$DI_{ZSN} = \frac{2}{I_{rp}} \left[((2I_L - I_{rp}) + I_{rp})(1 - D_{st}) + \left((I_L - \frac{I_{rp}}{2}) + (I_L + \frac{I_{rp}}{2}) \right) D_{st} \right] = \left[\frac{4I_L}{I_{rp}} \right] p.u. \quad (5.5)$$

The boost ratio of the ZSN is related to I_L and I_{rp} as follows:

$$B = \frac{1}{1-2D_{st}} = \frac{I_L}{I_{rp}}. \quad (5.6)$$

By substituting (5.6) in (5.5) a device conduction index expression for the ZSN-based charger is obtained as follows:

$$DI_{ZSN} = [4B]_{p.u.} \quad (5.7)$$

Figure 5.4 shows a device current conduction index comparison between the boost-converter-based and ZSN-based charger under different boost ratios. Notice that when the boost ratio is between 1 and 2, the ZSN-based charger has lower DI which leads to a smaller conduction loss.

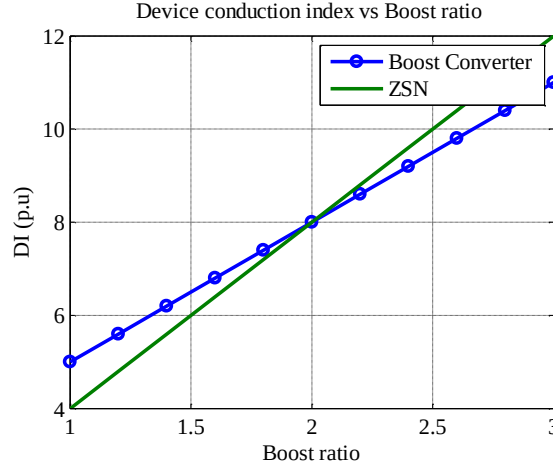


Figure 5.4 Device conduction index comparison between the boost-converter-based and ZSN-based wireless charger under different boost ratios.

5.2.3.2 Switching losses comparison

To obtain switching loss information of the two converters, it is assumed that all diodes are SiC, and that the converters are working under continuous conduction mode. As in the conduction losses analysis, the comparison is made under the same boost ratio.

Boost-converter-based wireless charger

At every switching cycle the boost converter switch S_b will have one “turn-on” and one “turn-off” transition (two switching transitions in total). The same happens with the four switches

at the H-bridge. Assuming that the voltage and current rising and falling time are the same, and equal to t_{rise} and t_{fall} , respectively, the switching time delay is defined as $t_d = t_{rise} + t_{fall}$. Then, the switching power loss in terms of boost ratio is approximated as follows:

$$P_{sw_b} = 2 \frac{1}{2} t_d [I_L V_b + 4 I_{rp} V_b] f_s, \quad (5.8)$$

where f_s is the system switching frequency, and V_b is the H-bridge inverter input voltage in Figure 5.2. I_L can be expressed in terms of I_{rp} and the duty cycle by using (5.3), resulting in:

$$P_{sw_b} = t_d f_s \left[\frac{I_{rp}}{1-D} V_b + 4 I_{rp} V_b \right] = t_d f_s I_{rp} V_b (B + 4) \quad (5.9)$$

By taking $t_d f_s I_{rp} V_b$ as a base value, the switching loss in a per-unit quantity is obtained as follows:

$$P_{sw_b}^{p.u.} = [B + 4]_{p.u.} \quad (5.10)$$

ZSN-based wireless charger

For the ZSN-based charger, at every switching cycle the 4 switches at the H-bridge have one “turn-on” and one “turn-off” transition (2 switching transitions in total) that occur between the shoot-through and active states’ time intervals. As mentioned before, during the shoot-through time intervals two of the switches will carry a current of $I_L - I_{rp}/2$ and the other two carry a current of $I_L + I_{rp}/2$. Following the same assumptions made for the boost-converter-based charger, the switching power loss in terms of boost ratio is approximated as:

$$P_{sw_{ZSN}} = 2 \frac{1}{2} t_d 2 V_Z \left[\left(I_L - \frac{I_{rp}}{2} \right) + \left(I_L + \frac{I_{rp}}{2} \right) \right] f_s = 4 t_d f_s I_L V_Z \quad (5.11)$$

where V_Z is the H-bridge input voltage in Figure 5.3. I_L can be expressed in terms of I_{rp} and D_{st} by using (5.6), resulting in:

$$P_{sw_{ZSN}} = t_d f_s (4 V_Z) \left(\frac{I_{rp}}{1-2D_{st}} \right) = t_d f_s V_Z I_{rp} (4B). \quad (5.12)$$

By taking the same base value as for the boost-converter-based charger ($t_d f_s I_{rp} V_Z$), the switching loss in a per-unit quantity is given as:

$$P_{swZSN}^{p.u.} = [4B]_{p.u.} . \quad (5.13)$$

Figure 5.5 shows the switching loss comparison between the boost-converter-based and ZSN-based charger under different boost ratios. Notice that when the boost ratio is between 1 ~ 1.34, the ZSN-based charger has a lower switching loss.

Based on the analysis made between the conduction and switching loss, the ZSN-based charger has a better performance under boost ratios between 1 ~ 1.34, whereas there is a trade-off between switching and conduction loss for boost ratios between ~1.34 and 2. For boost ratios greater than 2, the boost-converter-based charger has a better performance.

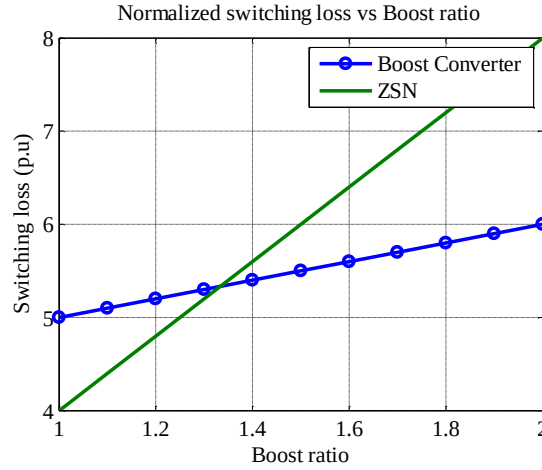


Figure 5.5 Switching loss comparison between the boost-converter-based and ZSN-based wireless charger under different boost ratios.

5.3 Analysis of the Proposed Z-Source-Based Wireless Charger

5.3.1 Shoot-Through Duty Cycle Derivation for Power Factor Correction

An expression for the shoot-through zero state duty cycle (D_{st}) in terms of the H-bridge output voltage (v_H) and the AC input voltage (v_{ac}) is derived in this subsection. This expression is used to shape the AC input current (i_{ac}) as a sinusoidal waveform while it is in phase with v_{ac} , and is based on the three different states of the ZSRC: active state, shoot-through zero state, and conventional zero state. The ZSRC simplified circuit used to derive this expression is shown in

Figure 5.6, and the H-bridge switches PWM, H-bridge output voltage (v_H), and the current at the resonant network primary side (i_{rp}) waveforms over one switching (resonant) cycle are shown in Figure 5.7. This figure also shows the time intervals for the three ZSRC states.

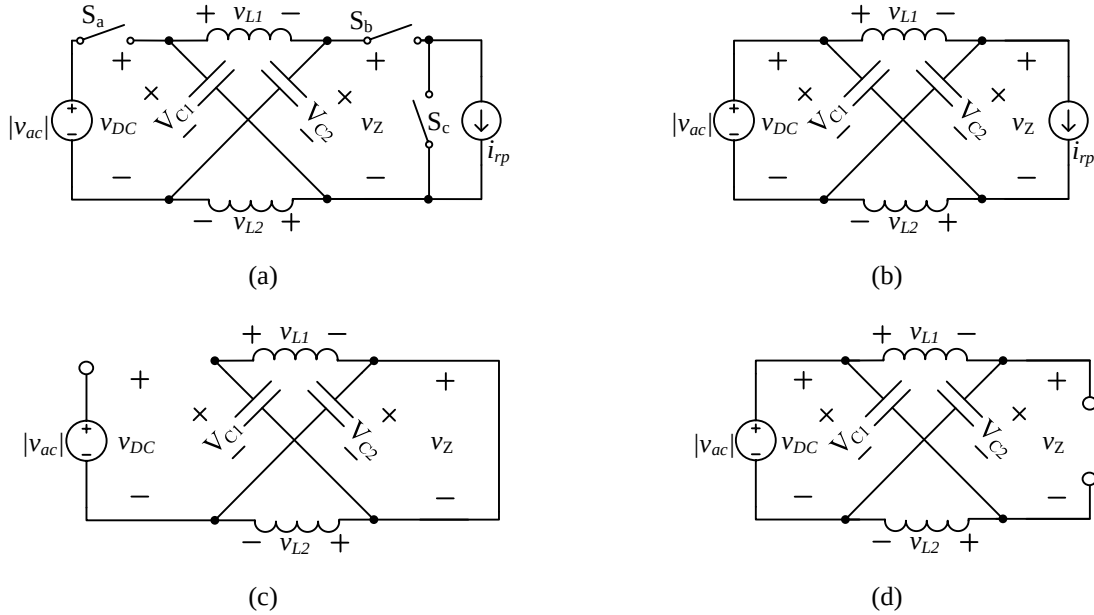


Figure 5.6 ZSRC simplified circuit (a): during active states (b), during shoot-through zero states (c), during conventional zero states (d).

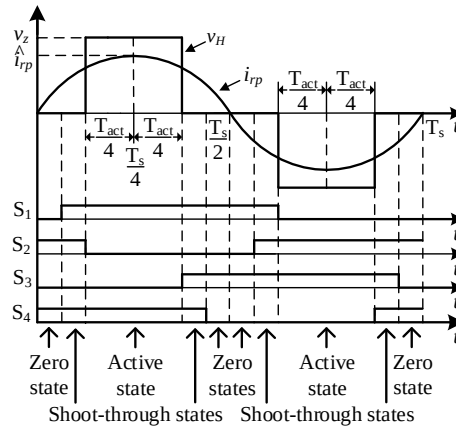


Figure 5.7 ZSRC H-bridge output voltage, primary side resonant current, and H-bridge switches PWM waveforms.

As can be seen in Figure 5.6a, for general analysis purposes, the AC voltage source together with the input rectifier were modeled as a DC voltage source with value of $|v_{ac}|$ (absolute value of AC input voltage) in series with a switch S_a . The H-bridge inverter was replaced by the switches

S_b and S_c . The resonant network together with the output rectifier and DC load were replaced by a current source (i_{rp}), since a sinusoidal stiff current is flowing through the resonant network at any time. This is because the resonant network acts as a band pass filter, allowing only the current at resonant frequency to flow. To simplify the analysis, the following derivation assumes that the ZSN is symmetrical. This means that the ZSN capacitors are equal ($C_1 = C_2 = C$), and the same regarding its inductors ($L_1 = L_2 = L$), therefore, $V_{C1} = V_{C2} = V_C$, and $v_{L1} = v_{L2} = v_L$.

5.3.1.1 Active states

During the two active states' time intervals ($T_{act}/2$, where T_{act} represents the total active states time interval in one switching cycle T_s), two diagonal switches in the H-bridge are ON while the two remaining are OFF. Also, the input side rectifier of the system is forward biased. This means that the switches in the simplified circuit (Figure 5.6a), S_a and S_b are ON, while the switch S_c is OFF, leading to the circuit shown in Figure 5.6b. Here, the voltage source as well as the inductors charge the capacitors, boosting the DC voltage across the inverter bridge [76]. Also, the power flows from the ZSN to the SRC and energizes the DC load. The inductor voltage for this time interval is given as:

$$v_L = \frac{1}{2}(|v_{ac}| - v_Z) = \frac{1}{2}(|\hat{v}_{ac} \sin(\omega t)| - v_Z). \quad (5.14)$$

where $\hat{v}_{ac}$ is the peak value of the AC input voltage, and ω is the line angular frequency.

5.3.1.2 Shoot-through zero states

During the four shoot-through zero states' time intervals ($T_{st}/4$, where T_{st} represents the total shoot-through time interval in one T_s), three switching devices in the H-bridge are ON and the remaining one can be either ON or OFF. Also, the input side rectifier is reverse-biased. This means that for the simplified circuit (Figure 5.6a), the switch S_a is OFF, and S_b and S_c are ON, leading to the circuit shown in Figure 5.6c. It is worth mentioning that in order to minimize

switching losses by extra switching actions, the shoot-through duty cycle should be evenly distributed just before and after each active state time interval as shown in Figure 5.7. Here, the capacitors will transfer their electrostatic energy to the inductors (this is how the ZSN can boost the voltage) [76]. The inductor voltage for this time interval is given as:

$$v_L = V_C. \quad (5.15)$$

5.3.1.3 Conventional zero states

During the four conventional zero states' time intervals ($T_{zer}/4$, where $T_{zer} = T_s - T_{act} - T_{st}$, represents the total conventional zero state time interval in one T_s), two horizontal switching devices in the H-bridge are ON while the other two are OFF. Also, the input side rectifier is forward biased. This means that the switches in the simplified circuit (Figure 5.6a) S_a and S_c are ON, while S_b is OFF, leading to the circuit shown in Figure 5.6d. Here, the voltage source and inductors charge the capacitors but no energy flows to the resonant network. The inductor voltage for this time interval is given as:

$$v_L = v_{DC} - V_C = |\hat{v}_{ac} \sin(\omega t)| - V_C. \quad (5.16)$$

To derive the expression for the shoot-through duty cycle, we will consider that the average voltage across the inductor ($\overline{v_L}$) over one switching cycle is zero at steady state. Therefore, by using (5.14), (5.15), and (5.16):

$$\overline{v_L} = 0 = \frac{T_{act}}{T_s} \left(\frac{|v_{ac}| - V_C}{2} \right) + \frac{T_{st}}{T_s} V_C + \frac{T_{zer}}{T_s} (|v_{ac}| - V_C), \quad (5.17)$$

where the switching cycle is defined as $T_s = T_{act} + T_{st} + T_{zer}$, the active state duty cycle is defined as $D_{act} = T_{act}/T_s$, and the shoot-through state duty cycle is defined as $D_{st} = T_{st}/T_s$. From [70], the ZSN capacitor voltage can be written as:

$$V_C = \frac{1-D_{st}}{1-2D_{st}} |v_{ac}|. \quad (5.18)$$

By substituting (5.18) in (5.17) the intermediate variable V_c can be eliminated, obtaining the following expression for the shoot-through duty cycle:

$$D_{st} = \frac{v_z - |v_{ac}|}{2v_z}. \quad (5.19)$$

The shoot-through duty cycle acts as another control variable to the system and is the one used for the PFC. Its control should always meet the equation $D_{act} + D_{st} + D_{zer} = 1$, where $D_{zer} = T_{zer}/T_s$ is the conventional zero state duty cycle.

5.3.2 Output Voltage/Power Regulation

An expression for the output voltage (V_o) in terms of the active and shoot-through state duty cycles (D_{act} and D_{st} respectively), and the AC input voltage (v_{ac}) is derived in this section by assuming that the system is ideal and operates in continuous conduction mode. Following these assumptions, the average power at the resonant network can be calculated based on Figure 5.7 as follows:

$$\overline{P_{res}}(t) = \frac{1}{T_s} \int_0^{T_s} v_H(\tau) i_{rp}(\tau) d\tau = \frac{2}{T_s} \int_{\frac{T_s}{4} - \frac{T_{act}(t)}{4}}^{\frac{T_s}{4} + \frac{T_{act}(t)}{4}} v_z(t) \hat{i}_{rp}(t) \sin(\omega_s \tau) d\tau, \quad (5.20)$$

where ω_s is the angular switching frequency, which is equal to the angular resonant frequency (ω_{res}) in this system, and $\hat{i}_{rp}$ is the peak value of the current flowing at the resonant network primary side. Changing the limits of integration in terms of the active state duty cycle, we have:

$$\overline{P_{res}}(t) = \frac{2}{T_s} \int_{\frac{T_s}{4} - \frac{D_{act}(t)T_s}{4}}^{\frac{T_s}{4} + \frac{D_{act}(t)T_s}{4}} v_z(t) \hat{i}_{rp}(t) \sin(\omega_s \tau) d\tau. \quad (5.21)$$

After integration, (5.21) becomes:

$$\overline{P_{res}}(t) = \frac{4v_z(t)\hat{i}_{rp}(t)}{T_s} \sin\left(\frac{D_{act}(t)\pi}{2}\right). \quad (5.22)$$

Assuming that the average value of the absolute value of the resonant network secondary side current ($|i_{rs}(t)|$) equals the output current (I_o), the instantaneous value of i_{rs} will be:

$$i_{rs}(t) = \frac{\pi I_o}{2} \sin(\omega_s t). \quad (5.23)$$

By transferring $i_{rs}(t)$ to the primary side, the expression for $\hat{i}_{rp}$ will be given as:

$$\hat{i}_{rp}(t) = \frac{\pi I_o}{2|k_{res}(\omega)|} = \frac{\pi V_o}{2|k_{res}(\omega)|R_o}, \quad (5.24)$$

where R_o is the system load, and the resonant gain factor (k_{res}) not only depends on the transformer turns ratio but also on the resonant network characteristics (which involves frequency). The way to obtain this factor will be discussed with details in the next sub section. An expression for v_z in terms of the shoot-through duty cycle can be obtained from (5.19), and is given as:

$$v_z = \frac{|v_{ac}(t)|}{1-2D_{st}(t)}. \quad (5.25)$$

Substituting (5.24) and (5.25) in (5.22):

$$\overline{P_{res}}(t) = \frac{V_o |v_{ac}(t)|}{|k_{res}(\omega)|R_o(1-2D_{st}(t))} \sin\left(\frac{D_{act}(t)\pi}{2}\right). \quad (5.26)$$

Since ideally the average power at the resonant network equals the instantaneous output power ($\overline{P_{res}}(t) = V_o(t)^2/R_o$), the expression for the instantaneous output voltage is given as:

$$V_o(t) = \frac{|v_{ac}(t)|}{|k_{res}(\omega)|(1-2D_{st}(t))} \sin\left(\frac{D_{act}(t)\pi}{2}\right). \quad (5.27)$$

Finally, the average output power is equal to the average of (5.26) over one fundamental period.

This is given as:

$$\overline{P_o}(v_{ac}, D_{st}, D_{act}) = \frac{1}{T} \int_0^T P_{res}(t) dt, \quad (5.28)$$

where T is the line period which is equal to $\frac{1}{60}$ s in this case. Similarly, the average output voltage is given as:

$$\overline{V_o}(v_{ac}, D_{st}, D_{act}) = \frac{1}{T} \int_0^T V_o(t) dt. \quad (5.29)$$

The equation (5.29) is the one used in the controller to regulate the output voltage. As can be seen in (5.28) and (5.29), the output power and consequently the output voltage can be

controlled by the shoot-through and active state duty cycles. For this system, the active state duty cycle is used to regulate the output voltage, while the shoot-through duty cycle will be in charge of the PFC. It is worth noticing that if the system is not operating in the continuous conduction mode, the equations derived in this section no longer hold. The derivation for discontinuous conduction mode is beyond the scope of this dissertation

5.3.2.1 Resonant gain factor derivation

The resonant gain factor can be obtained by using the resonant network simplified circuit shown in Figure 5.8. This circuit was obtained by transferring the impedances from the secondary to the primary side of the resonant network, and modeling the impedance seen from the left of the output rectifier as a resistor R_{orec} with voltage v_{orec} . The excitation to this equivalent circuit is the voltage at the H-bridge inverter right hand side, which is named as v_H . Also, N represents the transformer turns ratio (N_s/N_p), and the winding losses in the transformer have been modeled by the resistors R_p and R_s .

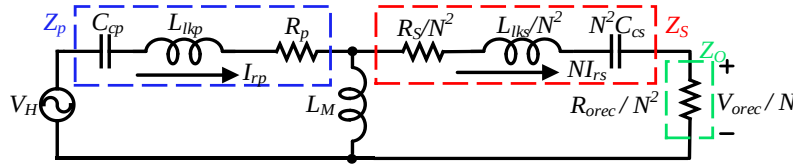


Figure 5.8 Simplified circuit of the resonant network.

The expression for R_{orec} can be obtained by assuming that only the fundamental component of v_{orec} is involved in the power transfer. This component is given by:

$$v_{orec,1}(t) = \frac{4V_o}{\pi} \sin(\omega_s t), \quad (5.30)$$

since the instantaneous waveform of v_{orec} is a square wave that equals to V_o when $\sin(\omega_s t)$ is positive, and to $-V_o$ when $\sin(\omega_s t)$ is negative. Then, the equivalent resistor is given as:

$$R_{orec} = \frac{v_{orec,1}(t)}{i_{rs}(t)} = \frac{\frac{4V_o}{\pi} \sin(\omega_s t)}{\frac{\pi I_o}{2} \sin(\omega_s t)} = \frac{8V_o}{\pi^2 I_o} = \frac{8}{\pi^2} R_o. \quad (5.31)$$

The previous simplified circuit can be analyzed in the frequency domain and, obtaining an expression for k_{res} as follows:

$$k_{res}(\omega) = \frac{I_{rs}}{I_{rp}} = \frac{\frac{1}{N} j\omega L_M}{j\omega L_M + Z_S + Z_o}. \quad (5.32)$$

As can be seen in (5.32), k_{res} is a frequency dependent variable. However, due to the band pass feature of the resonant network, only the resonant frequency is considered for this system, which means that $\omega = \omega_{res} = \omega_s$.

5.4 Simulation Results

Simulations of the proposed system have been performed at full load conditions (1kW) to validate the previous analysis. Table 5.1 shows the parameters and components values used for the simulations. The ZSN design was aimed at reducing the twice-line frequency ripple (2ω ripple) flowing through it, and was based on [72], [77]. On the other hand, the SRC design was based on [78], [79], specifically, the compensation capacitors were selected in such a way that the resonant frequency of the band pass filter equals the switching frequency. Switching frequencies for these systems range between 10 and 50 kHz [80]. In this research, 18.2kHz was selected.

Figure 5.9 shows the ZSRC simulation waveforms of the output voltage, AC input voltage and current. As can be seen, a high PF is achieved while the output voltage is regulated to 200 V dc as desired. Figure 5.10 shows the ZSRC simulation waveforms of the H-bridge output voltage and primary side resonant current. Notice that these waveforms agree with Figure 5.7, which was the base of the derivations made in the previous section. Also, Figure 5.11 shows for reference the ZSN capacitor and inductor voltage. It can be seen from the ZSN capacitor voltage waveform that the 2ω ripple is as small as desired.

Table 5.1 Simulation parameters and components value

Parameter	Value	Component	Value
Input voltage (v_{ac})	100V RMS	C_1, C_2	4.7mF
Line frequency	60Hz	L_1, L_2	1mH
Switching frequency	18.2kHz	C_{cp}	164nF
Resonant frequency	18.2kHz	L_{lkp}	0.4151mH
Output voltage (V_o)	200V	L_m	61.87 μ H
Input power	1kW	L_{lks}	1.072mH
Transformer turns ratio	15:20	C_{cs}	66nF
		R_o	40 Ω
		C_o	1mF

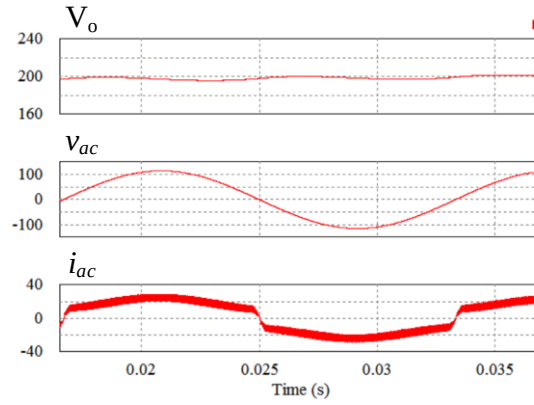


Figure 5.9 ZSRC simulation waveforms at full load versus time. From top to bottom: Output voltage (V), AC input voltage (V), and AC input current (A).

On the other hand, simulations for the primary and secondary charging pads (Figure 5.12) were performed to obtain a relationship between the unified coupling coefficient and misalignment (Figure 5.13). It can be seen from Figure 5.13 that as the center of the secondary side pad (which is located at the bottom of the EV) is aligned to the center of the primary side pad, the unified coupling coefficient is maximized. This is the case that achieves maximum power transfer efficiency between the two pads. As the EV is moved along the Z axis, the coupling factor will decrease along with the power transfer efficiency.

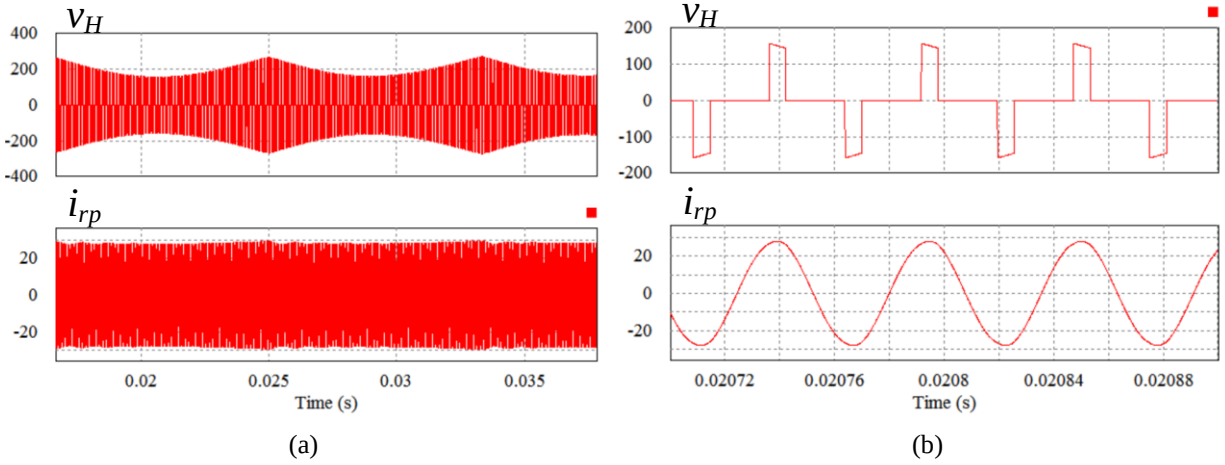


Figure 5.10 ZSRC simulation waveforms at full-load versus time: (a) complete waveform, (b) high-frequency component of (a). From top to bottom: H-bridge output voltage (V), and primary side resonant current (A).

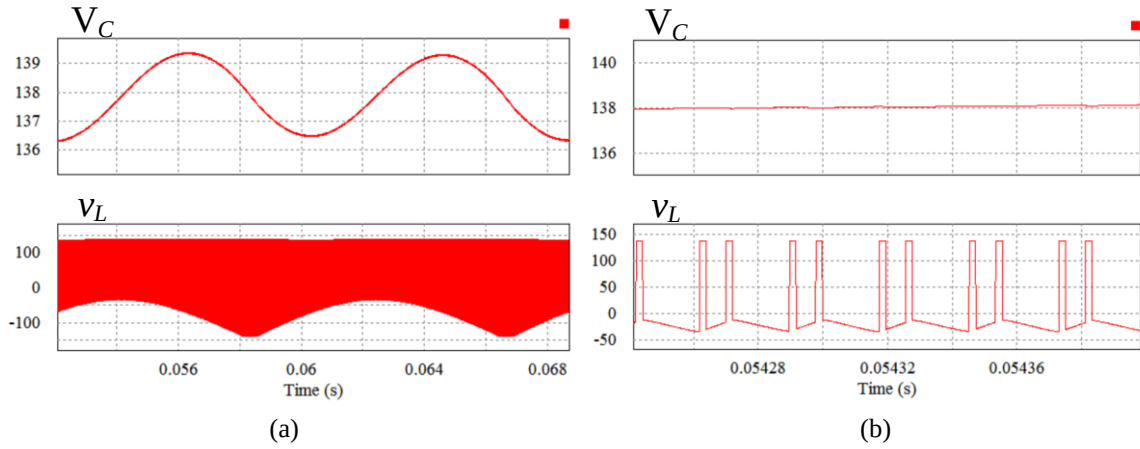


Figure 5.11 ZSRC simulation waveforms at full-load versus time: (a) complete waveform, (b) high-frequency component of (a). From top to bottom: ZSN capacitor voltage (V), and ZSN inductor voltage (V).

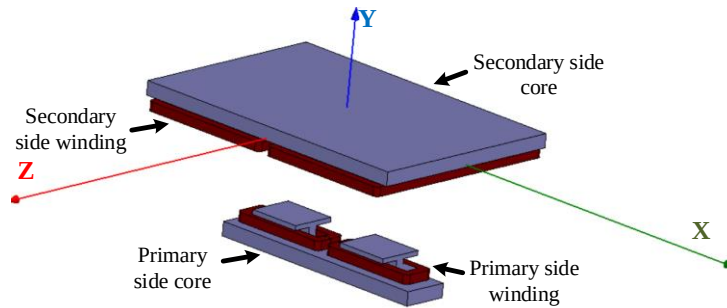


Figure 5.12 Charging pads simulation schematic.

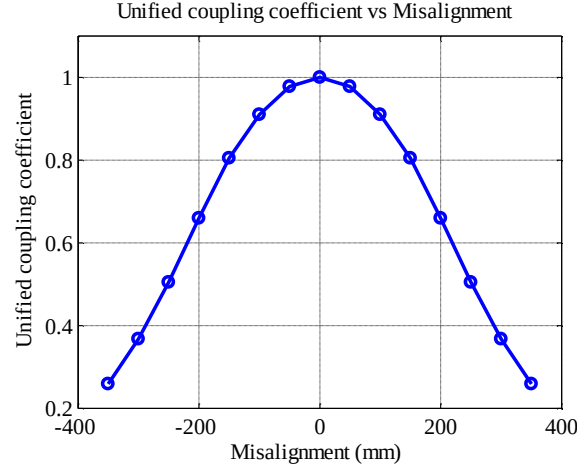


Figure 5.13 Relationship between the charging pads unified coupling coefficient and misalignment.

5.5 Experimental Results

Experiments have been performed to validate the previous simulations and analysis, and prove that the ZSRC-based WPT system inherently performs PFC while regulating the system output voltage. The ZSRC WPT system was based on a 1-kW prototype (Figure 5.14) with a 20-cm air gap between the converter's primary and secondary sides. The parameters used for the prototype are the same as the ones used for the simulations (Table 5.1). The transformer (see Figure 5.12) was made with a ferrite core, where the primary side has an I-shape structure and dimensions of 10cm by 60cm, and the secondary (pick up core) side has dimensions of 45cm by 60cm.

Figure 5.15 shows the control algorithm diagram used for the experimental results. As can be seen, three signals are fed to the controller, the AC input voltage (v_{ac}), the ZSN capacitor voltage (V_c), and the system output voltage (V_o). It is worth clarifying that V_c is used as one of the input signals to the controller since it is more stable compared to the ZSN output voltage (v_z). The expression that relates V_c and D_{st} can be obtained from (5.18).

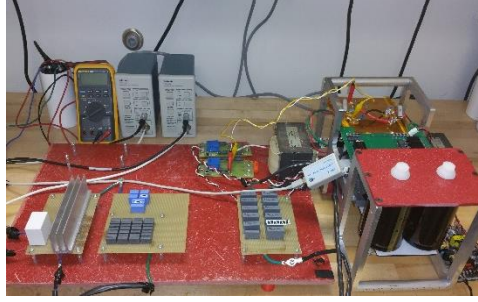


Figure 5.14 Prototype experimental setup: ZSRC primary and secondary side.

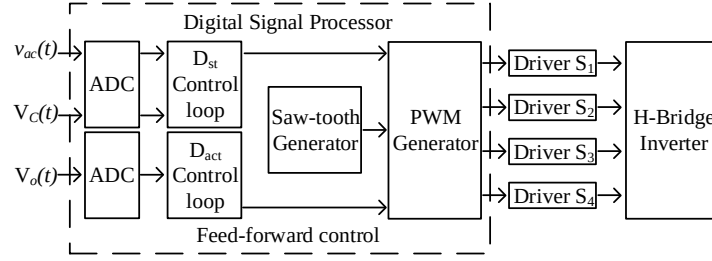


Figure 5.15 Control algorithm diagram.

The three signals are sampled at a rate of 18.2 kHz (same as the switching frequency). The signals v_{ac} and V_c are fed to the shoot-through duty cycle control loop, and V_o is fed to the active state duty cycle control loop. The D_{st} control loop uses (5.18) to calculate the shoot-through duty cycle that the H-bridge inverter switches need in order to perform the PFC, whereas the D_{act} control loop uses (5.29) to calculate the active state duty cycle needed to regulate the output voltage. The D_{st} and D_{act} command signals are then fed to the pulsed width modulated (PWM) generator that uses a logic comparing the D_{st} and D_{act} commands with a saw-tooth generator, to send the PWM signals (such the ones in Figure 5.7) to the H-bridge switches' drivers. The drivers make the switching action possible for the H-bridge semiconductor devices.

Only two operating points were tested: full and half load (1 kW and 500 W, respectively). For both cases, the grid voltage was 120 V rms, the ZSRC input voltage was softly tuned by a variable transformer (located between the grid side and the ZSRC) to be 100 V rms, while the system output voltage was regulated to 200 V dc. Figure 5.16a and Figure 5.16b shows the ZSRC experimental waveforms of the grid side input voltage and current at full and half loads,

respectively. It is worth mentioning that the voltage waveforms were measured by a Tektronix high voltage differential probe under the 50x attenuation factor, while the probe attenuation factor on the scope was 100x. Also, a digital power meter was used to measure the phase shift between the grid voltage and current fundamental component, as well as the RMS values of the current harmonics contained in the grid side, for both load conditions. With these measurements, the following parameters were calculated: PF displacement factor, grid current THD, PF distortion factor, and true PF. A summary of these calculations is shown in Table 5.2.

In addition, Figure 5.17 shows the grid-side current harmonics (for full and half load) normalized under the IEC 61000-3-2 Class A harmonic limitation standard. As can be seen, during full load only the 3rd, 33, 35, 37, and 39 harmonics met the standard, whereas for half load, only the 29, 33, 35, 37, and 39 harmonics met the standard. The general reason the standard was not met could be due to control problems, but further investigation is being performed. However, the harmonic components that do not meet the standard are just less than twice the limit. Finally, although for this power level a conventional PFC should meet the standards, the results obtained still support the hypothesis that the ZSN can be used to perform PFC and system output power in a single stage, which is the main concept in this dissertation. One way to actually improve the PF is to use a modified version of the Z-source, where the input current is continuous (e.g., Quasi-Z-source), which in fact very recently this was done [74].

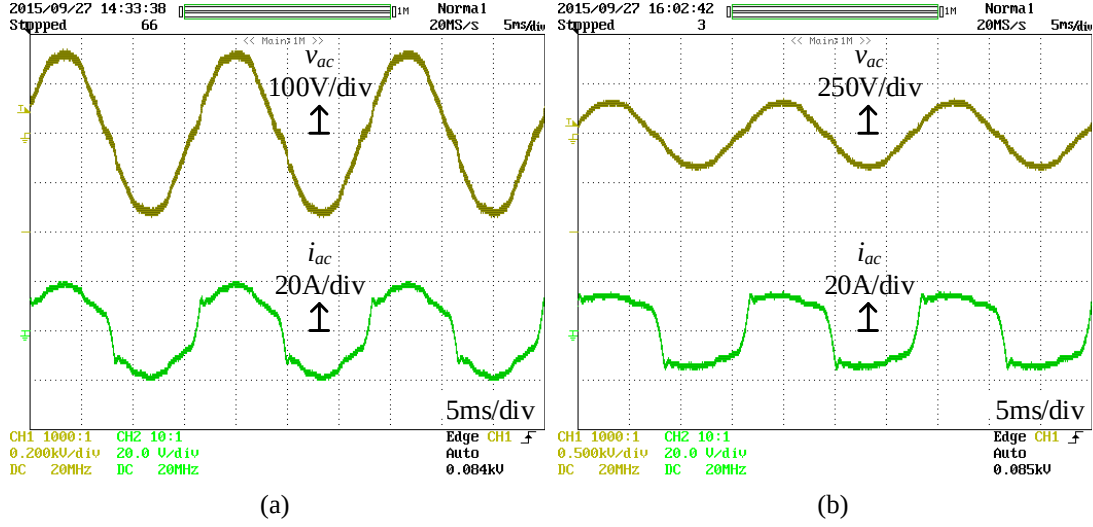


Figure 5.16 ZSRC experimental waveforms versus time: (a) full-load, (b) half-load. From top to bottom: AC input voltage (V), and AC input current (A).

Table 5.2 Experimental results summary

	Full load (1 kW)	Half load (500 W)
$\theta_{vac} - \theta_{iac}$	2.22°	4.43°
PF displacement factor	0.999	0.997
Grid current THD	15.67%	29.3%
PF distortion factor	0.988	0.960
True PF	0.987	0.957

Other key waveforms are shown in Figure 5.18. These figures show the H-bridge output voltage (v_H) and the current at the resonant network primary side (i_{rp}) for the full load condition. Notice that all experimental results are quite consistent with the simulation results shown in the previous section.

A break up of losses based on theoretical calculations is summarized in Figure 5.19. From there it can be seen that the winding losses are dominant, and this is because Litz wire was not used for the transformer's secondary. In an actual implementation Litz wire will be used which will definitely help improve the overall system efficiency. The next significant losses are the switching losses and this is because old Si-based IGBT was used, and the output voltage regulation method used for this prototype varies the active state duty cycle which leads to hard switching. Based on these losses, the proposed system achieved an efficiency of 72.1% at full load.

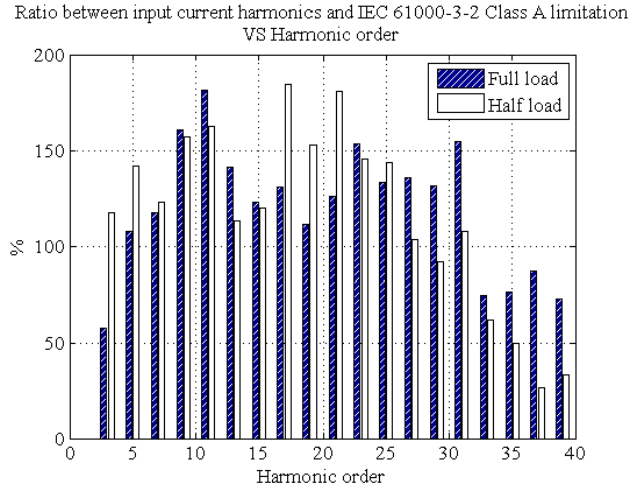


Figure 5.17 Normalized grid-side current harmonics.

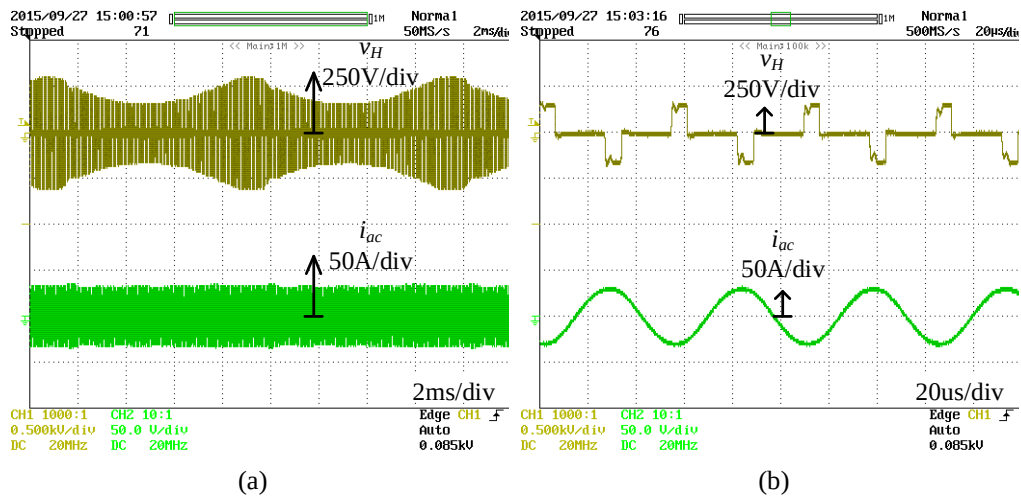


Figure 5.18 ZSRC experimental waveforms versus time at full-load: (a) complete waveform, (b) high-frequency component of (a). From top to bottom: H-bridge output voltage (V), and primary side resonant current (A).

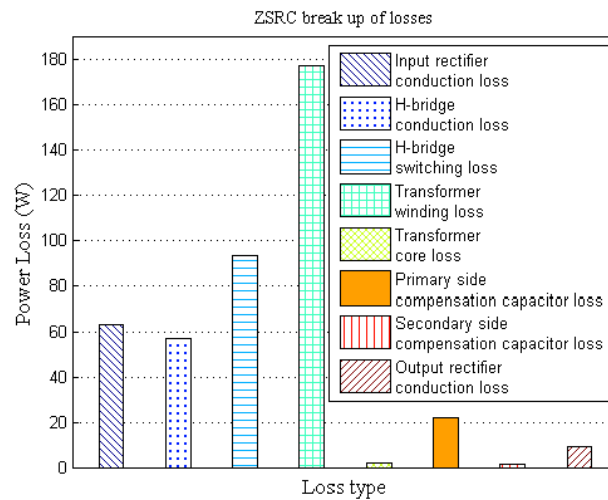


Figure 5.19 ZSRC break up of losses.

5.6 Summary

In this chapter, a Z-source-based wireless charger was proposed. Because of the ZSN, the ZSRC is immune to shoot-through states, which not only increases system reliability but adds one extra control variable (shoot-through state duty cycle) that can be used to perform PFC. This variable is encrusted in the SRC H-bridge inverter, and this is the reason why the ZSRC can realize the PFC and regulate the system output voltage/power in a single stage. In this chapter, the proposed ZSN-based charger was analyzed and compared to the conventional boost-converter-based charger. In summary, compared to the conventional boost PFC converter, the ZSN: has better performance for boost ratios between 1 and 1.34; does not requires additional semiconductor devices and control circuitry to perform the PFC; increases the charger reliability by being immune to random EMI shoot-through states; has a longer lifetime; and can be designed so as to be smaller and cheaper.

This dissertation validated the theoretical analysis by means of simulations and experimental results based on two operating points: full and half load. The proposed single stage PFC converter system achieved a PF of 0.987 at the full load condition while regulating the system output voltage to 200V. The experimental results were based on a 1-kW prototype with a 20-cm air gap between the converter primary and secondary side. These results were consistent with the simulations.

Chapter 6 Conclusions

This dissertation provided multiple solutions so as to improve plug-in and wireless chargers. The solutions address crucial features in these chargers such as: efficiency, size, cost, and reliability. The specific conclusions for each chapter are detailed below.

6.1 Chapter 2

Chapter 2 presented the proposal of a delta-connected CMI-based XFC station with an active charging-port configuration. The plug-in station is capable of charging multiple types of EVs while keeping balanced three-phase utility currents with unity power factor. The control system for the XFC station was discussed in details and validated through simulations results.

The main novelty of the proposed station relies on the charging-port configuration, which adapts depending on the EV type that is connected to the station. It was shown through theoretical analysis that by implementing such CPC the station achieves 40%-66.7% less power rating (thus, is cheaper and smaller) compared the one using the conventional CPCs and the same NoP. However, the proposed CPC sacrifices in the number of CSs the station can handle. In order to compensate for this, its NoP can be increased. It was shown that even when a station using CPC_P has higher NoP than one using the conventional CPC, it achieves similar or less power rating with more or similar CSs.

Due to the tradeoff between CSs and power rating, the benefit magnitude of using CPC_P depends on the needs of the desired station. Nevertheless, there is one feature that the proposed CPC has that is not possible with the conventional counterpart. This is the ability to parallel all (or the necessary) CP to charge L_{EV} with P_{demand} that may be too large to charge within ten minutes with a single charging-port (as with conventional CPC) or with three in parallel (as with the

proposed CPC). To better illustrate this, suppose that a L_{EV} with battery capacity of 1MWh is demanding full-load power to be charged within ten minutes. This can in theory be accomplished by using fifteen 400kW-CPs in parallel, something possible in a station with $NoP \geq 15$ and the proposed CPC. However, as it was explained in section 2.4, the complexity of its realization increases and is something that need to be considered. In addition to the aforementioned advantage, CPC_P promises to be more efficient since it makes better utilization of the PECs in the station. Specifically, any EV type demanding full-load power will inherently represent full-load condition for the PECs, while they may represent light- or mid-load condition (where the efficiency is typically degraded) for its PECs if the station was using the conventional CPCs.

It is worth mentioning that the proposed CPC can be implemented in other XFC topologies and is not limited to just the presented delta-connected CMI. Moreover, it was explained in terms of charging S_{EV} , M_{EV} , or L_{EV} , however, it can be done in terms of P_{demand} . Specifically, when assuming “ P_x ”, “ P_y ”, and “ P_z ” to be desired power quantities (which are equal to 400kW, 800kW, and 1.2MW, respectively, in this chapter), a CP is used for $P_{demand} \leq P_x$, two are used in parallel for $P_x < P_{demand} \leq P_y$, and three are used in parallel for $P_y < P_{demand} \leq P_z$. Stations with more than one unit in parallel (or with more than three CPs) can further charge EVs with $P_{demand} > P_z$ within ten minutes by paralleling more than three CPs.

Finally, although improvements in XFC stations represent a step forward mass adaptation of EVs, its implementation is still a challenge since current battery technology may not accept the high charging rate, and because even a highly-efficient charger will require the removal of high amounts of heat [1]. Also, it is worth mentioning that these stations are not limited to the plug-in technology, but can be applied wirelessly in the future as well.

6.2 Chapter 3

Chapter 3 presented the proposal of an online control strategy to reduce the core loss of the HFTxs in the XFC station presented on Chapter 2. This is done by reducing and/or clamping the HFTx's flux linkage while still supplying a desired power to the load. Theoretical analysis was validated with simulation results (based on Maxwell and LTspice) for a case study that uses an 8kW DAB controlled under single phase-shift. It was shown that the core loss can be reduced by around 50% at light load while by around 80% at full load when compared to not applying the proposed control strategy in the presented case study.

Although this dissertation focused on proving the concept and its usefulness in a DAB controlled under regular phase shift, the proposed method can be replicable in any converter that has enough freedom so as to control its power flow while applying a desired voltage across its HFTx's magnetizing inductance. DAB itself has many ways to do this, and it is worth mentioning that when this converter is controlled under dual and triple phase-shift, the same equation (3.5) is expected to hold true. However, for the case of triple phase-shift not only (3.5) can be used to insert zero states in the magnetizing inductance, but aligning the zero states in V_{Tx1} and V_{Tx2} achieves this as well, as it can be seen in (3.1). The more alignment in the zero states of V_{Tx1} and V_{Tx2} , the more core loss reduction is expected. Because there is more opportunity to insert zero states in v_{Lm} when using triple phase-shift, this control is expected to achieve the highest core loss reduction in a DAB. This control also have more flexibility in the way the proposed core loss reduction concept can be implemented since (3.5) does not really need to hold in the case of triple phase-shift as long as some zero states of V_{Tx1} and V_{Tx2} are aligned with each other.

It is worth mentioning that, since the core loss reduction method works while the converter is under operation, it can be applied into systems that are already built by modifying their control

strategy, something that may be too difficult or impossible to do with traditional core loss reduction methods. However, it can still be taken into consideration as part of the design stage of the system so as to build a transformer as small as possible without much sacrifice in its core loss (since any increase in flux density can be overcome later with the proposed control strategy).

Finally, dealing with transformer core loss is imperative especially in XFC stations, since due to the many cells these losses will be multiplied, specifically by 150 times in the proposed station. Therefore, the proposed solution is very meaningful to keep high efficiency in the system.

6.3 Chapter 4

Chapter 4 presented the proposal of a general equation for C_{dc} , which included the effect of the RN characteristics and the system's control variables. As opposed to the conventional equation, the proposed one avoids oversizing and reliability issues. The equation was validated with simulations based on the SS RN, and can be used to obtain the optimum dc-link capacitance for a wide load range by inspection or by running an optimization algorithm. It was found by inspection that the minimum C_{dc} needed to keep a desired $\Delta\tilde{v}_{cdc}$ at the dc-link for the SS can be obtained at the system rated power. The same C_{dc} can be used for the SP RN, however, there will be a difference in the system control and performance between the two topologies. For a more accurate value of the optimum C_{dc} , the resonant network model should be developed as accurate as possible. A way to do this is by considering higher order harmonics and not only the fundamental when deriving the expression for $\hat{i}_{rp}$. The analysis performed in this dissertation can be applied to any RN topology, thus, it provides an aid in the design process of EVs wireless chargers.

6.4 Chapter 5

Finally, Chapter 5 presented the proposal of a Z-source-based wireless charger. Because of the ZSN, the ZSRC is immune to shoot-through states, which not only increases system reliability but adds one extra control variable (shoot-through state duty cycle) that can be used to perform PFC. This variable is encrusted in the SRC H-bridge inverter, and this is the reason why the ZSRC can realize the PFC and regulate the system output voltage single stage; thus, eliminating the inherent size, cost and loss associated with the semiconductor devices need in the conventional two-stage charger. Also, a top-level comparison between the conventional and the proposed charger was made. In summary, compared to the conventional boost PFC converter, the ZSN: has better performance for boost ratios between 1 and 1.34; does not requires additional semiconductor devices and control circuitry to perform the PFC; increases the charger reliability by being immune to random EMI shoot-through states; has a longer lifetime.

The dissertation validated the theoretical analysis by means of simulations and experimental results based on two operating points: full and half loads. The proposed single stage PFC converter system achieved a PF of 0.987 at the full load condition while regulating the system output voltage to 200V. The experimental results were based on a 1-kW prototype with a 20-cm air gap between the converter primary and secondary side. These results were consistent with the simulations.

Chapter 7 Future Work

The proposed solutions in this dissertation provides a good foundation of work, but either improvements to them or additional validation can be done. The following sections describe possible work/ideas that can be done by other researchers for each chapter.

7.1 Chapter 2

The proposed XFC station top-level operation (control of the grid-side H-bridge) was validated through simulations in this dissertation; but simulation inside each cell was not done since they have nothing to do with achieving balanced utility currents and unity power factor, and they were not necessary to validate the active CPC idea. To make this work more complete, the following details must be addressed: 1) the full-system simulation, including balancing the cell voltages, as well as the power flow control in each of the DABs; 2) experimental validation, which can be challenging since access to the medium voltage grid is needed.

An idea to make the CPC study better is also described. It was shown that the implementation of the proposed CPC is challenging, and becomes even more as the number of ports increases (since six additional switches are needed per charging port). But, having more charging ports (or more charging units in parallel) can accommodate for charging even bigger EVs (>200kWh) within 10 minutes as well as more charging scenarios—a unique and attractive feature since this will not be practical (or possible) to do with the conventional CPC. It will be interesting to do a study on finding the break-even point of when (at how many number of ports) the cost and size reduced on the PECs with the proposed CPC starts to be outweigh by the increase in number of switches (and associated complexity) to achieve the reconfiguration. The study, should be made by taking into consideration the possibility of reducing the switches needed for the realization by

half (i.e., three switches per charging ports in a three-port station) by making all charging ports share the same ground.

7.2 Chapter 3

The proposed method to reduce core loss in HFTx was validated with a DAB controlled under single phase-shift by using simulation results. Although this validation was done with well-trusted simulators (ANSOFT Maxwell and LTspice), experimental results are needed to provide the final validation. Interesting studies to do with the proposed idea are as follows:

- 1) Compare which how much core loss can be reduced using other common controls for DAB, such as dual phase-shift, and triple phase-shift. As it was mentioned in the conclusion section, the triple phase-shift is expected to achieve the highest core loss reduction since it has more flexibility to insert zero states in the voltage across the transformer's magnetizing inductance.
- 2) As mentioned in the conclusion section, the proposed core loss reduction method is expected to help even if the transformer is designed for high efficiency, where the transformer power density is sacrificed. It will be interesting to compare the losses and power density achieved in a transformer that was designed for high efficiency while taking into account during the design stage that the proposed control strategy was going to be used while the converter operates. It is expected that the transformer designed with the proposed control strategy in mind will have higher power density while having the same efficiency as one just optimized for high efficiency with the traditional methods.

7.3 Chapter 4

The proposed equation to size the dc-link capacitor in conventional EV wireless chargers was derived by using the fundamental frequency approximation. Although a good matching between simulation and theoretical results was achieved, higher-order harmonics should be considered if a more accurate results is desired. Also, the equation was validated with a well-trusted simulation tool (PSim). However, experimental results are needed to provide the final validation. Interesting studies to do with the proposed equation are as follows:

- 1) Make a comparison between the different types of resonant networks (series-series, series-parallel, LCC, etc) to determine which one will require the least amount of capacitance for a given system and performance requirement.
- 2) The basic idea of how to derive this equation was detailed in this dissertation, thus, it can be expanded for parallel-primary topologies (e.g., parallel-series, parallel-parallel, CCL, etc), so as to reliably size their dc-link inductance. A study such as the one mentioned above can be done for these types of topologies as well, so as to determine which one require the least amount of dc-link inductance for a given system and performance requirement.
- 3) As it was mentioned in the chapter, the minimum dc-link capacitance was obtained by inspection for the series-series topology at the nominal state. However, this could not be replicated in the series-parallel topology, and although in theory the same dc-link capacitance can be used in both resonant networks, there will be a difference in the system control and performance between them. It will be interesting to develop an algorithm that provides the minimum capacitance needed for a desired system

performance, especially for the topologies that don't have the luxury of obtain this capacitance by inspection.

7.4 Chapter 5

The system's operation of the proposed Z-source-based wireless charger was experimentally validated but, its overall efficiency was low and in fact, do not meet the standards ($>85\%$). As it was shown in the chapter, the most dominant loss was due to the transformer's windings, which was something to be expected as no Litz wire was used in its secondary side. The next dominant loss was due to switching of the inverter, where Si-IGBTs were used. In addition, the switching frequency of the system (18.2kHz) do not meets the standards (85kHz). For a more realistic system implementation, and expected dramatical increase in the system's overall efficiency the following has to be done: 1) use the required 85kHz switching frequency and wide band-gap devices; 2) use Litz wire for the transformer windings.

Although the proposed wireless chargers achieve unity power factor and output power regulation in a single stage by using the Z-source, the exact same strategy can be implemented with any of the Z-source derivatives (i.e., quasi Z-source, trans Z-source, etc). It will be interesting to do a study which compares all Z-source derivatives in terms of: achievable power factor, efficiency, size, cost; to see which one will be the best candidate for the wireless charger application.

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