MULTI-BAND RECONFIGURABLE RFICS IN SI-BASED TECHNOLOGIES FOR A COMPACT AND ADAPTIVE RF FRONT-END

By

Asad Ali Nawaz

A DISSERTATION

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

Electrical Engineering — Doctor of Philosophy

2020

ABSTRACT

MULTI-BAND RECONFIGURABLE RFICS IN SI-BASED TECHNOLOGIES FOR A COMPACT AND ADAPTIVE RF FRONT-END

By

Asad Ali Nawaz

Recent advances in the wireless communication market have led to the coexistence of several networks such as cellular network, personal area network (PAN), wireless local area network (WLAN), etc. along with several different air interfaces (802.11a, 802.11g, Bluetooth, wireless code division multiple access (WCDMA), etc.). Thus, all the wireless devices need to be compatible with the different communication standards while still keeping similar performance, smaller die area and lower power consumption. The need to enable the "global roaming'' capability between a wide variety of networks operating at different frequencies calls for the development of reconfigurable radio-frequency integrated circuits (RFICs) which can achieve maximum hardware sharing between different standards and across various functions. The objective of this dissertation is to present novel topologies for RF components and blocks that can yield a Si-based frequency-agile RF front-end. The targeted applications for this work are 5G multi-band wireless communication and reconfigurable short/long range phased arrays for automobile radars. However, the concept of the proposed reconfigurable RF elements is generic in nature and can be applied to all emerging applications which require on-chip reconfigurability at microwave and mm-wave frequencies.

To demonstrate the concept of a reconfigurable RF front end, a Ka/V band-switchable TRX amplifier is developed in 0.13um BiCMOS SiGe process and a 18-50 GHz receiver is developed in 45nm SOI CMOS process. Unlike the traditional approach for a multi-band radio – where the dedicated single band transceivers composed of fixed RF components are designed and

multiplexed with the help of switches – the proposed idea utilizes the switches inside each RF block; thus, adding the reconfigurability inside each block and eliminating the need for separate front-ends. However, the catch in the latter approach is to maintain the RF performance while still being able to save the real-estate and power consumption. The proposed Ka/V band-switchable TRX amplifier consists of a band-switchable LNA, a band-switchable PA, and integrated T/R switches which saves a lot of area. The band-switch functionality is realized using thin-film microstrip based shunt stubs with reverse saturated SiGe switches. Design techniques for switch loss reduction and size miniaturizations are presented. This work illustrates that with the optimization of switch loss, appropriate selection of each block between wideband or band-switching topology and co-design of RF blocks, a highly integrated multi-band transceiver can be designed with the minimal degradation to the RF performance compared to state-of-the-art dedicated single band transceivers. To further explore reconfigurable transceivers, a direct quadrature down-conversion mixer first receiver with active channel select filters has been designed. The receiver supports 200MHz instantaneous RF bandwidth and can be reconfigured to receive any 200 MHz channel within 18-50 GHz frequency range. With the ever-evolving wireless standards like 4G/5G/6G, equipment manufacturers are required to add more functionality into the chips while still maintaining the backward compatibility with previous standards or fallback option to lower frequency bands. A low power, highly integrated, multi-band and multi-standard chipset has thus become a requisite in commercial products. The proposed concept of in-block reconfigurability and the presented design techniques to realize mm-wave frequency reconfigurable transceivers have a huge potential in this regard.

ACKNOWLEDGEMENTS

I am most indebted to my parents, Samina and Nawaz, who not only just supported me throughout this intellectual journey but also instilled in me a sense of rightness, a sense of purpose, and a sense of greater good. This would never have been possible without their prayers and blessings of Almighty Allah.

I am thankful to my undergrad advisor, Dr. Inam Elahi Rana, for introducing me to the microwave circuit design and inspiring me to pursue this path. I am extremely thankful to my advisor, Dr. Ahmet Cagri Ulusoy. If I know anything about IC design today, I owe it to him. He took me in his group despite my rudimentary knowledge of circuits and absolutely no experience in IC design. He would come to lab, sit down with me and allow me to ask anything about the subject no matter how basic or foolish questions I had. We did a lot of tape-outs and some did not work as expected. He was never harsh on me and always encouraged me to look at the bright side and to learn from my mistakes. He made me capable of carrying out research independently. I would also like to thank Dr. John Albrecht. Had he not been there, my admission to MSU would not have been possible. When all the doors at MSU closed at me, he opened one. He put me in contact with Dr. Ulusoy and arranged everything for me. He has also been a great support to me after Dr. Ulusoy left MSU. I found him as a person who would go an extra mile to help. I would also like to thank my committee members (Dr. Sangmin Yoo, Dr. Yuying Xie and Dr. John Papapolymerou) for guiding me throughout my PhD.

I am also grateful to my friends at MSU. I am fortunate to have met with wonderful colleagues: Siwook, Ibrahim, Shih-Chang, Jubaid, Xenophon and Adamantia. There have been times when I was happy and there have been times when I was sad. Siwook and Ibrahim always

stood by me. We have shared countless discussions over the cup of coffee and made gigabytes of cherish-able memories. I have also learnt a lot about IC design from Siwook and he has helped me many times in debugging a circuit. I am also thankful to my Pakistani friends at MSU. They saved me from getting bored when I was not busy at work. They helped me in getting adjusted at MSU and were always there when needed.

Last but not the least, I am extremely grateful to my wife, Sidra. I have spent innumerable weekends and pulled a couple all-nighters at lab. She has been very patient and given me all the time I needed to finish this thesis. She has been with me through thick and thin and inspired me in many ways. I would not be where I am today if it was not for your support, Sidra.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

KEY TO ABBREVIATIONS

PA	Power Amplifier
TMN	Tunable Matching Network
LNA	Low Noise Amplifier
SiGe	Silicon-Germanium
CMOS	Complementary Metal-Oxide Semiconductor
GSG	Ground-Signal-Ground
GSSG	Ground-Signal-Signal-Ground
IC	Integrated Circuit
NMOS	N-Channel Metal Oxide Semiconductor Field Effect Transistor
PMOS	P-Channel Metal Oxide Semiconductor Field Effect Transistor
Q-factor	Quality Factor
RF	Radio Frequency
λ	Wavelength [m]
f_{max}	Maximum Oscillation Frequency
f_{τ}	Transit Frequency
RX	Receiver
TX	Transmitter
TRX	Transceiver
DSB	Double sideband

in	Input
out	Output
max	Maximum
Th	Threshold
L	Load
min	Minimum

1 INTRODUCTION

1.1 Wireless Communication and Frequency Bands

Although clearly worlds apart from today's technologies, the true definition of wireless communications can reach all the way back to the times past when humans used smoke signals and carrier pigeons to communicate wirelessly. In today's world, wireless communication is defined as transmission of information between two or more points using radio waves. The very first use of radio transmitted coded information was a result of the works of Maxwell and Hertz with their pioneering experiments using electromagnetic waves and the term "radio" was incepted after Marconi demonstrated long-range communication over the air without needing any wires. Radio technologies continued development for over a hundred years as people began to unravel the intricacies of wireless communications. This resulted in highly categorized frequency bands and respective applications. Some of the applications include AM and FM radio transmission (153 kHz to 108 MHz), radio frequency identification (RFID) (120 to 150 kHz 13.56 MHz, 433 MHz, 3.1 to 10 GHz), global positioning system (GPS 1-2 GHz), cellular communication (800 MHz, 2.4 GHz), 5G cellular communication (28 and 38 GHz), Wi-Fi (2.4 GHz, 5 GHz, 60 GHz in future), satellite communication (4- 6 GHz) , military radar systems (8-12 GHz), digital satellite television (11-13 GHz), WPAN (60 GHz), automobile collision avoidance radars (24 GHz, 77 GHz), microwave back haul communication (6, 11, 18, 23 38 GHz, 71 to 77 GHz, 81 to 86 GHz), mm-wave body scanning and imaging (94 GHz), chip-to-chip communication (80 GHz and above), high resolution medical imaging (122 GHz,140 GHz and above), radio astronomy(ALMA project), short-distance high speed communication (300 GHz and above) and terahertz medical applications [1]. Some of the above-mentioned wireless systems have matured over the years and have been

commercialized, but some systems, especially mm-wave systems, are still in the research domain. A snapshot of some of the wireless technologies in operation is shown in Figure 1-1.

1.2 Motivation for Multi-Band Radio

Recent advances in the wireless communication market have led to the coexistence of several networks such as cellular network, personal area network (PAN), wireless local area network (WLAN), etc. along with several different air interfaces (802.11a, 802.11g, Bluetooth, wireless code division multiple access (WCDMA), etc.). Thus, the wireless devices need to be compatible with the different communication standards while still keeping similar performance, smaller die area and lower power consumption. The technology of the wireless devices also needs to allow for

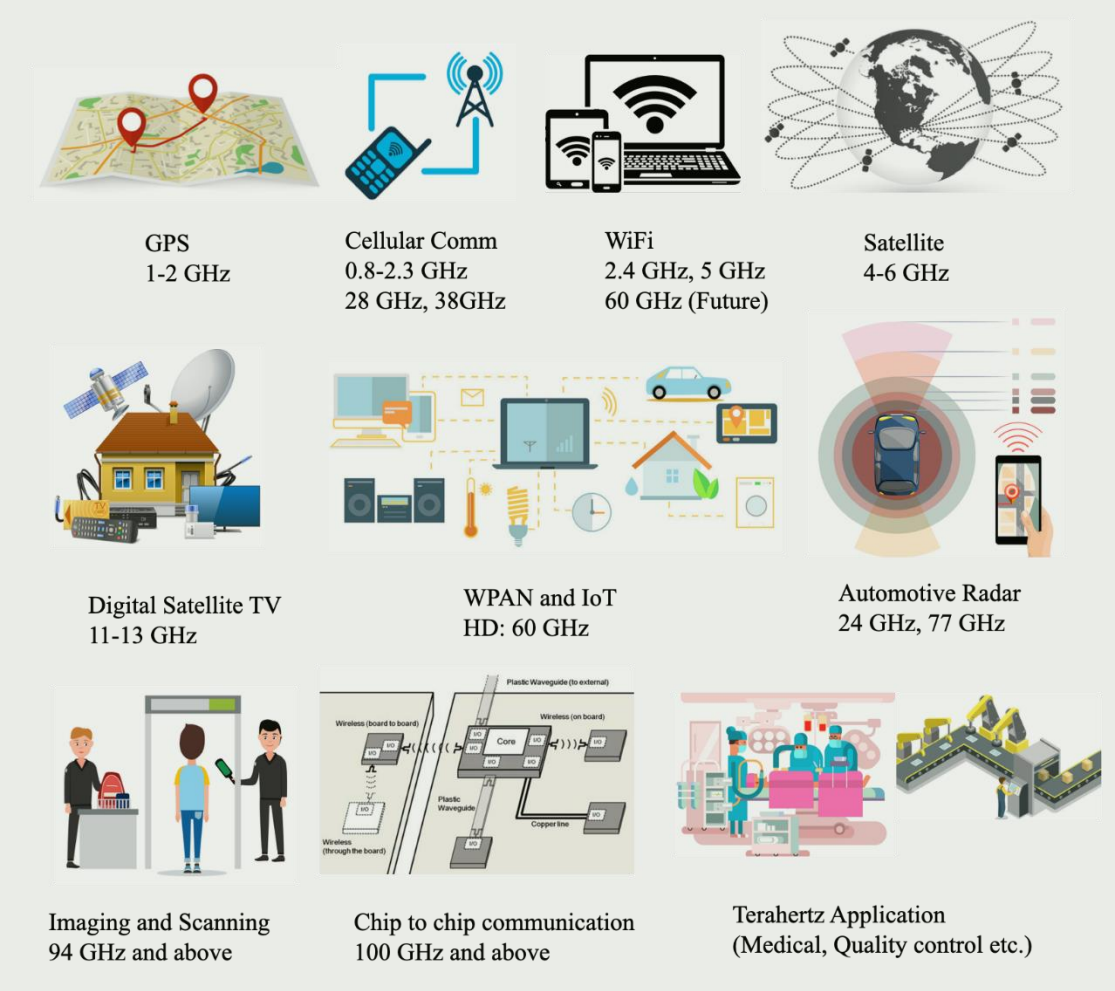


Figure 1-1 Wireless Technologies and Applications in Operation

a smooth migration to future generations of communication standards with higher data rates. The need to enable the "global roaming'' capability between a wide variety of networks operating at different frequencies calls for the development of compact and reconfigurable radio-frequency integrated circuits (RFICs) which can achieve maximum hardware sharing between different standards and across various functions. Such a compact RF front-end would require re-configurable RF blocks rather than switched radio architectures [2].

Most of the emerging wireless applications today, be it IoT (internet of things) devices, the 5G/6G communication system, the self-driving autonomous cars or land mobile communication in general, they all benefit from having a reconfigurable hardware integrated into them. Figure 1-2 shows some of the trending wireless applications which require some sort of RF hardware reconfigurability.

To emphasize the importance of reconfigurable RF hardware, a cellular phone example can be taken. The first (1G) and second generations (2G) of cellular network use GSM signals which are operated over 800/1900 MHz in Asia, Africa and Europe whereas 850/1900 MHz frequencies are used in Americas. The third generation (3G) employs UTMS system which require 1900/2100

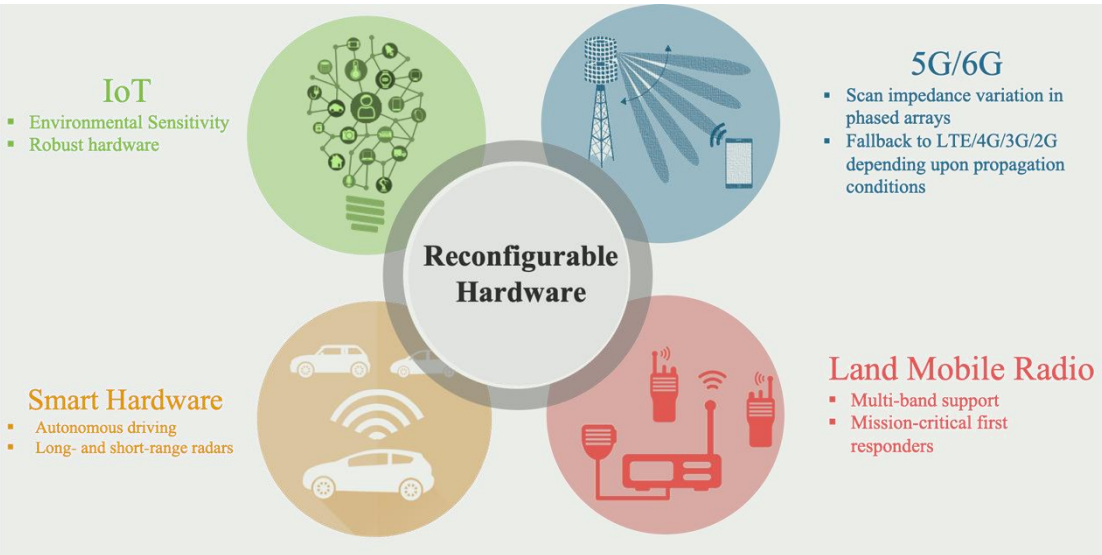
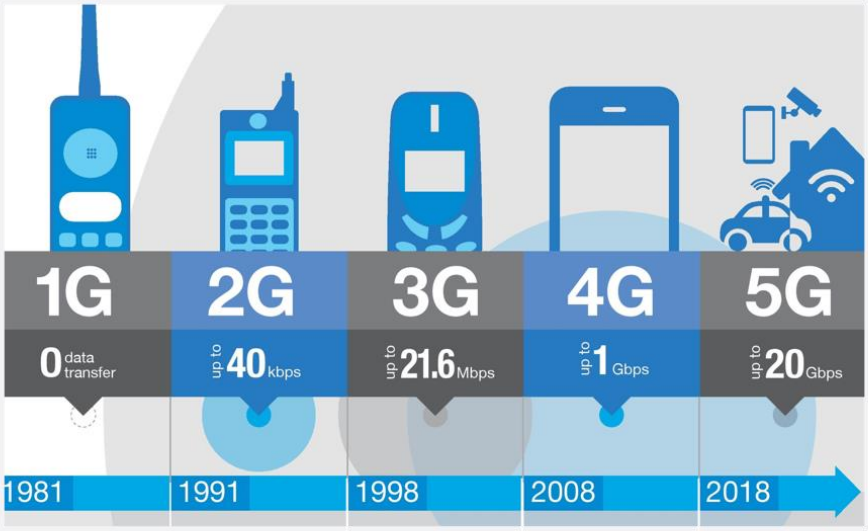


Figure 1-2 Emerging Wireless Application Requiring RF Hardware Reconfigurability

MHz band along with 600/700/1700 MHz bands in some countries. With the introduction fourth generation (4G) in cellular network, more than 80 LTE bands were added which supported frequencies starting from 400MHz-6000MHz range. The fifth generation (5G) now adds milli-meter wave bands extending from 24-40 GHz to the cellular network. Therefore, today's cellphone would at least require 6 frequency bands (800 MHz, 1900 MHz, 2100 MHz, 3500 MHz, 28 GHz, 39 GHz) in order to be compatible with all the generations of cellular network, at least in one part of the world. Figure 1-3 illustrates the most popular frequencies bands deployed in the world for different cellular generations [3].



GSM Bands	3G Bands	LTE Bands	5G Bands
800 MHz	1700 MHz	600 MHz	1900 MHz
850 MHz	1900 MHz	700 MHz	2100 MHz
1900 MHz	2100 MHz	800 MHz	2600 MHz
		900 MHz	3500 MHz
		1700 MHz	3700 MHz
		1800 MHz	4700 MHz
		1900 MHz	24.25-27.5 GHz
		2100 MHz	27.5-28.35 GHz
		2300 MHz	37-40 GHz
		2600 MHz	

Figure 1-3 Frequency Bands Required by A Multi-band Cellphone to be Compatible with all the Generations of Cellular Network (1G-5G)

1.3 Challenges in Milli-meter Wave Multi-Band Radio

The specifications placed on the reconfigurable RF element depends upon the RF block being designed. However, some common factors are:

1. Frequency tuning range and selectivity
2. Signal loss and DC power dissipation associated with tuning mechanism
3. Noise and Linearity degradation

An ideal reconfigurable element should be able to reconfigure to any frequency, provide zero loss and should not affect the linearity of the circuit. However, the available tunable components (e.g., varactor diodes) from the PDK have small tuning ratio, low-Q and large signal capacitance variation. Since these parameters are process dependents, therefore the achievable frequency tuning ratio and other metrics vary from process to process.

1.4 Existing Techniques for Multi-Band Radios

Some of the popular techniques for reconfigurable or multi-band RFICs are as follows:

1. Switched-radio using SPDT switches [4]
2. Tunable inductors or varactors [5]
3. Resonant LC tanks [6]
4. MEMS based switches in matching network [7]
5. Variable delay transmission lines [8]
6. Switched feedback and output load [9]
7. Tunable stubs using transistor switches [10]

Switched-radio approach uses individual transceivers with dedicated frequency bands and a wideband SPNT switch at input and output to shift between different frequencies. This increases

the IC area N times and becomes unacceptable method for mm-wave phased arrays which require tight element spacing. Therefore, it is not extensively employed. Tunable inductors or capacitors suffer from low tuning range and low-Q; these techniques are used when narrowband tuning is required. Resonant LC-tank is the popular approach for dual/tri band transceiver designs. However, this approach is sensitive to the LC product and variation in resonance frequency is observed from sample to sample. Also, after certain point, it becomes impractical to have more than two or three LC tanks connected at the same node in the layout. Therefore, this approach is used for dual or tri-band applications only. Using switches in the matching network is another common approach for multi-band operation. There are many ways switches can be used. For example, switches can be used to turn connect/disconnect capacitors or inductors in the matching networks; switches can be used to make tunable transmission lines by controlling the current return path; switches can be used to make tunable shorted stubs. The major drawback with using the switches is the ON loss of the switch, which is technology dependent and varies from process to process. For example, a CMOS switch is usually less lossy than SiGe switch. Another drawback associated with the switch is the granularity. While varactors or tunable inductors may achieve continuous tuning range, a switch-based approach only achieves discrete resolution depending upon the number of switches used.

1.5 Objective and Organization of the Dissertation

The objective of this dissertation is to design the reconfigurable RF components and blocks operating at mm-wave frequencies which can yield a Si-based frequency-agile and adaptive RF front-end. The targeted applications for this work are 5G multi-band wireless communication and reconfigurable short/long range phased arrays for automobile radars. However, the concept of the

proposed reconfigurable RF elements is generic in nature and can be applied to all emerging applications which require on-chip reconfigurability at microwave and mm-wave frequencies.

Chapter 2 presents an analysis on harmonic tuning of stacked power amplifiers. It is concluded that stacked power amplifiers do not benefit from harmonic tuning as much as traditional cascode amplifiers owing to the fact that voltage swing is shared across all the transistors in stacked amplifier. Thus, each transistor needs to be harmonic tuned. Presented analysis shows only tuning the output transistor is not enough.

Chapter 3 presents the design of a reconfigurable impedance matching network at 28 GHz. The matching network is designed to cover half-gamma space in Smith chart. The performance of matching network integrated with PA has been measured and shows the feasibility of this approach. The proposed system is useful in phased array where the scan impedance variation is observed with respect to scan angle.

Chapter 4 builds on the similar concept and used the reconfigurable matching network for frequency band switching. Band-switchable LNA and PA have been designed and measured. Moreover, the designed LNA and PA are put together with the integrated T/R switches to form a bi-directional band-switchable amplifier. The amplifier takes very small die area and shows state-of-the-art performance.

Chapter 5 presents a reconfigurable 18-50 GHz direct down conversion receiver. The receiver is based on mixer-first topology to achieve high linearity. It is designed in 45nm SOI process and consists of a differential quadrature coupler, two-phase double balanced mixer, anti-aliasing positive feedback low pass filter and baseband low noise amplifier. Digital control for gain, filter response and offset calibration has been added.

Chapter 6 summarizes the theme and contribution of this thesis.

2 HARMONIC TUNING OF STACKED POWER AMPLIFIERS

2.1 Introduction

The continuous scaling in modern semiconductor technologies for higher transit frequency (f_τ) leads to a monotonic decrease in the breakdown voltages of the devices, especially for silicon-based device technologies. Therefore, the achievable output power using conventional power amplifier (PA) architectures, where a single device provides the output voltage swing, also decreases more and more. To overcome the low breakdown voltage limitation, it is possible to stack several devices in series. Series stacking of transistors makes it theoretically possible to obtain a higher output voltage swing by dividing the voltage equally among the stacked transistors. For an unchanged output current swing, the output power and the optimal load impedance are higher, allowing a high output power, as well as low impedance transformation ratio for matching networks. On the other hand, power added efficiency (PAE) is often degraded due to parasitic capacitances of intermediate nodes and non-constructive addition of voltage swings because of phase variations. In order to boost PAE, waveform engineering is commonly applied to PAs by harmonic tuning. The harmonic terminations at the output are typically optimized using load pull measurements, resulting in lower power dissipation and PAE enhancement.

In this chapter, we study the applicability of harmonic tuning techniques to stacked amplifiers. We conduct basic circuit analysis to show that the impact of harmonic tuning done at the topmost transistor significantly depends on the number of stacked transistors and the base termination impedance. Therefore, enhancement in efficiency turns out to be quite low as lower transistors continue dissipating more power. As a proof of concept, different X-band PA cores (cascode, tri-stacked and quad-stacked) have been designed and characterized using an active load-pull system

with harmonic tuning capability. PAE contours are acquired for each case, and the measurements confirm the dependence of efficiency enhancement by harmonic tuning on the number of stacked transistors.

2.2 Theory

In a stacked PA, where the output transistor is terminated with a certain load impedance (at fundamental or harmonics), each transistor in the stack will see this impedance differently, mainly depending upon the base terminations. To clarify how the base termination affects the impedance seen by lower transistors, we analyze a generalized case as shown in Figure 2-1.

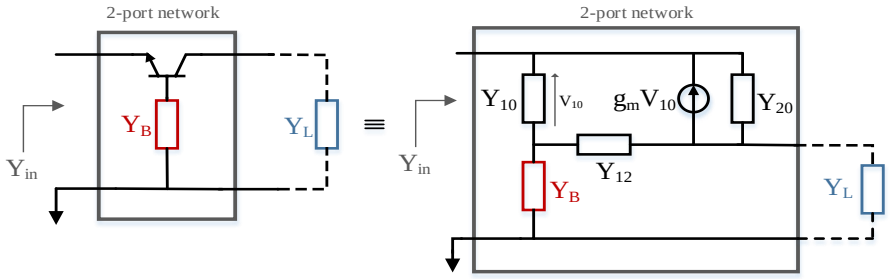


Figure 2-1 Y-parameter analysis of transistor with base and collector termination

Consider a transistor whose base is terminated with an admittance, YB, and the collector is terminated with a load admittance, YL. Using the small signal π-model as shown in Fig. 1, a Y-matrix can be derived. The input admittance of the two-port network can be written as:

$$Y_{in} = y_{11} - \frac{y_{12}y_{21}}{Y_L + y_{22}} \tag{1}$$

To clarify the impact of base termination, we will consider two limit cases:

2.2.1 When the base is shorted

Using $Y_B=\infty$, corresponding to a common-base topology, we get:

$$Y_{in} = g_m + Y_{10} - \frac{Y_{20}(g_m + Y_{20})}{Y_L + Y_{20} + Y_{12}} \quad (2)$$

Since a transistor's small signal ro is high and collector to emitter capacitance is small, Y_{20} becomes very small and we can neglect it. Therefore,

$$Y_{in} \approx g_m + Y_{10} \quad (3)$$

This shows that for the shorted base, Y_{in} becomes almost independent of load termination at output.

2.2.2 When the base is open

This can be further divided into two cases for simplification:

a) When the load is shorted, that is $Y_L=\infty$, (1) gives:

$$Y_{in,SL} = \frac{Y_{12}}{Y_{12} + Y_{10}}[g_m + Y_{10}] \quad (4)$$

b) When the load is open, that is $Y_L=0$, (1) gives:

$$Y_{in,OL} = Y_{in,SL} - \frac{y_{12}y_{21}}{y_{22}} \quad (5)$$

This shows that $Y_{in,OL}$ is smaller than $Y_{in,SL}$ by $\frac{y_{12}y_{21}}{y_{22}}$. This means that Y_{in} has not only become dependent upon Y_L, but also follows the same trend as Y_L; that is, when load is short, Zin becomes low and when load is open, Zin becomes high.

The above analysis draws an important conclusion that if the base of a transistor is terminated with high impedance, its input impedance (seen from the emitter) follows the load impedance (at collector); and if base is shorted (common base), the input impedance becomes independent of

load impedance. Since in stacked PAs, each lower transistor sees the load impedance through the emitter of the transistor above, this means that if the base termination of upper transistor is high, lower transistors can also see load harmonic impedances to a certain extent. However, as the number of stacked transistors increases, the load impedance seen by the lower transistors also reduces, eventually reaching a point where the impedance seen by lower transistors become independent of load impedance. This can be better understood with the help of examining a quad-stacked device as shown in Figure 2-2.

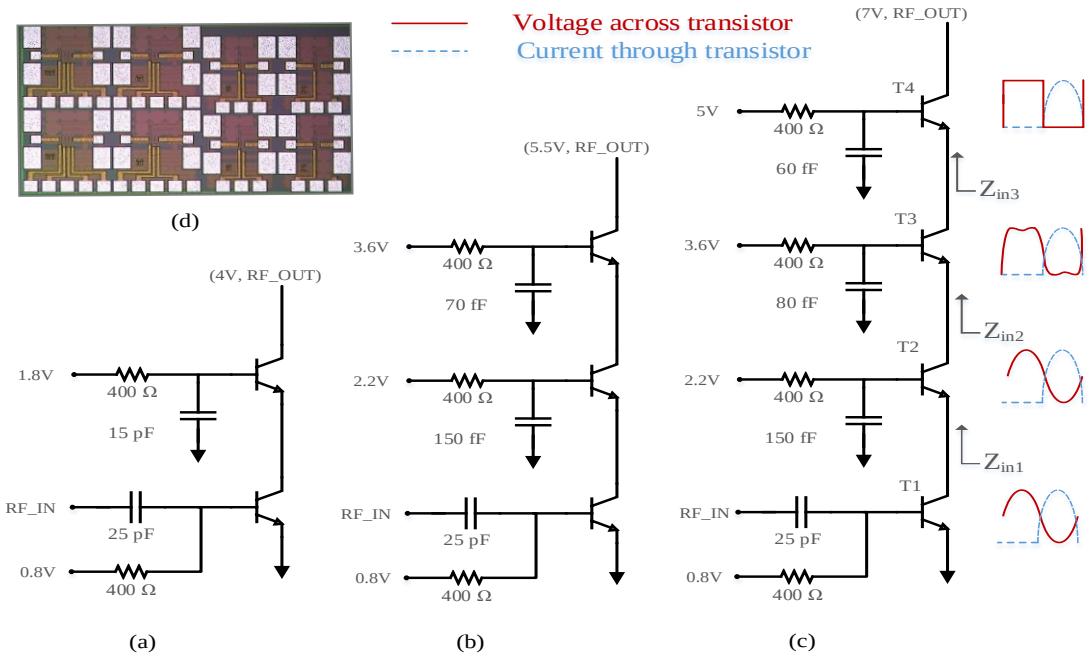


Figure 2-2 Designed X-Band power amplifiers: a) Cascode, b) Tri-stacked, c) Quad-stacked, d) Fabricated chip

Assume T4, the topmost transistor, is harmonically tuned for class-F operation where the second harmonic is shorted, and the third harmonic is presented with open circuit. This results in rectangular voltage waveform across T4. Transistor T3 sees the harmonic terminations through the emitter of T4. Considering that in a stacked design, the base termination impedance is high, the short and open are translated to some low and high impedances, as determined by (4) and (5), so voltage waveform across T3 also gets partially optimized for class F operation. However, T2 does

not benefit as it sees the open load through T3, which translates the open load impedance to a value which is not sufficiently high. Similarly, conditions for T1 tends to be even worse.

A simulation is also performed for the quad-stacked case to see how the impedance seen by each stacked transistor varies as a function of load impedance at the output node. Figure 2-3 shows a Smith chart plot of Z_{in1}, Z_{in2} and Z_{in3} while Z_L is varied from short to open. It can be observed that Z_{in3} follows the trend of Z_L; that is, when Z_L is short, Z_{in3} is also small and when Z_L is open, Z_{in3} is also high. Z_{in2} also follows the trend of Z_L but with smaller variation, whereas for Z_{in1} the variation is very small. This variation in Z_{in} keeps getting smaller as we increase the number of stacked transistors, and eventually converges to (4). Figure 2-3 also includes the case when the base of T4 is grounded and Z_{in3} becomes constant and independent of Z_L variation as expected from (3). These simulations confirm the theoretical analysis presented.

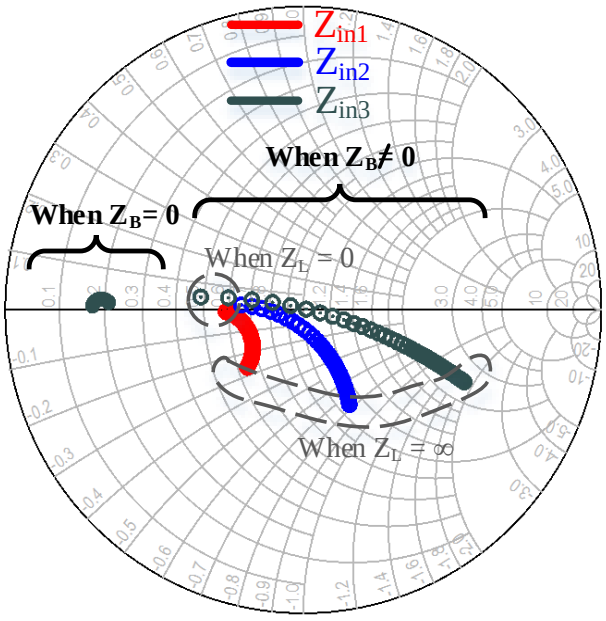


Figure 2-3 Variation of Z_{in1}, Z_{in2}, and Z_{in3} when Z_L is varied from short to open

2.3 Design of Power Amplifiers Core

Cascode, tri-stacked, and quad-stacked PA cores have been designed at X-band using IHP SG25H4 0.25 µm SiGe HBTs with a specified f_τ/f_{max} of 180/220 GHz.

Figure 2-3 shows the designed cascode topology where the upper base is terminated with ample capacitance to have AC ground at X-band frequencies. Also shown are the tri-stacked and quad-stacked topologies where the upper bases are not AC grounded; instead, they are terminated with specific capacitances, based on the guidelines provided here. The values of base capacitors and bias voltages have been optimized through simulations to allow equal voltage swings across each transistor. The 400 Ω resistors are included in bias paths and serve the purpose of RF blocking.

2.4 Measurements

The MT2000 (Maury Microwave) mixed-signal active load pull system is used to perform fundamental and harmonic load pull measurements. All the PAs have been measured with continuous wave (CW) operating conditions at 10 GHz. Source pull is performed for fundamental only, whereas load pull is performed up to three harmonics. On-wafer small signal calibration is done using SOLT standards, and an absolute large signal power calibration is performed using manufacturer supplied SOL standards.

All designed device topologies are biased in class B operation. First, input power and fundamental impedances are swept to find the optimum load and source impedance for maximum PAE, while 2nd and 3rd harmonics are terminated by 50 Ω. Having the fundamental impedance terminated at the desired point, the 2nd harmonic impedance is swept (keeping the 3rd harmonic terminated at 50 Ω), and PAE contours have been measured. After terminating fundamental and

2nd harmonic load impedances at the highest PAE point, 3rd harmonic impedances are swept and PAE contours have been measured. Figure 2-4 shows measured PAE contours, and Figure 2-5 shows measured fundamental output power contours at 2 dB gain compression point.

Table 2-1 lists the PAE and output power (Pout) enhancement by harmonic tuning, where enhancement means the difference between PAE or Pout when a harmonic is terminated at the best possible and the worst possible location. The cascode device shows the highest PAE improvement of 18% for the 2nd harmonic and 5% for 3rd harmonic tuning. The tri-stacked device shows a PAE improvement of 10% for 2nd harmonic, and 2% for 3rd harmonic tuning. The quad-stacked device shows 7% improvement for 2nd harmonic tuning and 1% for the 3rd harmonic. These results are in parallel with the expectations and the analysis provided here.

While recent work suggests individual tuning of harmonic impedance for each stacked transistor, the effectiveness of this technique will potentially be limited, because the suggested additional harmonic termination appears in parallel to the emitter impedance of the next transistor. Our analysis shows that this impedance approaches the value derived in Eq. (4) as the number of the stacked transistors increases, which as a result dominates the impedance at these intermediate nodes.

2.5 Conclusion

Stacked transistor PAs where only the output transistor is loaded with a harmonic termination network does not result in significant overall PAE enhancement. This chapter shows that the more the number of stacked transistors, the lesser the improvement in PAE. This, in part, has to do with the fact that voltage swing is shared between each transistor in a stacked power amplifier; but also due to the reduction of impedance presented by the emitters moving downward

in the stack. Our analysis furthermore shows importance of correct base termination that can lead to a higher impedance at the emitter.

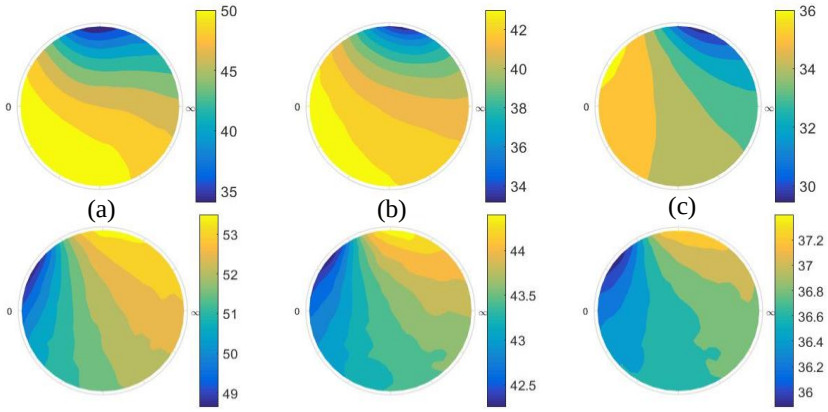


Figure 2-4 Measured PAE (%) contours for 2nd harmonic (top) and 3rd harmonic (bottom) impedance sweep: a) Cascode, b) Tri-stacked, c) Quad-stacked

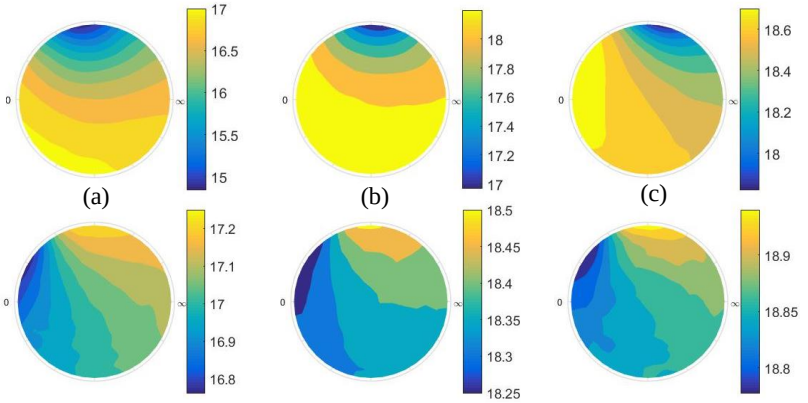


Figure 2-5 Measured fundamental output power (dBm) contours for 2nd harmonic (top) and 3rd harmonic (bottom) impedance sweep: a) Cascode, b) Tri-stacked, c) Quad-stacked

Table 2-1 Comparison of PAE and Pout by Harmonic Tuning

Topology	**Enhancement by 2nd Harmonic Tuning**		**Enhancement by 3rd Harmonic Tuning**	
	PAE (%)	**Pout (dBm)**	**PAE (%)**	**Pout (dBm)**
Cascode	18	2.1	5	0.44
Tri-stacked	10	1.4	2.3	0.26
Quad-stacked	7	0.9	1.6	0.18

3 A KA-BAND POWER AMPLIFIER WITH RECONFIGURABLE IMPEDANCE MATCHING NETWORK

This chapter focuses on the design of a tunable impedance matching network (TMN) at Ka-band. The TMN draws its motivation from the phased arrays where the antenna impedance changes with respect to the scan angle and hence output power and efficiency of the system is degraded due to the mismatch between antenna and the power amplifier. As a proof of concept, a Ka-band power amplifier (PA) is also designed and integrated with the TMN. The output power of the PA is observed as the function of load impedance. The sections below provide details on the analysis and design of PA and TMN.

3.1 Scan Impedance Variation in Phased Arrays

A phased array is an array of antennas where each antenna is excited with different phase to modify the overall radiation pattern and form a beam. Since the antenna elements are normally close to each other ($\lambda/2$ apart) and excited with different phase, there is mutual coupling between adjacent elements which induces stray current in antennas, hence changing the V/I ratio or the impedance of the antenna. The change in impedance depends on the phase difference between the antenna elements which is governed by the scan angle of the beam. Figure 3-1 shows the theoretical variation in reflection coefficient of an antenna element with respect to scan angle for half-wave infinite dipole array at 28 GHz.

3.2 Reconfigurable Impedance Matching Network for Phased Arrays

An analysis on infinite patch array suggests that the magnitude of reflection coefficient varies from 0 to 0.5 (on average) for scan angles up to 60° in E, H or D-plane [11]. Therefore, the design goal is set to match any load within half-gamma around center of the Smith chart. To realize

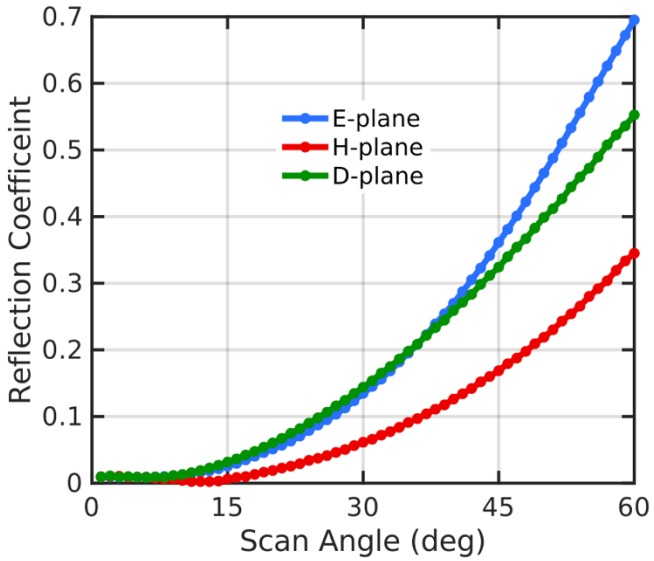


Figure 3-1 Variation in Reflection Co-efficient wrt Scan Angle in Dipole Array at 28 GHz

a more practical circuit, only 7 impedance points (3 inductive, 3 capacitive and one nominal 50 Ω) are chosen which would be able to provide magnitude mismatch of less than 0.2 (i.e., $|\Gamma|<0.2$) for all the loads in half-gamma circle. The mismatch can further be improved by having more impedance points, but it leads to increase in the size and the loss of TMN. Therefore, the loss in the TMN becomes higher than the performance gained by preventing the mismatch. The 0.2 gamma mismatch has been chosen as it provides acceptable performance degradation. This concept is illustrated in Figure 3-2.

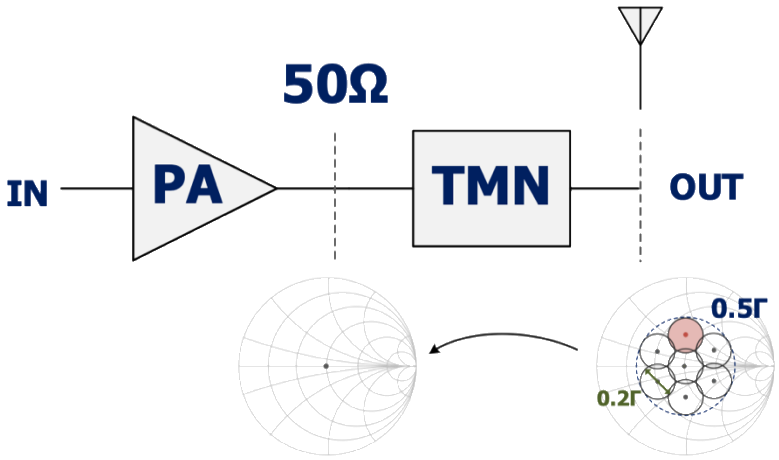


Figure 3-2 Block Diagram of the Proposed System

3.3 Design of Ka-Band PA

The power amplifier has been designed using IHP SG13G2 0.13 μm SiGe HBTs with specified f_τ/f_{max} of 300/500 GHz. The amplifier uses cascode topology and operates common-base transistor in weak-avalanche region. Input has been matched to 50 Ω for small signal conditions whereas output has been matched to 50 Ω for large signal conditions determined through load-pull analysis. Input series capacitor and output shunt capacitors are made low Q to make PA unconditionally stable. Large signal stability has been ensured by sweeping the input bias voltage and maintaining the k-factor greater than one. Figure 3-3 shows the schematic of the PA.

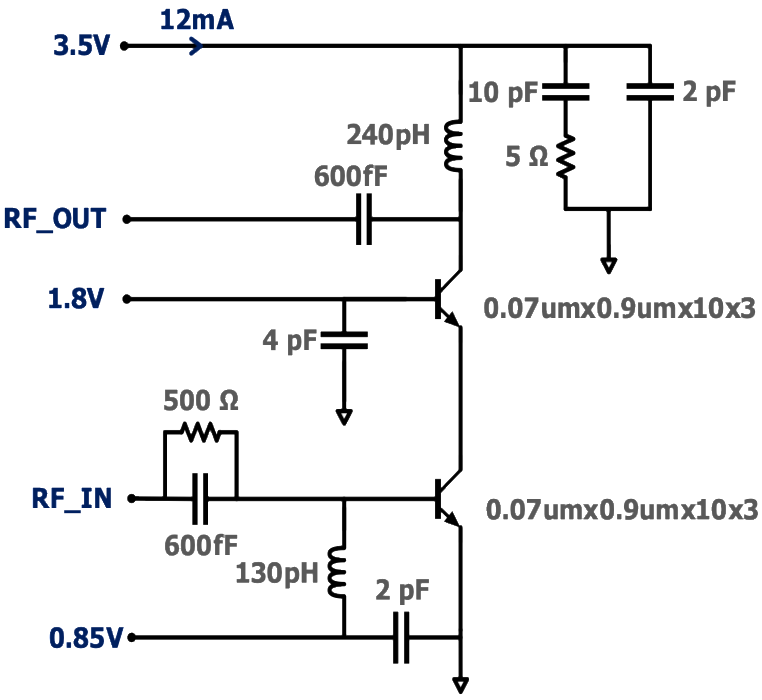


Figure 3-3 Schematic of the K-Band PA

3.4 Design of Reconfigurable Impedance Matching Network

To design a tunable matching network, transmission line based stubs have been preferred over varactors as the available varactors provided very limited tuning range with very low Q. Double shunt stub topology (Figure 3-4) has been chosen as it provides greater flexibility to move around in half-gamma circle and low loss compared to a L sections where the series tunable

element would appear in main signal path and incur more loss. To tune the stubs, transistor switches are used to short out the stub at various points, thus, controlling the effective length of the stub. The number of switches is dictated by the impedance points that are required to match. Since we are targeting 7 impedance points, we need at least 4 switches. However, with 4 switches, we can have 9 different ON/OFF configurations and generate 9 impedance points.

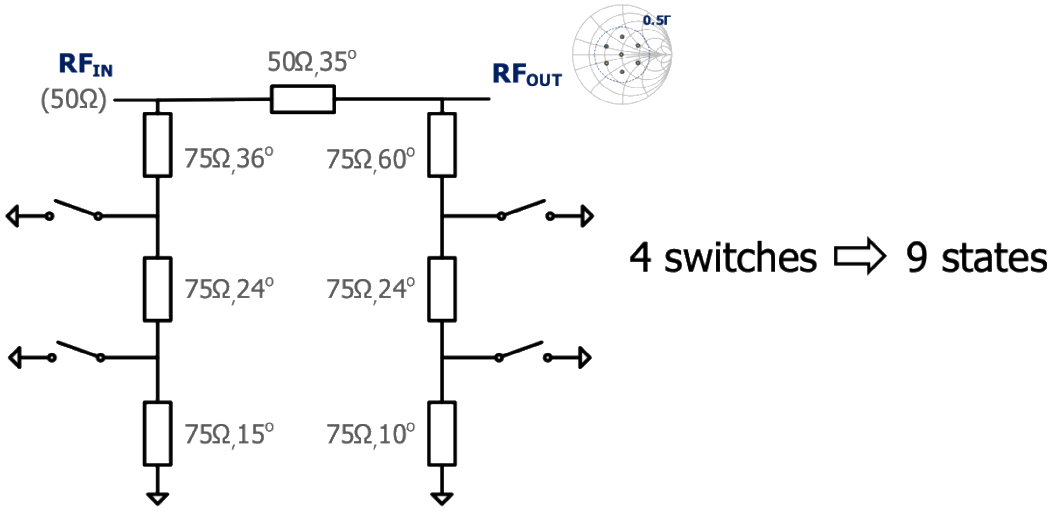


Figure 3-4 Double Stub Reconfigurable Matching Network

3.4.1 Switch Loss Optimization

To tune the stubs, transistor switches are used to short out the stub at various points, thus, controlling the effective length of the stub. The transistor switches are operated in reverse saturated mode where the collector is grounded, and the emitter is connected to RF signal path. This improves the insertion loss of the switch as the emitter is physically well isolated from the conductive silicon, therefore providing better isolation [12]. One concern of using transistors as switches at mm-wave frequencies is the tradeoff between the on resistance and off capacitance. However, since the transmission line itself is a distributed reactive element, it can be modeled as a series of inductors and capacitors, the capacitance of transistors in their off state can be absorbed into the transmission line model, allowing for much larger transistors to be used, which reduces

the on resistance. On the other hand, a too large transistor would have a large off state capacitance which, in turn, would reduce the required length of transmission line to such a point that the physical separation between two switches may not be enough. Also, after a certain size, the decrease in insertion loss (due to decrease in on resistance) is not significant. Therefore, an optimum size is determined by running simulations with different sizes (as shown in Figure 3-5 (a)). The collector of the transistor is DC blocked to avoid any static current while the switch is ON.

An additional concern is the linearity of the switch. This is critical in the OFF state, as the AC voltage present at the emitter leaks to the base of the switch and develops a base-emitter differential, which may self-actuate the switch. This can be alleviated by applying a reverse bias on the switch. Figure 3-5 (b) plots 1-dB compression point of the switch against reverse bias applied to it. The reverse emitter-base breakdown limit for HBT in this process is -1.6V, therefore we use a VBE of -1.5V, which gives 22 dBm compression point which is far higher than the PA 1dB output compression point of 15.5 dBm. Therefore, the linearity of the PA is not affected, and switch is not operated beyond its breakdown limit

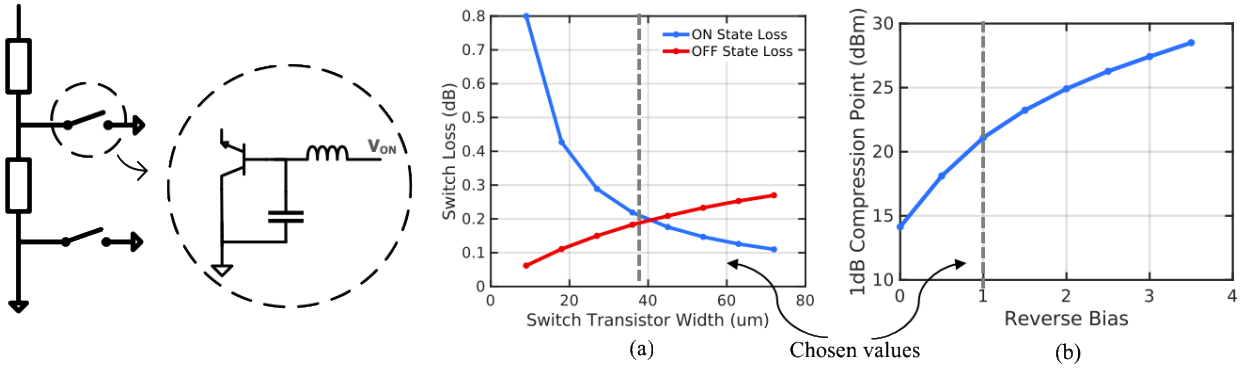


Figure 3-5 (a) Switch Loss against Switch size (Width), (b) P1dB of the Switch in OFF State against Reverse Bias Voltage

3.4.2 Shunt Stub Loss Reduction Technique (Theoretical Analysis)

Consider a transmission line stub of characteristic impedance Z_o, electrical length θ, and terminated by ON impedance of the switch R_{ON}. The impedance looking into the stub, Z_{in}, is given as:

$$Z_{in} = Z_o \frac{R_{ON} + jZ_o tan(\theta)}{Z_o + jR_{ON} tan(\theta)}$$

Rationalizing the denominator to separate real and imaginary parts:

$$Z_{in} = Z_o \left[\frac{Z_o R_{ON}(1 + tan^2\theta)}{Z_o^2 + R_{ON}^2 tan^2\theta} + j \frac{Z_o^2 tan\theta - R_{ON}^2 tan\theta}{Z_o^2 + R_{ON}^2 tan^2\theta} \right]$$

The quality factor of impedance Zin can be defined as:

$$Q = \frac{X_{in}}{R_{in}} = \frac{tan\theta(Z_o^2 - R_{ON}^2)}{Z_o R_{ON}(1 + tan^2\theta)}$$

using trigonometric identities, it can be simplified to following:

$$Q = \left[\frac{Z_o^2 - R_{ON}^2}{Z_o R_{ON}} \right] \left[\frac{sin2\theta}{2} \right]$$

Assuming R_{ON}= 5 Ω, Figure 3-6 (a) plots Q for different Z_o of the stub against θ. There are two important observations:

1. the quality factor of the Z_{in} increases as the characteristic impedance of the stub increases
2. the quality factor peaks at an electrical length of 45°

This means to have the highest quality factor (to reduce loss), the design procedure should be as follows:

1. start with the stub length of 45°and the highest characteristic impedance allowed by the process
2. optimize the characteristic impedance to meet the desired impedance for matching

Please note that the highest characteristic impedance of the stub is limited by the process design rules like width and spacing of the conductors. For example, the process used is this chapter requires minimum top metal width of 2 um which limits the characteristic impedance to 105 Ω if the stub is realized using a microstrip transmission line.

While the above analysis is valid for near lossless transmission lines, a lossy transmission line needs special treatment. The quality factor of lossy transmission line terminate with R_{ON} can be derived using the similar method as in previous subsection:

$$Q = \left[\frac{Z_o^2 - R_{ON}^2}{Z_o R_{ON}}\right]\left[\frac{tanh(\gamma l)}{1 + tanh^2(\gamma l)}\right]$$

where

$$\gamma = \alpha + j\beta$$

Here, α is the attenuation constant and β is the phase constant. The attenuation constant, α, is dependent on the physical width of the conductor used to realize the transmission line. For example, the attenuation constant for microstrip transmission line can be given as:

$$\alpha = \frac{R_s}{Z_o W}$$

where Rs and W are resistivity and width of the conductor, respectively. Above expression shows that attenuation constant is inversely related to the width of the conductor. Therefore, a stub of higher characteristic impedance (i.e., lower conductor width) has higher attenuation constant. This

means that we cannot use the highest characteristic impedance available from a given process as then the loss is then dominated by the physical conductor width. On the other hand, a small characteristic impedance stub also has poor quality factor as described in the previous subsection. This suggests there should exist an optimal characteristic impedance for which the loss reaches minima. Figure 3-6 (b) compares the quality factor of a lossless and a lossy stub against the characteristic impedance. It can be seen that while the Q-factor of the lossless line increases linearly with the characteristic impedance, the lossy line has peak Q-factor around 90 W characteristic impedance. This observation leads to the following design procedure:

1. sweep the characteristic impedance of the stub (while adjusting the electrical length to maintain a fixed impedance looking into the stub) to find optimal condition for peak Q
2. optimize the stub length to meet the desired impedance for matching

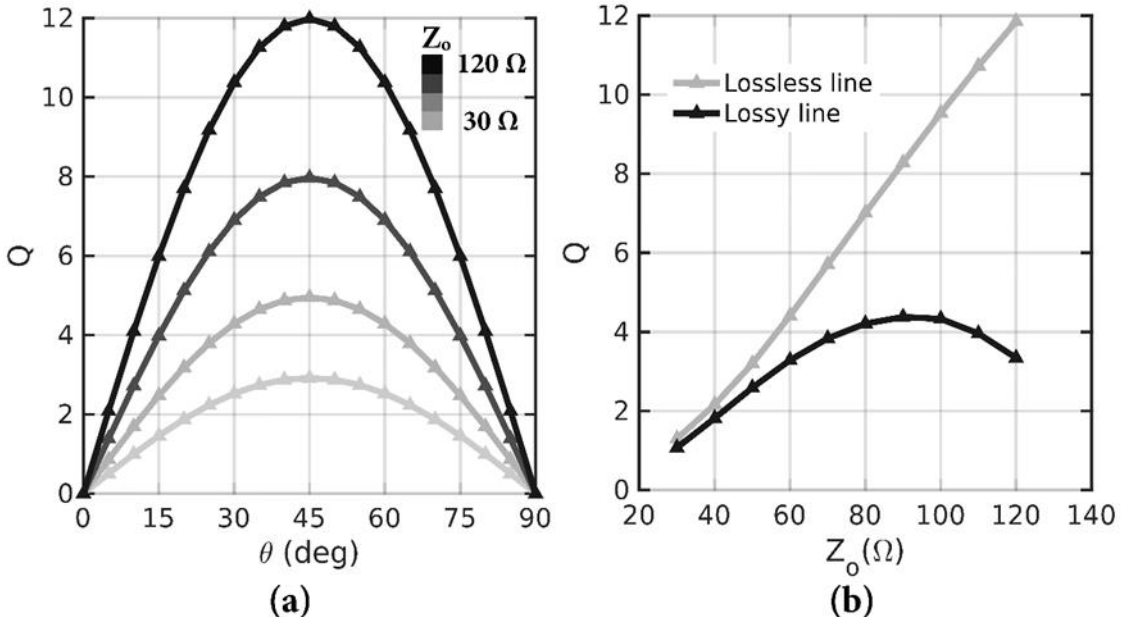


Figure 3-6 Quality factor of shunt stub: (a) against electrical length of lossless stub

3.4.3 Shunt Stub Loss Reduction Technique (Intuitive Analysis)

Consider two cases as shown in Figure 3-7. Let's say we want to match the impedance 36-j50 Ω as shown by the red dot in Smith chart. Say, we have designed first shunt stub and the series stub, and we need to design the second stub is supposed to provide Z_{sh2} impedance. Now, there are different (Z_o,θ) pairs that can be used in order to realize Z_{sh2} impedance. The choice of pair does not affect the stub loss. However, if the stub is terminated with switch impedance (say 5 Ω), the different (Z_o,θ) pairs are not able to generate the same Z_{sh2} impedance. It appears that the higher characteristic impedance, the closer the stub impedance gets to Z_{sh2} as shown in Figure 3-6. Therefore, a very high characteristic impedance is desired. However, as the characteristic impedance increases, the width of the transmission line becomes smaller which increases the metallic loss of the conductor. On the other hand, if characteristic impedance is reduced, we may

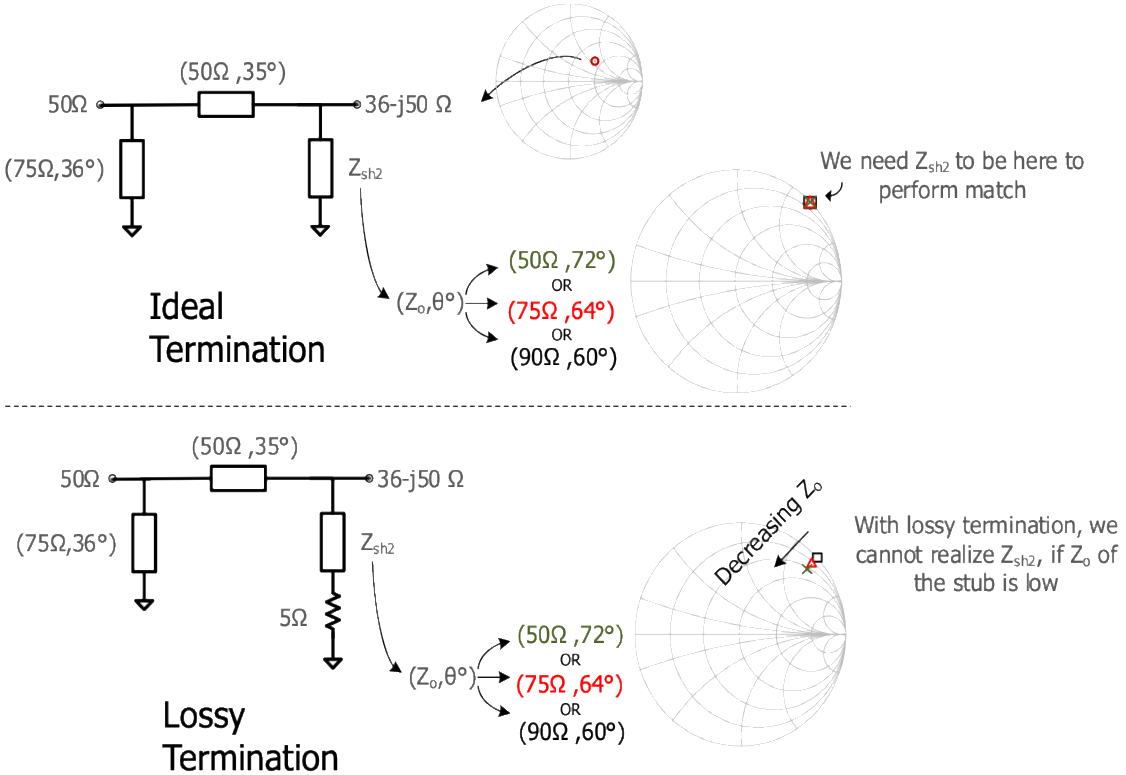


Figure 3-7 Explanation of Shunt Stub Characteristic Impedance Effect on Matching with and Without Lossy Termination

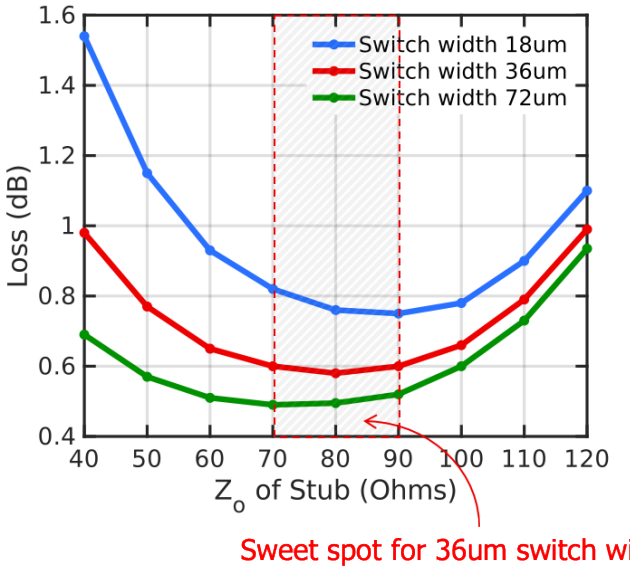


Figure 3-8 Stub Characteristic Impedance Showing Different Sweet Spots for Different Switch Widths (or Resistances)

not be able to generate Z_{sh2} impedance. Therefore, there exists is a sweet spot for characteristic impedance of the stub which depends on the switch resistance and the place where the stub is connected in the matching network. Figure 3-8 shows the variation of loss against the characteristic impedance of the stub.

3.5 Complete Schematic

Figure 3-9 shows complete schematic of TMN+PA and Figure 3-10 shows the chip photo.

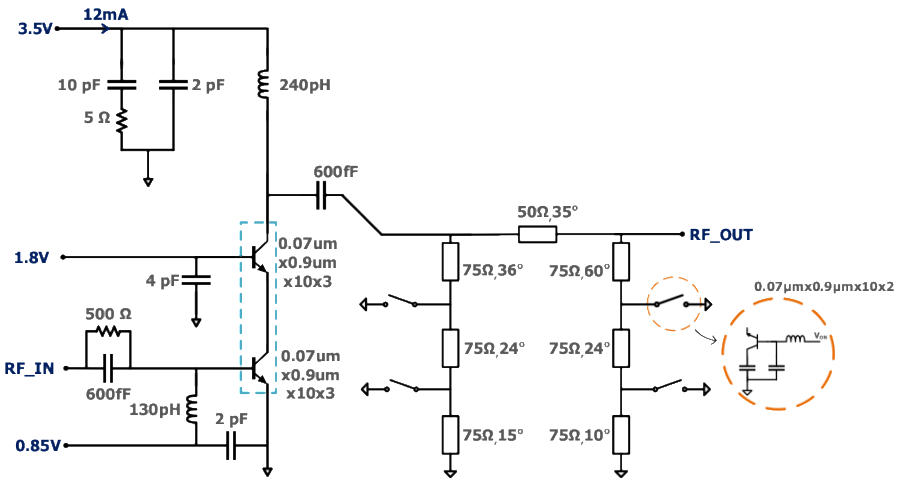


Figure 3-9 Complete Schematic

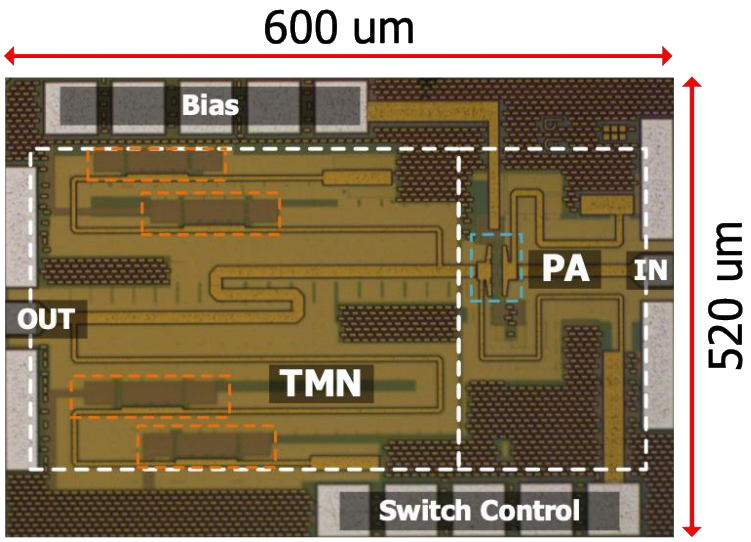


Figure 3-10 Chip Photo

3.6 Measured Results

Two sets of measurements have been performed. First, tunable matching network has been characterized by measuring small signal parameters using Agilent N5227A PNA. Figure 3-11 shows the simulated and measured Smith chart coverage at 26.5 GHz for various switch settings. The measured impedances are slightly off from the simulated impedances due to imperfections in

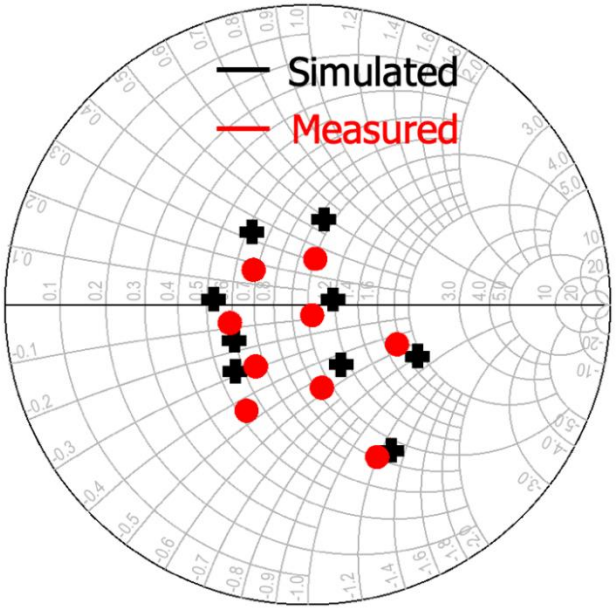


Figure 3-11 Measured and Simulated TMN Impedance Points for All Switch States

the layout. Second, large signal measurements of the PA integrated with TMN have been

performed at 26.8 GHz using MT2000 (Maury Microwave) active load pull system. Figure 3-12 shows 3 dB compressed output power contours and Figure 3-13 shows peak PAE contours for nine different switch states. The power contours shift to different impedance points depending upon the switch states, thereby covering more than half of the Smith chart. Figure 3-14 shows combined peak PAE and 3dB compression power contours which have been plotted by taking out the maximum of PAE and power from individual contours for each switch state. The contours are plotted with 5% PAE steps and 2 dBm Pout steps. The max PAE contour (20%) is very wide (compared to a typical non-tunable PA where max PAE happens only at a narrow region) which means the PA can match to different impedances within that contour and provide constant efficiency. Next, second PAE contour (15%) covers more than half of the Smith chart, and similarly power contours are very wide, indicating the ability of the PA+TMN to match different load impedances and provide constant performance throughout the half-gamma region.

3.7 Summary

This chapter shows a tunable matching network integrated with the PA at Ka-band for eliminating mismatch between PA and antenna due to scan impedance variation in a phased array system. The matching network uses double shunt stub topology with tunable stubs and covers half-gamma area in the Smith chart. Guidelines to optimize switch and stub loss has been presented. The measured results confirm the feasibility of this approach by showing wide and expanded PAE and Pout contours. The proposed integrated impedance matching networks can also be used to tune the center frequency of the PA or compensate for variations in the active device parameters due to temperature drift, fabrication tolerances or on-chip load pull purposes.

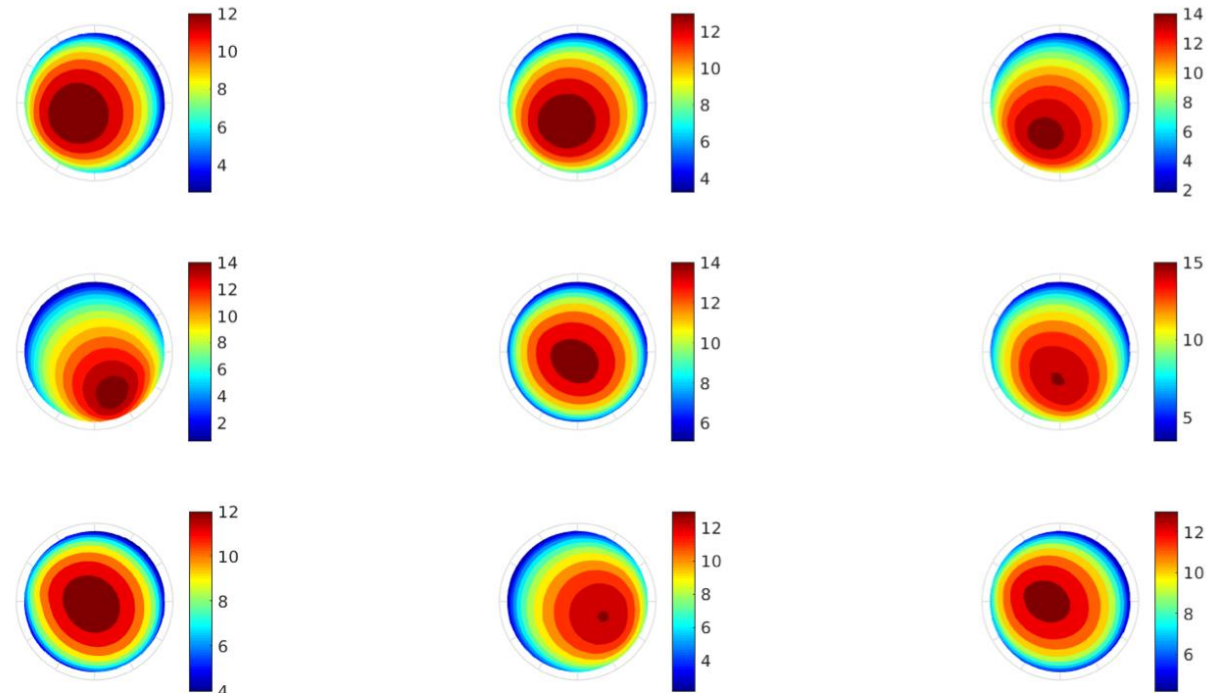


Figure 3-13 Measured 3dB Compressed Power (dBm) Contours for All Switch States

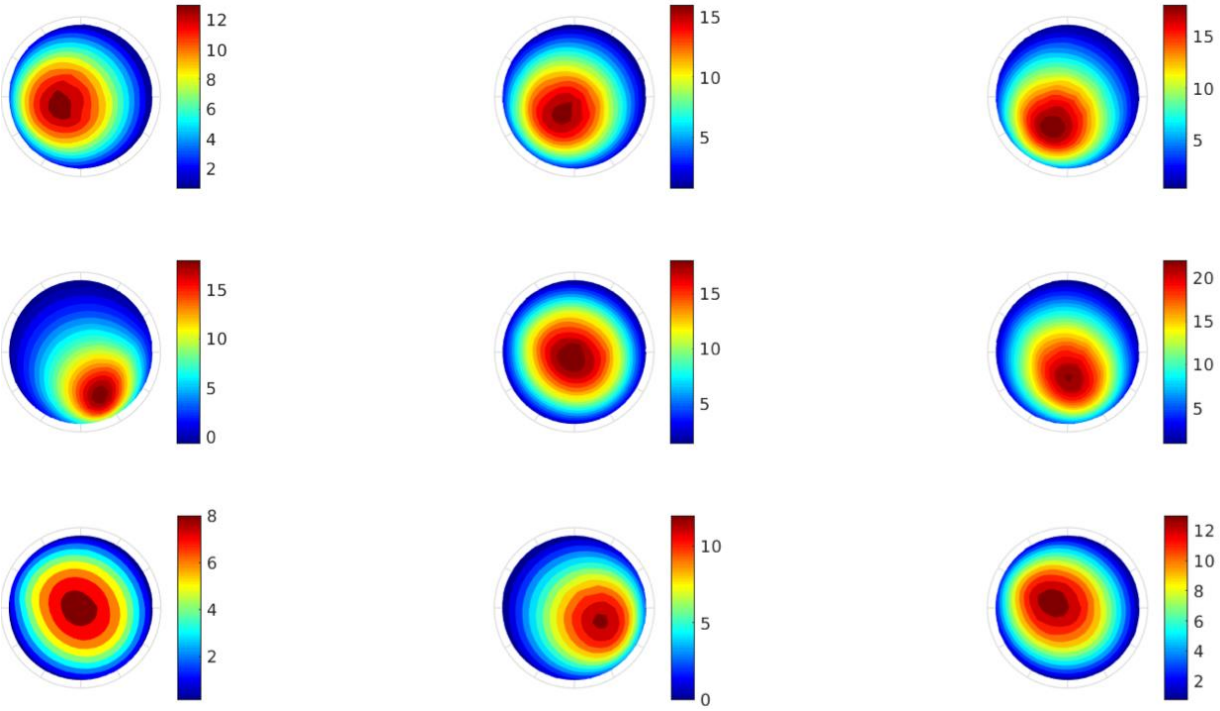


Figure 3-12 Measured Peak PAE (%) Contours for All Switch States

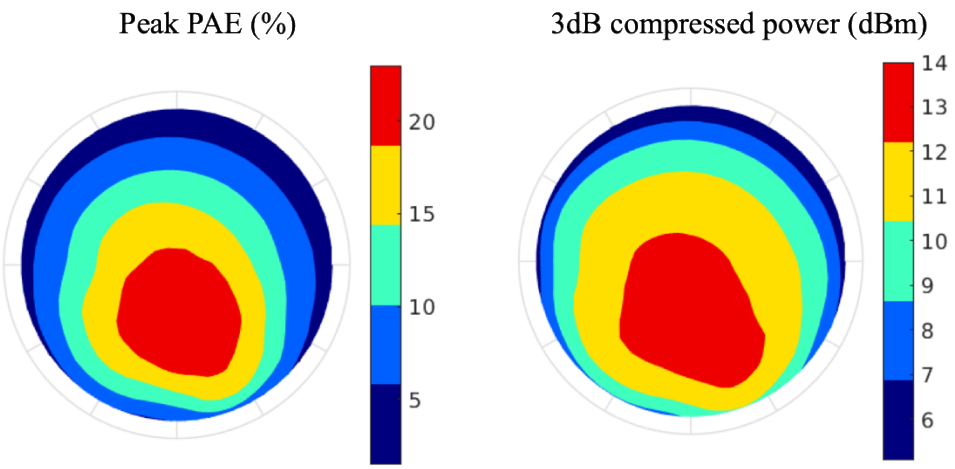


Figure 3-14 Combined Contours of Peak PAE and 3dB Compressed Output Power from Each Switch State

4 A COMPACT KA/V BAND-SWITCHABLE TRX AMPLIFIER WITH INTEGRATED T/R SWITCHES

This chapter builds on the previous chapter and uses the reconfigurable matching network to change the frequency band of operation. To demonstrate the effectiveness of this approach, a highly integrated 28/60 GHz band-switchable transmit-receive (TRX) amplifier is designed which consists of 28/60 GHz LNA, 28/60 GHz PA and integrated transmit-receive (T/R) switch. A dual-band transceiver operating at Ka/V band is of special interest for both radar and wireless communication purposes. The vast unlicensed bandwidth (7 GHz) at V-band can provide multi-Gbps data rate for communications or very high resolution for radar at V-band, whereas the low atmospheric and free-space propagation loss at Ka-band can provide long distance communication or higher range for radar. Furthermore, due to the varying propagation characteristics and capacities among different potential 5G bands, a reconfigurable or multi-band RF transceiver unit is proposed, which can use appropriate frequency band as required by the environment, country or application. The designed 28/60 GHz TRX amplifier achieves state of the art performance by co-designing the amplifiers with T/R switch, thereby occupying a very small real estate. Sections below discuss design of individual blocks and integration.

4.1 Ka/V Band-Switchable PA

The PA is designed in IHP SG13G2 BiCMOS process. The technology features high performance 130 nm HBTs with a specified f_T/f_{max} of 300/450 GHz. The collector-emitter breakdown voltage, BVCEO, equals 1.7 V and collector-base breakdown voltage, BVCBO, equals 4.8 V.

4.1.1 Amplifier Design

Figure 4-1 shows the circuit diagram of the designed PA. T1 (gm transistor) and T2 (cascode transistor) have been biased in class AB mode. T2 operates in weak avalanche region with its base terminated with a very low impedance (AC ground). SiGe HBT cascode PAs designed in this fashion with low upper base resistance allow large-signal collector voltage excursions beyond BV_{CEO} without occurrence of catastrophic damage and without impact to long-term hot-carrier reliability [13]. Device sizes and bias current are optimized through load pull simulations to achieve output power around 17 to 18 dBm. The base node of cascode transistor (T2), which is AC grounded, is very prone to oscillation at mm-wave frequencies. Therefore, large AC ground capacitors have been laid out as close to the base as possible, and EM simulations have been performed to ensure stability. Also, the low-frequency oscillations arising due to RF chokes in the bias paths have been suppressed by shunting the bias paths with proper low-Q capacitors. Figure 4-2 shows chip photo and EM simulation model.

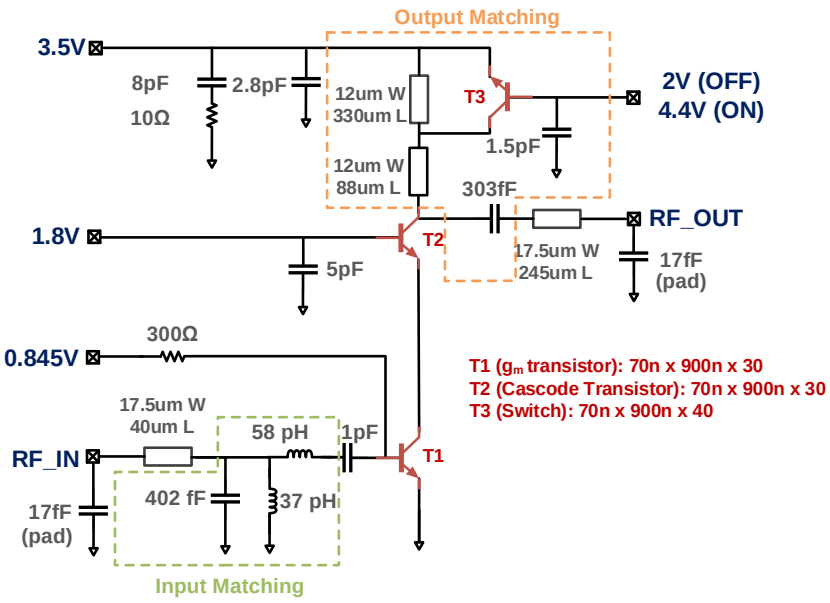


Figure 4-1 Schematic of Ka/V Band-Switchable PA

4.1.2 Matching Network Design

The input of the PA has been dual-band matched at 28/60 GHz by employing a parallel LC tank and a series inductor. This tank resonates around 36 GHz, thereby providing positive reactance below 36 GHz and a negative reactance above 36 GHz. Therefore, the LC tank behaves as an inductor at 28 GHz and as a capacitor at 60 GHz. In essence, it's an L-type matching network with a L_{shunt}-L_{series} topology at 28 GHz and a C_{shunt}-L_{series} topology at 60 GHz, as shown in Figure 4-3 (a). The output of the PA has been dual-band matched at 28/60 GHz by using a shunt stub and series capacitor. The shunt stub is a thin film microstrip line (TFML) with an HBT switch used to tune its length. When the switch is turned OFF, the RF signal sees a longer stub length and PA switches to the 28 GHz mode. When the switch is turned ON, it shorts a part of the stub to the ground, effectively reducing the length of the TFML, as shown in Figure 4-3 (b). Therefore, RF signal sees a shorter stub length and the PA switches to the 60 GHz mode.

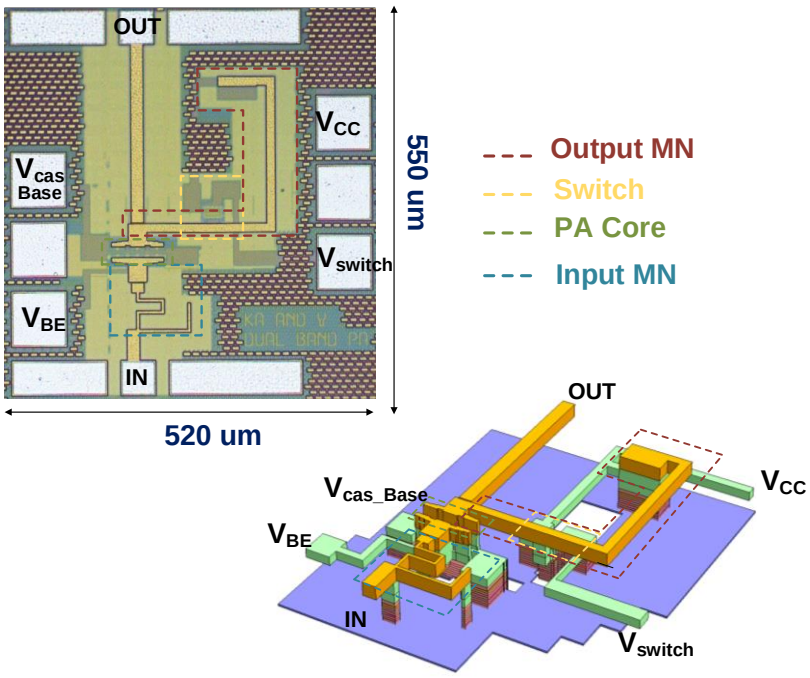


Figure 4-2 Chip Photo and EM Simulation Model

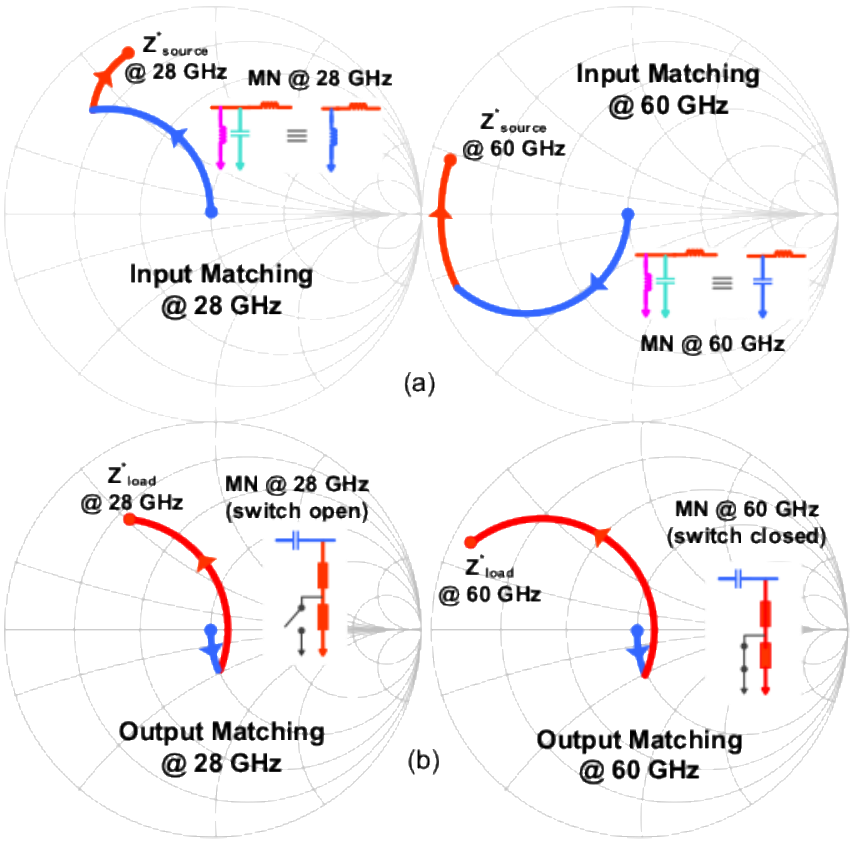


Figure 4-3 Illustration of Input Output Dual-Band Matching (a) at 28GHz, (b) at 60 GHz

4.1.3 Switch Design

The loss incurred by the switch in the TFML can be minimized by reducing the product I^2Z product as described in section 3.4.1 and 3.4.2. Figure 4-4 (a) shows dependence of the switch loss on the characteristic impedance of the stub. As we move to low characteristic impedances, input impedance of the shunt stub decreases, which increases the switch loss, whereas for high characteristic impedances metallic loss through conductor dominates (as physical width of the conductor decreases). Therefore, there exists an optimum where the loss is minimum. Figure 4-4 (a) shows this is Z0=60 Ω in this case. Therefore, while designing the shunt stub a 60 Ω characteristic impedance is chosen, and the length is then determined according to the matching network requirement. As for the switch ON resistance, R_{sw}, it can be minimized by increasing the

switch size. However, there is a trade-off between the ON resistance, OFF resistance and OFF capacitance. Since the transmission line itself is a distributed element, the capacitance of the switch in the OFF state can be absorbed into the transmission line, allowing for much larger transistors to be used with lower ON resistance. After a certain size, the reduction in insertion loss in ON state (due to decrease in ON resistance) becomes insignificant whereas the increase in insertion loss in OFF state (due to proportional decrease in OFF resistance) becomes significant. Also, at large switch size, there is additional drop to PAE due to the switch bias current. Figure 4-4 (b) captures these tradeoffs. Based on these tradeoffs, switch size of 0.09 x 36 mm^2 is chosen which results in 0.7dB loss in ON state, 0.3dB loss in OFF state and 2% additional decrease in PAE due to switch bias current. Switch is turned OFF by applying reverse bias which helps in improving the linearity as described in section 2.4.1.

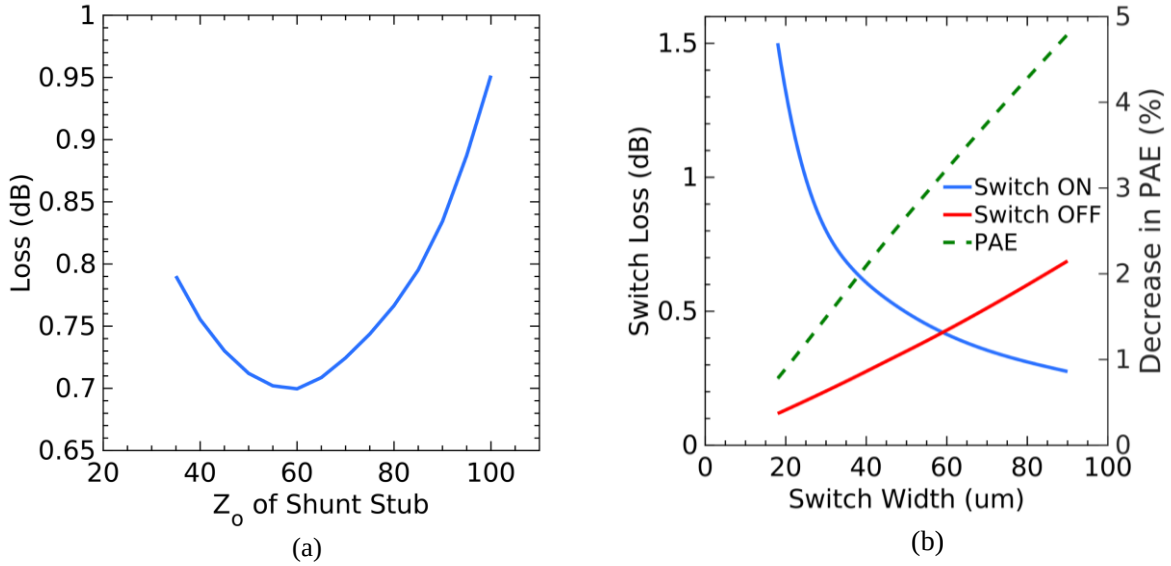


Figure 4-4 (a) Stub Loss vs Characteristic Impedance of Stub, (b) Switch Loss vs Switch Size

4.1.4 Measured Results

Small signal measurements have been performed using Keysight N5227A PNA network analyzer which is calibrated using SOLT standards from 0.1MHz to 67 GHz range. Figure 4-5 (a) and (b) shows measured and simulated s-parameters at 28 GHz and 60 GHz respectively. Measured

gain at 28/60 GHz is 16.2/11.8 dB and measured input return loss is -8/-19 dB. To measure the output power, input of the PA is excited using a Keysight E8257D analog signal generator and the output is measured using Keysight N9010B EXA signal analyzer. Figure 4-5 (c) shows measured and simulated PAE at 28/60 GHz and Figure 4-5 (d) shows measured and simulated output power at 28/60 GHz. Due to the measurement setup, there is measurement uncertainty of ± 0.2 dB in the output power which also adds uncertainty of ± 1.5 % to the peak PAE. The PA shows simulated

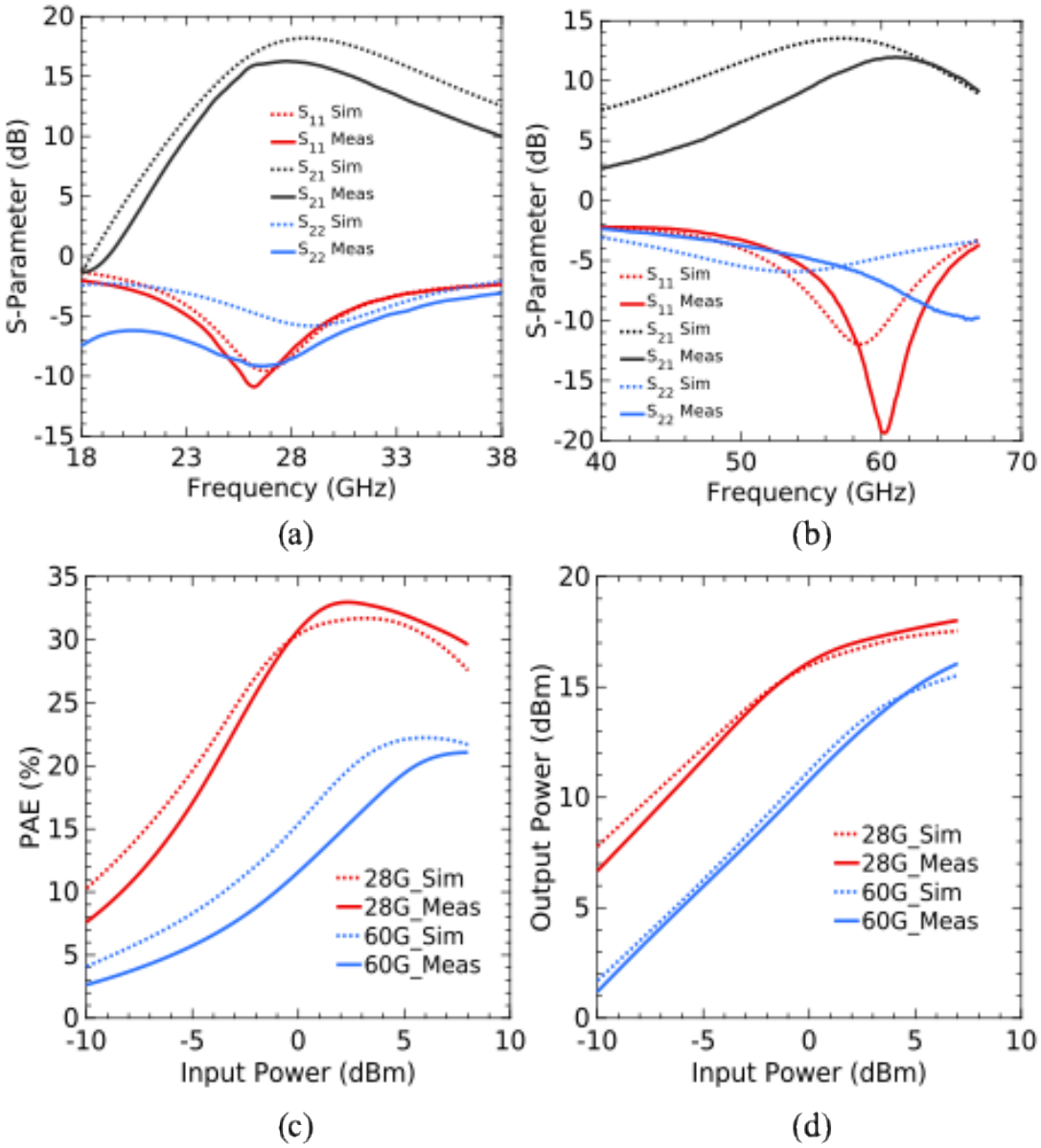


Figure 4-5 (a) S-param at 28 GHz, (b) S-param at 60 GHz, (c) PAE at 28 and 60 GHz, (d) Output Power at 28 and 60 GHz

P_{sat} of 18/16.5 dBm and simulated peak PAE of 32/22 % at 28/60 GHz whereas the measured Psat is 18.4/17.2 dBm and measured peak PAE is 33/21 % at 28/60 GHz. Table 4-1 compares this PA with the most recent single-band and wideband PAs around 28/60 GHz frequencies.

4.1.5 Summary

A band-switchable PA operating in 28 GHz and 60 GHz mode is presented. The PA employs cascode topology, LC tank at input matching network and tunable stub at the output matching network to shift the frequency of operation between 28 GHz and 60 GHz. Performances in each band are comparable to single band state of the art PAs. The designed PA is suitable for 5G transceivers or dual-band phased array radars.

Table 4-1 State-of-the-art Single Band, Multi-Band and Wideband PAs

Reference		Technology	Topology	Frequency (GHz)	P_{sat} (dBm)	Peak PAE (%)	Gain (dB)	Core Area (mm^2)
Dual-band PA	This Work	130 nm SiGe	Class AB Cascode	28	18.4	33	16.2	0.1
				60	17.2	21	11.8	
Dedicated Single Band PAs	2017 ISSCC [14]	45 nm SOI	Cascode	60	16.7	28.3	24	0.067
	2018 MWCL [15]	45 nm SOI	Cascode	60	18.5	25.5	15	0.12
	2016 ISSCC [16]	130 nm SiGe	Cascode	60	23.6	27.7	24	0.55*
	2015 ISSCC [17]	28 nm CMOS	Doherty	60	18.2	21	15.2	0.16
	2017 TMTT [18]	130 nm SiGe	Class AB Harmonically Tuned	28	18.8	35.3	15.5	0.27
	2018 MWCL [19]	45 nm SOI	Doherty	28	22.4	40	10	0.25*
	2018 RFIC [20]	45 nm SOI	Hybrid Class F/F^{-1}	28	18.6	45.7	11.4	0.14
	2018 RFIC [21]	90 nm CMOS	Cascode	28	26	34	16.3	0.4
	2016 JSSCC [22]	28 nm CMOS	CS w/ Source Degen.	28	14	35.5	15.7	0.155
Wideband PAs	2011 TMTT [23]	130 nm SiGe	Distributed	DC-77	17.5	13	10	2.2#
	2018 PAWR [24]	130 nm SiGe	Distributed	12-40	21.5	20.1	14	1.2#
	2016 JSSC [25]	90 nm SiGe	Distributed	14-105	15&	9.7	12	1.51#
	2017 MWCL [26]	180 nm CMOS	Distributed	2-22	14.5&	10	11.9	1.7#

4.2 Ka/V Band-Switchable LNA

The LNA is also designed in the same SG13G2 BiCMOS process. The design procedure of Ka/V band switching is almost the same as described in the section 4.1 for the PA. However, some details are presented here again.

4.2.1 Amplifier Design

Figure 4-6 shows the circuit diagram of the designed LNA. T_1 (g_m transistor) and T_2 (cascode transistor) have been biased in class AB mode. Device sizes and bias current are optimized through s-parameter simulations for minimum noise figure. Emitter degeneration inductor and base inductor at the input have been added to bring Γ_s and Γ_{opt} closer for simultaneous noise and input matching. The base node of cascode transistor (T_2), which is AC grounded, is very

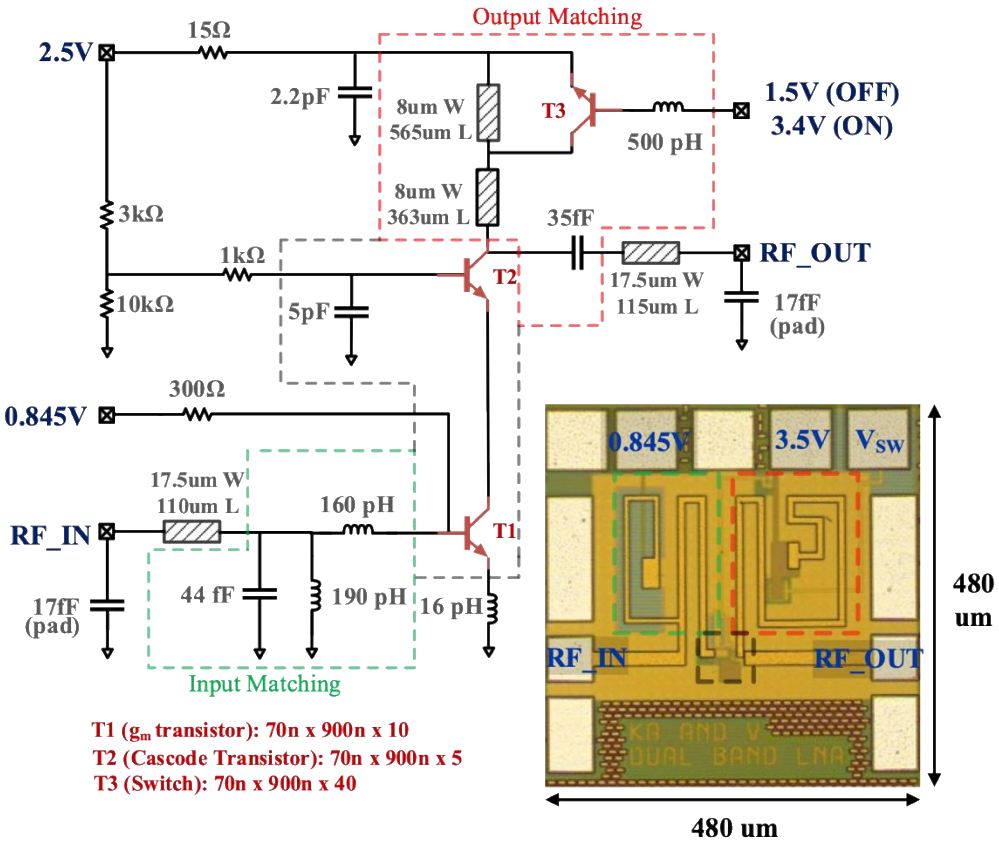


Figure 4-6 Schematic of Ka/V Band-Switchable LNA

prone to oscillation at mm-wave frequencies. Therefore, large AC ground capacitors have been

laid out as close to the base as possible, and EM simulations have been performed to ensure stability. A series resistor of 15Ω has been added in VCC path to suppress low-frequency oscillations arising due to RF choke.

4.2.2 Matching Network Design

The input of the LNA has been dual-band matched at 28/60 GHz by employing a parallel LC tank and a series inductor. This tank resonates around 54 GHz, thereby providing positive reactance below 54 GHz and a negative reactance above 54 GHz. Therefore, the LC tank behaves as an inductor at 28 GHz and as a capacitor at 60 GHz. In essence, it's an L-type matching network with a L_{shunt}-L_{series} topology at 28 GHz and a Cshunt-Lseries topology at 60 GHz, as shown in

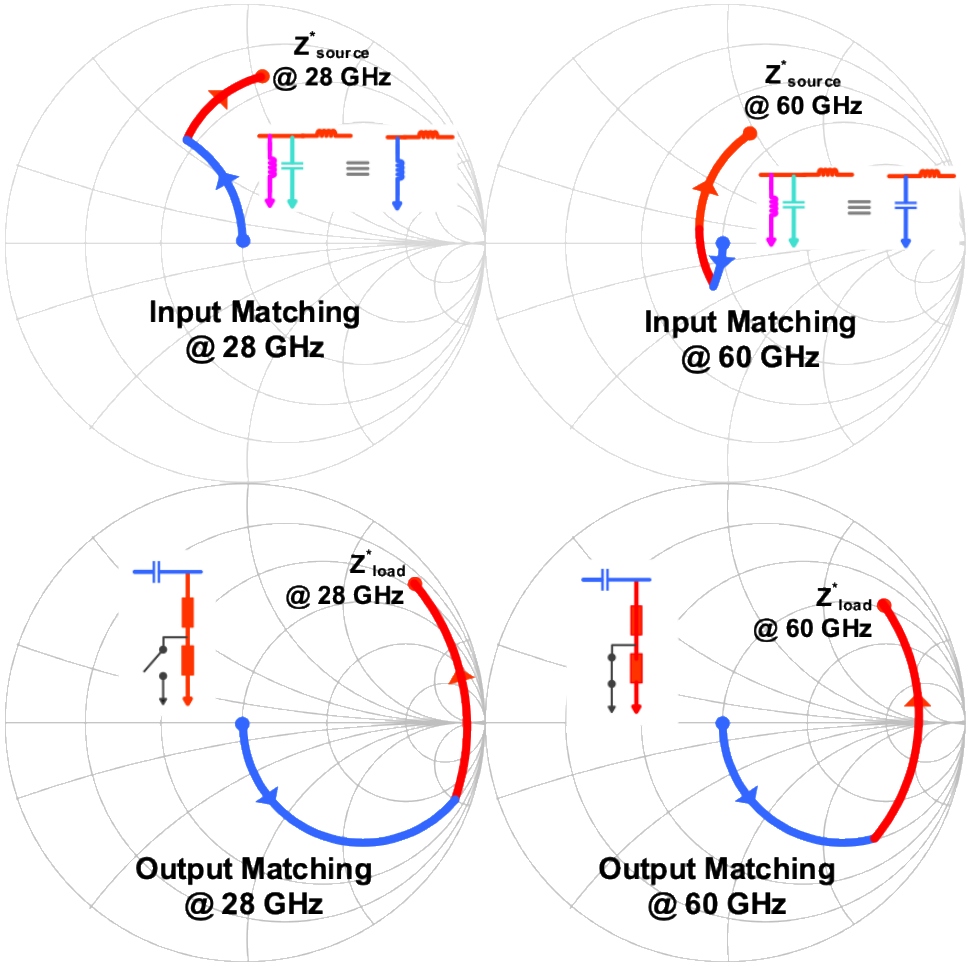
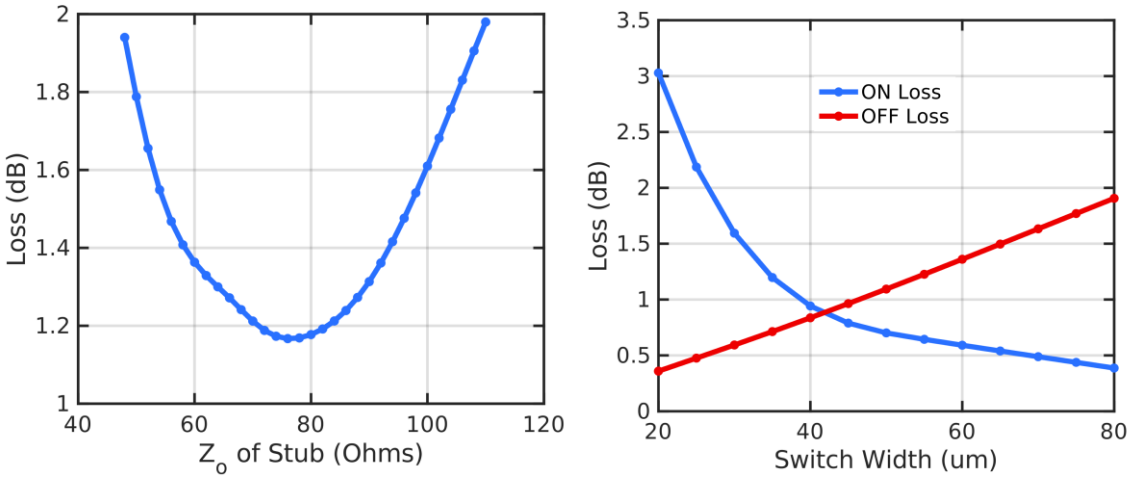


Figure 4-7 Illustration of Input Output Matching at 28 and 60 GHz

Figure 4-7. The output of the LNA has been dual-band matched at 28/60 GHz by using a shunt stub and series capacitor. The shunt stub is a thin film microstrip line (TFML) with an HBT switch used to tune its length. When the switch is turned OFF, the RF signal sees a longer stub length and LNA switches to the 28 GHz mode. When the switch is turned ON, it shorts a part of the stub to the ground, effectively reducing the length of the TFML. Therefore, RF signal sees a shorter stub length and the LNA switches to the 60 GHz mode.

4.2.3 Switch Design

The switch and stub loss have been optimized using the same guidelines as presented in section 4.1.3 for the power amplifier case. As mentioned in this section, the loss of the stub is dependent on the characteristic impedance of the stub, and there exists a sweet spot where the stub of the loss is minimum. This is shown in Figure 4-8 (a). The loss of the stub is minimum around 75 Ω, therefore we chose 75 Ω characteristic impedance for all the stub design. The switch loss depends on the switch size. However, after a certain size the reduction in loss is not appreciable, therefore through simulations a size has been chosen (as shown in Figure 4-8 (b) where ON loss



(a) (b)

Figure 4-8 (a) Stub Loss vs Z_o of Stub, (b) Switch Loss vs Switch Size

is not so high and OFF loss is also small. More details on design has already been presented in section 4.1.3.

4.2.4 Measured Results

Small signal measurements have been performed using Keysight N5227A PNA network analyzer which is calibrated using SOLT standards from 0.1MHz to 67 GHz range. Figure 4-9 shows measured and simulated s-parameters at 28 GHz and 60 GHz respectively. Measured gain at 28/60 GHz is 16.2/15 dB, input return loss is -10/-6 dB and the output return loss is -7/-8 dB. To measure the compression point, input of the PA is excited using a Keysight E8257D analog signal generator and the output is measured using Keysight N9010B EXA signal analyzer. The measured P1dB input compression point is -12/-7 dBm at 28/60 GHz whereas the simulated compression point is -11/-7 dBm at 28/60 GHz. Figure 4-10 shows gain and output power plots at 28 GHz and 60 GHz respectively.

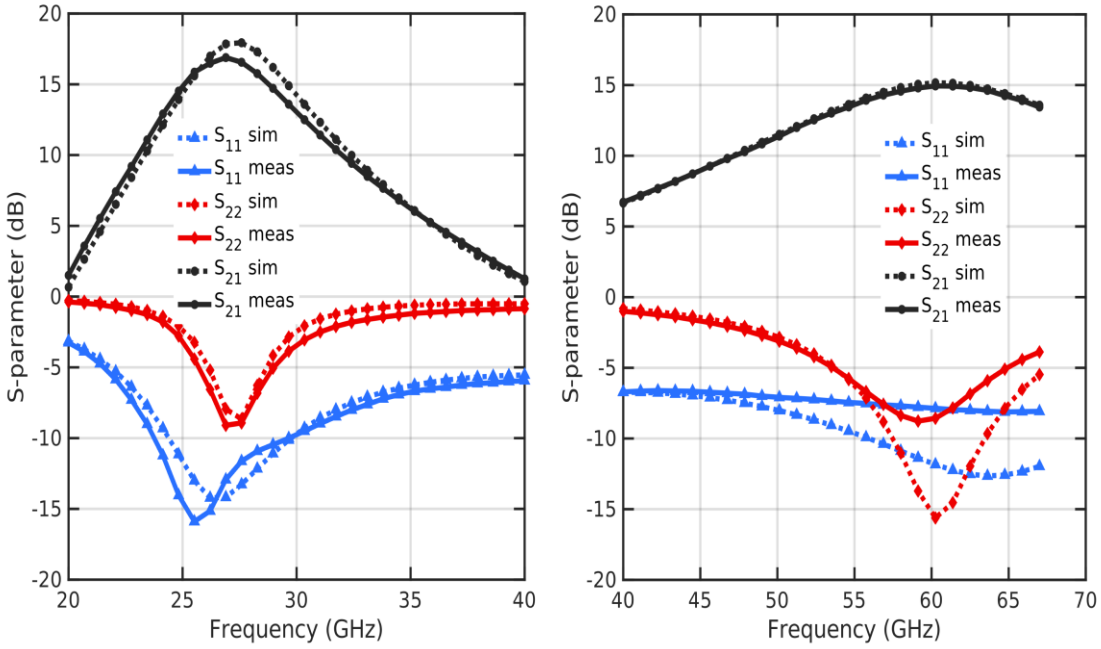


Figure 4-9 S-parameters at 28 GHz (left) and 60 GHz (right)

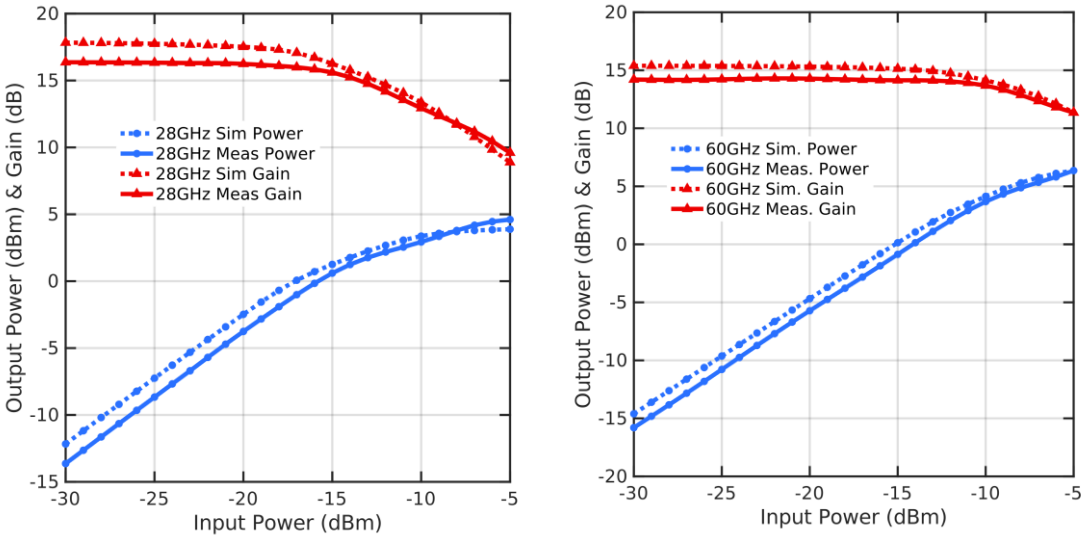


Figure 4-10 Output Power and Gain at 28 GHz (left) and 60 GHz (right)

The noise figure measurement setup at 60 GHz has been shown in Figure 4-12. A noise source with ENR around 17dB at 60 GHz has been used. Quinstar LNA with gain around 35dB and noise figure 4dB has been used to suppress the mixer and spectrum analyzer noise figure. Keysight smart mixer has been used to downconvert 60 GHz signal to IF which is within spectrum analyzer measurement range. The noise floor of spectrum analyzer itself has been mathematically subtracted by spectrum analyzer by using the "Noise Floor Extension" option in the spectrum analyzer. The losses of the cables and connectors have been measured using the Keysight E8257D signal generator. The signal generator has output power accuracy of ±1dB at 60 GHz (according to the manual). Therefore, there is 1dB uncertainty to the noise figure from signal generator. The writer is not sure about how to solve this problem and it is being ignore for this report. Spectrum analyzer resolution bandwidth has been set to 10 Hz with 512 samples average and an average detector. The noise output power measured by the spectrum analyzer fluctuates within ±0.2dB which also adds uncertainty of around ±0.2dB (exact amount can be calculated from Y-factor formula). The noise figure has been measured by using the Y-factor method and the noise associated with measurement setup has been de-embedded using the Friis formula. Figure 4-11

shows noise figure measured at 28 GHz and 60 GHz. Accuracy limits have also been plotted on the graphs. Note: these accuracy limits represent uncertainty only due to spectrum analyzer power measurement fluctuation. The uncertainty from the signal generator is being ignored for this report. Table 4-2 compares this LNA with the most recent single-band and wideband LNAs around 28/60 GHz frequencies.

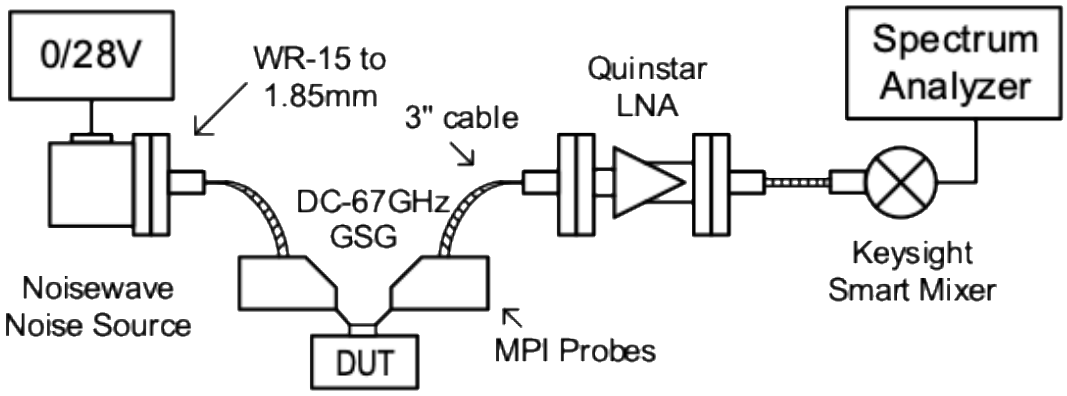


Figure 4-11 Noise Figure Measurement Setup at 60 GHz

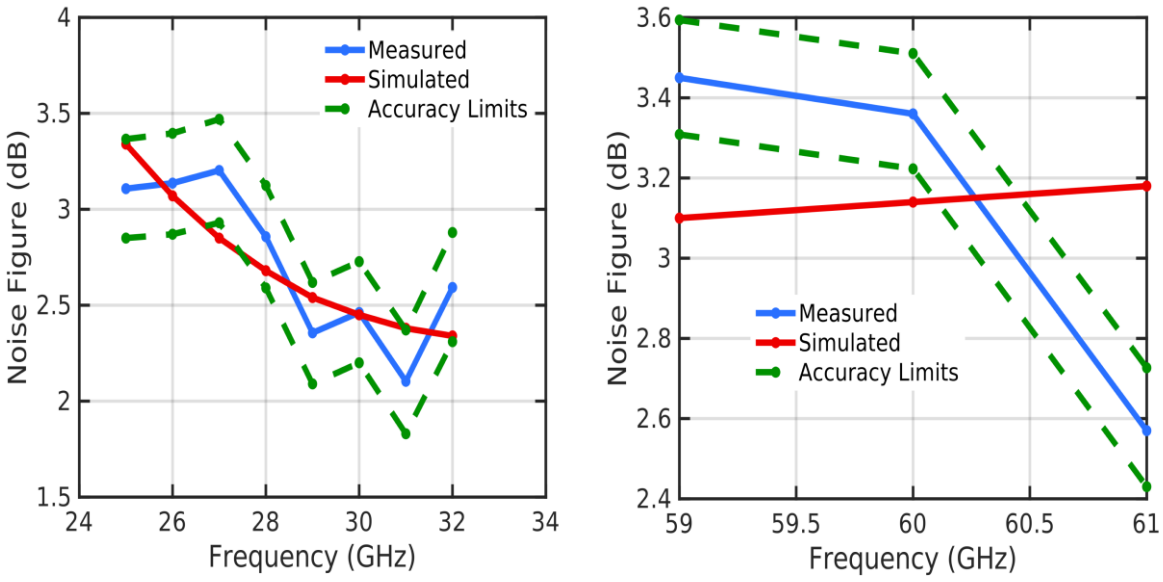


Figure 4-12 Noise Figure Plots at Ka-Band (left) and V-Band (right)

Table 4-2 State-of-the-art Single Band, Multi-Band and Wideband LNAs

Reference		Technology	Frequency (GHz)	Gain (dB)	Noise Figure (dB)	P1dB IN (dBm)	PDC (mW)
Dual-band LNA	This Work	130nm SiGe	28	16.2	2.8	-12	8.2
			60	15	3.4	-7	21
Dedicated Single Band LNAs	2017 IMS [27]	130nm SiGe	60	15	3.3	-13.5	19.6
	2015 RFIC [28]	40nm CMOS	60	12.5	3.8	N/A	20.4
	2015 RFIC [29]	32nm SOI	60	21	3.3	-24	18
	2007 MWCL [30]	120nm SiGe	28	17*	2.6	N/A	11
	2018 IMS [31]	45nm SOI	28	12.8	1.4	N/A	15
Wideband LNAs	2013 SiRF [32]	180nm SiGe	13.5/24/35.5	22.3/24.6/22.2	3.7/3.3/4.3	N/A	36
	2018 GSMM [33]	45nm SOI	22-44	18-20	4.2-5.5	N/A	58

*deduced from plots

4.2.5 Summary

A band-switchable LNA operating in 28 GHz and 60 GHz mode is presented. The LNA employs cascode topology, LC tank at input matching network and tunable stub at the output matching network to shift the frequency of operation between 28 GHz and 60 GHz. Performances in each band are comparable to single band state of the art LNAs. The designed LNA is suitable for 5G transceivers or dual-band phased array radars.

4.3 Band-Switchable TRX Amplifier with Integrated Switches

The PA and LNA designed in previous sections have been put together to form a band-switchable TRX (transmit-receive) amplifier. The T/R switches have been co-designed with the LNA and PA which results in compact die area compared to the conventional SPDT switch. The block diagram is shown in Figure 4-13.

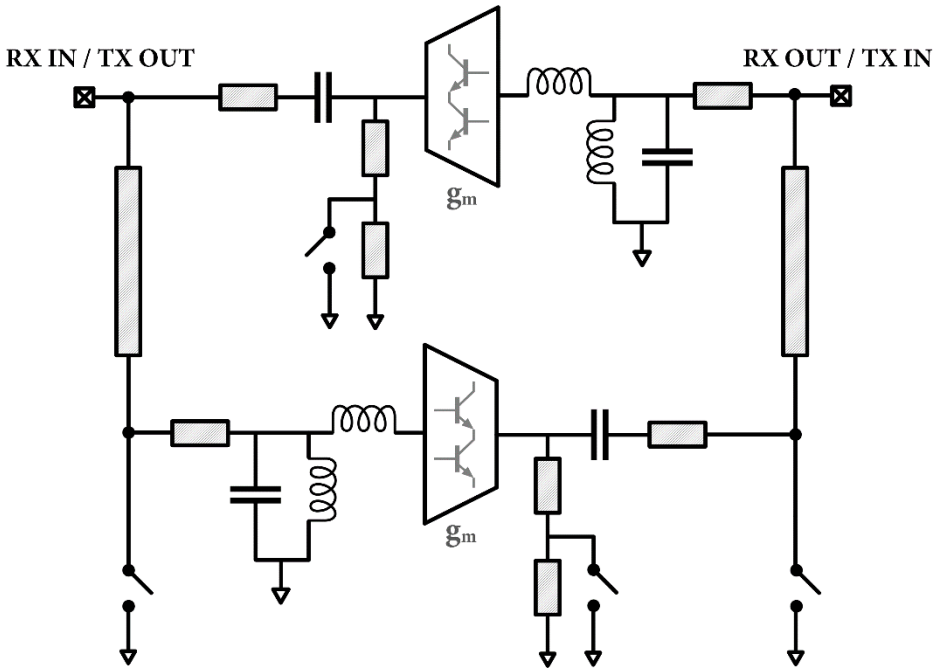


Figure 4-13 Conceptual schematic of the proposed amplifier

4.3.1 T/R Switch

Co-design of the LNA, PA and T/R switch enables the incorporation of the switch matching network into the design of the LNA and the PA, minimizing area and losses. The schematic of the T/R switch is shown in Figure 4-14. The T/R switch consists of two quarter-wave long transmission lines, TL1 and TL2, and one transistor switch. This approach is similar to SPDT switch design but different in terms that:

1) It only uses one transistor switch
2) It has more design optimization potential as the switches are integrated with other blocks allowing trade-offs
3) The output routing from the amplifiers can be used as transmission line segments leading to a very compact design

As the circuits in the 60 GHz band have relatively high noise figure and less gain compared to the 28 GHz band, the design choices (lengths and widths of TL1 and TL2) are made in favor of 60 GHz band to achieve reasonable performance in both bands. In TX mode, the LNA is turned OFF and the T/R switch (T7) is ON. The low impedance of switch is transformed to high impedance looking through the quarter-wave line (TL1). This is represented by the impedance Z1. Ideally, we would like to make Z1 an open-circuit, so that LNA does not load the PA at all. However, with the inherently narrow-band quarter-wave line, this is only possible at one frequency band. To present high Z1 at both bands, the length of the line is optimized through simulations and illustrated on the Smith chart in Figure 4-14. A length of 800 um (about 97° at 60 GHz) and width of 15 um (about 54 W) is chosen for TL1 which presents simulated insertion loss of 2.2 dB 28 GHz and 1.1 dB at 60 GHz. Please note that loss at 28 GHz is higher by design choice to favor 60 GHz. In RX mode, the PA and the T/R switch are turned OFF. The OFF-capacitance of the switch is absorbed

in the LNA matching network. The output routing from the PA has been meandered to form another quarter-wave line (TL2). This line transforms the OFF-impedance of the PA to a high value, and prevents the input signal from being loaded by the PA. A length of 750 um (about 91° at 60 GHz) and width of 15 um (about 54 W) is chosen for TL2 which presents simulated insertion loss of 1.1 dB 28 GHz and 1.5 dB at 60 GHz.

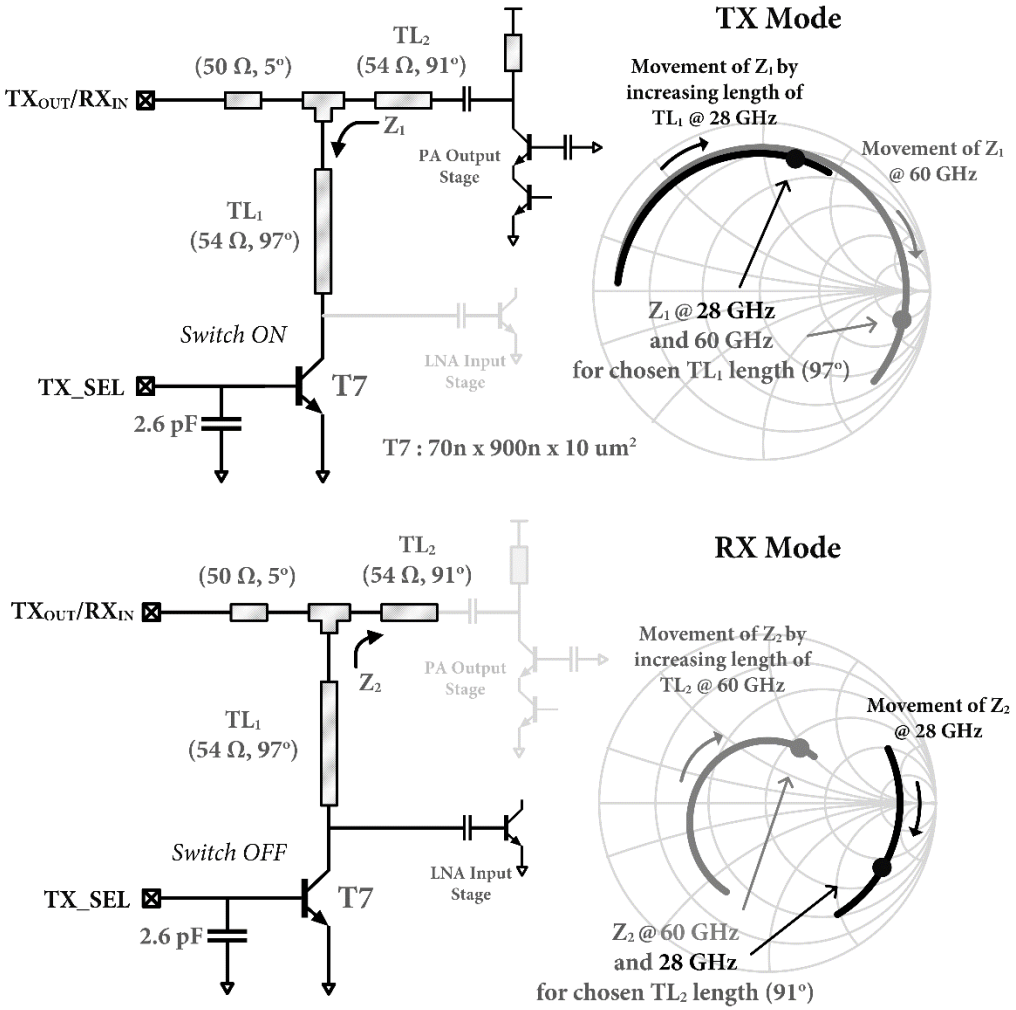


Figure 4-14 Schematic of the T/R switch incorporated into LNA and PA design.

4.3.2 Chip Photo

A layout picture of the designed TRX amplifier is shown in Figure 4-15. The chips take 890x685 um^2 area including the pads and 680x480 um^2 without pads.

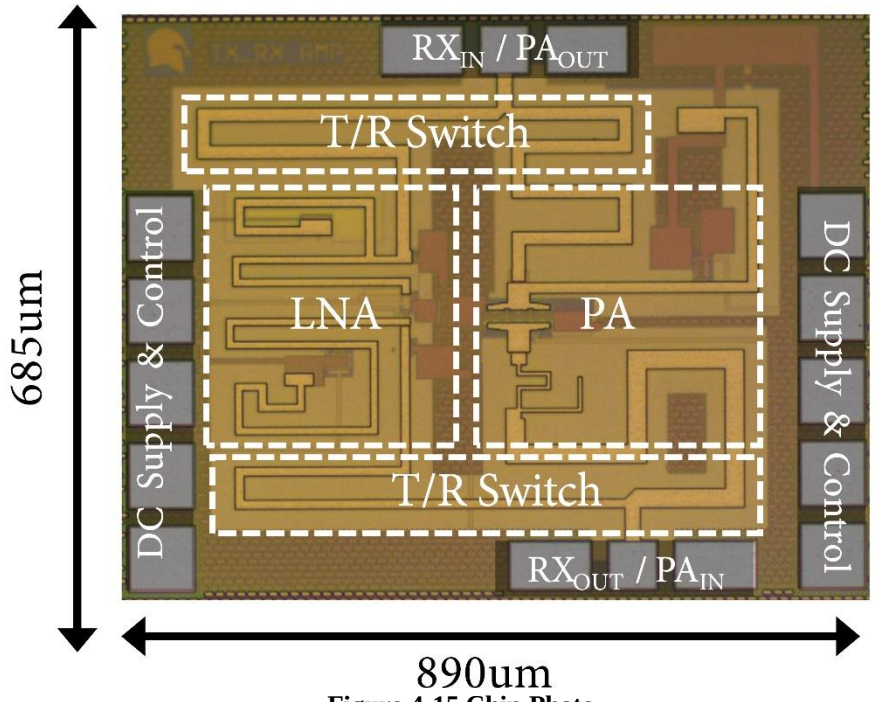


Figure 4-15 Chip Photo

4.3.3 Measurements

The noise figure setup has been shown before. The measured noise power fluctuates by ±0.1 dB which results in ±0.2 dB uncertainty in the Y -factor. Figure 4-16 plots the noise figure at 28

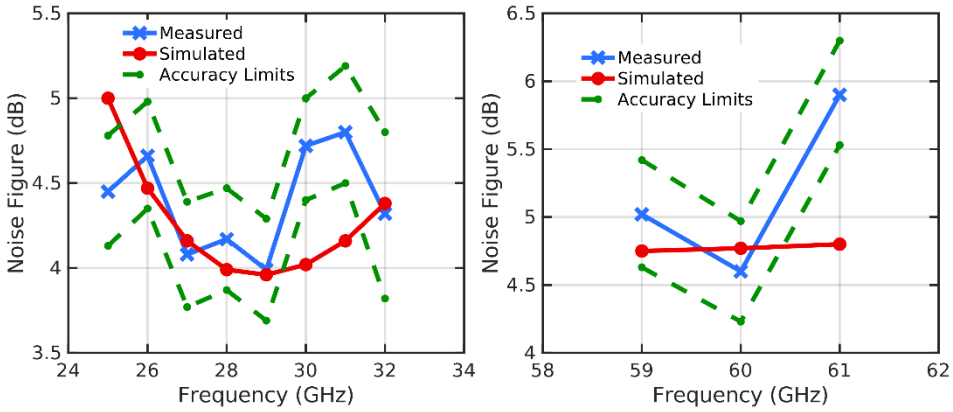


Figure 4-16 Measured Noise Figure

and 60 GHz band with ±0.2 dB uncertainty in the Y-factor, which is shown as accuracy limit in the plots. Small signal measurements have been performed using the Keysight N5227A power network analyzer (PNA) from 0.1 MHz to 67 GHz range. The PNA was calibrated using SOLT standards. Figure 4-17 shows simulated and measured s-parameters of the chip. The exact values of gains and return losses are listed in Table 4-3. The large signal measurements have been performed by exciting the input with PSG and measuring the output using EXA. The input power has been swept and output power along with gain and PAE have been measured and reported in Figure 4-18 for TX and in Figure 4-19 for RX. Due to the measurement setup, there is measurement uncertainty of ±0.2 dB in the output power. Also reported in the figures are OIP3 and IIP3 measurements for two tone spacing of 10 MHz. The exact values of measured results have been listed in Table 4-3.

Overall, the measured results agree well with simulations for all the measurements reported. However, some discrepancies can be seen such as the measured gain at 28 GHz band is 1.1 dB lower for RX and 1.6 dB lower for TX. Also, the measured output P1dB at 60 GHz is 2 dB lower for RX and 2.5 dB lower for TX. Authors believe these deviations come partly from imperfect EM modelling of the layout, partly from the transistor model in saturation region and process variations.

Table 4-3 compares this transmit-receive amplifier with the most recent multi-band amplifiers around 28/60 GHz frequencies. The designed amplifiers show state-of-the-art performance in terms of noise, output power and efficiency while including the loss of two T/R switches. A promising dual-band performance is achieved by minimizing switch loss, and small die area is achieved by integrating T/R switches into the amplifiers.

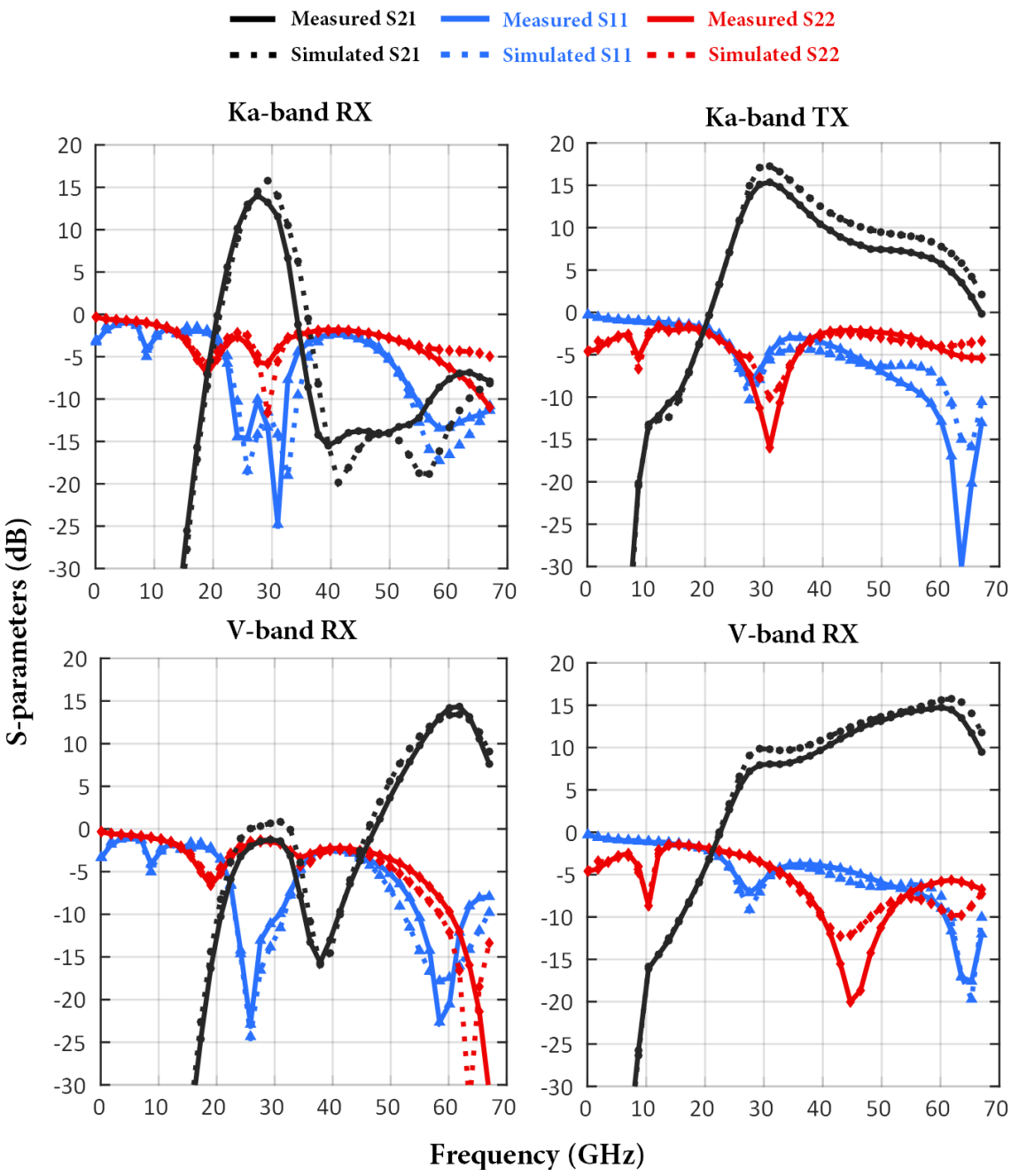


Figure 4-17 Measured s-parameters

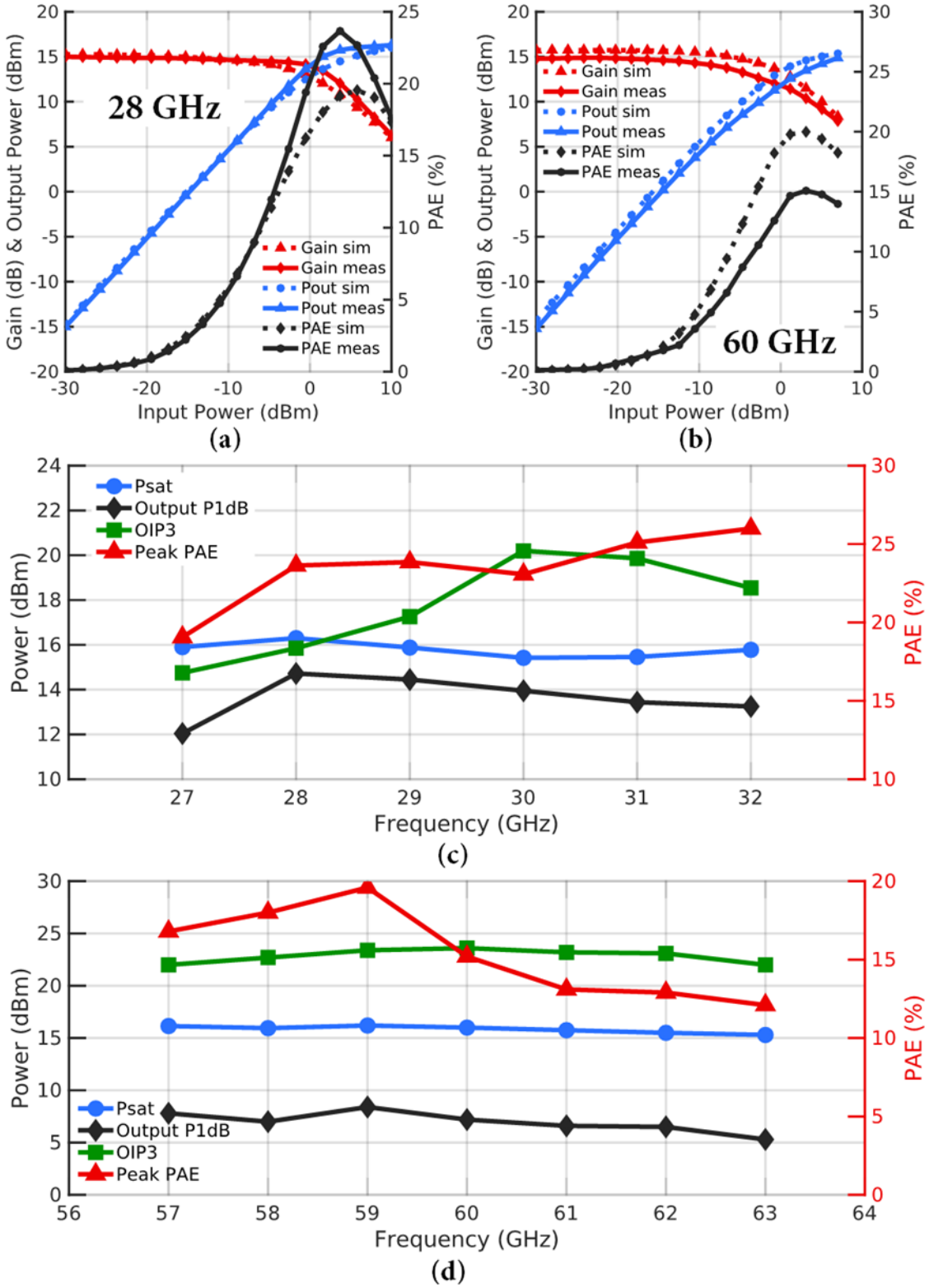


Figure 4-18 Large Signal Transmit Performance

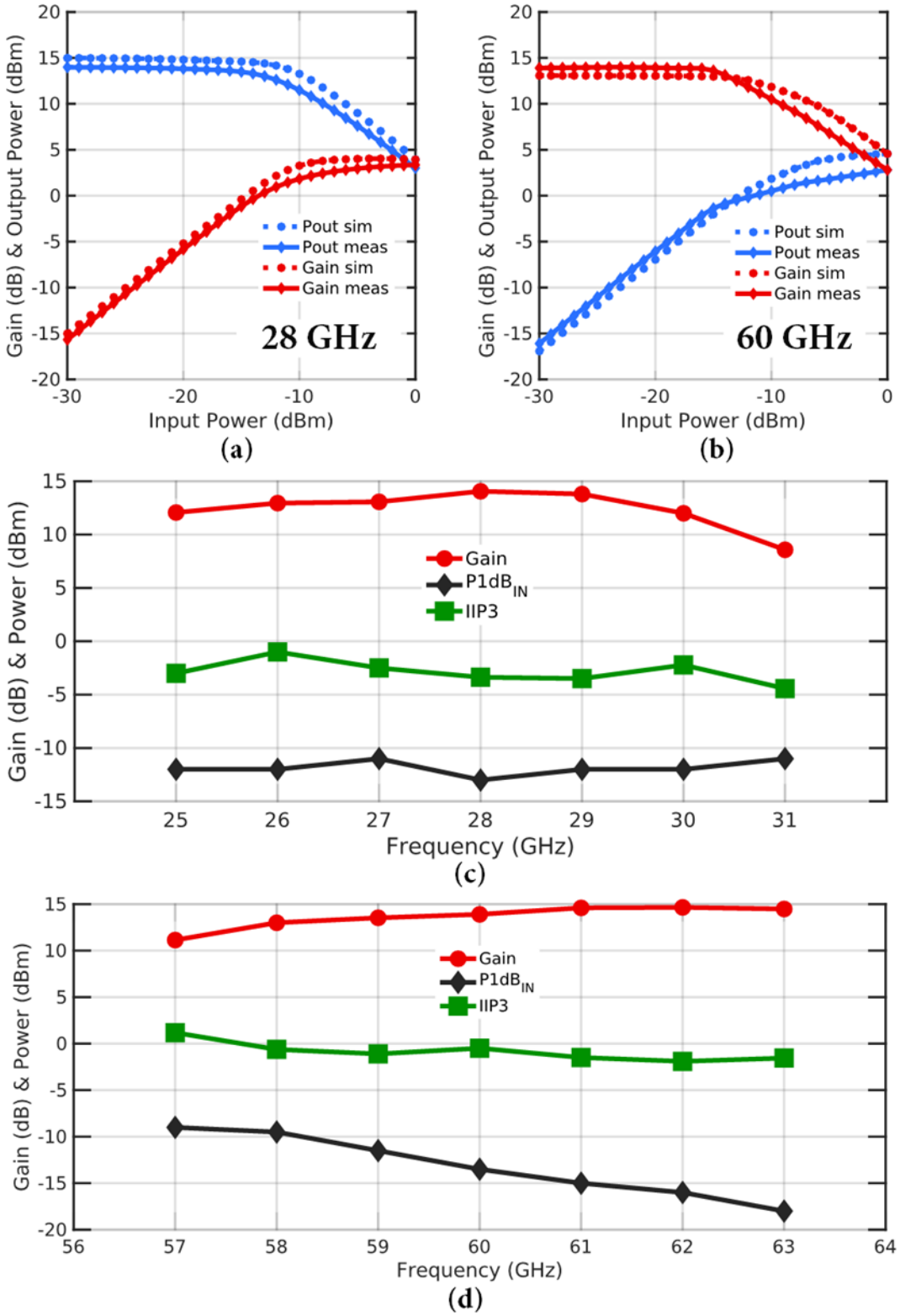


Figure 4-19 Large Signal Receive Performance

Table 4-3 Performance Summary and State of the Art

	Process	This Work 130nm SiGe		[35] ISSCC'19 65nm CMOS			[36] IMS'19 28nm CMOS			[37] CSICS'15 90nm SiGe
	Frequency (GHz)	28	60	28	38	60	28	38	60	70
RX	Gain (dB)	13.9	14.1	16.1	10.9	8.3	-	-	-	9.6
	NF (dB)	4.2	4.6	6.2	7	7.9	-	-	-	8.6
	S_{11} (dB)	-10.4	-22	-13.2	-15.1	-12.8	-	-	-	-
	$P1dB_{in}$ (dBm)	-13	-13.5	-15.7	-14.5	-12.8	-	-	-	-
	IIP3 (dBm)	-3.4	-0.5	-	-	-	-	-	-	-
	DC Power (mW)	10	24	37.6			-	-	-	21
TX	Gain (dB)	14.1	14.7	28.5	25.2	20.3	22	38	12	14.5
	S_{11} (dB)	-8.2	-9	-	-	-	-	-	-	-
	P_{sat} (dBm)	16.3	16	15.8	16.8	16.7	11	14	10	7.2
	$P1dB_{out}$ (dB)	14.7	7.2	14.1	15.2	13.5	-	-	-	-
	Peak PAE (%)	23.6	15.2	15	18.8	14.9	-	-	-	-
	OIP3 (dBm)	15.8	23.6	4	5	6	-	-	-	-
	DC Power (mW)	31.5	63	116.2			430			85
	Area (um^2)	0.4		0.48			0.87 (with pads)			0.646 (with pads)
	Functionality	Bi-directional		Bi-directional			Transmitter			Bi-directional

4.4 Conclusion

The loss of switches at mm-wave frequencies is typically expected to be high and it still remains elusive to circuit designers whether the switches are worth using at these frequencies. This chapter makes an effort to address this issue by presenting a 28/60 GHz transmit-receive amplifier which employs four switches for frequency and operational mode control. The switches are utilized in shunt configuration; they are co-optimized and integrated with the amplifiers to reduce area and matching network losses. Theoretical analysis on switch loss is presented and guidelines have been given to reduce loss. The switch achieves simulated ON-loss of a dB at 60 GHz, thereby enabling the transmit-receive amplifier to exceed state-of-the-art performance. Thanks to the low-loss switches, multi-band and reconfigurable mm-wave electronics can be realized using simpler circuits.

5 A 18-50 GHZ RECONFIGURABLE MIXER-FIRST RECEIVE RF FRONT-END

This chapter presents the design of 18-50 GHz receive RF frontend. Such a receiver finds applications in military communications where the frequency of a transceiver needs to be reconfigured to avoid jamming and de-sensitization in a hostile environment. It can also be used for multi-band applications like 5G where different mm-wave bands are used in different regions of the world or for reconfigurable applications like phased array radars where different frequencies can be utilized to get different range/resolution settings.

5.1 System Specifications

Table 5-1 Specifications of Required 18-50 GHz RX

Metrics	**Specifications**
Frequency Range	18 – 50 GHz
Instantaneous RF Bandwidth	200 MHz
Voltage Gain	17 dB
Integrated DSB Noise Figure	8 dB
IIP3	4 dBm
Baseband Filter Passband	DC-100 MHz
Baseband Filter Passband Ripple	1.5 dB
Baseband Filter Stopband Attenuation	-20dBc at 300 MHz
Max DC Power Consumption	≤ 72 mW
Max Chip Area	500 x 700 um^2
LO/RF Input Return Loss	≥ -10 dB
LO Input Power (Differential)	0 dBm

This project is part of DARPA Millimeter Wave Digital Arrays (MIDAS) program [34] and required specifications of the desired receiver are given in Table 5-1.

5.2 System Design

The most challenging requirement of this project is to achieve high linearity (21 dBm OIP3) in a small size and power budget. A receiver's IIP3 and NF are dictated by LNA. If LNA has high gain, it suppresses noise figure of subsequent blocks. However, it also suppresses IIP3s of subsequent blocks and consequently they need to be designed for very high IIP3 in order to improve the overall IIP3 of the cascade. While do-able, this requires high DC power consumption and IM3 cancellation techniques. Therefore, if a highly linear receiver is desired, it is natural to remove the gain of very first stage in cascade, which means removing the LNA. Such receive topologies are called mixer-first receivers because mixer is the very first block of the receiver with no LNA before it. The challenge in designing such receivers is to maintain a smaller noise figure as there is no LNA now to suppress the noise of mixer and baseband stages. To reinforce the importance of mixer-first receivers, Figure 5-1 shows that overall IIP3 of receiver is reduced a lot when LNA and subsequent receive chain is cascaded. LNA and subsequent RX chain IIP3s are assumed to be 10 dBm which is an optimistic choice and the 17dB required gain is distributed between LNA (7 dB) and subsequent chain (10 dB).

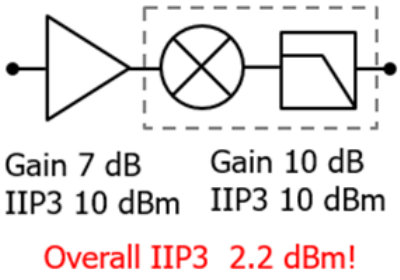


Figure 5-1 IIP3 Degradation by the Gain of LNA

Existing mixer-first receivers employ passive mixers with 4-phase mixing. For example, Figure 5-2 shows a 4-phase mixer-first receiver which operates in 0.05-2.4 GHz frequency range [35]. The mixer switches employ 25% duty cycle LO and each switch is turned ON one instant at a time. This way the input node of I and Q mixers can be connected to each other without needing any isolation network. Also, since passive mixers have no reverse isolation, it means they can also upconvert baseband voltage (at IF side) to RF voltage (at antenna side.) This property can be utilized to form a bandpass filter at the input by programming the low-pass impedance terminations at baseband (IF side of mixer). This property can also be used to present 50 Ω input at RF side by controlling the baseband impedance, thus eliminating the matching network. It is important to mention that these properties exist if the baseband time constant (means RC product of baseband impedance) is very large compared to LO cycle which is generally true as LO is at much higher frequency in direct-down conversion or low-IF receivers. This large time constant acts like a

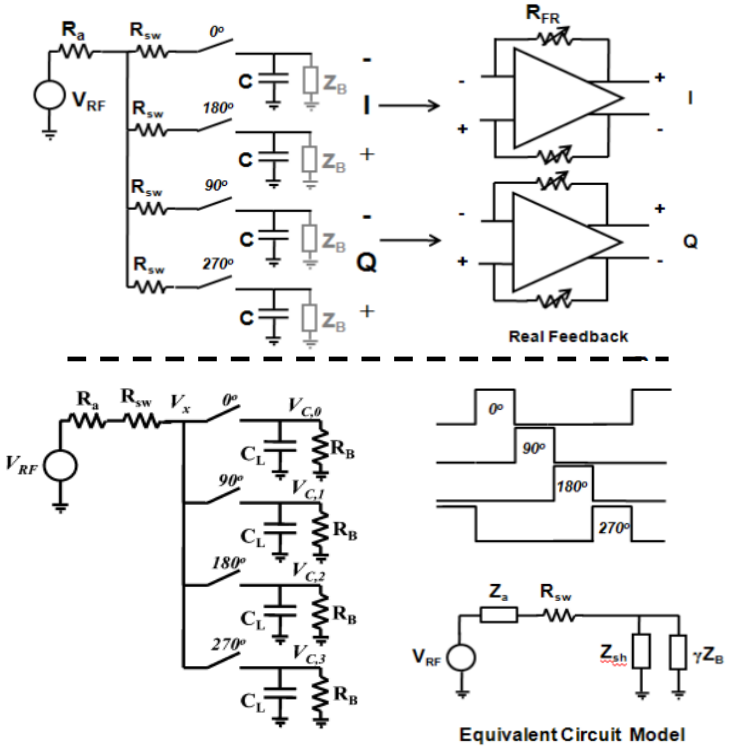


Figure 5-2 A 0.05-2.4 GHz 4-Phase Mixer-First Receiver [35]

sampler and holds the voltage across the capacitor over the LO cycle. It can be shown [35], the voltage V_x (shown in Figure 5-2) then takes the shape of staircase function. The spectrum of this staircase function shows presence of LO harmonics. These LO harmonics result in harmonic currents from baseband to antenna (by the virtue of no reverse isolation) causing an additional loss and increase in noise figure. This is usually modelled by a shunt resistor in parallel with baseband impedance. The whole circuit action can be modelled as an LTI system with equivalent circuit model shown in Figure 5-2. Noise introduced by presence of LO harmonics at the baseband voltage V_x can be reduced by controlling the antenna impedance at harmonics of LO. If antenna's impedance can be made high at these harmonics, then there is no current flow from baseband to antenna at RF resulting in no loss. However, antenna's impedance may not always be in designer's control as they usually are resonant structures behaving like a shunt LC tank, and therefore provide low impedances at harmonics. Therefore, 8-phase or higher order mixing may be employed to reduce LO harmonics at the baseband. This way noise contribution from LO harmonics is minimized.

Four phase mixer-first receivers have also been demonstrated at mm-Wave frequencies. However, the very properties of the 4-phase mixing approach like no input matching required, no isolation required, wideband operation and formation of bandpass filter at RF side are somewhat lost. Parasitic capacitance of mixer switches appears in parallel to the up-converted impedance of baseband, thus reducing its effect and limiting the impedance tuning range. This parasitic capacitance also provides low impedance to LO harmonics and increases their noise contribution. An inductor is used to resonate this capacitance out which also makes it narrowband. Figure 5-3 shows a 20-30 GHz 4-phase mixer [36]. Since it is very power consuming to provide square wave drive to the mixer switches at mm-Wave frequencies, usually sinusoidal drive is provided.

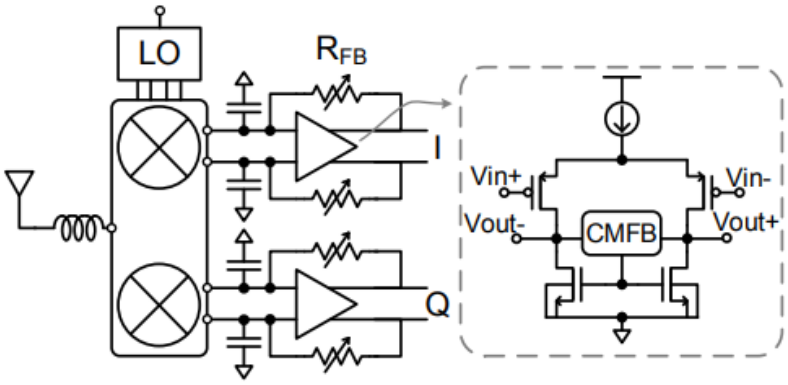


Figure 5-3 A 20-30 GHz 4-Phase Mixer-First Receiver [36]

However, 4-phase sinusoidal CLK generation becomes an issue and also requires a decent amount of DC power. In [36], 4-phase CLK is generated by consuming 30 mW of DC power. The LO is split to a differential quadrature using passive RLC circuits. The resulting 50% duty cycle waveforms are then buffered and passed through a transmission gate controlled by adjacent quadrature clocks to create the non-overlapping 25% duty cycle waveforms. Figure 5-4 shows this circuit. This receiver achieves 8 dB noise figure, -9.7dBm IIP3 and 20.6 dB gain using 41 mW power.

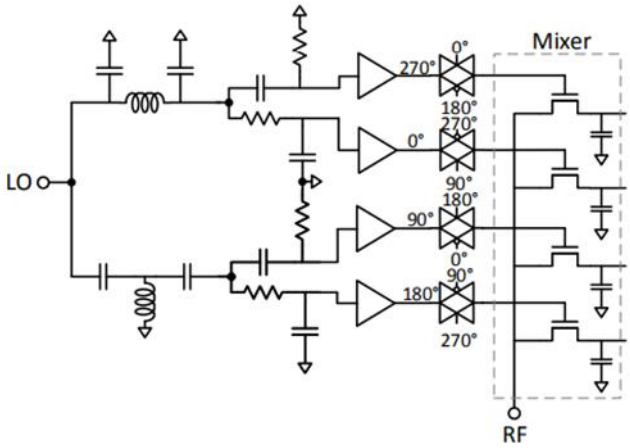


Figure 5-4 A 20-30 GHz 4-Phase CLK Generation Circuit [36]

Previous study shows that while 4-phase mixing is a good solution at RF frequencies, it potentially loses some of its benefits at mm-Waves and besides generating 4-phase CLK becomes very power-hungry task at these frequencies. Therefore, our proposed mixer-first receiver employs 50% duty cycle. However, as hinted earlier, 50% duty cycle I & Q mixers cannot be directly

connected at input node without needing isolation network which we solved by putting quadrature coupler before the mixers. This coupler also provides wideband input matching eliminating the need of matching networks.

The proposed receiver is designed using 45nm CMOS SOI process. The block diagram of the receiver is shown in the Figure 5-5. The first block is wideband 18-50 GHz quadrature coupler which is at the receive input. In addition to splitting the RF input into quadrature (I & Q), the coupler also provides near perfect match at the input by cancelling the reflected waves from I and Q port which arrive at the input with opposite phase but same magnitude. This way, there is no need to interpose a matching network between the coupler and the next RF block to prevent reflections. The second block is a double-balanced passive mixer which down-converts the RF signal to IF and cancels the LO and RF feedthroughs from input to output due to double-balanced topology. Passive mixer is employed for high linearity and low flicker noise. The mixer is driven

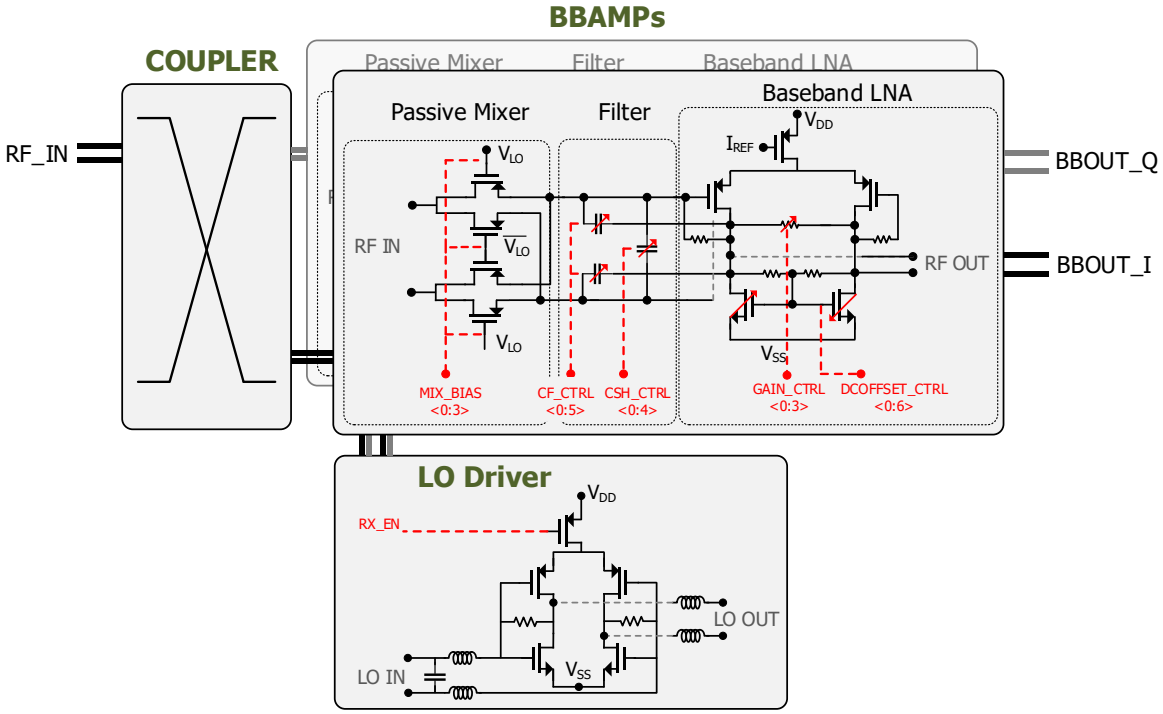


Figure 5-5 Block Diagram of Designed 18-50 GHz Receiver

by a broadband LO driver which is based on complementary common-source amplifier. The third stage is a baseband LNA with integrated low pass Sallen-Key filter. The filter is composed of common source PMOS amplifier with NMOS active load and local common mode feedback. Digital control for filter response, amplifier gain, mixer bias and DC offset calibration has been included. The details of each block in the receiver are given below.

5.3 Differential Quadrature Coupler

A quarter-wave transmission-line based coupler is designed to ease in bending around the lines to fit into the layout and to provide broadband response by over-coupling the lines. The coupler employs broadside coupled differential transmission lines as shown in Figure 5-6.

The design procedure starts with a quarter-wave long line at geometric center frequency (30 GHz) of the desired band (18-50 GHz). This results in a perfect coupler with 0 dB amplitude mismatch and 90 degrees phase difference between I and Q only at very narrow band around 30 GHz. To enhance the BW, the coupler with different center frequencies can be designed and cascaded. This approach is called multi-section coupler and takes considerable IC area. Another approach is to specify target amplitude mismatch and quadrature phase mismatch and adjust the coupling between broadside coupled lines. By over-coupling the broadside coupled lines within the target specs, a wideband response can be achieved and then the BW is defined over which the target specs are met. The over-coupling can be achieved by selecting the right metal layers in the stack for a given process. This requires several iterations with the different metal layers. Figure 5-5 shows the chosen metal layer for this process (45nm SOI) are UA and C2. Metal UA is 1.2um thick whereas C2 is 0.175 um thick only. In order to reduce loss of C2 metal, it is stacked with

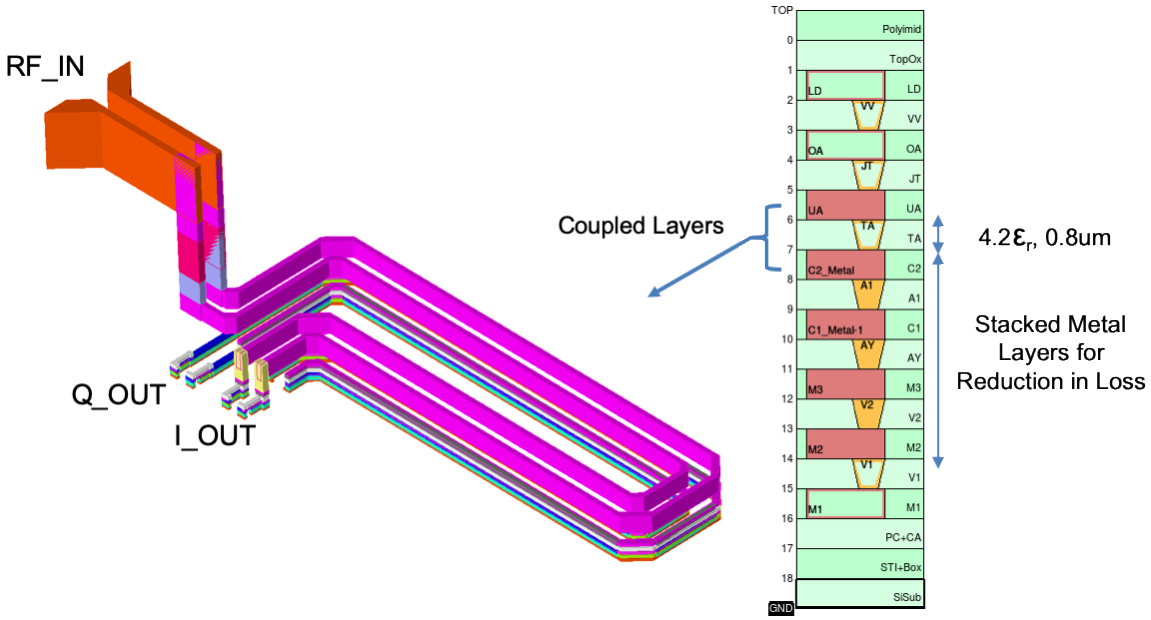


Figure 5-6 Quadrature Coupler

lower metals all the way down to M2. The target specs for this design are 1.5 dB amplitude balance and ±5 degrees quadrature phase imbalance. Figure 5-7 shows the simulated response of designed 18-50 GHz coupler which achieves 1.5 dB amplitude imbalance and less than 5 degrees quadrature phase imbalance. It has maximum excess loss of about 2 dB at 50 GHz.

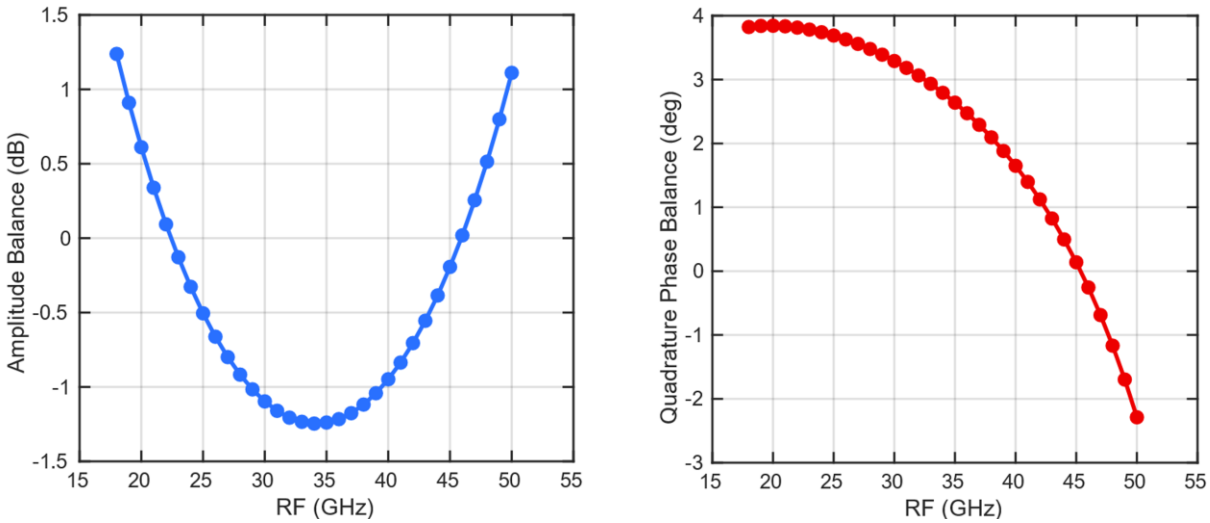


Figure 5-7 Simulated Amplitude and Phase Imbalance of Quadrature Coupler

Since the quadrature coupler forms the very first block of proposed receiver, therefore it's noise figure directly adds to overall noise figure of receiver. However, we do not include split loss in noise figure calculation as that loss is eventually recovered when I and Q signals are added back to form the original signal. Therefore, we assume coupler's noise figure to be equal to its excess loss only. On the other hand, IIP3 of the receiver is also directly improved dB by dB from the coupler's loss (excess + split). It is interesting to note that IIP3 improvement also includes improvement due to split loss, but noise figure degradation does not include split loss degradation.

5.4 Passive Mixer

The passive mixer has been chosen over the active mixer topologies because of:

- Low flicker noise: passive mixer is biased near threshold voltage and zero drain-source voltage, therefore there is no static current flowing through it which reduces the flicker noise.
- High linearity: passive mixers do not have any transconductance device which is the main source of non-linearity in active topologies. Instead, passive mixers use transistors as switches and the linearity depends on the ON impedance variation with input signal.
- No power consumption: passive mixers don't consume any DC power.

Figure 5-8 shows the designed passive mixer. PMOS transistors with smallest length have been used as they provided slightly smaller flicker noise compared to NMOS transistors. The size and bias optimization of passive mixer is presented below.

A two-phase passive mixer can be modelled as an LTI system as shown in Figure 5-9 [37]. This model assumes that antenna impedance is fixed which means same impedance at harmonics. Let's compute the values of γ and R_{sh} for N=2 and N=4.

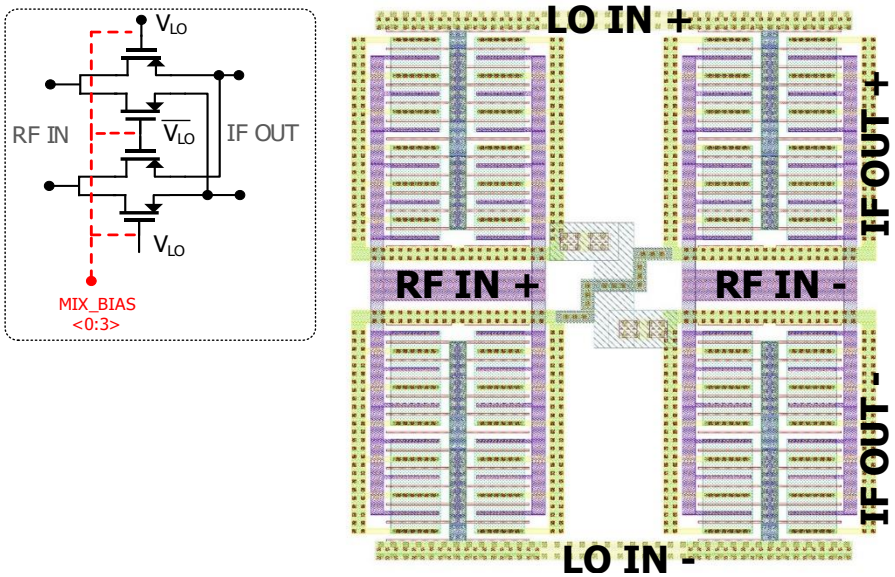
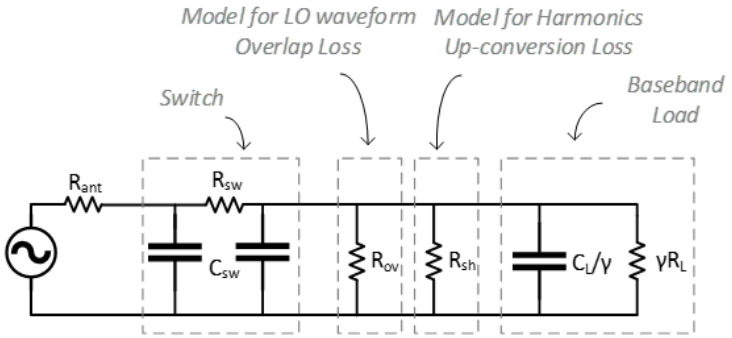


Figure 5-8 Passive Mixer Schematic and Layout



$$\gamma = \frac{sinc^2\left(\frac{\pi}{N}\right)}{N} \quad \text{(where N is number of phases)}$$

$$R_{sh} = (R_{ant} + R_{sw})\frac{N\gamma}{1 - N\gamma} \quad \text{(assuming antenna impedance does not vary with frequency)}$$

$$R_{ov} = \frac{3}{\pi} \times \frac{NR_{sw}}{\omega_{LO}\tau} \quad \text{(where } \tau \text{ is the overlap period between LO phases)}$$

Figure 5-9 LTI Model of N-Phase Passive Mixer

For two phase mixing, N=2 => $\gamma \approx 0.203$ and $R_{sh} = 4.3\ (R_{sw}+R_{ant})$

For four phase mixing, N=4 => $\gamma \approx 0.203$ and $R_{sh} = 0.68\ (R_{sw}+R_{ant})$

This shows that while impedance transformation properties (γ) are similar between 2 and 4 phase mixing, the harmonic loss ($\propto 1/R_{sh}$) is much higher for two phase mixing. This has to do

with the fact that a switch in two-phase mixer is ON 50% of the time, resulting in more charge leakage. However, since generating 4-phase clock for 18-50 GHz is power and area hungry task, we have opted to use 2-phase clock.

Noise figure of passive mixer can be derived to be [37]:

$$F = 1 + \frac{R_{sw}}{R_{ant}} + \frac{R_{sh}}{R_{ant}}\left(\frac{R_{ant}+R_{sw}}{R_{sh}}\right)^2 + \frac{R_{ov}}{R_{ant}}\left(\frac{R_{ant}+R_{sw}}{R_{ov}}\right)^2 + \frac{\gamma R_L}{R_{ant}}\left(\frac{R_{ant}+R_{sw}}{\gamma R_L}\right)^2 + \gamma\frac{{V_a}^2}{4kTR_{ant}}\left(\frac{R_{ant}+R_{sw}}{\gamma R_L} + \frac{R_{ant}+R_{sw}+R_{ov}+R_{sh}}{R_{sh}}\right)^2$$

where v_a^2 is input referred noise voltage of baseband amplifier.

Above equation shows that to minimize noise figure, we need to decrease R_{sw} and increase R_{sh}, R_{ov} and R_L. R_{sw} can be decreased by increasing the transistor size. However, a too big transistor will also have shunt parasitic capacitor which would present low impedance to the LO harmonics present at baseband node. This results in more reverse or re-radiation current effectively reducing the value R_{sh} which increase the noise figure. Therefore, there is optimal size of switch that results in minimum noise figure. On the other hand, the gain of mixer keeps on increasing as the device size becomes larger. This is because parasitic switch capacitor is not big enough at fundamental frequency to produce any leakage effects whereas it is big enough for harmonics. Since R_{sh} is

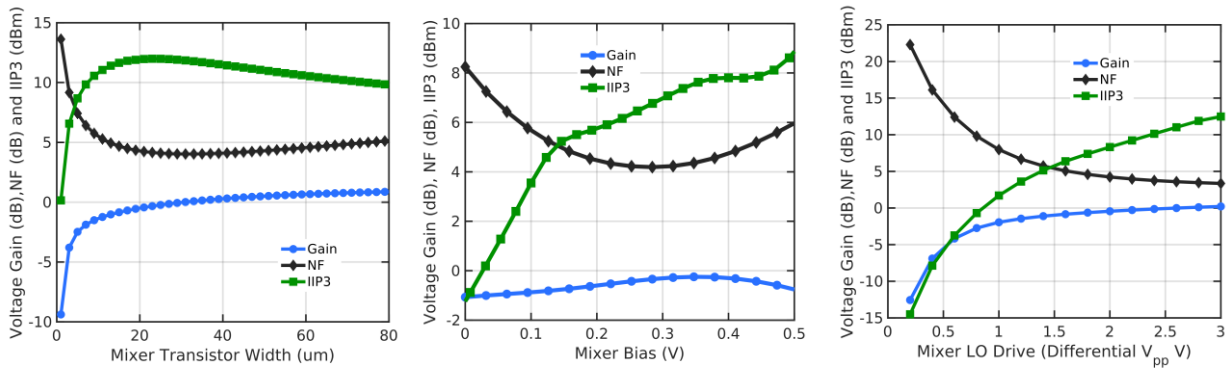


Figure 5-8 Mixer Gain, NF and IIP3 against Different Design Parameters

affected by harmonics, therefore noise figure is affected more by parasitic switch capacitor. These trade-offs are captured in Figure 5-10.

Passive mixers also show trade-off between noise and linearity against mixer bias. Increasing the mixer bias reduces R_{sw}, thus improving noise and linearity. However, Figure 5-10 shows that there is an optimal bias for minimum noise figure after which noise starts increasing with the bias. This is because mixer LO drive is sinusoidal and adding bias offset to it increases its duty cycle. Increasing duty cycle above 50% creates overlap between LO waveform. During these periods all mixer switches are turned ON wasting the input signal as it appears as common mode at output. It reduces signal gain and increases noise figure. However, since by adding DC offset, LO peak voltage is also increased which means switches undergo bigger overdrive and this produce lesser noise as R_{sw} reduces. These two effects counter each other with latter being dominant at low DC bias. As the bias increases further, overlap period between LO waveform increases and at one point dominates the noise figure. Therefore, an optimal bias point exist where the cumulative effect of both results in minimum noise figure. These effects can be modelled by another shunt resistor, R_{ov}, as shown in Figure 5-9. This R_{ov} is dependent on mixer bias and will have highest value at optimal bias.

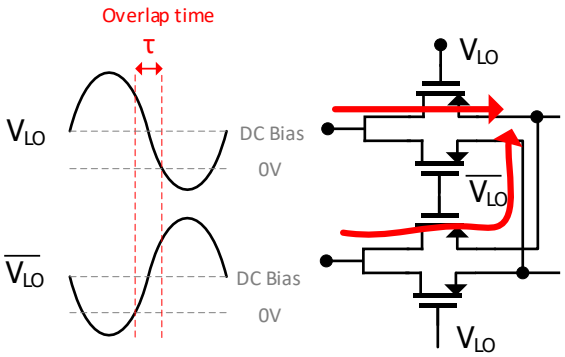


Figure 5-9 Effects of Adding DC Bias to Sinusoidal LO Drive

As far as LO drive is concerned, mixer's performane increases as the LO drive increases. Figure 5-10 shows that increasing LO drive increases gain and iip3 whereas noise figure is reduced. However, providing wideband 18-50 GHz LO drive to mixer capacitor is very challenging and power hungry task. Therefore, eventually mixer's size is determined by its input capacitance for which sufficient LO drive can be provided.

Considering the trade-offs presented above, a size of 40um (width) has been chosen which results in 4.5dB double sideband noise figure, 8dBm IIP3 and 0.5dB insertion loss at 50 GHz. Since there is a direct trade-off between mixer's noise and linearity, a bias adjusting circuit has been included to optimize the mixer bias at different RF frequencies. At lower end of RF frequencies (18-30 GHz), coupler's loss is relatively smaller and therefore improvement in IIP3 is also smaller, we use higher bias to increase the mixer's IIP3 so that overall receiver's IIP3 is similar. On the other hand, at higher end of RF frequencies (30-50 GHz) mixer's noise figure is higher, we lower the mixer's bias to reduce noise figure. The bias voltage has been generated by using current DAC. Binary weighted current sources are controlled through series switches. When a switch is ON, additional current flows through the bias resistor (5.6 kΩ), creating more drop

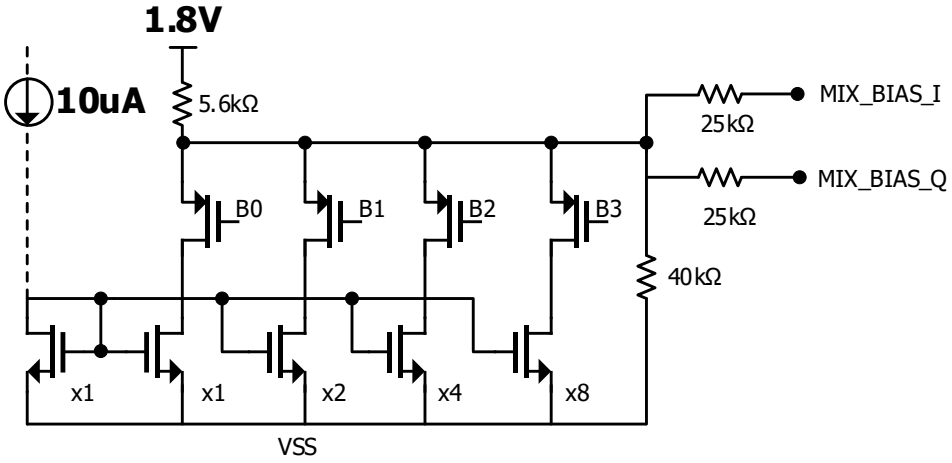


Figure 5-10 Current DAC for Mixer's Bias Adjustment

across it and hence changing the output voltage level. Figure 5-12 shows this circuit. We have used 4-bit control here which can provide 260:12:450 mV VGS range across mixer.

5.5 LO Driver

LO waveform must ideally be a square wave to ensure abrupt switching and hence maximum conversion gain. Since at mm-wave frequencies, it is very hard to generate square wave, the LO is usually a sinusoidal signal. As the sinusoids change gradually, there is substantial portion of the time where all of the mixer transistors are ON, treating RF as common mode input. That is, the input signal is "wasted" because it produces no differential component. The gradual rise and fall response may also raise the noise figure. Therefore, we choose a large LO signal so as to obtain a high slew rate and ensure a minimum overlap time where all the transistors turn ON. Also, high LO amplitude is desired to fully turn ON and OFF the switch in order to reduce insertion loss or improve isolation respectively. Therefore, an LO driver is inserted between mixer and LO to

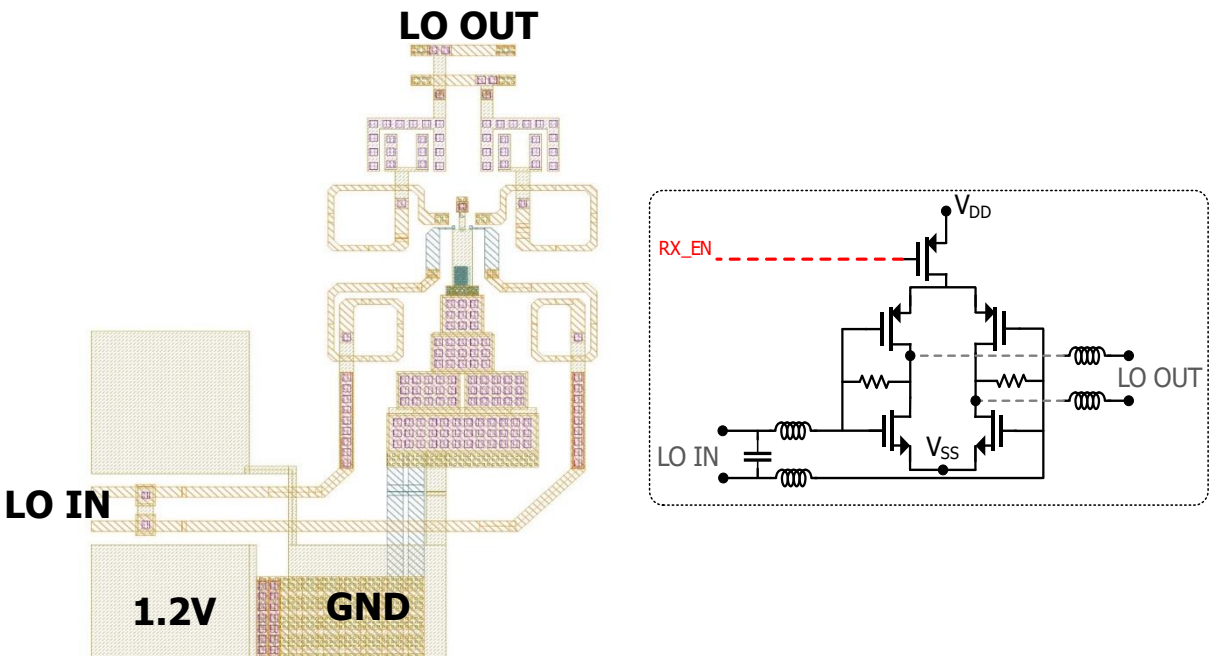


Figure 5-11 LO Driver Layout and Schematic

increase the LO signal. Based on mixer's IIP3 and NF simulations and transistors breakdown concerns, we set target LO swing of 2Vpp differential.

Figure 5-13 shows the LO driver schematic and layout. The LO driver uses complementary common source amplifier with resistive feedback. This amplifier eliminates the need for bias inductor and provides double g_m (compared to CS cascode). This topology is better than cascode as cascode provides low gain when loaded by mixer capacitance whereas complementary CS still provides higher gain due to double transconductance. Short-channel (40nm) thin oxide transistors have been used to get higher g_m and reduce parasitic caps. Since short-channel transistors have very small breakdown voltage (1.2 V), we would like to avoid creating any parallel resonance at transistors drains as it leads to increase in voltage swing across the transistors causing breakdown concerns. Therefore, eliminating the bias inductor (by using PMOS) proves helpful. Since this LO driver needs to drive gate capacitance of mixers, we can utilize series resonance for passive voltage amplification. It is known that in a series RLC resonator, the voltage across inductor or capacitor

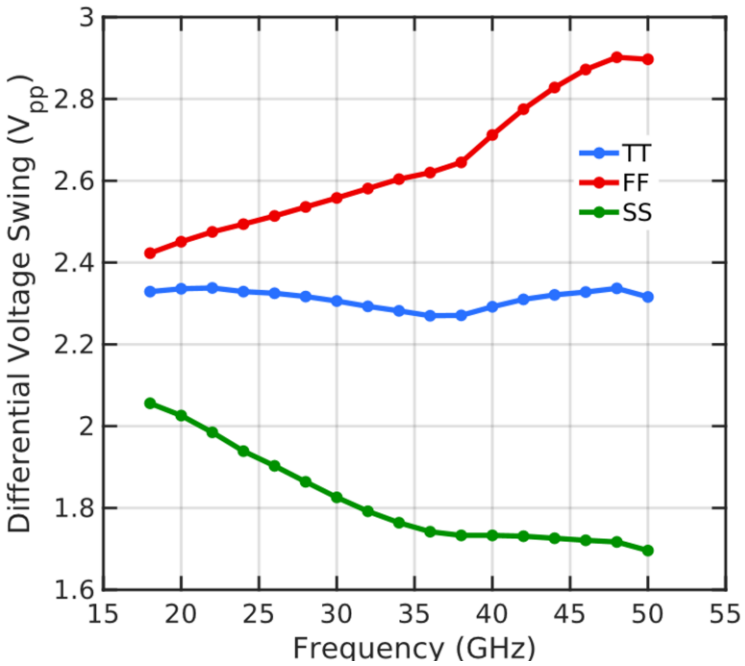


Figure 5-12 Output Swing of LO Driver

is Q times higher than voltage across resistor. A transistors output can be modelled as voltage source with a series resistor. Therefore, if we insert a series inductor between load capacitor and transistor output, it will behave as series resonator and enhance the voltage across capacitor by the quality factor of the network. A high Q-factor would give big voltage amplification but narrow bandwidth. Therefore, Q is reduced to get 2Vpp differential swing within 18-50 GHz bandwidth. Reduction in Q requires bigger size of transistors which increases the DC power consumption. Q can also be reduced by adding feedback resistor between drain and source, thereby sacrificing some gain. The feedback resistor and load capacitor also generate broadband real part at the input impedance of the driver. Therefore, input can be broadband match with just a single LC section. A series PMOS switch has been added in VDD path to turn OFF LO driver in power down mode of receiver. Figure 5-14 shows the desired and achieved output voltage swing for different process corners at 0 dBm input power.

5.6 Baseband LNA and Filter

The baseband amplifier is required to suppress the noise of ADC and amplify the signal to the full scale of ADC so that ADC operates at its maximum SNDR. An anti-aliasing low pass filter is also integrated to remove the frequency contents in the signal past the Nyquist frequency. The baseband amplifiers consist of common source stage with PMOS input transistors, NMOS as active load and local common mode feedback. Positive feedback capacitor and shunt capacitor at input is added to create a ‘resistor-less’ Sallen-key filter. Figure 5-15 shows the schematic of baseband amplifier.

5.6.1 Flicker Noise Optimization

Since flicker noise is a big issue in direct-conversion receiver, we were required to reduce flicker noise corner as much as possible. Flicker noise of a MOSFET is represented at the gate and given by following expression:

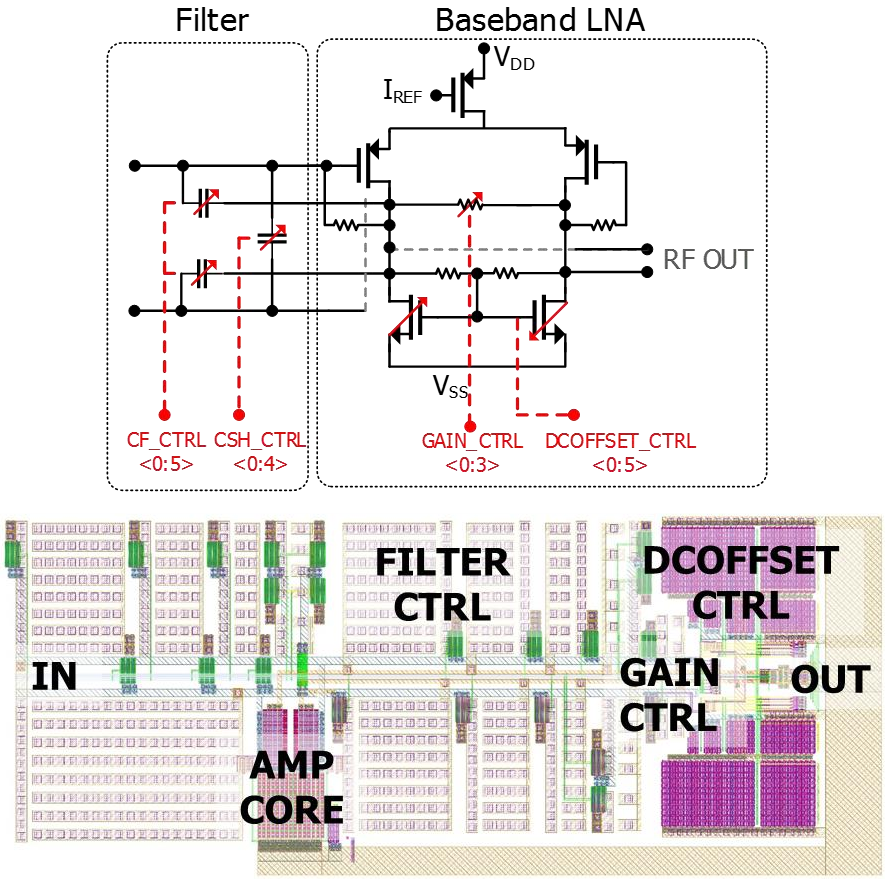


Figure 5-13 Baseband LNA with Integrated Sallen-Key Low Pass Filter

$$V_n^{\,2} = \frac{K}{WLC_{ox}}\frac{1}{f}$$

Above expression shows that the flicker noise of MOS transistor is inversely proportional to size and oxide thickness. Increasing the transistor size (both length and width) and using thick oxide reduces the flicker noise corner. A thick oxide 112 nm PMOS input transistor has been chosen as input transistor of baseband amplifier. This transistor provided the lowest flicker noise corner

compared to other transistors in the PDK. A size of 250 um is chosen to reduce the flicker noise as much as possible while remaining within the power budget. Similarly, size of NMOS load transistor is chosen to be 300 um wide and 2 um long. Bigger length allows higher output impedance at the cost of higher overdrive voltage.

5.6.2 Thermal Noise Optimization

Thermal noise in MOS arises from its channel noise which for long channels can be given as:

$$V_n^{\,2} = 4kT\gamma g_m$$

Channel charge fluctuation also gives rise to induced gate noise which is correlated to channel noise. However, we will consider channel noise here only. Since channel noise voltage is proportional to square root of g_m and signal gain is directly proportional to g_m, we would like to increase g_m of input PMOS transistor to increase the SNR at output. As NMOS load transistor does not contribute to any signal gain in terms of its g_m, the g_m of load transistor is minimized to reduce the noise produced at output. Therefore, long channel 2 um transistors are used for NMOS load, but short channel 112 nm transistors are used for PMOS.

5.6.3 Positive Feedback Filter

Since RC filters have gentle roll-offs and create 3dB loss at pole frequencies, RLC filters are desired where poles can made complex giving rise to the possibility of Butterworth, Chebyshev and other filter responses. Since we need 100 MHz cutoff filter, size of inductor required at these frequencies reaches tens of nH at the least. Therefore, we resort to active filter topologies to create complex poles. Sallen-Key filter is a type of positive feedback filter where positive feedback capacitor appears to be negative looking from input of amplifier. This negative capacitor has

positive reactance making it essentially an inductor, however with different frequency response. Therefore, to create a low pass filter with complex poles, positive feedback filter topology can be utilized. However, care must be taken as it may also make system unstable.

To understand how positive feedback can generate complex poles, a transfer function is derived. Consider a differential positive feedback filter shown in Figure 5-16. For simplicity, the transistor is assumed to be ideal and parasitic free. The voltage V_x can be found as to be:

$$\frac{V_x - V_{in}}{R_G} + sC_G V_x + sC_F(V_x - V_o) = 0$$

$$V_x = \frac{V_{in} + sC_F R_G - V_o}{1 + sR_G C_G + sR_G C_F}$$

Output voltage can be given as:

$$V_o = g_m V_x Z_L$$

Putting value of V_x in above equation:

$$\frac{V_o}{V_{in}} = g_m Z_L \times \frac{1}{1 + sR_G C_G + sR_G C_F - sR_G C_F g_m Z_L}$$

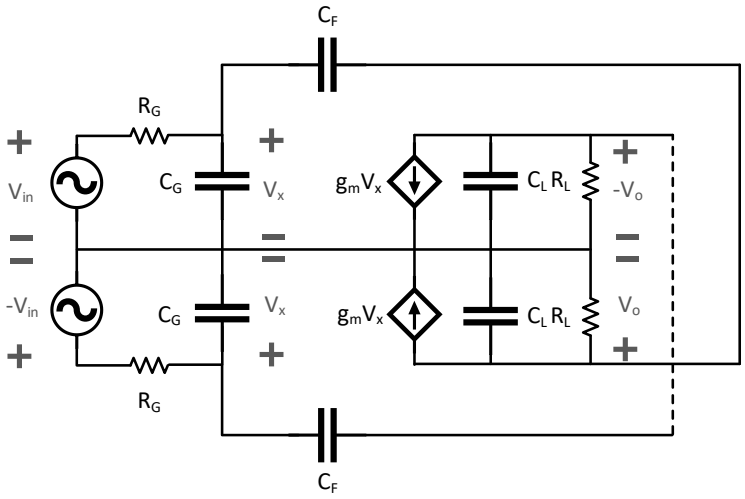
Putting value of Z_L (parallel of R_L and C_L) in above equation:

$$\frac{V_o}{V_{in}} = g_m R_L \times \frac{1}{(R_G R_L C_T C_L)s^2 + (R_L C_L + R_G C_T - R_G R_L g_m C_F)s + 1}$$

Re-ordering the above expression in standard second order low pass filter format:

$$\frac{V_o}{V_{in}} = g_m R_L \times \frac{\frac{1}{R_G C_T R_L C_L}}{s^2 + \frac{R_L C_L + R_G C_T - R_G R_L g_m C_F}{R_G R_L C_T C_L} s + \frac{1}{R_G R_L C_T C_L}}$$

Where Q and ω_n can be defined as now:



- R_G is mixer ON impedance
- C_G and C_F are inserted to form low-pass filter
- C_L and R_L come from transistors output impedance

Figure 5-14 Small Signal Model with Positive Feedback Capacitor

$$\omega_n^2 = \frac{1}{R_G R_L C_G C_L}$$

$$Q = \frac{\sqrt{R_G R_L C_T C_L}}{R_L C_L + R_G C_T - g_m R_G R_L C_F}$$

And the poles can be given as:

$$p_1, p_2 = \frac{-\omega_n}{2Q} \pm j\frac{\omega_n}{2Q}\sqrt{4Q^2 - 1}$$

Let's test the derived formulas for different cases.

5.6.3.1 Test Case: When C_F= 0

Let's say that C_F is zero. The Q can be written as:

$$Q = \frac{\sqrt{R_G R_L C_T C_L}}{R_L C_L + R_G C_T}$$

It can be proved that the maximum Q above expression can achieve is 0.5 for any values of R_G, C_G, R_L and C_L. This is because positive feedback is eliminated, and system behaves as a cascade of two RC filters which have maximum Q of 0.5 when two poles coincide.

5.6.3.2 Test Case: When $C_F \neq 0$ and feedback is negative

If feedback is negative, Q factor would have same formula as for positive feedback but with negative g_m sign, therefore:

$$Q = \frac{\sqrt{R_G R_L C_T C_L}}{R_L C_L + R_G C_T + g_m R_G R_L C_F}$$

Above expression also does not exceed Q of 0.5 because denominator is always bigger than numerator by at least twice. Therefore, a negative feedback filter would also behave as RC low pass filter. However, in this case much smaller values of C_F capacitor can used to provide higher time constant as the time constant gets multiplied by g_m (an artifact of miller effect).

5.6.3.3 Test Case: When $C_F \neq 0$ and feedback is positive

We have derived Q formula for positive feedback to be:

$$Q = \frac{\sqrt{R_G R_L C_T C_L}}{R_L C_L + R_G C_T - g_m R_G R_L C_F}$$

It is interesting to note that now denominator can be made much smaller than numerator by controlling the values of g_m and C_F. This means we can achieve any quality factor from 0 to ∞ and it can even be made negative in which case system would go unstable. A quality factor higher than 0.5 generates complex poles which create resonance around cut-off frequency and give rise to gain ripple and steep roll-offs. This way we can meet our filter requirement by tolerating some in-band gain ripple and achieving sharp roll-offs (much like Chebyshev).

However, as Q can potentially go negative making system unstable, values of C_F should be carefully chosen. For system to be stable, the denominator of Q expression should be greater than zero.

$$R_L C_L + R_G C_T + g_m R_G C_L C_F > 0$$

Therefore, the upper bound on C_F can be given as:

$$C_F < \frac{R_L C_L + R_G C_G}{R_G (g_m C_L - 1)}$$

5.6.3.4 Digital Control

In practice, since there are process variations that can affect value of C_F and potentially make it higher than the above expression, we have added a capacitor banks to control the value. This also allows us to change the filter Q on-the-go. Figure 5-17 shows capacitor banks with their ranges. We have also added gain control to perform AGC functionality. To change the gain of baseband amplifier, load resistor is varied. A resistor bank is added at the output as shown in Figure 5-17.

DC offset can be a big issue in direct conversion receivers as it can off-center the AC signal which in extreme cases can start clipping and exceed ADC full-scale. Therefore, we have added output DC offset control of baseband amplifier. To adjust the offset, the size of NMOS load

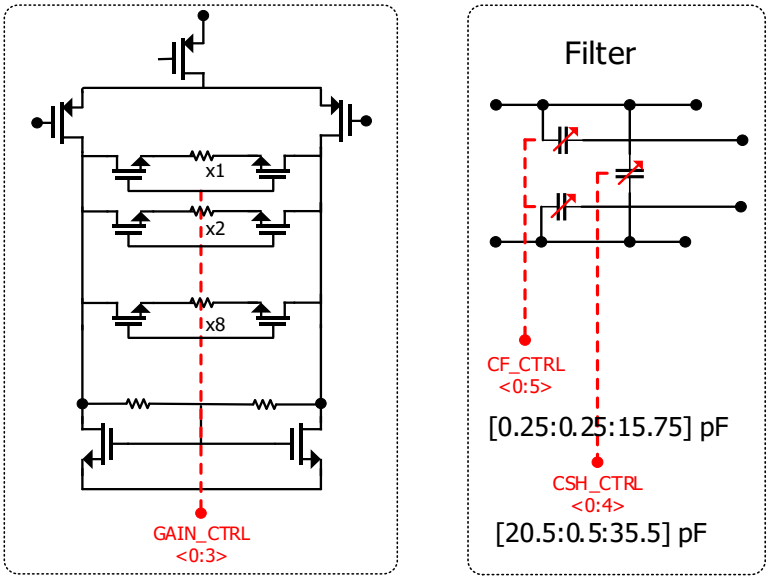


Figure 5-15 Gain and Filter Control Banks

transistor is varied. If the size of left transistor is decreased, the size of right transistor is increased by same amount. This differential steering helps in getting more linear range. For example, if only the size of, say, left transistor is decreased by factor x, neglecting channel length modulation, it's overdrive or V_{DS} across it will increase by square root of x. This means, when we start decreasing size, we would get bigger changes in V_{DS} and as we keep on increasing size, the change in V_{DS} becomes smaller and smaller, that is the resolution is not fixed. The same problem would exist in differential steering but in this case the differential voltage will change by 2 times square root of x (one from decreasing left transistor and one from increasing right transistor). However, above analysis would be inconsistent if we consider that gate of two transistors are connected together through common mode feedback, suggesting that both transistors would change potential together giving zero differential output voltage. Another benefit of differential steering is that since it changes left and right transistors V_{DS} in opposite direction, the average value of V_{DS} remains same which is what gets applied through common mode feedback to the transistors gate. Therefore, gate voltage does not change but V_{DS} will steer differentially (because of channel length modulation now). Figure 5-18 shows the offset control circuit. It was found through Monte Carlo simulations that there is 7mV one sigma variation of DC offset at the baseband output. Therefore, offset correct resolution was chosen to be around 7mV.

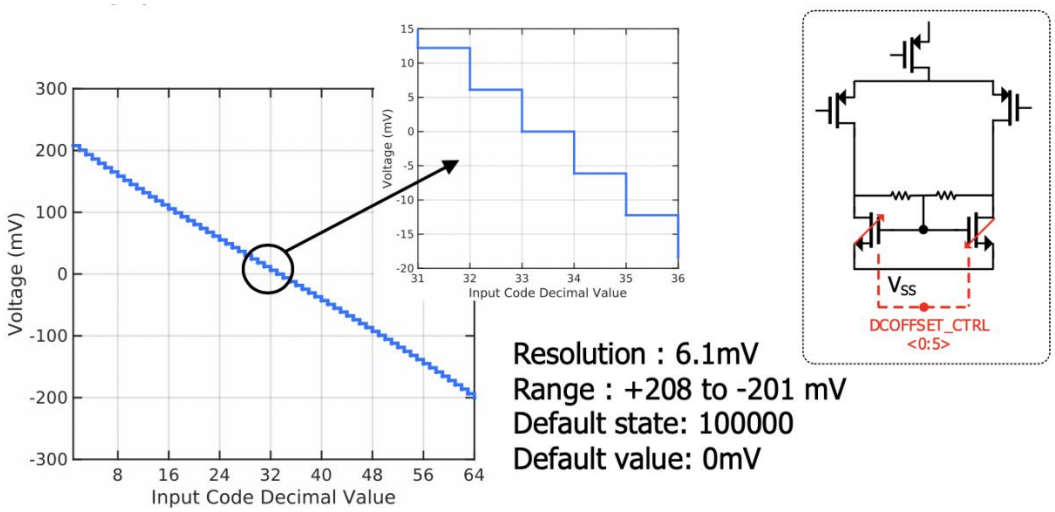


Figure 5-16 DC offset control

5.7 Layout

The layout of complete RX is shown in Figure 5-19. RF input, Baseband output and DC are supplied through pads whereas LO input comes on-chip from another block.

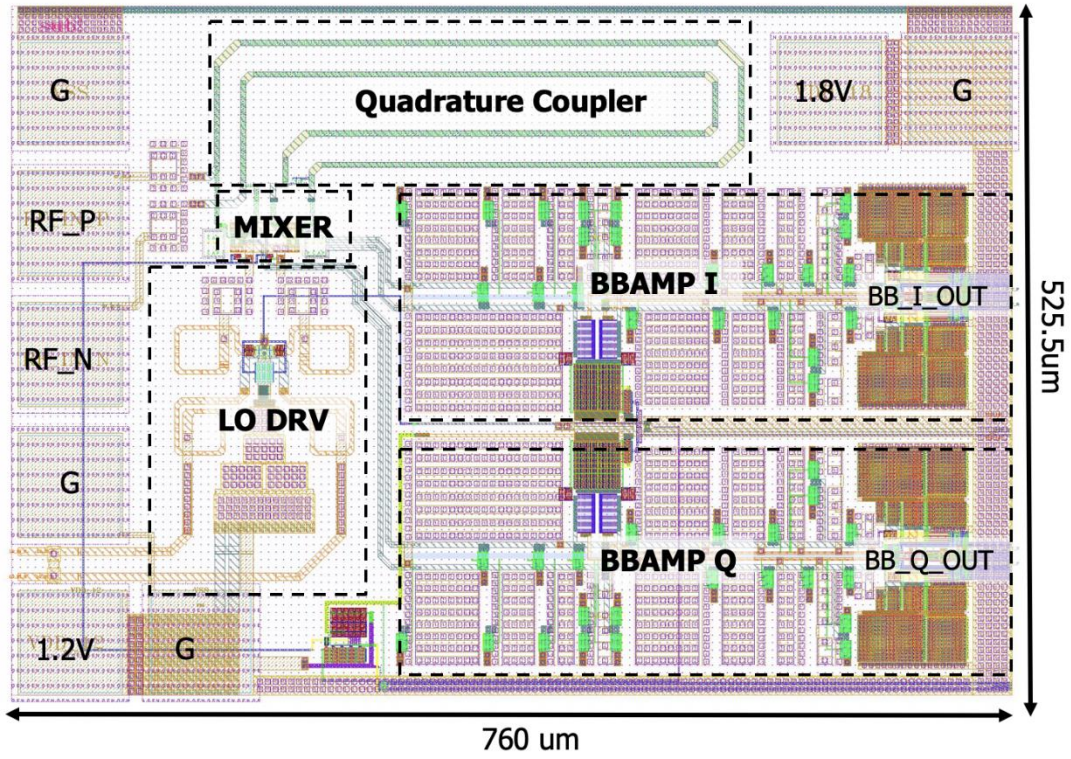


Figure 5-17 Chip Layout

5.8 Simulated Results

The chip was not measured at the time of writing this thesis, therefore simulated results are presented below.

5.8.1 Noise Figure

Double sideband integrated noise figure from 0.1kHz-100MHz has been used as noise figure metric. Figure 5-20 shows the plotted noise figure. The noise figure does not include coupler 3dB split loss which is assumed to get compensated when I and Q signals are combined.

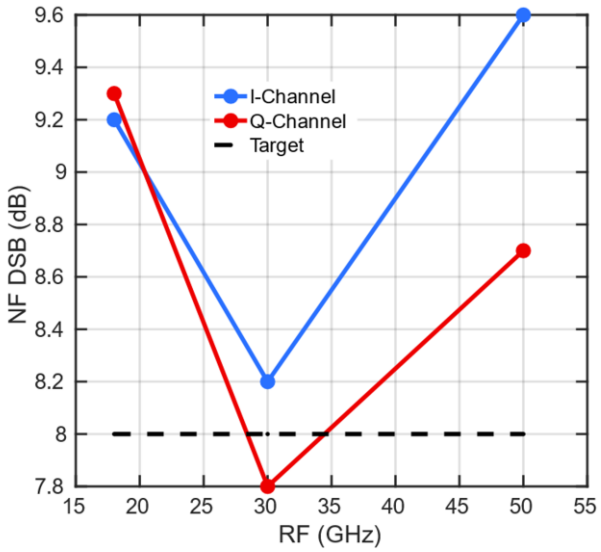


Figure 5-18 Noise Figure vs RF Frequency

5.8.2 Gain and Filter Response

Voltage gain and the filter response has been plotted across 0-100 MHz IF frequency for different RF frequencies as shown in figure 5-21. The voltage gain does not include the 3dB split loss from the coupler.

5.8.3 IIP3

Figure 5-22 shows the IIP3 response across IF frequency for different RF frequencies. It can be seen that there is a dip in IIP3 around 80 MHz IF frequency. This happens because of the positive feedback of filter. As mentioned before, a filter with Q factor higher than 0.5 tends to resonate at damped resonance frequency given as:

$$\omega_d = \sqrt{4Q^2 - 1}\frac{1}{2Q}\omega_n$$

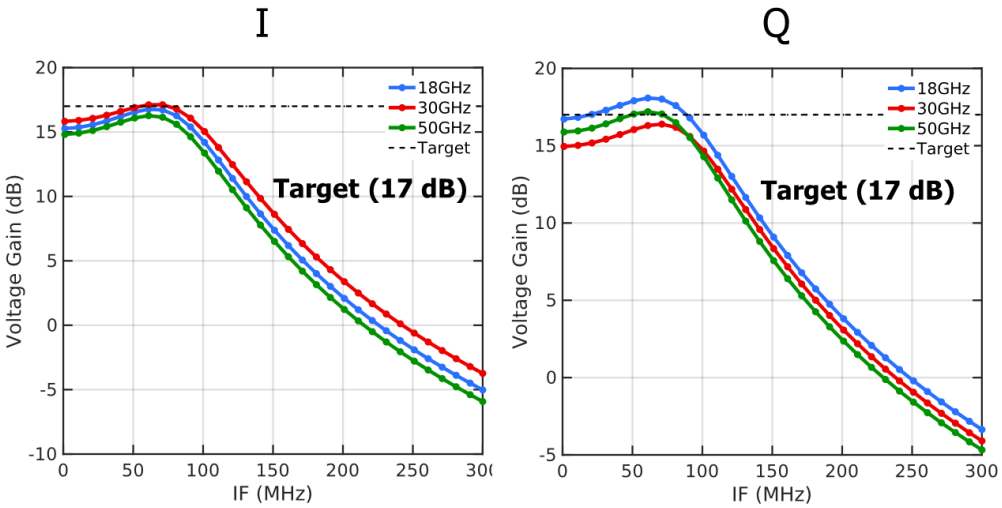


Figure 5-19Voltage Gain and Filter Response

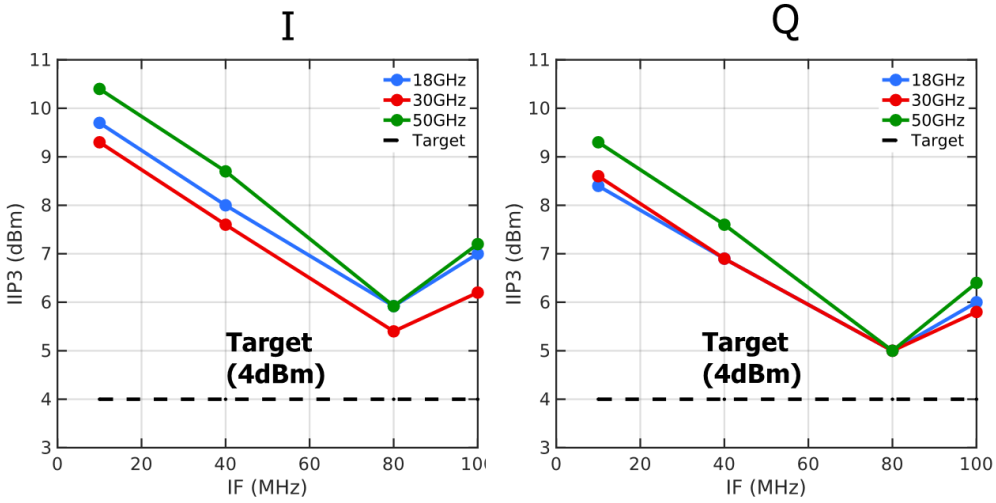


Figure 5-20 IIP3 Response Across Frequency

Therefore, voltage peak is created at ω_d frequency which increases the g_m non-linearity of the amplifier. This frequency happens to be 80 MHz in our case which was chosen to meet the in-band ripple requirement.

5.8.4 DC Power

Receiver consumes 47 mW total (I+Q). Following is the power distribution:

- LO Driver: 1.2 V supply with14.3 mA (17.2 mW)
- RX Mixer: Passive (0 mW)
- RX Coupler: Passive (0 mW)
- BB Amplifier: 1.8 V supply with 16.3 mA (29.4 mW)

5.8.5 RF and LO Input Return Loss

RF and LO input return loss is plotted in Figure 5-23. RF input is well matched thanks to the 'balanced' topology where reflections from I and Q channel end up cancelling at RF input. LO input match is close to -10 dB.

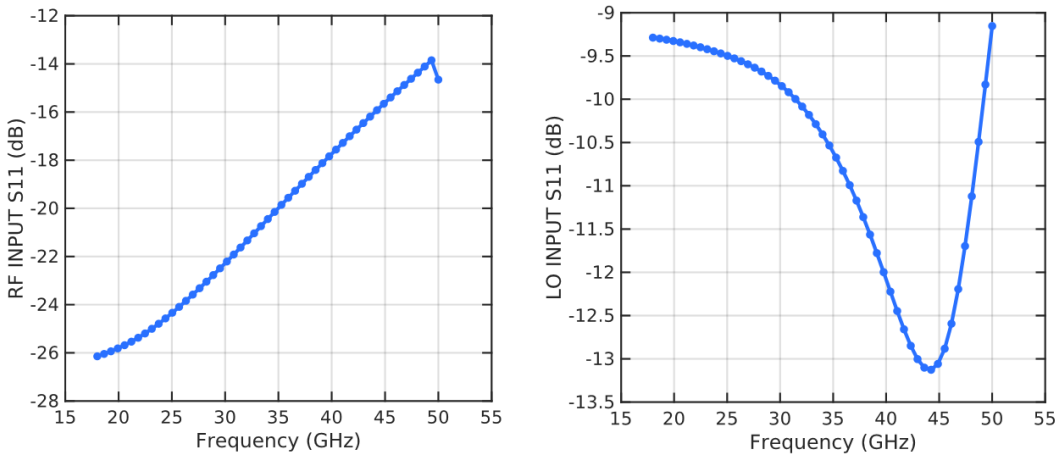


Figure 5-21 RF and LO Input Match

5.9 Summary

A wideband frequency tunable 18-50 GHz receiver design is presented. The receiver is designed in 45nm SOI and has mixer-first architecture with baseband low pass filter, baseband low noise amplifier, broadband LO driver, broadband quadrature coupler and different digital control circuits. Techniques to optimize linearity and reduce noise are explained. Positive feedback is utilized to realize a compact 2^{nd} order low-pass filter. The designed receiver is the first demonstration of low power 18-50 GHz receiver with more than 5dBm IIP3, 15 dB voltage gain and maximum 10 dB noise figure throughout the 18-50 GHz band.

6 CONCLUSION

With the ever-evolving wireless standards, such as Wi-Fi (1-6), and the ever expanding range of frequencies, such as 4G/5G, the equipment manufacturers are required to pack more bands and functionality into the chips while still maintaining the backward compatibility with previous standards or fallback option to lower frequency bands. A low power, highly integrated, multi-band and multi-standard chipset has thus become a requisite in commercial products. The work in this dissertation aims to demonstrate the design and potential of reconfigurable and multi-band RFICs operating in mm-wave band. To this end, a Ka-Band impedance reconfigurable power amplifier is designed in 130nm SiGe process which can reconfigure its output impedance to match to the antenna impedance in phased array radars where scan impedance variation is common. A Ka/V band-switchable bi-directional amplifier is designed in 130nm SiGe process. The amplifier consists of LNA, PA and T/R switches; and can switch its frequency band of operation between 28 GHz and 60 GHz. A tunable 18-50 GHz linear receiver is designed in 45nm CMOS SOI process. The receiver is direct down-conversion and continuously tunable within 18-50 GHz with reconfigurable IF bandwidth, gain and DC offset control. These demonstrations signify the importance of reconfigurable RF hardware and show state-of-the-art performance while significantly reducing the IC area and power consumption. With more and more functionality packed in a chip, the reconfigurable RFICs have become indispensable. The proposed concept of in-block reconfigurability and the presented design techniques to realize mm-wave frequency reconfigurable receivers have a huge potential in this regard.

BIBLIOGRAPHY

BIBLIOGRAPHY

[1] W. T. Khan, "Design and Development of Organically Packaged Components and Modules for Microwave and Millimeter- Wave Applications", PhD dissertation, Georgia Institue of Technology, Atlanta, 2014. Accessed on: Mar 6, 2020. [Online]. Available: https://smartech.gatech.edu/bitstream/handle/1853/53085/KHAN-DISSERTATION-2014.pdf

[2] R. Mukhopadhyay *et al.*, "Reconfigurable RFICs in Si-based technologies for a compact intelligent RF front-end," *IEEE Trans. Microw. Theory Tech.*, vol. 53, no. 1, pp. 81–93, 2005.

[3] "Cellular Frequencies." Wikipedia, Updated: 27-Feb-2020. [Online]. Available: https://en.wikipedia.org/wiki/Cellular_frequencies. [Accessed: 06-Mar-2020].

[4] J. W. M. Rogers *et al.*, "A fully integrated multi-band MIMO WLAN transceiver RFIC," *IEEE Symp. VLSI Circuits, Dig. Tech. Pap.*, vol. 2005, no. 8, pp. 290–293, 2005.

[5] W. C. E. Neo *et al.*, "Adaptive multi-band multi-mode power amplifier using integrated varactor-based tunable matching networks," *IEEE J. Solid-State Circuits*, vol. 41, no. 9, pp. 2166–2176, 2006.

[6] C. Huynh, J. Bae, and C. Nguyen, "A millimeter-wave 0.18-μm BiCMOS dual-band power amplifier," *2014 IEEE Int. Wirel. Symp. IWS 2014*, pp. 1–3, 2014.

[7] T. Purtova, B. Tillack, A. Ç. Ulusoy, H. Schumacher, and M. Kaynak, "24 to 79 GHz frequency band reconfigurable LNA," *Electron. Lett.*, vol. 48, no. 25, pp. 1598–1600, 2012.

[8] S. Shlafman, B. Sheinman, D. Elad, A. Valdes-Garcia, and M. A. T. Sanduleanu, "Variable Delay Transmission Lines in advanced CMOS SOI technology," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, pp. 111–114, 2014.

[9] V. K. Dao, Q. D. Bui, and C. S. Park, "A multi-band 900MHz/1.8GHz/5.2GHz LNA for reconfigurable radio," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 1, pp. 69–72, 2007.

[10] S. M. Bowers, K. Sengupta, K. Dasgupta, B. D. Parker, and A. Hajimiri, "Integrated self-healing for mm-wave power amplifiers," *IEEE Trans. Microw. Theory Tech.*, vol. 61, no. 3, pp. 1301–1315, 2013.

[11] D. M. Pozar and D. H. Schaubert, "Analysis of an Infinite Array of Rectangular Microstrip Patches with Idealized Probe Feeds," *IEEE Trans. Antennas Propag.*, vol. 32, no. 10, pp. 1101–1107, 1984.

[12] R. L. Schmid, A. C. Ulusoy, P. Song, and J. D. Cressler, "A 94 GHz, 1.4 dB insertion loss single-pole double-throw switch using reverse-saturated SiGe HBTs," *IEEE Microw. Wirel. Components Lett.*, vol. 24, no. 1, pp. 56–58, 2014.

[13] M. A. Oakley, U. S. Raghunathan, B. R. Wier, P. S. Chakraborty, and J. D. Cressler, "Large-signal reliability analysis of SiGe HBT cascode driver amplifiers," *IEEE Trans. Electron Devices*, vol. 62, no. 5, pp. 1383–1389, 2015.

[14] T. Chi, F. Wang, S. Li, M. Y. Huang, J. S. Park, and H. Wang, "A 60GHz on-chip linear radiator with single-element 27.9dBm Psat and 33.1dBm peak EIRP using multifeed antenna for direct on-antenna power combining," *Dig. Tech. Pap. - IEEE Int. Solid-State Circuits Conf.*, vol. 60, pp. 296–297, 2017.

[15] J. Xia, X. H. Fang, and S. Boumaiza, "60-GHz Power Amplifier in 45-nm SOI-CMOS Using Stacked Transformer-Based Parallel Power Combiner," *IEEE Microw. Wirel. Components Lett.*, vol. 28, no. 8, pp. 711–713, 2018.

[16] C. R. Chappidi and K. Sengupta, "Frequency Reconfigurable mm-Wave Power Amplifier With Active Impedance Synthesis in an Asymmetrical Non-Isolated Combiner: Analysis and Design," *IEEE J. Solid-State Circuits*, vol. 52, no. 8, pp. 1990–2008, 2017.

[17] and D. B. A. Larie, E. Kerhervé, B. Martineau, L. Vogt, "A 60 GHz 28 nm UTBB FD-SOI CMOS reconfigurable power amplifier with 21% PAE, 18.2 dBm P1dB and 74 mW PDC," in *IEEE ISSCC Dig. Tech. Papers*, 2015, pp. 1–3.

[18] A. Sarkar and B. A. Floyd, "A 28-GHz harmonic-tuned power amplifier in 130-nm SiGe BiCMOS," *IEEE Trans. Microw. Theory Tech.*, vol. 65, no. 2, pp. 522–535, 2017.

[19] N. Rostomyan, M. Ozen, and P. Asbeck, "28 GHz Doherty Power Amplifier in CMOS SOI with 28% Back-Off PAE," *IEEE Microw. Wirel. Components Lett.*, vol. 28, no. 5, pp. 446–448, 2018.

[20] T. W. Li and H. Wang, "A continuous-mode 23.5-41GHz hybrid Class-F/F-l power amplifier with 46% peak PAE for 5G massive MIMO applications," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 2018–June, pp. 220–223, 2018.

[21] W. C. Huang, J. L. Lin, Y. H. Lin, and H. Wang, "A k-band power amplifier with 26-dBm output power and 34% PAE with novel inductance-based neutralization in 90-nm CMOS," *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 2018–June, pp. 228–231, 2018.

[22] S. Shakib, H. C. Park, J. Dunworth, V. Aparin, and K. Entesari, "A Highly Efficient and Linear Power Amplifier for 28-GHz 5G Phased Array Radios in 28-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 51, no. 12, pp. 3020–3036, 2016.

[23] J. Chen and A. M. Niknejad, "Design and analysis of a stage-scaled distributed power amplifier," *IEEE Trans. Microw. Theory Tech.*, vol. 59, no. 5, pp. 1274–1283, 2011.

[24] S. Li, D. Fritsche, C. Carta, and F. Ellinger, “Design and characterization of a 12-40 GHz power amplifier in SiGe technology,” *PAWR 2018 - Proc. 2018 IEEE Top. Conf. Power Amplifiers Wirel. Radio Appl.*, vol. 2018–Janua, pp. 23–25, 2018.

[25] K. Fang, C. S. Levy, and J. F. Buckwalter, “Supply-Scaling for Efficiency Enhancement in Distributed Power Amplifiers,” *IEEE J. Solid-State Circuits*, vol. 51, no. 9, pp. 1994–2005, 2016.

[26] Y. Zhang and K. Ma, “A 2-22 GHz CMOS distributed power amplifier with combined artificial transmission lines,” *IEEE Microw. Wirel. Components Lett.*, vol. 27, no. 12, pp. 1122–1124, 2017.

[27] S. Zihir and G. M. Rebeiz, “A wideband 60 GHz LNA with 3.3 dB minimum noise figure,” *IEEE MTT-S Int. Microw. Symp. Dig.*, pp. 1969–1971, 2017.

[28] H. Gao *et al.*, “A 48-61 GHz LNA in 40-nm CMOS with 3.6 dB minimum NF employing a metal slotting method,” *Dig. Pap. - IEEE Radio Freq. Integr. Circuits Symp.*, vol. 2016–July, pp. 154–157, 2016.

[29] J. Plouchart *et al.*, “A 18mW, 3.3dB NF, 60 Ghz LNA in 32nm SOI CMOS technology with automatic NF calibration,” 2015 IEEE Radio Frequency Integrated Circuits (RFIC), Phoenix, AZ, 2015, pp. 319–322.

[30] B. W. Min and G. M. Rebeiz, “Ka-band SiGe HBT low noise amplifier design for simultaneous noise and input power matching,” *IEEE Microw. Wirel. Components Lett.*, vol. 17, no. 12, pp. 891–893, 2007.

[31] C. Li, O. El-Aassar, A. Kumar, M. Boenke, and G. M. Rebeiz, “LNA Design with CMOS SOI Process-l.4dB NF K/Ka band LNA,” *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 2018–June, pp. 1484–1486, 2018.

[32] J. Lee and C. Nguyen, “A 13/24/35-GHz concurrent tri-band LNA with feedback notches,” *2013 IEEE 13th Top. Meet. Silicon Monolith. Integr. Circuits RF Syst. SiRF 2013 - RWW 2013*, pp. 252–254, 2013.

[33] V. Chauhan and B. Floyd, “A 24-44 GHz UWB LNA for 5G cellular frequency bands,” *2018 11th Glob. Symp. Millim. Waves, GSMM 2018*, pp. 18–20, 2018.

[34] T. M. Hancock, S. Gross, and T-H. Chang, "Millimeter Wave Digital Arrays (MIDAS): An Overview," Government Microcircuit Applications & Critical Technologies Conference (GOMAC 2019), Albuquerque, NM.

[35] C. Andrews and A. C. Molnar, "A passive-mixer-first receiver with baseband-controlled RF impedance matching, ≪ 6dB NF, and ≫ 27dBm wideband IIP3," *2010 IEEE International Solid-State Circuits Conference - (ISSCC)*, San Francisco, CA, 2010, pp. 46-47.

[36] C. Wilson and B. Floyd, "20–30 GHz mixer-first receiver in 45-nm SOI CMOS," *2016 IEEE Radio Frequency Integrated Circuits Symposium (RFIC)*, San Francisco, CA, 2016, pp. 344-347.

[37] D. Yang, C. Andrews and A. Molnar, "Optimized Design of N-Phase Passive Mixer-First Receivers in Wideband Operation," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 11, pp. 2759-2770, Nov. 2015.