MILLIMETER-WAVE MICROSYSTEMS USING ADDITIVE MANUFACTURING PROCESS

By

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ABSTRACT

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In recent years, researchers have been working to explore the millimeter-wave frequency domain for wireless technology to cope with the immense demand for high bandwidth for faster wireless applications such as communication and remote sensing in general. In wireless communication technology, high frequency of the mm-wave systems offers high bandwidth transmission for faster data transmission. The mm-wave frequency has also been approved by FCC for commercial applications like 5G communications that will deliver a more reliable, dependable and scalable cellular technology with high rate and low latency for the network users. It also promises to facilitate high data communication among devices and humans as well as other devices, the phenomena that gave rise to an emerging field known as the "Internet-of-Things." For remote sensing, higher frequencies of the mm-wave offer higher spatial and range resolution that can enable more intelligent sensor technologies.

The fabrication and manufacturing process of mm-wave systems become increasingly difficult and expensive due to size reduction at smaller wavelengths. To overcome these problems, system on package (SoP) technology has gained a lot of attention. The SoP approach combines multiple integrated circuits and passive components using different packaging and interconnect approaches into a miniaturized micro-system module. Additive manufacturing (AM), also colloquially known as 3-D printing, is considered as a promising method for packaging in SoP solutions because it enables rapid prototyping and large-scale production at an affordable cost and minimal environmental impact.

This work primarily focuses on the development of mm-wave microsystems by integrating chips with AM process using aerosol jet printing (AJP). Several mm-wave transceiver components that ranges from Ka-band to W-band are designed and realized in a state-of-the-art silicon-germanium IC foundry process, and are characterized to be used in complete transceiver system using 3-D printing packaging. These include a 28-60 GHz Single-Pole Double-Throw (SPDT) switch, 28-60 GHz Low-noise amplifier (LNA), 15-100 GHz downconverting mixer, K-Band upconverting mixer, V-band upconverting mixer, and a 90 GHz MMIC frequency tripler.

The feasibility of using AJP in mm-wave regime and the ink characteristics were also studied. For any AM process to be an all-in-one packaging solution, it should have the capability of realizing conducting as well as dielectric materials. Silver and polyimide inks were used in this work to demonstrate a chip-to-chip interconnection and a comparison with the traditional packaging technique is also discussed. An ultra-wideband interconnect from 0.1-110 GHz was implemented using AJP. The conductivity of the silver ink and its viability to be used in flexible electronics was also considered.

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CHAPTER 1

INTRODUCTION

In 1947, John Bardeen, Walter Brattain and William Shockley invented the first-ever transistor at Bell Labs that paved the path of solid-state electronics. Although the bulky vacuum tubes were replaced by this tiny invention, the extensive wiring and connections requirements of the transistors limited the miniaturization of the circuits. The engineers were forced to think out of the box and they eventually came up with the idea of putting the transistors and associated electronics together on a single chip that gave rise to Integrated Circuit (IC). The concept of IC was first introduced by Geoffrey Dummer in 1952, followed by Jack Kilby's demonstration of the first ever IC at Texas Instruments in July 1958. IC has revolutionized the electronic world since and has become an integral part of our daily life.

1.1 Motivation and Problem Description

Since the advent of IC technology, they have grown to be ubiquitous electronic components finding its applications ranging from home appliances to radio-astronomy [1]. The demand for such applications in the market drives the relentless pursuit to enhance the systems and elevate them to the commercialization phase. To emphasize this fact, we can consider the example of the mobile communication industry and the evolution of 5G communication technology. The unprecedented growth of consumer devices like smartphones and tablets has resulted in "data explosion". According to the annual visual network index (VNI) reports released by Cisco in 2016, the global mobile data traffic was 7.2 Exabytes per month, which has increased 16-folds in last five years (since 2011) [2]. It is expected to reach 49 Exabytes per month in 2021 with the number of networked devices per capita increasing from 7.8 to 13.2 in the United States alone. It would be very convenient for the consumers if their personal data can be automatically and readily

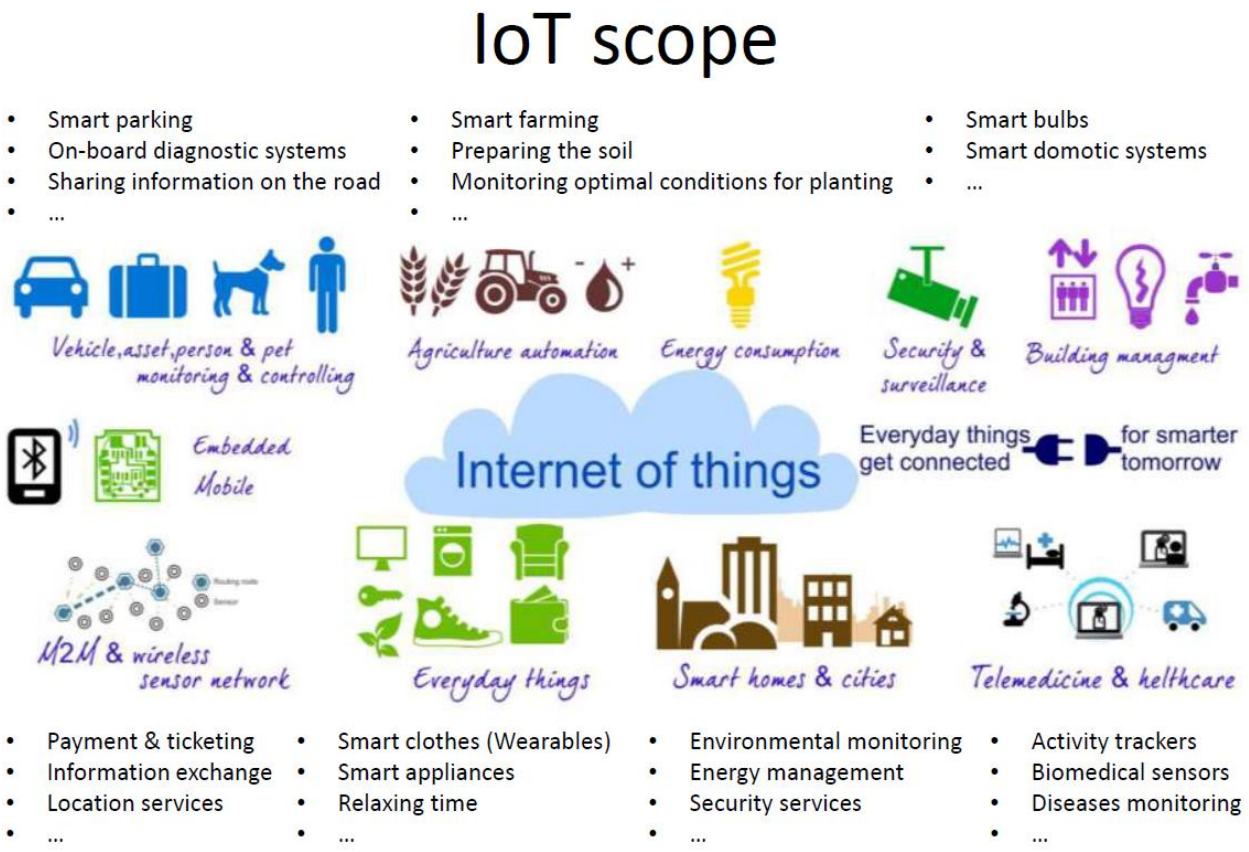


Figure 1.1 Image depicting the scope of Internet-of-Things (IoT).

transferred among their devices. That would require the establishment of systems capable of facilitating high data communication among devices without much human interventions. This idea has given rise to an emerging field called the 'Internet of things' (IoT) [3].

Figure 1.1 depicts the scope of IoT [4]. Recently, it has grown in popularity making its mark on every industry ranging from auto industry enabling real-time data sharing on the road for self-driven cars to farming empowering smart agriculture. Over the period of next 10 years, an estimated $6 billion will be invested to support the IoT infrastructure which is expected to generate $13 trillion by 2025. However, IoT requires a more reliable, scalable and dependable cellular technology. This is where the 5G mobile communication technology comes into picture and

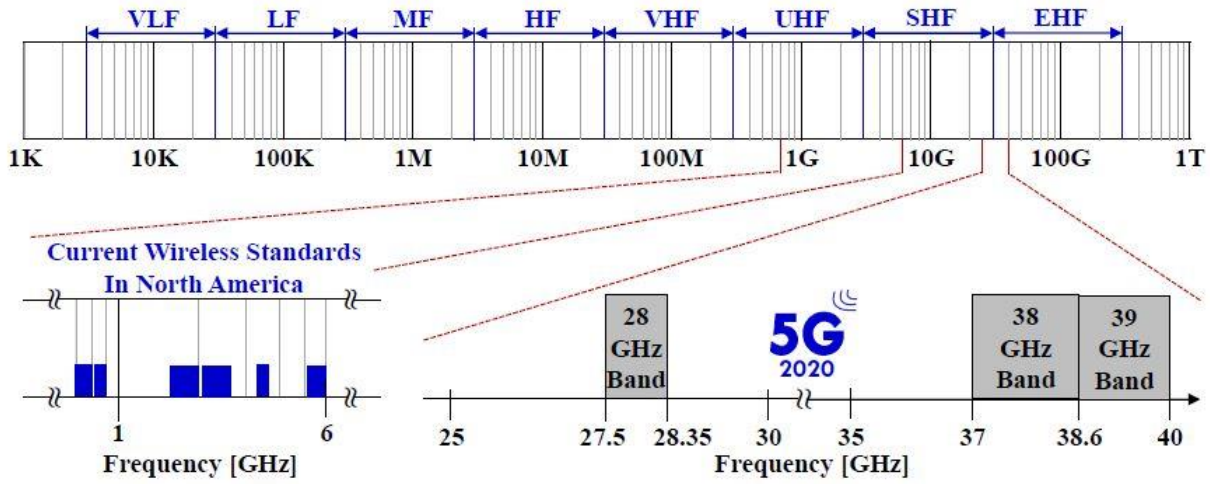


Figure 1.2 The ITU allocated current wireless standard spectrum in North America and the spectrum of the upcoming 5G standard approved by FCC.

promises to deliver all the necessary attributes with high rate and low latency [5] and it is expected to kick-off in 2020.

The current cellular wireless standard spectrum allocation for North America on the International Telecommunications Union (ITU) radio band scale is shown in Figure 1.2. However, the sub-6 GHz bands of the current frequency spectrum is populated by wireless mobile bands (7), WiMAX, WiFi and other wireless standards and it is not capable of supporting the wider bandwidth required for higher data rates and increased capacity of the 5G [6]. Therefore, the idea is to migrate to the underutilized millimeter-wave (mm-wave) band that offers much wider bandwidth and is capable of handling the so-called “data-explosion”.

This dissertation focuses on the implementation of the necessary hardware required to support the long-anticipated mm-wave infrastructure at an affordable cost without sacrificing the performance. The problems addressed in this work are:

- Applications like IoT requires the interaction of multiple devices operating in different frequency spectrums. Wideband transceiver components are realized that can support

multiple bands to adapt according to application needs or support multiple communication standards.

- With the number of networked devices per capita almost doubling from 7.8 to 13.2 at United States in 2021, there is an increasing demand of low-cost hardware to make individual devices affordable. This work concentrates on the development of such components using relatively cheap silicon technology.
- Sometimes, the specifications of a transceiver may be stringent and require expensive hardware. For example, in a typical transmitter chain the power amplifiers (PA) usually needs to deliver high power and they are realized in expensive Gallium Arsenide (GaAs) process whereas the upconverting mixer that follows the PA can be in silicon process. Hence these two components are packaged together as a transmitter module. In this work, additive manufacturing (3D printing) has been demonstrated as an alternative packaging technique.

1.2 Thesis Statement

The objective of this dissertation is to develop a set of next generation microsystems using the state-of-the-art high performance SiGe (silicon-germanium) technology and additive manufacturing. The main contributions are the realizations and characterizations of different multi-band and wideband transceiver components using SiGe process that covers Ka-band, Q-band, V-band and W-band; the demonstration of an ultra wideband chip-to-board interconnect and the chip-to-chip interconnect using 3-D printing.

1.3 Millimeter-wave Integrated Circuit and Its Applications

Millimeter-wave (mm-wave) corresponds to the radio frequency from 30-300 GHz, with the wavelength ranging from 10 mm to 1 mm. The advancement in IC technology enabled the

exploration of mm-wave for applications in many fields such as medical imaging (94 and 140 GHz) [7], [8], radio-astronomy (ALMA Project) [1], prospective 5G communication (28 and 38 GHz) [9], [5], automobile collision-avoidance radars (26 and 77 GHz) [10] and chemical and bio-sensing. Scientists are particularly interested in mm-wave domain because of the advantages unique to its properties. In wireless communication technology, the high frequency of the mm-wave systems offers high bandwidth transmission for faster wireless applications. For remote sensing, higher frequencies of the mm-wave offer higher spatial and range resolution. Shorter wavelength allows size reduction and compact designs for different RF modules, antennas and sensors.

1.4 Silicon Germanium Process Technology for Millimeter-wave Frequency Domain

As IC-based electronics have grown to be ubiquitous part in our daily-life, large-scale production of such hardware is imperative. When it comes to choosing a process technology for hardware implementation, the obvious choice will be the one that give a better performance with a high level of integration at an affordable cost. Generally, III-V and SOI technology offer superior Radio Frequency (RF) performance but they are very expensive. In contrast, silicon and SiGe technology seems to be the best candidate that satisfies the "one-technology-fits-all" criterion [11]. It is the low-cost platform that can fulfill the demands for large-scale productions without compromising too much in terms of performance.

The SiGe materials and devices are anticipated to grow to $5 billion by 2021, at a compound annual growth rate (CAGR) of 13.7% from 2016 to 2021 [12]. This market growth is attributed to the increasing demand for high performance radars and sensors in the automotive industry, and emerging opportunities like 5G. The SiGe technology has been on par with the

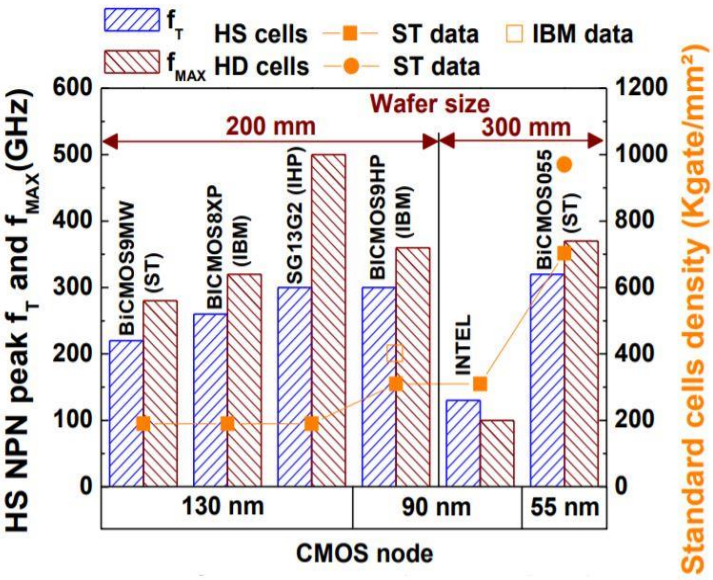


Figure 1.3 Comparison of different BiCMOS Processes available in the industry.

demands and has continued to push the barrier to develop faster and better devices. Figure 1.2 shows the different nodes of various SiGe BiCMOS (Bipolar Complementary Metal-Oxide Semiconductor) foundry processes offered by the industries and research institutes [13]. As can be seen, their peak f_T/f_{max} values and cell density are comparable and even better than some high-performance processes.

Many millimeter-wave RFICs like Passive Millimeter-wave Imaging [14], Q-band transmitter for satellite communication [15], and 5G transceivers have been demonstrated. In this thesis, we present some similar transceiver blocks using the state-of-the-art IHP SG13G2 SiGe BiCMOS technology that demonstrate superior performance than most of the blocks found in existing literature.

1.5 Additive Manufacturing for Millimeter-wave Circuits

The fabrication and manufacturing process of mm-wave systems is getting increasingly difficult and expensive due to size reduction at smaller wavelengths. To overcome these problems, the system on package (SoP) technology has gained a lot of attention [16]. SoP is the technique of

integrating discrete components like passives and MMIC on a single packaging substrate. These components are fabricated separately to ensure their individual best performances. Additive manufacturing, also known as 3D printing, has drawn substantial interest as an alternative method for interconnecting ICs on SoP solutions. The process is extremely low-cost and enables faster prototyping with minimal environmental waste. Inkjet printing and Aerosol jet printing, two of the front runners of digital printing technology, have already been demonstrated for interconnects up to 40 GHz [16][17]. However, the IC and the test structures in both cases were a passive antenna and simple transmission line. To the best of author's knowledge, no chip-to-chip interconnection involving any millimeter-wave circuit has been shown so far. One of the aims of this thesis is to demonstrate the interconnection of two IC chips using aerosol jet printing (AJP).

1.6 Dissertation Outline

The dissertation is outlined as follows: Chapter 2 discusses extensively the design procedure and measurement characterization of different transceiver blocks that have been fabricated as part of this thesis. These blocks include a 28-60 GHz Single-Pole Double-Throw (SPDT) switch, 28-60 GHz LNA, 15-100 GHz downconverting mixer, K-Band upconverting mixer, V-band upconverting mixer, and a 90 GHz MMIC frequency tripler. Chapter 3 briefly discusses the digital printing technology we will be using, followed by the detailed design and performance of an ultra-wideband interconnect using AJP, that demonstrates AJP as the most suitable candidate for millimeter-wave interconnections. Chapter 4 focuses on the plan where we intend to demonstrate a full functional SoP system using our designed ICs and AJP interconnects.

CHAPTER 2

MILLIMETER-WAVE TRANSCEIVER COMPONENTS

2.1 Introduction

The term “transceiver” is given to a circuit block that comprises of both the transmitter and receiver in a single package. Figure 2.1 depicts the RF front-end of a typical transceiver block. Generally, the transmitter and receiver chains of a transceiver may or may not share some of the circuit blocks. The example shown in Figure 2.1 shares the same antenna and switch for both transmitter and receiver. The remaining of the receiver path consists of a Low Noise Amplifier (LNA) followed by the downconverting mixer. In the receiver mode, the mixer converts high Radio-frequency (RF) to low intermediate frequency (IF). The IF frequency then passes though the Analog-to-Digital (ADC) converter and finally to the digital circuitry. Similarly, the upconverting mixer in the transmitter chain receives analog input from the Digital-to-analog (DAC), upconverts it to RF frequency. The power amplifier (PA) increases the transmit power of the signal and the antenna transmits it when the transceiver is operating in transmitter mode.

In this chapter, we will discuss the millimeter-wave (mm-wave) RF components that have been fabricated and characterized as part of the dissertation. We will start with the common switch block, followed by LNA and downconverting mixer for the receiver chain, and the upconverting mixer of the transmitter. A frequency multiplier that can be used as Local Oscillator (LO) is also designed and characterized. Though the multiplier is designed for W-band, the same architecture can be used to implement multipliers at lower frequency bands. Finally, we will end the chapter with a brief conclusion.

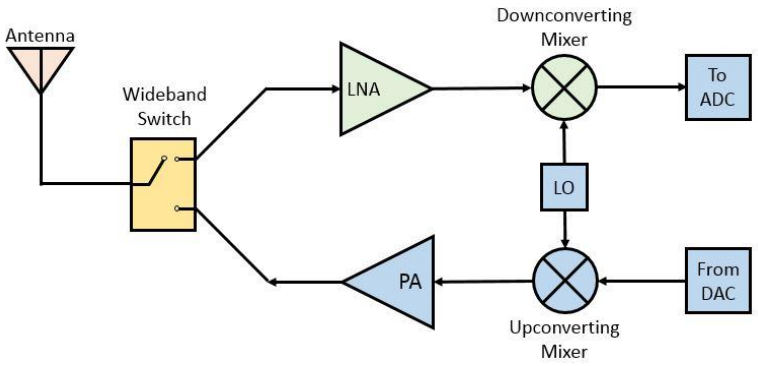


Figure 2.1 Typical RF Front-end Transceiver Block Diagram.

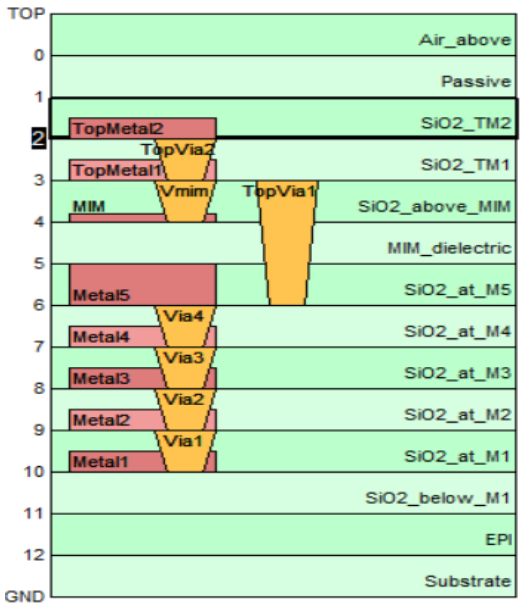


Figure 2.2 0.13-µm IHP SG13G2 SiGe-process substrate.

2.2 The IHP SG13G2 Technology

All the millimeter-wave components presented in this dissertation was realized using the 0.13-μm IHP Microelectronics SG13G2 SiGe-HBT technology with f_T /f_{MAX}/VB_{CEO} of 300-GHz/500-GHz/1.7-V. The process substrate is given in Figure 2.2. It has the silicon dioxide (SiO_2) layer of 15.75 µm thickness epitaxially grown on top of 370 µm bulk silicon substrate. The process

offers seven metallization layers with two thick top-metal layers. Apart from that, the design kit also has MIM (Metal-Insulator-Metal)-capacitors and resistors.

2.3 Single-Pole Double-Throw Switch

Typically, most transceivers that have a single antenna uses single-pole double-throw (SPDT) switches to change operation between transmitting and receiving mode. It is a critical component since its insertion loss, isolation and linearity effects the overall performance of the entire RF block [18]. We demonstrate a 20-60 GHz ultra-wideband SPDT switch in 0.13-μm SiGe BiCMOS technology. The effect of base loading of the HBTs within the switch is studied and it was found that the bandwidth of the switch can be tuned by proper selection of the inductance at the HBT base. Hence, a large RF choke is connected at the HBT base along the control path to achieve the required bandwidth and linearity of the switch. Additionally, the HBTs are operated in reverse-saturation mode that improves the insertion loss and isolation of the switch. The switch has less than 3 dB insertion loss from 20-60 GHz, more than 22.5 dB isolation and 17 dBm input-referred 1-dB compression point which is comparable to any state-of-the-art switch in CMOS and BiCMOS processes.

2.3.1 Circuit Description

The three most common topologies for designing an SPDT switch are series, shunt and series-shunt as shown in Figure 2.3. Among them, the series-shunt topology is the most popular topology for the microwave frequency applications. However, in the mm-wave frequencies, both series and series-shunt topology adds loss in the ON-state and causes a parasitic capacitive feedthrough path in the OFF-state at millimeter wave [19]. Hence, the quarter-wave shunt topology is widely used for mm-wave switches.

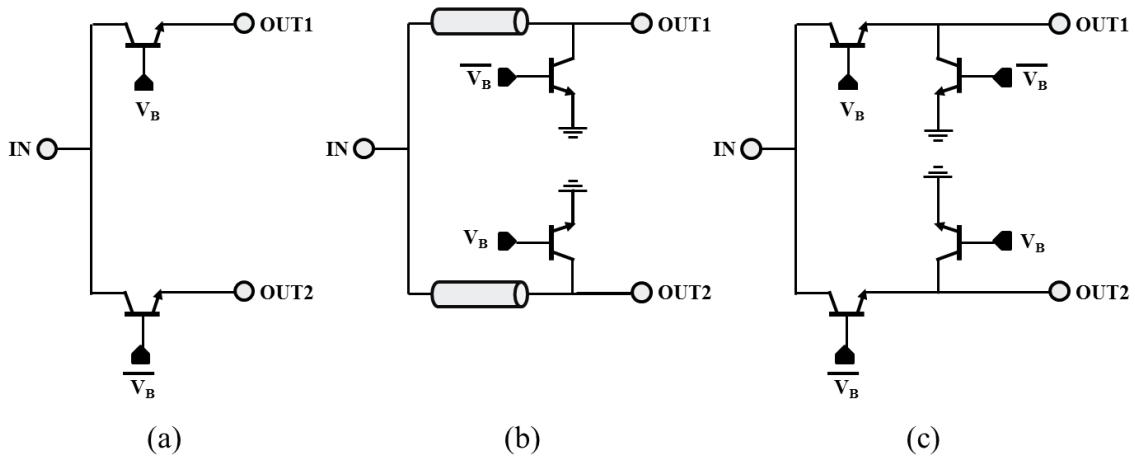


Figure 2.3 Common SPDT Switch Topologies- (a) series, (b) shunt, and (c) series-shunt.

To determine the most suitable topology, S21 in the ON and OFF state were plotted for all three topologies with different HBT sizes as depicted in Figure 2.4. Series-shunt switches seems to have the best S21_OFF but poorest S21_ON. Quarter-wave shunt topology exhibits the best S21_ON with moderate S21_OFF.

The ultra-wideband switch is designed using the quarter-wave shunt topology as shown in Figure 2.5. In this approach, however, the bandwidth is limited by the quarter-wavelength transformer, and as will be shown by the base termination of the HBTs in the switch.

The shunt HBTs are operated in "reverse saturation" mode, as shown in Figure 2.5, by connecting the emitter to the RF path and collector to the ground with a V_{CE} potential of 0 V. This configuration enhances the switch performance due to the bandgap engineering and physical isolation of the emitter from the conductive silicon [20], while providing sufficient switching speed for most applications. Figure 2.6 shows the scanning electron microscope (SEM) cross-section of the SG13G2 HBT [21] and equivalent small-signal circuit model of the HBT when operated in forward and reverse saturation. Since the emitter is well-isolated from the bulk silicon, the junction capacitance between the collector and substrate is eliminated in the reverse saturation mode, hence

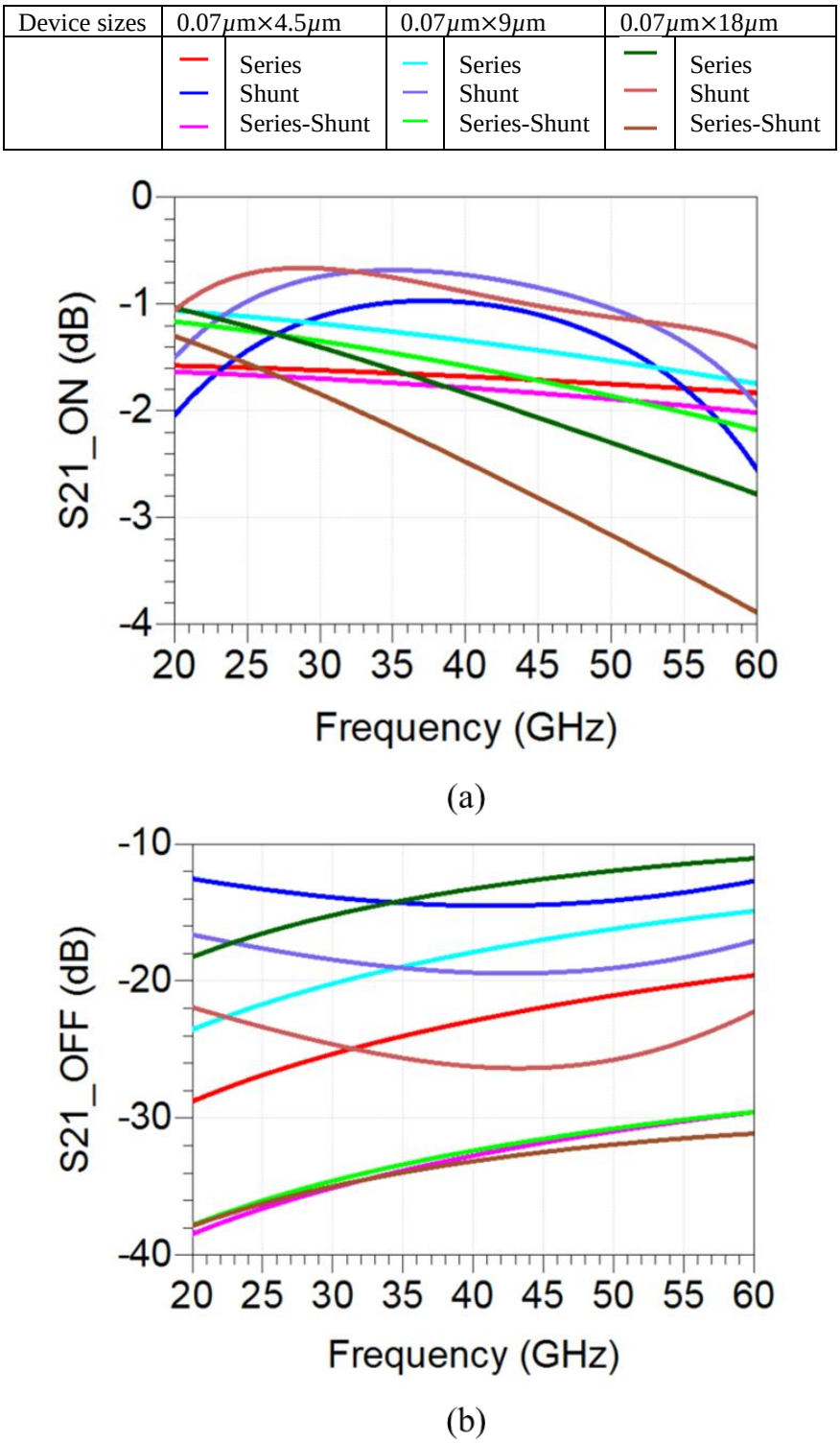


Figure 2.4 S21_ON and S21_OFF for series, shunt and series-shunt topologies.

reducing the parasitic. In addition, due to the higher doping concentration of the emitter and Ge-induced band reduction in the base, electrons see a larger barrier when traveling from emitter to

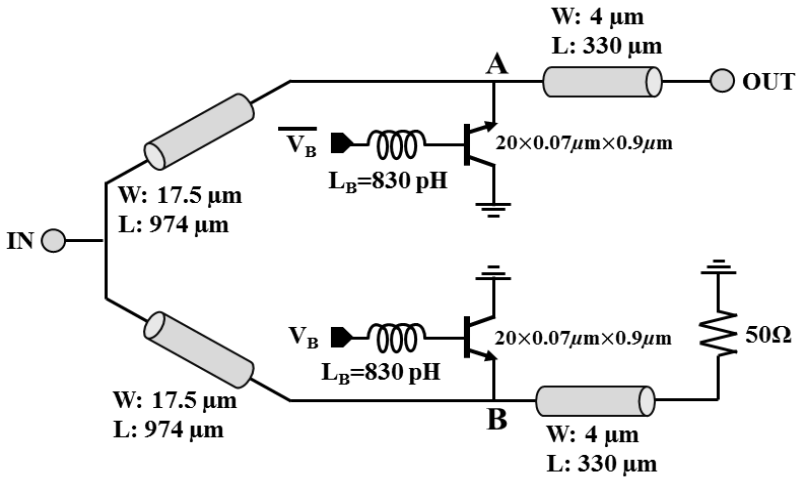


Figure 2.5 Circuit schematic of the ultra-wideband SPDT switch.

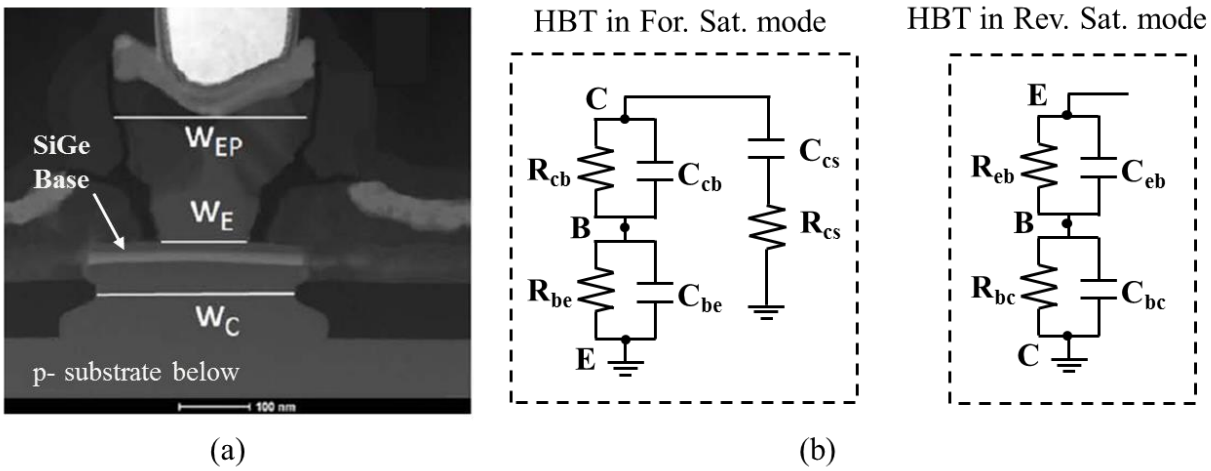


Figure 2.6 (a) SEM cross-section of the IHP's SG13G2, and (c) the equivalent small-signal circuit model for the forward and reverse saturation.

base. Figure 2.7 shows the energy band diagram of the HBT with zero potential at all nodes. The conduction band potential barrier is higher from emitter to base (ΔE_{CE}) than from collector to base (ΔE_{CC}).

The equivalent off-state and on-state shunt resistance (R_{off} and R_{on}) are simulated and depicted in Figure 2.8. For the quarter-wave shunt topology it is desirable to have a larger R_{off} and smaller R_{on}. A higher R_{off} reduces the RF leakage from the switch port to ground, whereas a smaller

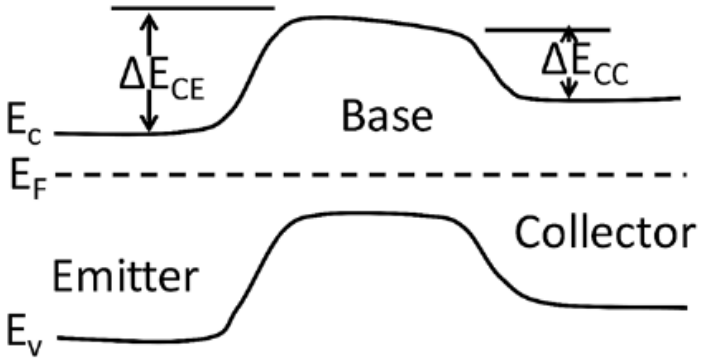


Figure 2.7 The OFF-state equilibrium energy band diagram of a SiGe HBT.

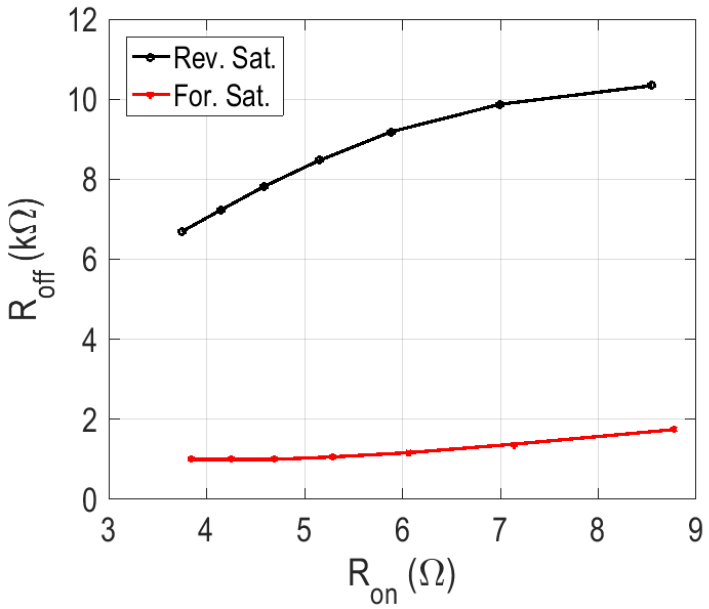


Figure 2.8 Roff and Ron for the SG13G2 device configurations at 44 GHz.

R_{on} established a better short at the switch port which, in turn, is transformed to an open for the input port.

To choose a proper device size, the S21_ON and S21_OFF where simulated as a function of the emitter length both for the forward and reverse saturated configuration (Figure 2.9). As the device gets larger, the improvement in S21_ON gets insignificant whereas the larger devices consume more power. Hence a device size of 0.07 μm × 18 μm was chosen.

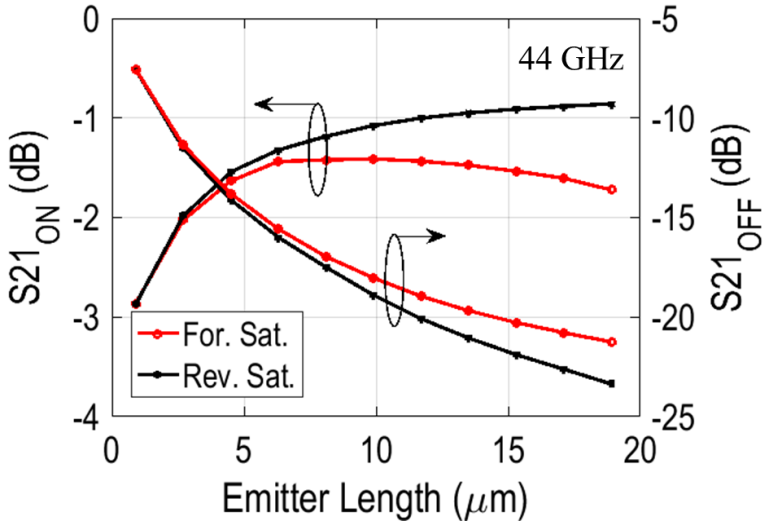
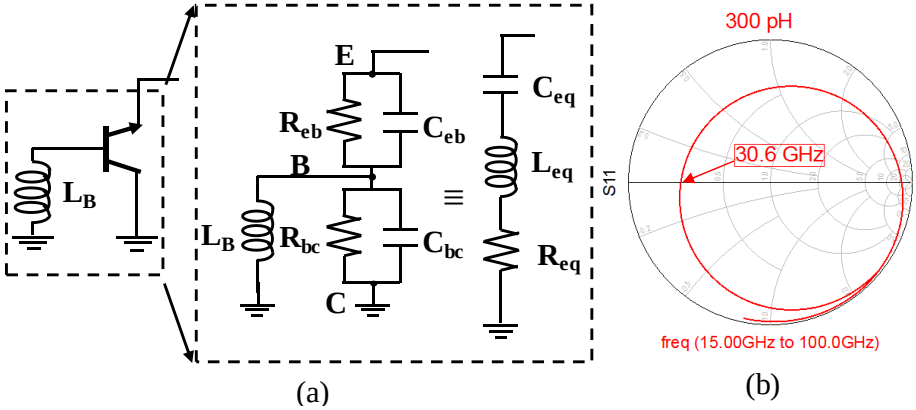
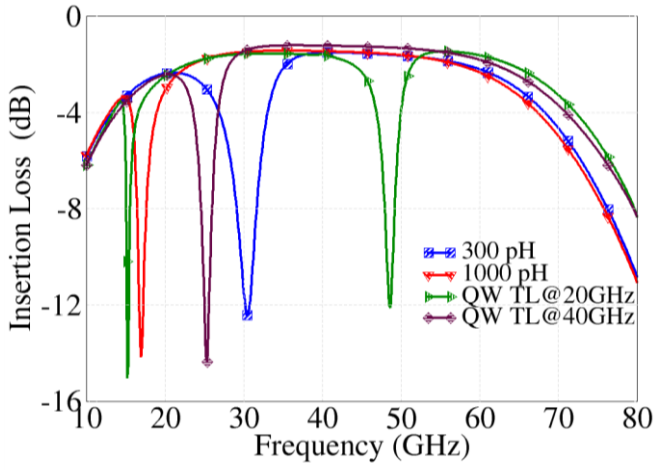


Figure 2.9 Simulated S21_On and S21_OFF for forward and reverse saturated HBTs as a function of emitter length.



(a) (b)



(c)

Figure 2.10 (a) Equivalent circuit for the common-collector HBT, (b) Smith Chart plot of the S11 at the emitter of a common-collector HBT with inductor-connected base, and (c) SPDT switch insertion loss for various inductances L_B at the base of the HBTs.

A critical design variable is the termination impedance at the base of the HBTs, as shown

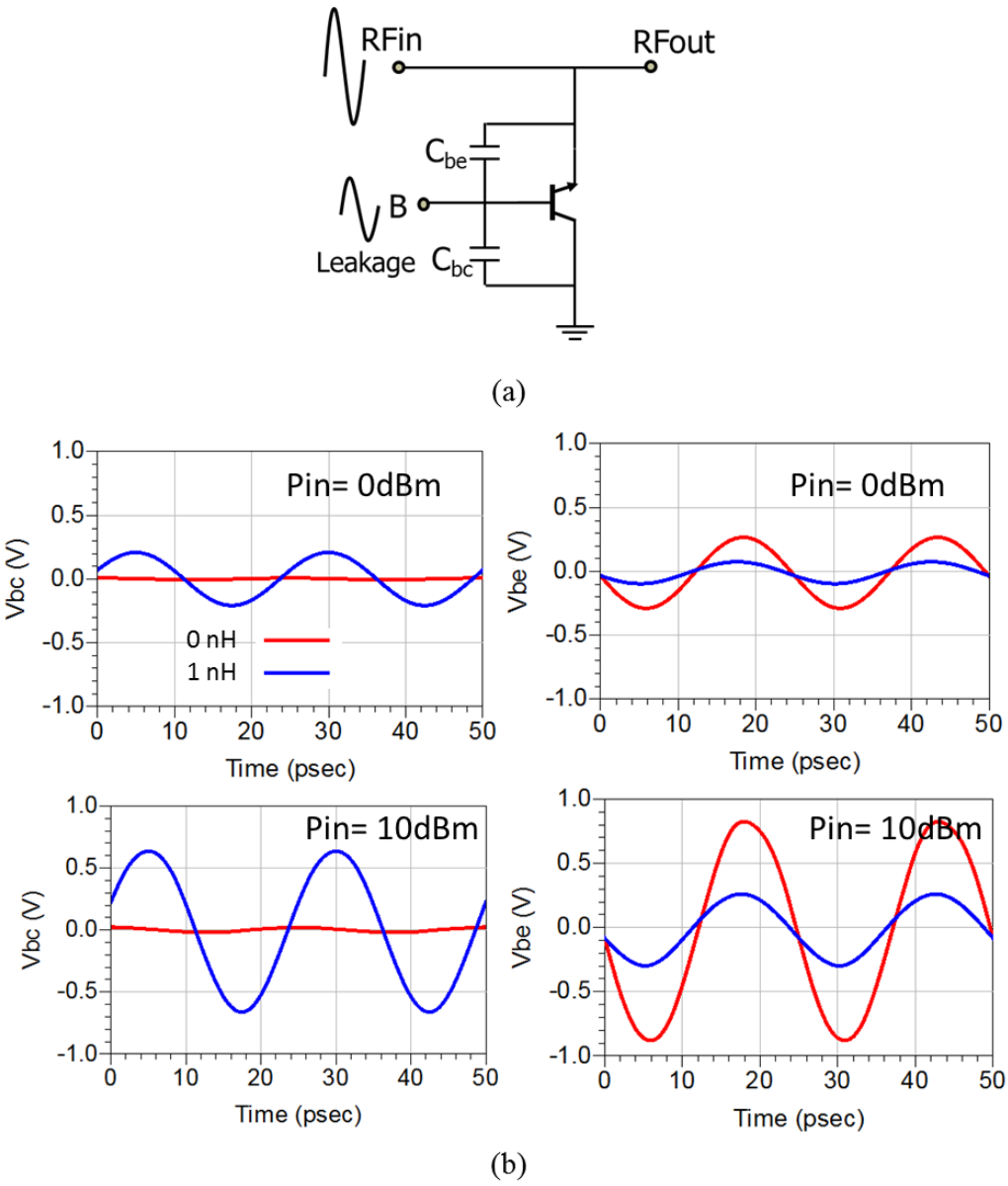


Figure 2.11 (a) Capacitive coupling at the base of the HBT, and (b) voltage swings across the parasitic capacitances (C_{be}) and (C_{bc}).

in Figure 2.10. This impedance can enhance the linearity and reduce the insertion loss of the switch.

Regarding linearity, a large RF swing at the switch port of the OFF-state HBT can be capacitively coupled to the base of the HBT due to the emitter-base (C_{be}) and base-collector (C_{bc}) capacitances and cause self-actuation as displayed in Figure 2.11(a). Having a large inductor at the

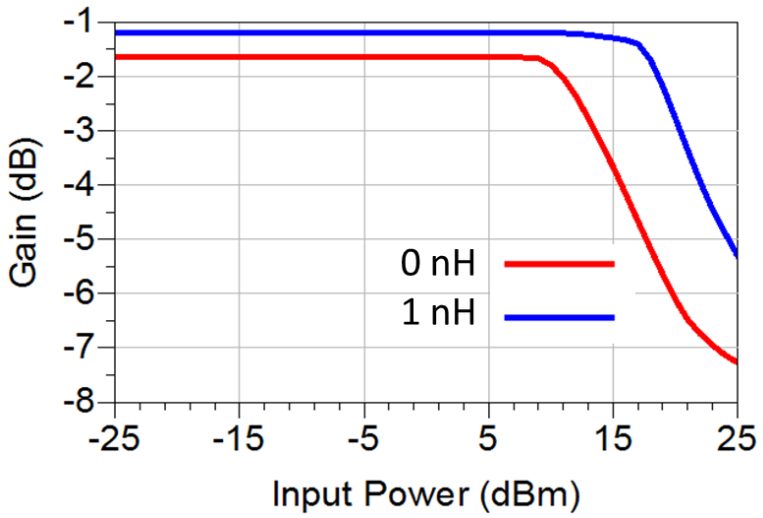
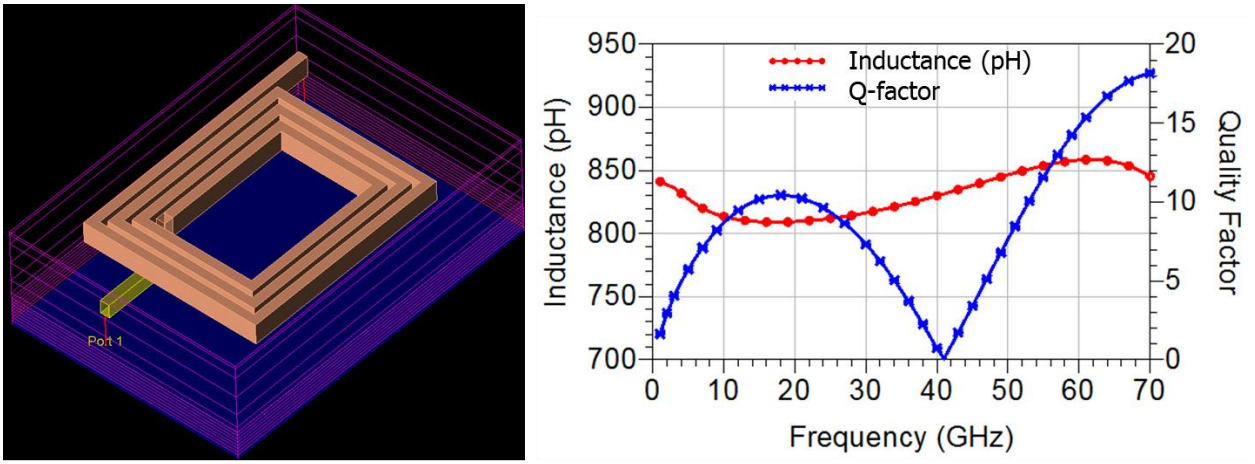


Figure 2.12 Gain as a function of input power (at 44GHz) with and without a high RF impedance at the base.

base will present a high RF impedance, increase the voltage swing at the base and reduce the voltage differential between the emitter and base, which in turn will stop self-actuation. Figure 2.11(b) shows the time-domain simulation of the SPDT switch with and without inductor at the base of the HBTs. For higher input power, it is clear that not having a high RF impedance results in a large voltage swing between base and emitter, causing it to self-actuate. Figure 2.12 shows the simulated gain as a function of input power and the effect of having the high impedance at the base. A large inductor of 1 nH at the base improves the simulated input-referred 1-dB compression point by 3 dB. A common practice to avoid this is to use a quarter-wave line at the control path for the designed frequency. However, a quarter-wave transmission line will limit the switch bandwidth with an in-band resonance. The resonant behavior of the switch core is studied with a one-port simulation. Since, for a common-collector configuration, the parasitic RC network associated with the substrate is not present at the emitter [20], the equivalent circuit for the common-collector configured HBT with an inductor at the base can be represented as shown in Figure 2.10(a) and behaves like a series R-L-C circuit. The impedance of any complex load is a function of frequency



(a) (b)

Figure 2.13 (a) EM model of the base inductor in ADS momentum, and (c) the simulated inductance and Q-factor.

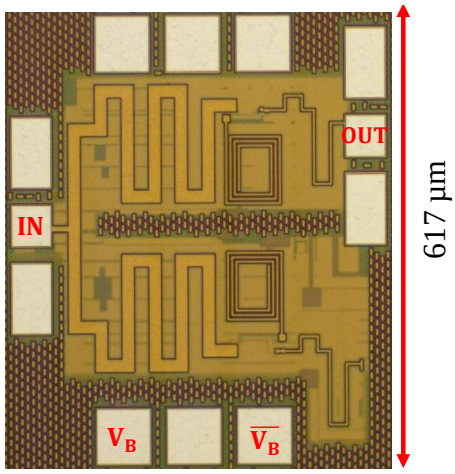


Figure 2.14 Chip photograph of the ultra-wideband 20-60 GHz SPDT switch.

and the S11 will rotate along the Smith Chart with frequency, the load will change from capacitive to inductive and vice versa with self-resonant frequency f_R. An analytical expression for f_R was derived to be

$$1/2\pi\sqrt{L_{eq}C_{eq}} = 1/2\pi\sqrt{2L_1C_1}$$

and verified using simulation with $L_1 = L_B$ and $C_{be\_off} = C_{bc\_off} = C_1 \approx 45\ fF$. The S11 from the one-port simulation with $L_B = 300\ pH$ shows a resonance at 30.6 GHz as shown in Figure 2.10(b).

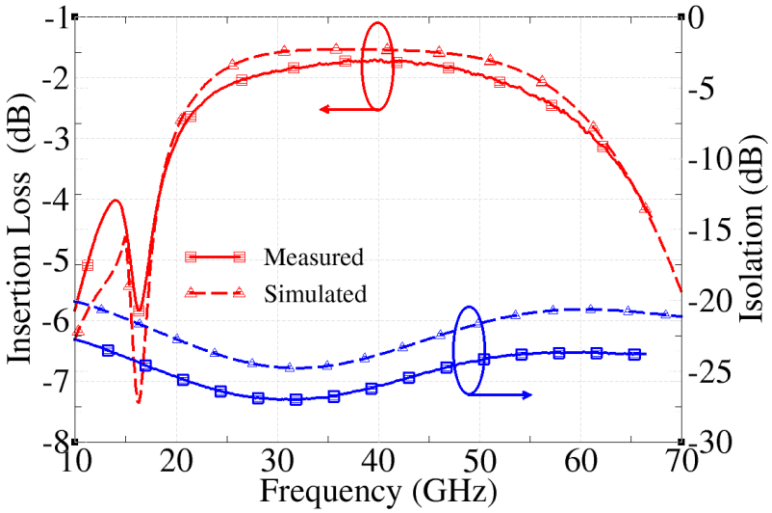


Figure 2.15 Measured (solid) and Simulated (dashed) insertion loss and isolation of the reverse-saturated SPDT switch.

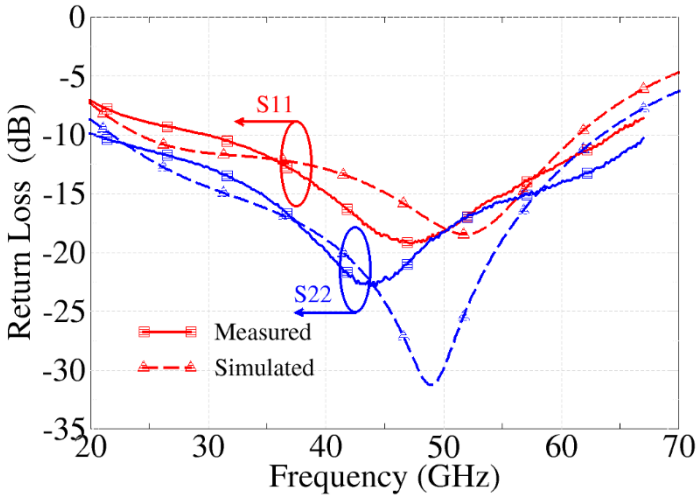


Figure 2.16 Measured (solid) and Simulated (dashed) return loss of the input and output port.

A two-port simulation of the switch in Figure 2.5 was performed with different inductances and quarter-wave transmission lines at the HBT base and the insertion loss for the frequency sweep is displayed in Fig. 2.10(c). The self-resonance of the switch core limits the switch bandwidth and the bandwidth can be tuned by adjusting the base inductance L_B, which in turn changes f_R. Hence, the L_B for the designed switch was EM simulated using ADS Momentum and tuned to obtain a flat insertion loss for the desired frequency band. Final value of L_B was chosen to be 830 *pH* that had

the resonant effect at 16.2 GHz yielding insertion loss less than 3 dB from 20–60 GHz. Figure 2.14 shows the EM-model of the base inductor and the value of its inductance and quality factor.

2.3.2 Measurement Results

The 20-60 GHz SPDT switch is realized in 0.13-μm IHP Microelectronics SG13G2 SiGe-HBT technology with f_T /f_{MAX} of 300-GHz/500-GHz. The die occupies an area of 535 μm × 613 μm and the photograph is shown in Figure 2.14. The transmission lines and inductors were designed as thin-film microstrip line (TFMSL) using the topmost and the bottom layer of the seven metallization layers offered by the technology. Control voltages of 0 V and 1 V are used to turn ON and OFF the devices and the switch consumes 10 mW power when turned on. One of the switch outputs is terminated using an on-chip 50 Ω resistor to obtain a two-port measurement configuration.

The insertion loss and isolation are plotted in Figure 2.15. The minimum insertion loss is 1.7 dB at 40 GHz, excluding the pad loss of 0.3 dB [22], while it is better than 3 dB from 20-60 GHz. The measured isolation is better than 22.5 dB for the entire design band frequency. Figure 2.16 shows the input and output return loss. The input return loss is less than 7.5 dB from 20-65 GHz and less than 10 dB from 30 GHz onward. The output return loss is better than 10 dB for the whole band.

The linearity is presented in Figure 2.17 and the input-referred 1-dB compression point is measured to be 17 dBm at 32 GHz, which is very close to the simulated value of 18 dBm. The switching speed of the SPDT switch was simulated. Figure 2.18 indicates that both turn ON and turn OFF speed of the switch is less than 200 psec. Table 2.1 shows the comparison of the designed ultra-wideband switch with other published results using other technologies. The switch achieves

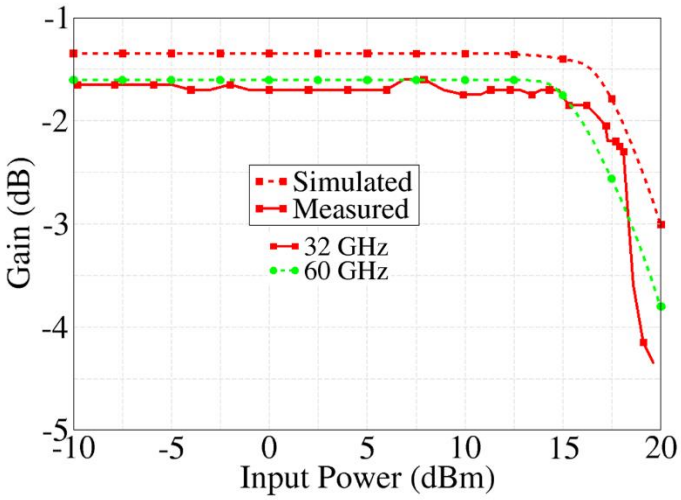


Figure 2.17 Measured (solid) and Simulated (dashed) insertion loss against input power at 32 GHz and 60 GHz.

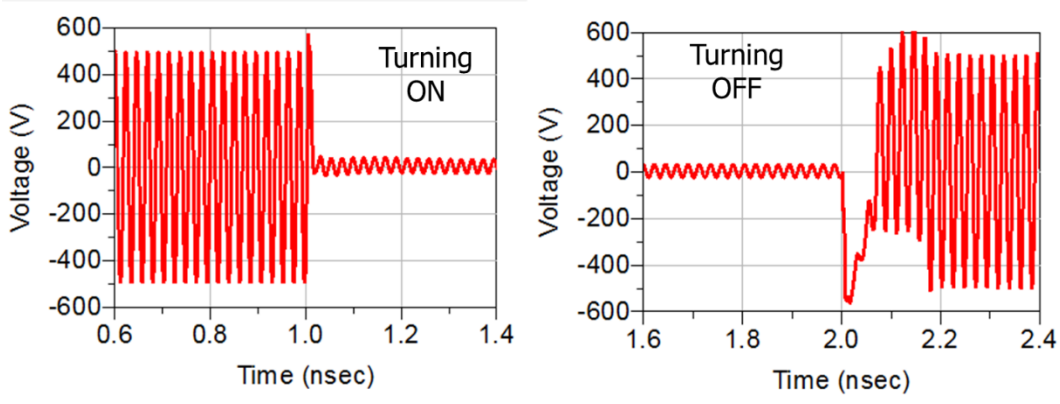


Figure 2.18 Simulated transient response of the realized SPDT switch.

performance metrics very similar to the state-of-the-art with a clear advantage in terms of bandwidth when it comes to silicon technologies.

2.4 Low-Noise Amplifier

In a receiver chain, the overall noise figure (NF) is an important parameter because a low NF is desired to obtain a high Signal-to-Noise ratio (SNR). The noise factor of a cascade of stage is given by Friis formula:

$$F_{total} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \cdots + \frac{F_n - 1}{G_1 G_2 \ldots G_{n-1}} + \cdots \quad (2.1)$$

Table 2.1 Performance Comparison of SPDT Switch with the State-of-the-art

Reference	Technology	Topology	Freq. (GHz)	Frac. BW (%)	Min. IL (dB)	Iso. (dB)	RL (dB)	P1dB (dBm)	Size (mm^2)	P_{DC} (mW)
This work	**130nm SiGe**	**$\lambda/4$-shunt**	**20-61**	**101.2**	**1.7^{+}**	**>22.5**	**>7.2/ >10†**	**18**	**0.194***	**10**
IJSSC'10 [22]	90nm CMOS	$\lambda/4$-shunt	50-70	33.3	1.5	>25	>8	13.5	0.27*	0
MWCL'17 [23]	65nm CMOS	Lumped 4-way combiner	58-85	37.8	1.8	>22	>10	10	0.015*	0
NEWCAS'16 [24]	55nm SiGe	$\lambda/4$-shunt	35-75	72.7	2.6	>27	>10	14	0.28*	0
SiRF'12 [25]	200nm SiGe	Diode-connected HBT in series-shunt	8-40	75	1.6	>20.3	>9	10	0.2*/ 1.4	5.6
MTT'12 [26]	350nm SiGe	Differential SPDT	42-70	50	1.25	>18	>3	1	0.78	-
MWCL'17 [27]	100nm GaAs pHEMT	Distributed 6 shunt stacked HEMTs	35-70	66.7	2.2	>40	>15	20.2	0.96	0
MTT'04 [28]	100nm GaAs pHEMT	Traveling wave	15-80	136.8	1.2	>25	>5	27.5	2.25	0
MTT'17 [29]	130nm SOI	Series-shunt, with matching network	DC-50	200	<2.1$^{\$}$	>27$^{\$}$	>9	10.5	0.04*	-

*Without pads $^{+}$Without pad loss $^{\$}$@50 GHz †@29.7-64.5 GHz

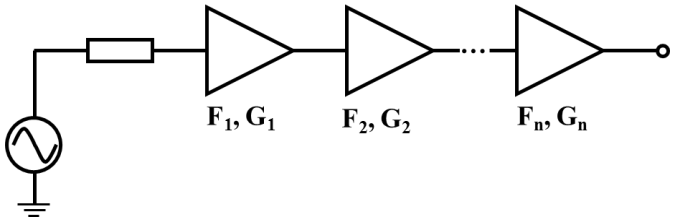


Figure 2.19 A conventional cascade of stages for RF blocks.

where F_n and $G_n$are the noise factor and gain of the n^{th} stage as shown in Figure 2.19. It is evident that the first block contributes most of the overall noise figure of the receiver, and therefore low-noise amplifiers (LNA), being the first building block, should have enough gain to suppress the noise of the subsequent blocks. For our project, we designed a multiband LNA ranging from 22.5 GHz- 65.6 GHz. The measured gain of the LNA is greater than 10 dB from 22.5GHz- 66.6 GHz and greater than 14 dB from 27.5 GHz- 60.1 GHZ. The simulated mean noise figure (NF) is 2.87 dB for 28-60 GHz with the minimum being 2.271 dB at 32.1 GHz. The measured S11 is less than -10 dB from 22 GHz-67 GHz.

2.4.1 Circuit Description

The LNA was designed using the two-stage cascode topology as depicted in Figure 2.20. The two-stage was chosen for the design because it allowed for more design of freedom. The first stage was optimized to reduce the NF while the second stage was more concentrated on boosting the gain. Even though the cascode topology has slightly more noise than common-emitter configuration, it was chosen as it offers higher gain and improves bandwidth by isolating input and output better than a common-emitter design.

The expression for the minimum noise figure (NF_{min}) for Si and SiGe technologies is given by

$$F_{MIN} \cong 1 + \frac{n}{\beta_0} + \frac{f}{f_T} \times \sqrt{\frac{2I_C}{V_T}(r_b + r_e)\left(1 + \frac{f_T^2}{\beta_0 f^2}\right) + \frac{n^2 f_T^2}{\beta_0 f^2}} \qquad (2.2)$$

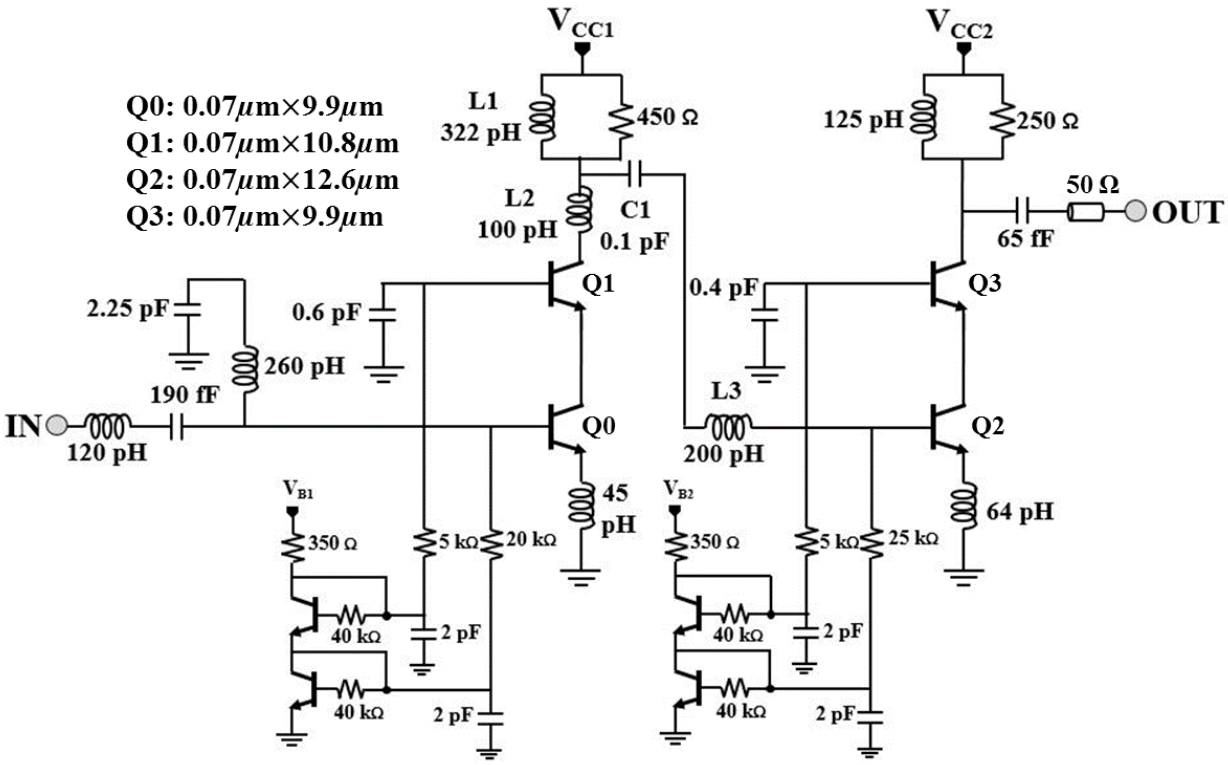


Figure 2.20 Circuit Schematic of the multi-band LNA.

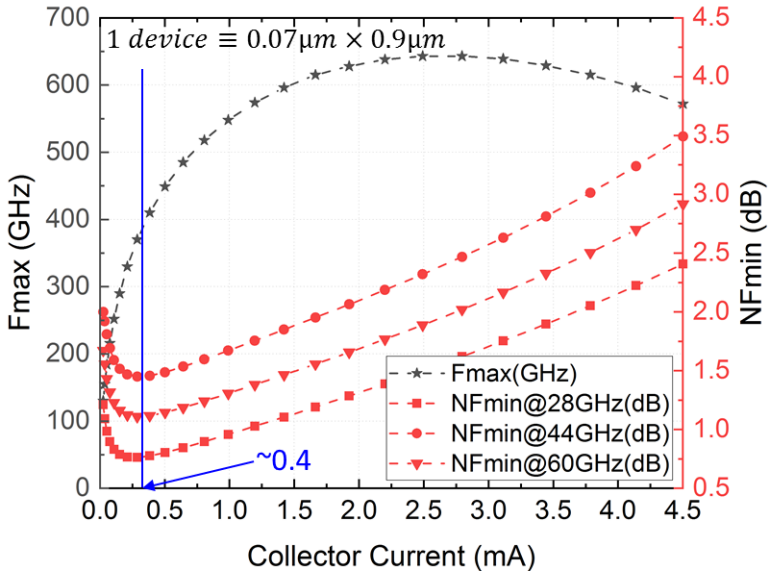


Figure 2.21 The F_{max} and NF_{min} for a 0.07 μm × 0.9 μm transistor.

where n is the collector ideality factor, β_0 is the dc current gain, f is the design frequency, f_T is the transit or cut-off frequency, r_b is the base resistance and r_e is the emitter resistance [30]. As

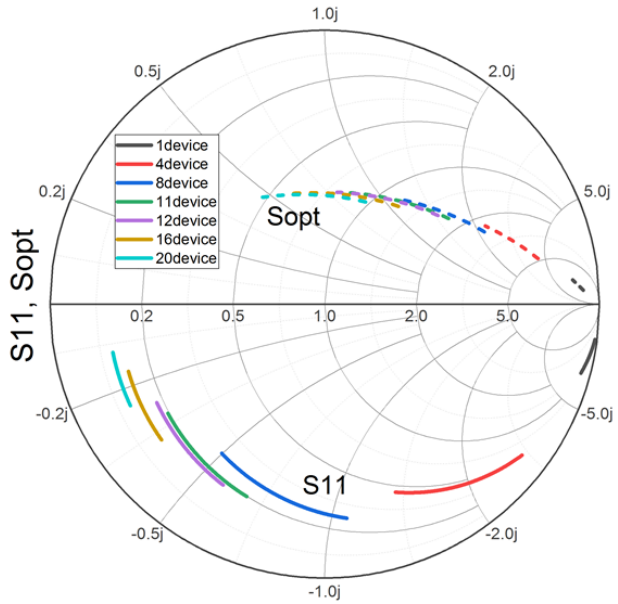


Figure 2.22 The simulated S11 and Sopt for different devices sizes.

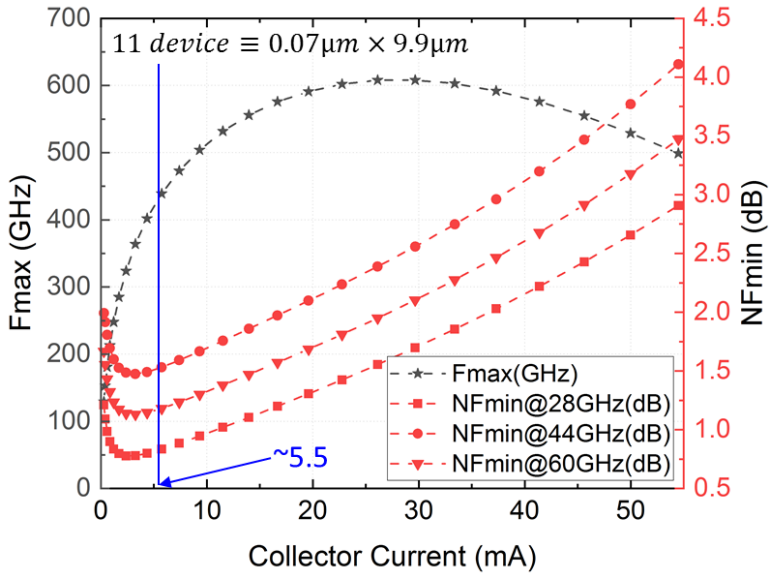


Figure 2.23 The F_{max} and NF_{min} for a 0.07 μm × 9.9 μm transistor.

long as the emitter length to width ratio is larger than 10, the minimum noise figure is practically independent of the transistor size and depends only on the collector current density. Hence, the NF_{min} and the f_{max} for the smallest device of dimension 0.07 μm × 0.9 μm was simulated as shown

in Figure 2.21. However, the input impedance and the optimum noise source impedance of a single device is very high.

The input impedance of the LNA is very crucial because it requires to match for noise and power simultaneously. Hence the transistor sizes were scaled and selected such that the optimum noise source resistance is around 50 Ω. The bottom transistor size of the first stage was chosen to be 0.07 μm × 9.9 μm with a total collector current of 5.5 mA. Figure 2.22 depicts the input impedances (S11) and optimum noise source impedance (S_{opt}) for various device sizes and Figure 2.23 shows the NF_{min} achievable for the chosen size at 28 GHz, 44 GHz and 60 GHz respectively. The noise correlation susceptance is then canceled using the inductors at the base and emitter. Since the emitter degeneration inductor, when lossless, provides a real input impedance of 50 Ω without changing the optimum noise source impedance, it was optimized to bring the S11 on the 50 Ω circle of the Smith Chart. However, the emitter degeneration tends to make the gain equation a weaker function of the transconductance (g_m) of the common-emitter (bottom) transistor without worsening the NF [31]. In other words, there is a trade-off between choosing a perfect 50 Ω real part matching and gain. Finally, the input matching network at the base is used to achieve a reasonable input power match [32]. Figure 2.24 depicts the input matching network, the S11*, the gain degradation and NF with and without emitter degeneration. An inductance value of 45 pH was chosen for emitter degeneration which gave an S11 less than -10 dB sacrificing 3 dB gain and insignificant deterioration in NF.

A T-type matching topology was used for the interstage matching (IMN) [33]. Since, the noise of the second stage of the 2-stage cascode is not very significant, only the output impedance of the first was matched so that it sees an optimal load impedance for power match. The IMN was realized by matching the output of the 1st stage and input of the 2nd stage to 50 Ω separately. Since

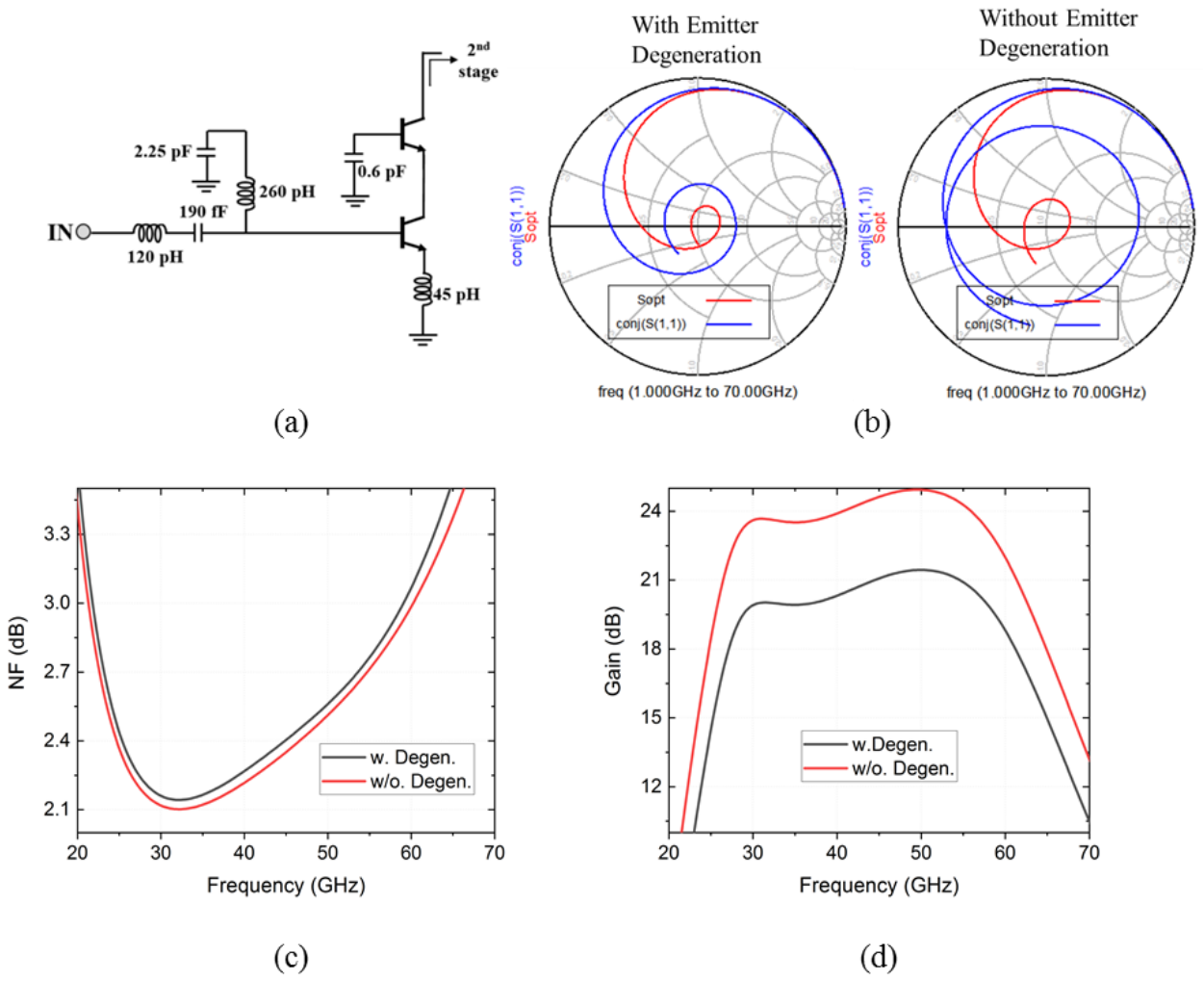


Figure 2.24 (a) The input matching network of the LNA; and the effect of emitter degeneration on (b) S11* and Sopt, (c) NF and Gain.

the primary goal was to achieve a wideband matching, the peak for the 1st stage was skewed to the lower frequency of the band of interest and the 2nd stage peak gain skewed more towards the higher frequency within the band. The detailed steps are given in Figure 2.25. In the first step, the input of the 2nd stage was matched using the same approach used for the 1st stage- emitter degeneration (L_E) to match the real part followed by the inductor L_3 for the imaginary part (Figure 2.25 (a)). For the output of the 1st stage, it was more challenging to match the impedance at the collector of the cascode, hence a T-type matching with a parallel resistor R_1 was employed to match the entire frequency band of interest (Figure 2.25 (b)). Finally, the two stages are combined and optimized

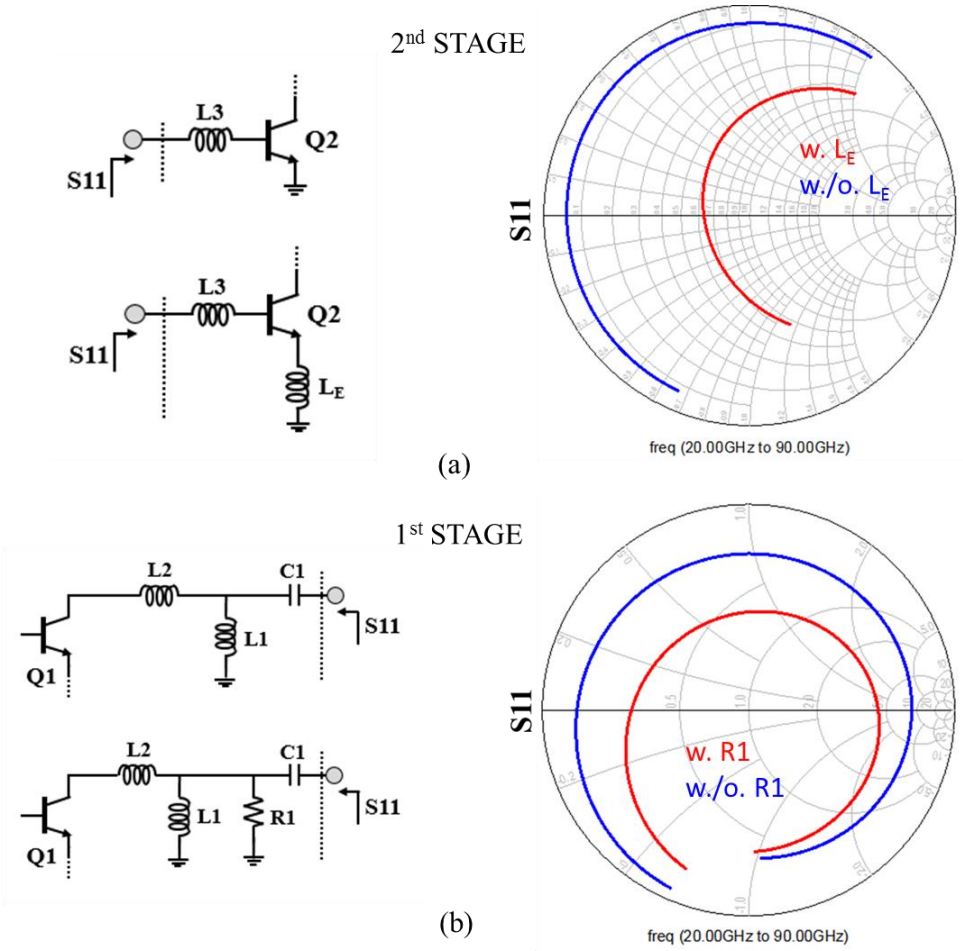


Figure 2.25 The circuit schematic and the S11 for (a) the input of the 2nd stage, (b) the output of the 1st stage, (c) overall IMN with S11 for both of the above matching sections.

to obtain a wideband performance by bringing input and output of the two stages closer (Figure 2.25 (c)). The resulting gain and IMN are depicted in Figure 2.26 and shows excellent gain flatness

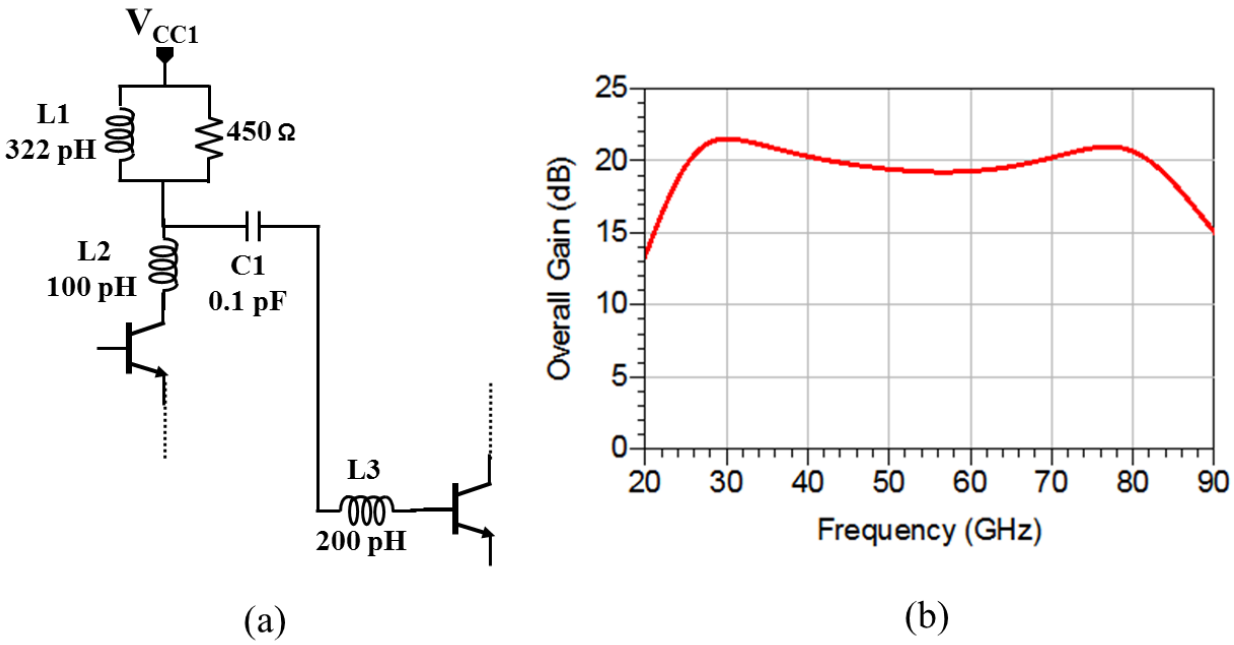


Figure 2.26 (a) The optimized IMN with the exact values; and (b) the overall simulated gain after IMN.

within 3-dB of 21.5 dB gain at the desired bandwidth (24-84 GHz).

For the output, a broadband output matching would cause gain roll-off at higher frequencies as it will follow the trend of the maximum available gain (MAG). Hence, a narrow-band L-type matching network with a resistor in shunt with the inductor was realized as shown in Figure 2.20.

All the passives including the inductors and capacitors used for input, interstage and output matching were optimized by electromagnetic (EM) simulation using ADS Momentum. For example, the EM simulated interstage matching network is shown in Figure 2.27.

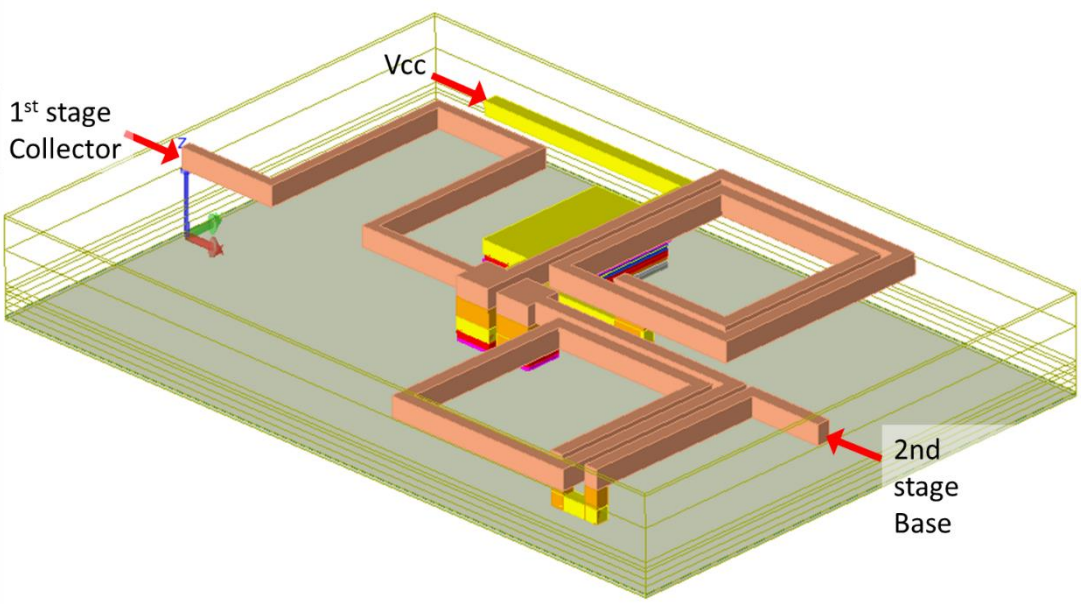


Figure 2.27 EM simulated IMN structure using ADS Momentum.

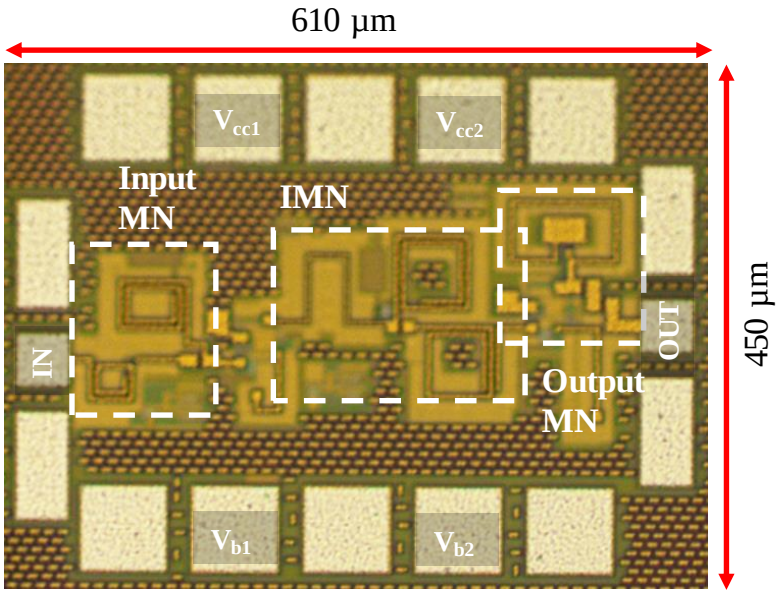


Figure 2.28 Chip photograph of the multiband LNA.

2.4.2 Measurement Results

The Multiband LNA was fabricated in 0.13-µm IHP Microelectronics SG13G2 process as shown in Figure 2.28. The overall dimension of the chip is 610 μm × 450 μm and 510 μm × 290 μm excluding the pads. The common-emitter (lower) transistors sizes for the were chosen to be 11

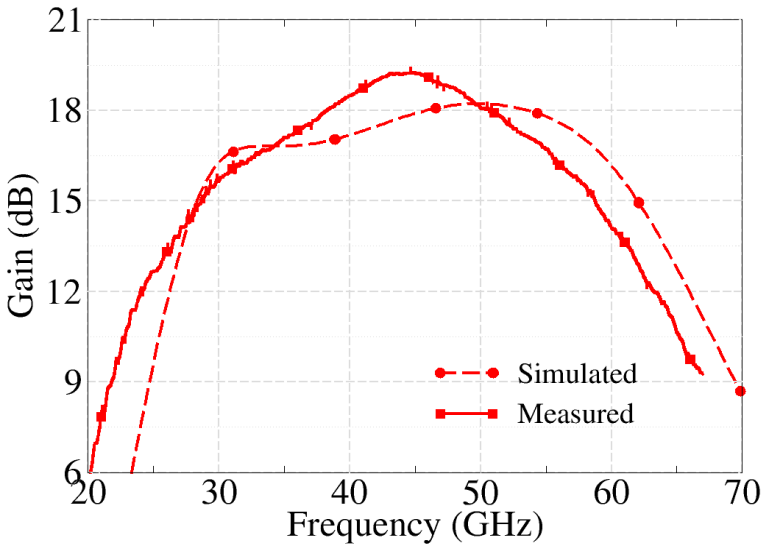


Figure 2.29 Measured and Simulated Gain of the LNA.

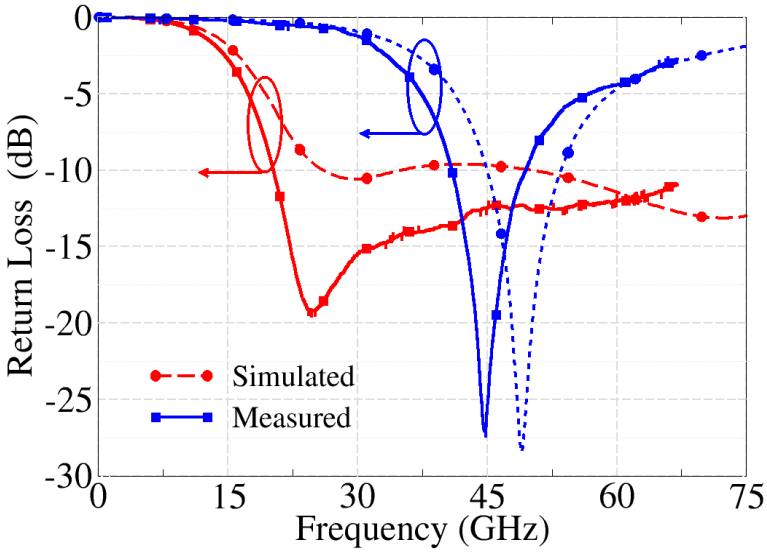


Figure 2.30 Measured and Simulated Return Loss of the LNA.

× 0.07 μm × 0.9 μm and 14 × 0.07 μm × 0.9 μm for the first and second stage and the common-base (upper) transistors were 12 × 0.07 μm × 0.9 μm and 11 × 0.07 μm × 0.9 μm respectively.

The measured and simulated S-parameters of the multiband LNA is shown in Figures 2.29 and 2.30. S-parameters were measured using the Agilent N5227A PNA Network Analyzer (for 0.1-67 GHz) and 100 µm probe pitch GSG MPI Titan probes. The measured gain of the LNA is

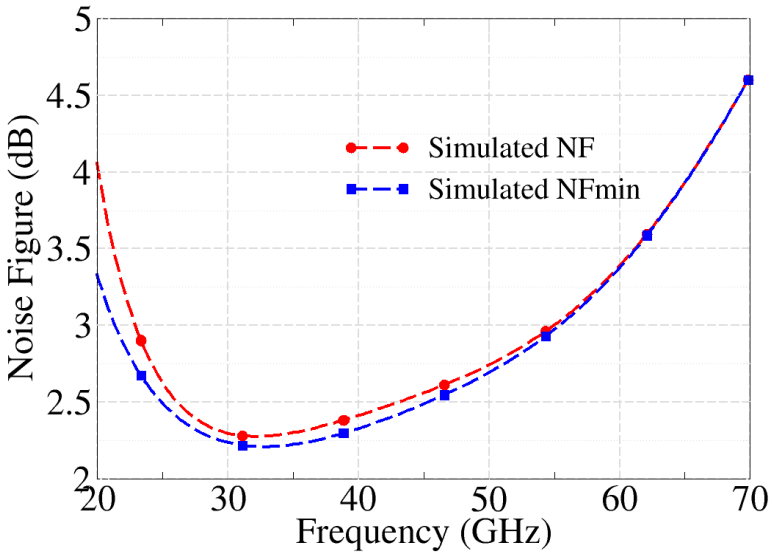


Figure 2.31 Simulated NF and NFmin of the LNA.

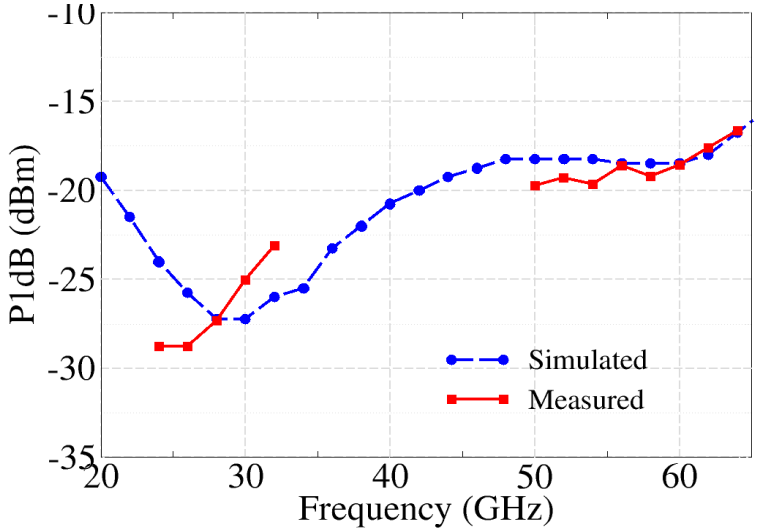


Figure 2.32 The measured and simulated input-referred P1dB of the LNA at 28 GHz and 60 GHz.

greater than 10 dB from 22.2-65.5 GHz with maximum gain of 19.25 at 45 GHz. Gain is greater than 14 dB from 28 GHz-60 GHz with 14.5 dB and 14.1 dB at 28 GHz and 60 GHz respectively. The measured input return loss is less than -10 dB from 22-67 GHz. Figure 2.31 shows the simulated NF and NF_{min}. The mean noise figure from 28 GHz-60 GHz is 2.87 dB with 2.361 dB at 28 GHz and 3.38 at 60 GHz. Due to equipment limitations, the linearity for the LNA was

measured around Ka- and V-band and plotted in Figure 2.32. The input-referred P1dB was found to be -27.3 dB and -18.6 dB for 28 GHz and 60 GHz.

A comparison of the realized LNA with published state-of-the-art K-band, Q-band and V-band LNA is shown in Table 2.2. Based on the figure-of-merit calculated, the realized LNA's performance is comparable to other designs at narrow-bands, but if the bandwidth and multi-band feature is taken into account along with other performance metrics, the realized LNA is superior to most of the published LNAs in similar silicon and SiGe technologies.

2.5 Downconverting Mixer

A mixer is a non-linear RF block that translates one frequency to another frequency depending upon the application. The downconverting mixer converts a high radio-frequency (RF) signal to a low intermediate frequency (IF) signal and it is part of the receiver chain. In this section, we discuss the design of the wideband downconverting mixer that achieves a bandwidth in excess of 100 GHz.

Different types of circuit topologies have been proposed for the design of mixers [34]–[40] in silicon technologies with wide RF and IF bandwidth. Some of the most common topologies include distributed mixers [36], [39], [40], cascode mixer [35] and ring mixer [38]. All of these examples achieve limited performance and typically require large chip area.

In our work, we realized an extremely compact downconversion mixer using the micromixer topology [41]. To facilitate further miniaturization, active baluns are incorporated at the LO and IF ports. The inherent property of the micromixer to provide well-defined matching impedance at the RF input along with the active baluns enables the wideband operation of the circuit.

Table 2.2 Performance Comparison of the Multi-band LNA with the State-of-the-art

	Reference	Technology	Freq. (GHz)	Gain (dB)	Noise Figure (dB)	IP1dB (dBm)	Area (mm^2)	F.O.M.	Power (mW)
	This work	**130 nm SiGe**	**28-60**	**14.5@28GHz 19.2@45GHz 14.1@60GHz**	**2.87* (mean) 2.36@ 28GHz 3.38@ 60GHz**	**-27.3*@28GHz -19@44GHz -18.5@60GHz**	**0.142**	**4.28 (Ka-) 8.09 (Q-) 1.94 (V-band)**	**26.8**
K-band	MTT'14 [32]	180 nm SiGe	16-24	19	2.2	-16	0.485[a]	5.63	22.5
	BCTM'17 [42]	250 nm SiGe	19.25-21.5	32.8	3.5	-34.3	0.117	4.22	7
	CSICS'13 [43]	45 nm CMOS SOI	16-24	19.5	2.2	-18.5	0.15	7.03	18.5
	RFIT'15 [44]	90 nm CMOS	22.7-24.7	20	3.6	-	0.349	0.93	16.5
Q-band	MTT'12 [45]	90 CMOS (LP)	29-44	13.8 @37 GHz	3.8** @ 37 GHz	-11.1	0.4826	4.11	18
V-band	IMS'17 [46]	130 nm SiGe	55-66	15	3.3-3.6	-13.5	0.11	3.44	19.6
	MWCL'16 [47]	180 nm SiGe	43-67	32.5	6[b]	-38	0.39	13.33	11.7
	IJSSC'13 [33]	250 nm SiGe	47-77	22.5	6.8[b]	-17.5	0.5	2.24	52
	MTT'15 [48]	28 nm SOI CMOS	54.5-72.5	13.8	4	-12.5	0.38	3.45	24
	EuMC'13 [49]	90 nm CMOS	55-61	22	3.7	-23	0.6	3.62	13.5

$F.O.M. = \frac{Gain(dB).BW(GHz)}{[NF(dB)-1].P_{DC}(mW)}$ *simulated [a]including pads [b]average noise figure

The micromixer achieves a conversion gain of 6±1 dB for measured 5-67 GHz and simulated up to 120 GHz RF frequency with fixed 1 GHz IF, an IF bandwidth of 16 GHz, the input-referred P1dB of -13.4 and -12.7 for an RF of 28 and 60 GHz and occupies an area of 152μm × 120μm excluding pads. The RF, LO and IF port return losses are less than -10 dB for the frequency band. When compared to any single circuit topology in terms of both RF and IF bandwidth, the realized mixer shows superior performance than rest of the mixers in similar silicon and III-V technologies.

2.5.1 Circuit Description

A. Micromixer Core

The circuit schematic of the realized downconversion mixer is shown in Figure 2.33. The RF stage consists of one common-base (CB) amplifier M3 and one common-emitter (CE) amplifier M2. When M1 and M2 are connected as current mirror, M3 and M2 achieves transconductance gain of equal magnitude but 180º out-of-phase, hence performing the single to differential-ended conversion. Since the input impedance of the RF stage is $1/g_{m3} \,||\, (1/g_{m1} + 200)$ Ω, the bias current was chosen such that the input impedance is 50 Ω. Also, such matching eliminates reactive components that are frequency dependent and bulky. Minimum device size was chosen for M5-M8 for faster switching. Resistive loads were used for wide IF bandwidth. Higher resistance values provide higher conversion gain at the expense of voltage headroom, whereas the gain from smaller resistance is inadequate to deliver sufficient gain. Therefore, a value of 250 Ω was chosen for moderate conversion gain while maintaining low supply voltage and wide bandwidth. The dimensions of the M1-M4 and M5-M8 transistors were 0.07μm×1.8μm and 0.07μm×0.9μm each.

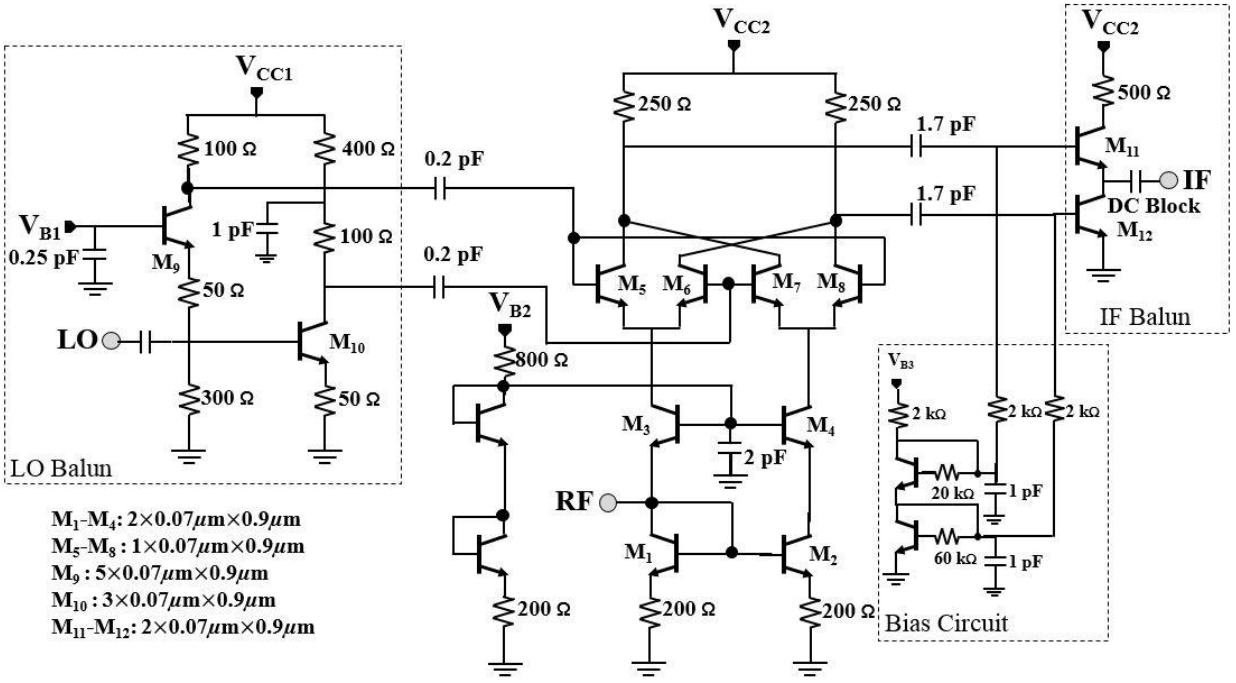


Figure 2.33 Circuit Diagram of the Downconversion Mixer.

B. LO and IF Balun

A common-emitter/common-base (CE/CB) topology was chosen for the LO balun design to convert the single-ended LO input to differential input for the switching core. The emitter-degeneration and DC path resistor of the transistors of the LO balun was chosen so that the LO input was 50 Ω as well [50]. Since the frequency response of the CB amplifier is better compared to CE amplifier due to the Miller capacitance, the CB transistor (M9) was chosen to be larger than the CE (M10) to compensate for this effect. The performance of the LO balun was simulated separately and then optimized with the mixer core. M9 and M10 has device sizes of 0.07μm×4.5μm and 0.07μm×2.7μm. The simulated amplitude and phase imbalance were within 1 dB and 14º for the frequency band. DC blocking capacitors were placed between the LO balun and the switching core and the core was biased using a separate bias circuit.

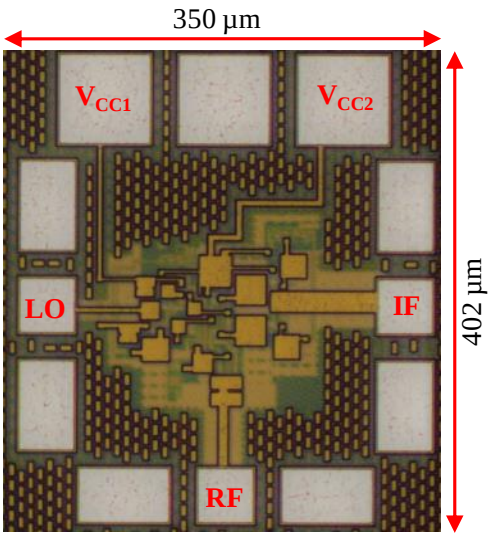


Figure 2.34 Chip photograph of the Downconversion Micromixer.

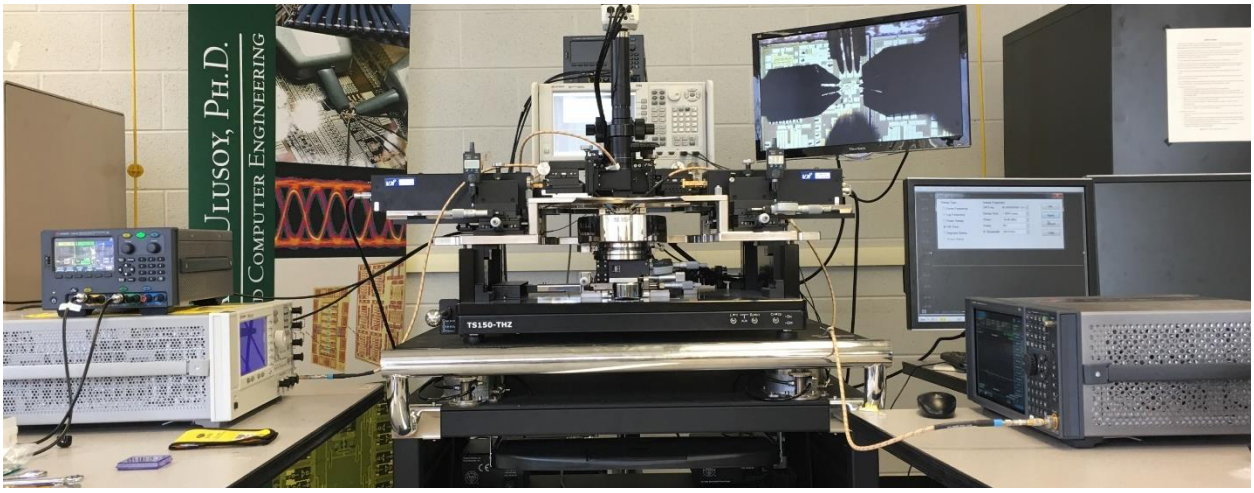


Figure 2.35 Measurement Setup.

In a similar design approach, the IF balun uses a Common-emitter/common-collector (CE/CC) push-pull configuration. Both M11 and M12 were 0.07μm×1.8μm. The output impedance is adjusted to be 50 Ω by adjusting the collector current.

2.5.2 Measurement Results

The micromixer was implemented in 0.13-μm IHP Microelectronics SG13G2 BiCMOS process with 300 GHz-f_T/500 GHz-f_{MAX} occupying a total area of 0.14 mm^2, whereas 0.019 mm^2

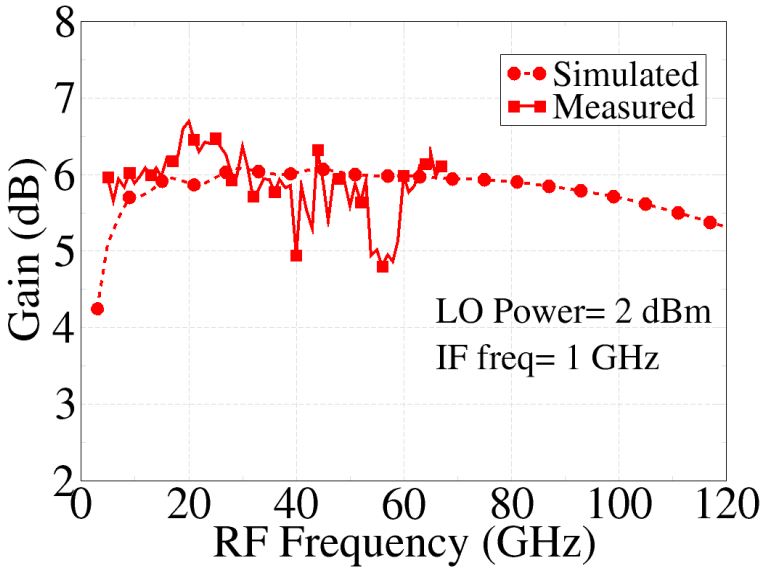


Figure 2.36 Simulated and measured conversion gain of the micromixer as a function of RF frequency.

excluding the pads. The mixer uses a 3.5 V DC supply and consumes 45 mW power. The chip micrograph is displayed in Figure 2.34.

The measurement setup is shown in Figure 2.35. The setup uses the Keysight E8257D signal generator for the LO input, Agilent N5227A PNA Network Analyzer in CW-mode as RF excitation and a Keysight EXA Signal Analyzer to measure the IF frequency and power. The measured performance is shown in Figure 2.36, 2.37 and 2.38.

Figure 2.36 shows the simulated and measured conversion gain up to 120 GHz and 5-67 GHz RF frequency with constant IF frequency of 1 GHz and an LO power of 2 dBm. The measured conversion gain was found to be 6±1 dB from 5-67 GHz which is in close agreement with the simulated result. Based on this measurement, it can be asserted that the RF bandwidth follows the trend similar to simulation and it is expected to yield an RF bandwidth of 120 GHz. Due to equipment limitations, the W-band measurement for the mixer could not be performed. The LO power was also swept at 60 GHz RF and 59 GHz LO frequency and it was found that the output

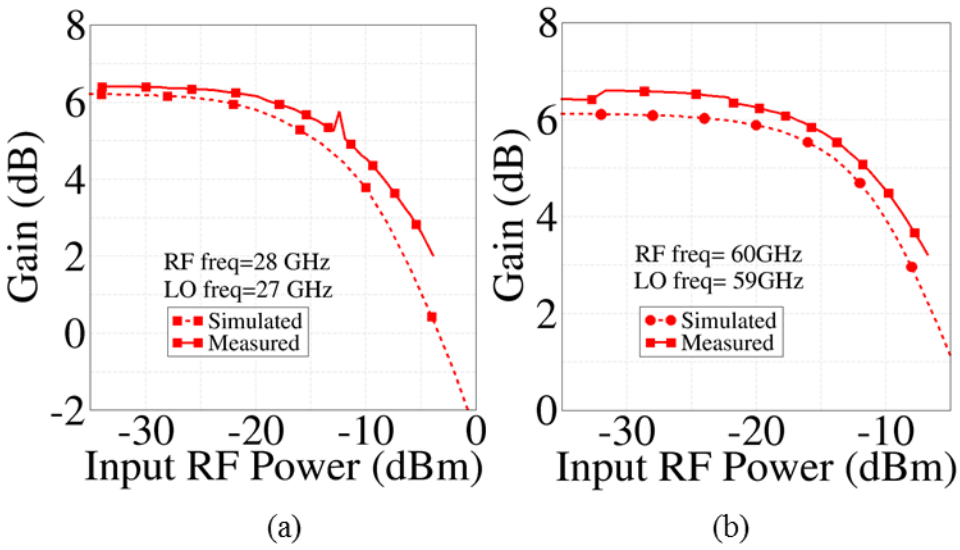


Figure 2.37 Simulated and measured conversion gain of the micromixer as a function of RF power with (a) 28 GHz RF frequency, and (b) 60 GHz RF frequency.

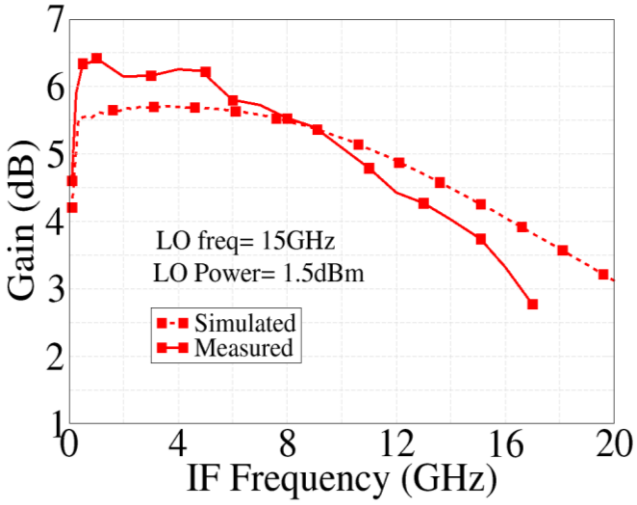


Figure 2.38 Simulated and measured gain of the micromixer as a function of IF frequency.

power starts to saturate after 0 dBm. Therefore, we opted to use an LO power of 2 dBm. The gain of the micromixer as a function of RF input power at 28 and 60 GHz is plotted in Figure 2.37. The measured input-referred P1dB was determined to be -13.4 dBm for 28 GHz and -12.7 for 60 GHz. The IF was measured with an LO frequency of 15 GHz and LO power of 1.5 dBm. The 3-dB bandwidth for the IF port was found to be 16 GHz and displayed in Figure 2.38. The return losses for the RF, LO and IF ports were measured and depicted in Figure 2.39. All of them have less than -10 dB loss for their respective bands of interest.

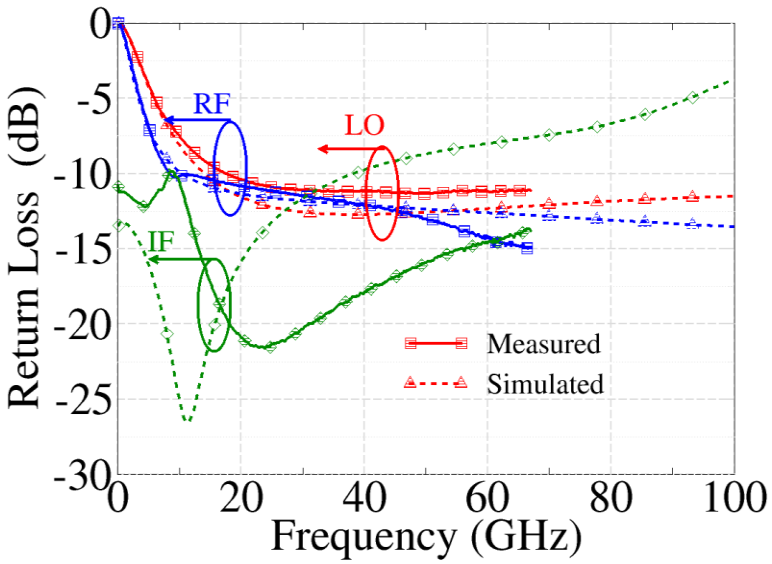


Figure 2.39 Return Losses for the RF, LO and IF ports.

A comparison of the realized downconverting mixer with other state-of-the-art wideband mixers is tabulated in Table 2.3. The performance of the realized mixer is better than most of the state-of-the-art mixers in similar technologies. However, the extremely compact size gives the micromixer a clear advantage over the other mixers in terms of chip area.

2.6 Upconverting Mixer

The upconverting mixer is one of the most important blocks for transmit-section of the transceivers, particularly in millimeter-wave regime for converting low intermediate frequency (IF) to high radio-frequency (RF) transmit signal at the input of the power amplifier (PA) followed by the transmitting antenna. The power-handling capability and the linearity of the upconverting mixer is therefore important as it needs to provide the required input power to the PA. Although III-V technologies are commonly the preferred choice for PAs, the other transmitter components are typically built in silicon technologies which provide high integration density and a low-cost platform for large-scale market production.

Table 2.3 Performance Comparison of the Wideband Downconverting Micromixer with the State-of-the-art

Reference	Techno-logy	Topology	RF BW (GHz)	RF Frac. BW (%)	CG (dB)	IF BW (GHz)	Area (mm^2)	LO Power (dBm)	Pdc (mW)
This work	**0.13-µm SiGe**	**Micromixer**	**5-120 (sim) 5-67 (meas)**	**184% (sim) 172% (meas)**	**6**	**16**	**0.019 0.14***	**2**	**45**
ICNF'17 [34]	0.13-µm SiGe	Double balanced Mixer	5-50	164%	9	0.001-0.1	0.014^{+}	0	100
TTST'15 [35]	0.13-µm SiGe	Cascode	5-95	180%	5.5 14.5	5.8(at RF 20GHz) 5(at RF 70GHz)	1.2 2	1	130 170
IMS'16 [36]	0.18-µm SiGe	Distributed mixer using NMOS HBT Darlington cell	2-67	188%	3	0.59	0.418	0	17.5
MTT'16 [37]	90 nm CMOS	Fundamental Drain/Gate Pumped	30-90	100%	-7.7±1.5 -10.1± 1.5	dc-26 @LO 30GHz dc-23 @LO 60GHz	0.389	2.3-2.6 (30-67 GHz)	0.6
MTT'12 [38]	90 nm LP CMOS	Fundamental Ring	40-110	94%	-1±2	1.5	0.22	-2	7.2
MTT'09 [39]	0.13-µm CMOS	Fundamental distributed drain pump	0.8-77.5	196%	-5.5	2	0.388	10	0
MWCL'13 [40]	0.18-µm CMOS	Distributed Cascoded Mixer	5-45	160%	-12	5	0.66	8	1.4
IMS'18 [51]	GaAs pHEMT 0.1-µm	Cascode	34-53	44%	3-13	0.8- -1.1(@ LO 31GHz 0.4- -2.1@ LO 35GHz -2- -4@ LO 40GHz	2.25	0	36

*including pads $^{+}$Active area without on-chip baluns

As part of this dissertation, we present one Ka-band and one V-band GHz upconverting mixer for millimeter-wave transmitters in a 0.13-μm SiGe BiCMOS process. Both circuits show excellent linearity with OP1dB of -1.5 dBm at 28 GHz for the Ka-band and -1.4 dBm at 60 GHz for the V-band. The Ka-band mixer has maximum conversion gain of 13.7 dB at 26.5 GHz, 3-dB bandwidth of 24-32 GHz and has an area of 0.218 mm^2. For the V-band mixer, the maximum conversion gain is 13.4 dB at 57 GHz, 3-dB bandwidth is 50-67 GHz and occupies 0.146 mm^2. Both mixers use transformer-based baluns at the LO and RF ports to achieve the very compact design. Such performance is comparable to any state-of-the-art Ka-band and V-band in III-V technologies while they outperform most of those that are demonstrated in CMOS and BiCMOS processes.

2.6.1 Circuit Description

In this section, we will discuss in detail the design of the upconverting mixers. We will start with the design procedure of the on-chip transformer for the Ka-band that enabled the compact design. Similar approach was used for the V-band design as well.

The schematic of the Ka-band upconverter mixer is shown in Figure 2.40. It consists of a double-balanced Gilbert cell core with two on-chip transformer baluns. The transformer baluns were preferred for efficient usage of chip area, as they allow DC feeding via the center tap, and at the same time act as resonant loads at the desired frequency. However, the symmetry of the balun becomes crucial for the mixer performance. Figure 2.41(a) depicts the equivalent circuit for the balun transformer including the parasitic component C_F generated due to capacitive coupling between the coils. This configuration leads to a strong asymmetry because C_F results in different low-pass response for each half of the circuit. The upper half in Figure 2.41(a), having the C_F in the feedback path, exhibits a lower corner frequency than the lower half [31], where C_F shunts L_{S2},

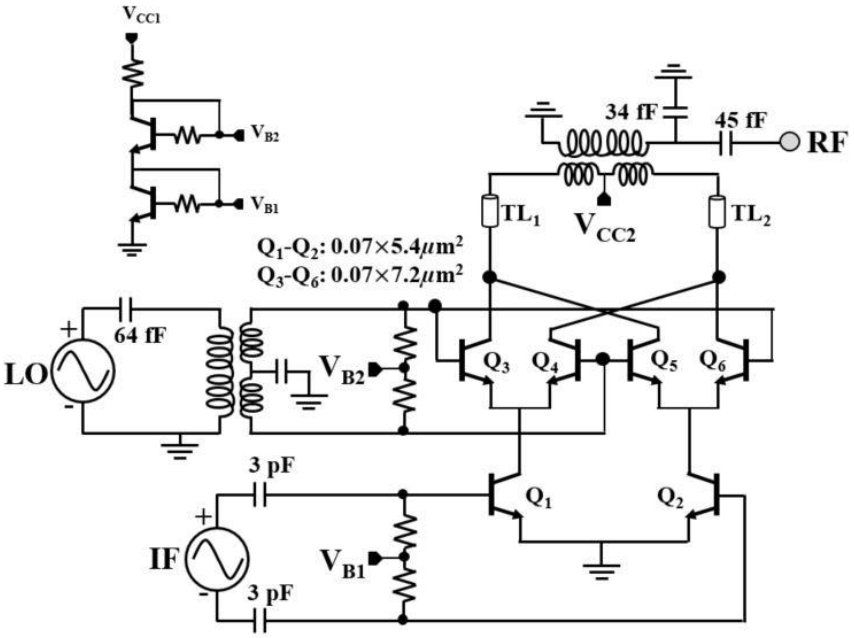


Figure 2.40 Circuit diagram of the Ka-band Upconverting Mixer.

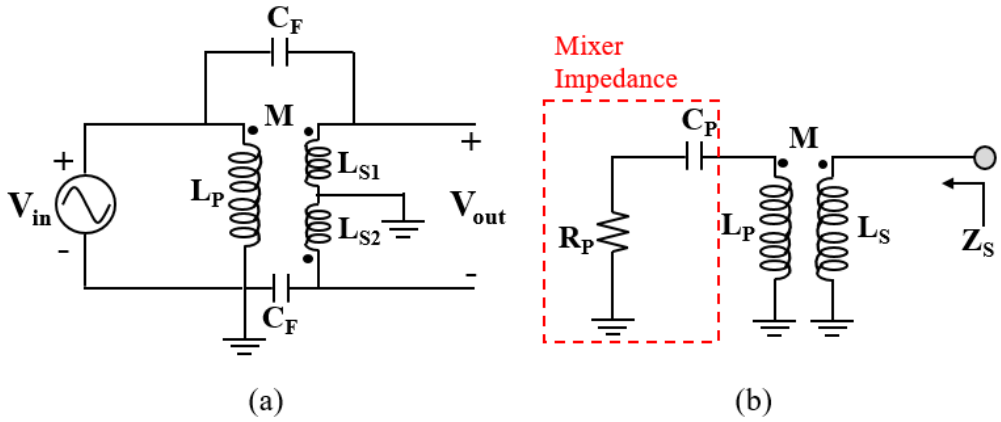


Figure 2.41 Transformer (a) as a balun including capacitive coupling between the windings, (b) resonant load connected to mixer output.

creating a lowpass response with higher cut-off frequency [31]. The difference in cut-off frequency in each half results in amplitude and phase imbalance when operated as a balun.

The simplest approach to reduce the impact of C_F is to minimize the transformer dimensions. This, however, will reduce the coupling factor of the transformer, significantly limiting the bandwidth of the circuit. The impact of low coupling factor is analyzed through the

circuit shown in Figure 2.41(b). Here, we assume the transformer is connected to an arbitrary complex load modeled by a resistor and capacitor; for instance, this could be seen as the output impedance of the mixer. When we analyze the resulting impedance Z_S, we acquire the following expression:

$$Z_S = \frac{C_P M^2 \omega^2 + C_P M^2 \omega^2 L_P R_P}{(1 + R_P C_P L_P)^2 + (\omega C_P L_P)^2} + j\omega \left[L_S - \frac{{C_P}^2 M^2 \omega^2 L_P}{(1 + R_P C_P L_P)^2 + (\omega C_P L_P)^2} \right] \quad (2.3)$$

Here, M is the mutual inductance with $M = k\sqrt{L_P L_S}$ and k is the coupling coefficient. From this expression, we see that the real part of Z_S is proportional to the square of M, while the imaginary part is inversely proportional to the square of M. The outcome of this analysis is that a too small coupling factor will result in a mostly imaginary impedance, requiring a high-Q, possibly higher order matching network. On the other hand, a too large transformer will perform poorly as a balun, due to the capacitive coupling between the windings. In order to demonstrate this effect, simulations of various transformer baluns are provided in Table 2.4. In Figure 2.42 details of the designed transformer are presented.

The baluns are designed in two basic configurations either using the two top-most metals (TM2-TM1) or using a top-metal layer with two lower layers tied together (TM1-M5+M4). A broadside coupled design is preferred, as sufficient coupling can be achieved while enabling a very compact implementation. The width of the coils was chosen to be 6 µm to achieve desired coupling factor, without contributing too much to the capacitive coupling between the stacked coils. The simulation results confirm the predictions; a larger transformer yields a higher coupling factor but a stronger imbalance. As the transformer size is reduced, balun performance improves, but low coupling

Table 2.4 Balun Dimensions for Ka-Band Upconverter

Metal Layers	W_{in} (μm)	L_{in} (μm)	Coupling factor	Imbalance	
				Amp. (dB)	Phase (°)
TM2-TM1	39	201	0.547	0.302	1.088
TM2-TM1	39	281	0.619	0.441	1.815
TM2-TM1	149	281	0.846	0.601	3.052
TM1-M5+M4	27	281	0.871	0.612	6.195
TM1-M5+M4	39	281	0.935	0.605	6.585

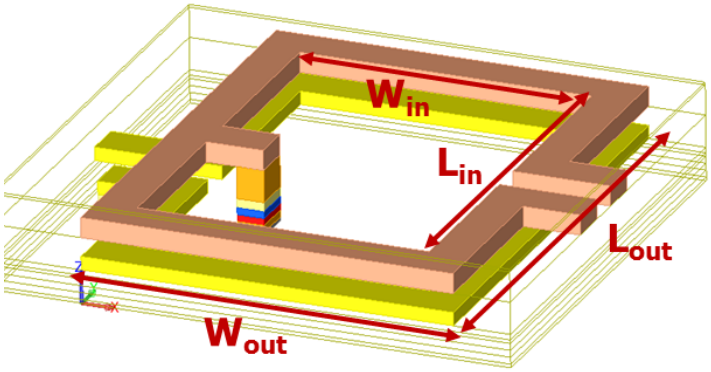
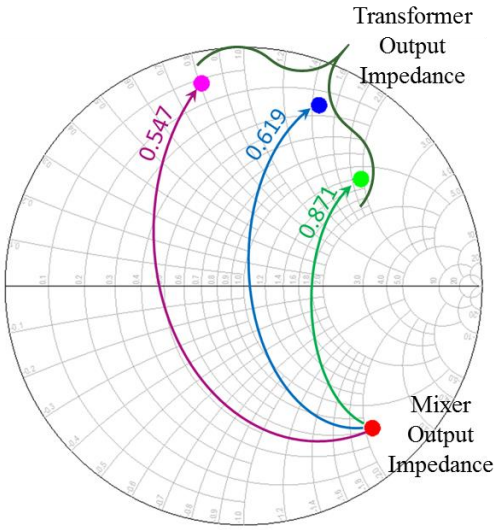


Figure 2.42 Transformer balun used for LO and RF ports.



Metal Layers	Transformer Balun size	Coupling factor	Imbalance	
			Amp. (dB)	Phase (°)
TM2-TM1	Small	0.547	0.302	1.088
TM2-TM1	Optimum	0.619	0.441	1.815
TM1-M5+M4	Large	0.871	0.612	6.195

Figure 2.43 Impedance Transformation by the transformer for different coupling factors.

factor converts the mixer impedance to a high-Q point. For instance, for a k=0.871, the mixer output impedance is closer to the origin whereas for k=0.547, it is the furthest (Figure 2.43). Based

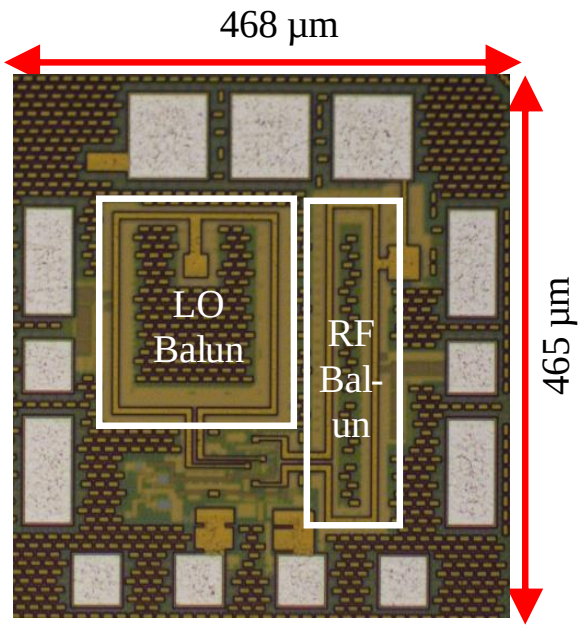


Figure 2.44 Chip photograph of the fabricated Ka-band upconverting mixer.

on these studies, we choose the TM2-TM1 transformer with a coupling factor of 0.619, trading off circuit size, balun performance and bandwidth. By providing sufficient coupling factor, the rest of the matching network design, as shown in Figure 2.40, is significantly simplified, and a simple network consisting of a shunt capacitor and series transmission line that performs the connections to the measurement pads is sufficient. Figure 2.42 and Table 2.5 shows the dimensions of the LO and RF baluns. The simulated coupling factor of the LO and RF baluns are 0.6 and 0.619. The baluns are highlighted on the chip micrograph shown in Figure 2.44.

Table 2.5 LO and RF Balun Dimensions for Ka-Band Upconverter

Metal Layers	W_{in} (µm)	L_{in} (µm)	Linewidth (µm)	Coupling factor
LO Balun	149	171	6	0.6
RF Balun	39	281	6	0.619

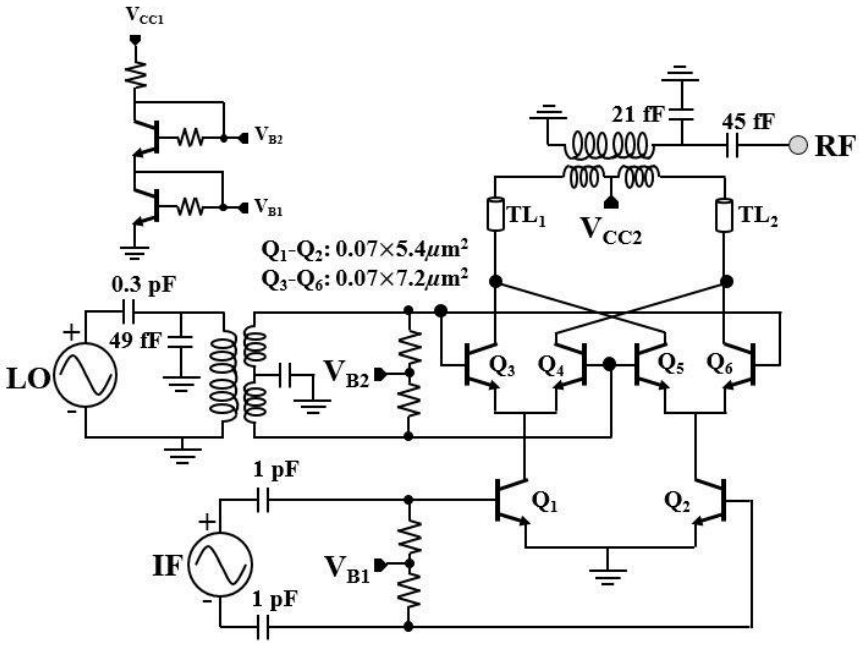


Figure 2.45 Circuit diagram of the V-band Upconverting Mixer.

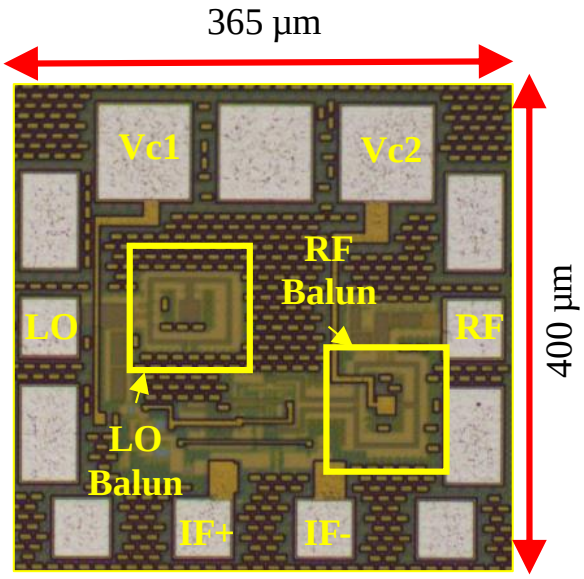


Figure 2.46 Chip micrograph of the V-band upconverting mixer.

However, with the V-band mixer, a transformer using TM1 and M5+M4 with the coupling factor of 0.62 yielded an easier matching scheme and reasonably good performance. The circuit schematic and the chip photograph for the V-band Upconverting mixer is shown in Figure 2.45 and 2.46. The same balun was used for the RF and LO ports but rotated 90º to better fit the floor

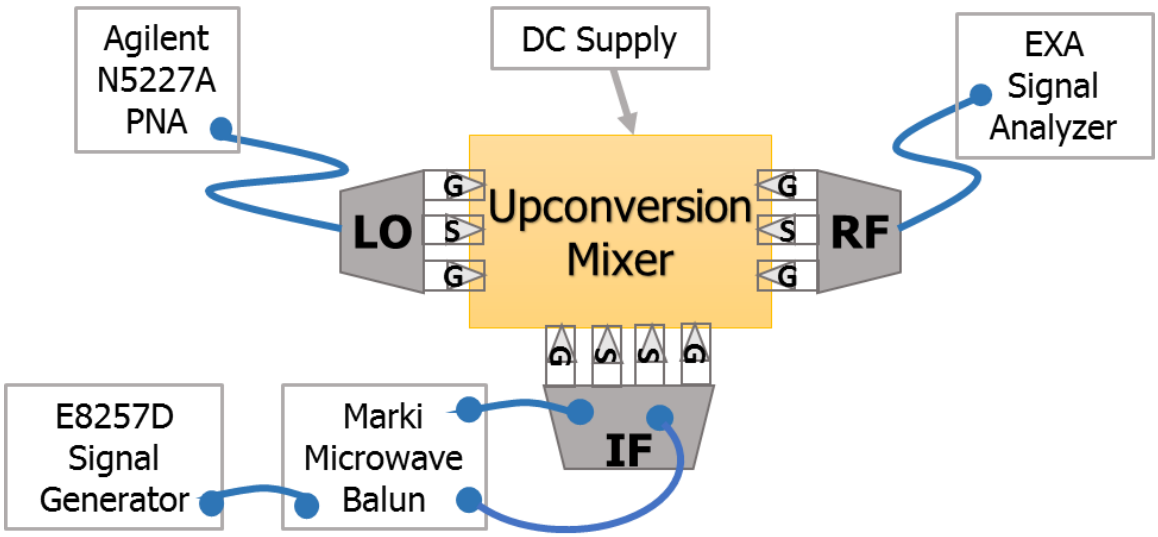


Figure 2.47 Measurement Setup for the Upconverting Mixer.

plan. They are highlighted on the chip photograph given in Figure 2.46. All the passives (including the LO and RF baluns and MIM capacitors) were EM simulated using the 2.5-D ADS Momentum simulator and optimized to enhance the performance of the mixer.

The emitters of the transconductance stage are grounded forming a pseudo-differential pair that saves voltage headroom and offers larger dynamic range. Moreover, the output RF balun does not introduce any distortion to the RF signal and hence preserves linearity [52], [53].

2.6.2 Measurement Results

The measurement setup, as displayed in Figure 2.47, consists of a Keysight E8257D signal generator with an off-chip balun from Marki Microwave as the IF input, Agilent N5227A PNA Network Analyzer in CW-mode as LO input and a Keysight EXA Signal Analyzer for measuring the RF output. 100-µm probe pitch GSG probes from GGB Picoprobes were used for chip probing. Since the Signal Analyzer can measure up to 32 GHz, an external harmonic mixer was used for V-band characterization. Both the chips were fabricated using the IHP Microelectronics SG13G2 process.

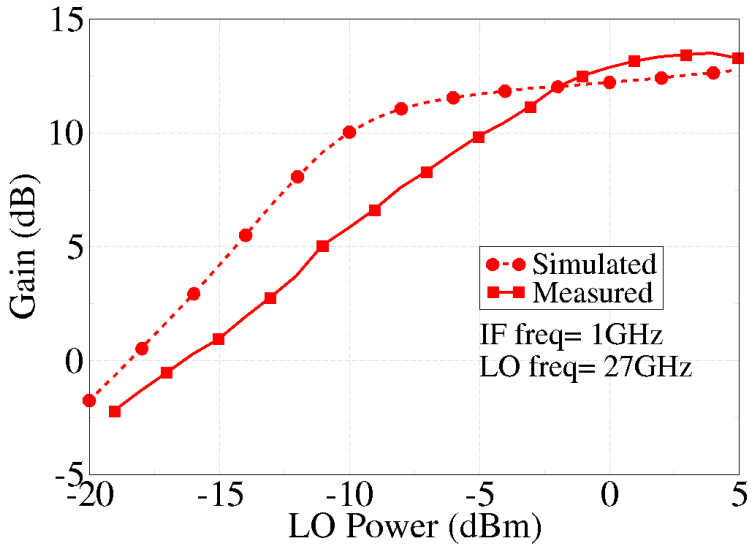


Figure 2.48 Measured and Simulated gain as a function of LO power as IF frequency is constant.

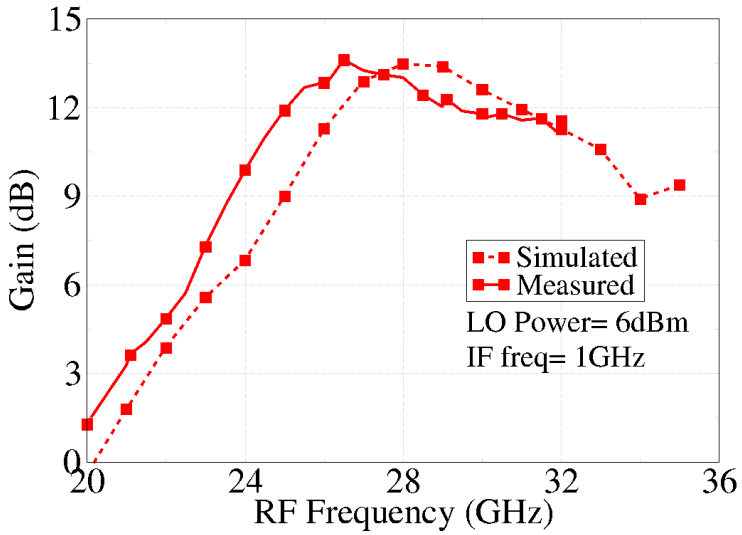


Figure 2.49 Measured and Simulated Gain as a function of RF frequency as IF frequency is constant.

2.6.2.1 Ka-band Upconverter

The realized chip of the upconverting mixer is shown in Figure 2.40 and has a total area of 0.218 mm^2. The mixer operates with a 2.5 V supply and consumes a total of 90mW DC power. The performance of the upconverter mixer are displayed in Figure 2.48, 2.49, 2.50, 2.51 and 2.52. To find an optimum value, the LO power of the mixer is swept at 27 GHz LO frequency and at 1 GHz IF frequency and the gain is plotted as shown in Figure 2.48. It is found that the gain remains

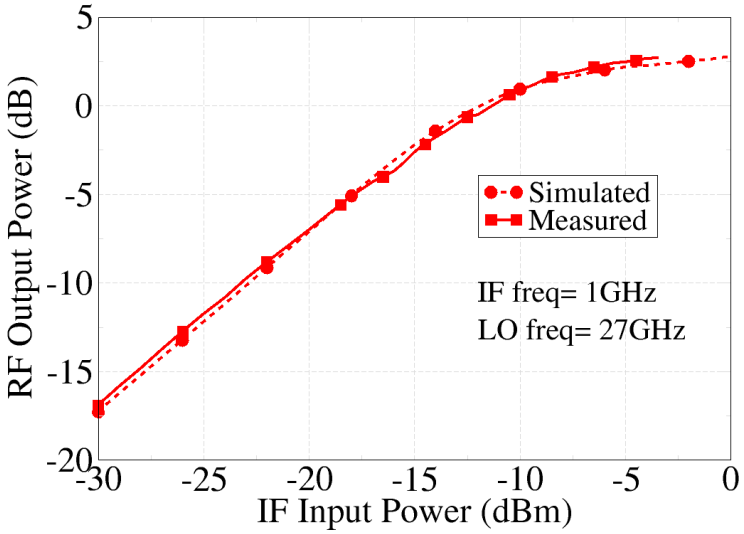


Figure 2.50 Measured and Simulated RF output power as a function of IF input power.

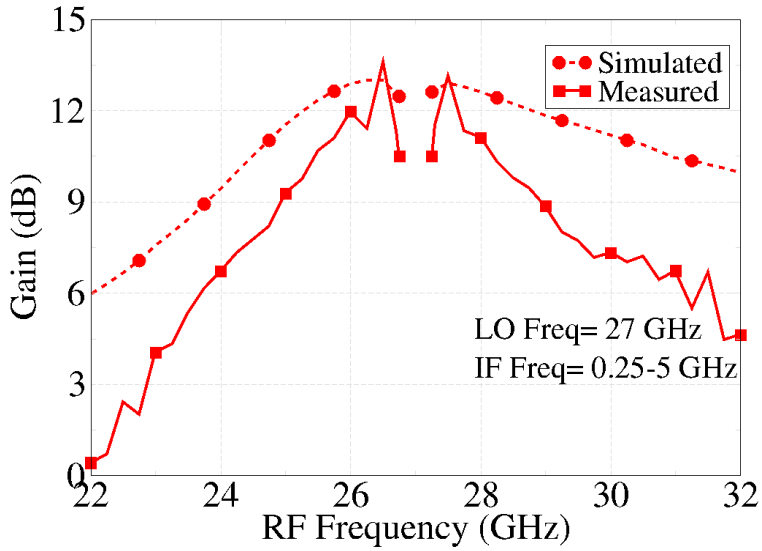


Figure 2.51 Measured and Simulated Gain as a function of RF frequency as LO frequency is constant.

constant beyond 2 dBm LO power. The conversion gain as a function of RF frequency is plotted in Figure 2.49 with constant 1 GHz IF frequency and swept LO frequency of 6 dBm power. Maximum gain of 13.7 dB at 26.5 GHz, 13 dB gain at 28 GHz and a 3-dB bandwidth from 24-32 GHz RF frequency were measured. The RF output power is displayed in Figure 2.50. The mixer has an OP1dB of -1.5 dBm at 28 GHz and can deliver 0 dBm power at -11 dBm IF input power. In terms of OP1dB, the designed circuit outperforms most of the other mixers in similar processes

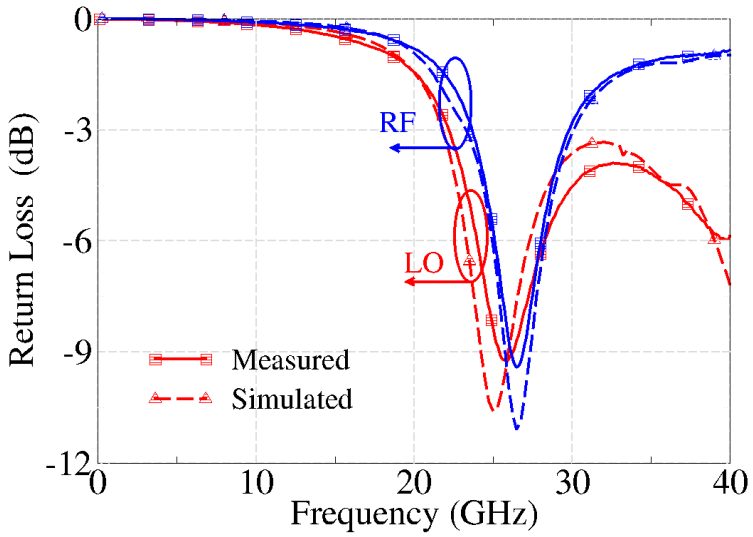


Figure 2.52 Measured and Simulated Return loss of LO and RF ports.

except [54], [55] and [56]. However, since all these use various methods to boost linearity, their chip areas are at least 3.5 times larger than this designed mixer. Only [57] has smaller chip area than the one in this work but the linearity is very poor. A comparison of the realized mixer with the state-of-the art circuits are listed in Table 2.6. Figure 2.51 shows the measured IF frequency bandwidth of 0.25-1.25 GHz on both sidebands with 27 GHz LO frequency. The return loss for the RF and LO ports is shown in Figure 2.52 and is lower than -9 dB around 28 GHz.

2.6.2.2 V-band Upconverter

The V-band upconverter occupies a total area of 0.146 mm^2 and 0.052 mm^2 with and without pads. On-chip characterization of the V-band mixer was done, and the performances are displayed in Figure 2.53, 2.54, 2.55, 2.56 and 2.57. In Figure 2.53, the gain of the mixer is plotted as a function of LO power with 59 GHz LO frequency and 1 GHz IF frequency. The optimum LO power was found to be 3 dBm beyond which the gain remains unchanged.

Table 2.6 Performance Comparison of Ka-band Upconverting Mixer with the State-of-the-art

	Freq. (GHz)	Technology	CG (dB)	OP1dB (dBm)	Power (mW)	Chip size (mm^2)	LO input (dBm)	Topology
This work	**24-32**	**130 nm SiGe BiCMOS**	**13.7* @ 26.5GHz 13 @ 28GHz**	**-1.46 @ 28GHz**	**90**	**0.21762 (0.468x0. 465)**	**5.96 @ 27GHz**	**Gilbert Cell with on-chip transformer baluns**
[58]	10-40	130 nm SiGe	3 @ 40GHz	-9 (calc.)	93	0.544	-7	Gilbert Cell
[54]	21-25	180 nm SiGe	27.5± 2.5	1.36	72	1.08	-2	Gilbert Cell
[59]	30-35	180 nm SiGe	24.5± 2.5	-2.4 @35GHz	72	NR	0.6	Gilbert Cell
[60]	19-31	180 nm SiGe	-0.8	-8.6	38	1	-4	Modified Gilbert Cell with series-conn. triplet at IF port
[55]	27.5-43.5	65 nm CMOS	-5	0.42	14	0.686	5	Modified Gilbert Cell
[56]	23.4-29.2	130 nm CMOS	-1.9	0.3	22.8[$] (core)	0.86	0	Gilbert Cell with a low distortion Gm-stage
[61]	25-27.5	130 nm CMOS	1.3	-21.7	3.9	NR	NR	Current-mode Mixer
[62]	18-28	130nm CMOS	-2- 0.7	-7- -5.2	8	0.47	3	Dual gate
[57]	15-50	180nm CMOS	-14.5± 1.5	-11.5- -7.5	0	0.2	10	Resistive Ring Mixer
[63]	30-65	150 nm GaAs pHEMT	2.22± 1.5	-2.4 @40GHz	105	1.68	2	Gilbert Cell

*maximum [$]39.3 mW for core + LO buffer

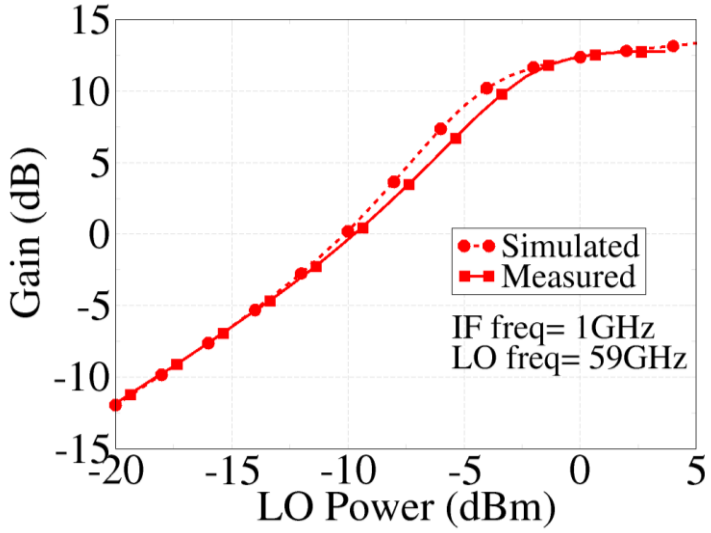


Figure 2.53 Measured and Simulated Gain as a function of LO power.

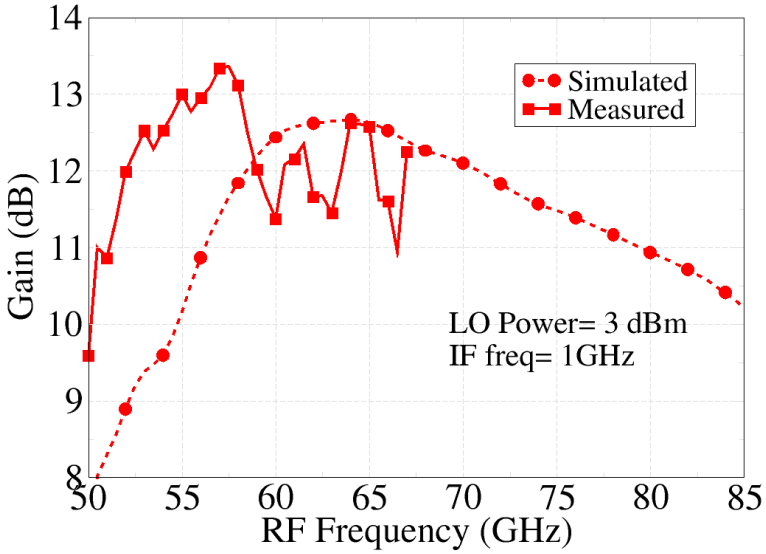


Figure 2.54 Conversion gain vs RF frequency with constant IF.

The conversion gain is obtained by sweeping the LO frequency from 49-66 GHz with 3 dBm LO power while keeping the IF frequency constant at 1 GHz. Figure 2.54 displays the measured conversion gain vs the RF frequency. It has a maximum gain of 13.4 dB at 57 GHz, 11.4 dB gain at 60 GHz and a 3-dB bandwidth from 50 to above 67 GHz RF frequency. The RF output power is shown in Figure 2.55. The mixer achieves an OP1dB of -1.4 dBm and at 3-dB compression it can deliver 0.61 dBm output power with -8.2 dBm IF input power. Figure 2.55 also

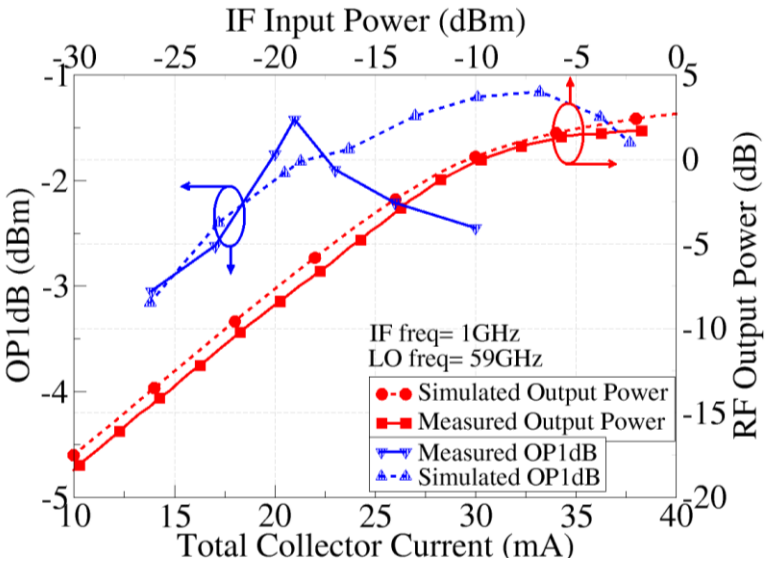


Figure 2.55 OP1dB for different bias current at 60 GHz RF frequency (left and bottom axis) and RF output power as a function of IF input power (right and upper axis).

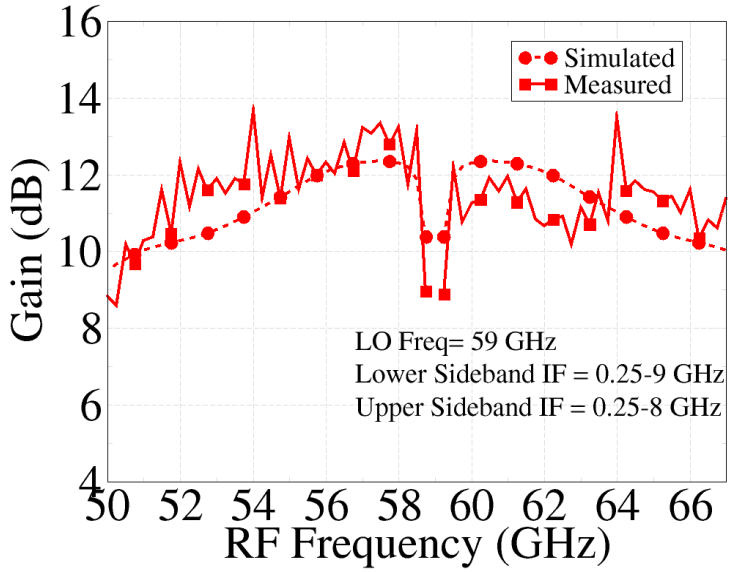


Figure 2.56 Measured and Simulated Gain as a function of RF frequency with constant LO frequency.

shows the measured OP1dB for different bias current. The realized mixer has the smallest chip area when compared to other state-of-the art circuits, as can be seen in Table 2.7. It also exhibits the best linearity except [64][65] but they require much larger chip area then this mixer. The measured IF frequency bandwidth is shown in Fig. 2.56. The IF bandwidth depends on the RF bandwidth and has a 3-dB bandwidth of 0.5-8.5 GHz on both sidebands with 59 GHz LO that

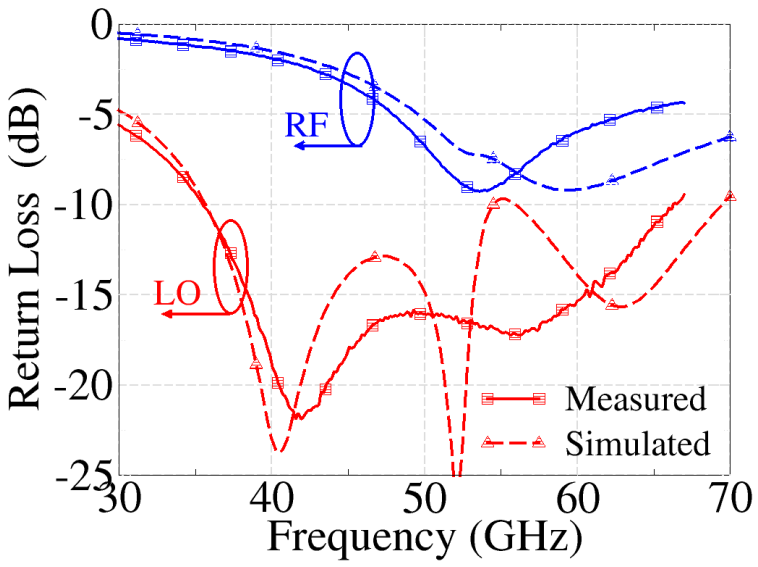


Figure 2.57 Measured and Simulated Returns loss of LO and RF ports.

corresponds to 50-67 GHz RF frequency. Figure 2.57 displays the measured return loss for the RF and LO ports. The LO port and RF port return loss are less than -10 dB and -5 dB from 50-67 GHz.

2.7 Frequency Tripler

Local Oscillators (LO) sources are one of the most vital components in RF receivers. For low-frequency circuits, synthesizers with good performance are readily available. However, for W-band transceivers, LO synthesis in not trivial. Having an on-chip high-frequency signal generation circuit is intrinsic to most mm-wave transceivers. It is very challenging to design mm-wave voltage-controlled oscillators (VCO) due to parasitic effects and passive loss. VCOs may also suffer from unwanted effects, such as injection pulling due to the high output power of the nearby power amplifier (PA) [31]. A rather simpler approach is to cascade a lower frequency VCO with a frequency multiplier. Frequency doublers are in general easier to implement than triplers, because of natural self-mixing topologies creating higher second harmonic components [66]. However, the second harmonic power generated from the PA nonlinearity can still be sufficient to detune the LO frequency.

Table 2.7 Performance Comparison of V-band Upconverting Mixer with the State-of-the-art

	Freq. (GHz)	Frac. BW (%)	Technology	CG (dB)	OP1dB (dBm)	Power (mW)	Chip size (mm2)	LO input (dBm)	Topology
This work	**50-67 (meas.) 54-85 (sim.)**	**29 (meas.) 45 (sim.)**	**130 nm SiGe**	**13.4 * @57 GHz 11.38 @60 GHz**	**-1.4**	**52 66 $**	**0.146 (with pads) (0.365x0.4) 0.052 (0.175x0.3)**	**3 @ 59GHz**	**Gilbert Cell with on-chip transformer baluns**
IMS'14 [64]	71-86	19	130 nm SiGe	1.5	1	80	1.8	3	Multi-tanh
MWCL'17 [65]	57-66	14	130 nm SiGe	-2.5	-2.1+	27	0.22	0	Mixing stage only
RFIC'06 [67]	35-65	60	180 nm SiGe	-7 $\pm$ 1.5	-25 @40GHz	14	0.27	5	Gilbert Cell Mixer
RFIT'07 [68]	60	-	250 nm SiGe	-6.5	-6	82.5	1.21	0	Micromixer
RFIC'08 [69]	58-62	7	65 nm CMOS	-7.5	-6.5	29	0.98	5	Gilbert cell with current steering
MOTL'16 [70]	53-65	20	90 nm CMOS	0.78	-11	27.8	0.75	NR	Gilbert-Cell
E. Lett.'08 [71]	59-65	10	130 nm CMOS	2 $\pm$ 2	-5.6	24	0.15	0	Gilbert Cell
IMS'10 [57]	15-50	107	180nm CMOS	-14.5 $\pm$ 1.5	-11.5- -7.5 (-10)	0	0.2	10	Resistive Ring Mixer
MTT'12 [38]	40-108	92	90nm LP CMOS	0 $\pm$ 2	-12 @60GHz	9.6	0.23	0	Weak inversion ring mixer with IF buffer
MOTL'12 [63]	30-65	74	150 nm pHEMT	2.22 $\pm$ 1.5	-2.4 @40GHz	105	1.68	2	Gilbert Cell

*maximum $including bias circuit +calculated from OIP3=OP1dB+9.6 dBm

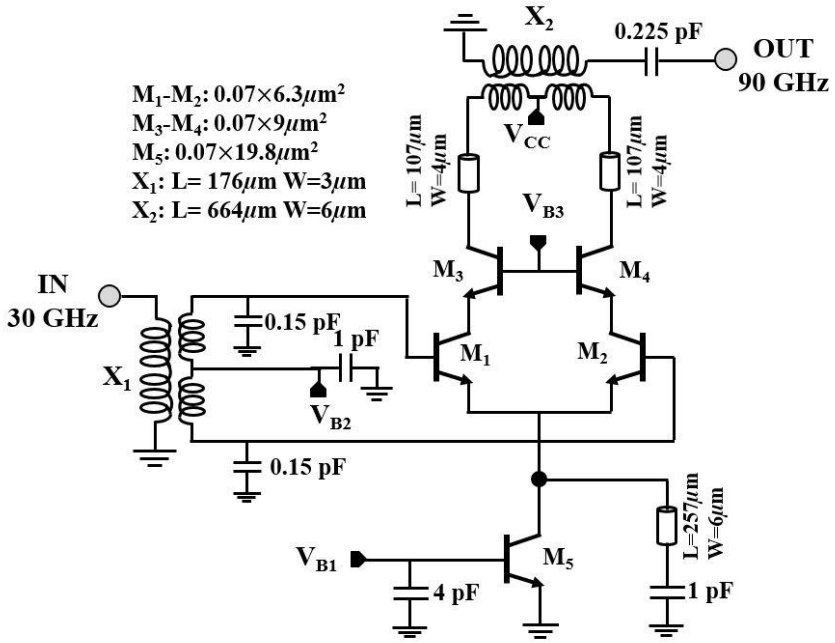


Figure 2.58 Circuit diagram of the W-band Tripler.

For certain frequency plans, however, frequency triplers are desired, and as part of this dissertation, a W-band harmonic-based frequency tripler (HBFT) is implemented using a 0.13-µm SiGe BiCMOS process. The multiplier core is biased at Class A and overdriven that generates significant third harmonic content [72]. The output power is improved by enhancing the second harmonic component at the common node of the differential pair to promote its mixing with the input frequency. The tripler exhibits better performance while occupying only half of the chip area than most of the state-of-the art circuits in similar technologies.

2.7.1 Circuit Description

The HBFT tripler is designed using a single-balanced cascode differential pair as shown in Figure 2.58. The input and output of the tripler uses on-chip transformer baluns to convert unbalanced to balanced signals and vice versa. The design procedure of the transformer baluns is not trivial and requires careful consideration and trade-offs regarding transformer size, choosing an appropriate coupling factor, amplitude and phase imbalance, quality factor and impedance

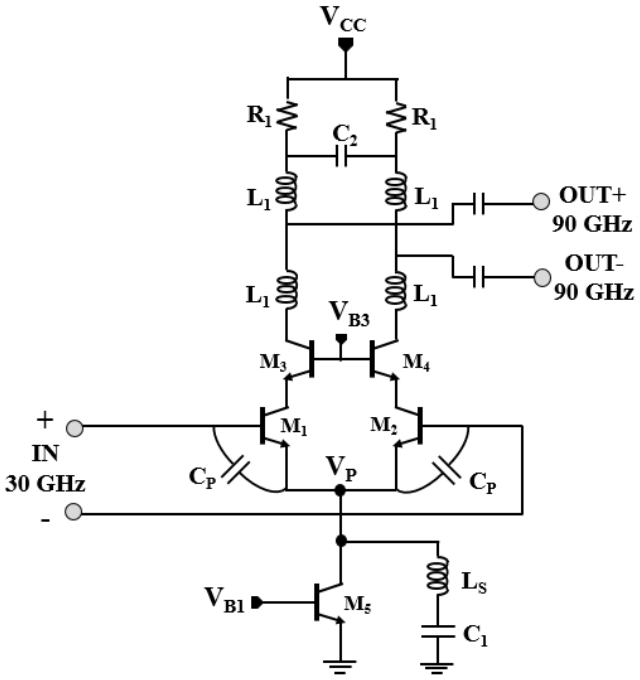


Figure 2.59 Circuit schematic of the proposed tripler with differential input and output.

matching. A study on these details can be found in [73]. The single-ended input signal at 30 GHz is converted to differential one using the balun and fed to the differential core that amplifies the signal and the harmonic terms. At the output of the tripler, the signal is converted from differential to single-ended using the W-band transformer balun to enable stand-alone measurement. The baluns are realized using the two topmost thick metal layers (TM2 and TM1) with linewidth of 6 µm and 3 µm for the input and output balun.

The size and bias of the transistor M5 is chosen such that the differential pair (M1-M2) is biased at Class A. When the tripler is overdriven in Class A, it results in significant odd order harmonic generation along with higher fundamental gain [72]. The input transistors M1-M2 are followed by M3-M4 as common-base amplifiers to amplify the third harmonic.

The third harmonic content at the output is further improved by facilitating the self-mixing of the input signal with its own generated second harmonic at the common node. Figure 2.59 shows

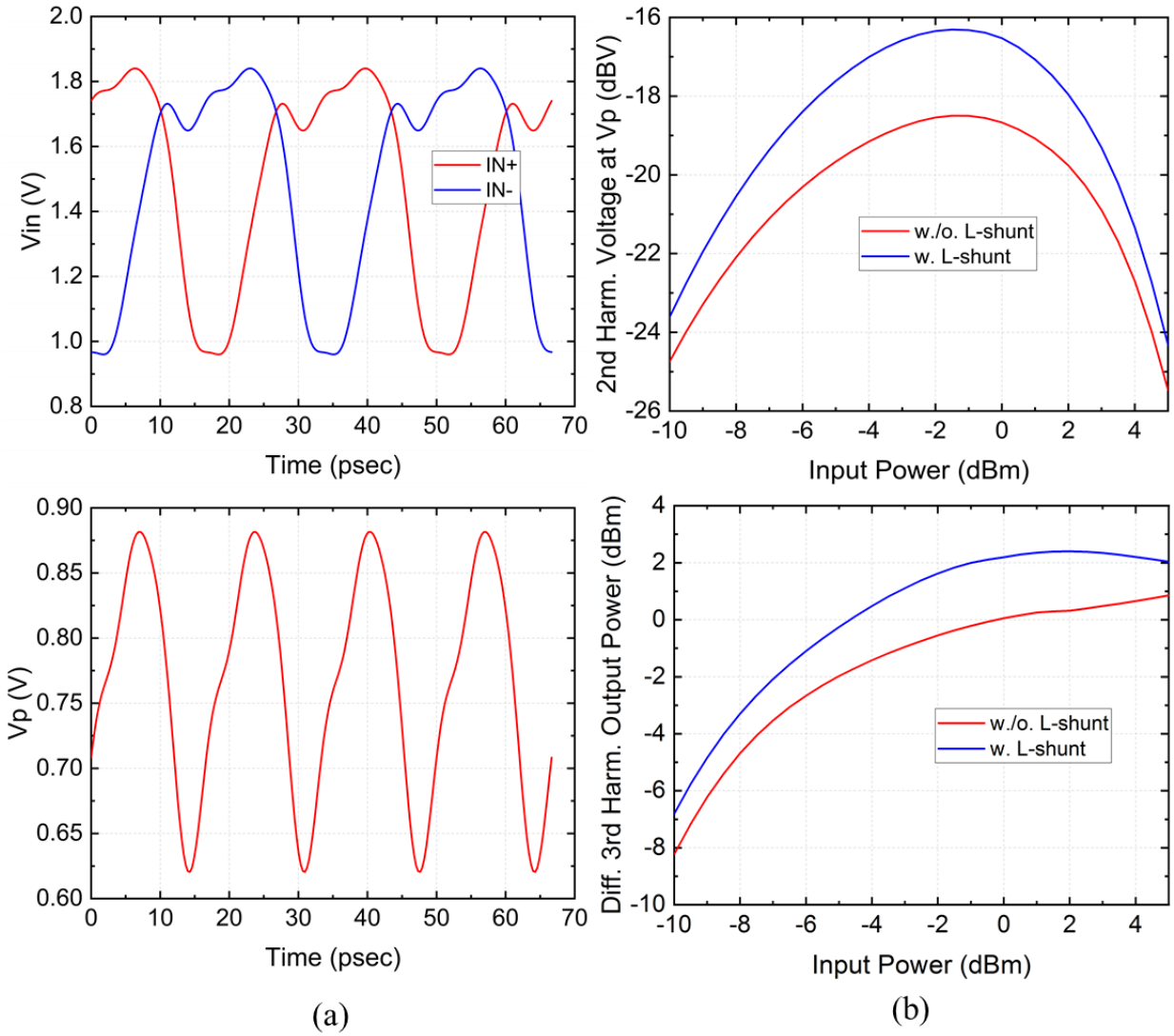


Figure 2.60 (a) Simulated voltage swing at input nodes and common-node Vp and (b) Simulated 2nd harmonic voltage at Vp and differential 3rd harmonic output power.

the circuit schematic of the proposed tripler with the base-emitter parasitic capacitance (Cp) and differential input and output. When the differential pair is overdriven, the large amplitudes at the input gives rise to the nonlinearity of Cp, which in turn produces a signal at Vp with half the time period of input as shown in Figure 2.60(a) [31]. This component at Vp, with double the frequency of the input ($2f_o$), mixes with the input frequency (f_o) and contribute to the overall third harmonic at the output ($3f_o$). $2f_o$ at Vp can be enhanced by inserting a shunt inductance to resonate parallelly with M5 at $2f_o$ and increase the overall impedance seen at the second harmonic. Figure 2.60(b)

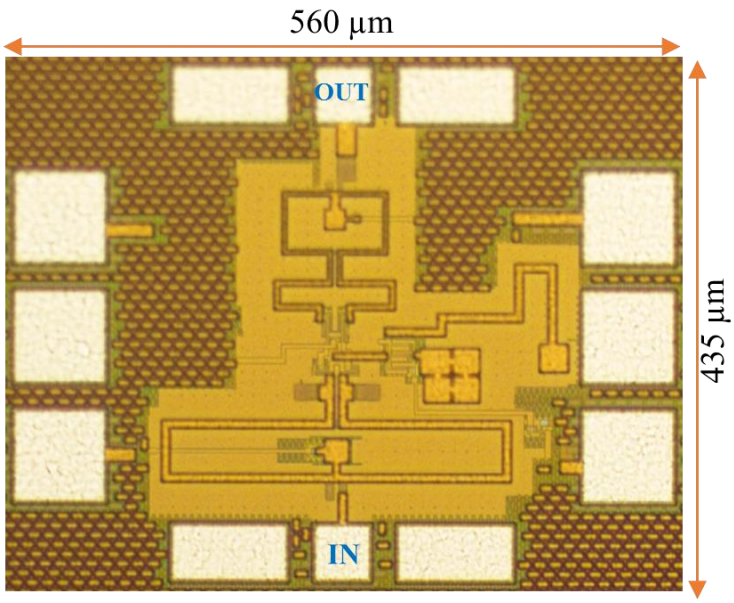


Figure 2.61 Chip micrograph of the realized W-band Frequency Tripler.

shows the increase in second harmonic at Vp and differential third harmonic output as a function of input power with and without L-shunt. Based on simulation, having a high impedance at the second harmonic improves the output power by 2 dB.

The chip micrograph of the W-band tripler is depicted in Figure 2.61. It was implemented using the 0.13-μm IHP Microelectronics SG13G2 BiCMOS process [74] with 300 GHz- f_T /500 GHz- f_{MAX} occupying a total area of 0.24 mm^2. The transistor sizes of M1-M2 is 0.07×6.3µm^2, M3-M4 is 0.07×9µm^2 and M5 is 0.07×19.8µm^2. The tripler uses a 3.3V power supply and consumes 88 mW DC power.

2.7.2 Measurement Results

The desired output power at the third harmonic and the unwanted fundamental, second and fourth harmonic was measured using the PSG E8257D Signal Generator and the EXA Signal Analyzer paired with smart W-band harmonic mixer as shown in the block diagram in Figure 2.62. The input frequency was swept from 25-32 GHz with 0 dBm and 3 dBm input power. Figure 2.63

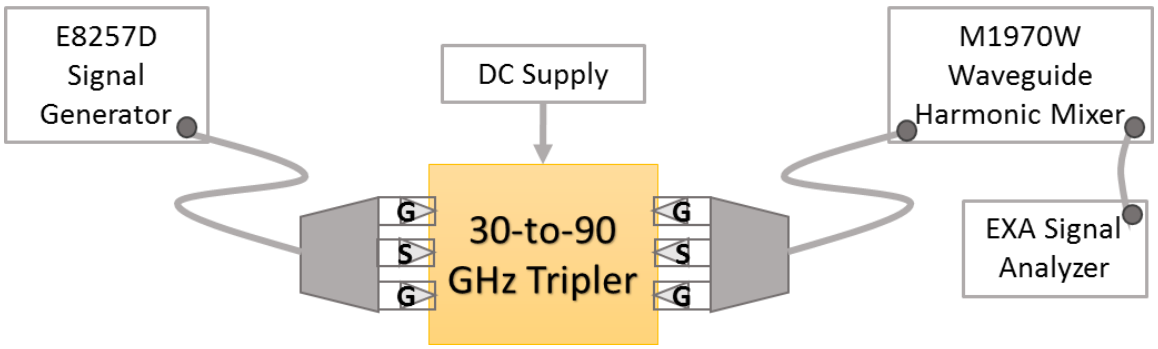


Figure 2.62 Measurement Setup for the W-band Tripler.

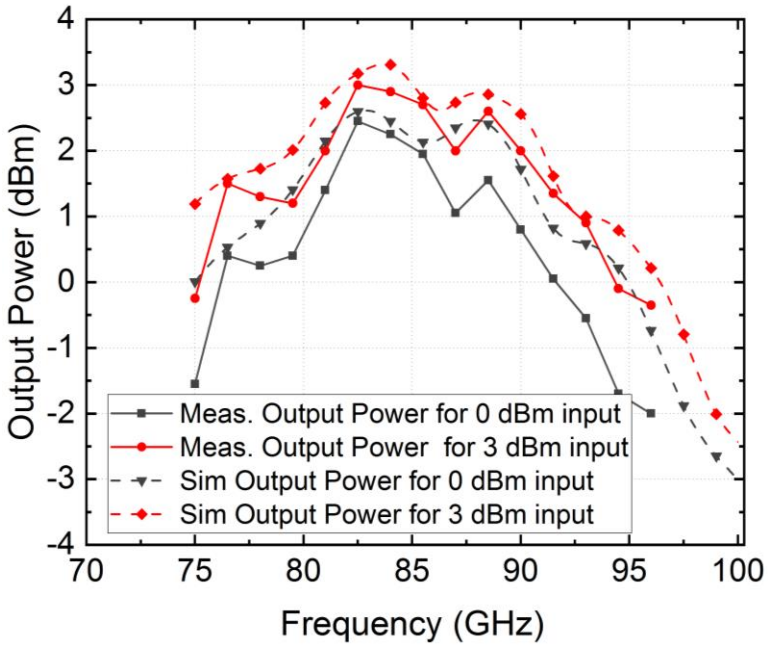


Figure 2.63 Simulated and Measured output power as a function of output frequency.

shows the simulated and measured third harmonic output from 75-96 GHz. The tripler generates a maximum of 2.45 dBm and 2.9 dBm output power at 82.5 GHz and 84 GHz with input powers of 0 and 3 dBm respectively. The 3-dB fractional bandwidth is 24.56% from 75-96 GHz with 3 dBm input and 20.12% from 76-93 GHz with 0 dBm input. Figure 2.64 and 2.65 shows the harmonic rejection for the first, second and in-band fourth harmonic. The in-band fourth harmonic was only measured up to 112 GHz due to equipment limitations and it is found be greater than 25 dBc and 20 dBc for 0 dBm and 3 dBm input. The second harmonic rejection is better than 25 dBc for both

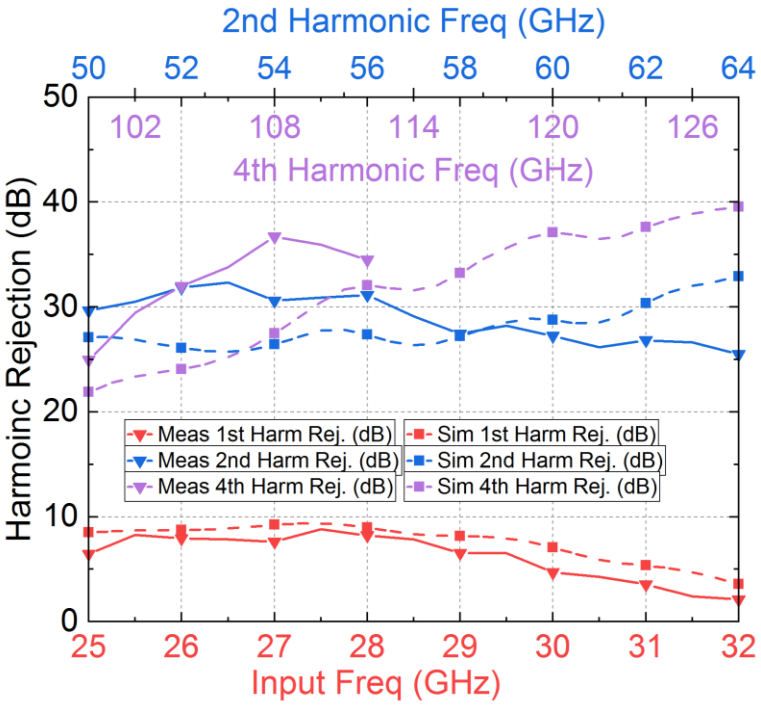


Figure 2.64 Measured and Simulated 1st, 2nd and 4th harmonic rejection at 0 dBm input power.

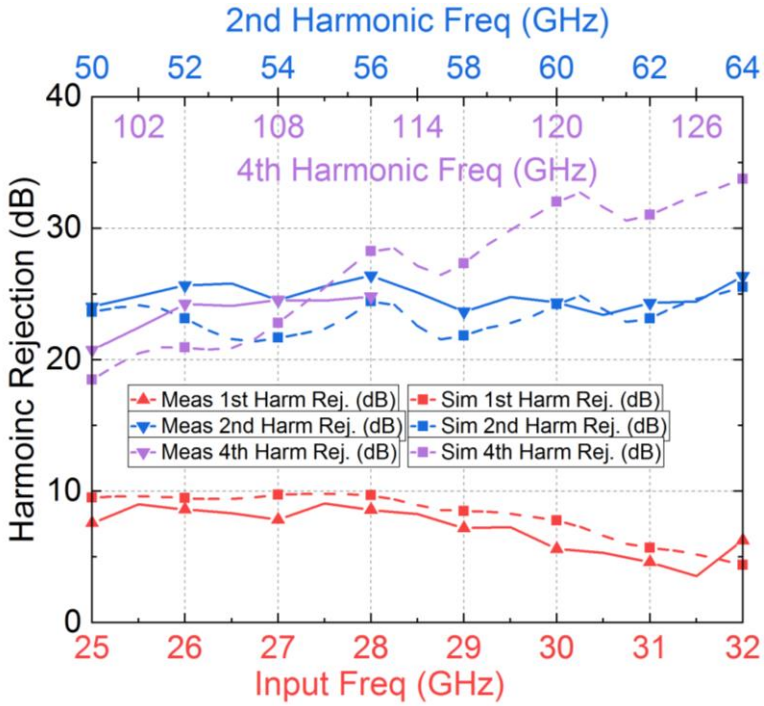


Figure 2.65 Measured and Simulated 1st, 2nd and 4th harmonic rejection at 0 dBm input power.

input powers. However, the fundamental rejection is poor and goes as low as 5 dBc but it is acceptable as it is very far from the desired frequency band and it is most likely to be further

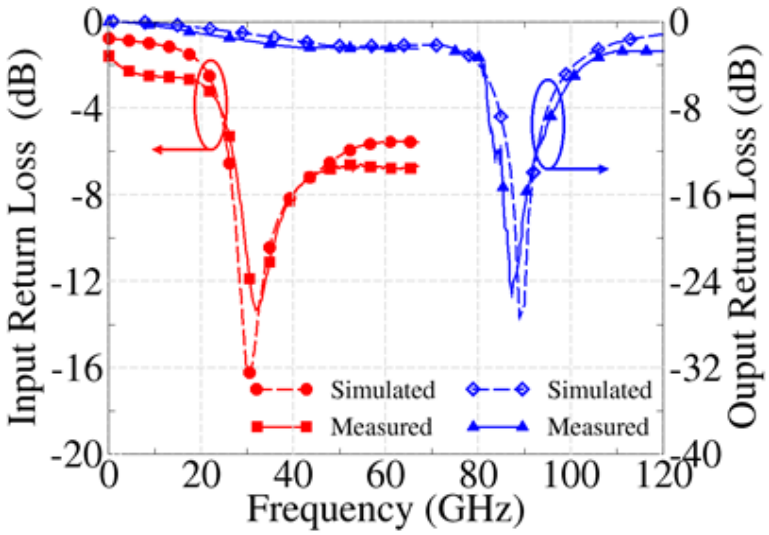


Figure 2.66 Input and Output return loss of the W-band Tripler.

suppressed by other W-band components to follow. The small-signal S-parameters were measured and displayed in Figure 2.66. The input and output return loss are less than -10 dB from 25-32 GHz and 82-95 GHz. The realized tripler is compared with other state-of-the-art triplers and multipliers in Table 2.8. A new figure-of-merit (FOM) is derived from [75] for mm-wave multipliers that also takes chip area into account. Based on the FOM and all the performance metrics, the realized tripler out-performs the other W-band triplers in similar technologies while occupying only half of the chip area.

2.8 Conclusion

In this chapter, we discussed the millimeter-wave ICs that are implemented using the state-of the-art 0.13-µm IHP Microelectronics SiGe BiCMOS process. The performances of these individual transceiver blocks are comparable to the state-of-the-art and can be integrated together to realize a high performing millimeter-wave module.

Table 2.8 Performance Comparison of W-band Frequency Tripler with the State-of-the-art

Reference	**Tech-nology**	**Type**	**Fout (GHz)**	**3 dB BW (%)**	**Pin (dBm)**	**Pout (dBm)**	**Drain Effic-iency (%)**	**F.R. (dBc)**	**2nd H.R. (dBc)**	**3rd/4th H.R. (dBc)**	**FOM**	**Pdc (mW)**	**Area (mm^2)**
This work	**0.13µm SiGe**	**×3**	**76-93/ 75-96**	**20.12/ 24.56**	**0/ 3**	**2.45/ 2.9**	**2/ 2.21**	**>3/ >5**	**>25/ >25**	**>25/ >20**	**23.44 /23.9**	**88**	**0.24**
IMS'18 [76]	0.13µm SiGe	×3	65-90	22.1	2/ 2*	-2/ 9.9#	0.6/ 6.14#	>35	>35	-	13.65	105/ 158	0.53
MWCL'14 [77]	0.13µm SiGe	×3	56-72	25	18	-2	0.18	>20	-	-	0.82	362	0.52
IMS'15 [78]	0.13µm SiGe	×3	46-54/ 48-58*	16/ 19*	0/ 0*	-4.4/ 9.5*	0.59/ 4.05*	38/ 28*	31/ 36*	34/ 35* (4^{th})	24.1	62/ 220*	0.19/ 0.94*
MTT'12 [79]	0.18µm SiGe	×3 HBFT	90-101	10.9	0	-10.5	0.13	>20	>20	-	0.61	75	1.9
MTT'12 [79]	0.18µm SiGe	×3 ILFT	92-99	5.55	0	-7	0.27	>20	>20	-	0.44	75	1.8
HSIC'12 [80]	90nm CMOS	×3	49.5-60	19	4	-5	5.85	>31	>37	-	17.77	5.4	0.46
EuMIC'15 [81]	0.13µm SiGe	×4	56-80	35	-6	13	5.7	>70	>40	>60 (3^{rd}) >45 (5^{th})	8.72	350	2.71
SiRF'14 [82]	0.13µm SiGe	×4	50-75	40	-10	0	1.09	>28	>20	>28 (3^{rd})	37.81	92	0.3
EuMIC'15 [81]	0.13µm SiGe	×8	56-71	23	0	13.5	5.46	-	>70	>60 (6^{th}) >45 (10^{th})	5.72	410	2.71

Table 2.8 (cont'd)

Reference	Tech-nology	Type	Fout (GHz)	3 dB BW (%)	Pin (dBm)	Pout (dBm)	Drain Effi-ciency (%)	F.R. (dBc)	2nd H.R. (dBc)	3rd/4th H.R. (dBc)	FOM	Pdc (mW)	Area (mm^2)
MTT'13 [83]	65nm CMOS	×9	88-99.5	12.2	14.2	8.5	1.62	>45	>50	>35 (7^{th}/8^{th}/10^{th})	9.99	438	0.45
MWCL'10 [84]	130nm CMOS	×2	94-108	13.86	-7.7	-8.7	-	-	-	-	-	-	0.2 (w/o pad)
EuMIC'11 [85]	65nm CMOS	×2	75-110	37.84	5	-11	0.6	>20	-	-	22.58	13.8	0.28
MWCL'19 [86]	0.15µm GaAS pHEMT	×2	88-99.5	13.27	10	7.1	4.7	>17	-	-	1.55	110	2
MWCL'14 [87]	0.1µm GaAS pHEMT	×2	85-110	25.64	5	8.2	11.2	>30			7.69	56	1.35

FR-Fundamental Rejection; HR- Harmonic Rejection; HBFT- Harmonic-based frequency tripler; ILFT- Injection-locked frequency tripler

*, #-With tripler amplifier, $FOM = \left[10\log\left(\frac{100\times P_{out}}{P_{in}+P_{dc}}\right) + HR\right] \times \frac{BW}{Area}$, where HR corresponds to harmonic rejection near the output frequency

CHAPTER 3

ADDITIVE MANUFACTURING FOR MILLIMETER-WAVE PACKAGING

3.1 Introduction

This chapter focuses on the implementation of millimeter-wave packaging using 3D printing technology. Recently, 3D printing has drawn a lot of attention from researchers as it enables faster prototyping and cheaper large-scale production. As part of this dissertation, we would like to propose aerosol jet printing as an alternative packaging technique.

In the first part of this chapter, the merit of the aerosol jet printing (AJP) for millimeter-wave interconnect is evaluated. A dummy chip was connected to the packaging substrate using transmission lines operating from DC-110 GHz. Later, attempts were made to demonstrate an aerosol-jet (AJ) printed interconnect to connect between two of the previously designed chips. However, the bare dies from the IHP process had aluminum pads which readily oxidizes and forms a thin-film of aluminum oxide, hence hindering an electrical path. Therefore, commercial-off-the-shelf (COTS) dies with gold pads were used to demosntrate AJ printed interconnect between two bare dies.

3.2 Aerosol Jet Printing

The two most popular practices for interconnecting ICs and other components to the packaging substrate in System-on Package (SoP) solutions are wire-bonding and flip-chip bonding as shown in Figure 3.1. However, in wire-bonding technique, the discontinuity due to bond wires influence the overall mm-wave performance. Also, the series reactance of the bond wire changes significantly with increasing frequency, hence constraining the system to a narrow-band [88]. On the other hand, flip-chip interconnects suffer from detuning, the affect arising due to the presence

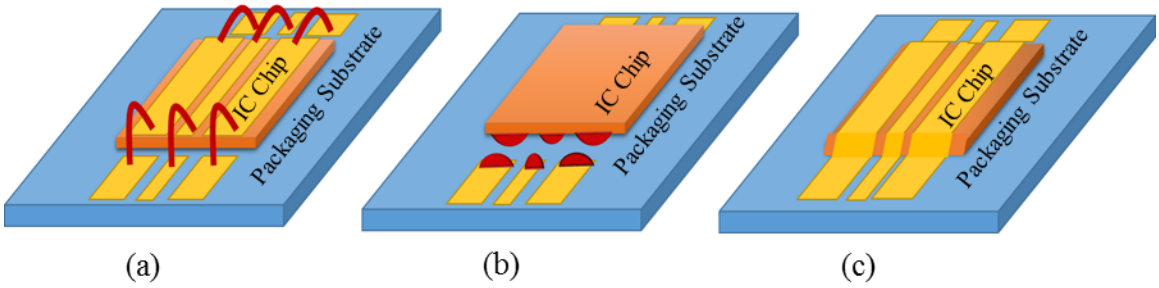


Figure 3.1 Different types of interconnects- (a) Wire-bonding; (b) Flip-chip bonding; and (c) AJP 3D interconnects.

of metal underneath the flipped chip [89], and co-efficient of thermal expansion (CTE) mismatch between the chip and package substrate [90].

Recently an alternative cost-efficient process called additive manufacturing (or 3D printing) has emerged that overcomes the aforementioned challenges. Inkjet printing has been demonstrated for interconnects up to 40 GHz [16], [91]. Pushing this technology to higher frequency gets increasingly challenging due to its limited resolution. Also, inkjet printing becomes lossy at higher frequencies. The work in [16] has a resolution of 20 µm which is the highest demonstrated to the authors' knowledge. Another novel additive manufacturing (AM) technology using aerosol jet printing (AJP) has been shown to provide a resolution as small as 10 µm, which is comparable to standard photolithographic processes [92].

3.3 Ultra Wideband Interconnect using Dummy Chip

This work presents a wideband interconnect technology using AJP (Figure 3.1(c)). The technique used in this demonstration is known as the 'chip-first' approach, where the dies are first placed on the substrate and the package is built around them rather than starting with a cavity. In this part of the project, a trapezoidal structure as a dummy chip was 3D printed using "Vero White" dielectric material on LCP, which here serves as the packaging and carrier substrate, and CPW

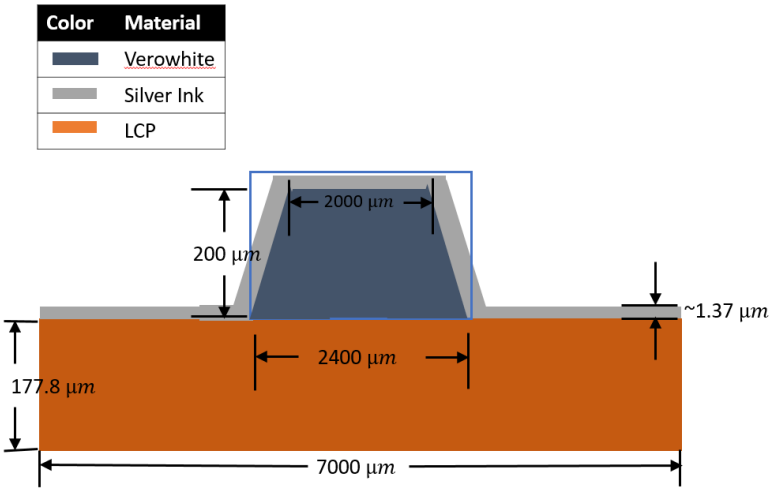


Figure 3.2 Cross-sectional view of the System-on-Package to demonstrate AJP interconnects.

lines were printed on them. The SoP was measured from 0.1 to 110 GHz. Loss was found to be 0.38 dB/mm for LCP only, and 0.49 dB/mm for the entire structure including the trapezoidal transition. Previously, [17] has demonstrated the AJP interconnects up to 40 GHz. This paper extends the frequency bandwidth to 110 GHz which is almost 2.5 times the previous work.

3.3.1 Fabrication Process of the Interconnect

3.3.1.1 System of Package

Figure 3.2 shows the cross-sectional view of the structure. A trapezoidal structure was 3D printed using the Objet Connex350 3D printer on LCP to imitate IC to board interconnection, and for the accurate characterization of such envisioned interconnection. Ultralam 3850HT Roger's LCP board with 7 mil (175 µm) thickness was used as the package substrate. The board came with a copper cladding of 9 µm on each side. Bare LCP was acquired by etching off the copper from it.

3.3.1.2 CPW Lines with AJP

The CPW lines were printed using the Optomec Aerosol Jet 5X printer, shown in Figure 3.3, available at the MSU facility. To obtain a quantitative insight, identical CPW lines were printed on LCP and Vero White substrates, separately. The printer has three axes of linear motion,

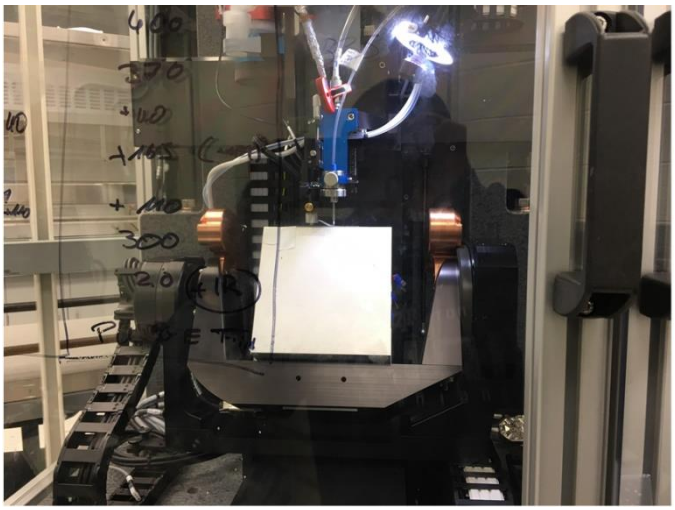
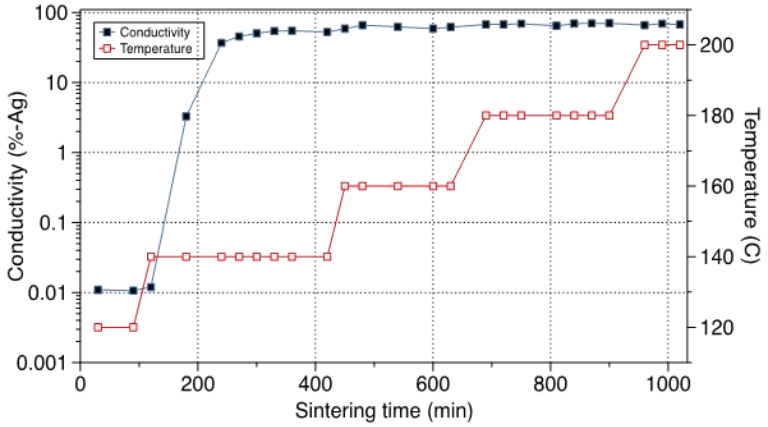


Figure 3.3 The Optomec Aerosol Jet 5X Printer in Michigan State University (MSU).

two axes of rotation and can print with 10 μm resolution. A silver nanoparticle ink, product name EXPT Prelect TPS 50 was acquired from Clariant, diluted at the ratio one-part ink to three-part water, and then used for printing. A dense aerosol is created from a liquid silver nanoparticle ink by atomization and aerodynamically focused into a collimated ink to print the lines [93]. Three layers of silver ink was deposited which gave a thickness of 1.37 μm.

The sintering procedure for the ink was studied [94]. A 10 mm×10 mm Ag layer was printed on a glass slide. The square was sintered on a hot plate at different temperatures for various time durations. The percentage values were measured relative to the conductivity of bulk Ag (~6.3×10^7 S/m) and plotted in Figure 3.4. It was found that a specific conductivity can be obtained either by sintering for a long time at a lower temperature or in a short time at a higher temperature. However, most of the substrates might not be suitable for such temperature. Therefore, for our case the ink was then sintered at 200 ˚C for one hour in a well-regulated oven. As a result, forty percent of the conductivity of bulk silver was obtained.



(a)

(b)

Figure 3.4 (a) Electrical conductivity of printed Ag as a function of temperature and sintering time; and (b) the characterization plot was obtained by sintering using the hot plate.

3.3.2 Design of the test structure

The trapezoidal structure has top width of 2 mm, bottom width of 2.4 mm and a height of 200 µm. A rigid photopolymer material, Vero White was used to print the object because it has a low dielectric constant similar to LCP [95]. The overall length of the printed transmission line was 7 mm. CPWs are one the most useful and easily realizable transmission lines. One big advantage of CPW is that it has the signal line and the ground line on the same side of the substrate, making it easy to characterize using conventional measurement systems. CPW with no ground plane at the bottom was selected for ease of fabrication. Since LCP has a low dielectric constant, the 50 Ω

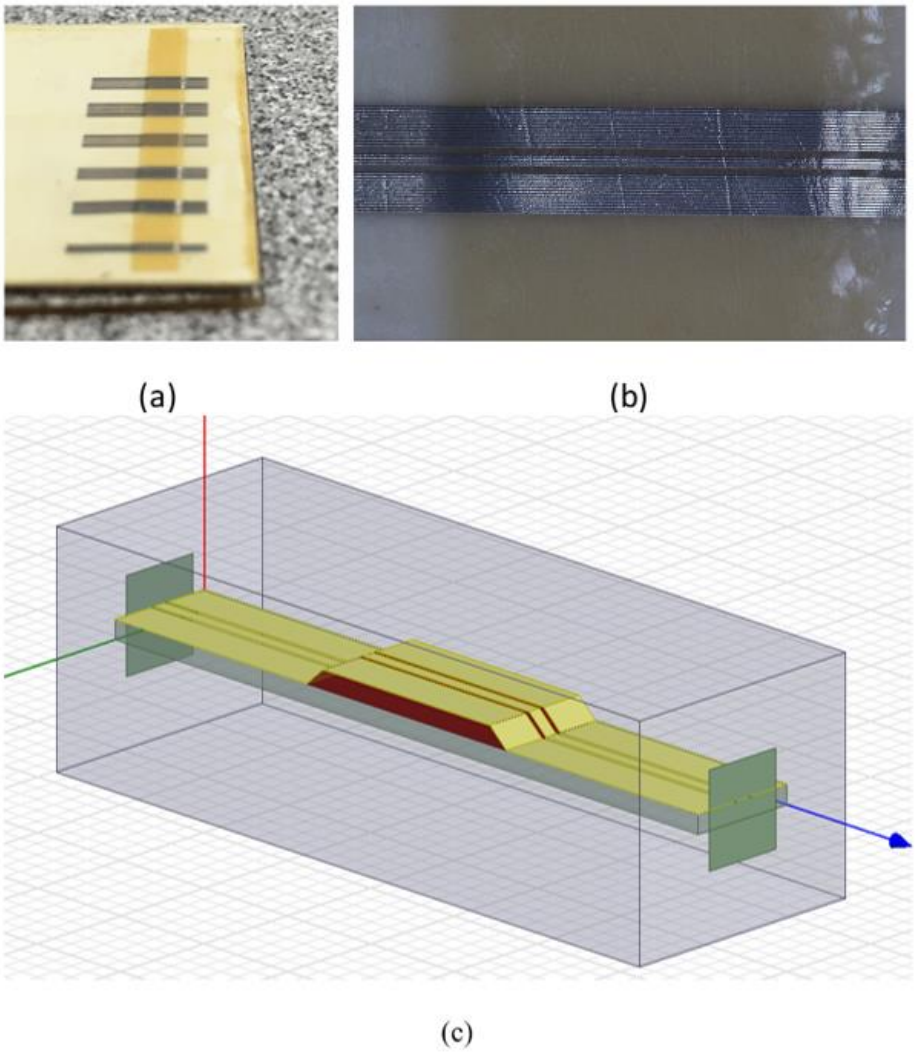
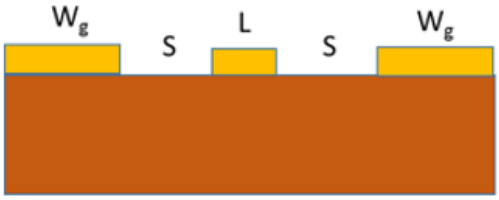


Figure 3.5 (a) Image of the System-on-Package, (b) 85 Ω CPW lines with 50 µm gapwidth and (c) the 3D model used in the HFSS simulation.



Impedance (Ω)	80
Line width L (µm)	121
Gapwidth S (µm)	50
Ground width (µm)	424

Figure 3.6 The dimensions of the designed CPW.

CPW lines dimensions with a gapwidth of 10 µm (smallest resolution realizable with Optomec Aerosol Jet 5X) are too large to measure using the available 110 GHz probes. Keeping this limitation in mind, different CPWs were designed for varying impedances, gaps and substrate

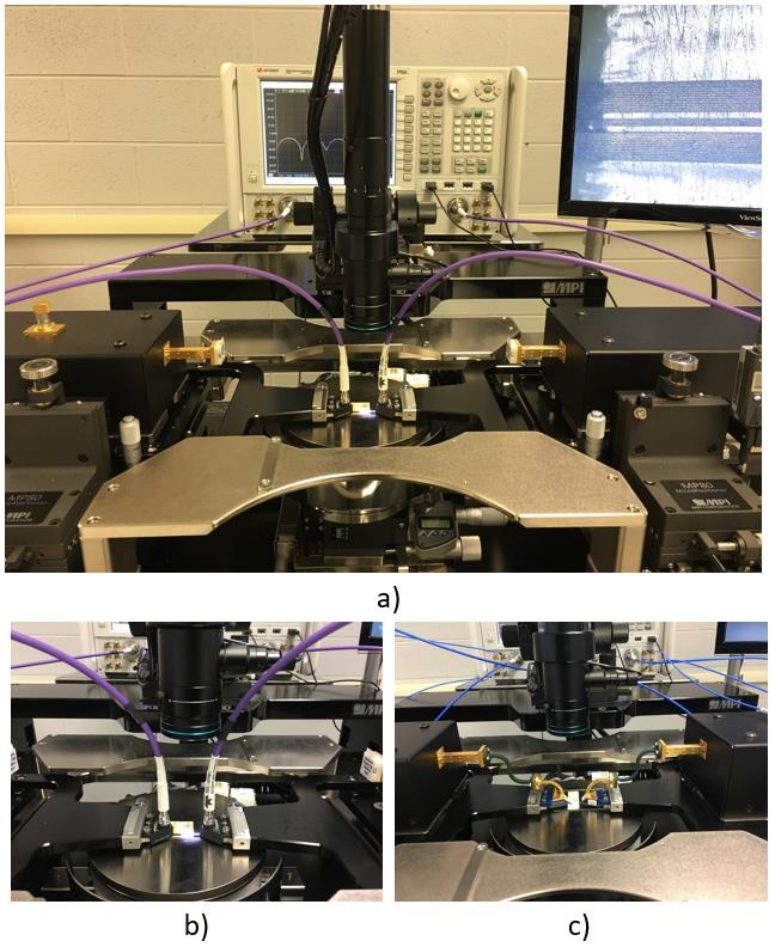


Figure 3.7 Image of (a) the complete measurement setup; (b) 250 µm probe pitch GSG Picoprobes and (c) Cascade Microtech 150 µm probe pitch GSG 110-GHz probes.

thicknesses. CPW lines with 80 Ω characteristic impedance having 50 µm gap on top of 7 mil (175 µm) LCP yielded best result under these constrains. Full electromagnetic simulation of the SoP was performed using Ansoft HFSS. Figure 3.5 shows the image of SoP sample and Figure 3.6 shows the complete dimensions of the CPWs.

3.3.3 Measurement Results

The measurement set up for the SoP is shown in Figure 3.7. An Agilent N5227A PNA Network Analyzer (for 0.1-67 GHz) and VDI WR10-VNAX extension modules (for 75-110 GHz) were used to measure the S-parameters of the CPW SoP, LCP, and Vero White. Since the system

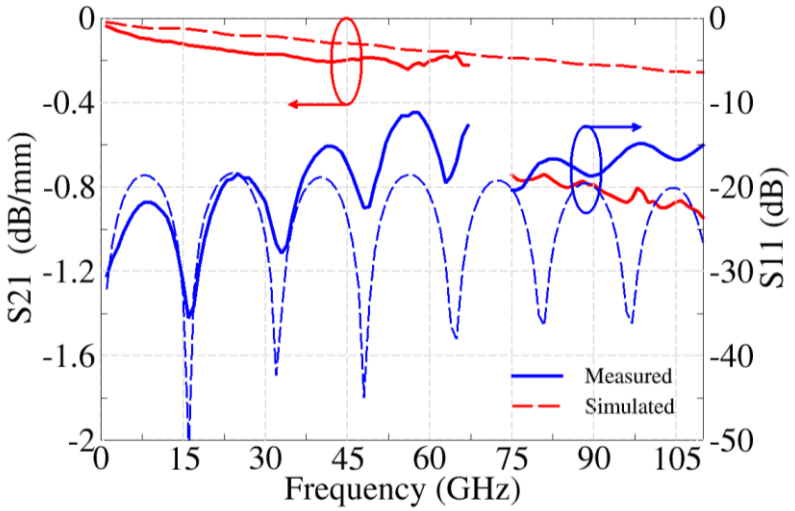


Figure 3.8 Simulated and measured S-parameters of the printed CPWs on Vero White substrate.

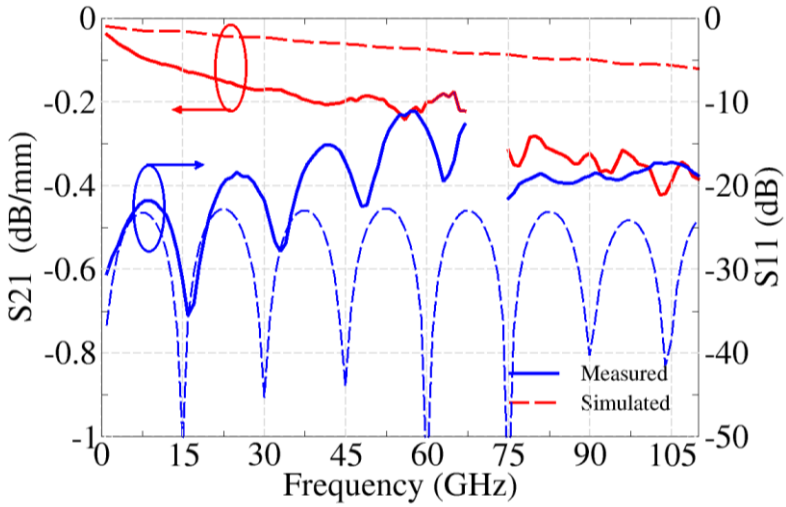


Figure 3.9 Simulated and measured S-parameters of the printed CPWs on LCP substrate.

was designed for a very wide band, two different sets of probes had to be used. 250 µm probe pitch GSG Picoprobes were used to measure from 0.1 to 67 GHz and Cascade Mircotech 150 µm probe pitch GSG 110-GHz probes for 75 to 110 GHz. Owing to the limitation of the equipment, there is a gap from 68-74 GHz in measurement results. Losses associated with the equipment were corrected by performing LRRM calibration for 0.1-67 GHz and SOLT calibration for 75-110 GHz.

The measured and simulated S-parameters for CPWs on LCP are depicted in Figure 3.8. CPW on LCP shows an insertion loss of 0.38 dB/mm at 110 GHz that is approximately three-fold

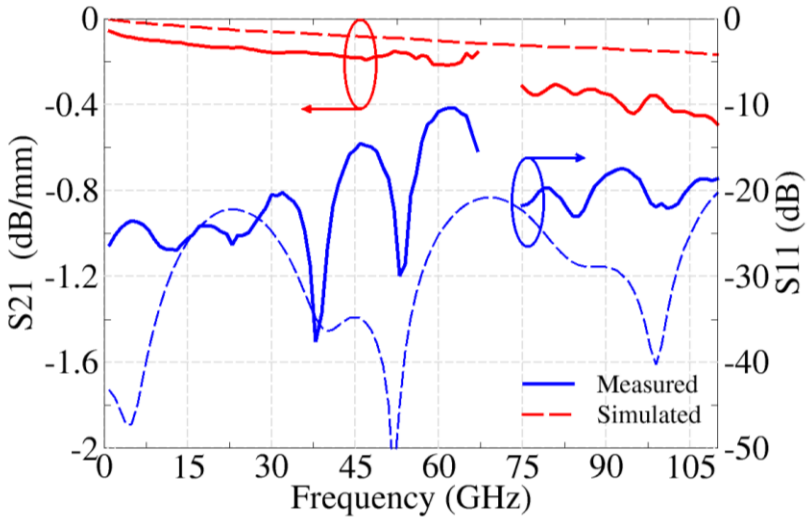


Figure 3.10 Simulated and measured S-parameters of the printed CPWs on the test System-on-Package that constitutes the interconnects and dummy IC.

better than the reported loss for inkjet printing lines [96] and comparable to copper CPWs fabricated using standard photolithography [97]. The best reported performance for inkjet printing is -3 dB/mm [96] and copper traced CPW is 0.088-0.25 dB/mm [97]. Figure 3.9 shows the results for CPWs on Vero White substrate. Since the dielectric constant of Vero White is slightly less than LCP (2.4-2.6) [95], the results are lossy due to slight variation of impedances. The simulated and measured insertion and return loss from 0.1-110 GHz for interconnects on SoP is given in Figure 3.10. The interconnects on SoP exhibit 0.49 dB/mm loss which was calculated from the insertion loss by dividing it with length of the CPW lines. The obtained result is comparable to simulation given the fact that the Vero White material is lossy at high frequencies. Also, very little is known and studied about the characteristics of Vero White material in the mm-wave regime. Considering that the trapezoid is a dummy chip and it will be replaced by low-loss IC chips in practical scenario, the result shows promise as an alternative method to conventional interconnects.

3.4 DC-to-Ka-band Broadband Chip-to-Chip Interconnects

In this work, we present the implementation of AJP to connect two ICs realized in GaAs technology using a chip-first approach to packaging. All the previous works using AM were concentrated on die-to-packaging substrate interconnects. To the author's best knowledge, this is the first demonstration of a die-to-die interconnect. The chips used for the demonstration are COTS 0-dB attenuators with conductor-backed coplanar waveguide pads with ground-signal-ground (GSG) interfaces on gold pads. The chips are connected to each other using aerosol-jet (AJ) printed coplanar waveguide (CPW) lines. The interconnect operates from DC-30 GHz with an insertion loss of 0.27 dB per interconnect at 30 GHz, which is similar to the die-board interconnect loss from the chip-first approach [98] and hence indicates the approach as a substrate-agnostic process. Traditional wire-bonding was done using identical chips and the results are compared with the AJ printed interconnect. The absence of the grounding connection at the bottom of the die, along with the substrate agnosticism of the chip-first approach, demonstrates the versatility and potential of the AJ printed interconnects.

3.4.1 Design and Fabrication

3.4.1.1 System-on-Package

Figure 3.11 conceptually illustrates the whole packaging process. The bare ICs are glued on a mechanically robust carrier substrate using high temperature double-sided Kapton tape. The ICs were placed closely with the smallest gap of approximately 50 µm where the chips were closest to each other and approximately 98 µm gap on the furthest side. The COTS 0-dB attenuators, KAT-0-DG+, were acquired from Mini-Circuits. These ICs were fabricated using highly repeatable processing with thin film resistors on GaAs substrates with a thickness of 100 µm and have a characteristic impedance of 50 Ω. The overall dimensions of the chips were 750 µm ×700

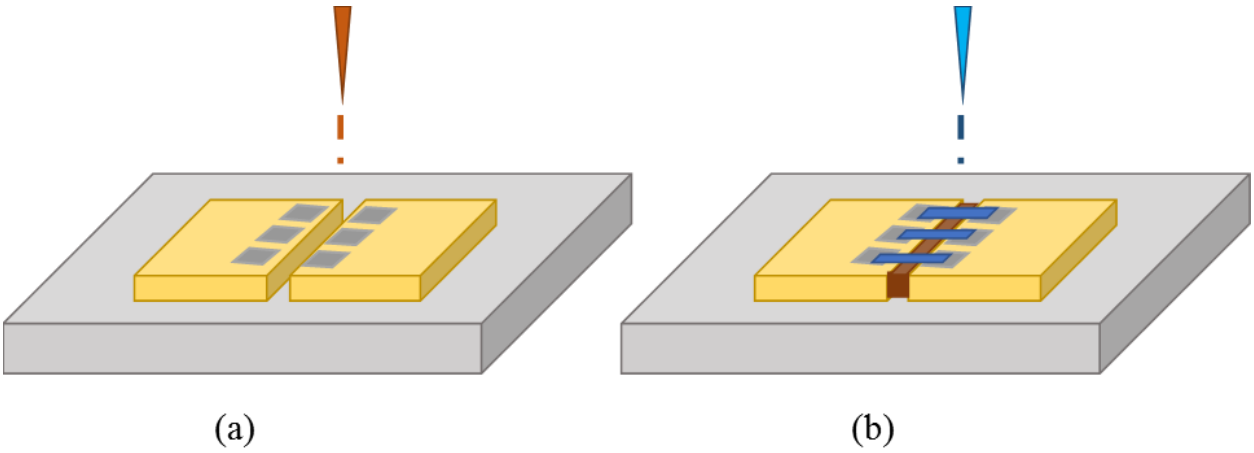


Figure 3.11 (a) Adhering the chips to the packaging substrate and printing polyimide in the gap and (b) printing CPW lines as interconnect using aerosol jet printed silver ink.

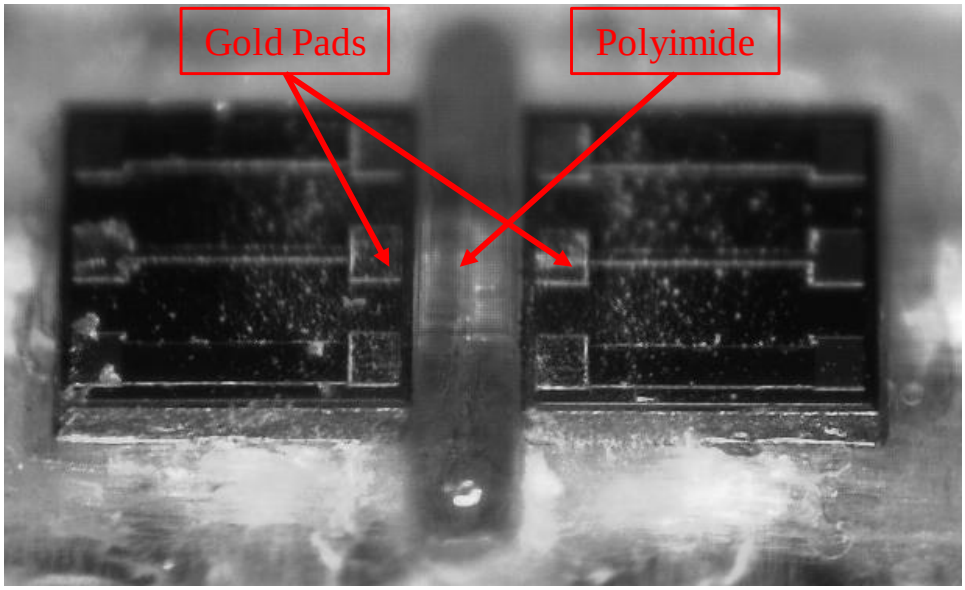


Figure 3.12 3D image of the SoP using the chip-first approach.

µm, the signal and ground pads were 125 µm × 100 µm and the gap between the signal and ground pad was 125 µm. Double-sided Kapton tape (polyimide tape) with a thickness of approximately 50 µm adhered to 1 mm thick glass was used as the carrier substrate. The ICs were mounted manually on top of the packaging substrate without any controlled process; hence they were not perfectly aligned. Figure 3.12 shows the 3-D image of a typical system-on-package (SoP) using

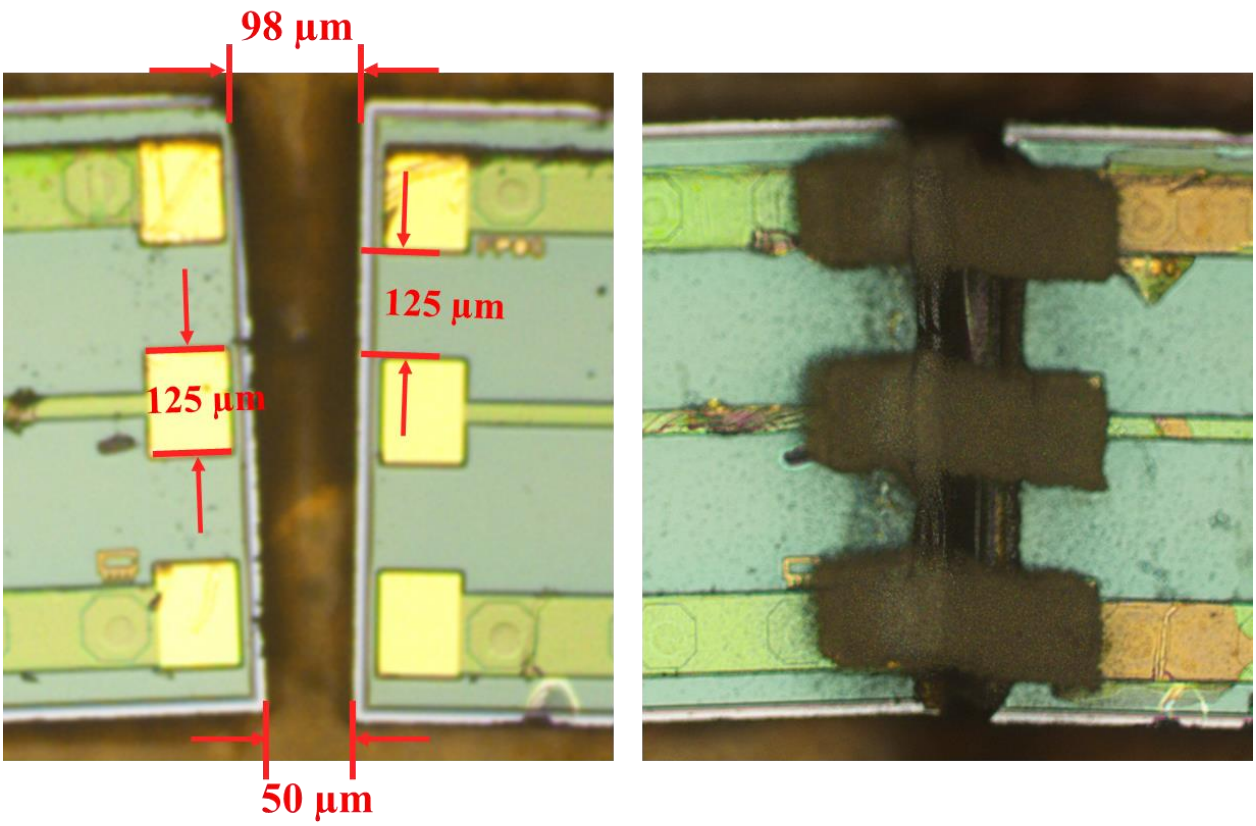


Figure 3.13 (a) The spacing between the two bare dies, and (b) Silver printed CPW interconnect lines between the dies.

the chip-first approach and Fig. 3.13(a) shows the spacing and dimensions of the pads of the test sample.

3.4.1.2 Aerosol Jet Printing (AJP)

The AM process for this work was done using the Optomec Aerosol Jet 5X printer. The printer has two axes of rotation, three axes of linear motion, and print on surfaces of almost any shape. The process is totally contactless, maskless and can achieve as fine as 10 µm resolution which is comparable to standard photolithographic resolution. Unlike photolithography, the printer disposes minimum waste and thus it is extremely low-cost and environmentally friendly.

The gap between the ICs was filled by printing polyimide as dielectric using the Optomec 5X. The polyimide precursor ink was acquired from Sigma-Aldrich and has a composition of 15% wt. polyamic acid in N-methyl-2-pyrrolidinone (NMP). To tone out the viscosity of the ink, it was further diluted such that the precursor ink was 5% wt. polyamic acid. The calculated viscosity was found to be 1 Pa-s. Since it is difficult to estimate the depth of the gap, initially we printed 15 layers of polyimide during the first run and did a profilometry scan to verify whether the gaps between the ICs were bridged or not. The ink was printed using the pneumatic atomizer and 200 µm nozzle with focusing sheath flow rate of 78 SCCM and aerosol flow rate of 50 SCCM. A total of 52 passes were printed to bridge the gap. The polyimide was cured in a nitrogen environment for 2 hours by ramping up the temperature from 20º C to 200º C and back to 20º C.

The interconnect was printed using the Clariant Type: TPS 50G2 silver ink. 1 ml of the ink was mixed with 2 ml of distilled water. The mix was printed using the ultrasonic atomizer of the Optomec 5X and initially the 100 µm nozzle with a focusing sheath flow rate of 30 SCCM and gas atomizer flow rate of 23 SCCM was used to print 3 layers of silver ink. However, due to overspray issues the nozzle was changed to 200 µm with 65 SCCM focusing sheath flow rate and 23 SCCM for the atomizer sheath flow rate which yielded a linewidth of 35 µm per pass. A total of 18 passes of silver ink was printed. The CPW lines were printed between the pads with a signal linewidth of 125 µm and a gap of 125 µm between the signal and ground lines as shown in Fig. 3.13(b). The silver was sintered at 120º C for 1 hour, then 140º C for 18 hours, followed by 160º C and 180º C for 2 hours at each temperature. The conductivity of the ink is reported to be 50% of bulk silver for similar curing profile (Figure 3.4(a)). The CPW lines were printed at a skew angle to overcome the misalignment that occurred while gluing the chips as shown in Figure 3.13(b).

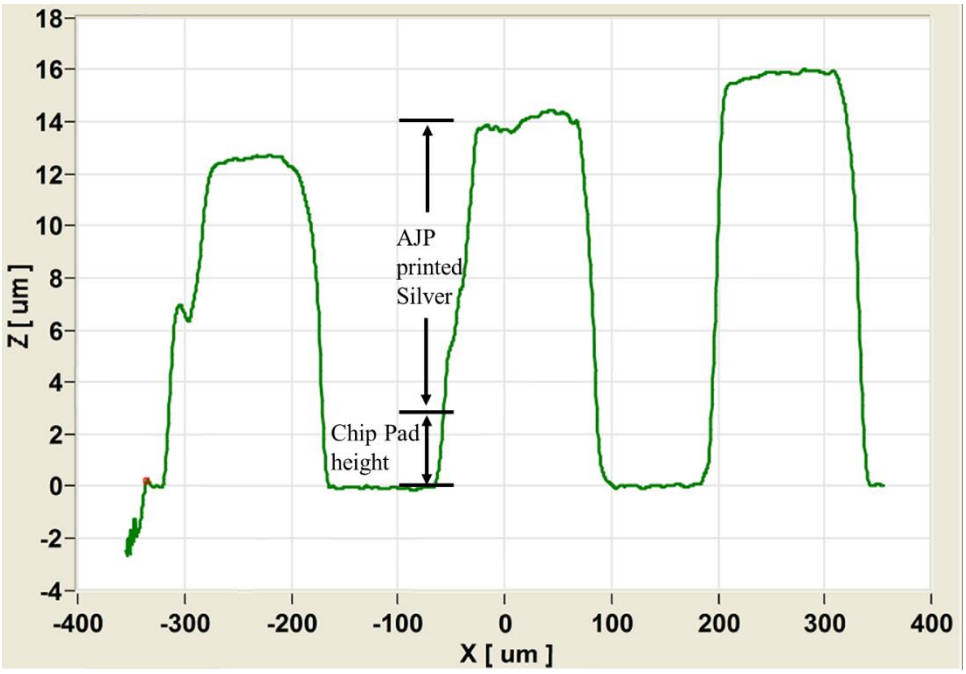


Figure 3.14 2D scan of the chip pads cross-section after silver is printed.

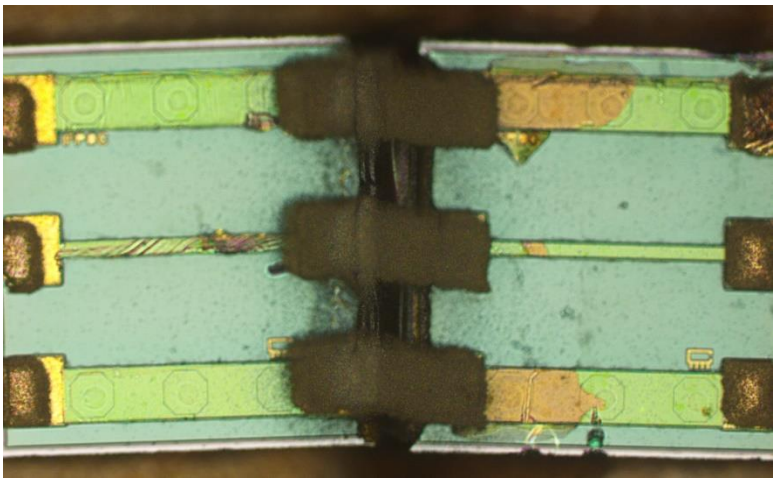


Figure 3.15 SoP with AJ printed CPW interconnect lines.

This also showcases the distinct feature of 3D printing that enables adjusting of the patterns within the fabrication cycle rather than starting over, which is the case for photolithography. The pads on the chips are scanned after silver post-printing using the NanoMap-500LS Surface Profilometer and is shown in Figure 3.14. The CPW lines connecting the pads are clearly visible and the height

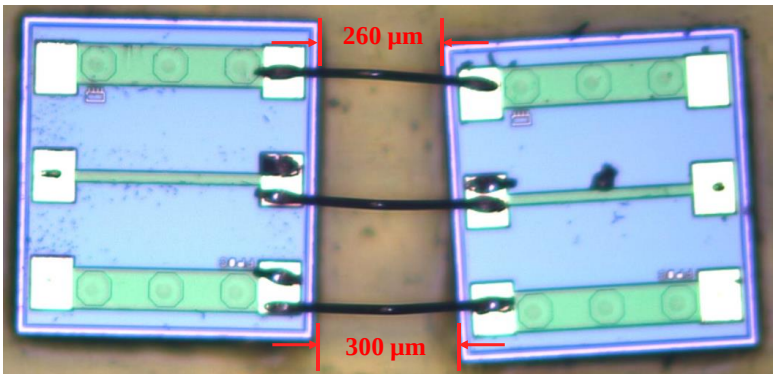


Figure 3.16 SoP with Wire-bonded interconnects.

of the silver was found to be 11 µm with a surface roughness of 0.25 µm. The complete SoP with CPW transmission lines interconnect and GaAs chips are displayed in Figure 3.15.

3.4.1.3 Wire-bonding

To evaluate the performance of the proposed interconnect, another SoP was fabricated with wire-bonding as shown in Figure 3.16. Initially, wire-bonding was attempted by bringing the bare dies as close as possible. But the stress on shorter sections of wires resulted in breakage. Eventually a smallest gap of approximately 260 µm provided stable wire-bonded connections. Aluminum wires with a wedge-wedge configuration were used.

3.4.2 Measurement Results

The S-parameters of the SoPs with AJ printed interconnect and wire-bonds and the bare die microstrip line were measured from 0.1-30 GHz using the Agilent N5227A PNA Network Analyzer and 250 µm probe pitch GGB Picoprobes. Losses associated with the equipment were corrected by LRRM calibration and moving the reference plane at the tip of the probes. The measured insertion loss is plotted in Figure 3.17. The insertion loss of a single interconnect can be estimated from the difference of the measured interconnected SoP and twice the loss of the single transmission line on the chip. It was determined to be 0.27 dB at 30 GHz for the AJP interconnect

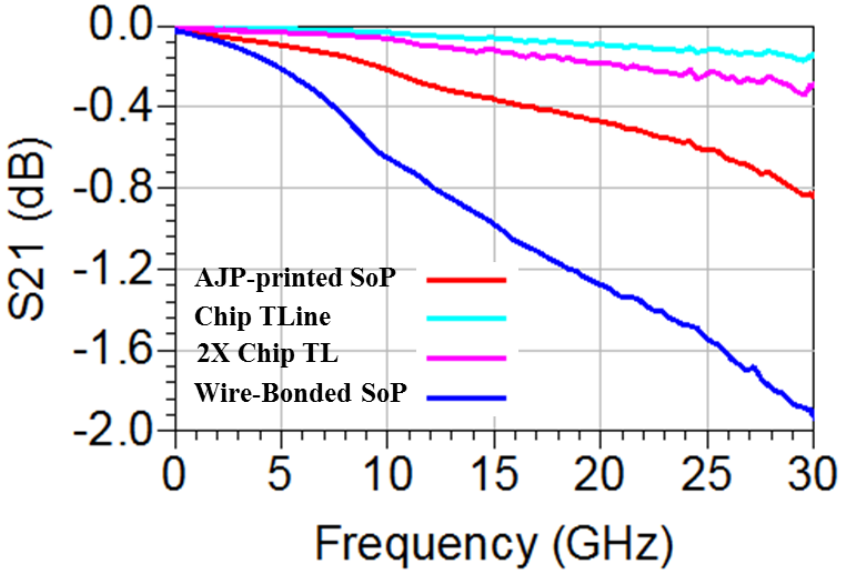


Figure 3.17 Measured S21 of the SoPs including the dies and interconnect.

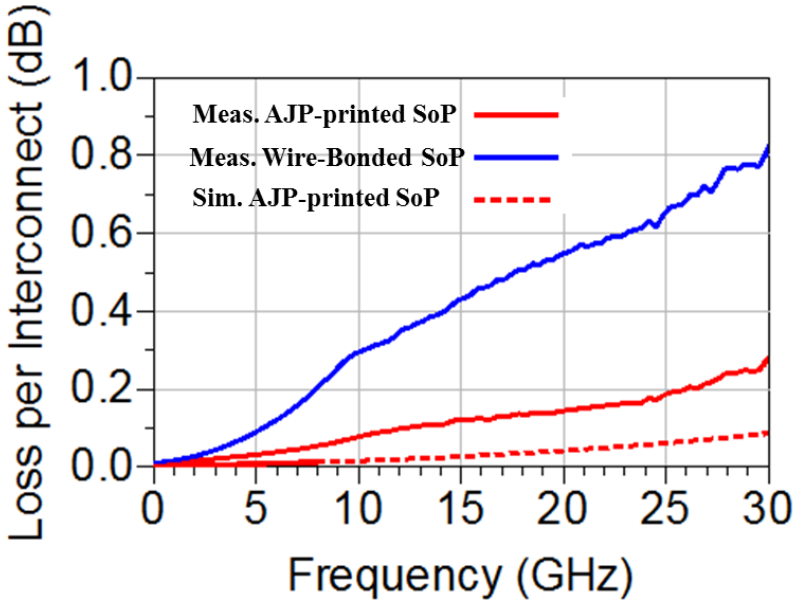


Figure 3.18 Measured interconnect loss calculated by subtracting the measured loss of the stand-alone dies from the SoPs.

whereas it was 0.8 dB with the wire-bonded interconnect as displayed in Figure 3.18. The return loss for the AJP SoP is better than 15 dB from 0-30 GHz as plotted in Figure 3.19 and 3.20, where a degradation of the bandwidth is evident for the wire-bonded SoP owing to its series inductances. Also, unlike the wire-bonding technique, the chip-first approach using AJP allows smaller die

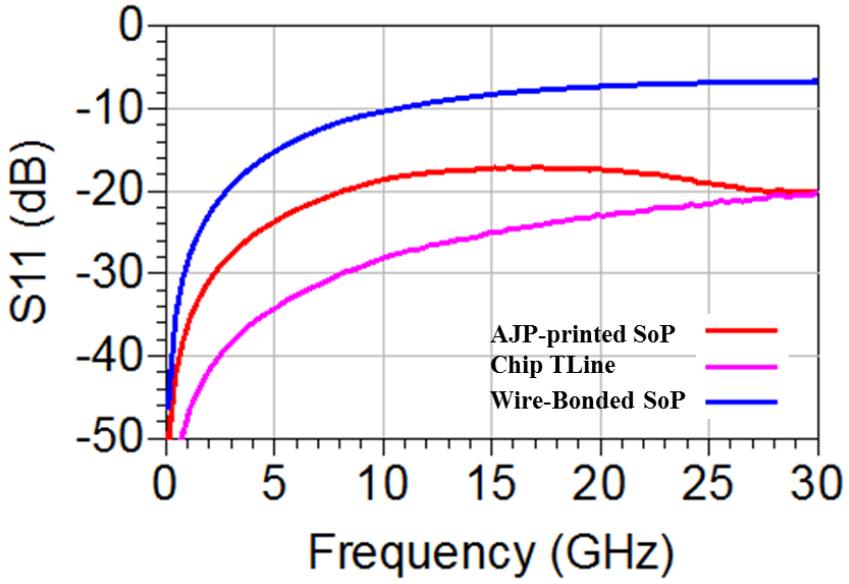


Figure 3.19 Measured S11 of the SoPs and stand-alone die.

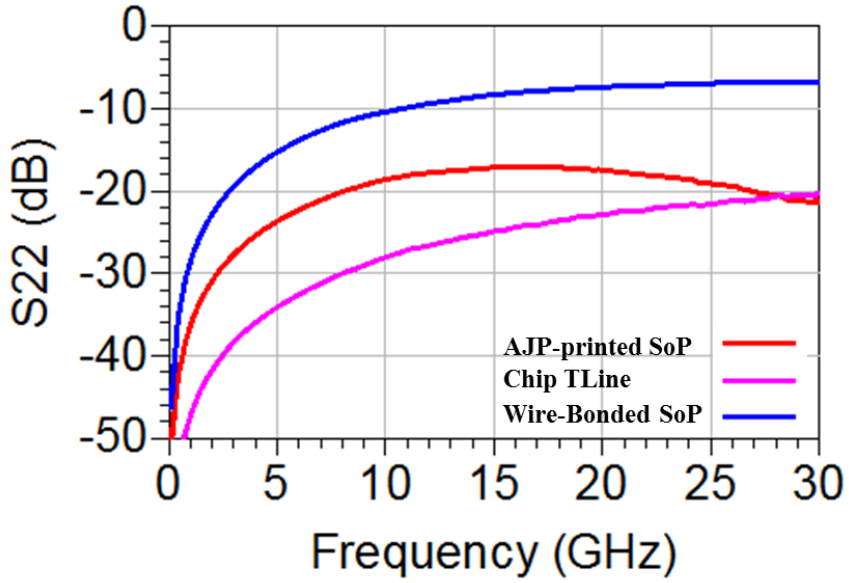


Figure 3.20 Measured S22 of the SoPs and stand-alone die.

spacing, reducing the overall loss of the interconnect and dimension of the package. The performance of the realized AJP interconnect is compared to the recent AM interconnects and tabulated in Table 3.1. The chip-to-chip AJP interconnects realized using the chip-first approach shows the best performance among other AM processes. It achieves very similar performance to the previously demonstrated die-to-package chip-first packaging solution.

Table 3.1 Performance comparison of the realized interconnect with the state-of-the-art

	Packaging Technique	Die	S21 (20 GHz)/dB	S21 (30 GHz)/dB
This Work[$]	**AJP**	**COTS GaAs***	**-0.143**	**-0.269**
	Wire-bonding		**-0.545**	**-0.803**
MWCL'19 [8]	AJP	COTS GaAs*	-0.146	~-0.26
APMC'18 [9]	AJP		-0.22	N/A
EuMC'18 [10]	AJP	PCB	~-1	~-1.4
GeMiC'18 [1]	AJP	PCB	~-1.3	N/A
IMS'16 [5]	Inkjet	Blank Si	~-1.5	~1.6
EuMC'18 [6]	Inkjet	COTS GaAS[+]	-0.5 @ 24.5GHz	~-0.8

[$]die-to-die interconnect

[*]Minicircuits KAT-0-DG+ die

[+]Triquint TGL4201-00 die

3.5 Conclusion

In this chapter we suggested the application of additive manufacturing technology for ultra-wideband interconnect as an alternative approach to conventional bonding processes. This novel technique does not suffer from disadvantages like discontinuity, detuning and parasitic effects while still being cost-effective, fast, clean and reliable.

In the first section, a dummy chip was employed to imitate the die to package interconnection. For the second part, two COTS GaAs 0-dB attenuators was utilized. The attenuators were attached to a glass slide using Kapton tape and a die-to-die interconnection was demonstrated. The performance of this realized interconnect, being similar to the state-of-the-art demonstrated die-to-package interconnect using AJP, substantiates that it is a substrate independent process. A control sample using the more traditional wire-bonded interconnect was also demonstrated for comparison and it had a loss of 0.8 dB per interconnect, which is three times worse than the proposed approach.

CHAPTER 4

CONCLUSION

4.1 Summary

In this dissertation, a next generation microsystem has been proposed and demonstrated using the state-of-the-art IC technology and additive manufacturing. We begin this work by investigating two advanced technologies, both of which aim to deliver high performing systems. Our goal was to integrate the two technologies in developing a new set of microsystems, where the drawbacks of one technology can be recovered by the other and vice versa.

In chapter 2, we designed, simulated and characterized multiple transceiver components for mm-wave applications. High performance SiGe process was utilized for the realization of these blocks because it offers a high level of integration at an affordable cost without sacrificing too much in terms of RF performance. With an immense increase in the number of networked devices, the current sub-6 GHz bands will struggle to support the "data explosion" and the migration to the mm-wave bands is imminent. Therefore, we focused on the development of mm-wave components that can support multiple communication standards and adapt according to specific applications.

We designed a quarter-wave shunt SPDT switch with reverse-saturated HBTs that supports a frequency range of 20 to 60 GHz. We studied the effect of base loading and its role in improving the linearity of the switch as well as in tuning the bandwidth of the switch. The minimum insertion loss was measured to be 1.7 dBm at 40 GHz with less than 2.7 dBm loss for the entire band of interest. The fractional bandwidth of the switch is 101.2 %, which is the highest value for similar bands in silicon technologies.

Following the SPDT switch, we designed a 28 to 60 GHz multi-band LNA for the receiver chain. A two-stage cascode topology with emitter degeneration was chosen to achieve the desired

bandwidth without trading-off too much noise and gain. The LNA design procedure is explained meticulously- beginning with the choice of transistor sizes, followed by biasing, topology and matching networks. The inter-stage matching network, that enabled the wider bandwidth, was designed using a T-type topology. A step-by-step guideline was provided to demonstrate how it can improve the bandwidth of the LNA. The LNA achieved a mean NF of 2.87 dB, with 2.4 dB and 3.4 dB NF at 28 and 60 GHz respectively. It exhibited more than 14 dB gain and 10 dB input return loss from 28 to 60 GHz. In terms of bandwidth, multi-band functionality, and NF, the realized LNA shows better performance than other state-of-the-art LNAs in similar technologies.

To convert the high mm-wave RF signal to IF signal, a compact ultra-wideband downconverting mixer was realized using the micromixer topology. The inclusion of the active baluns at the LO and IF ports along with the micromixer topology enabled such performance with a chip area of 0.019 mm^2. The measured conversion gain is 6 ± 1 dB for 5-67 GHz RF frequency while the simulated result shows that the bandwidth extends up to 120 GHz.

Two separate upconverting mixers were designed for the transmitter chain at the Ka- and V-band using the doubled-balanced Gilbert-cell topology with on-chip transformer baluns at the LO and RF ports. Designing such transformer baluns requires careful considerations. Therefore, a proper guideline for realizing them was presented along with the design of the upconverting mixers. For the Ka-band mixer, the maximum conversion gain obtained is 13.7 dB at 26.5 GHz and an OP1dB of -1.5 dBm at 28 GHz. The V-band mixer has a maximum conversion gain of 13.4 dB at 57 GHz and OP1dB of -1.4 dBm at 60 GHz.

To evaluate the performance of the SiGe at W-band, a frequency tripler was also developed. It uses a single-balanced differential pair core which is generally a popular topology for realizing doublers. However, in our work, the third harmonic component was mainly generated by

overdriving the core as Class A amplifiers followed by harmonic amplification. Further improvement was achieved by promoting the mixing of the fundamental input signal with its own generated second harmonic at the common node. The performance of the realized tripler was found to be comparable to those of the state-of-the-art triplers in similar technologies whilst occupying only half of the chip area.

In chapter 3, we developed a module integrating additive manufacturing and ICs. An ultra-wideband interconnection between chip-to-board was demonstrated using the 'chip-first' approach. Aerosol Jet printing, one of the front runners among digital printing technologies, was used. A curing profile for the silver nanoparticle ink was also developed. The interconnects had an insertion loss of 0.49 dB/mm at 110 GHz which agreed with the simulated result.

Eventually, two commercial-off-the-shelf (COTS) 0-dB attenuators in GaAs were connected using the chip-first approach and coplanar waveguide lines (CPW) and no bottom ground connection. The approach is substrate-agnostic and facilitates interconnections with smaller die spacing on any host substrate. Our chips that are designed using the SiGe process uses aluminum pads that readily oxidize when they come in contact with air. Due to this thin layer of native oxide, adhesion with the printed silver ink is poor. Also, the DC electrical connection cannot be established. Owing to these reasons, we used COTS dies with gold pads for this demonstration. The interconnect operates from DC-30 GHz with maximum loss of 0.27 per interconnect dB at 30 GHz.

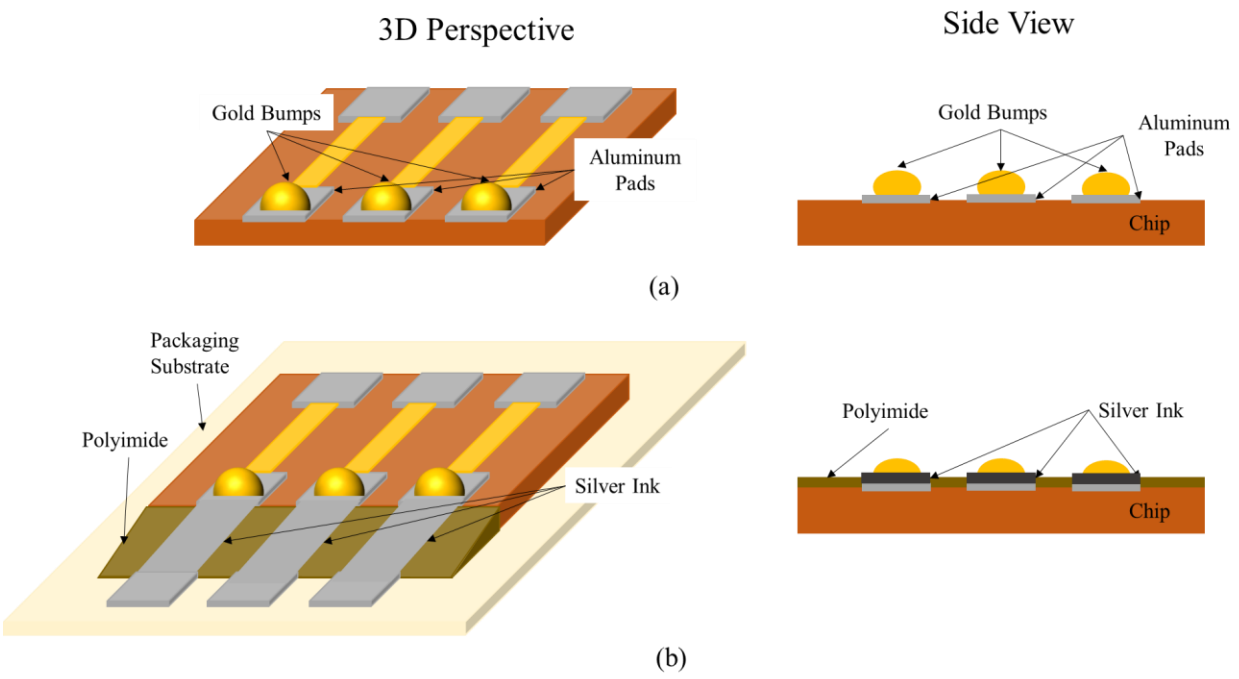


Figure 4.1 Diagrammatic representation of the packaging approach using ball bonds and AJP.

4.2 Further Work

4.2.1 Packaging ICs with Aluminum Pads

Since all the ICs designed as part of the project have aluminum pads, we propose a solution to overcome the difficulties that limit the usage of AJP for packaging ICs with aluminum pads. The proposed approach uses gold bumps on aluminum pads as depicted in Figure 4.1. Wire-bonders with ball bonds option can be used for this purpose. Such method ensures that a strong electrical connection is formed between the pads and the balls sitting on top of the pads. The ball material, being gold, is much for resilient to oxidation in the presence of atmospheric air. Thus, the issue arising from the native aluminum oxide can be resolved. Then the gold bonds can be either connected to the packaging substrate as shown in Figure 4.1 (b) or can be connected between two bare ICs using the AJ-printed silver ink. Preliminary experiment was performed using the in-house wire-bonder and a transimpedance amplifier IC in SiGe process as displayed in Figure 4.2.

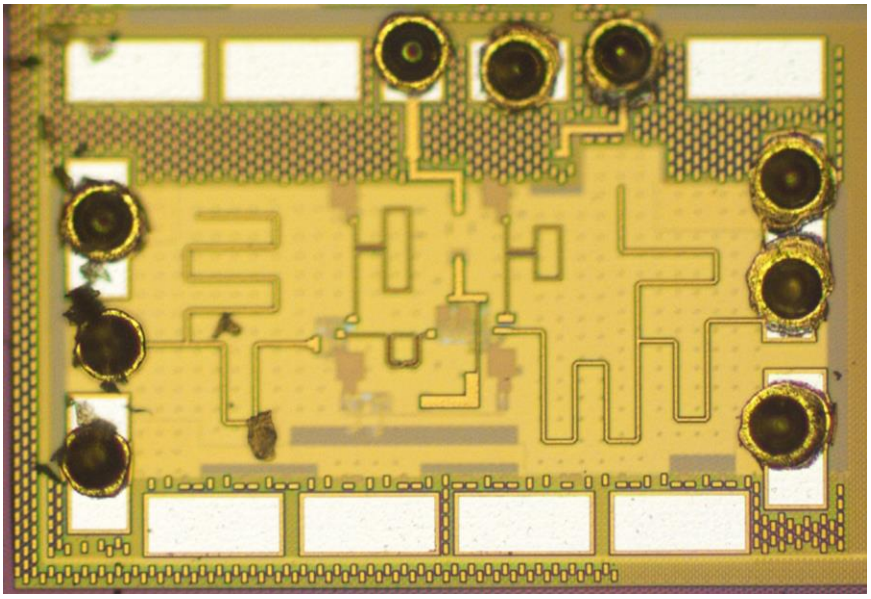


Figure 4.2 A typical IC in SiGe process with ball bonds on top of the aluminum pads.

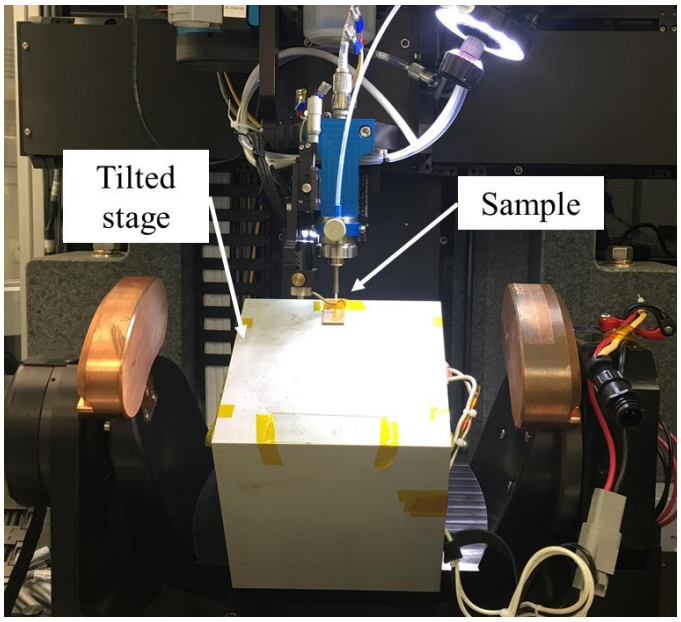


Figure 4.3 The Optomec Aerosol Jet 5X Printer in a tilted-stage configuration.

Unfortunately, due to bigger ball bonds formed by the wire-bonder, the signal and ground pads were shorted. In future, the approach can be tested using a wire-bonder that can support finer bonding tip and smaller ball bonds.

One problem that the proposed approach may suffer from is the printing of the silver ink at the base of the ball bonds where they meet the pads. If the surface of the ball bond is perpendicular to the surface of the pad, the silver line from the ball bond to the substrate might be discontinuous. To ensure a continuous connection, the mounting stage of the Optomec 5X printer can be tilted and additional layers of silver can be printed at the intersection of the ball bonds and pads as shown in Figure 4.3.

4.2.2 Packaging Active Circuits

The work done so far can be further extended by repeating this chip-to-chip interconnection using active chips such as LNAs and mixers. Since, the AJP printed interconnect is substrate-agnostic, active devices on different platforms can be integrated together without performance degradation. The printing process is clean and does not impose any mechanical stress on the chips, the chips can be recovered from their corresponding packages and can be reused like a Lego.

4.3 Conclusion

In conclusion, the proposed approach of realizing mm-wave modules using AJP and advanced IC technologies is very promising and can replace the existing packaging technologies like wire-bonding and flip-chip bonding. It does not suffer from unwanted effects like series inductance from bond wires or detuning due to coefficient of thermal expansion in case of flip-chip bonds. In addition, circuit parasitics that are more evident in mm-wave circuits can be minimized using AJP interconnects.

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