EFFICIENCY AND LINEARITY ENHANCEMENT TECHNIQUES FOR SWITCHED-CAPACITOR POWER AMPLIFIERS AND TRANSMITTERS

By

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ABSTRACT

EFFICIENCY AND LINEARITY ENHANCEMENT TECHNIQUES FOR SWITCHED-CAPACITOR POWER AMPLIFIERS AND TRANSMITTERS

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As wireless communication standards evolve, radio frequency (RF) transmitter (TX) systems with higher linearity and wider bandwidth at increased output power (P_{OUT}) are required to meet the high demand for faster communication speeds and increased data traffic. Meanwhile, mobile and wearable applications require a smaller form factor and low-cost solutions. Low power consumption is also critical for increased battery life, which improves user experience. Digital TX is a promising architecture for a small area and low power consumption because conventional TX sub-blocks, such as digital-to-analog converter (DAC), mixer, driving amplifier, and power amplifier (PA), can be merged into a single block. Furthermore, the linearity, area, and power consumption of a digital TX can be significantly enhanced with the evolution of complementary metal oxide semiconductor (CMOS) technology that provides faster operation and finer segmentation at lower power dissipation. It is easy to migrate to the next generation CMOS process because the digital TX mostly comprises digital circuits. These advantages are more critical when there are multiple TXs in a single system, such as multi-standard and multi-in multi-out systems. A switched-capacitor (SC) PA or an SC RFDAC is employed as a base architecture in this study, ideally providing 100% peak efficiency as a segmented switching-mode PA; further, unlike conventional PAs, it does not suffer from a large output signal swing that modulates output impedance, causing amplitude and phase nonlinearities.

This study demonstrates various architectures and design techniques for compact, highly efficient, and highly linear digital TXs. The contributions of this study are as follows:

First, a watt-level highly efficient and highly linear quadrature digital TX with a dual-supply Class-G quadrature *IQ*-cell-shared SCPA architecture is proposed, which maximizes the P_{OUT} and efficiency of the quadrature digital TX. To enable the Class-G operation in the quadrature *IQ*-cell-shared SCPA architecture, a merged-cell-switching technique is proposed. Linearization techniques for the Class-G operation are proposed to compensate for the amplitude and phase mismatches between the two Class-G modes.

Second, a compact and highly linear quadrature digital TX based on quadrature *IQ*-cell-shared SC RFDAC with linearization techniques is proposed; the linearization techniques increase the TX dynamic range by improving the TX linearity in both high and low P_{OUT} regions. Impedance linearization techniques for the output stage and an offset mid-tread code mapping technique improve the TX linearity in the high and low P_{OUT} regions, respectively. The area and power consumption of the RFDAC are minimized by sharing sub-circuits between the two RFDAC cells.

Finally, a multimode multi-efficiency-peak SCPA architecture is proposed to maximize power back-off (PBO) efficiency in a polar digital TX. The multimode operation is achieved through an efficient combination of the dual-supply Class-G, Doherty, and 2-way time-interleaving techniques, thus, maximizing the PBO efficiency by introducing six efficiency peaks down to 18-dB PBO. A single-supply current-reuse Class-G switch is proposed for the highly efficient Class-G operation without any additional power management unit. Moreover, a LO-signal-restoration technique is presented to minimize both the power dissipation and area for the LO signal distribution.

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First of all, I am grateful to the Lord for guiding me to pursue my Ph.D. degree and taking care of me and my family every moment. I dedicate this dissertation to the Lord, who is the shepherd of my life. Also, I supplicate to the Lord that every moment of my life will be in his plan.

My gratitude to my family is boundless. My parents' prayer and sacrifice made me finish my Ph.D. successfully. My wife, Seunghee, my two daughters Dain and Dajeong, and my son Seojin always made me happy and strong during my Ph.D. Their presence and love enabled me to overcome all difficulties.

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I send many thanks to lab mates at MSU. I am fortunate to have met with wonderful colleagues: Asad, Ibrahim, Xenofon, Shih-Chang, Jubaid, and Adamantia. They always stood by me and gave me plenty of precious memories. I learned many things from Asad, and he helped me every time for my research. Xenofon always helped me revise my papers.

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1 INTRODUCTION

In the recent times, small form factor, low power consumption, and low cost along with large-scale integration are essential for several mobile and wearable systems with wireless communication. Of late, the demand for cutting-edge cellular applications, such as fifth-generation (5G) cellular communications providing high data rates, and wireless connection among several devices over the internet, such as the Internet of Things (IoT), has rapidly increased. Therefore, to keep pace with technological innovation and benefit more people, it is crucial to develop compact, power-efficient, and low-cost wireless communication solutions. The advancement of complementary metal oxide semiconductor (CMOS) technology is expediting the development of these solutions by means of enabling high density, low cost, and low power consumption for digital integrated circuits. A significant part of wireless communication systems comprises digital circuits such as digital signal processors (DSPs). However, in a wireless communication system, if the bulky and high power-consuming analog and radio frequency (RF) functions can be replaced with the maximum number of digital functions as possible, the wireless communication system can significantly benefit from the advancement of CMOS technology. This study focuses on the realization of the digital transmitter architecture in wireless communication systems.

1.1 Basics of Wireless Communication System

Wireless communication is a method of transmitting and receiving information between two or more points, without electrical conductors such as wires or cables, and information is transmitted in the form of radio waves from transmitters (TXs) to receivers (RXs). The distance between the TX and RX can range from tens of centimeters for near-field communication (NFC)

or even thousands of kilometers for satellite communication. A block diagram of a conventional wireless communication system is presented in Figure 1-1.

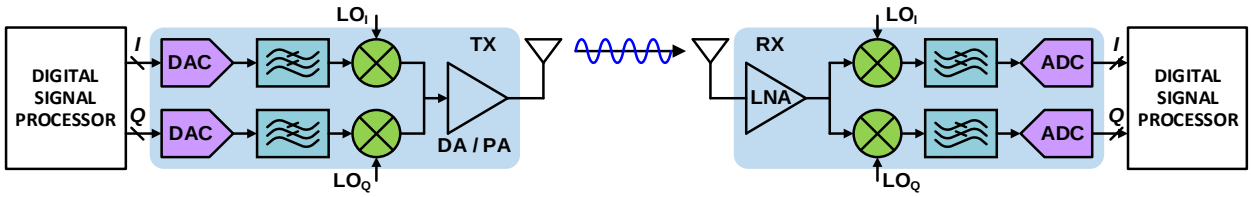


Figure 1-1. Block diagram of a wireless communication system.

A conventional quadrature RF TX comprises digital-to-analog converters (DACs), reconstruction filters, up-conversion mixers, a driving amplifier (DA), and a power amplifier (PA), as illustrated in Figure 1-1. In-phase (*I*) and quadrature (*Q*) digital baseband signals from a DSP are converted to sampled analog signals through DACs; thereafter, the reconstruction filter suppresses the spectral images of the sampled analog signals. The mixer upconverts the baseband analog signal to an RF signal by mixing the local oscillator (LO) signal. The DA and PA amplify and transmit the RF signal through the antenna.

Conventional RF RX comprises a low-noise amplifier (LNA), down-conversion mixers, lowpass filters, and analog-to-digital converters (ADCs), as illustrated in Figure 1-1. The RX operation is performed in a manner complementary to the TX operation. The LNA amplifies the weak signal received by the antenna; thereafter, the mixers downconvert the RF signal to the baseband *I* and *Q* analog signals by mixing the orthogonal LO signals. The lowpass filters reject other out-of-band signals that could be present in the received spectrum. Finally, the filtered analog output signals are converted to digital signals through the ADCs. Subsequently, the converted digital signals are processed in the DSP.

1.2 Modern Wireless Communication System

As wireless communication standards evolve, TX systems with a higher linearity and wider bandwidth at increased output power (P_{OUT}) are required to meet the high demand for enhanced communication speeds and increased data traffic. Meanwhile, mobile and wearable applications demand a smaller form factor and low-cost solution. Low power consumption is also critical for increased battery life, enhanced user experience, and multi-standard and multi-input multi-output (MIMO) systems with multiple transceivers (TRXs) in a single system. An example of multiple TRXs in a single system is presented in Figure 1-2.

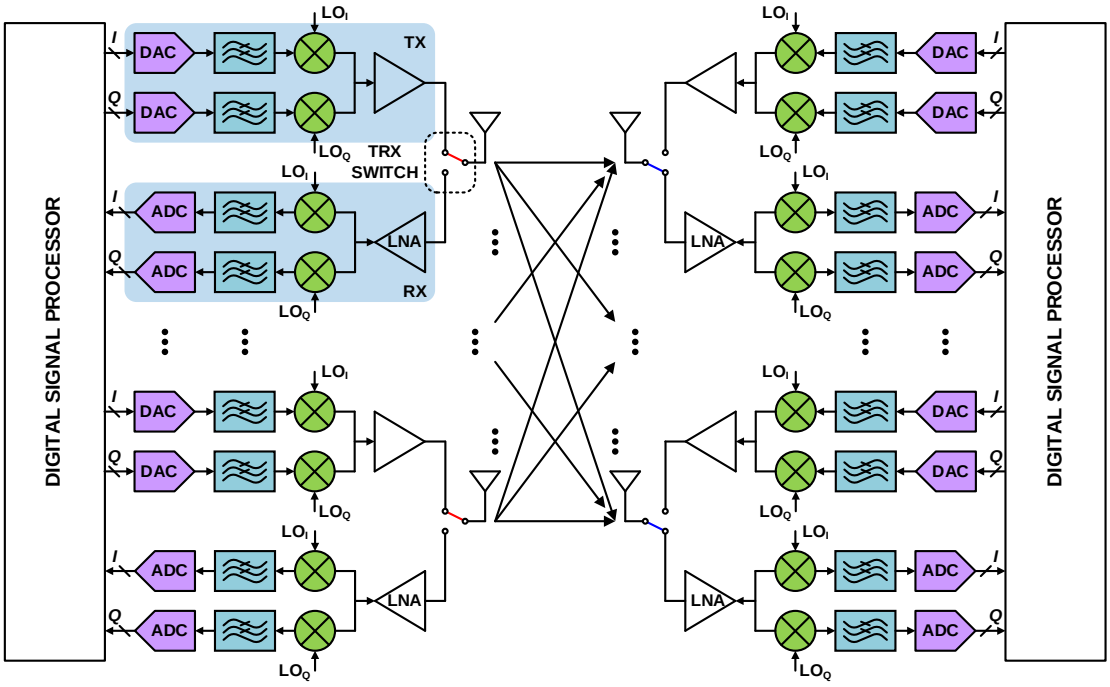
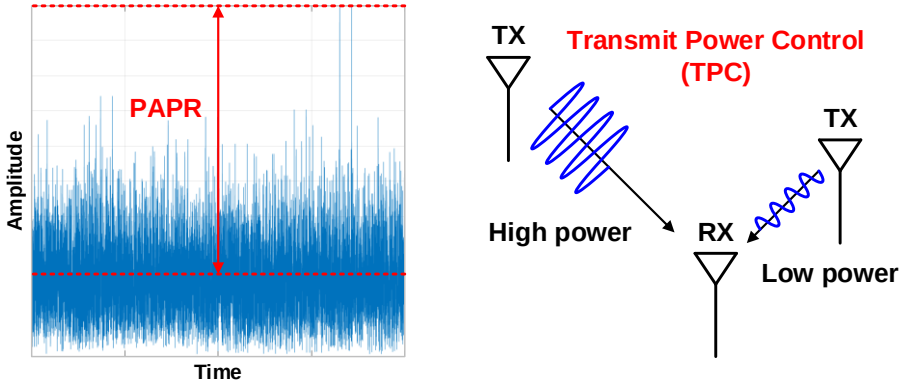


Figure 1-2. Example of multiple TRXs in a single system.

Additionally, high energy efficiency, especially at power back-off (PBO), is also required. Furthermore, along with the increasing demand for high data rates with the finite frequency bandwidth, highly-spectrally-efficient modulation schemes such as high-order quadrature amplitude modulation (QAM) orthogonal frequency-division multiplexing (OFDM) are essential

for wireless communication systems. However, the complex modulation schemes usually require a large peak-to-average power ratio (PAPR) (e.g., 10 to 13 dB), as illustrated in Figure 1-3(a), and this forces the TX to operate in the deep PBO region. Furthermore, TX P_{OUT} changes with the requirement for a transmit power control (TPC), as illustrated in Figure 1-3(b), and high efficiency for a wide range of P_{OUT} is required in the modern communication systems.



(a) (b)

Figure 1-3. (a) Large PAPR and (b) TPC.

1.3 Motivation for Digital TX

The demand for a high-performance TX with energy-, area-, and spectral-efficiency has increased in the era of multi-standards and MIMO wireless communication systems, which provide very high data throughput. Driven by the continuous evolution of process technology, digital TXs have garnered significant attention in the modern wireless communication system.

The conventional TX architecture has long been the standard architecture because it enables easy and efficient analog signal processing such as control gain and filtering. However, the conventional TX sub-blocks occupy a large area and consume high static current even when delivering a low P_{OUT}. Moreover, it is difficult to benefit from the CMOS process migration because the process scaling cannot be directly applied to the analog sub-blocks.

However, the digital TXs or digital PAs, which use an array of small unit PA cells controlled by a digital code word to modulate amplitude and phase, have exhibited significant promise towards small and low-power TXs [1]–[43]. The digital TXs can save a significant amount of power consumption and area because they combine the function of the DAC, upconversion mixer, DA, and PA into a single circuit block, as illustrated in Figure 1-4. The digital TX with the advanced process technology is even more beneficial, providing faster switching and finer segmentation at a lower power dissipation.

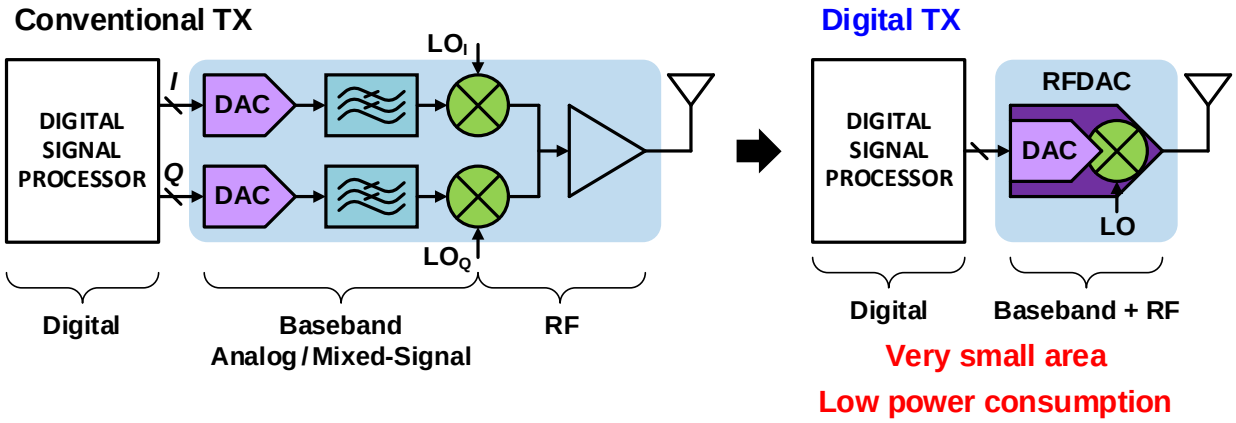


Figure 1-4. Area- and power-efficient digital TX.

1.4 Challenges facing Digital TX Design

It is significantly more challenging to design a RFDAC in the digital TX than the baseband DAC in the conventional TX for the following reasons: First, an additional resolution is required for the RFDAC to achieve the same resolution identical the conventional TX in the PBO region because the digital TX does not have any gain stage in the TX chain. Second, it is not easy to maintain high linearity in RFDAC because P_{OUT} and the operating frequency of the RFDAC are typically much higher than those of the baseband DAC. Third, unlike the conventional TX, the digital TX can emit spectral images because it does not have an analog low pass filter. To suppress

the spectral images and meet the federal communications commission (FCC) emission limits and spectral mask requirements, digital signal processing for filtering function or increased sampling rates are required.

1.5 Switched-Capacitor Power Amplifier

Among the digital PA architectures, switched-capacitor PA (SCPA) [11] has advantages in efficiency, linearity, and compatibility for several efficiency enhancement techniques. The SCPA provides high efficiency based on switching operations. Moreover, unlike conventional PAs, SCPA does not suffer from the large output signal swing that modulates output impedance and degrades the amplitude and phase linearities such as amplitude modulation (AM)–AM and AM–phase modulation (PM) distortions. Additionally, it achieves good linearity because capacitors provide excellent matching in a CMOS process.

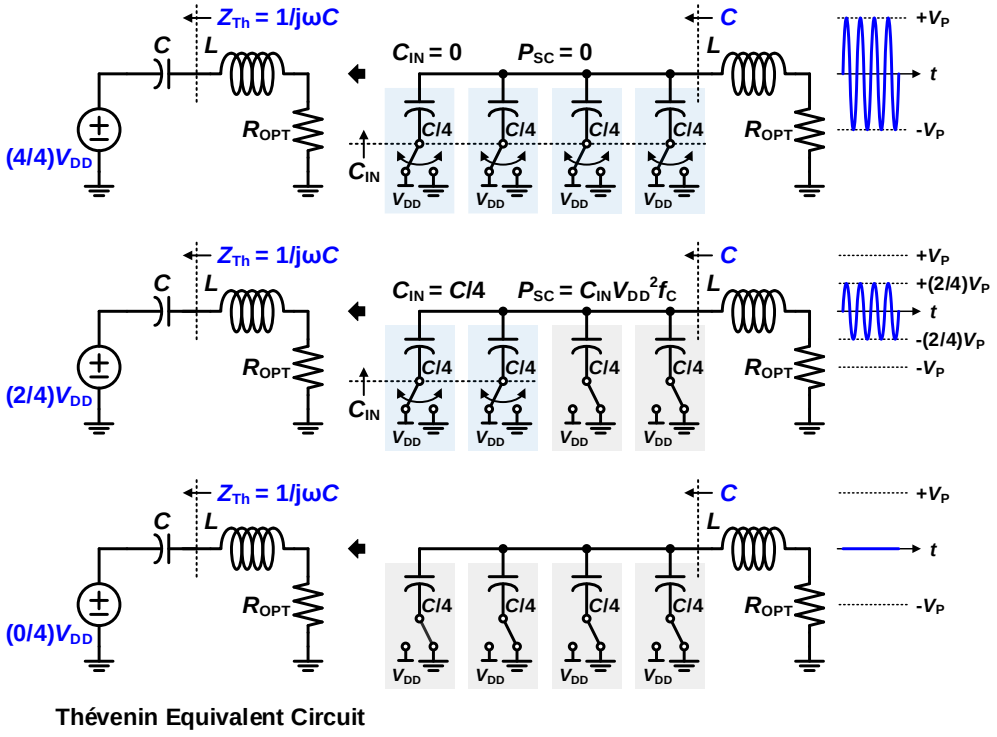


Figure 1-5. Schematic and operation of the SCPA.

In Figure 1-5, the schematic and operation principle of the SCPA are presented. The number of capacitors switching between V_{DD} and V_{SS} in the capacitor array determines the P_{OUT} of the SCPA, as illustrated in Figure 1-5. For example, if four capacitors are switching simultaneously, the SCPA generates the highest voltage. When only two capacitors are switching among the four capacitors, the SCPA generates only half the voltage. In this case, there is power dissipation in the capacitor array for charging and discharging the capacitors at RF.

Efficiency-enhancement techniques such as Class-G [12][23][27][33], Doherty [34]–[38], and subharmonic switching [39][40] have been employed to improve the average efficiency of the SCPA.

1.6 Polar and Quadrature Transmitters

The polar PA [1]–[15][28][31][34]–[40][42], illustrated in Figure 1-6(a), exhibits high P_{OUT} and high efficiency because it can transmit maximum P_{OUT} to every angle with high energy efficiency, but it requires a complex coordinate rotation digital computer (CORDIC) and wideband phase modulator. In addition, it is not easy to precisely align amplitude and phase data in two separate paths, and the mismatch between the two paths leads to signal distortion [11]. Meanwhile, a quadrature architecture, as illustrated in Figure 1-6(b), demonstrates a simple structure and a wide bandwidth without a supply modulator or CORDIC. However, this architecture exhibits a lower P_{OUT} with degraded efficiency because the output signal requires representation using two orthogonal *I* and *Q* vectors. Consequently, this conventional fixed *I* / *Q* array architecture provides 3–6 dB lower P_{OUT} and a degraded drain efficiency than those of the equivalent polar digital TX.

A quadrature *IQ*-cell-shared digital TX architecture [25]–[27][33][41][43], as illustrated in Figure 1-6(c), provides increased P_{OUT} and energy efficiency in a quadrature architecture with an

I / *Q* input signal. First, this architecture combines *I* and *Q* unit vectors in the digital domain and then generates a set of new *IQ*-combined unit vectors that are 45° phase-shifted from *I* and *Q*. The architecture delivers the maximum P_{OUT} at 45°/135°/225°/315° in which signals can be represented with a single *IQ*-combined unit vector. Figure 1-7 presents the four-phase unit vectors generated from the *I* /*Q* combination. The *IQ*-combined unit vectors and their *I* and *Q* component vectors are denoted by [*i*, *q*], [*i*, 0], and [0, *q*], respectively, where both *i* and *q* are ±1. In Figure 1-7, 25% duty cycle LO signals are employed for the *I* /*Q* vectors that yield 50% duty cycle *IQ*-combined LO signals [25].

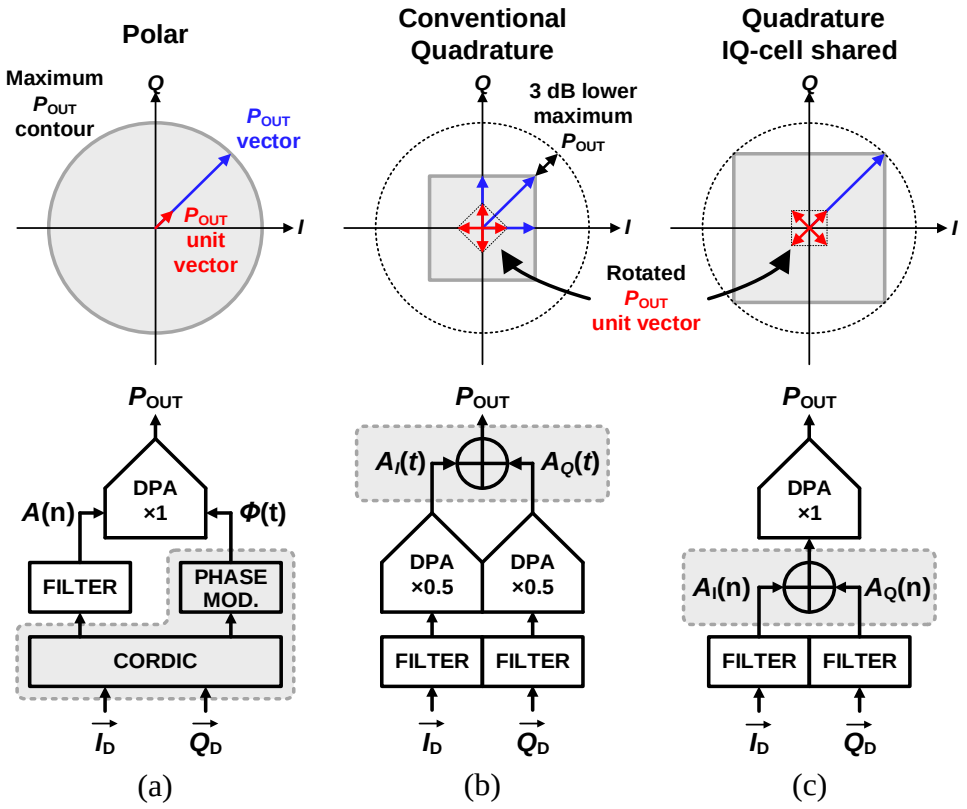
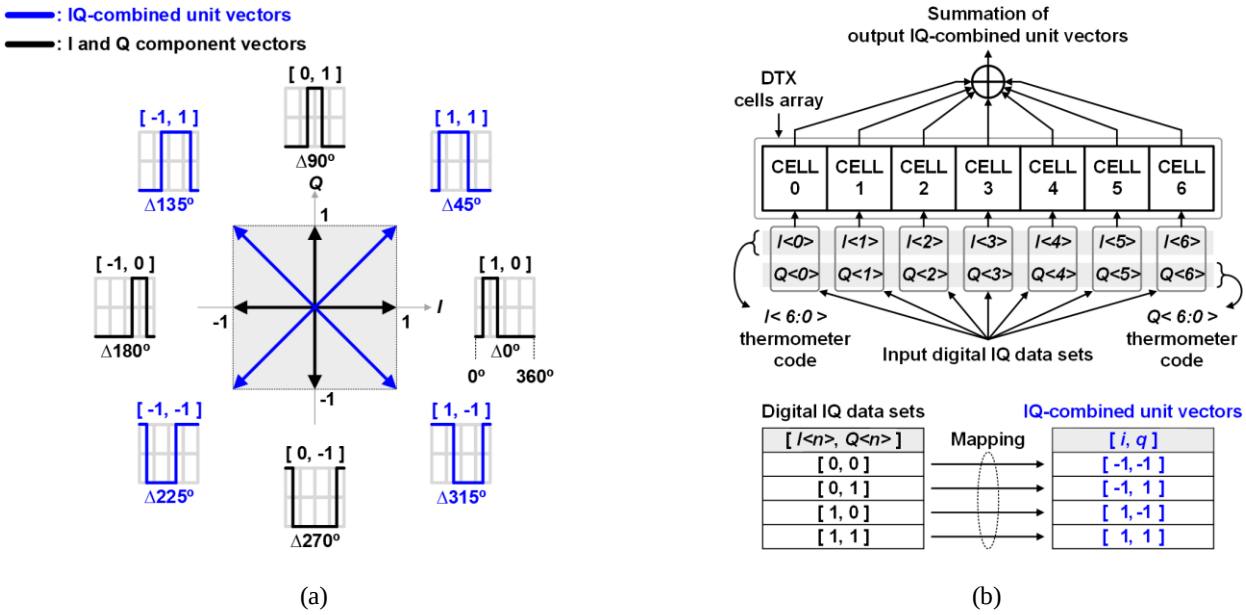


Figure 1-6. (a) Polar, (b) conventional quadrature, and (c) quadrature *IQ*-cell-shared digital TX architectures.

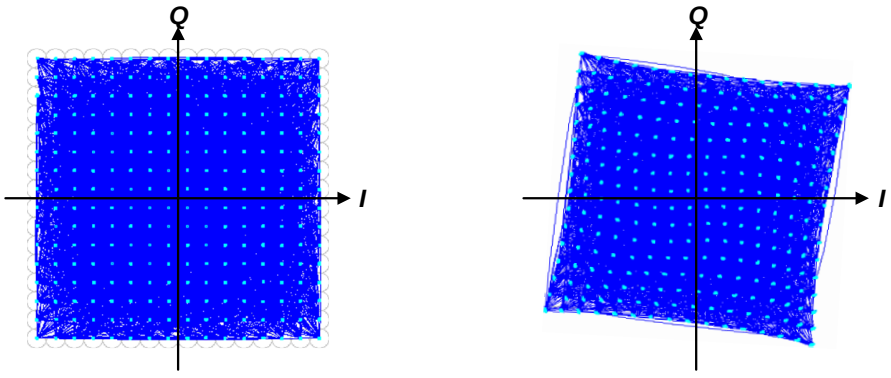
Second, all the digital TX cells can be assigned to the same vector simultaneously because there are no dedicated *I* /*Q* arrays, as illustrated in Figure 1-7. For example, a 3-bit digital TX

operates with seven pairs of thermometer codes I <6 : 0> and Q <6 : 0> that comprise IQ data set [I <n>, Q<n>] of each digital TX cell, as described in Figure 1-7(a). Each cell outputs one of the four IQ-combined unit vectors, as illustrated in Figure 1-7(b), and they are combined at the summing node of the digital TX. Consequently, the quadrature IQ-cell-shared digital TX achieves an increased P_{OUT} and drain efficiency without any designated I /Q arrays.



(a) (b)

Figure 1-7. (a) *IQ*-combined unit vectors of quadrature *IQ*-cell-shared digital TX. (b) An Example of 3-bit quadrature *IQ*-cell-shared digital TX.



(a) (b)

Figure 1-8. Examples of (a) ideal constellation and (b) constellation with 2-D distortion.

Among the digital TX architectures, polar architecture is complex in both digital and analog domains owing to the CORDIC and phase modulator, respectively. However, the RFDAC in a polar digital TX is simple and generates only amplitude data. Alternatively, a quadrature digital TX realizes a complete TX system without the need for additional circuits and can support a wide bandwidth. However, its RFDAC is significantly more complex than that of the polar digital TX owing to the two-dimensional (2-D) I/Q data. The linearity of two one-dimensional (1-D) RFDACs; quadrature RFDAC cells operate with 90 phase-shifted signals that dynamically modulate the output impedance, causing 2-D distortion illustrated in Figure 1-8 and typically require complex, 2-D digital pre-distortion (DPD). Furthermore, compared to a polar RFDAC with phase rotation in the system, a quadrature RFDAC has 1.5b less-effective resolution to represent signals with random distribution (e.g., OFDM).

High-density modulation (e.g., 1024 QAM) for modern wireless standards such as IEEE 802.11ax requires -35 dB error vector magnitude (EVM), and <-40 dB EVM is preferred, considering additional phase noise and other nonlinearities. Moreover, for 20 to 30 dB of TPC, the RFDAC requires an additional 3-to-5b of the resolution, which significantly complicates the design.

1.7 Efficiency Enhancement Techniques for Digital TX/PA

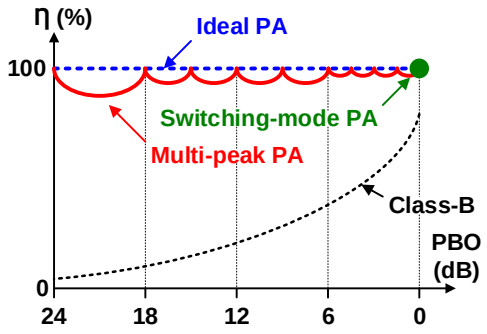


Figure 1-9. Drain efficiency of switching-mode PA with multiple efficiency peaks.

A switch-mode PA combined with efficiency-enhancement techniques is a suitable architecture for high average efficiency because a switch-mode PA has ideally 100% efficiency at the peak P_{OUT}. Meanwhile, digital TX or digital PA [1]–[43] has been extensively investigated with the advances of CMOS technology. Digital PA architectures correspond with the switch-mode PA because the digital PA can be implemented with a segmented switch-mode PA. Furthermore, efficiency-enhancement techniques can be easily integrated into digital PAs to enhance PBO efficiency by providing additional efficiency peaks. For a digital PA, each segmented PA cell can independently change the operation mode for efficiency enhancement, resulting in a significantly improved, seamless efficiency, and linearity at PBO [12][15][33]–[42]. Multiple efficiency peaks with a seamless efficiency curve connecting them can realize a near-ideal efficiency for a wide range of P_{OUT}, as illustrated in Figure 1-9.

1.7.1 Class-G SCPA

The Class-G technique significantly enhances average efficiency by employing multiple supply voltages. In the SCPA architecture, the Class-G technique not only introduces additional efficiency peaks but also seamless transitions between the peaks such as Doherty, as illustrated in Figure 1-10 [12]. The seamless efficiency curve can be achieved in the SCPAs because each capacitor can switch with different supply voltages owing to the capacitor as a direct current (DC) blocking component, as illustrated in Figure 1-10. However, multiple supply voltages require extra hardware, such as external PMUs, leading to increased power consumption and cost. Multiple supply voltages may also cause linearity degradation owing to the mismatch between the supply voltages.

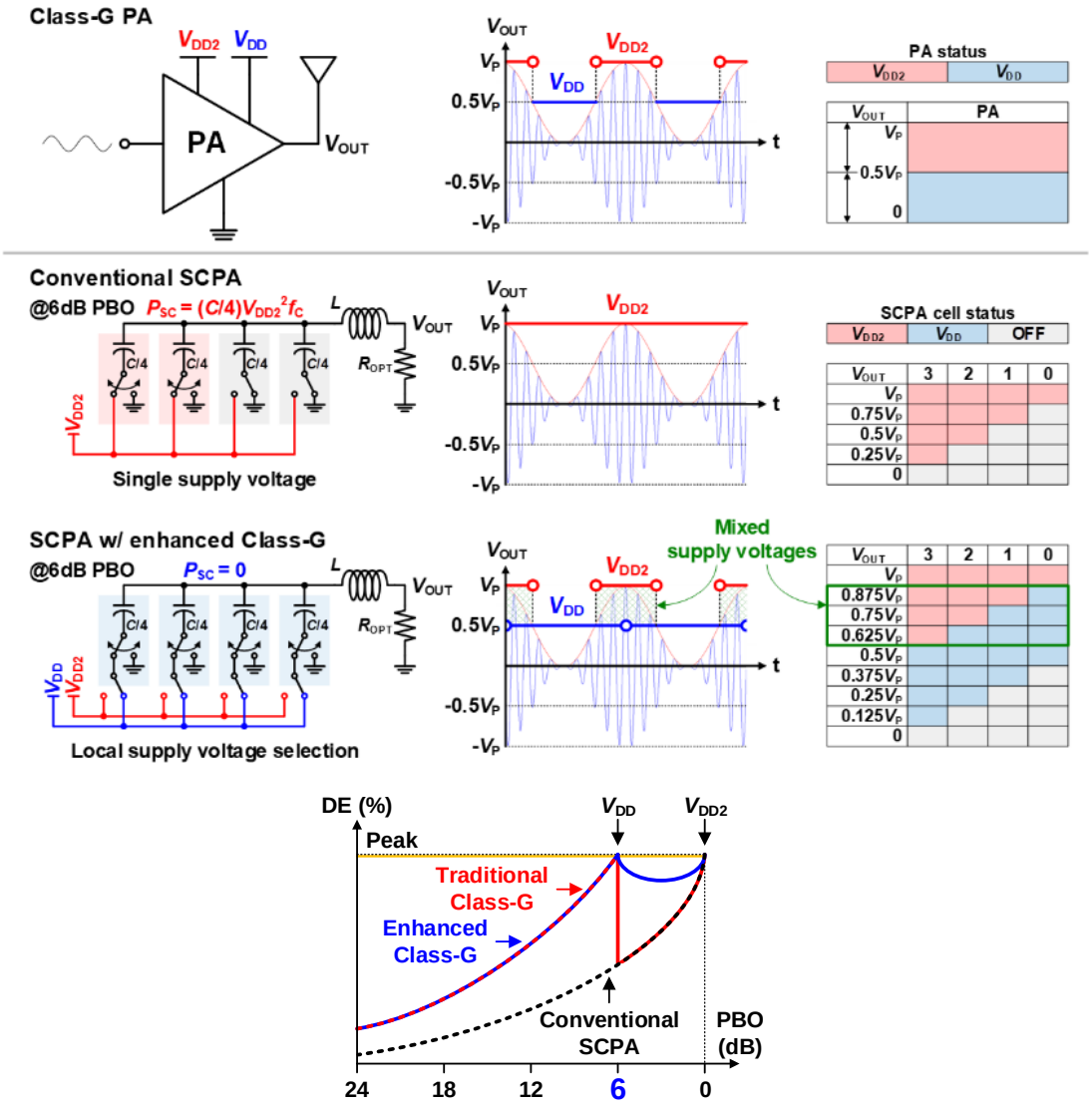


Figure 1-10. Operation and drain efficiency of Class-G SCPA.

1.7.2 Transformer-based Doherty SCPA

The transformer (XFMR) based Doherty technique achieves load modulation and introduces additional efficiency peaks with seamless transitions between the peaks in the PBO region through the sequential operation of peak SCPA cells, as illustrated in Figure 1-11. With an N-way XFMR power combining, for example, N-1 additional efficiency peaks can be achieved in the PBO region [34]. However, owing to the unideal and unbalanced XFMR power combining, efficiency enhancement can be limited [30][35]. The concept of unideal and unbalanced XFMR power

combining is illustrated in Figure 1-12(a). The P_{OUT} of the main-PA is coupled to the XFMR and back to the peak-PA through the reverse coupling at PBO. Accordingly, energy is lost in the unideal XFMR and switched capacitor network. Meanwhile, better efficiency can be achieved through balanced power combining while suppressing the reverse coupling, as illustrated in Figure 1-12(b). However, this approach experiences difficulties with the configuration of multiple PAs.

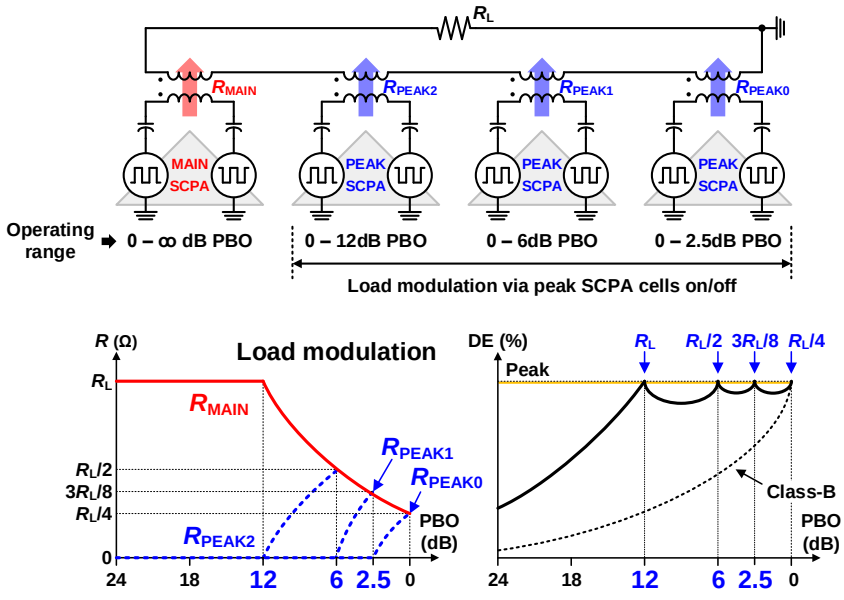


Figure 1-11. Operation and drain efficiency of XFMR-based Doherty SCPA.

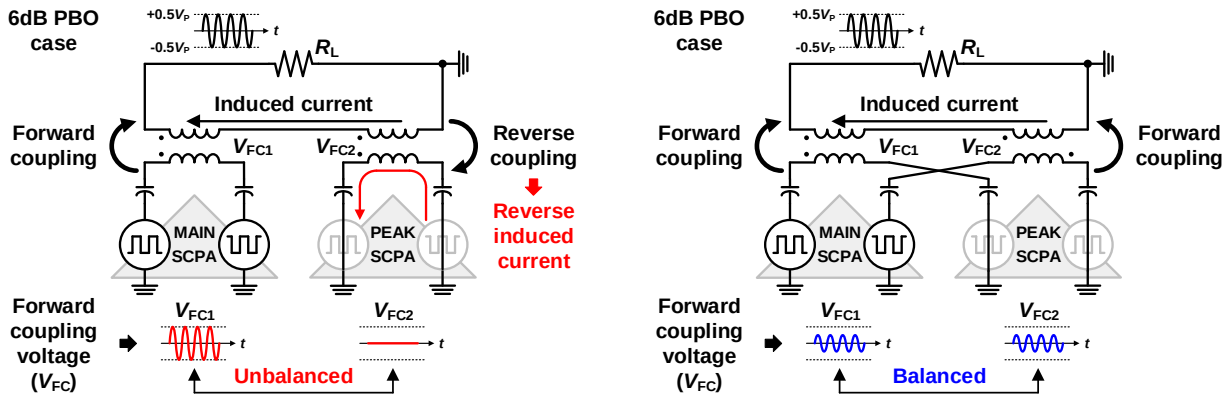


Figure 1-12. XFMR-based Doherty SCPA with (a) unbalanced XFMR power combining and (b) balanced XFMR power combining.

1.7.3 Time-Interleaved SCPA

Subharmonic switching technique [39][40] can provide additional efficiency peaks with seamless transitions at PBO by sequentially switching digital PA cells between fundamental LO signal and LO signals with subharmonic frequency components (LO1 and LO2). The subharmonic switching technique with phase interleaving [40] can be understood as a time-interleaving (TI) technique in the time domain, operating PA cells in the PA in a time-interleaved manner.

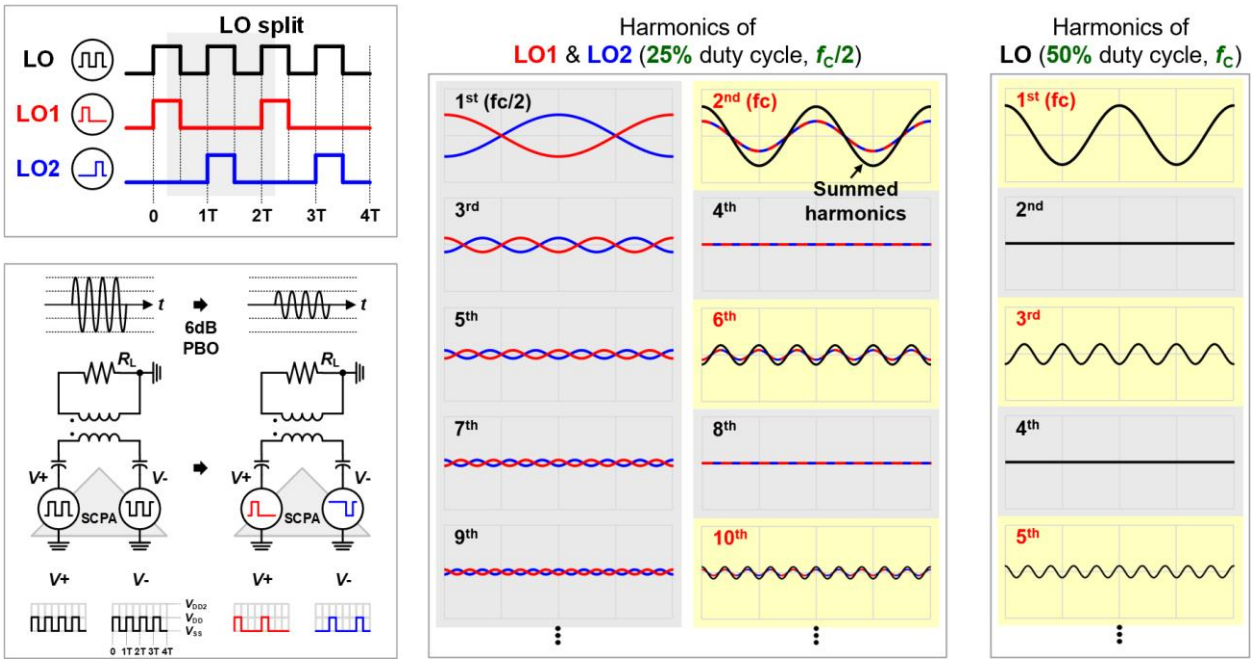


Figure 1-13. Concept of TI SCPA.

As presented in the upper-left figure in Figure 1-13, the 50% duty-cycle LO signal can be split into two time-interleaved 25% duty-cycle LO signals operating at half frequency. In the figure on the right, a frequency domain analysis is demonstrated. The sum of the harmonics of the time-interleaved 25% LO signals at half RF frequency matches the harmonics of the normal LO signal. This harmonic analysis indicates the function of time-interleaved LO signals in the frequency domain. The time-interleaved LO signals can be used to introduce an efficiency peak for 6 dB lower P_{OUT}. For example, when the normal LO signals in the SCPA are replaced with the time-

interleaved LO signals, the P_{OUT} of the SCPA reduces by 6 dB, as presented in the lower-left figure in Figure 1-13. If all the SCPA cells are operating with the time-interleaved LO signals, there is no power dissipation in the capacitor array resulting in an efficiency peak at the 6-dB PBO.

The TI technique can provide not only additional efficiency peaks but also seamless transitions such as Class-G and Doherty. The seamless efficiency can be achieved by applying the sequential switching of the SCPA cells from the fundamental LO signal to the time-interleaved LO signal, comparable to the operation of the enhanced-efficiency Class-G SCPA illustrated in Figure 1-10.

1.8 Outline of the Dissertation

This study proposes design techniques for small, highly efficient, and highly linear digital TXs that replace the conventional TXs. The proposed digital TX techniques can be employed in the overall wireless communication systems including cellular and wireless connectivity applications, such as fourth-generation long-term evolution (LTE), sub-6 GHz 5G communications, Wi-Fi, IoT, and Bluetooth.

Chapter 2 presents a watt-level quadrature digital TX with a quadrature dual-supply Class-G *IQ*-cell-shared SCPA architecture. An extensive review of the digital TX architectures based on the SCPA is provided. A detailed and thorough analysis regarding P_{OUT} and drain efficiency is demonstrated for the following conventional and proposed SCPA architectures: i) conventional polar SCPA, ii) enhanced-efficiency Class-G SCPA, iii) quadrature SCPA with dedicated *IQ* cells, iv) quadrature *IQ*-cell-shared SCPA, and v) quadrature Class-G *IQ*-cell-shared SCPA. For the circuit implementation, a merged cell switching (MCS) technique employed to achieve dual-supply Class-G operation in the quadrature *IQ*-cell-shared SCPA is described. Furthermore,

linearization techniques to compensate for amplitude and phase mismatches in Class-G operation are presented.

Chapter 3 presents a compact quadrature digital TX based on *IQ*-cell-shared SC RFDAC with linearization techniques. Nonlinearities in SC RFDAC are investigated, and three linearization techniques are proposed, which are aimed at minimizing impedance variation at the output stage and systematic nonlinearity between unary and binary cell groups in RFDAC. For the circuit implementation, on-resistance linearization techniques for the RFDAC output switches and an offset mid-tread code mapping technique are presented to minimize the output impedance variation and RFDAC error in unary/binary cell groups in the deep PBO region. Furthermore, the number of logic circuits is minimized by sharing digital circuits between the two RFDAC cells to reduce the chip area and power consumption.

Chapter 4 presents a multimode multi-efficiency-peak SCPA architecture for maximized PBO efficiency in a polar digital TX. A detailed and thorough analysis of the ideal and practical drain efficiency of the SCPA with three different efficiency-enhancement techniques is presented. Efficiency-enhancement techniques such as dual-supply Class-G, Doherty, and 2-way TI are discussed and compared. After the review and comparison of six combinations of the two different efficiency-enhancement techniques, an efficient combination of the three techniques is proposed. The discussed efficiency-enhancement techniques are as follows: i) dual-supply Class-G, ii) Doherty, iii) two-way TI, iv) Class-G-based Doherty, v) Doherty-based Class-G, vi) Class-G-based TI, vii) TI-based Class-G, viii) TI-based Doherty, ix) Doherty-based TI, and x) Class-G, Doherty, and TI. For the circuit implementation, a single-supply current-reuse Class-G switch for linear and efficient dual-supply Class-G operation is introduced. In addition, an LO-signal-

restoration technique is presented to minimize power dissipation and area for the LO signals distribution.

Chapter 5 presents the conclusion of this study.

2 WATT-LEVEL QUADRATURE CLASS-G SWITCHED-CAPACITOR POWER AMPLIFIER

Figure 2-1 presents a basic schematic of the conventional SCPA architecture. The unit capacitors in the capacitor array are selectively switched at RF for the generation RF P_{OUT}. Assuming that an ideal inductor is in series with the capacitor array, the square wave at the capacitor top plate is filtered by an ideal bandpass network. Further assuming that the filter is ideal, only a fundamental component is delivered at the output.

The equivalent circuit of the capacitor array is connected in series with an inductor L and output resistor R_{OPT} for calculating the P_{OUT} and ideal drain efficiency of the SCPA, as illustrated in Figure 2-1. The capacitor array in both polar and quadrature architectures are detailed in Figures 2-2 and 2-4. For simplicity, the numbers of capacitors switched at RF (ON) and unswitched (OFF) are depicted in a bar chart that demonstrates the operation of capacitors in the capacitor array. The vectors with different phases are illustrated as square waves with different delays at the top of the bar chart. A vector distribution from the switched to unswitched capacitors for enhanced-efficiency Class-G operation [12] is illustrated with arrows and square waves in Figures 2-2(b) and 2-4(c).

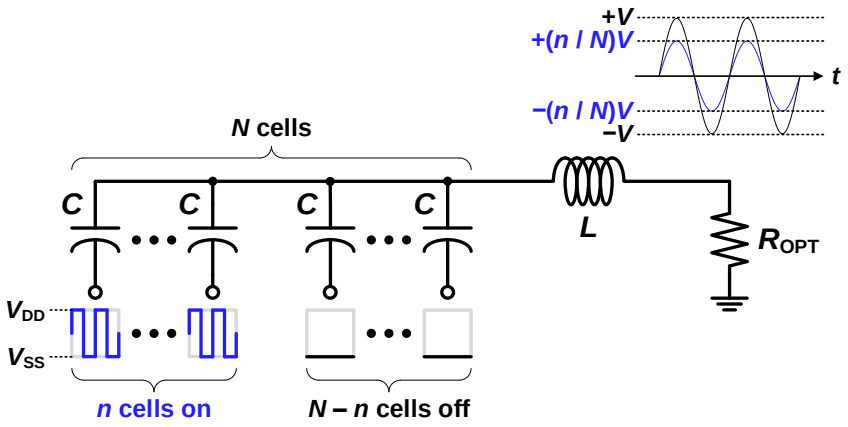


Figure 2-1. Schematic of the basic SCPA architecture.

2.1 Conventional Polar SCPA

The fundamental component of output voltage (V_{OUT}) and P_{OUT} in the conventional polar SCPA [11], as shown in Figure 2-2(a), is as follows:

$$|V_{OUT}| = \frac{2}{\pi}\frac{n}{N}V_{DD} \tag{2.1}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\frac{{V_{DD}}^2}{R_{OPT}} \tag{2.2}$$

where N, n, and R_{OPT} denote the total number of SCPA capacitors (C_{TOT}), the number of capacitors switched between V_{DD} and V_{SS}, and the output resistance [11] for the desired peak P_{OUT}, respectively. Term $2/\pi$ denotes the Fourier coefficient for the fundamental frequency of the square wave.

Assuming very fast switching operation, the dynamic power dissipation of the SCPA in the capacitor array (P_{SC}) is determined as follows:

$$P_{SC} = C_{IN}{V_{DD}}^2 f = \frac{n(N-n)}{N^2}C_{TOT}{V_{DD}}^2 f \tag{2.3}$$

where C_{IN} denotes the series capacitance of the selected n and unselected $N - n$ capacitors, as illustrated in Figure 2-2(a). The ideal drain efficiency of the SCPA is determined as follows:

$$\eta_{IDEAL} = \frac{P_{OUT}}{P_{OUT} + P_{SC}}. \tag{2.4}$$

Substitution of (2.2) and (2.3) into (2.4) yields the drain efficiency, as illustrated in Figure 2-3(a) in 2-D *IQ* domain and in 1-D as depicted in Path A.

A loaded quality factor (Q_{LOAD}) of three for the output matching network is used for the efficiency calculation [11] throughout this chapter. The Q_{LOAD} is defined as follows:

$$Q_{\mathrm{LOAD}} = \frac{2\pi f L}{R_{\mathrm{OPT}}} = \frac{1}{2\pi f C_{\mathrm{TOT}} R_{\mathrm{OPT}}}. \tag{2.5}$$

For higher drain efficiency, a high Q_{LOAD} is preferred because P_{SC} is proportional to C_{TOT} which is the capacitance of the output matching network.

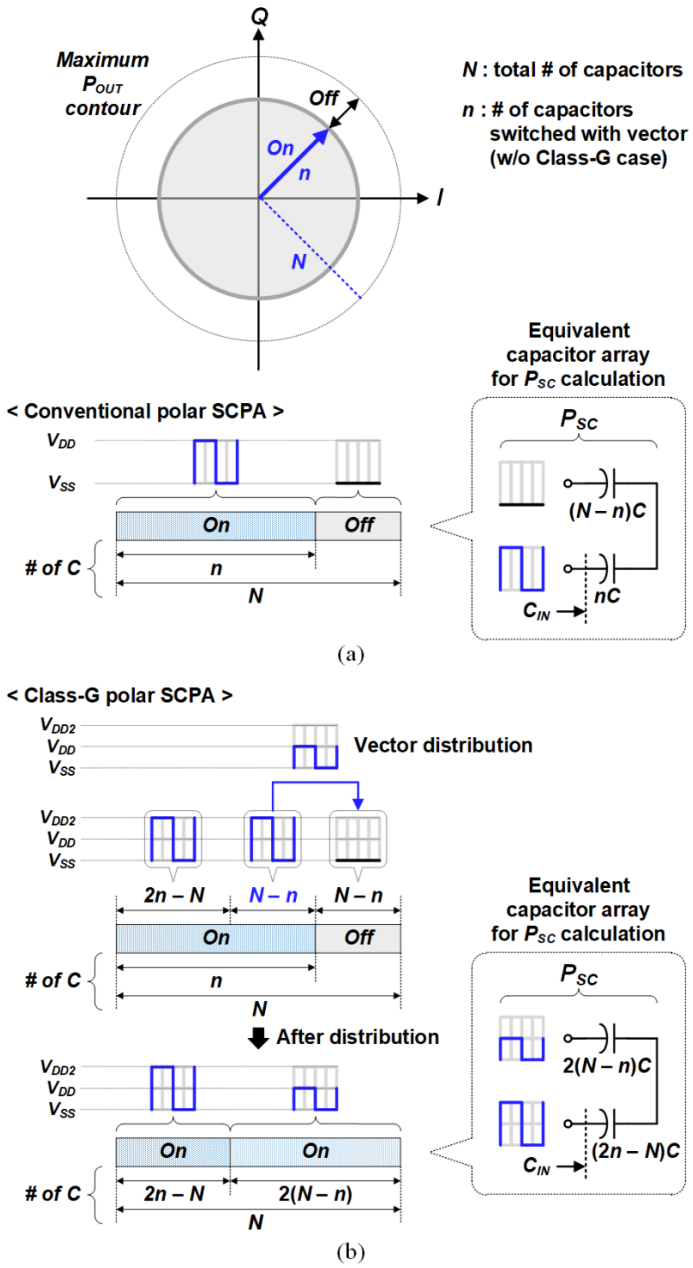


Figure 2-2. SCPA operation in the polar TX. (a) Conventional SCPA and (b) Class-G SCPA with the dual-supply voltage.

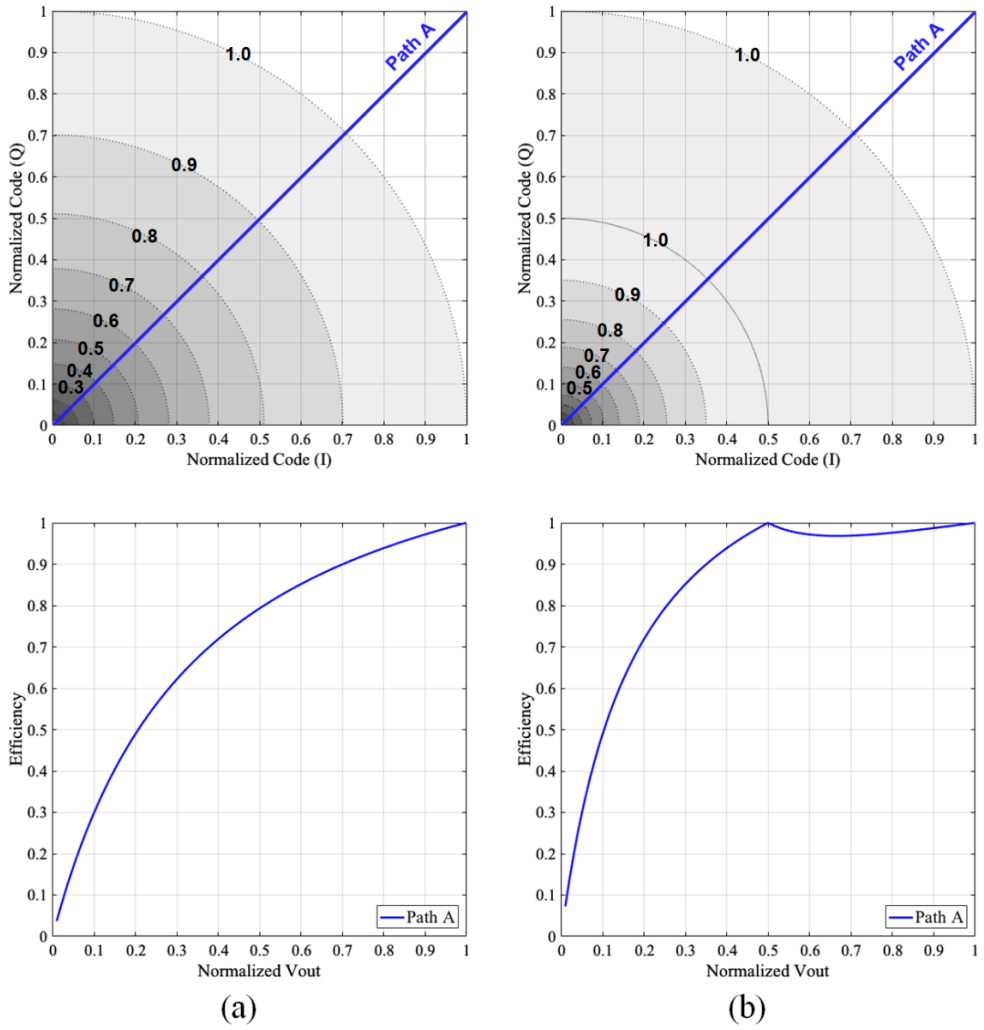


Figure 2-3. Theoretical 2-D drain efficiency map for quadrant 1 when Q_{LOAD} is 3. (a) Conventional polar SCPA. (b) Class-G polar SCPA.

2.2 Enhanced-Efficiency Class-G SCPA

The drain efficiency of a Class-G SCPA using a dual-supply voltage, V_{DD2} and V_{DD}, is detailed in [12] [Figure 2-2(b)]. Ideally, V_{DD2} is double V_{DD}. The total number of capacitors and input codes are defined as N and M, respectively, where $M = 2N$. The number of selected cells is n, where $0 \leq n \leq N$ and the selected code is m, where $0 \leq m \leq M$. In the case of $m \leq N$, V_{OUT}, P_{OUT}, and ideal drain efficiency can be expressed in a similar manner to the conventional SCPA (2.1)–(2.4) because the operation of both SCPAs is similar.

When $m > N$, V_{OUT} and P_{OUT} are determined using the following expressions:

$$|V_{OUT}| = \frac{2}{\pi}\left[\left(\frac{n}{N}\right)V_{DD2} + \left(\frac{N-n}{N}\right)V_{DD}\right] \tag{2.6}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left(\frac{N+n}{N}V_{DD}\right)^2\frac{1}{R_{OPT}}. \tag{2.7}$$

The dynamic power dissipation of the Class-G SCPA is as follows:

$$P_{SC} = C_{IN}(V_{DD2} - V_{DD})^2 f = C_{IN}{V_{DD}}^2 f. \tag{2.8}$$

The ideal drain efficiency calculated from (2.4), (2.7), and (2.8) is shown in Figure 2-3(b).

2.3 Quadrature SCPA With Dedicated I/Q Cells

The conventional quadrature SCPA has two sub-SCPAs for *I* and *Q* signals, as illustrated in Figure 1-6(b). The total number of capacitors is *N*, and each sub-SCPA for the dedicated *I* and *Q* has half of the array, as illustrated in Figure 2-4(a). Because the *I* and *Q* signals are orthogonal, the amplitude of the V_{OUT} and P_{OUT} can be determined as follows:

$$|V_{OUT}| = \frac{2}{\pi}\sqrt{\left(\frac{i}{N}\right)^2 + \left(\frac{q}{N}\right)^2}V_{DD} \tag{2.9}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left[\left(\frac{i}{N}\right)^2 + \left(\frac{q}{N}\right)^2\right]\frac{{V_{DD}}^2}{R_{OPT}} \tag{2.10}$$

where $0 \le i \le 0.5N$ and $0 \le q \le 0.5N$ denote the number of capacitors switched between V_{DD} and V_{SS} for the *I* and *Q* SCPAs, respectively.

In the quadrature SCPA, the total dynamic power dissipation can be expressed as the sum of each dynamic power because the two independent quadrature signals operate with a different charge and discharge timing for their capacitors as follows:

$$P_{SC} = P_{SC\_I} + P_{SC\_Q} \tag{2.11}$$

$$P_{\mathrm{SC\_I}} = \frac{i(N-i)}{N^2} C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f \tag{2.12}$$

$$P_{\mathrm{SC\_Q}} = \frac{q(N-q)}{N^2} C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f. \tag{2.13}$$

Therefore, the ideal drain efficiency is obtained from (2.4) and (2.10)–(2.13) and is illustrated in Figure 2-5(a).

2.4 Quadrature IQ-Cell-Shared SCPA

As illustrated in Figure 2-4(b), the quadrature *IQ*-cell-shared SCPA uses two orthogonal vectors as in the conventional quadrature SCPA. Therefore, the V_{OUT} and P_{OUT} can be obtained in a similar manner to the conventional quadrature SCPA as follows:

$$|V_{\mathrm{OUT}}| = \frac{2}{\pi} \sqrt{\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2}\, V_{\mathrm{DD}} \tag{2.14}$$

$$P_{\mathrm{OUT}} = \frac{1}{2} \frac{|V_{\mathrm{OUT}}|^2}{R_{\mathrm{OPT}}} = \frac{2}{\pi^2} \left[\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2\right] \frac{{V_{\mathrm{DD}}}^2}{R_{\mathrm{OPT}}} \tag{2.15}$$

where a and b denote the number of capacitors switched between V_{DD} and V_{SS}, representing vectors A and B, respectively. In this architecture, the relationship among a, b, and N can be expressed as $0 \leq a + b \leq N$ because a and b can be flexibly allocated within the total number of capacitors N, as illustrated in Figure 2-4(b).

The dynamic power dissipation can also be calculated using a similar method to the conventional quadrature SCPA as follows:

$$P_{\mathrm{SC}} = P_{\mathrm{SC\_A}} + P_{\mathrm{SC\_B}} \tag{2.16}$$

$$P_{\mathrm{SC\_A}} = \frac{a(N-a)}{N^2} C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f \tag{2.17}$$

$$P_{\mathrm{SC\_B}} = \frac{b(N-b)}{N^2} C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f. \tag{2.18}$$

The ideal drain efficiency can therefore be obtained from (2.4) and (2.15)–(2.18). Although the equations seem to be similar to that of the quadrature SCPA with fixed *I* /*Q* cells, the *IQ*-combined unit vectors with flexible vector allocation result in a different efficiency map, as illustrated in Figure 2-5(b). With no dedicated, half-sized *I* /*Q* cells, it exhibits an increased V_{OUT} (P_{OUT}) and better efficiency in the PBO region.

2.5 Quadrature Class-G IQ-Cell-Shared SCPA

Figure 2-4(c) shows the Class-G operation in a quadrature *IQ*-cell-shared SCPA. Unlike polar SCPA and conventional quadrature SCPA with dedicated *I* /*Q* cells, the input digital code to *IQ*-shared cells has not only amplitude but also phase information. Consequently, the Class-G technique introduced in [12] for a polar SCPA and in [23] for a conventional quadrature SCPA that processes only amplitude information cannot be directly applied to the quadrature *IQ*-cell-shared architecture.

For the enhanced-efficiency Class-G operation with an efficiency peak at 6-dB PBO in the efficiency contour in the quadrature *IQ*-cell-shared architecture, the output vectors with an amplitude of V_{DD2} in the SCPA cell are distributed to the turned-off cells, as depicted in Figure 2-4(c). The number of turned-on cells for vectors *A* and *B* with an amplitude of V_{DD2} is defined as *a* and *b*, respectively, and turned-off cells are defined as *k*. The range of *k* is chosen as less than half of the total number of cells, *N*, for the Class-G operation within 0–6-dB PBO region. *k* is divided into two groups α and β that receives the distributed vectors *A* and *B* with an amplitude of V_{DD}, respectively, where $0 \le \alpha \le a$, $0 \le \beta \le b$, and $\alpha + \beta = k$. After vector distribution, the amplitude of the vectors *A* and *B* are $(a - \alpha)V_{DD2} + 2\alpha V_{DD}$ and $(b - \beta)V_{DD2} + 2\beta V_{DD}$, respectively, as illustrated in Figure 2-4(c). The V_{OUT} and P_{OUT} of the quadrature Class-G *IQ*-cell-shared SCPA can be obtained by replacing V_{DD} with V_{DD2} in (2.14) and (2.15) for the quadrature *IQ*-cell-shared SCPA

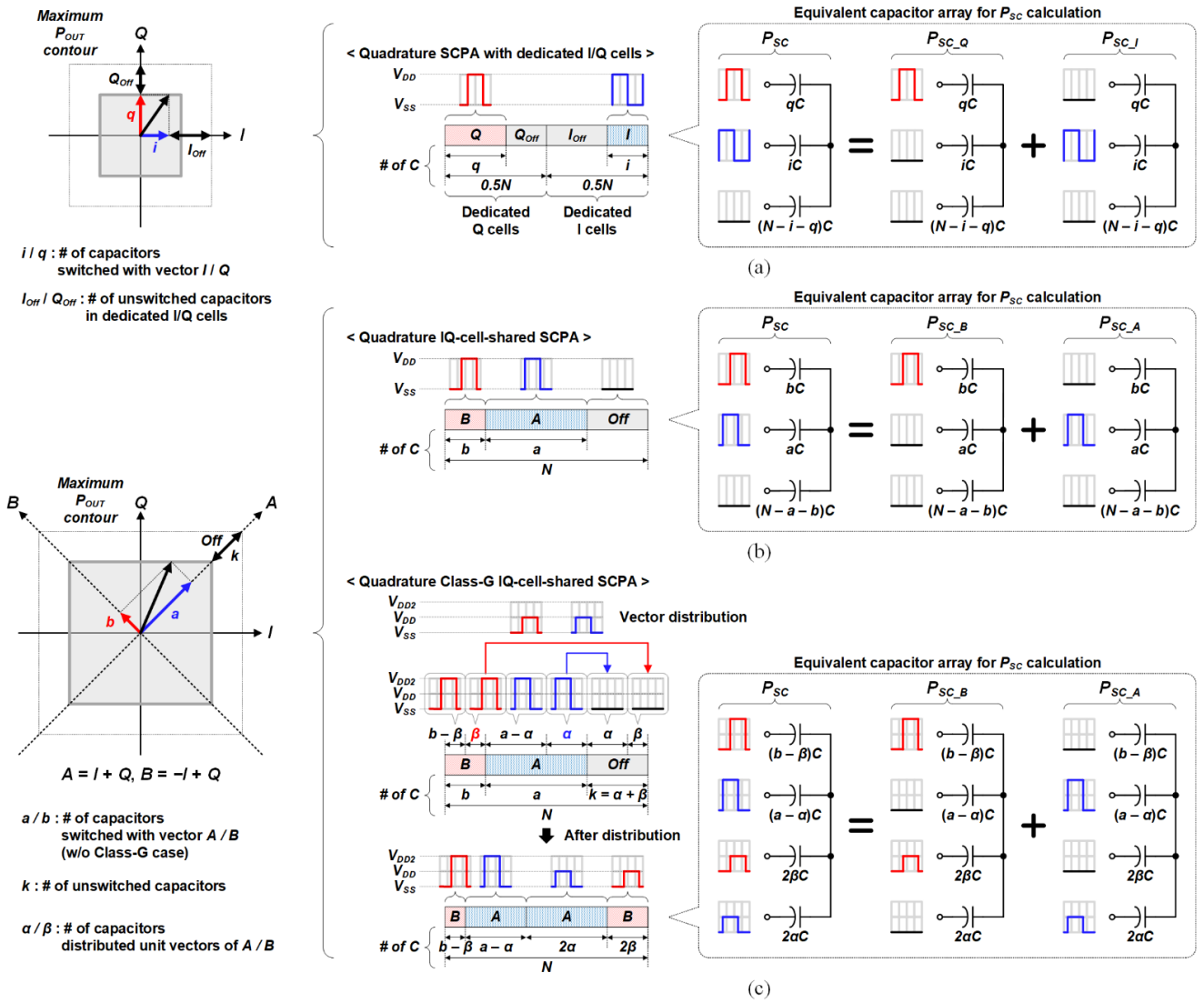


Figure 2-4. SCPA operation in quadrature transmitter. (a) SCPA with dedicated *I* /*Q* cells, (b) *IQ*-cell-shared SCPA, and (c) Class-G *IQ*-cell-shared SCPA.

$$|V_{\mathrm{OUT}}| = \frac{2}{\pi}\sqrt{\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2}\, V_{\mathrm{DD2}} \tag{2.19}$$

$$P_{\mathrm{OUT}} = \frac{2}{\pi^2}\left[\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2\right]\frac{{V_{\mathrm{DD2}}}^2}{R_{\mathrm{OPT}}}. \tag{2.20}$$

In the region deeper than the 6-dB PBO, the operation is similar to the quadrature *IQ*-cell-shared SCPA without Class-G (Chapter 2.4), because all the vectors with an amplitude of V_{DD2} have been distributed and only the vectors with an amplitude of V_{DD} remain. The ideal drain efficiency can be obtained from similar equations.

For calculating the ideal drain efficiency in the 0–6-dB PBO region, the dynamic power dissipation of the Class-G operating cells for the vectors *A* and *B* needs to be analyzed. In Figure 2-4(c), the equivalent capacitor arrays of the SCPA and their input voltages are demonstrated to calculate the dynamic power dissipation. Unlike other architectures discussed, thus far, in Chapter 2, the dynamic power dissipation cannot be derived directly with C_{IN} because the capacitor network has three ports with different potentials. Thus, the dynamic power dissipation for each capacitor switched between V_{DD2} and V_{SS}, V_{DD} and V_{SS}, and unswitched capacitors can be calculated separately as follows:

$$P_{\mathrm{SC\_A}} = P_{\mathrm{SC\_A1}} + P_{\mathrm{SC\_A2}} + P_{\mathrm{SC\_A3}} \tag{2.21}$$

$$P_{\mathrm{SC\_B}} = P_{\mathrm{SC\_B1}} + P_{\mathrm{SC\_B2}} + P_{\mathrm{SC\_B3}} \tag{2.22}$$

where $P_{\mathrm{SC\_A1}}$($P_{\mathrm{SC\_B1}}$), $P_{\mathrm{SC\_A2}}$($P_{\mathrm{SC\_B2}}$), and $P_{\mathrm{SC\_A3}}$($P_{\mathrm{SC\_B3}}$) denote the powers dissipated to charge/discharge the capacitors switched between V_{DD2} and V_{SS}, V_{DD} and V_{SS}, and unswitched capacitors, respectively.

The total dynamic power dissipation is determined as follows:

$$P_{\mathrm{SC}} = P_{\mathrm{SC\_A}} + P_{\mathrm{SC\_B}} \tag{2.23}$$

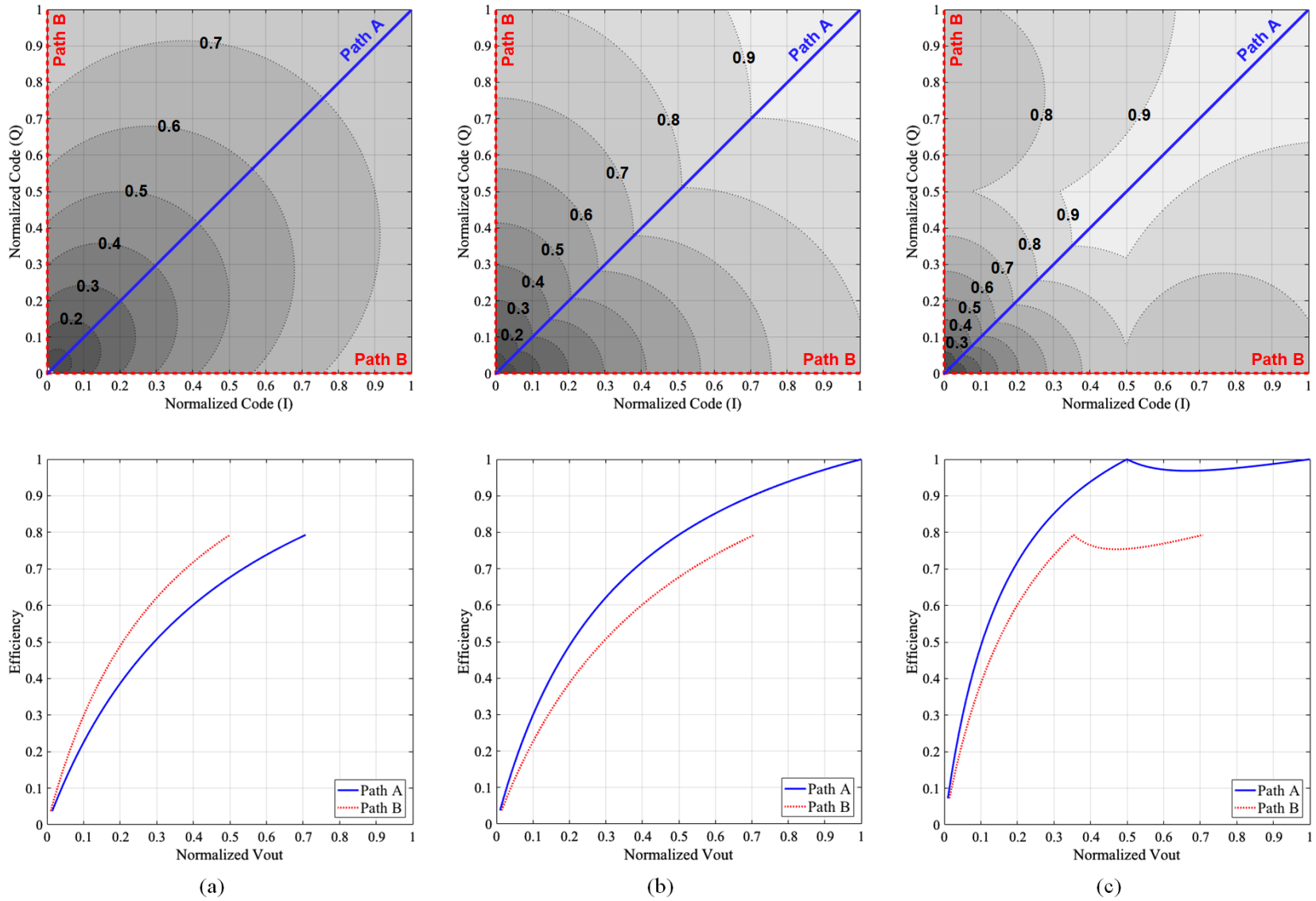


Figure 2-5. Theoretical 2-D drain efficiency map for quadrant 1 when Q_{LOAD} is 3. (a) Conventional quadrature SCPA. (b) Quadrature *IQ*-cell-shared SCPA. (c) Quadrature Class-G *IQ*-cell-shared SCPA.

$$P_{\mathrm{SC\_A}} = \left[\frac{4(a-\alpha)}{N}\left(\frac{N-a}{N}\right)^2 + \frac{2\alpha}{N}\left(\frac{N-2a}{N}\right)^2 + \frac{b+\beta}{N}\left(\frac{2a}{N}\right)^2\right] C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f \quad (2.24)$$

$$P_{\mathrm{SC\_B}} = \left[\frac{4(b-\beta)}{N}\left(\frac{N-b}{N}\right)^2 + \frac{2\beta}{N}\left(\frac{N-2b}{N}\right)^2 + \frac{a+\alpha}{N}\left(\frac{2b}{N}\right)^2\right] C_{\mathrm{TOT}} {V_{\mathrm{DD}}}^2 f \quad (2.25)$$

where $0 \le \alpha \le a$, $0 \le \beta \le b$, and $N = a + b + \alpha + \beta$. The ideal drain efficiency is obtained from (2.4) and (2.20)–(2.25), as illustrated in Figure 2-5(c).

2.6 Merged Cell Switching Technique

In contrast to the conventional dual-supply Class-G SCPAs that process 1-D amplitude information in a polar architecture or a quadrature architecture with dedicated *I* /*Q* cells, the Class-G technique cannot be directly applied to the *IQ*-cell-shared architecture because various vectors with different amplitudes and phases require processing in a single SCPA cell. The operation theory is detailed in this Chapter 2.6. The high average drain efficiency is achieved with an additional efficiency peak associated with the Class-G operation. Furthermore, power dissipation in the digital logic circuits operating at RF such as the digital mixer, level shifter, and control blocks can be reduced by half, leading to an improved system efficiency (SE) as well.

2.6.1 Proposed Merged SCPA Cell

To achieve a reduced chip area and an enhanced drain efficiency associated with the efficiency Class-G operation in quadrature architecture, four conventional quadrature SCPA cells, presented in Figure 2-6(a), are merged into two cells by adopting the *IQ*-cell-shared architecture [25], as illustrated in Figure 2-6(b); thereafter, the two cells are further merged into a single cell that operates with a dual-supply voltage, as illustrated in Figure 2-6(c), and discussed in this section. After the merger, a Class-G operation is performed using the merged cell switching (MCS) technique described in Chapter 2.6.2.

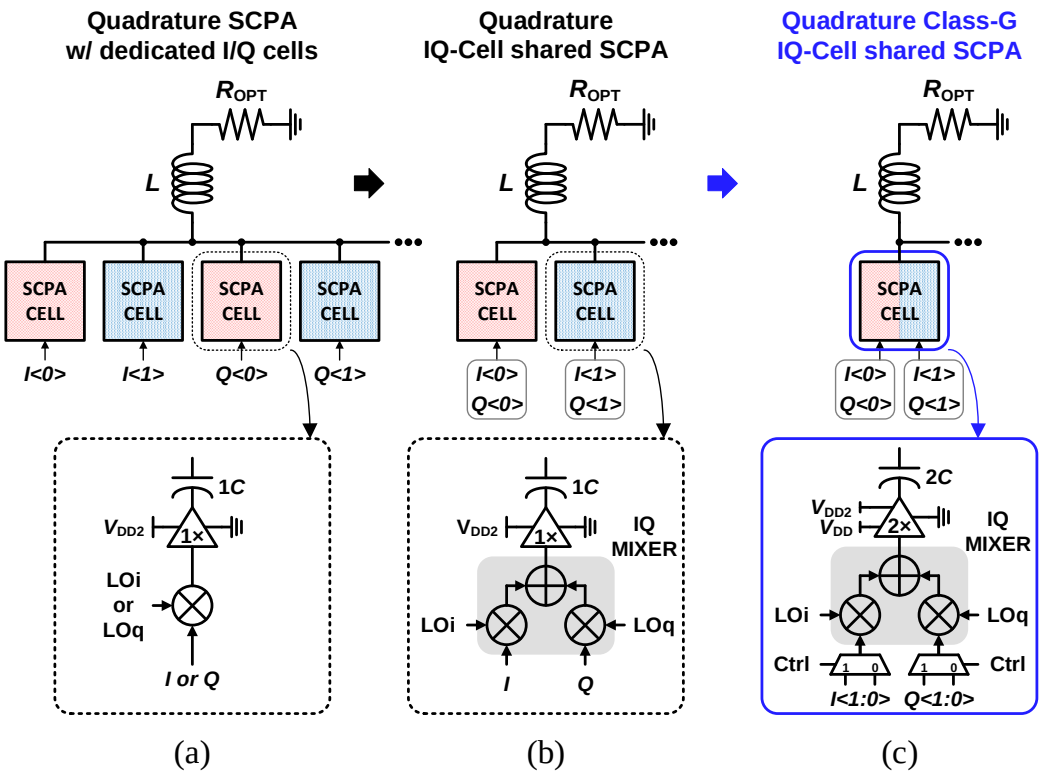


Figure 2-6. Quadrature SCPA cells with two thermometer codes. (a) Four cells of quadrature SCPA with dedicated *I*/*Q* cells, (b) two cells of quadrature *IQ*-cell-shared SCPA, and (c) one merged cell for quadrature dual-supply Class-G *IQ*-cell-shared SCPA.

The merged cell for the Class-G operation presented in Figure 2-6(c) processes two input *IQ* data sets, [*I* <0>, *Q*<0>] and [*I* <1>, *Q*<1>]. Because each SCPA cell has just one digital mixer that processes a single *IQ*-combined unit vector, it cannot process the two *IQ* data sets simultaneously. Accordingly, multiplexers select only one *IQ* data set out of the two using a selection signal from the control logic in each SCPA cell. The basic operation of the merged cell is as follows:

1) If the two *IQ* data sets are the same, the output switch delivers the signal with an amplitude of V_{DD2} regardless of the multiplexer selection signal.
2) If the two *IQ* data sets that the multiplexers receive are different, the multiplexers select one or the other, based on the code selection scheme discussed in Chapter 2.6.2.

3) If the two *IQ* data sets of the SCPA cell are deactivated, the switch is not switched and connected to signal ground.

2.6.2 Merged Cell Switching Operation

The MCS technique, comprised the vector amplitude switching (VAS) and vector phase switching (VPS) techniques as illustrated in Figure 2-7, is implemented on chip along with other digital control logic gates. The MCS technique enables an enhanced-efficiency Class-G operation in the quadrature *IQ*-cell-shared SCPA architecture. The VAS enables the vector distribution introduced in Chapter 2.5, and the VPS conserves the amplitude and phase information when the cells are merged.

First, the SCPA cell is turned off by the 180° out-of-phase (OOP) data removal operation [25] in the *IQ*-shared cells. The pairs of *IQ* data sets that are deactivated are as follows: [1, 0], [0, 1] or [1, 1], [0, 0]. Examples of the 180° OOP operation are presented in the pairs of gray dashed rectangles in Figure 2-7.

The VAS operation is described in Figure 2-7(a). If the two input *IQ* data sets of the SCPA cell are the same and their VAS paired cell is turned off, the VAS operation splits a vector with an amplitude of V_{DD2} into two smaller vectors with an amplitude of V_{DD}, distributing half of the vector from the fully turned-on (V_{DD2}) cell to the paired turned-off (OFF) cell. This operation maintains the same output voltage at the top plate of the capacitors after the vector distribution.

The VPS operation is presented in Figure 2-7(b). It maintains the vector information when one of the SCPA cells has two different input *IQ* data sets. Each SCPA cell can process only one *IQ* data set because it has only one *IQ* mixer, and the unselected data require compensation. The unselected data are transferred to the cell with an auxiliary (AUX) input that processes the extra

IQ data set. The AUX input is controlled by the digital phase comparator that detects the difference between the two *IQ* data sets. If the two data sets to an SCPA cell are different, the AUX input is activated to compensate for the unselected data.

The detailed SCPA operation with both VAS and VPS is directly related to the merged SCPA cell described in Chapter 2.6.1 and is as follows:

1) If the two input *IQ* data sets are the same, the SCPA cell outputs a square-wave signal of amplitude V_{DD2} modulated with the *IQ* data set. Otherwise, it distributes one of the two data sets to the VAS-paired cell that is OFF. In this case, both operate with V_{DD} for better drain efficiency.
2) If one of the two input *IQ* data sets is canceled by the 180° OOP data removal, the SCPA cell delivers a signal of amplitude V_{DD} modulated with the remaining *IQ* data set.
3) If both *IQ* data sets are deactivated by the 180° OOP data removal operation, the SCPA cell remains OFF and connected to a signal ground because there is no *IQ* data set to be distributed from the paired cell in the deep PBO region. In the case of 0–6-dB PBO, the SCPA cell outputs the distributed signal with an amplitude of V_{DD} from its VAS-paired cell.
4) If the two *IQ* data sets are not the same, only one of them is selected in the SCPA cell to generate a modulated signal of amplitude V_{DD}, and the unselected *IQ* data set is distributed to the cell with the AUX input through the VPS operation.

The VAS operation is performed between the VAS paired SCPA cells as illustrated in Figure 2-8. Figure 2-9 shows a comparison of the SCPA operations between the without VAS and with VAS cases. For the former case, when the P_{OUT} of the SCPA is shrinking, the cells are turned off two by two and the output capacitors of the turned-off cells become a capacitive loading for the

operating cells. Meanwhile, for the latter case, from 0 to 6-dB PBO, the cells in groups 2 and 3 provide vector information to groups 4 and 1, respectively. After finishing the amplitude vector distribution, all cells operate in V_{DD} mode. In this case, ideally, there is no capacitive loading between the SCPA cells, resulting in an efficiency peak at 6-dB PBO. From 6-dB to the deepest PBO, the SCPA cells are turned off two by two, which is the same operation to the without VAS case.

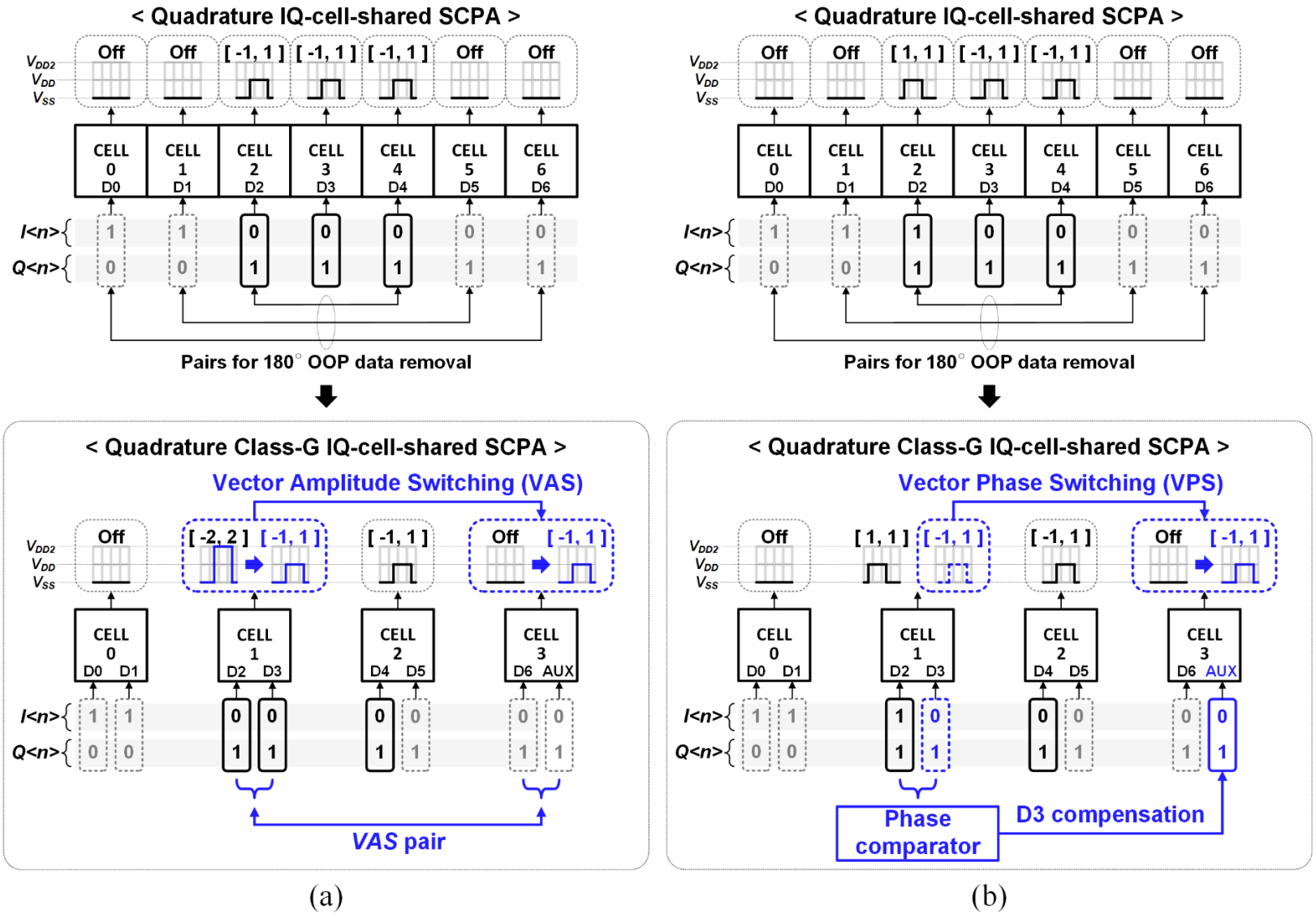
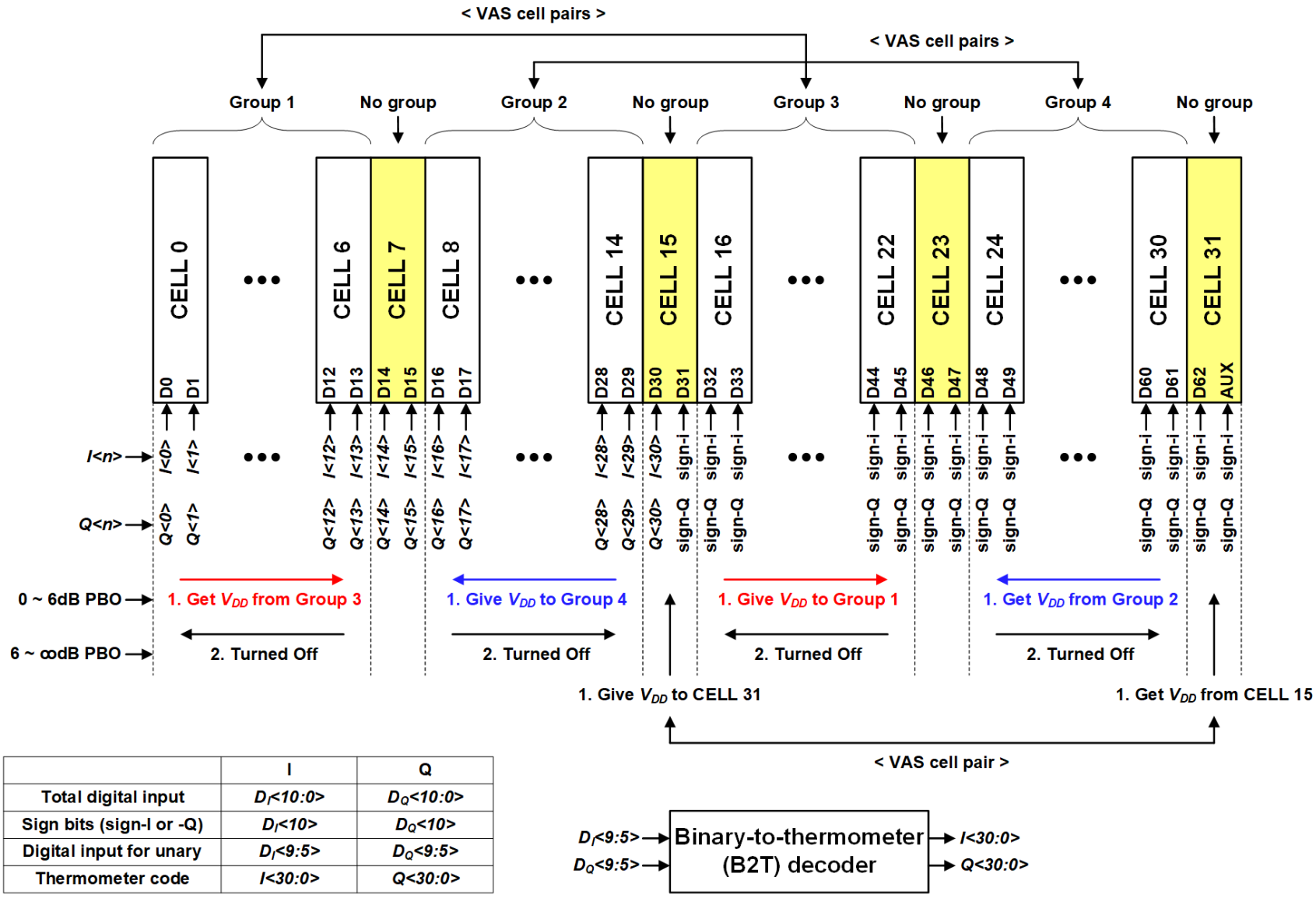


Figure 2-7. Operation of the MCS technique. (a) VAS and (b) VPS.



	I	Q
Total digital input	D_I<10:0>	D_Q<10:0>
Sign bits (sign-I or -Q)	D_I<10>	D_Q<10>
Digital input for unary	D_I<9:5>	D_Q<9:5>
Thermometer code	I<30:0>	Q<30:0>

Figure 2-8. Implemented VAS pairs for 6b unary cells.

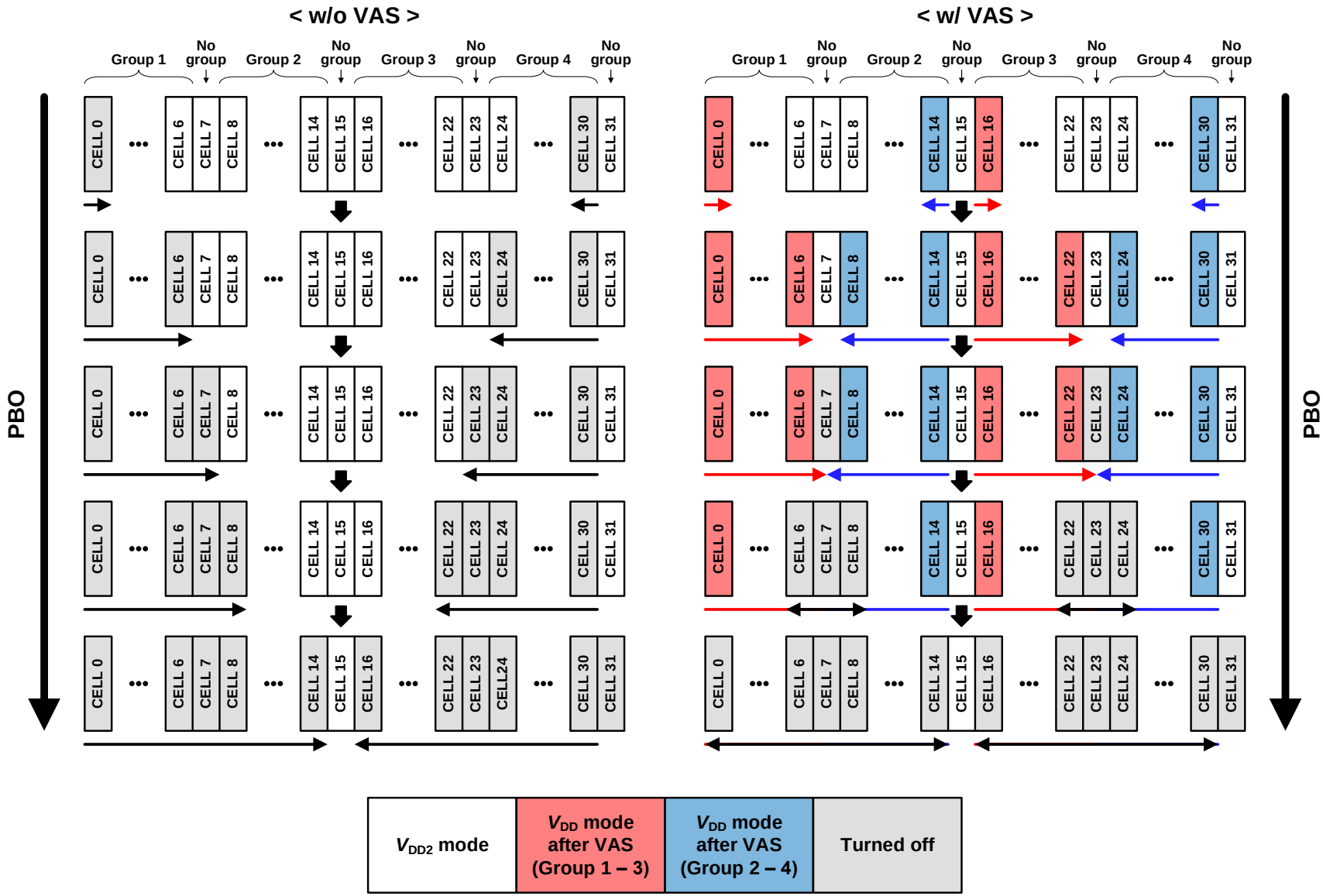


Figure 2-9. SCPA operation without VAS and with VAS.

2.7 Linearization Techniques for Class-G SCPA

As discussed in Chapter 2.2, the enhanced-efficiency Class-G SCPA has a significant advantage in improving the drain efficiency. Class-G with multiple supply voltages in SCPA is more linear than in the conventional Class-G PAs because the abrupt switching produces glitches. The power-domain change is very smoothly and seamlessly made in SCPA because: 1) the voltage domain changes when the switches are disabled and is not connected to any supply voltage and 2) the voltage does not change abruptly for the entire PA, but rather changes in a continuous manner while using both supply voltages simultaneously for enhanced efficiency and linearity. However, the multiple supply voltages still result in signal distortion owing to the mismatches in the supply voltages and different signal paths, necessitating compensation with predistortion. The linearization techniques for the amplitude and phase discussed in this section improve the linearity and minimize the requirement of DPD.

2.7.1 Supply Voltage Mismatch Insensitive Class-G SCPA

Figure 2-10 presents a conventional switch for a dual-supply Class-G SCPA [12] and the proposed switch that is insensitive to the supply voltage mismatch. In Figure 2-10, the matching network for the output stage is not provided. The Class-G switches employ the two different voltages, V_{DD2} and V_{DD}, to generate an output voltage for large/small output power. In the conventional switch in Figure 2-10(a), V_{DD2} should be equal to $2 \times V_{DD}$ to generate an accurate output voltage. However, the value of V_{DD} is not always one half of V_{DD2} and can differ owing to process (P), voltage (V) and temperature (T) (PVT) variation. Any mismatch generates nonlinearity and should be corrected with DPD. Even after DPD, it is still susceptible to any dynamic change if there are uncorrelated changes or glitches in both voltages during actual

operation. The amplitude of the distorted output voltage in the V_{DD} mode for low power, shown in Figure 2-10(a), can be expressed as follows:

$$|V_{OUT}| = V_{DD} + \Delta V - V_{SS} \tag{2.26}$$

where ΔV denotes the mismatch between the two supply voltages.

The proposed switch for Class-G SCPA depicted in Figure 2-10(b), however, is very robust to any supply voltage mismatch. It uses the average of $V_{DD2} - V_{DD}$ and $V_{DD} - V_{SS}$ to generate $V_{DD2}/2$ instead of V_{DD} in the low power mode (V_{DD} mode). It splits a conventional Class-G switch cell into two half-sized cells that operate between $V_{DD} - V_{SS}$ and $V_{DD2} - V_{DD}$, and shares the outputs at the capacitor top plates through capacitor combining using a half-sized capacitor (C_S). The mismatch voltage can be canceled out at the summing node at the top plate of the capacitors. The amplitude of the linearized output voltage in the V_{DD} mode can be expressed as follows:

$$\begin{aligned} |V_{OUT}| &= \frac{(V_{DD2} - V_{DD} - \Delta V) + (V_{DD} + \Delta V - V_{SS})}{2} \\ &= \frac{V_{DD2} - V_{SS}}{2} = V_{DD} - V_{SS}. \end{aligned} \tag{2.27}$$

The reduction of the dynamic power consumption in the output switches and switch drivers is essential in improving the efficiency of the SCPA. The dynamic power is dissipated to charge and discharge the capacitor array and parasitic capacitance at the transistor switch itself. The power consumption to charge/discharge the capacitor array can be reduced by using the Class-G technique or using small capacitors as discussed in Chapters 2.1–5. However, owing to the additional transistors for the Class-G operation, the drain efficiency improvement can be compromised, especially in the deep PBO region. To maximize efficiency improvement, an area and power-efficient switch is proposed for the Class-G SCPA, as illustrated in Figure 2-11.

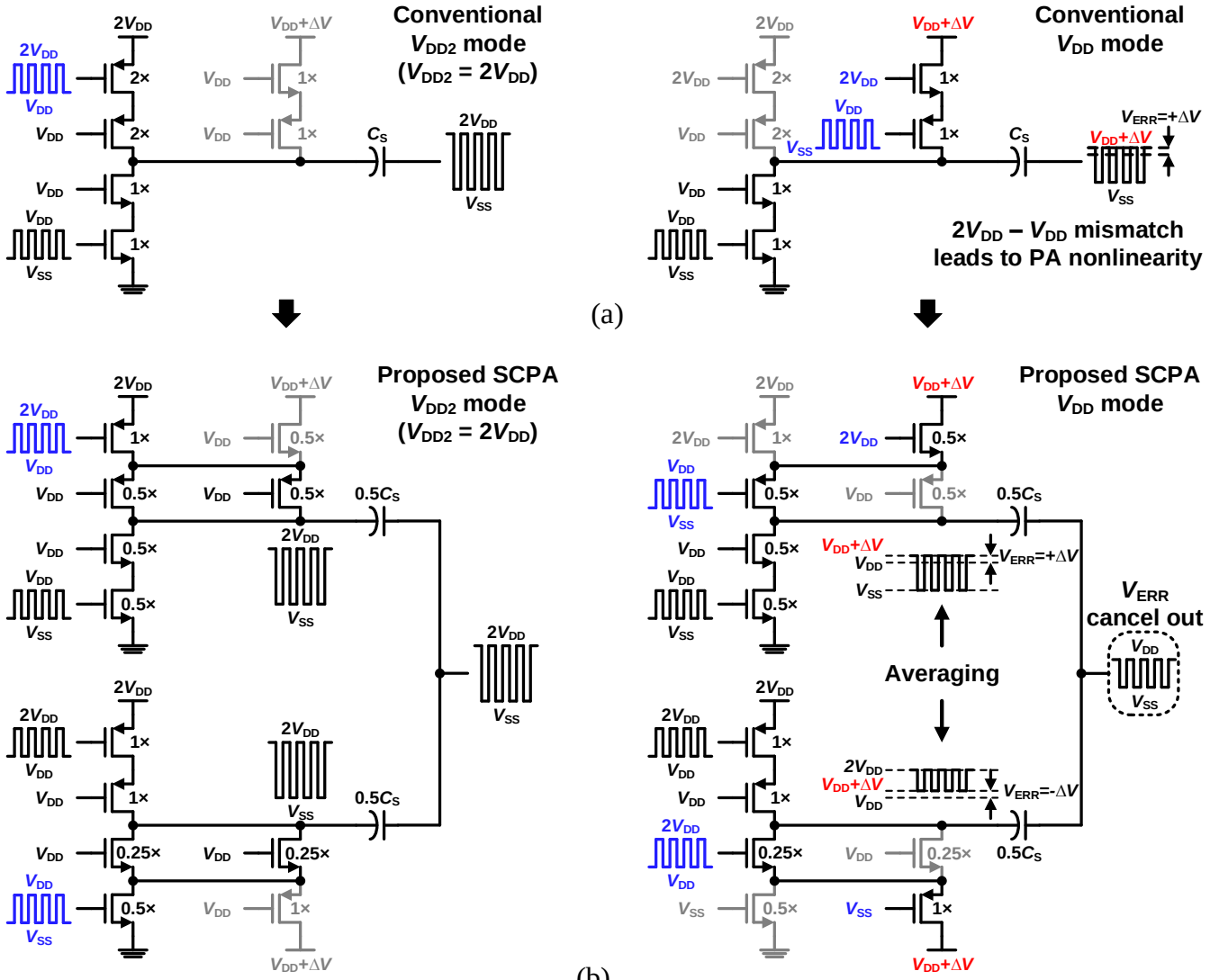


Figure 2-10. Switch cells for Class-G dual-supply voltage SCPA. (a) conventional switch and (b) proposed switch cell for amplitude mismatch compensation.

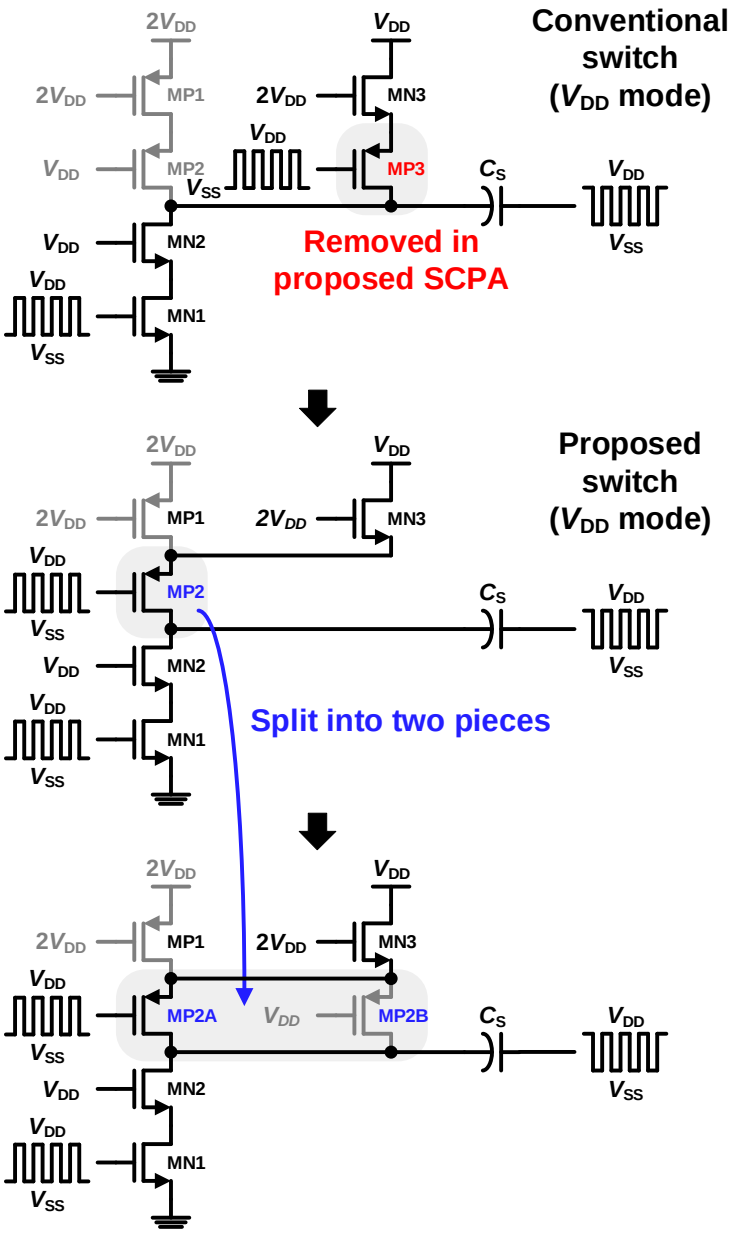


Figure 2-11. Area- and power-efficient Class-G SCPA switch.

For a simplified explanation, we describe the proposed switch without the supply-voltage-insensitive switch structure, but it is applied to both split switches as illustrated in Figure 2-10. For the low power mode in the conventional switch for the Class-G operation, MP3 switches at carrier frequency while MN3 is ON to provide V_{DD} to the switching network. The proposed switch architecture removes MP3 from the conventional switch and reuses an existing cascode transistor,

MP2, as a switching device in V_{DD} mode to reduce the parasitic capacitance at the switch output. Furthermore, if the ON-resistance of MN3 is small, only a part of MP2 requires switching when it operates from V_{DD} to save the dynamic power consumption in the buffer chain driving MP2. In this design, only half of the MP2 is used for the MP2A that switches in the V_{DD} mode. The gate of the remaining transistor, MP2B, is biased at V_{DD} and is turned off in the V_{DD} mode.

2.7.2 Delay Mismatch Compensation Scheme for Class-G SCPA

Although there is no amplitude mismatch between V_{DD2} and V_{DD} modes when V_{DD2} and V_{DD} are ideally matched, a delay mismatch can exist because the proposed SCPA operates with two different supply voltages. The delay mismatch in the two different signal paths will directly result in a phase mismatch. Notably, any difference in buffer size for driving NMOS/PMOS switches of different sizes will make a difference in the switching time. Additionally, the parasitic capacitance cannot be exactly matched with a different fan out. Furthermore, the supply voltage difference can result in an even larger variation in signal delay due to different switching times. An ideal switch can be the best solution for eliminating the phase mismatch. However, an efficient compensation technique for the delay (phase) mismatch is required with finite switch performance. It is more significant at a higher frequency because the same delay mismatch results in a larger phase mismatch at the higher operating frequency. In this design, a dynamic path delay control scheme is proposed to compensate for the non-ideal switching performance of the transistor switch, as illustrated in Figure 2-12. A path-dependent adjustable delay is introduced to match the delay in both V_{DD2} and V_{DD} modes. The proposed delay control technique minimizes the mismatch by aligning the output signals from different supply voltages. The signal path is dynamically changing according to the two Class-G operation modes, and each of the paths has its own delay cell to control the delay independently.

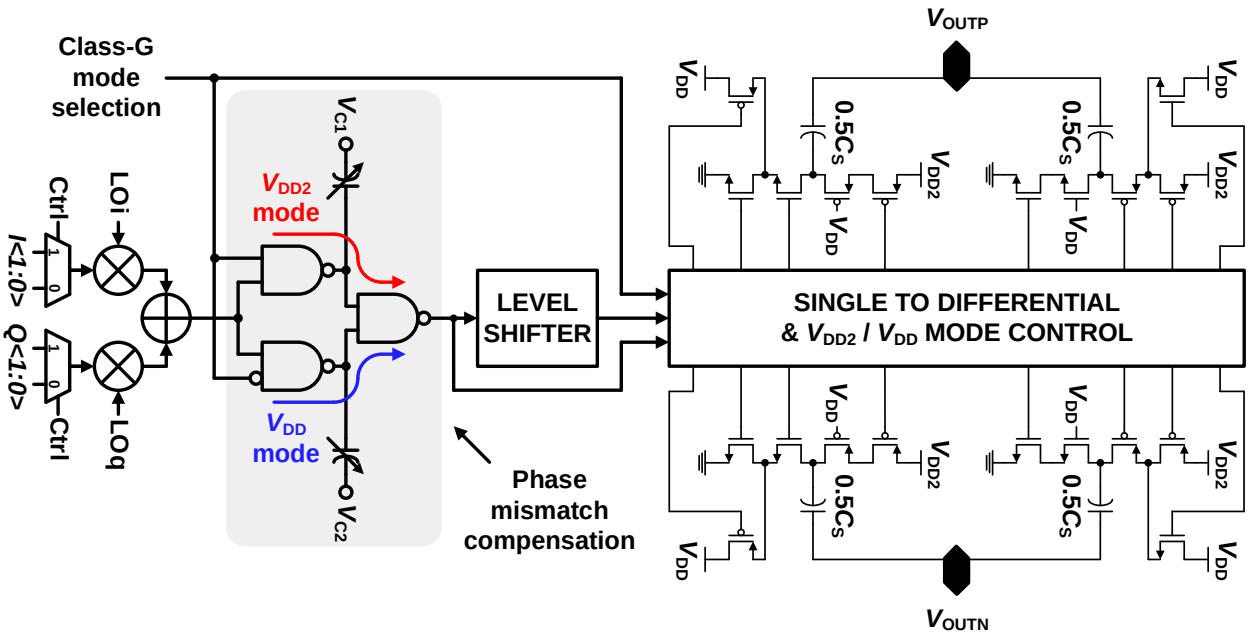
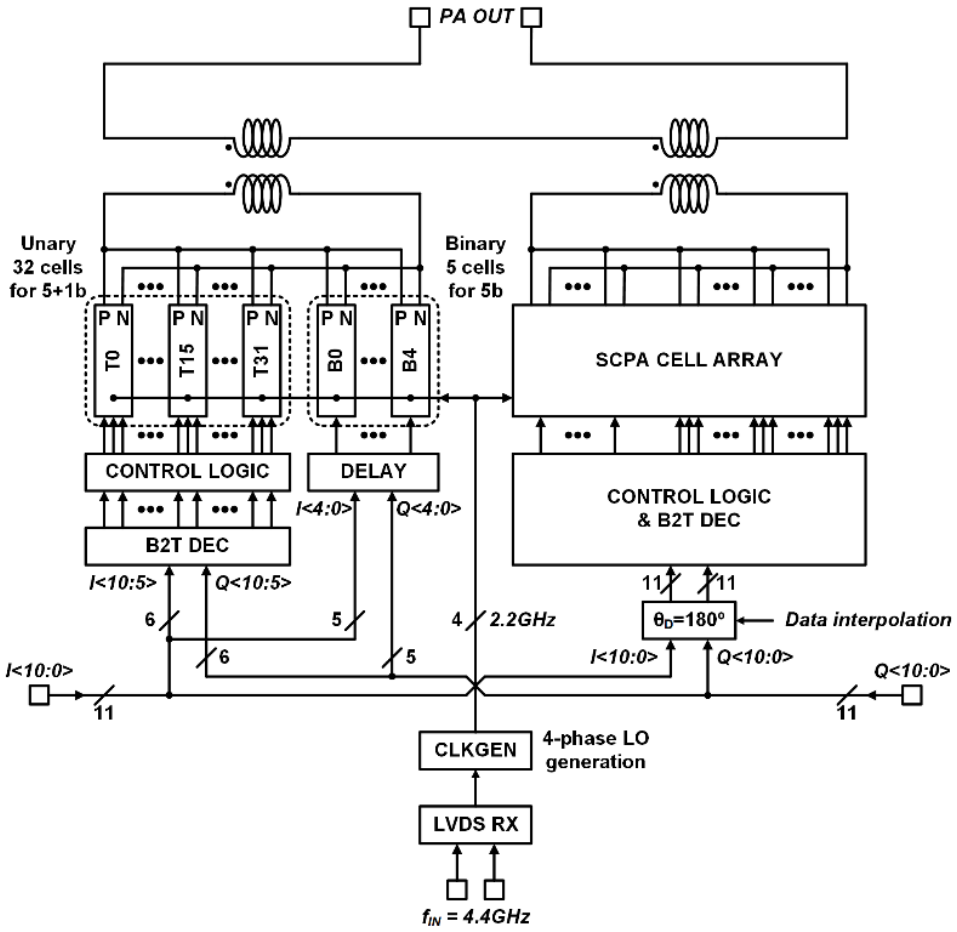


Figure 2-12. Phase mismatch compensation technique for Class-G SCPA.

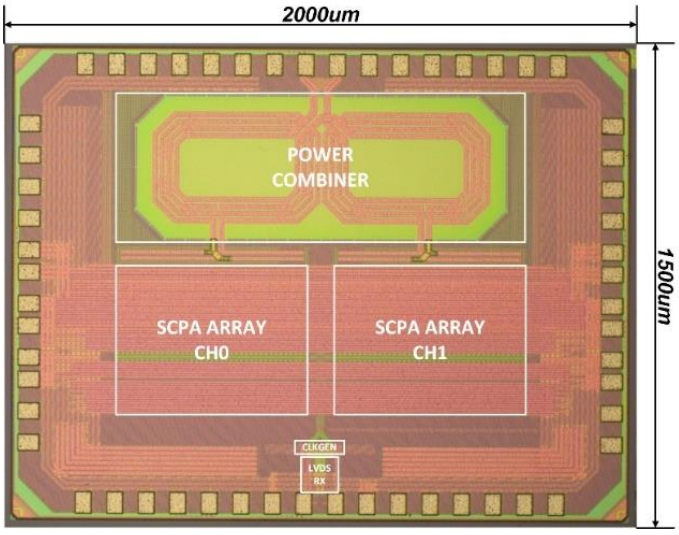
2.8 Measurement Results

Figure 2-13(a) presents a block diagram of the quadrature Class-G SCPA with MCS and linearization techniques. It has two 11-bit SCPAs with a power-combining transformer for delivering more than 30-dBm P_{OUT}. The 11-bit array comprises 6-bit unary and 5-bit binary cells. *IQ* data are interpolated with the two SCPAs in a time-interleaved manner to suppress the spectral images resulting from a low sampling rate. A four-phase clock generator and a low-voltage differential signaling (LVDS) receiver are implemented on the chip for generating four-phase *IQ*-combined unit vectors.

The prototype quadrature SCPA is fabricated in a 65-nm RF CMOS process and occupies an area of 2.0 × 1.5 mm^2, including a power-combining transformer, two SCPAs, a four-phase clock generator, an LVDS receiver, decoupling capacitors, and bonding pads. The chip micrograph is presented in Figure 2-13(b).



(a)



(b)

Figure 2-13. Chip implementation. (a) Block diagram. (b) Micrograph.

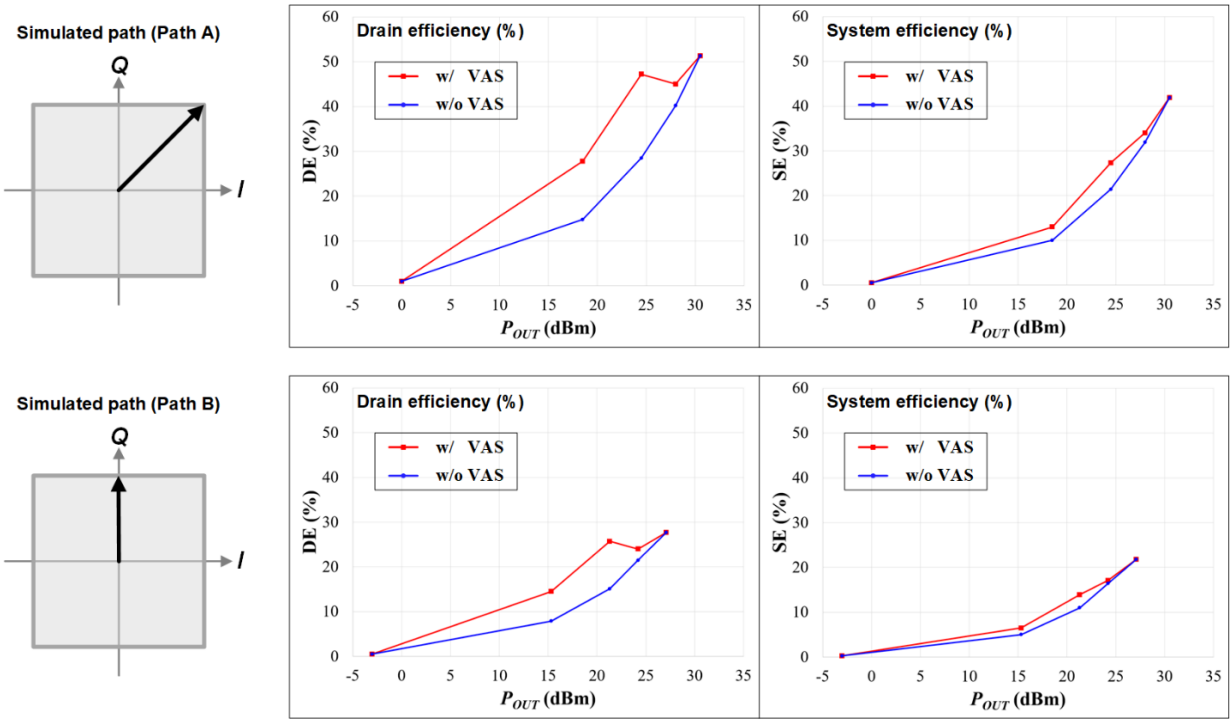


Figure 2-14. Simulated (a) DE vs. P_{OUT} and (b) SE vs. P_{OUT} for a CW signal.

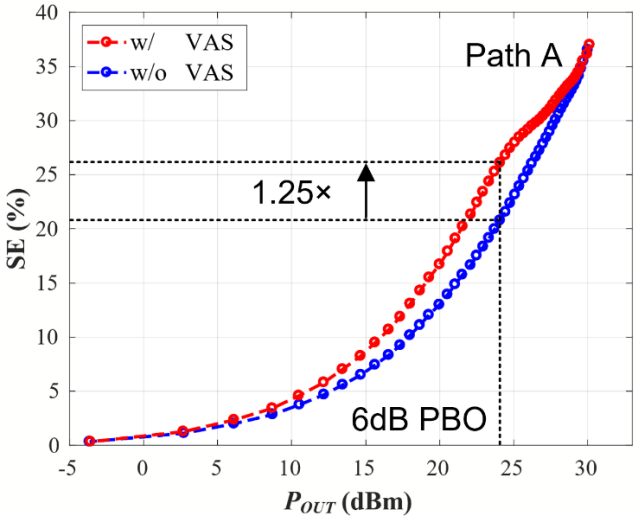


Figure 2-15. Measured SE vs. P_{OUT} for a CW signal.

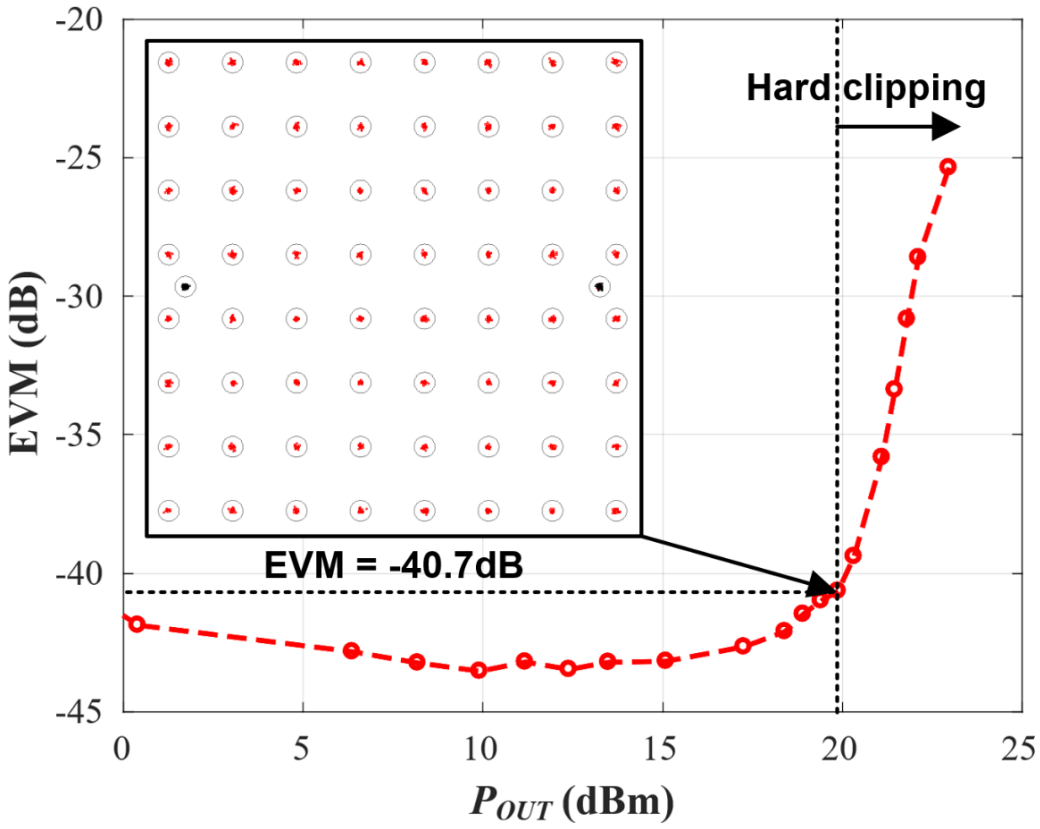
2.8.1 CW Signal Measurement

Figure 2-14 illustrates the extracted simulation results for drain efficiency (DE) versus P_{OUT} and SE versus P_{OUT} with a continuous-wave (CW) signal. Figure 2-15 illustrates the measured SE

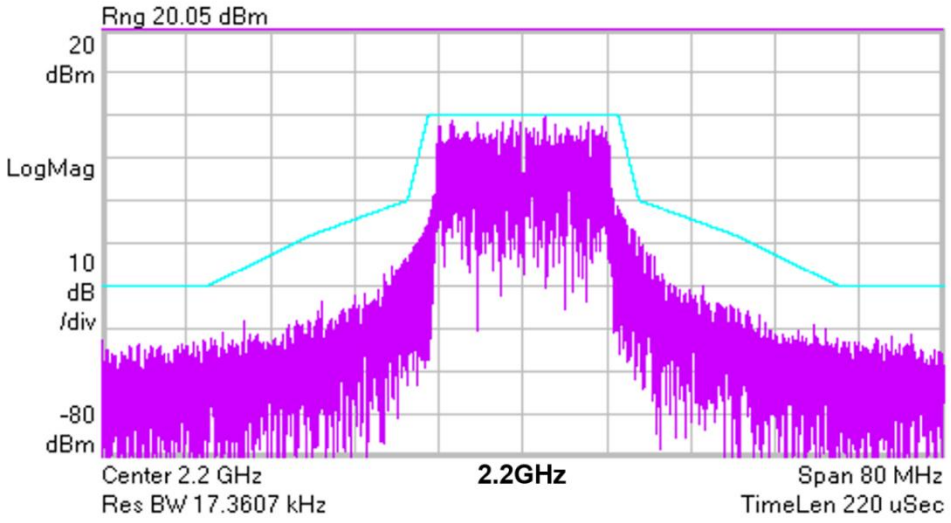
versus P_{OUT} with the CW signal. The prototype SCPA transmits a peak P_{OUT} of 30.1 dBm with a peak SE of 37.0% at 2.2 GHz. With VAS applied for the Class-G operation, the measured SE at 6-dB PBO is 26.1%, which is 1.25 times better than the SE of 20.8% without VAS owing to an additional efficiency peak. In addition, the graph also indicates that the proposed VAS technique for the Class-G SCPA improves SE within 0–6-dB PBO region without any abrupt discontinuity in the efficiency curve [12]. Further SE improvement can be achieved in advanced fine-line CMOS technology because of the reduced power dissipation in digital logic and buffers for driving switches.

2.8.2 Modulated Signal Measurement

Figure 2-16(a) illustrates the EVM versus the average P_{OUT} measured with a 20-MHz, 802.11g 64-QAM OFDM signal with PAPR of 10.6 dB. P_{OUT} is adjusted by changing the digital I /Q input signal. The prototype exhibits an excellent EVM of better than -40 dB for more than 20 dB of P_{OUT} range after DPD. It achieves an EVM of -40.7 dB at an average P_{OUT} of 19.5 dBm. The EVM degradation above 19.5 dBm is due to the hard clipping of signal which also reduces PAPR. A wider dynamic range can be achieved with increased system resolution and accuracy. Figure 2-16(b) illustrates a close-in frequency spectrum at an average P_{OUT} of 19.5 dBm. Figure 2-17 demonstrates the measured data with a modern 802.11ax 1024-QAM OFDM signal. Figure 2-17(a) and (b) illustrate a constellation and a close-in frequency spectrum, respectively, at an average P_{OUT} of 17.7 dBm after DPD. Figure 2-18 presents the out-of-band (OOB) frequency spectrum of the 802.11g with a baseband I /Q data sampling rate of 400 MS/s. The images at 2.2 GHz ± 400 MHz are suppressed by more than 10 dB with interpolated I /Q data. The spectral image can be significantly reduced with a high sampling rate, signal processing techniques, and filtering.

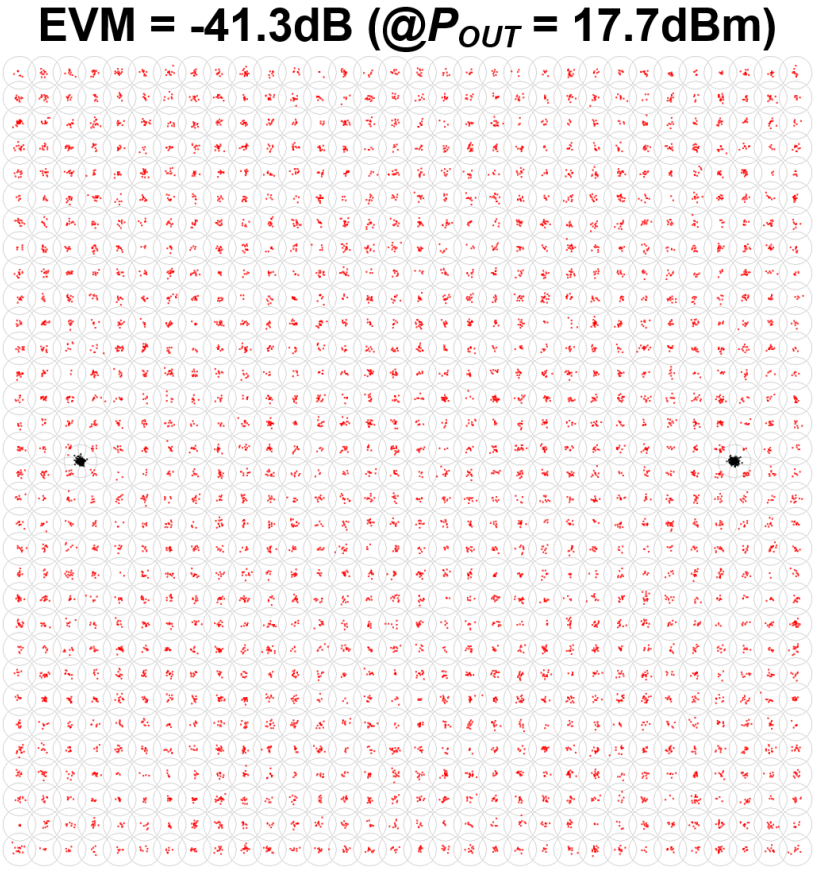


(a)

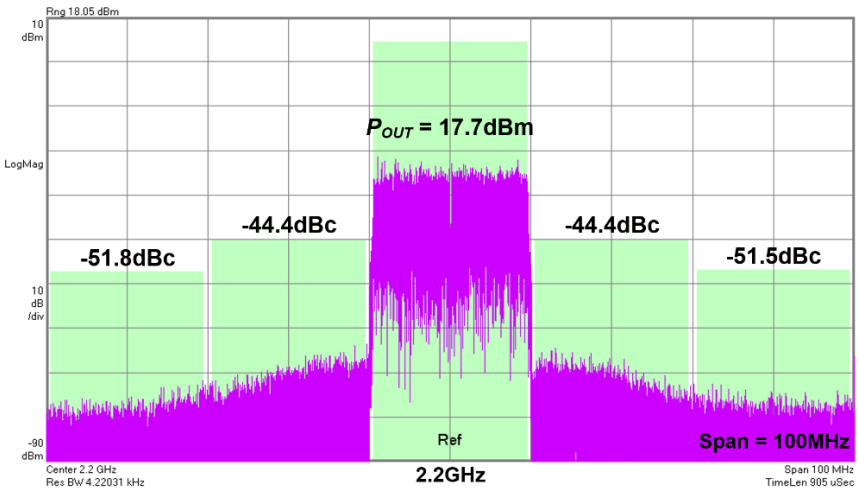


(b)

Figure 2-16. (a) EVM versus average P_{OUT} and (b) its spectrum at average P_{OUT} of 19.5 dBm (after DPD) measured with 802.11g OFDM signal.

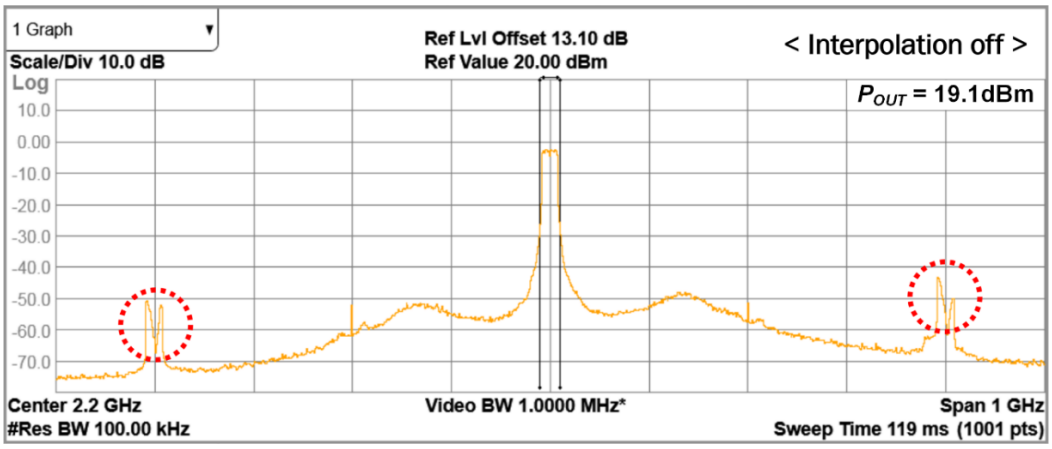


(a)

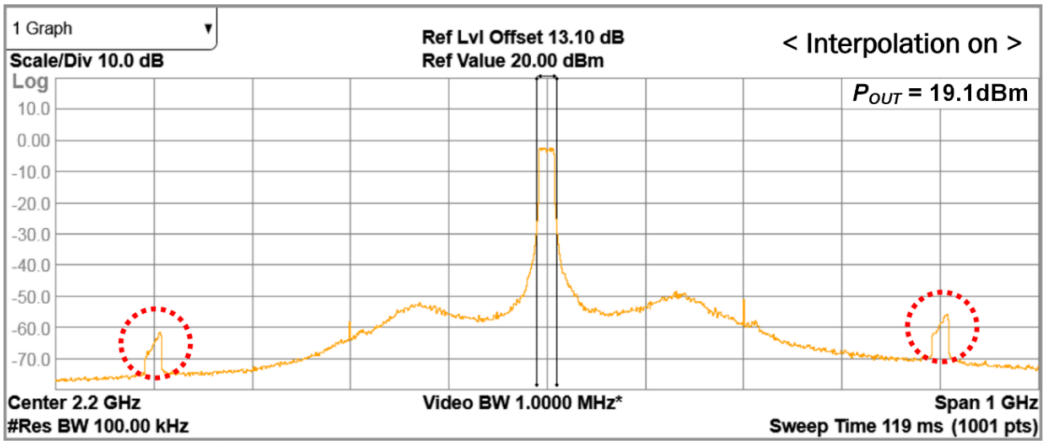


(b)

Figure 2-17. (a) Constellation and (b) spectrum at average P_{OUT} of 17.7dBm (after DPD) measured with 802.11ax 1024-QAM OFDM signal with 12.4-dB PAPR.



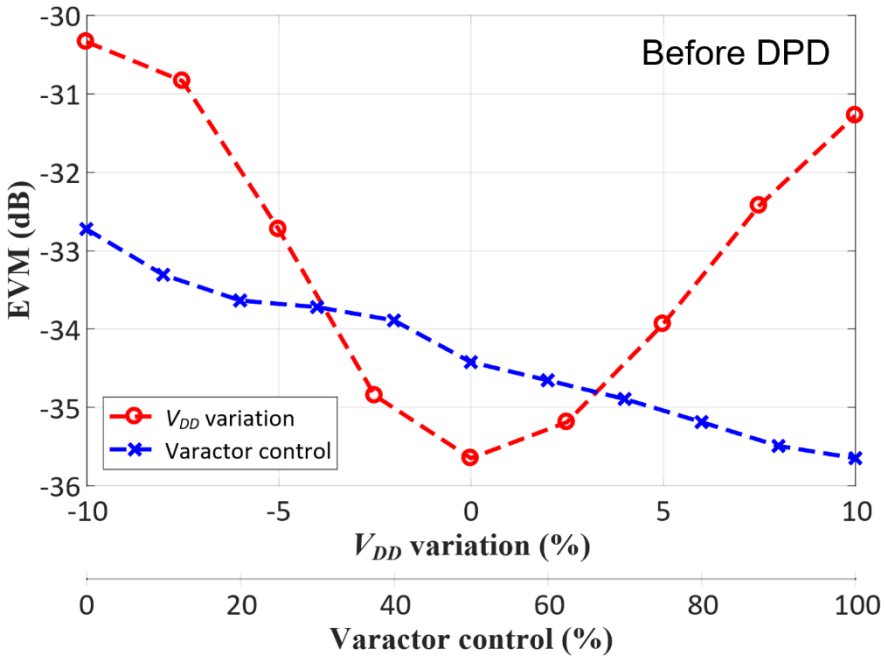
(a)



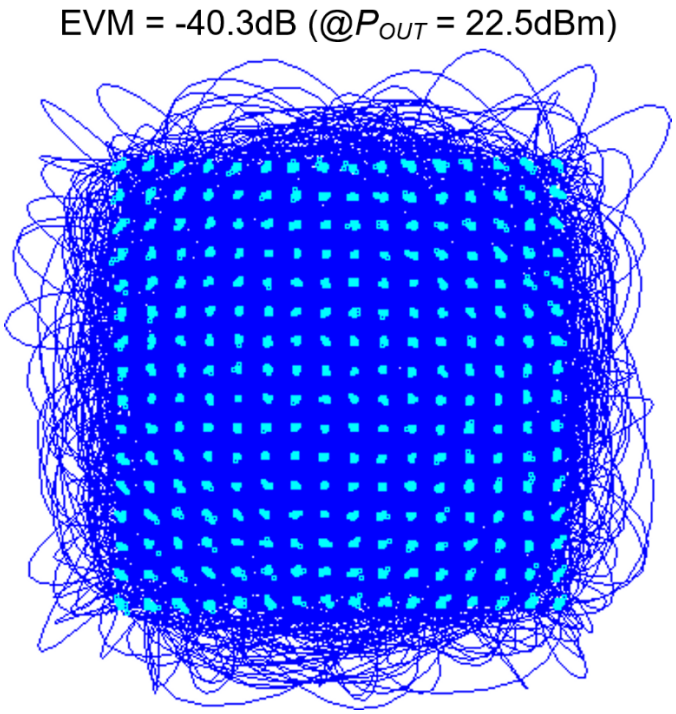
(b)

Figure 2-18. Measured OOB frequency spectrum for 802.11g 64-QAM OFDM signal. (a) Data interpolation OFF and (b) Data interpolation ON.

The performances of the proposed linearization techniques are also verified over V_{DD} variation using a 20-MHz single-carrier 256-QAM signal with a PAPR of 7.6 dB. Figure 2-19(a) presents two EVM curves with the supply voltage and delay mismatches in the V_{DD2} and V_{DD} modes for the Class-G operation. DPD is not applied for demonstrating the effectiveness of the linearization techniques. For the experiment, ±10% of V_{DD} supply voltage is varied while V_{DD2} is fixed to maintain a constant P_{OUT}.



(a)



(b)

Figure 2-19. (a) EVM versus V_{DD} variation and varactor control voltage (before DPD) and (b) Constellation (after DPD) measured with 20-MHz single-carrier 256-QAM signal.

The measured EVM, represented as a red dashed line, demonstrates excellent linearity, better than -32 dB, across the ±5% of V_{DD} variation. Delayed mismatch in the V_{DD2} and V_{DD} modes causes the degradation in EVM. The two separate signal paths operating with different supply voltages of $V_{DD2} - V_{DD}$ and $V_{DD} - V_{SS}$ are directly affected by a different delay and rise/fall time. Notably, the advanced CMOS technology can improve the EVM. The switching speed in advanced CMOS is significantly fast; thus, the transition time and associated delay mismatch can be minimized.

A delay calibration using varactors compensates the phase mismatch between the two Class-G modes, and EVM versus varactor control range is depicted as a red dashed line in Figure 2-19(a). Owing to the insufficient delay control range in this design, the EVM improvement is limited. The measured constellation and EVM are presented in Figure 2-19(b). At an average P_{OUT} of 22.5 dBm after DPD for a 20-MHz 256-QAM signal, the EVM is -40.3 dB.

2.9 Summary

A quadrature Class-G *IQ*-cell-shared SCPA with MCS and linearization techniques is implemented in a 65-nm RF CMOS process. The MCS technique, comprising VAS and VPS, improves SE through enabling a Class-G operation that seamlessly employs dual-supply voltages for a quadrature SCPA. The linearization techniques also enhance the linearity by compensating amplitude and phase mismatches when the PA is driven from two separate supply voltages with the Class-G operation. The outputs of two time-interleaved SCPAs are coupled using a power-combining transformer to achieve watt-level peak output power and minimized spectral image. The prototype 11-bit SCPA achieves peak P_{OUT} and SE of 30.1 dBm and 37.0%, respectively. With an 802.11g 64-QAM OFDM signal, it shows an average P_{OUT} and SE of 19.5 dBm and 14.7%, respectively, while achieving EVM of -40.7 dB after DPD. The prototype with a novel supply-voltage mismatch insensitive output switch cell exhibits EVM better than -32 dB across

±5% V_{DD} variation while delivering an average P_{OUT} and SE of 22.5 dBm and 18.3%, respectively, with a 20-MHz single-carrier 256-QAM signal. A summary of the performance and comparison with the current state of the art is shown in Table 2-1.

Table 2-1 Performance summary and comparison with the state-of-the-art

	JSSC 2016 [23] W. Yuan	JSSC 2017 [25] H. Jin	JSSC 2017 [26] R. Bhat	JSSC 2017 [15] V. Vorapipat	This work	
Architecture	Quadrature Class-G SCPA	Quadrature IQ-cell-shared SCPA	Quadrature IQ-cell-shared SCPA	Polar Voltage Mode Doherty Class-G SCPA	Quadrature Class-G IQ-cell-shared SCPA	
Process (CMOS)	65 nm	28 nm	65 nm	45 nm SOI	65 nm	
Supply	2.4 / 1.2 V	1.1 V	2.6 V	2.4 / 1.2 V	2.5 / 1.2 V	
Resolution (U + B)	7b (5b + 2b)	6b (5b + 1b)	9b (5b + 4b)	9b (5b + 4b)	11b (6b + 5b)	
Carrier freq.	2.0 GHz	0.8 GHz	2.2 GHz	3.5 GHz	2.2 GHz	
Peak power	20.5 dBm	13.9 dBm	30.3 dBm	25.3 dBm	30.1 dBm	
Peak system efficiency	20.0%	40.4%	34.0%	30.4%	37.0%	
Modulation	LTE 10 MHz 64-QAM	LTE 10 MHz 16-QAM	20 MHz Single-Carrier 64-QAM	10 MHz 32 Carrier 1024-QAM	20 MHz Single-Carrier 256-QAM	802.11g 20 MHz 64-QAM
Avg. power	14.5 dBm	6.97 dBm	24.0 dBm	14.8 dBm	22.5 dBm	19.5 dBm
PAPR	6.0 dB	6.9 dB	6.0 dB	10.5 dB	7.6 dB	10.6 dB
Avg. system efficiency	12.2%	29.1%	16.0%	18.0%	18.3%	14.7%
EVM	-28.9 dB	-26.0 dB	-29.2 dB*	-40.3 dB	-40.3 dB	-40.7 dB
EVM floor	-	-	-	-41.0 dB*	-	-43.5 dB (@12.0 dBm)

* Estimated from graph

3 COMPACT QUADRATURE DIGITAL TRANSMITTER BASED ON SWITCHED-CAPACITOR RFDAC WITH LINEARIZATION TECHNIQUES

In this chapter, we present a highly linear digital quadrature *IQ*-cell-shared TX with a small area and low power consumption. For the digital TX architecture, an SC RFDAC is employed [11], and an operational example of the *IQ*-cell-shared SC RFDAC is demonstrated in Figure 1-7 and [25]–[27][33][41][43]. The proposed digital TX employs three linearization techniques and can transmit a 1024-QAM signal with up to 40-MHz bandwidth. The prototype of the quadrature digital TX achieves better than -40-dB EVM over 32-dB P_{OUT} range and uses neither external phase modulator nor DPD.

3.1 Overall Architecture

The overall architecture of the 13-bit digital TX is presented in Figure 3-1. The digital I/Q bits are directly converted into the corresponding RF signal by a single quadrature SC RFDAC. An *IQ* cell sharing with a 25% duty cycle LO signal is used [25]. 6-bit unary cells along with 7-bit binary cells are utilized to achieve a 13-bit resolution in a small area with low power consumption. For an RFDAC with low P_{OUT}, chip area and power consumption are dominated by the total number of unary/binary cells, logic gates and flip-flops, and associated LO distribution in a less advanced CMOS technology node. Even though many unary cells are preferred for excellent linearity, the complexity, area, and power consumption double with each additional bit. The number of unary cells can be reduced by using more binary cells. Besides careful layout techniques, linearity is improved significantly using on-resistance linearization techniques for both switched and unswitched transistors in the DAC array with an RFDAC code-mapping technique.

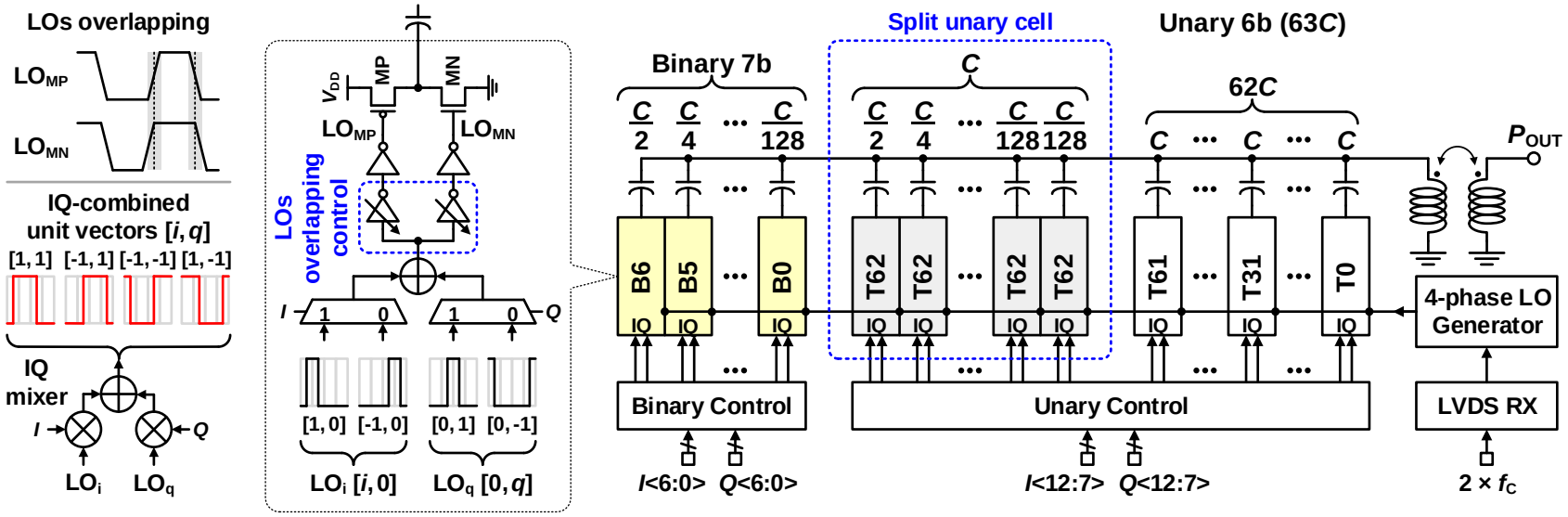


Figure 3-1. Overall architecture of the proposed 13b SC RFDAC.

3.2 Output Switch Linearization Techniques

Linearity goals for information-dense, wideband standards such as 802.11ax, without DPD have not been attained by conventional digital TXs. An equivalent circuit that includes unideal resistive parasitics in both switched and unswitched capacitors is illustrated in Figure 3-2. Nonlinearity is introduced if the source resistance in the Thévenin equivalent circuit, R_S, changes according to the number of switched cells [11]. However, if R_S is either very low, or high even though constant, excellent linearity can be achieved. The combined impedance of switched/unswitched P-type metal-oxide-semiconductor (PMOS) and N-type metal-oxide-semiconductor (NMOS) transistors changing with the input codes determines R_S, as illustrated Figure 3-3. The dynamic changes in R_S are attributed to following two major factors: (1) finite switching duration with changing impedance and (2) on-resistance mismatch between the PMOS and NMOS switches.

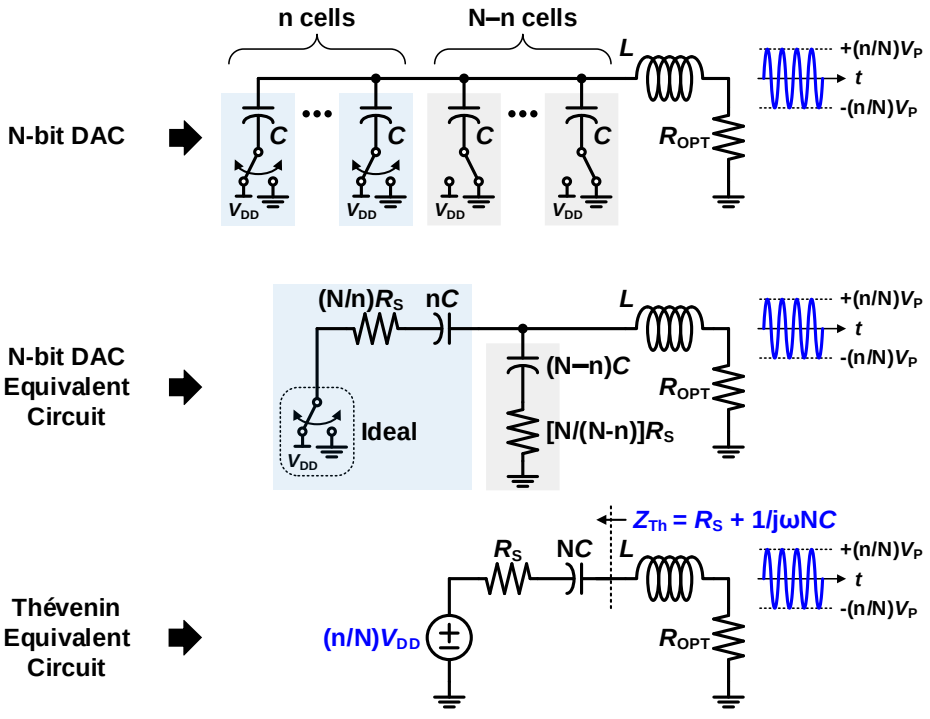


Figure 3-2. Schematic of SC RFDAC with nonlinear switch resistance.

In Figure 3-4, two switch linearization techniques are employed for the high P_{OUT} region. For the switching transistors, partially overlapping clocks provide a more constant on-resistance compared to the on-resistance provided by regular clocks during switching transitions while minimizing dynamic high-impedance states to achieve better linearity. Unwanted large impedance fluctuations are avoided. Assuming a 50% duty cycle and a minimal high-impedance period, the parasitic resistance of each switch pair (R_{SO}) connected to a unit capacitor is approximately $(R_P+R_N)/2$.

In a conventional SC RFDAC in which all unswitched capacitors are connected to V_{GND}, the ground-path parasitic resistance is a function of R_N only, as illustrated Figure 3-3. In this design, half of the unswitched capacitors are connected to V_{GND} and the other half to V_{DD}, as illustrated in Figure 3-4. Thus, the R_{SO} for each unswitched capacitor is also approximately $(R_P+R_N)/2$. Furthermore, in differential implementation, the alternate array has exactly the opposite connection to V_{DD} and V_{GND}. These techniques provide enhanced switch linearity over a wide P_{OUT} range, especially for digital TX in older CMOS technologies with slow switches (e.g., 65 nm vs. 28 nm) or at higher operating frequencies.

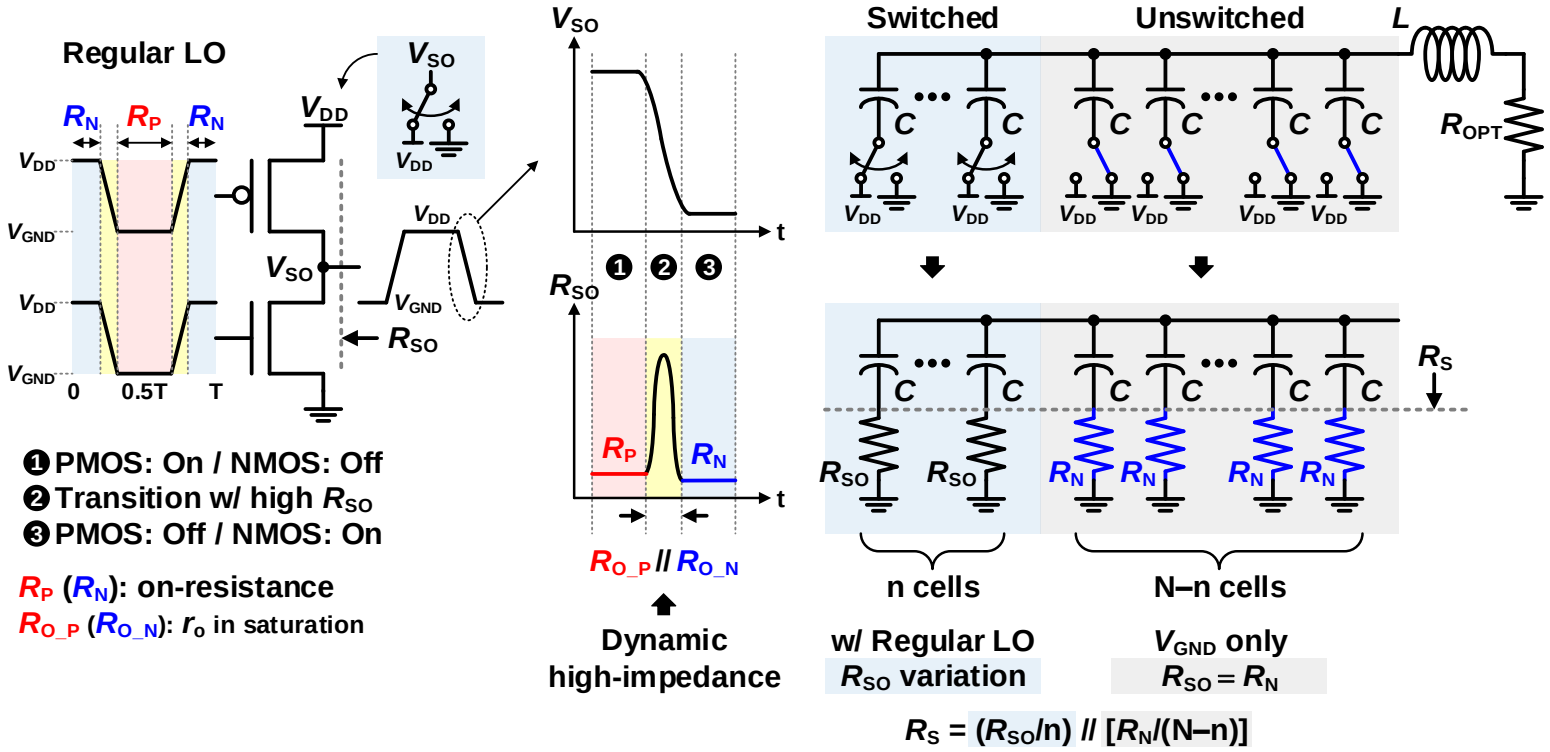


Figure 3-3. Switch impedance of the conventional SC RFDAC.

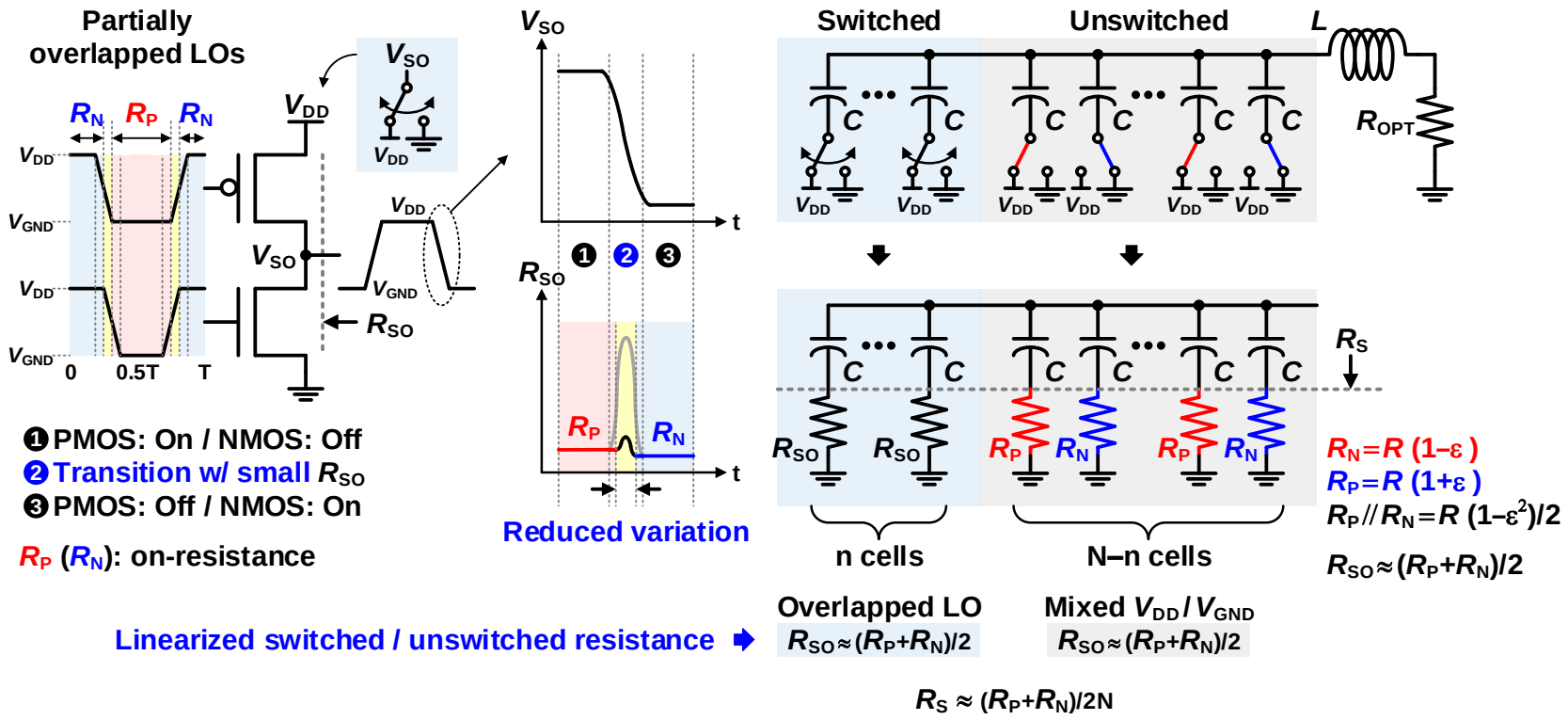


Figure 3-4. Switch impedance of the proposed SC RFDAC.

3.3 Code Mapping Technique for RFDAC Linearization

For a DAC, cells require segmentation into unary and binary cell groups for optimizing area and power consumption, while maintaining the required accuracy. The linearity of the DAC can be degraded due to the mismatch between the unary and binary cell groups and among the binary cells. For the digital TX with an RFDAC, nonlinearity occurs in both amplitude and phase domain owing to the mismatches. Even though the mismatches can be reduced by careful design and layout, the mismatches that are retained due to the PVT variation and imperfect phase calibration among the cells still limit the linearity of the digital TX.

3.3.1 Digital-Code-Mapping Techniques for RFDAC

Figure 3-5 demonstrates an instance of the mismatch between the unary and binary cell groups for 1-D/2-D DACs with 3-bit unary cells; each coarse unary-code region (red) is divided into finer binary-code regions (blue). At a low P_{OUT}, the RFDAC operation involves the switching of a few unary cells and relatively more binary cells. Assuming the unary and binary cells do not match perfectly, maximum mismatch occurs at unary cell transitions where all the binary cells are also switching.

An offset-mid-tread mapping technique for the RFDAC that achieves high linearity at low P_{OUT} is introduced. A conventional mid-rise mapping [25][27][33] presented in Figure 3-6(a) has an abrupt unary code transition at the origin, which dominates nonlinearity at low P_{OUT}. Conventional mid-tread mapping Figure 3-6(b) with no unary-code transition at the origin improves linearity, but the adjacent transitions still occur at relatively low P_{OUT}. The low P_{OUT} linearity is increased using the proposed offset mid-tread code-mapping method presented in Figure 3-6(c) wherein no unary cell transition occurs at the origin and code distances to the first transitions are doubled compared to conventional mid-tread mapping. In a similar manner, the

delay (phase) nonlinearities are reduced, as illustrated in Figure 3-7. The presented mapping is especially effective for a RFDAC that does not use a conventional mixer with its attendant transmit LO leakage and concomitant DC offset calibration.

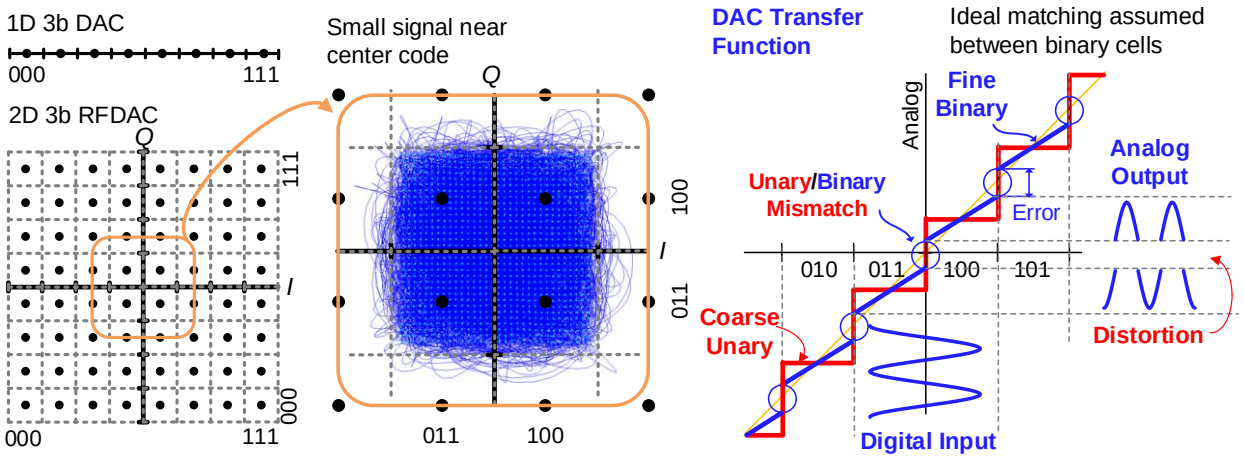


Figure 3-5. Example of linearity degradation from the mismatch between unary and binary cell groups.

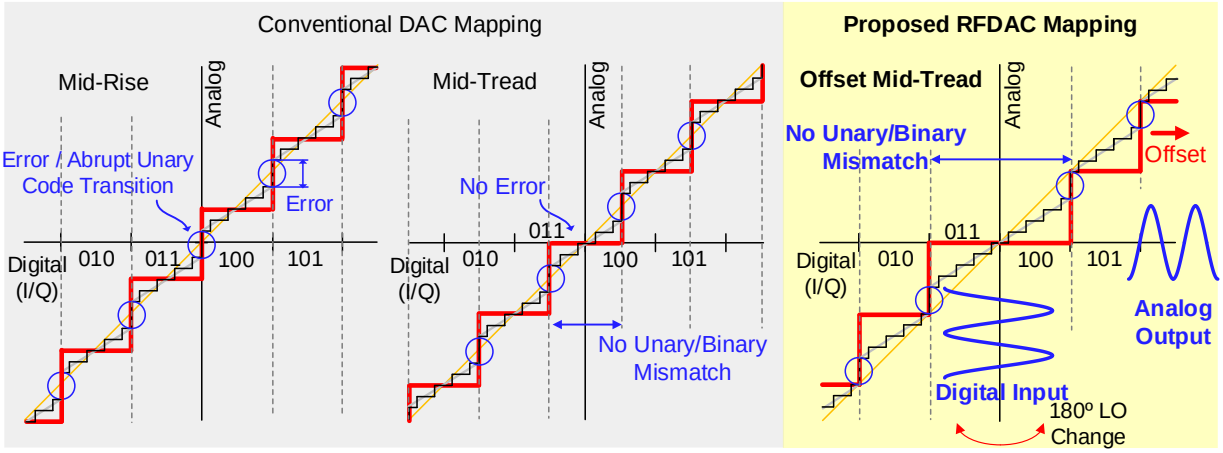


Figure 3-6. Comparison between (a) Mid-rise, (b) mid-tread, and (c) offset mid-tread code mapping techniques for a 1-D DAC.

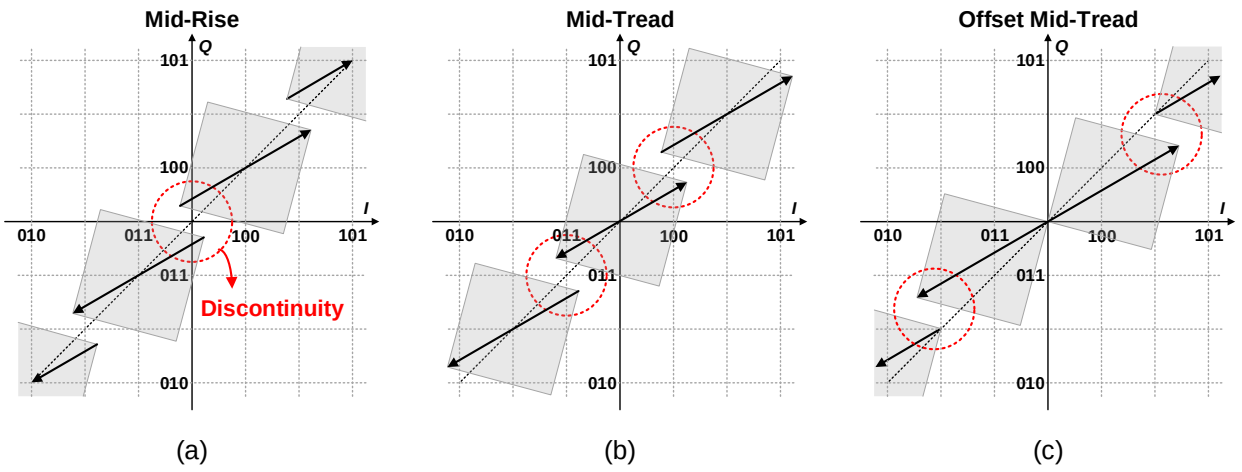


Figure 3-7. Comparison between (a) Mid-rise, (b) mid-tread, and (c) offset mid-tread code mapping techniques for a 2-D DAC.

3.3.2 Mid-Rise and Offset Mid-Tread Code Mapping Techniques in Complex Domain

As illustrated in Figure 3-8, the conventional mid-rise code mapping [25][27][33] represents the deepest PBO region by merging a single unary vector and multiple binary vectors, which are 180º OOP from each other. Therefore, the mismatch between the unary and binary vectors leads to an abrupt transition near the origin in the *IQ* plane, as illustrated in Figure 3-9. In this example, for simplicity, it is assumed that there is only phase mismatch (θ_{MIS}) between the two cell groups, and all the binary vectors are ideally matched.

Unlike the conventional mid-rise technique, the proposed offset mid-tread technique represents the deepest PBO region only with the binary-weighted vectors, preventing the abrupt transition near the origin in the *IQ* plane as illustrated in Figure 3-10.

Even if the θ_{MIS} between the unary and binary cell groups in Figures 3-9 and 3-10 are the same, the phase distortion (θ_{ERR}) of the vector sum is considerably improved by the offset mid-tread code mapping, as illustrated in Figure 3-10. The θ_{ERR} is the same as θ_{MIS} in the proposed offset mid-tread code mapping.

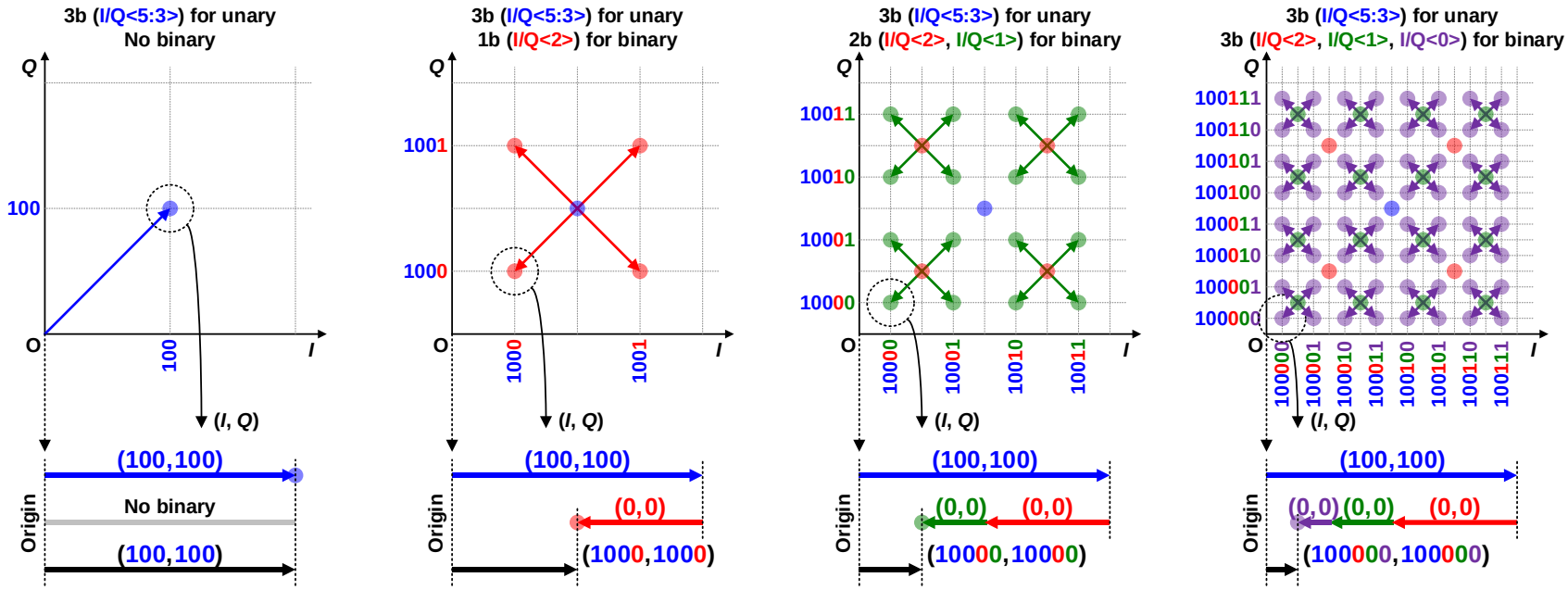


Figure 3-8. Conventional mid-rise code mapping.

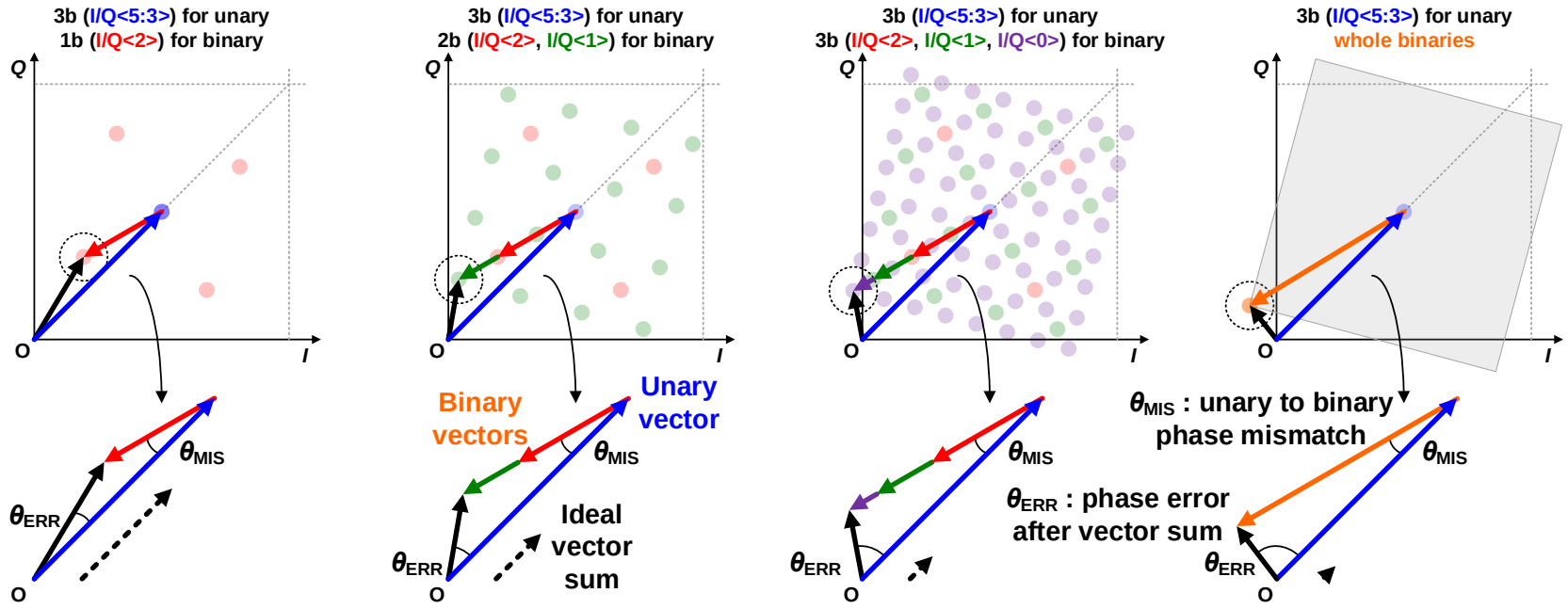


Figure 3-9. Conventional mid-rise code mapping with a phase mismatch (θ_{MIS}) between unary and binary cell groups.

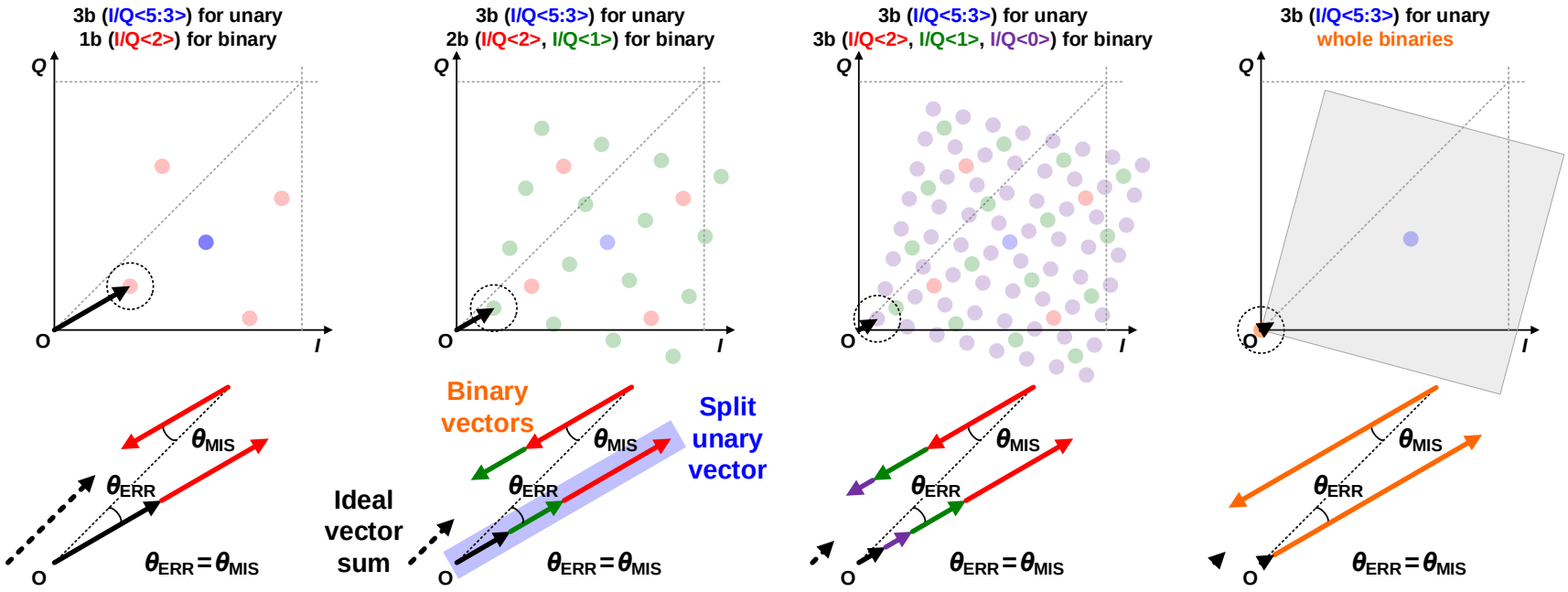


Figure 3-10. Offset mid-tread code mapping with a phase mismatch (θ_{MIS}) between unary and binary cell groups.

3.3.3 Implementation of RFDAC with Offset Mid-Tread Code Mapping

To implement the proposed mid-tread code mapping, a single unary vector is split into multiple binary-weighted vectors with the same resolution as the binary vectors in the SC RFDAC. Therefore, vector cancellation occurs between the split unary and corresponding binary-weighted split-unary vectors when they have 180º OOP relations. Because the split-unary vector better matches the binary vectors than a single unary vector, the linearity at the deepest PBO region significantly improves, as shown in Figure 3-10. For further enhanced linearity, a digital domain vector removal technique [25] is applied between the split-unary and binary vectors, as illustrated in Figure 3-11. Even if the split-unary vector matches the binary vectors better than a single unary vector, mismatches between the split-unary and binary vectors can persist. The digital domain vector removal technique completely cancels out the errors and leaves no residual mismatches by pairing the vector with 180º OOP relations and deactivating those cells. By employing the offset mid-tread code mapping, the unary code of the TX output can be defined without any discontinuity at the origin in the *IQ* plane, and the discontinuity due to the unary code transition shifts to the higher P_{OUT} region. This is because the unary vectors only become activated after both split-unary and binary vectors are fully turned on with the same phase.

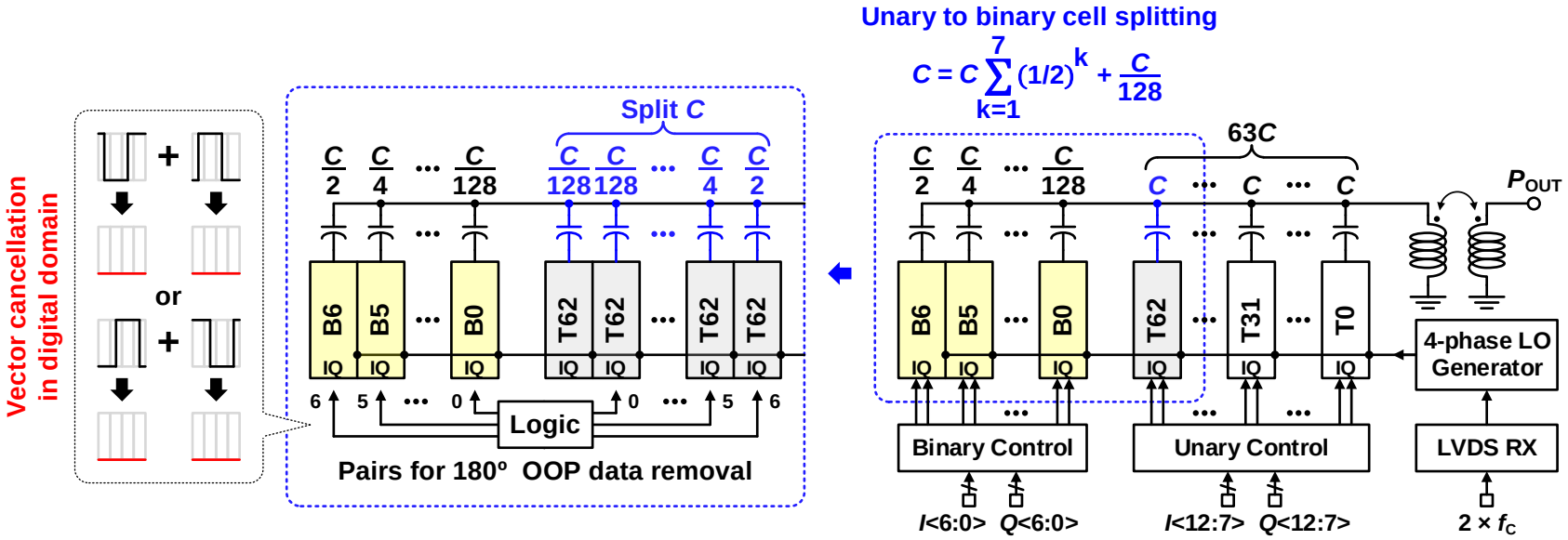


Figure 3-11. Implementation of the offset mid-tread code mapping.

3.4 Proposed Merged SC RFDAC Cell

In addition to the area- and power-efficient unary and binary cell segmentation, the sub-circuit sharing technique between the two quadrature *IQ*-cell-shared SC RFDAC cells is proposed for further reduction of the area and power consumption. As illustrated in Figure 3-12, the two quadrature *IQ*-cell-shared SC RFDAC cells are merged into a single cell, halving the number of the sub-circuits that operate at RF, such as digital mixers, logic gates, and signal buffers.

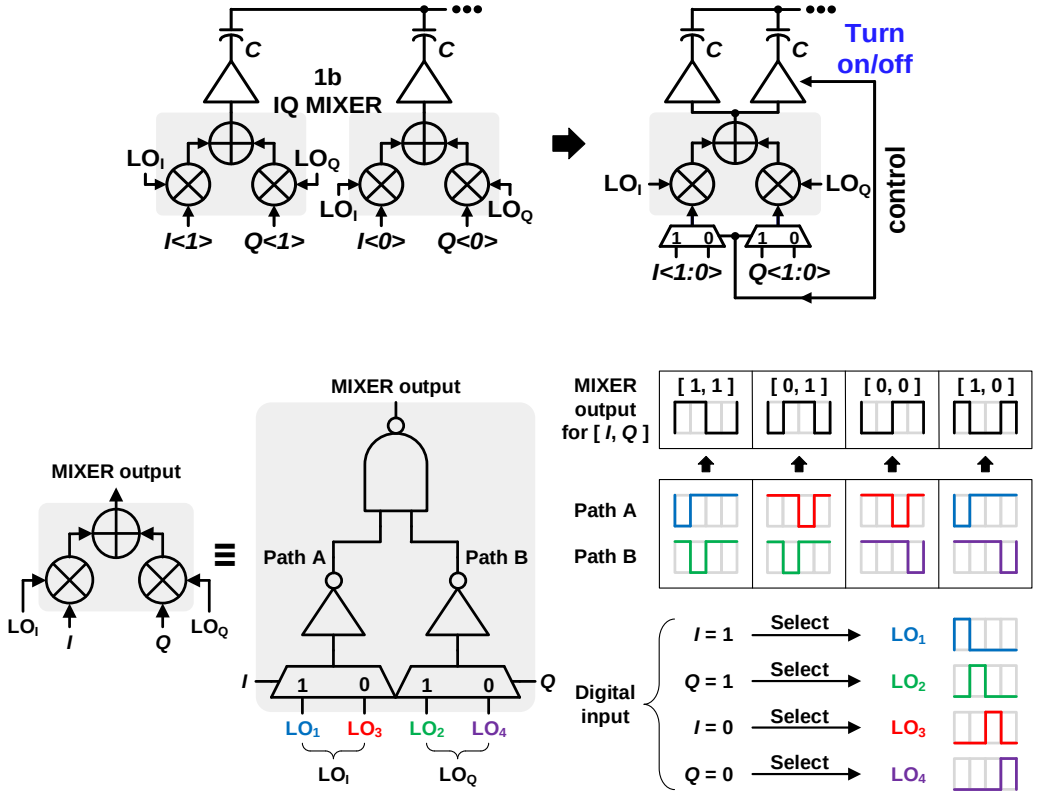


Figure 3-12. Proposed quadrature *IQ*-cell-shared SC RFDAC cell and its 1b *IQ* mixer.

Because each merged SC RFDAC cell has only one *IQ* mixer, it cannot process the two input *IQ* data sets [*I*<*n*>, *Q*<*n*>] simultaneously. Therefore, only one of the two *IQ* data sets is selected as an input of the SC RFDAC cell by a control signal. The proposed SC RFDAC cell operation is as follows: i) If the two *IQ* data sets are the same, the multiplexers select any one of them, and the control signal activates both output switches in the SC RFDAC. ii) If the two data sets are different

or iii) one of them is disabled by the 180º OOP data removal as illustrated in Figures 3-13(a) and (b), the control signal only selects the enabled *IQ* data set and deactivates one of the two output switches. In case ii), the unselected *IQ* data set can be compensated by the reserved SC RFDAC cell with the vector switching operation as presented in [27][33] and Figure 3-13(b). iv) If both data sets are disabled, the cell is turned off, as illustrated in Figure 3-13(b).

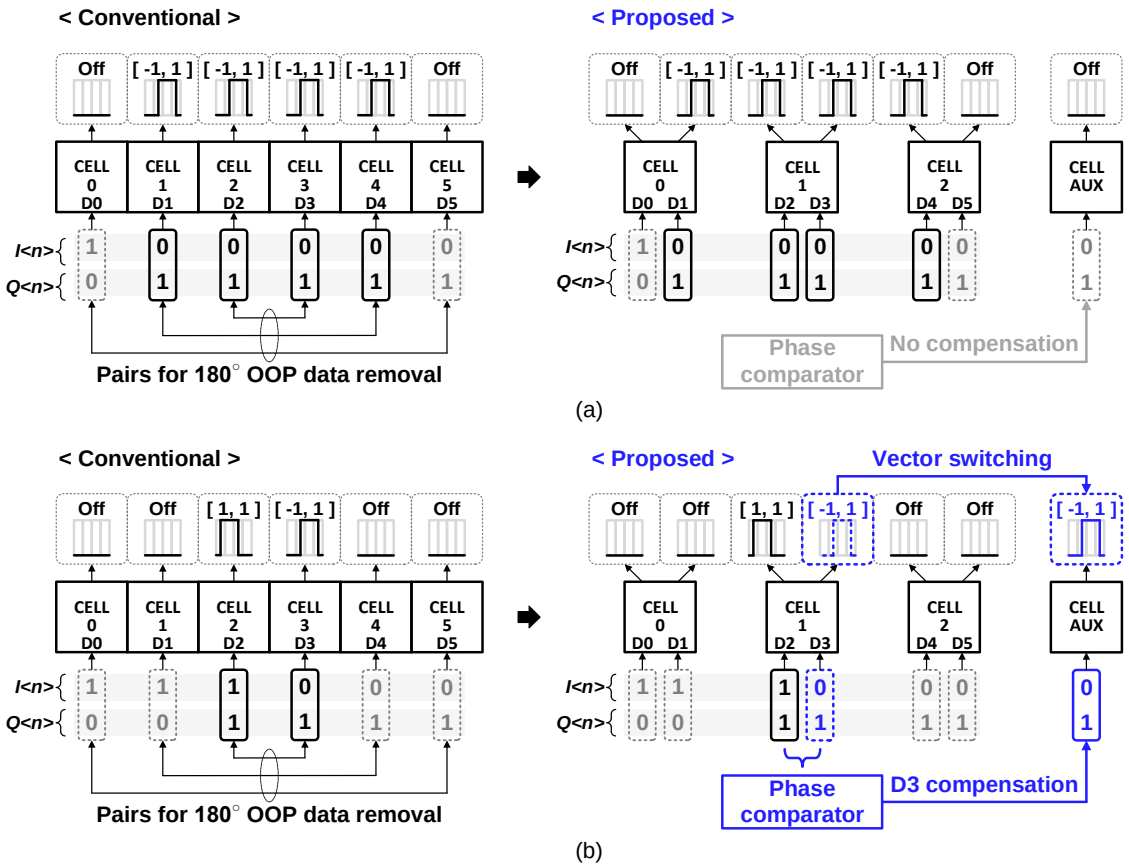


Figure 3-13. Examples of the proposed quadrature *IQ*-cell-shared SC RFDAC operation. (a) Without vector switching and (b) with vector switching.

3.5 Measurement Results

The digital TX incorporating all three linearization techniques is implemented in a 65-nm CMOS. A measured constellation for single-carrier 1024-QAM signals is presented in Figure 3-14.

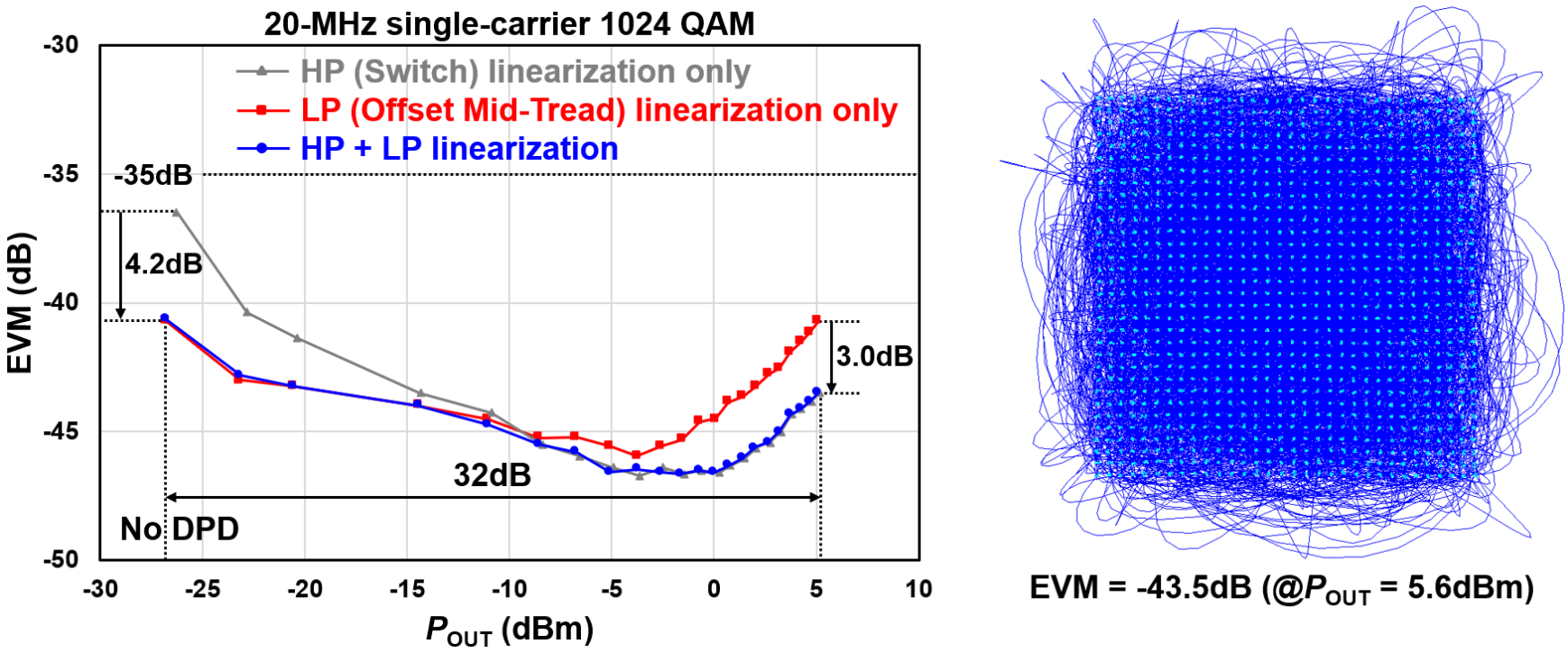


Figure 3-14. Constellation and EVM vs. P_{OUT} for 1024-QAM signal before/after linearization techniques for high P_{OUT} (HP) and low P_{OUT} (LP) applied.

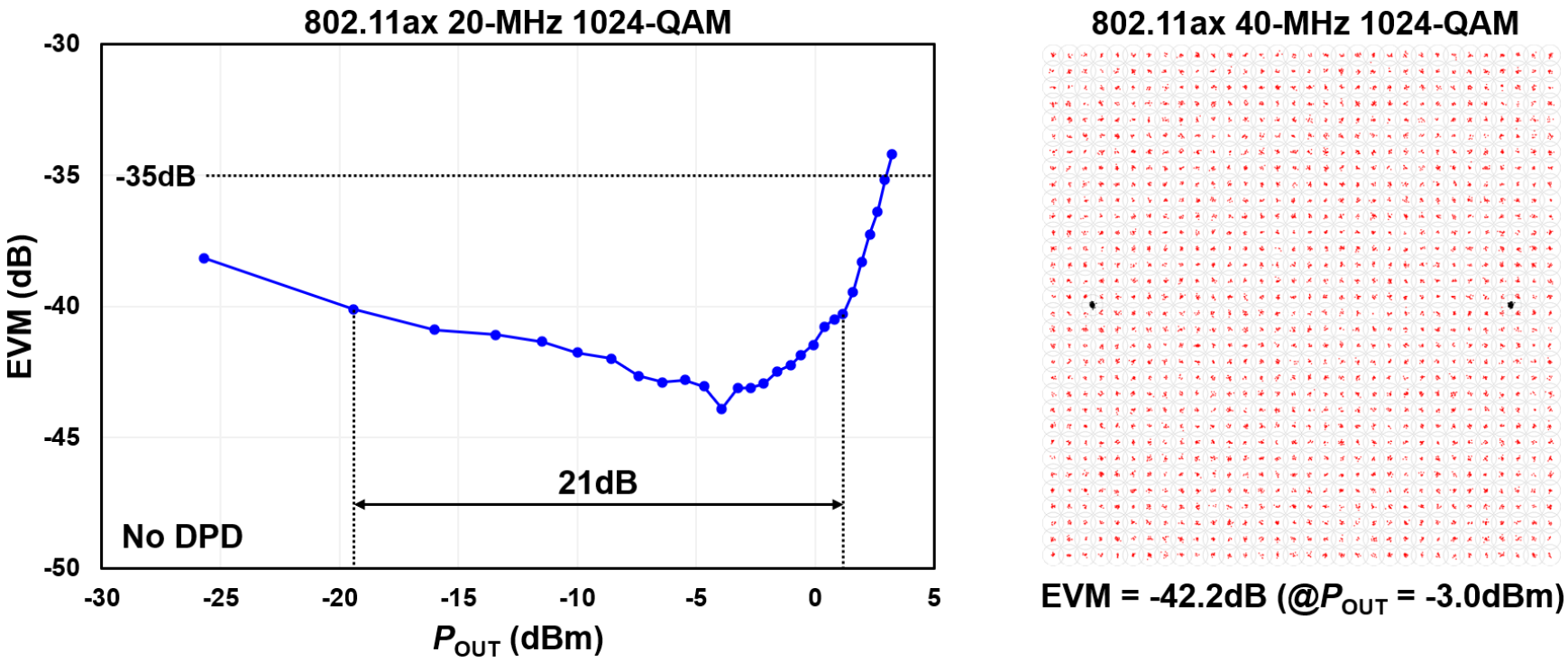


Figure 3-15. EVM and constellation for an 802.11ax 20/40 MHz.1024-QAM OFDM signal.

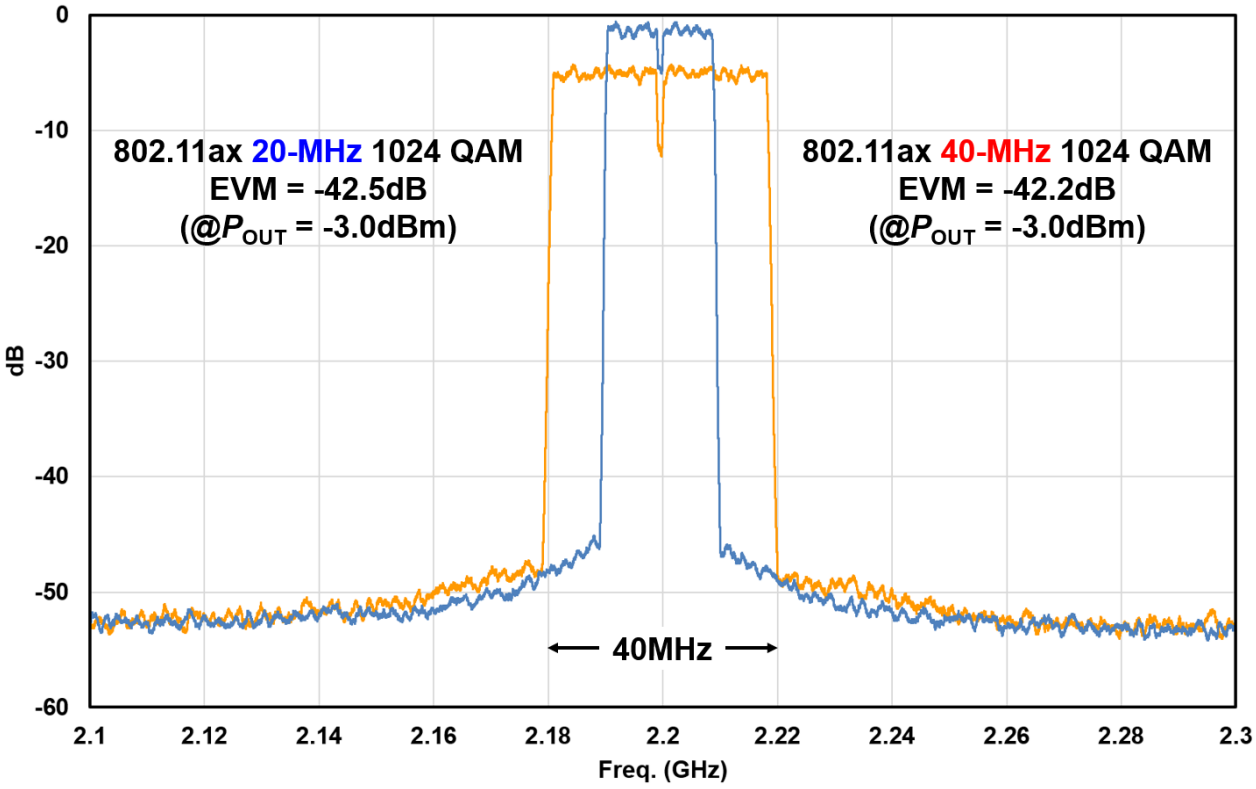


Figure 3-16. Spectra for an 80211ax 20/40 MHz 1024-QAM OFDM signal.

Additionally, measured EVM vs. P_{OUT}, in which the separated and combined effects of the three linearization techniques are illustrated, has been shown; EVM is improved by more than 3 dB for both high and low P_{OUT}. At 2.2 GHz, the design demonstrates an excellent EVM of better than -40 dB over 32-dB P_{OUT} range with a minimum EVM of -46.6 dB without any DPD. For 802.11ax 20-/40-MHz 1024-QAM OFDM signals with 12.5-/13.1-dB PAPR, the quadrature RFDAC-based TX demonstrates excellent EVM of -42.5/-42.2 dB (Figure 3-15) at -3.0-dBm P_{OUT}, without any DPD. The measured spectra with the 802.11ax 20-/40-MHz 1024-QAM OFDM signals are demonstrated in Figure 3-16. Compared to recent prior-art designs in more advanced 28-nm CMOS technologies (Table 3-1), the prototype Digital TX, even in a 65-nm CMOS, consumes reduced chip area and achieves higher linearity over a greater P_{OUT} range and wider bandwidth. A die micrograph is presented in Figure 3-17.

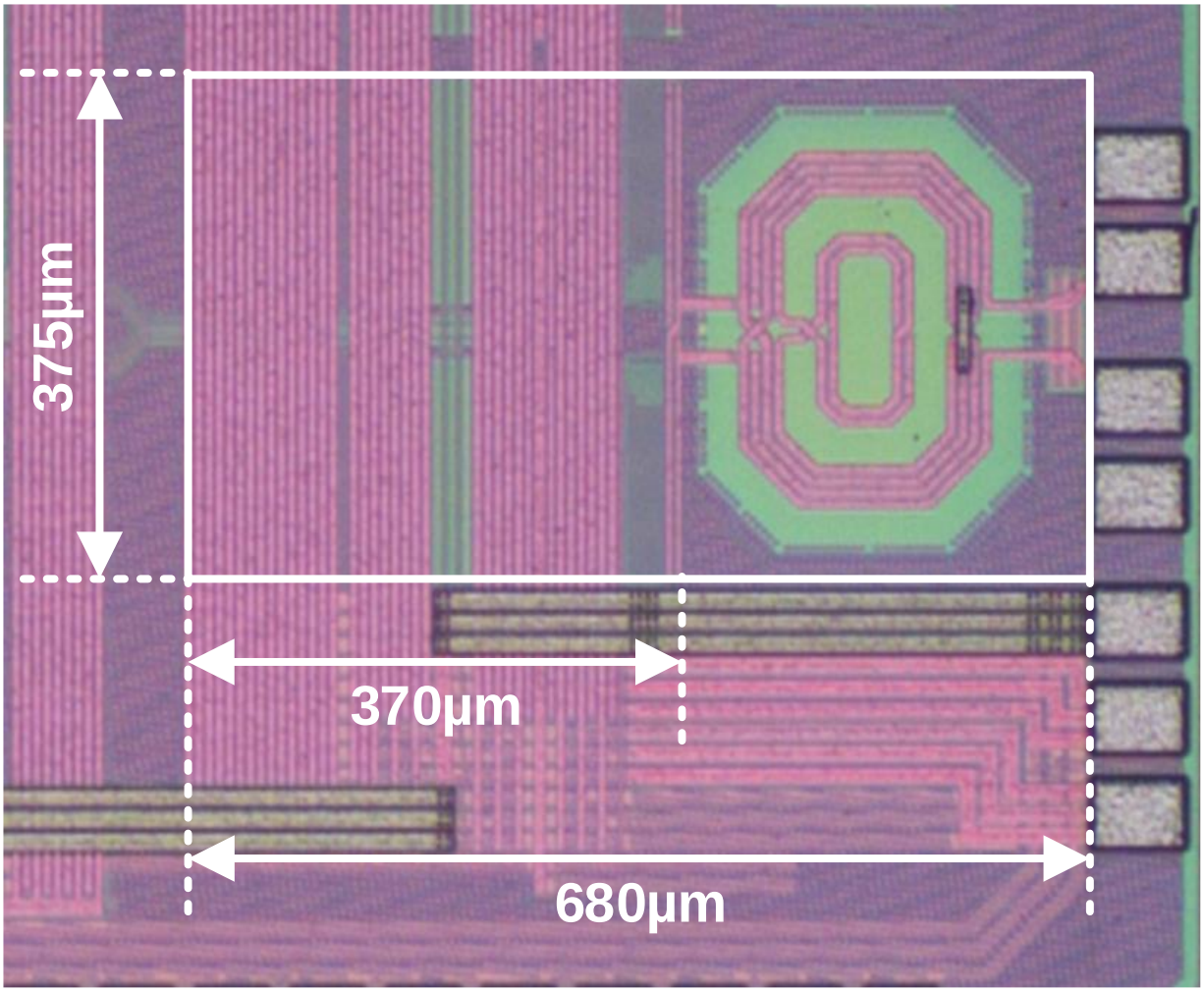


Figure 3-17. Chip micrograph.

3.6 Summary

For the small and low-power digital TX solution, a compact, highly-linear quadrature digital TX that achieves better than -40-dB EVM over 32-dB P_{OUT} range without any DPD is presented. High linearity over the complete P_{OUT} range is achieved with three linearization techniques for minimized impedance variation and systematic enhancement in unary/binary cell utilization. This prototype in a 65-nm CMOS occupies only 0.26 mm^2 with on-chip matching and exhibits -42.5/-42.2-dB EVM for an 802.11ax 20/40-MHz 1024-QAM OFDM signal at -3-dBm P_{OUT} at 2.2 GHz without any DPD.

Table 3-1 Performance summary and comparison with the state-of-the-art

REF		VLSI 2018 [28]	ISSCC 2017 [13]	ISSCC 2016 [29]	This work	
Architecture		Polar Class-D^{-1}	Polar CDAC	Quadrature RQDAC	**Quadrature CDAC**	
Phase Modulator		Required	Required	NOT Required	**NOT Required**	
Process (nm)		28	28	28	**65**	
Supply (V)		0.9	1.0 / 1.1 / 1.3	0.9 / 1.1	1.2	
Resolution (bit)		10	15 (10+5)	12 (5+7)	13 (6+7)	
Frequency (GHz)		4.95 – 6.05	2.3 – 2.8	2.4	2.2	
Peak P_{OUT} (dBm)		11.0	-	3.5	**13.0**	
Modulation	Bandwidth (MHz)	2.5	20	20	**20**	**20 (40)**
	Type	1024 QAM	LTE	Multi-tone	**1024 QAM**	**802.11ax 1024 QAM**
	PAPR (dB)	-	-	7.0	7.6	12.5 (13.1)
	EVM (dB) @P_{OUT} (dBm)	-41.3 @-2.7	-31.7 @6.0	-36.0 @-3.5	**-46.6 @0**	**-42.5 @-3.0 (-42.2 @-3.0)**
	DPD	DPD	No DPD	DPD	**No DPD**	**No DPD**
	Power Control (dB) / Max. EVM (dB)	-	~60 / -31.7	-	**32 / -40, >40 / -35**	**21 / -40, >30 / -35**
Current (mA) @P_{OUT} (dBm)		51.1 @-2.7	43.0 @-18	27.5† @-3.5	42.0 @-3.0	
Area (mm^2)		2.62	-	0.22	**0.14 (0.26 w/ Matching)**	
Matching		On-chip	On-chip	Off-chip	**On-chip**	

† Estimated from graph

4 MULTIMODE MULTI-EFFICIENCY-PEAK DIGITAL POWER AMPLIFIER

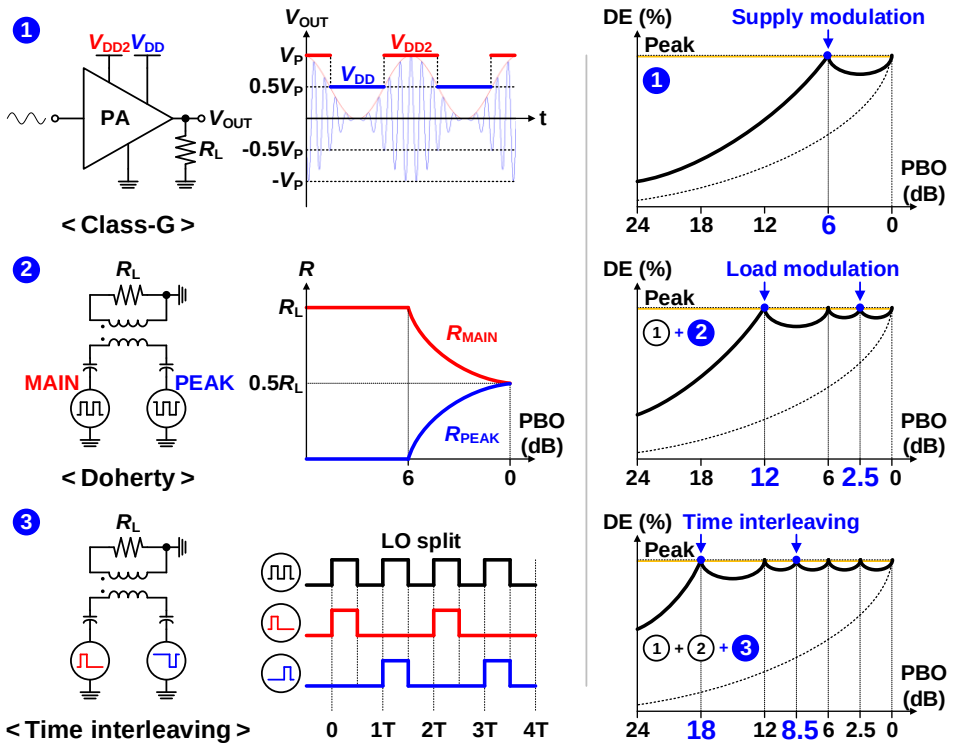


Figure 4-1. Ideal efficiency of the proposed multimode SCPA with a combination of three efficiency enhancement techniques: dual-supply Class-G, transformer-based Doherty, and 2-way TI.

In this study, a multimode multi-efficiency-peak digital PA with six outstanding efficiency peaks down to 18-dB PBO is proposed by utilizing three different efficiency-enhancement techniques, namely, Class-G, Doherty, and TI, as shown in Figure 4-1. The overall efficiency can be improved without any substantial hardware burden using various techniques in different switching sequences. Different combinations can be accomplished using different efficiency-enhancement techniques. In the proposed SCPA with various efficiency-enhancement techniques, the Class-G technique is used to present an additional efficiency peak at 6-dB PBO. Next, the combination of Class-G and Doherty provides two additional efficiency peaks at 2.5- and 12-dB

PBOs. Finally, by using the TI technique, two additional efficiency peaks are introduced at 8.5- and 18-dB PBOs. Moreover, the continuous efficiency curves between the efficiency peaks are attained by the seamless transitions between the operation modes.

To further boost the system-level efficiency and linearity, we propose a single-supply current-reuse Class-G switch that enables a dual-supply Class-G operation from a single supply without any additional supply voltage. The conventional Class-G technique with multiple supply voltages usually entails an additional supply voltage from extra hardware, such as external PMU. An LO signal restoration technique for the TI operation is proposed to lessen the chip area and power consumption for the LO signal distribution.

4.1 Efficiency of the Switched-Capacitor Power Amplifier with Efficiency-Enhancement Techniques

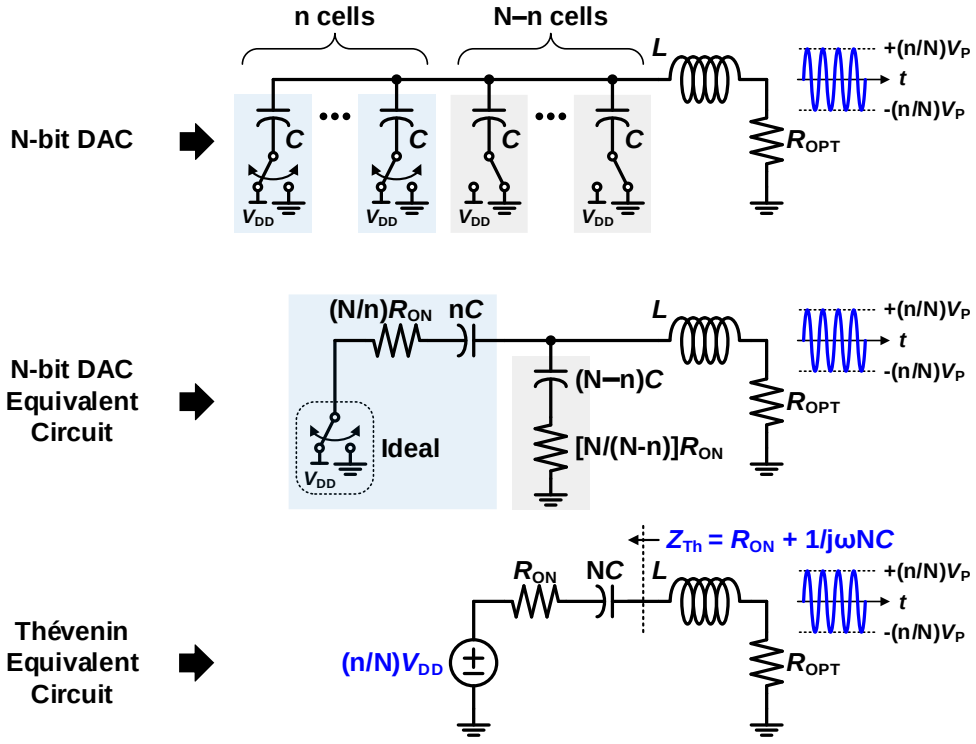


Figure 4-2. Schematic of the basic SCPA architecture.

Figure 4-2 displays a diagram of the conventional SCPA [11]. The number of capacitors switching between V_{DD} and V_{SS} at RF regulates the P_{OUT} of the SCPA. An ideal bandpass network, which is an ideal inductor in series with the capacitor array, filters the square wave and provides a fundamental component at the output. The output voltage (V_{OUT}), output power (P_{OUT}), dynamic power dissipation in the capacitor array (P_{SC}), and ideal drain efficiency (η_{IDEAL}) are detailed in [11] and summarized as follows:

$$|V_{OUT}| = \frac{2}{\pi}\frac{n}{N}V_{DD} \tag{4.1}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left(\frac{n}{N}\right)^2\frac{{V_{DD}}^2}{R_{OPT}} \tag{4.2}$$

$$P_{SC} = \frac{n(N-n)}{N^2}C_{TOT}{V_{DD}}^2 f \tag{4.3}$$

$$\eta_{IDEAL} = \frac{P_{OUT}}{P_{OUT}+P_{SC}} = \frac{1}{1+\frac{\pi}{4}\frac{N-n}{n}\frac{1}{Q_{LOAD}}} \tag{4.4}$$

where N, n, C_{TOT}, R_{OPT}, and Q_{LOAD} are the total number of capacitors, number of switching capacitors, total capacitance of the capacitor array, optimum load resistance, and loaded quality factor of the matching network, respectively.

In Chapter 4-2, the efficiencies of the dual-supply Class-G, Doherty, and 2-way TI SCPAs are introduced. The efficiencies of the SCPAs with each efficiency-enhancement technique are evaluated and compared with one another. In Chapter 4-3, a detailed theoretical analysis on the efficiency and implementation of the multimode SCPA and the manner by which these efficiency-enhancement techniques improve SCPA efficiency at PBO are presented. The efficiencies of the SCPAs with a combination of two different techniques, such as Class-G–Doherty, Class-G–TI, and TI–Doherty are examined and compared one another to determine the optimum combination of the three techniques. For a comprehensive comparison, the efficiencies of the SCPAs are

calculated, including non-ideal components, such as the switching loss (P_{SW}) of the output switch with the parasitic capacitance of the output node, transformer insertion loss (α), and output voltage division across the switch resistance (β) due to the parasitic on-resistance (R_{ON}) [11][32].

The practical DE (η) of the SCPA with the nonideal components is expressed as

$$\eta = \frac{\alpha\beta^2 P_{OUT}}{\beta P_{OUT} + P_{SC} + P_{SW}} \tag{4.5}$$

$$\beta = \frac{R_{OPT}}{R_{OPT} + R_{PAR}} \tag{4.6}$$

where R_{PAR} is the parasitic switch resistance and is $2R_{ON}$ for a differential configuration.

In Figure 4-3, the operations of an SCPA with dual-supply Class-G, Doherty, and 2-way TI techniques are presented. A pair of sub-SCPAs are utilized to apply the Doherty technique employing the main and peak PA and the 2-way TI technique using an even number of sub-SCPAs. For a reasonable comparison of the efficiencies between each efficiency-enhancement technique, the dual-supply Class-G SCPA is evaluated as a pair. The maximum output powers of the three efficiency-enhancement techniques are equal if all capacitors in the capacitor arrays are switching between V_{DD2} and V_{SS} altogether.

4.1.1 Dual-Supply Class-G SCPA

The operation of the dual-supply Class-G SCPA is exemplified in Figure 4-3(a) and detailed in [12]. From 0- to 6-dB PBO, the supply voltages of the switching capacitors in both sub-SCPAs are successively altered from V_{DD2} to V_{DD}. Preferably, V_{DD} is precisely half of V_{DD2}. If all the capacitors are switching only with V_{DD}, there is no power dissipation in the capacitor arrays, resulting in an additional efficiency peak at 6-dB PBO. V_{OUT}, P_{OUT}, P_{SC}, and P_{SW} of the differential dual-supply Class-G SCPA with two sub-SCPAs shown in Figure 4-3(a) are stated as follows:

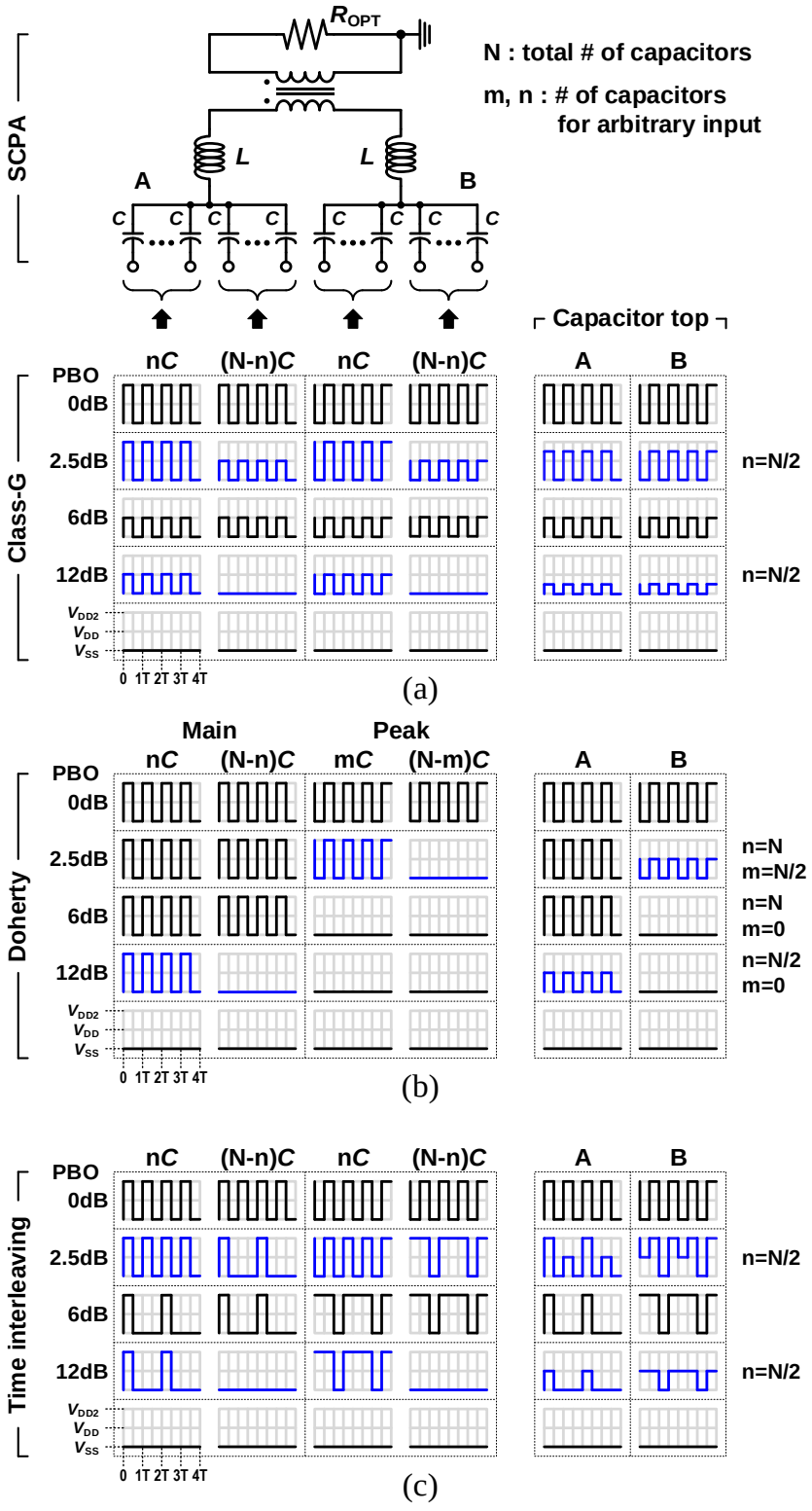


Figure 4-3. SCPA operations with two sub-SCPAs with (a) dual-supply Class-G, (b) Doherty, and (c) 2-way TI techniques. (a) can be implemented in a single SCPA, whereas (b) and (c) need two sub-SCPAs.

$$|V_{\mathrm{OUT}}| = 2\left(\frac{2}{\pi}\frac{n}{N}V_{\mathrm{DD2}} + \frac{2}{\pi}\frac{N-n}{N}V_{\mathrm{DD}}\right) = \frac{4}{\pi}\frac{N+n}{N}V_{\mathrm{DD}} \tag{4.7}$$

$$P_{\mathrm{OUT}} = \frac{1}{2}\frac{|V_{\mathrm{OUT}}|^2}{R_{\mathrm{OPT}}} = \frac{8}{\pi^2}\left(\frac{N+n}{N}V_{\mathrm{DD}}\right)^2\frac{1}{R_{\mathrm{OPT}}} \tag{4.8}$$

$$P_{\mathrm{SC}} = 2\frac{n(N-n)}{N^2}C_{\mathrm{TOT}}{V_{\mathrm{DD}}}^2 f \tag{4.9}$$

$$P_{\mathrm{SW}} = 2C_{\mathrm{SW}}\left(\frac{n}{N}{V_{\mathrm{DD2}}}^2 + \frac{N-n}{N}{V_{\mathrm{DD}}}^2\right)f \tag{4.10}$$

where n, C_{TOT}, and C_{SW} are the number of capacitors switching between V_{DD2} and V_{SS}, total capacitance of the capacitor array in each sub-SCPA, and total parasitic capacitance at all switch output nodes connected to the capacitor array in each sub-SCPA, respectively. C_{SW} comprises the overall junction capacitance and other parasitic capacitance at the switch output nodes. Here, C_{SW} is presumed to be common to V_{DD2} and V_{DD} operation modes in the same Class-G switch structure. Basically, C_{SW} of the V_{DD2} and V_{DD} operation modes can be dissimilar due to varying switch structures. P_{SW} can be assessed with a figure of merit of the output switch (f_{SW}), which is $1/(2\pi R_{\mathrm{ON}}C_{\mathrm{SW}})$ because $R_{\mathrm{ON}}C_{\mathrm{SW}}$ is constant in a certain process technology [35]. Then, P_{SW} is expressed as

$$P_{\mathrm{SW}} = \frac{1}{\pi R_{\mathrm{ON}} f_{\mathrm{SW}}}\left(\frac{n}{N}{V_{\mathrm{DD2}}}^2 + \frac{N-n}{N}{V_{\mathrm{DD}}}^2\right)f. \tag{4.11}$$

From 6-dB to the deepest PBO, the capacitors switching between V_{DD} and V_{SS} in both sub-SCPAs are successively unswitched as in the conventional SCPA. P_{SW} is given by

$$P_{\mathrm{SW}} = \frac{1}{\pi R_{\mathrm{ON}} f_{\mathrm{SW}}}\frac{n}{N}{V_{\mathrm{DD}}}^2 f \tag{4.12}$$

where n is the number of capacitors switching between V_{DD} and V_{SS}. Assuming $\alpha = 0.71$, $\beta = 0.83$ ($R_{\mathrm{ON}} = 0.1R_{\mathrm{OPT}}$), and $f_{\mathrm{SW}} = 24$ GHz, the calculated η_{IDEAL}, η, P_{SC}, and P_{SW} of the Class-G SCPA

are presented in Figure 4-4. η at 6-dB PBO is the same as that at peak P_{OUT} because P_{SW} scales well with $P_{OUT,}$ as shown in Figure 4-4.

4.1.2 Doherty SCPA

The operation of the Doherty SCPA is shown in Figure 4-3(b) and detailed in [35]. From 0 to 6-dB PBO, the capacitors switching between V_{DD2} and V_{SS} of the peaking PA are unswitched successively, whereas the main PA stays fully turned on. The unswitched capacitors are connected to the signal ground. In this way, the load impedance perceived by the main and peaking PAs is modulated from $R_{OPT}/2$ to R_{OPT} and from $R_{OPT}/2$ to 0, respectively. If all capacitors in the main and peaking SCPAs are switching with V_{DD2} and remain unswitched, respectively, then no power is dissipated in the capacitor arrays, resulting in an additional efficiency peak at 6-dB PBO. V_{OUT}, P_{OUT}, P_{SC}, and P_{SW} of the Doherty SCPA presented in Figure 4-3(b) are expressed as follows:

$$|V_{OUT}| = \frac{2}{\pi}V_{DD2} + \frac{2}{\pi}\frac{m}{N}V_{DD2} = \frac{2}{\pi}\frac{N+m}{N}V_{DD2} \tag{4.13}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left(\frac{N+m}{N}V_{DD2}\right)^2\frac{1}{R_{OPT}} \tag{4.14}$$

$$P_{SC} = \frac{m(N-m)}{N^2}C_{TOT}{V_{DD2}}^2 f \tag{4.15}$$

$$P_{SW} = \frac{1}{2\pi R_{ON} f_{SW}}\frac{N+m}{N}{V_{DD2}}^2 f \tag{4.16}$$

where m is the number of capacitors switching between V_{DD2} and V_{SS} in the peaking SCPA.

From 6-dB to the deepest PBO, the peaking SCPA is fully turned off, and the capacitors switching between V_{DD2} and V_{SS} in the main SCPA are sequentially unswitched, similar with the peaking SCPA in the 0–6-dB PBO region. P_{SW} is given by

$$P_{SW} = \frac{1}{2\pi R_{ON} f_{SW}}\frac{n}{N}{V_{DD2}}^2 f \tag{4.17}$$

where n is the number of capacitors switching between V_{DD2} and V_{SS} in the main PA. The calculated η_{IDEAL}, η, P_{SC}, and P_{SW} of the Doherty SCPA are displayed in Figure 4-4. Particularly, the efficiency at 6-dB PBO is degraded because P_{SW} stays relatively high when P_{OUT} is decreased by 6 dB, as shown in Figure 4-4.

4.1.3 2-Way TI SCPA

The operation of the 2-way TI SCPA is shown in Figure 4-3(c), and the underlying theory is presented in [40]. The normal 50% duty-cycle LO signal can be split into two time-interleaved 25% duty-cycle LO signals operating at half frequency, as shown in Figure 4-1. The sum of the harmonics of the time-interleaved LO signals matches that of the normal LO signal [40]. The harmonic analysis shows that the split and time-interleaved LO signals can produce 6 dB lower P_{OUT} without any spurs. For example, when the normal LO signals in both sub-SCPAs are substituted with the time-interleaved LO signals, P_{OUT} of the 2-way TI SCPA decreases by 6 dB, as shown in Figure 4-3(c). If all the SCPA cells are functioning in a time-interleaved manner, then there will be no power dissipation in the capacitor arrays, resulting in an additional efficiency peak at 6-dB PBO. The 2-way TI operation can provide not only an additional efficiency peak but also a continuous efficiency curve between the efficiency peaks, similar with the Class-G and Doherty operations. From 0- to 6-dB PBO, the seamless efficiency curve can be attained by sequentially altering the toggling signals of the capacitors from the normal LO signals to the time-interleaved LO signals, as shown in Figure 4-3(c). V_{OUT}, P_{OUT}, P_{SC}, and P_{SW} of the 2-way TI SCPA displayed in Figure 4-3(c) are expressed as follows:

$$|V_{OUT}| = 2\left(\frac{2}{\pi}\frac{n}{N} + \frac{1}{\pi}\frac{N-n}{N}\right)V_{DD2} = \frac{2}{\pi}\frac{N+n}{N}V_{DD2} \tag{4.18}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{2}{\pi^2}\left(\frac{N+n}{N}V_{DD2}\right)^2\frac{1}{R_{OPT}} \tag{4.19}$$

$$P_{\mathrm{SC}} = 2\frac{n(N-n)}{N^2}C_{\mathrm{TOT}}{V_{\mathrm{DD2}}}^2\frac{f}{2} \tag{4.20}$$

$$P_{\mathrm{SW}} = \frac{1}{\pi R_{\mathrm{ON}} f_{\mathrm{SW}}}\frac{N+n}{N}{V_{\mathrm{DD2}}}^2\frac{f}{2} \tag{4.21}$$

where n is the number of capacitors switching between V_{DD2} and V_{SS} with the normal LO signal in a sub-SCPA.

From 6-dB to the deepest PBO, the number of capacitors switching with the time-interleaved LO signals in both sub-SCPAs is sequentially decreased, whose operation is similar as in the conventional SCPA. P_{SW} is given by

$$P_{\mathrm{SW}} = \frac{1}{\pi R_{\mathrm{ON}} f_{\mathrm{SW}}}\frac{\mathrm{n}}{\mathrm{N}}{V_{\mathrm{DD2}}}^2\frac{f}{2} \tag{4.22}$$

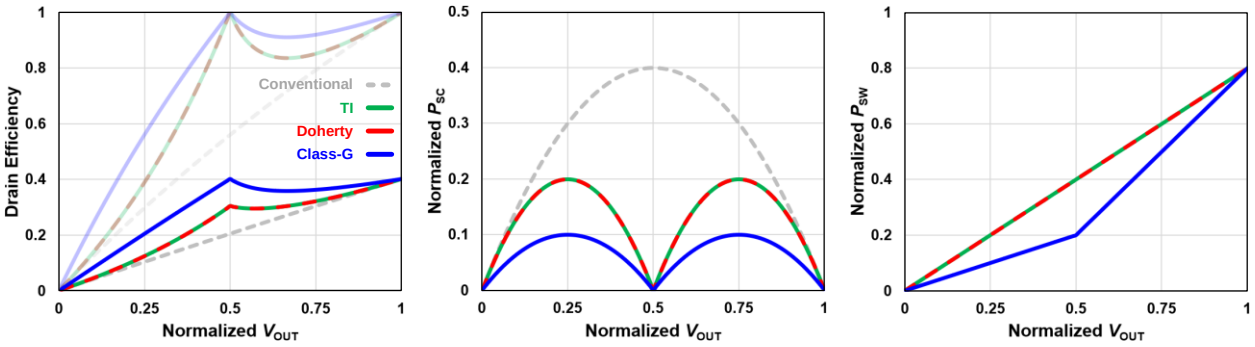
where n is the number of capacitors switching between V_{DD2} and V_{SS} with the time-interleaved LO signals in a sub-SCPA. The calculated η_{IDEAL}, η, P_{SC}, and P_{SW} of the 2-way TI SCPA are presented in Figure 4-4. The efficiency at 6-dB PBO is degraded because P_{SW} remains relatively high when P_{OUT} is reduced by 6 dB, as shown in Figure 4-4.

4.1.4 Evaluation of the Efficiency-Boosting Techniques

η_{IDEAL} and η of the SCPAs with a single efficiency-enhancement technique are presented in Figure 4-4(a). The transparent and opaque solid lines represent η_{IDEAL} and η, respectively, and the blue, red, and green colors stand for the dual-supply Class-G, Doherty, and 2-way TI SCPAs, respectively. The Doherty and 2-way TI SCPAs have similar efficiency, as discussed in Chapter 4.1.2 and 4.1.3. The efficiency of the conventional SCPA indicated by the gray dotted line is also presented for the comparison.

Among the SCPAs, the Class-G SCPA shows the highest DE at PBO due to the least P_{SC}

and P_{SW}, as shown in Figure 4-4(b) and (c). P_{SC} of the Class-G SCPA is exactly half that of the Doherty and 2-way TI SCPAs. For all SCPAs, there is no P_{SC} at half of the maximum V_{OUT}, resulting in an additional efficiency peak at 6-dB PBO.



(a) (b) (c)

Figure 4-4. Comparison of the dual-supply Class-G, Doherty, and 2-way TI SCPAs in terms of (a) drain efficiency, (b) dynamic power dissipation in the capacitor array (P_{SC}), and (c) switching loss (P_{SW}) (Q_{LOAD} = 1, α = 0.71, β = 0.83, R_{ON} = 0.3 Ω, f_{SW} = 24 GHz, and f = 2.4 GHz).

For the dual-supply Class-G SCPA, in the 0- to 6-dB PBO region, P_{SW} changes linearly from the maximum P_{SW} at 0-dB PBO to a quarter of the maximum P_{SW} at 6-dB PBO, representing a noteworthy improvement in P_{SW} at PBO, as shown in the blue solid line in Figure 4-4(c). A lower P_{SW} is attained because the supply voltage of all SCPA cells sequentially changes from V_{DD2} to V_{DD}, assuming identical C_{SW} for the V_{DD2} and V_{DD} operation modes. It results in the same η at 6-dB PBO with that of the peak P_{OUT}. From 6-dB to the deepest PBO, P_{SW} also decreases in proportion to V_{OUT} from a quarter of maximum P_{SW} to 0. Meanwhile, for the Doherty and 2-way TI SCPAs, P_{SW} decreases in proportion to V_{OUT} from the 0-dB PBO to the deepest PBO as in the conventional SCPA, as shown in the red and green dashed lines in Figure 4-4(c), which results in a more substantial roll-off of the efficiency curve at PBO. Thus, η at 6-dB PBO is always lower than η at peak P_{OUT} in the Doherty and 2-way TI SCPAs, as shown in Figure 4-4(a).

4.2 Output Power and Efficiency of the Multimode Switched-Capacitor Power Amplifier

Two distinct efficiency-enhancement techniques can be combined to produce three additional efficiency peaks at 2.5-, 6-, and 12-dB PBO [41]. Techniques A and B can be combined in two ways: a technique can be used as a local efficiency-enhancement technique, while the other technique can be used as a global one, i.e., A-based B and B-based A, as shown in Figure 4-5. In the A-based B, A and B are presented as a local and global efficiency-enhancement technique, respectively. The transition at 6-dB PBO integrates the change in the global efficiency-enhancement technique B, whereas the local enhancement technique A is employed within 0–6-dB and deeper than 6-dB PBOs.

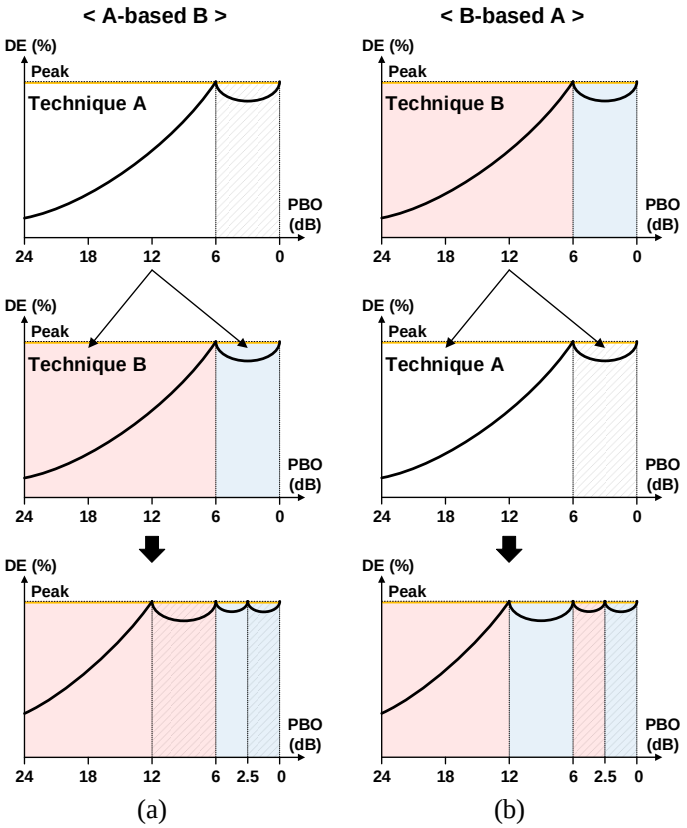


Figure 4-5. Combinations of the two single efficiency-enhancement techniques: (a) A-based B and (b) B-based A.

4.2.1 Dual-Supply Class-G Doherty SCPA

For the dual-supply Class-G and Doherty techniques, the Class-G-based Doherty approach using Doherty as a global efficiency-enhancement technique was introduced in prior papers [15] and [41]. In this chapter, the Doherty-based Class-G approach is introduced, and the two techniques are compared in terms of PBO efficiency.

The SCPA operations with the two different combinations are presented in Figure 4-6(a). From 0- to 2.5-dB PBO, for both combinations, the supply voltages of the switching capacitors in the peaking PA are sequentially changed from V_{DD2} to V_{DD}. When all capacitors in the main and peaking PAs are switching only with V_{DD2} and V_{DD}, respectively, there is no power dissipation in the capacitor arrays, resulting in an additional efficiency peak at 2.5-dB PBO.

From 2.5- to 6-dB PBO, for the Class-G-based Doherty case, the switching capacitors in the peaking PA are sequentially unswitched. At 6-dB PBO, the main and peaking PAs are fully turned on and off respectively, demonstrating no power dissipation in the capacitor arrays and an additional efficiency peak. Meanwhile, for the Doherty-based Class-G case, the supply voltages of the switching capacitors in the main PA are sequentially changed from V_{DD2} to V_{DD}. When all capacitors in the main and peaking PAs are switched only with V_{DD}, there is no power dissipation in the capacitor arrays resulting in an additional efficiency peak at 6-dB PBO.

From 6- to 12-dB PBO, for the Class-G-based Doherty case, only the main PA operates in the Class-G mode. For the Doherty-based Class-G case, the main and peaking PAs operate in Doherty configuration with only V_{DD} supply voltage. At 12-dB PBO, for both cases, the main PAs are fully turned on with V_{DD}, and peaking PAs are turned off. Therefore, no power is dissipated in the capacitor arrays, resulting in an additional efficiency peak. Below 12-dB PBO, the number of operating cells gradually decreases as in the conventional SCPA.

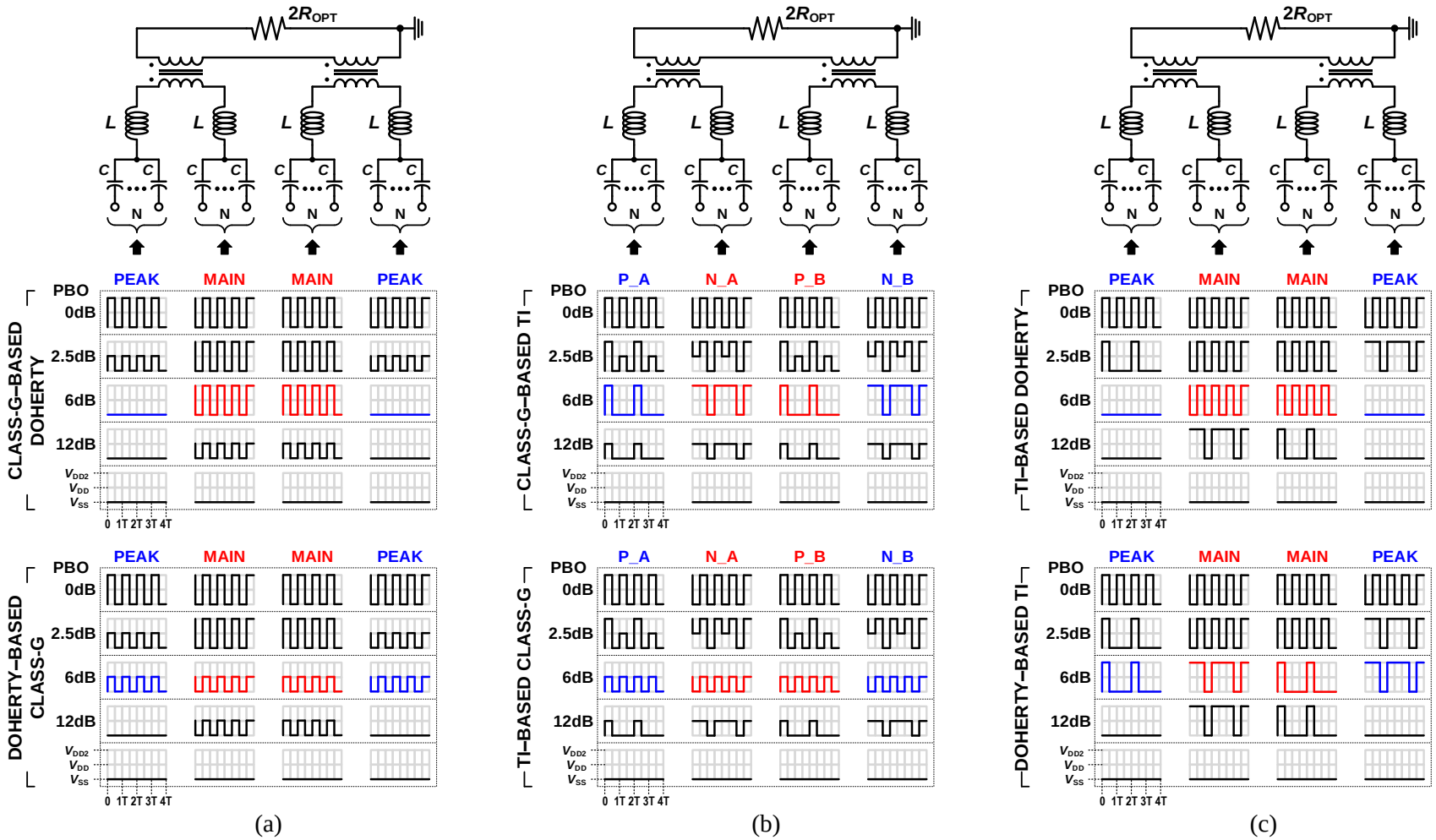


Figure 4-6. SCPA operations with four sub-SCPAs with the following combinations: (a) dual-supply Class-G and Doherty, (b) dual-supply Class-G and 2-way TI, and (c) 2-way TI and Doherty techniques. (a) and (b) can be implemented with two sub-SCPAs, and (c) needs four sub-SCPAs.

Because the SCPA operation change according to the four PBO regions, different power losses need to be considered for each PBO region to calculate η. P_{SC} of both combinations can be calculated using (4.9) for each region. P_{SW} of the Class-G-based Doherty combination follows (4.11) in the 0–2.5-dB and 6–12-dB PBO regions, and (4.12) in the 2.5–6-dB and deeper-than-12-dB PBO regions. Furthermore, P_{SW} of the Doherty-based Class-G combination follows (4.11) and (4.12) in the 0–6-dB and deeper-than-6-dB PBO regions, respectively. The calculated η, P_{SC}, and P_{SW} of the dual-supply Class-G Doherty SCPA are presented in Figure 4-7.

4.2.2 Dual-Supply Class-G 2-Way TI SCPA

The SCPA operations with the dual-supply Class-G and 2-way TI are shown in Figure 4-6(b). For the dual-supply Glass-G 2-way TI architecture, dynamic supply voltage or the dynamic voltage difference for the switching capacitors changes between V_{DD2} and V_{DD} every other normal LO cycle. From 0- to 2.5-dB PBO, for Class-G-based TI and TI-based Class-G cases, the dynamic supply voltages for the switching capacitors are sequentially changed in a time-interleaved manner between the sub-SCPAs, as shown in Figure 4-6(b). When all capacitors in each capacitor array are switching with the same dynamic supply voltage, there is no power dissipation in the capacitor array resulting in an additional efficiency peak at 2.5-dB PBO.

From 2.5- to 6-dB PBO, for the Class-G-based TI case, the toggling signals of the capacitors operating with the dynamic supply voltage are sequentially changed to the time-interleaved LO signals toggling between V_{DD2} and V_{SS}. At 6-dB PBO, all sub-SCPAs are fully turned on with the time-interleaved LO signals toggling between V_{DD2} and V_{SS}, and the sub-SCPAs have no power consumption in the capacitor arrays, resulting in an additional efficiency peak. Meanwhile, for the TI-based Class-G case, the toggling signals of the capacitors operating with the dynamic supply voltage are sequentially changed to the normal LO signals toggling between V_{DD} and V_{SS}. When

all capacitors in the SCPAs are toggling only with the normal LO signal with V_{DD}, no power is dissipated in the capacitor array, resulting in an additional efficiency peak at 6-dB PBO.

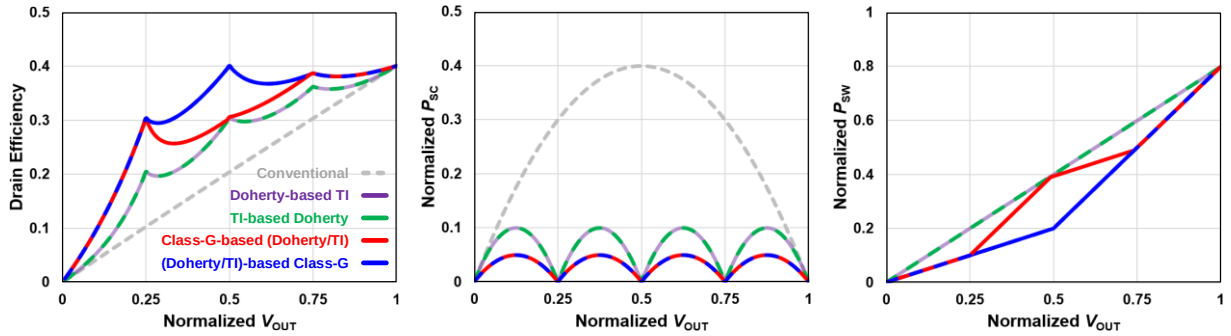
From 6- to 12-dB PBO, for the Class-G-based TI case, the supply voltages of the switching capacitors in all sub-SCPAs are sequentially changed from V_{DD2} to V_{DD}. For the TI-based Class-G case, the normal LO signals of the capacitors are sequentially changed to the time-interleaved LO signals. At 12-dB PBO, for both cases, the sub-SCPAs are fully turned on with the time-interleaved LO signals. Therefore, no power is dissipated in the capacitor array, resulting in an additional efficiency peak. Below 12-dB PBO, the number of operating cells gradually decreases as in the conventional SCPA.

P_{SC} of both cases can be calculated using (4.9) for each PBO region. The amplitude of the toggling signal of the switching capacitors in all sub-SCPAs is sequentially changed as much as V_{DD}. For the same reason as the P_{SC} calculation, P_{SW} of the Class-G-based TI case can be calculated using (4.11) in the 0–2.5-dB and 6–12-dB PBO regions, and (4.12) in the 2.5–6-dB and deeper-than-12-dB PBO regions. Likewise, P_{SW} of the TI-based Class-G case can be obtained using (4.11) and (4.12) in the 0–6-dB and deeper-than-6-dB PBO regions, respectively. The calculated η, P_{SC}, and P_{SW} of the dual-supply Class-G 2-way TI SCPA are presented in Figure 4-7.

4.2.3 2-Way TI Doherty SCPA

The operations of the 2-way TI Doherty SCPAs illustrated in Figure 4.6(c) are comparable to those of the dual-supply Class-G Doherty SCPAs. The transition between the normal LO and time-interleaved LO signals in the 2-way TI Doherty SCPAs can be similarly understood as the transition between V_{DD2} and V_{DD} in the dual-supply Class-G Doherty SCPAs presented in Chapter 4.2.1. Here, the LO signals toggle between V_{DD2} and V_{SS}.

The TI-based Doherty and Doherty-based TI combinations have the same P_{SC} and P_{SW}. P_{SC} can be calculated using (4.20) for each PBO region. P_{SW} of the TI-based Doherty case follows (4.21) in the 0–2.5-dB and 6–12-dB PBO regions and (4.22) in the 2.5–6-dB and deeper-than-12-dB PBO regions. Furthermore, P_{SW} of the Doherty-based TI case follows (4.21) and (4.22) in the 0–6-dB and deeper-than-6-dB PBO regions, respectively. The calculated η, P_{SC}, and P_{SW} of the 2-way TI Doherty SCPA are presented in Figure 4-7.



(a) (b) (c)

Figure 4-7. Comparison of the dual-supply Class-G Doherty, dual-supply Class-G 2-way TI, and 2-way TI Doherty SCPAs in terms of (a) drain efficiency, (b) dynamic power dissipation in the capacitor array (P_{SC}), and (c) switching loss (P_{SW}) (Q_{LOAD} = 1, α = 0.71, β = 0.83, R_{ON} = 0.3 Ω, f_{SW} = 24 GHz, and f = 2.4 GHz).

4.2.4 Multimode SCPA with the Three Efficiency-Enhancement Techniques

As shown in Figure 4-7(a), the Doherty/TI-based Class-G cases show the highest η at PBO among the six combinations. The Class-G-based Doherty/TI cases also have the advantages of the Class-G technique, but both demonstrate less PBO efficiency than that of the Doherty/TI-based Class-G cases, as shown in Figure 4-7(a), due to increased P_{SW}, as shown in Figure 4-7(c). The 2-way TI and Doherty combinations show the lowest η at PBO because it consumes the largest P_{SC} and P_{SW} due to the use of a single supply voltage V_{DD2} for the entire PBO region. Furthermore, among the Doherty/TI-based Class-G cases, the TI-based Class-G can be less efficient because the supply voltage changes every other normal LO cycle.

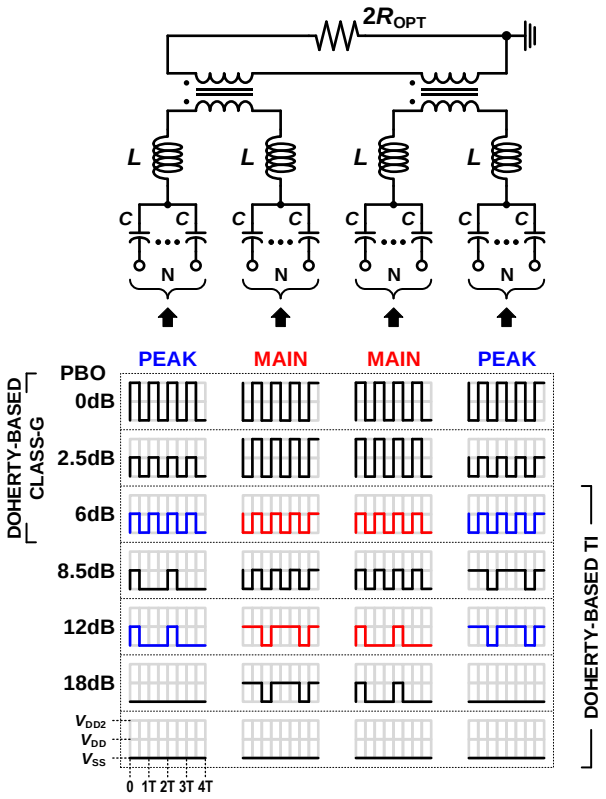
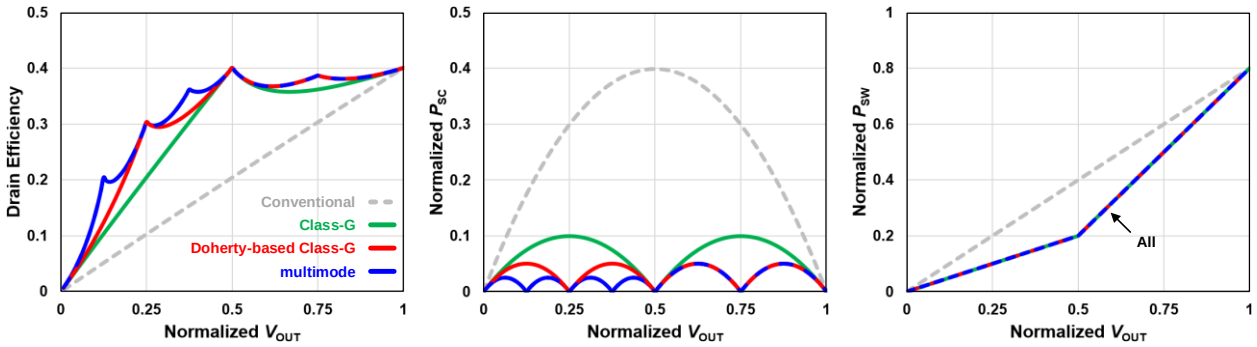


Figure 4-8. Multimode SCPA operation.

For this reason, the Doherty-based Class-G is chosen as a base efficiency-enhancement technique, and the 2-way TI technique is applied in the selective PBO region for a highly-efficient multimode SCPA operation. In this design, the 2-way TI technique is applied only to deeper than 6-dB PBO because high efficiency can be achieved in the 0–6dB PBO region even without the TI considering the seamless efficiency curve between the peaks. The combination of the three efficiency-enhancement techniques provides six efficiency peaks at 0-, 2.5-, 6-, 8.5-, 12-, 18-dB PBOs. However, a total of eight efficiency peaks can theoretically be realized with a combination of the three efficiency-enhancement techniques: dual-supply Class-G, Doherty, and 2-way TI. The operation of the multimode SCPA is illustrated in Figure 4-8, and the calculated η, P_{SC}, and P_{SW} of the multimode SCPA are compared to those of the Class-G and Doherty-based Class-G SCPAs in Figure 4-9.



(a) (b) (c)

Figure 4-9. Comparison between the multimode, Doherty-based Class-G, and Class-G SCPAs in terms of (a) drain efficiency, (b) dynamic power dissipation in the capacitor array (P_{SC}), and (c) switching loss (P_{SW}) (Q_{LOAD} = 1, α = 0.71, β = 0.83, R_{ON} = 0.3 Ω, f_{SW} = 24 GHz, and f = 2.4 GHz).

4.3 Circuit Implementation

A block diagram of the multimode multi-efficiency-peak SCPA is shown in Figure 4-10(a). In this design, four differential sub-SCPAs are combined with a parallel–series transformer. The 10-bit digital PA consists of 5-bit unary and 5-bit binary cell groups for the optimized area and power consumption in a 65-nm CMOS process. More unary bits are beneficial for better linearity over a wide P_{OUT} range because the matching between the unary-weighted cells is significantly better than that of the binary-weighted cells. However, the number of unary cells doubles with each additional unary bit, which leads to high power consumption and large area. In more advanced CMOS technology, a larger number of unary bits can be employed without a significant area and power consumption penalty for an improved linearity.

Each sub-SCPA cell has a linear single-supply current-reuse Class-G switch. An LO signal restoration technique is proposed to reduce the area and power consumption for LO signal distribution. Figure 4-10(b) shows the operation of the prototype multimode multi-efficiency-peak SCPA. In this work, six efficiency peaks with continuous transitions are realized by combining the

dual-supply Class-G, Doherty, and 2-way TI techniques. Even if the PA operation is explained in a single-ended mode, a differential PA architecture is employed for an improved linearity. Moreover, the two transformer inputs are balanced because unbalanced inputs in an unideal transformer power-combining network can result in an unideal energy loss and efficiency degradation in the PA [30][35].

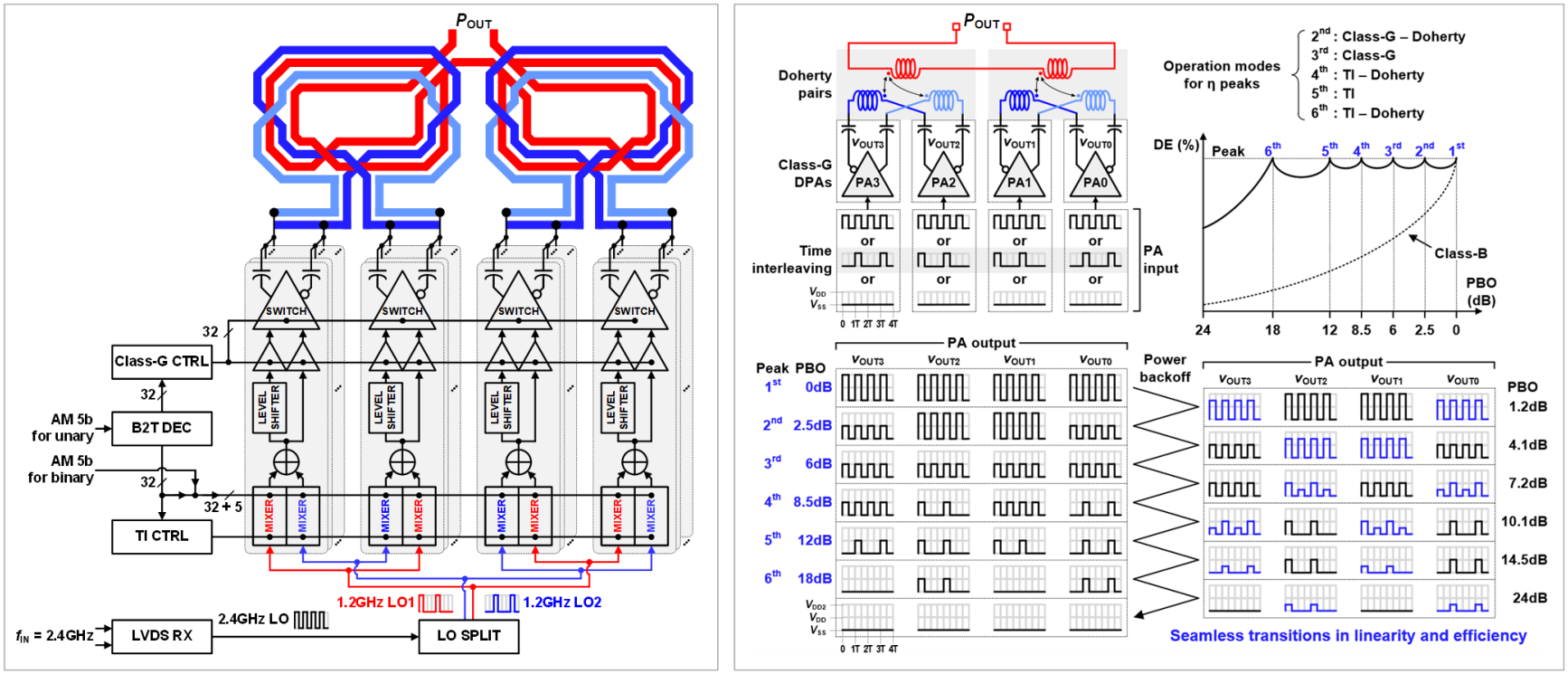


Figure 4-10. (a) Overall architecture and (b) operation of the proposed multimode SCPA.

4.3.1 Single-Supply Current-Reuse Class-G Switch

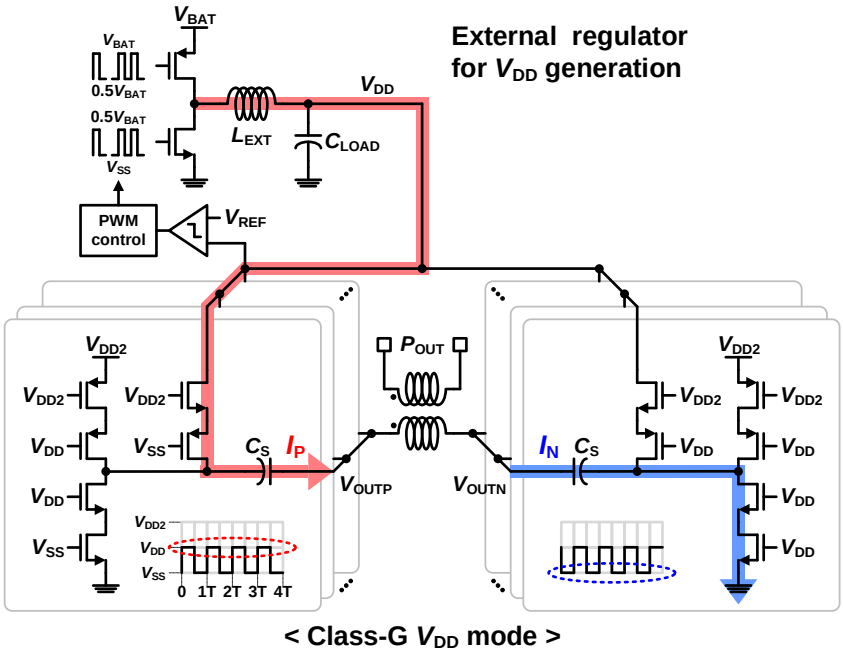
In Figure 4-11(a), a conventional dual-supply Class-G switch is presented [12]. Conventional Class-G techniques necessitate various supply voltages for multiple efficiency peaks. A supplementary supply voltage requires an additional accurate, high-current regulator, which results in bigger complexity and system cost. Moreover, in conventional Class-G architectures, any supply voltage mismatch between multiple supply voltages can result in a linearity degradation.

The Class-G switch in Figure 4-11(b), initially proposed in [33], can provide a high-accuracy dual-supply Class-G operation from a single high-current supply voltage, V_{DD2}, by dividing a Class-G cell into two, taking the average of two split cells at the output using two split capacitors, and reusing the current from V_{DD2} for V_{DD}.

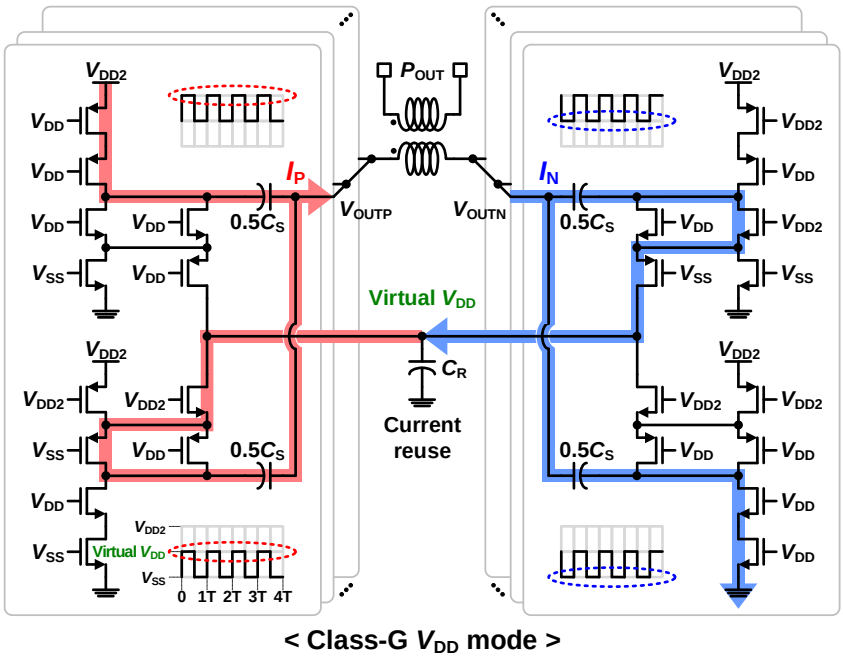
As shown in Figure 4-11(b), the sinking current of the upper switches between V_{DD2} and V_{DD} can be reused as the sourcing current of the lower switches between V_{DD} and V_{SS}. Therefore, there is no high current flow required for V_{DD} from an external PMU or voltage supply. The current reuse occurs between the upper and lower switches and also between the differential architectures every half-RF cycle. In the proposed prototype, reservoir capacitors are added to stabilize the virtual V_{DD}, as shown in Figure 4-11(b), and the external voltage supply for V_{DD} is removed. A small low-dropout (LDO) regulator can be used to accurately regulate V_{DD}, but the precise control of V_{DD} is not required due to the inherent accuracy of the proposed architecture.

The proposed Class-G switch is insensitive to the supply voltage mismatch using the average of $V_{DD2}–V_{DD}$ and $V_{DD}–V_{SS}$ for the V_{DD} mode. Any mismatch voltage between V_{DD2} and V_{DD} can be averaged and canceled out at the capacitor summing node, as shown in Figure 4-12(a) [33]. As a result, the virtual V_{DD} does not need to be exactly half of V_{DD2}. Moreover, a remaining phase mismatch can be compensated through the dynamic signal delay control by employing separate

signal paths with different delays according to the Class-G operation, as shown in Figure 4-12(b) [33].

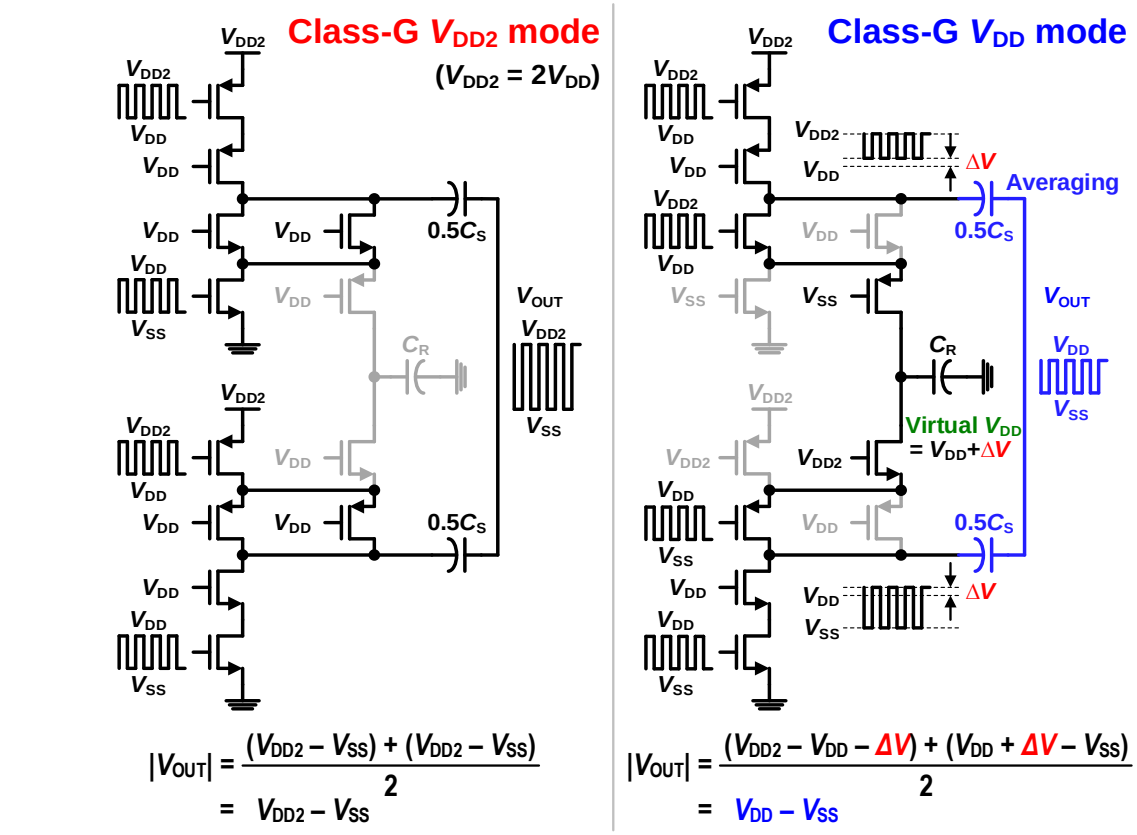


(a)

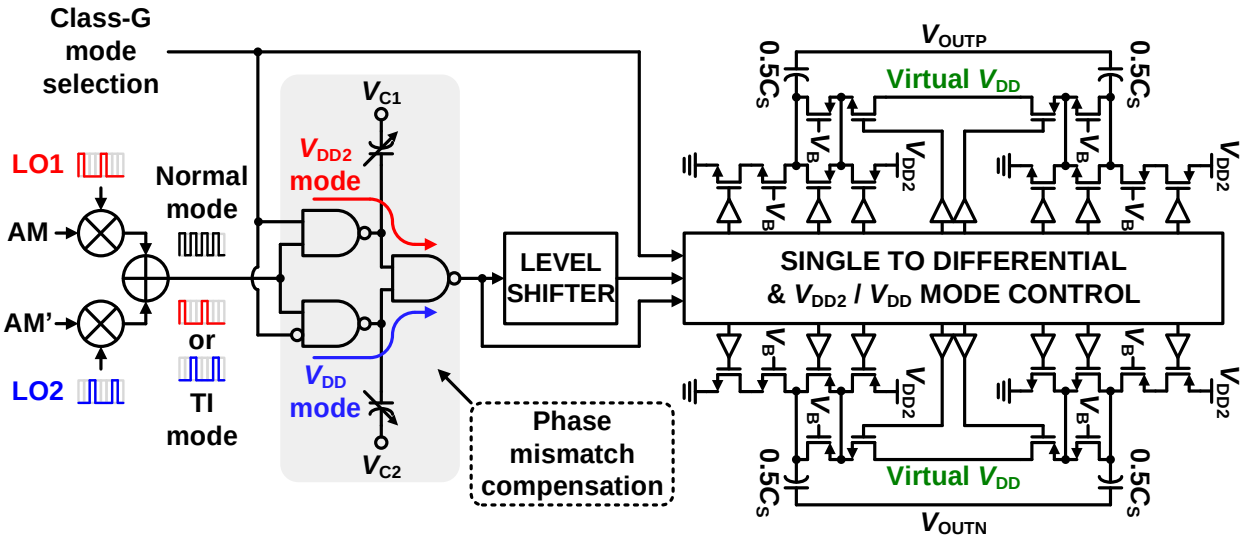


(b)

Figure 4-11. Class-G switches: (a) conventional and (b) proposed switch structures.



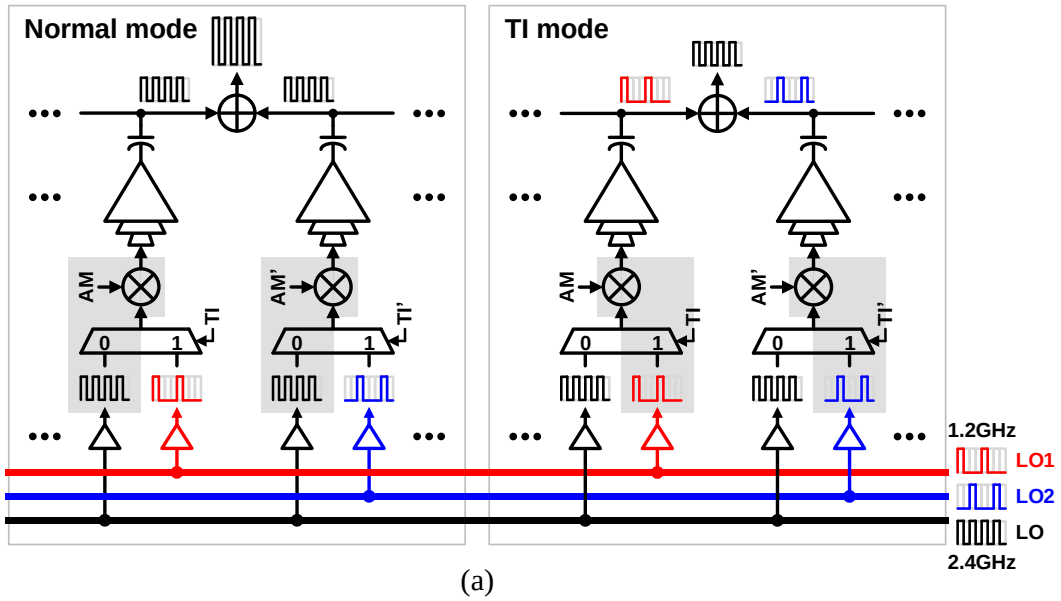
(a)



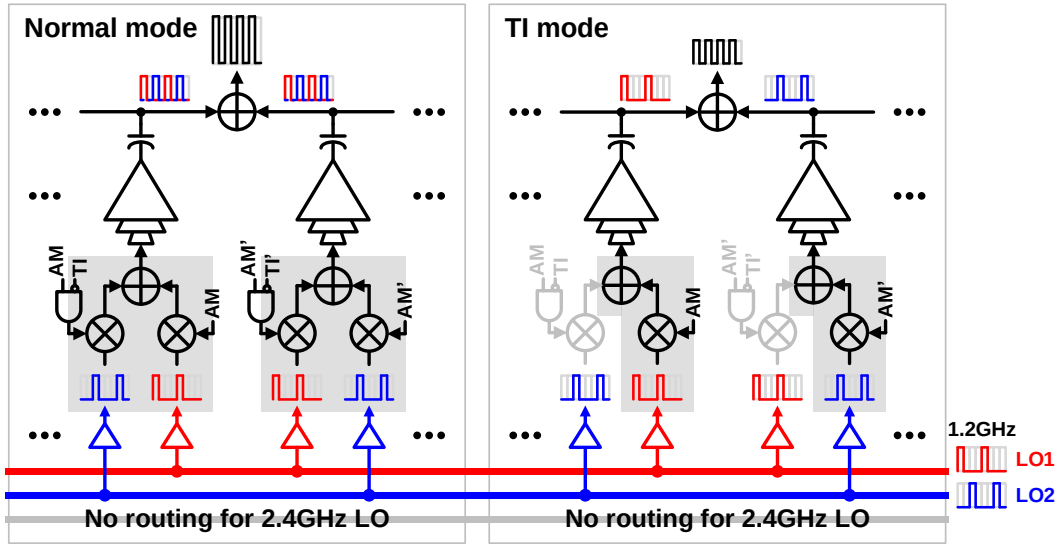
(b)

Figure 4-12. (a) Supply voltage mismatch insensitive Class-G switch and (b) dynamic path delay control for phase mismatch compensation.

4.3.2 LO Signal Distribution



(a)



(b)

Figure 4-13. LO signal distribution: (a) conventional and (b) proposed the LO signal restoration technique.

The LO signal distribution is important to the linearity of the time-interleaved digital PA and needs additional area and power consumption. Distributing normal LO signal and time-interleaved LO signals necessitates additional area and power consumption, as shown in Figure 4-13(a) [40].

In this prototype, the LO signal restoration technique is suggested to realize a small area and low power consumption, as shown in Figure 4-13(b). A normal LO signal is synthesized from the two time-interleaved LO signals at each SCPA cell. In this case, the area and power consumption can be significantly reduced because only the time-interleaved LO signals need to be distributed.

For an accurate normal LO signal synthesis and linear TI operation, a precise timing matching between the time-interleaved LO signals is required. The timing mismatches between the time-interleaved LO signals cause undesired in-band and out-of-band nonlinearities. Because the time-interleaved LO signals are generated from the same input LO signal, the precise matching between the time-interleaved LO signals can be realized with a symmetrical signal path design.

4.4 Measurement Results

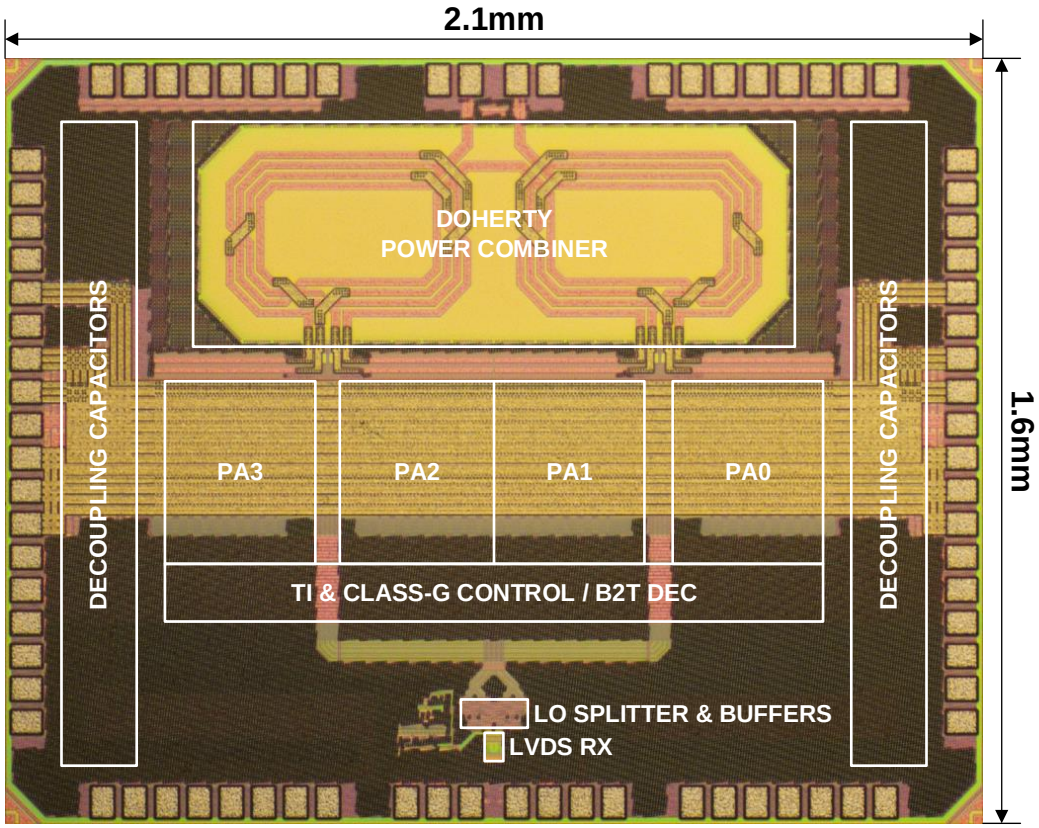


Figure 4-14. Chip micrograph.

Figure 4-14 shows a chip micrograph of the fully integrated multimode multi-efficiency-peak SCPA. The prototype fabricated in a 65-nm RF CMOS process occupies 2.1 × 1.6 mm^2, including a power-combing transformer, four sub-SCPAs, a low-voltage differential signaling (LVDS) receiver, time-interleaved LO signals generator, decoupling capacitors, and wire-bonding pads. Four differential SCPAs are combined with a parallel–series transformer to realize a Doherty operation and 10-bit resolution. Only a single supply voltage of 2.5 V is used to generate an output power in the Class-G switch.

4.4.1 CW Signal Measurement

The DE, AM–AM, and AM–PM are measured with a continuous-wave (CW) signal at 2.4 GHz. The measured DE versus P_{OUT} is shown in Figure 4-15. The prototype SCPA delivers a peak P_{OUT} of 30.0 dBm with a peak DE of 40.2% at 2.4 GHz. With an efficient combination of the dual-supply Class-G, Doherty, and 2-way TI techniques, six efficiency peaks with continuous efficiency curves between the peaks are realized down to 18-dB PBO. The prototype achieves DE (normalized DE) of 40.2% (100%), 37.9% (94.3%), 38.8% (96.3%), 36.3% (90.2%), 29.4% (73.0%), and 19.7% (48.9%) at 0-, 2.5-, 6-, 8.5-, 12-, and 18-dB PBOs, respectively. The proposed techniques substantially improve the efficiency both at and between the peaks for a wide range of P_{OUT}. Further DE enhancement can be realized in advanced fine line CMOS technology due to the less parasitic capacitance, less on-resistance, and reduced crowbar current in switches.

The measured AM–AM and AM–PM versus the normalized input code are shown in Figure 4-16. Due to the seamless transitions between the operation modes, there is no abrupt nonlinearity. The measured AM–PM distortion is less than ±1°, indicating an excellent linearity.

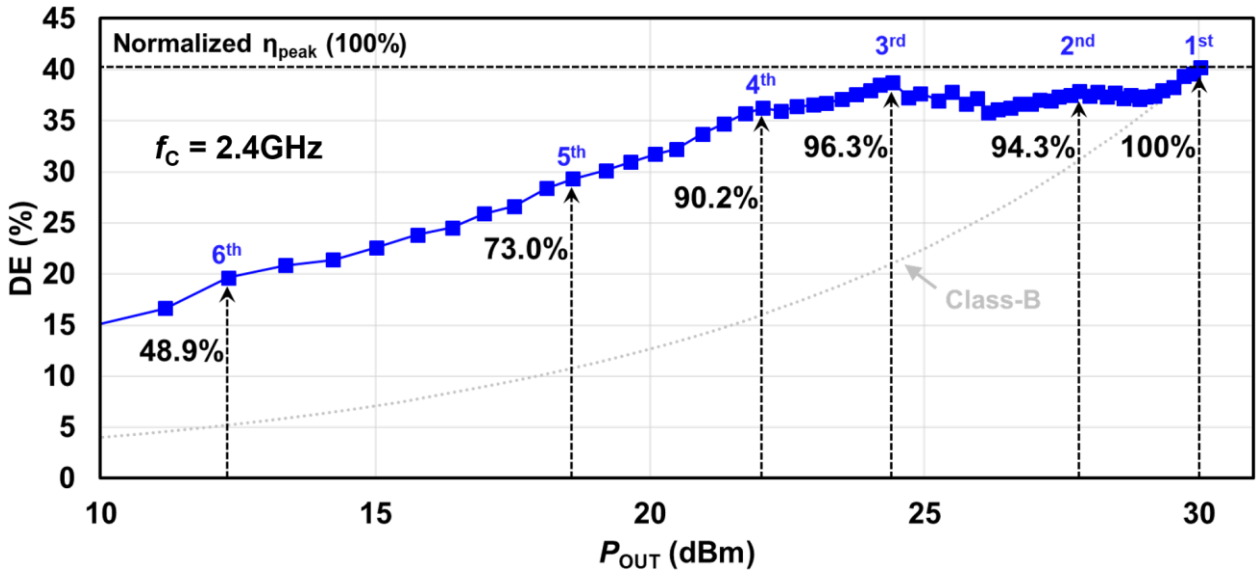


Figure 4-15. Measured DE vs. P_{OUT} for a CW signal.

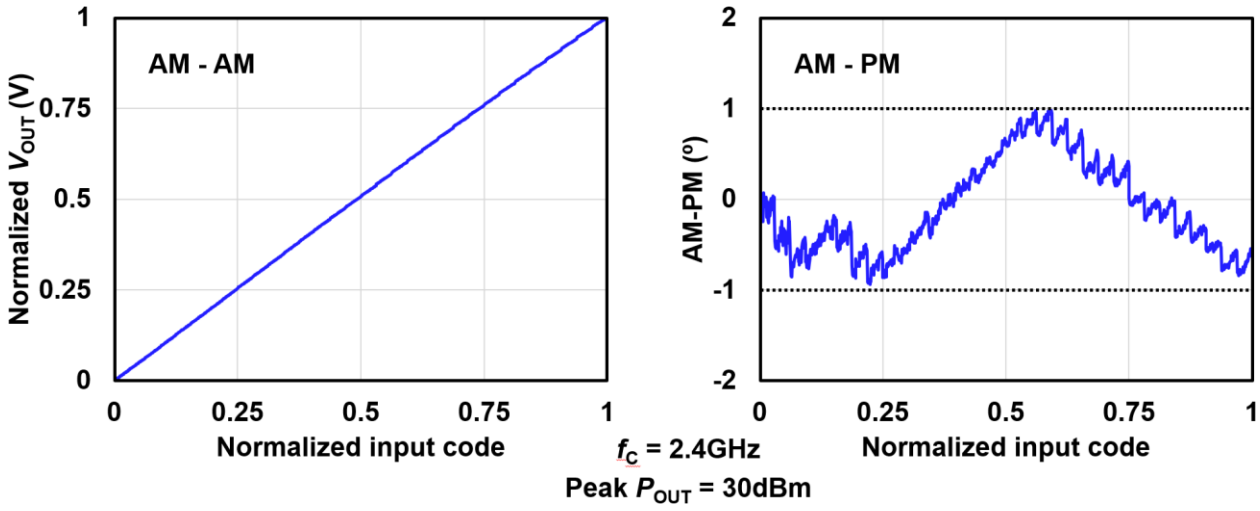


Figure 4-16. Measured AM–AM and AM–PM vs. normalized input code for a CW signal.

4.4.2 Modulated Signal Measurement

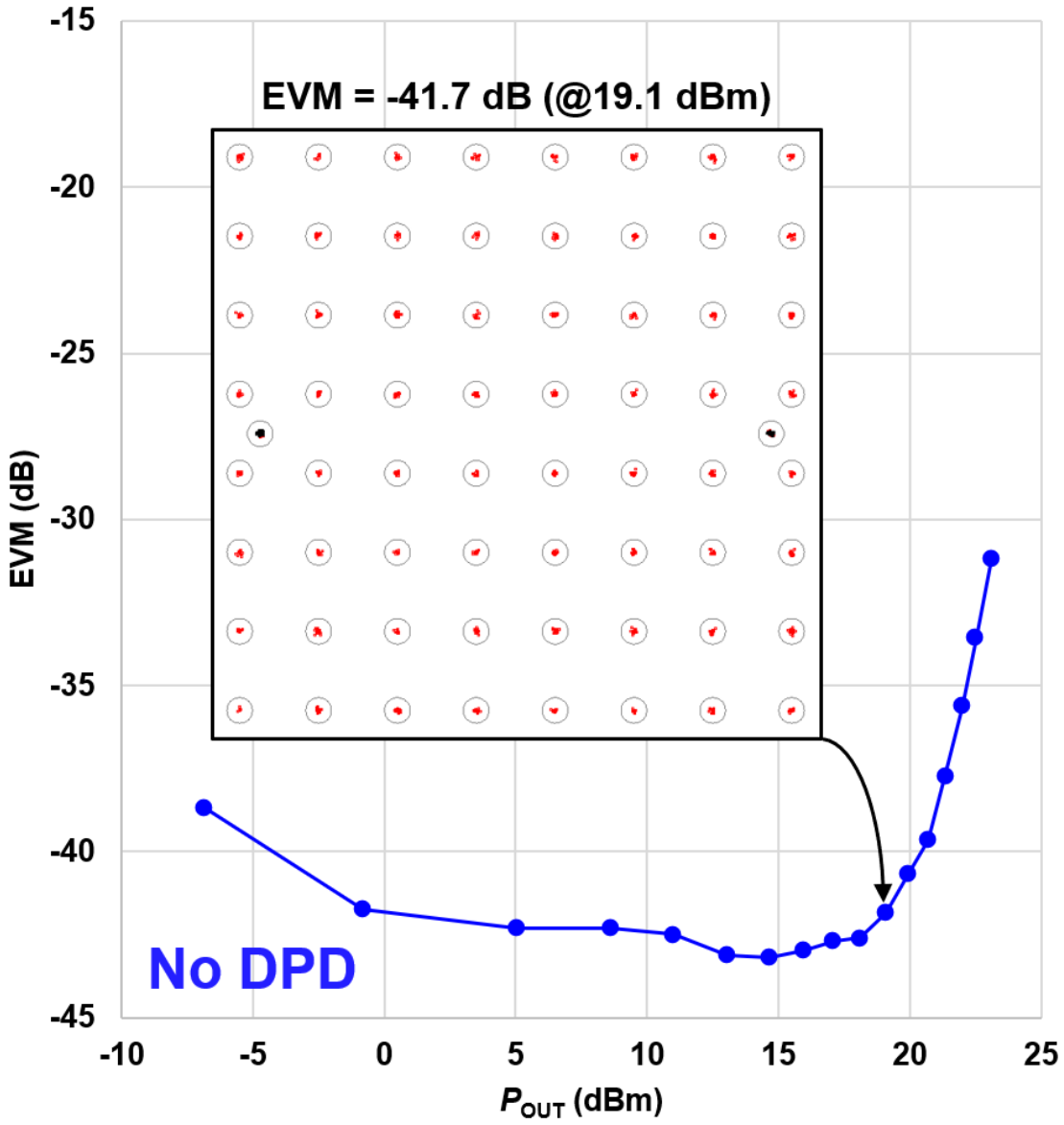


Figure 4-17. EVM vs. average P_{OUT} measured with 10-MHz 64-QAM OFDM signal.

Figure 4-17 illustrates the constellation and EVM versus the average P_{OUT} measured with a 10-MHz 64-QAM OFDM signal with a PAPR of 10.9 dB. The prototype demonstrates an excellent linearity better than –40-dB EVM over around 25-dB P_{OUT} range without any digital pre-distortion (DPD). It achieves –41.7-dB EVM at an average P_{OUT} of 19.1 dBm, and the EVM is degraded above 19.1-dBm due to the hard clipping of the modulated signal.

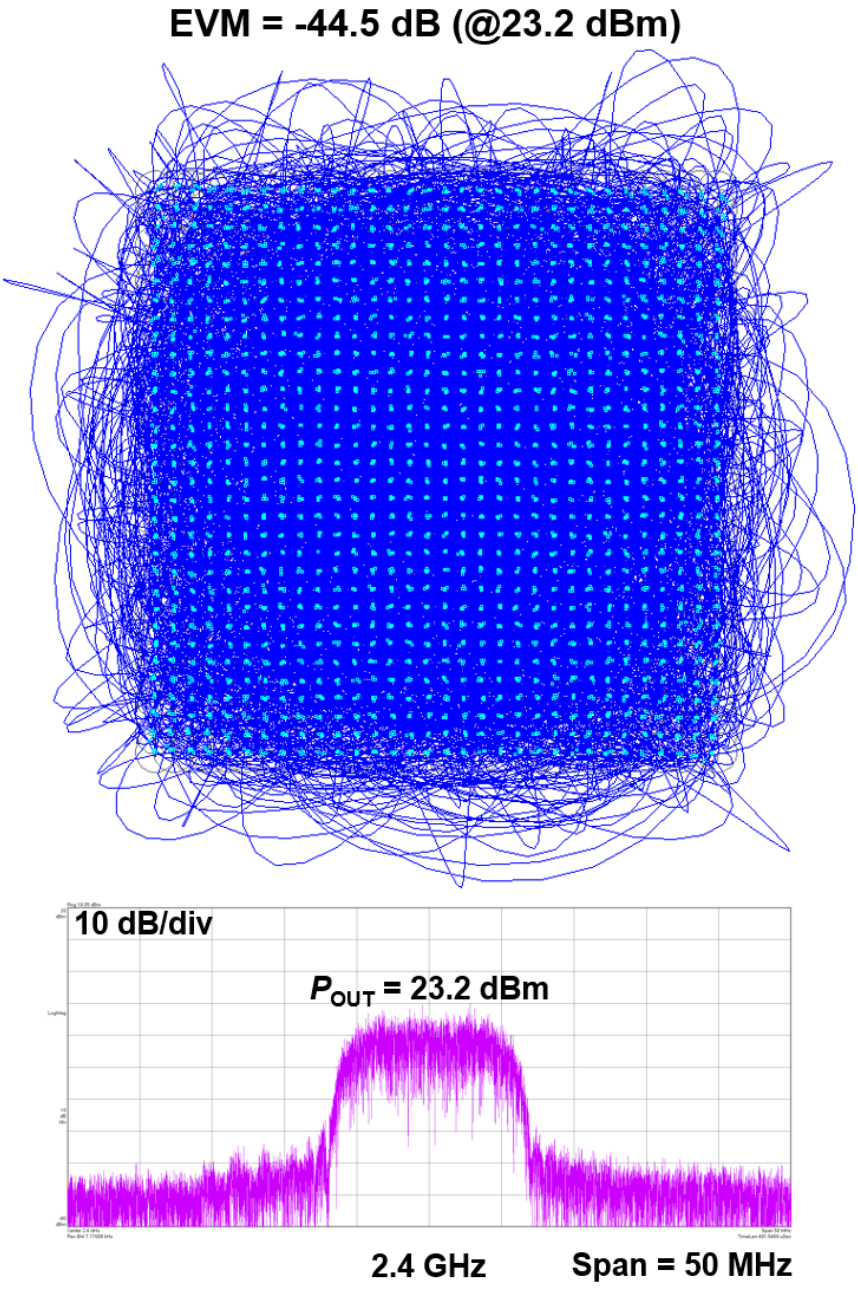


Figure 4-18. EVM vs. average P_{OUT} measured with a 10-MHz single-carrier 1024-QAM signal.

Figure 4-18 demonstrates the measured constellation and close-in frequency spectrum with a 10-MHz single-carrier 1024-QAM signal with 6.8-dB PAPR. The prototype attains an excellent EVM of –44.5 dB and a clear constellation at a high average P_{OUT} of 23.2 dBm without any DPD. It shows no sign of any substantial AM–AM and AM–PM distortions in conventional

transconductance-based PAs. The measured data evidently prove the excellent linearity of the single-supply current-reuse Class-G technique and digital PA architecture based on SCPA.

4.5 Summary

A multimode multi-efficiency-peak SCPA is implemented in a 65-nm RF CMOS process. A multimode operation is proposed to attain multiple efficiency peaks with continuous efficiency curves between the peaks in the PBO region. The combinations of the dual-supply Class-G, Doherty, and 2-way TI techniques are employed in an efficient manner to maximize PBO efficiency. Six outstanding efficiency peaks are realized. A single-supply current-reuse Class-G switch is presented to allow a highly linear Class-G operation without any external supply voltage regulators. Moreover, an LO signal restoration technique is suggested to lessen the power dissipation and area for the LO distribution. The normalized DE remains above 50% over around 18-dB P_{OUT} range. The measured AM–PM distortion is less than ±1°, and the measured EVM is better than –40 dB over around 25-dB P_{OUT} range for an OFDM signal even without any DPD. A summary of the performance and comparison of the proposed SCPA with other state-of-the-art is shown in Table 4-1.

Table 4-1 Performance summary and comparison with the state-of-the-art

		JSSC 2017 [15] V. Vorapipat	RFIC 2019 [41] S.-C. Hung	ISSCC 2019 [40] A. Zhang	ISSCC 2019 [37] L. Xiong	This work	
Architecture (SCPA)		Polar Doherty Class-G	Quadrature Doherty Class-G	Polar Multi-SHS Class-G	Polar Switched XFMR	Polar TI-Doherty single-supply Class-G	
Process (CMOS)		45 nm SOI	65 nm	65 nm	40 nm	65 nm	
Supply for P_{OUT}		2.4 / 1.2 V	2.55 / 1.25 V	3.6 / 2.4 V	1.1 V	2.5 V	
Resolution (U + B)		9b (5b + 4b)	12b (6b + 6b)	-	9b (7b + 2b)	10b (5b + 5b)	
Carrier freq.		3.5 GHz	2.2 GHz	2.2 GHz	2.4 GHz	2.4 GHz	
Peak P_{OUT}		25.3 dBm	27.8 dBm	28.7 dBm	20.9 dBm†	30.0 dBm	
# of η peaks		3	4	5	4	6	
η peaking PBOs		0 / 6 / 12 dB	0 / 2.5 / 6 / 12 dB	0 / 3.5 / 7 / 9.5 / 13 dB	0 / 6 / 12 / 18 dB	0 / 2.5 / 6 / 8.5 / 12 / 18 dB	
Efficiency	Peak	30.4% (PAE) / 100%	32.1% (SE) / 100%	42.4% (DE) / 100%	28.7% (PAE) / 100%	40.2% (DE) / 100% (Normalized)	
	2.5 dB PBO	27.0%† / 88.8%	27.5%† / 85.7%	35.0%† / 82.5%	24.0%† / 83.6%	37.9% / 94.3%	
	6.0 dB PBO	25.3% / 83.2%	22.5%† / 70.1%	30.0%† / 70.8%	20.0% / 69.7%	38.8% / 96.3%	
	8.5 dB PBO	20.0%† / 65.8%	16.0%† / 49.8%	25.0%† / 59.0%	15.0%† / 52.3%	36.3% / 90.2%	
	12.0 dB PBO	17.4% / 57.2%	10.0%† / 31.2%	20.7% / 48.8%	9.6% / 33.4%	29.4% / 73.0%	
	18.0 dB PBO	8.0%† / 26.3%	4.0%† / 12.5%	-	3.1% / 10.8%	19.7% / 48.9%	
Modulation		10-MHz 32 sub-carriers 256-QAM	20-MHz single-carrier 1024-QAM	5-MHz 52 sub-carriers 16-QAM	20-MHz 64-QAM WLAN	10-MHz single-carrier 1024-QAM	10-MHz 64-QAM OFDM
Avg. P_{OUT}		17.1 dBm	21.0 dBm	22.8 dBm	14.7 dBm	23.2 dBm	19.1 dBm
PAPR		8.2 dB	6.8 dB	7.2 dB	-	6.8 dB	10.9 dB
Avg. efficiency		21.4% (PAE)	18.4% (SE)	31.4% (DE) *	20.1% (PAE)	36.2% (DE)	30.3% (DE)
EVM		-40.1 dB	-43.0 dB	-24.7 dB *	-25.0 dB	-44.5 dB	-41.7 dB
P_{OUT} range for <-40 dB EVM		20 dB†	>10 dB† (802.11ax)	-	-	-	~25 dB
DPD		Yes	Yes	Yes	Yes	No	No

† Estimated from graph * Measured at 1.9 GHz

5 CONCLUSION

This study demonstrates very promising solutions of compact, highly efficient, and highly linear digital TX systems for modern communication standards.

For a high P_{OUT}, highly efficient and linear quadrature digital TX solution, a dual-supply Class-G *IQ*-cell-shared SCPA architecture is realized in a 65-nm CMOS process. The proposed MCS technique enables the Class-G operation in the quadrature *IQ*-cell-shared SCPA architecture and significantly improves PBO efficiency. The proposed Class-G linearization techniques enhance the Class-G SCPA linearity by compensating the amplitude and phase mismatches between the two Class-G modes. The prototype with the proposed Class-G switch achieves EVM better than -32 dB without any DPD over ±5% V_{DD} variation while delivering an average P_{OUT} and SE of 22.5 dBm and 18.3%, respectively, with a 20-MHz single-carrier 256-QAM signal.

For a low P_{OUT}, compact, highly-linear digital TX solution, an *IQ*-cell-shared SC RFDAC with linearization techniques for minimized output impedance variation and systematic enhancement in unary/binary cell utilization is implemented in a 65-nm CMOS process. The proposed linearization techniques fundamentally enhance the TX dynamic range by improving the TX linearity in both high and low P_{OUT} regions. The on-resistance linearization techniques for the output switches and the offset mid-tread code mapping technique improve the TX linearity in the high and low P_{OUT} regions, respectively. The prototype achieves better than -40-dB EVM over 30-dB P_{OUT} range with a 20-MHz single-carrier 1024-QAM signal without any DPD. The prototype occupies only 0.26 mm^2, including an on-chip matching by sharing the sub-circuits between the two RFDAC cells.

For a highly-efficient, highly-linear polar digital TX solution, a multimode multi-efficiency-peak SCPA architecture is designed and fabricated in a 65-nm CMOS process. The multimode operation maximizes the PBO efficiency by efficiently combining dual-supply Class-G, Doherty, and 2-way TI techniques. The seamless transitions between the operation modes result in six efficiency peaks with a continuous efficiency curve between the peaks in the PBO region. The proposed single-supply current-reuse Class-G switch enables highly linear and efficient Class-G operation without any external PMU. Additionally, the LO-signal-restoration technique minimizes the power dissipation and area for the LO signals distribution. The normalized DE remains greater than 50% over around 18-dB P_{OUT} range. The AM–PM distortion is less than ±1°, and the EVM is better than -40 dB over around 25-dB P_{OUT} range for a 10-MHz 64-QAM OFDM signal without any DPD.

The proposed digital TX and PA solutions demonstrate very promising results for future TX architectures with excellent efficiency and linearity. Unlike conventional TXs with conventional analog building blocks, the digital TX directly benefits from the advancement in CMOS technology because more resolution and function can be integrated into a smaller area owing to minuscule transistors with significantly improved switching performance.

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