

ADVANCED ELECTRIC VEHICLE DRIVES TOPOLOGY AND CONTROL

By

Ameer Janabi

A DISSERTATION

Submitted to

Michigan State University

in partial fulfillment of the requirements
for the degree of

Electrical Engineering - Doctor of Philosophy

2021

ABSTRACT

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In the thesis, the author focuses on solving three problems related to voltage source inverter (VSI) in general and VSI used in an electric and hybrid electric vehicle in particular.

The first problem is related to the fact that using pulse width modulated (PWM) voltage to supply the motor causes a common-mode voltage (CMV) at the motor bearings. To solve this problem, a hybrid space vector PWM is proposed that reduces the CMV amplitude and frequency to the maximally allowable extent. This can be done by utilizing a special switching sequence that takes into consideration the phase angle between the load voltage and current.

The second problem is related to the optimal PWM sequence that allows the elimination of selected low order odd harmonics. Previously, this optimization problem used to be solved using an offline approach. There have been several attempts to implement the control algorithm in real-time. All of the proposed methods in the literature, at some points, use initial guessing or iteration. This leads to an online approach with non-deterministic execution time and with the possibility to fail to reach convergence. The author shows that the optimal PWM can be implemented in real-time with deterministic execution time and without compromise. Furthermore, a significantly more generalized algorithm is proposed that allows the modulation of selected harmonics rather than merely eliminating them. The opportunities opened up by the generalized algorithm are limitless and currently being explored. The potential applications include wireless charging and digital wave generation. Modulation of several harmonics to arbitrarily prescribed values is impossible to implement using an offline approach.

The third problem is to address the limitations associated with the fact that VSI is a buck converter. For applications where the available dc voltage is limited, an additional dc-dc boost converter is needed to obtain the desirable ac voltage. Commercial hybrid vehicles typically use an inductor based dc-dc converter to boost the voltage. At higher power, the dc-dc converter becomes

inefficient. Therefore, the application of the boost stage is seen only in hybrid vehicles with a battery of a few kWh. The author proposes a new family of bidirectional dc-ac boost converters that utilizes a switched-capacitor network to boost the voltage. The switched-capacitor and the inverter are modulated as one unit, which allows the removal of the large output filtering capacitor and the reverse blocking diode required by a typical switched-capacitor converter. This effort results in extending the power level of switched-capacitor based converters from existing sub kW range to tens kW and beyond with much mitigated penalty on device utilization.

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For my parents
Hussein and Zahrah

ACKNOWLEDGMENTS

First of all, I would like to express my appreciation to my advisor, Dr. Bingsen Wang, for his guidance and support during my study at Michigan State University. Working with Dr. Wang for the past six years was one of the most rewarding experiences of my life.

I would also like to thank Dr. Elias Strangas, Dr. Joydeep Mitra, and Dr. Guoming Zhu for their support and for serving as part of my committee.

I owe a big thanks to Dr. Wei Qian for her valuable technical guidance and support.

I also would like to thank my colleagues within the power group at Michigan State University, Abdulrhman Alshaabani, Shukai Wang, Jacob Buys, Matt Meier, Dr. Xiaorui Wang, Dr. Yunting Liu, Dr. Deepak Gunasekaran, Dr. Ujjwal Karki, Dr. Yaqub Mahnashi and other lab members who have helped me over the years at MSU.

I would like to extend my thanks to my friends, Mohammad Al-Rubaiai, Maher Al-Sahlany, Khalil Sinjari, Montassar Sharif, Hussam Jabbar, Mohaned Alzuhiri, Ali MH Al-Hajjar, and Petros Taskas.

Last but not least, I would like to thank my parents, my brothers and my sisters for their constant support and encouragement along the way. Special thanks to Emily Higuera for her company and for editing my research articles.

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Chapter 1

Introduction

Over the last 800,000 years, the global average atmospheric carbon dioxide (CO₂) levels, as indicated by the ice-core data, have fluctuated between 170 and 300 parts per million by volume (ppmv). CO₂ in 2018 was 407.4 ppmv, with a range of uncertainty of plus or minus 0.1 ppmv. Carbon dioxide levels today are higher than at any point in at least the past 800,000 years.

The way the climate reacts is also complex; The main reason is that climate is a sum of three contributing factors: cyclical effect, random noise, and anthropic activities (human activities). If the anthropic term becomes significant, it drowns out the other two terms, and it would be too late to do anything. The strict correlation between the rise of greenhouse gasses and the rise of temperature is a well-understood phenomenon since 1824.

In the united states, the primary contributor of greenhouse emissions is transportation (29% in 2017). The largest sources of transportation-related greenhouse gas emissions include passenger cars and light-duty trucks, including sport utility vehicles, pickup trucks, and minivans. These sources account for over half of the emissions from the transportation sector. The remaining greenhouse gas emissions from the transportation sector come from other modes of transportation, including freight trucks, commercial aircraft, ships, boats, and trains, as well as pipelines and lubricants.

Form this stems the unique importance of vehicle electrification. EVs typically produce fewer

life-cycle emissions than conventional vehicles because most emissions are lower for electricity generation than burning gasoline or diesel. The exact amount of these emissions depends on the electricity mix, which varies by geographic location.

One important factor of expediting electric vehicle adoption is the technology advancement and the substantial cost cut resulting from it. Key enablers are developments in battery chemistry and the expansion of production capacity in manufacturing plants. Other important solutions include the design of vehicle power electronic units, which mainly consists of the motor drive inverter and the on-board battery charger. In this thesis, the author focuses on advancing the motor driver inverter from both control and topology perspectives. From the control perspective, the author shows that it is possible to tackle several optimization problems without any additional cost or additional hardware. In the first part, the common-mode voltage (CMV) is addressed. CMV is one of the most common failure causes in electric motors. Mitigating the CMV effects leads to improved reliability of the motor and longer lifetime. In the second part, the optimization of the PWM pattern is addressed. A real-time approach is developed that allows eliminating the low-order odd harmonics with deterministic execution time. The elimination of the low-order harmonics leads to a close-to-sinusoidal load current with minimized switching losses. In the last part of this thesis, a new type of boost converter is presented. The switched-capacitor boost converter increases the effective dc-link voltage without relaying of bulky inductors. This approach has the benefit of potentially increasing the power density of the converter.

Chapter 2

Hybrid SVPWM Scheme to Minimize the Common-mode Voltage Frequency and Amplitude in VSI Drives

Voltage source inverters (VSIs) are widely used in motor drive applications. The use of VSI ranges from high power (e.g., wind turbines) to medium power (e.g., electric and hybrid electric vehicles). Ever since the invention of the insulated gate bipolar transistor (IGBT), increasing the switching frequency of the power converter has been a trend due to the reduction of the footprint and the increase of power density [1, ?]. Recent development of wide bandgap devices has equipped the power switches with even faster switching speed [3]. However, the increase in the switching frequency has generated several unwanted consequences, one of which is the high-frequency common-mode voltage (CMV) [4], [6]. The high-frequency CMV can cause electromagnetic interference (EMI) that adversely affects the other components of the system [7]. The induced over-voltage stresses the winding insulation of the drives and also can increase the shaft current [8]. In particular, the shaft current is the result of the fluctuation of the CMV, which is strictly related to the sequence of the inverter switching states [9]. Several studies presented in the literature discussed the reduction of CMV effects. They can be classified into hardware solutions and algo-

rithmic solutions. The hardware ones require either increasing the number of switches [10]- [15], passive components [16]- [25], or both [26, 27]. The study in this chapter is mostly related to the algorithmic approaches that require no additional hardware.

The early attempt to reduce the CMV proposed in [9] uses only the odd or only the even voltage vectors. This approach results in DC CMV. However, the linear region in this approach is reduced to $MI \leq \frac{4}{3\sqrt{3}}$. Later a number of CMV reduction methods were proposed such as the active zero states PWM (AZSPWM1-2 and AZSPWM3), remote state PWM (RSPWM1, RSPWM2, and RSPWM3), and near-state PWM (NSPWM) [28]- [31]. In each one, several active voltage vectors are utilized to meet the voltage second requirements and avoid using the zero vectors. The non-zero switching vectors generate lower magnitude CMV but the conventional space vector PWM uses zero vectors as it helps in reducing the THD [32, 35]. The latter methods, except for NSPWM, utilize all of the linear region, which leaves the high frequency of the CMV remaining an issue. The high common-mode $\frac{dv}{dt}$ causes electric discharge machining (EDM) across the bearing races. Furthermore, the CMV reduction methods assume ideal switches and fail when non-idealities such as the dead-time and line-line voltage reversal are considered [34].

On the other hand, to further improve the performance of CMV reduction methods, combined approaches are used in different operating conditions. For instance, to make full use of NSPWM, another CMV reduction method is activated at low modulation index such as AZSPWM1 [36]. The modified SVPWM presented in [37] combines both RSPWM and regular SVPWM at low and high modulation index, respectively. This method makes a trade-off between DC-link voltage utilization and common-mode current (CMC) reduction. However, the dead-time effect causes CMV amplitude to reach half of DC-link voltage [38]- [40].

In this chapter, a hybrid approach for minimizing the amplitude and the frequency of the CMV is proposed. The control concept is based on dividing the space vector hexagon into various segments and synthesizing the reference voltage vector by using vectors that correspond to a minimal CMV. Full treatment of the dead-time effect is presented. The proposed method avoids any CMV peaks or unwanted variations during the dead-time intervals.

The rest of the chapter is organized as follows. In section 2.1, the regular SVPWM is briefly revisited. The proposed control method is presented in Section 2.2. Dead-time effect is presented in Section 2.3. A complete solution to the dead-time effect is presented in Section 2.4. Performance analyses including CMV characteristics, harmonic distortion factor (HDF), DC current ripple, and the switching losses are presented in Section 2.5. Hardware results and conclusion are presented in section 2.6 and 2.7, respectively.

2.1 Conventional SVPWM

For the two-level, three-phase voltage source inverter shown in Fig. 2.1, the reference value of the inverter output voltage can be represented by the following space vector:

$$\mathbf{V}_{ref} = \frac{2}{3}(v_a + v_b e^{j\frac{2\pi}{3}} + v_c e^{-j\frac{2\pi}{3}}) \quad (2.1)$$

where v_a , v_b , and v_c are the three phase voltages. Since the DC-link should not be shorted, each phase voltage can only attain either V_{dc} or $-V_{dc}$. This also restricts the feasible switching states to only eight states. The eight converter states as well as the corresponding differential-mode voltage (DMV) and common-mode voltage are shown in Table 3.1. The linear combination of the possible eight vectors span a hexagonal area as shown in Fig. 2.2.

Table 2.1 The feasible voltage vectors and the corresponding DMV and CMV.

Dwell time	Voltage vector	v_a	v_b	v_c	$\mathbf{v}_{dm}$	v_{cm}
tv_0	$\mathbf{V}(0,0,0)$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$
tv_1	$\mathbf{V}(1,0,0)$	V_{dc}	$-V_{dc}$	$-V_{dc}$	$\frac{4}{3}V_{dc}$	$-\frac{V_{dc}}{3}$
tv_2	$\mathbf{V}(1,1,0)$	V_{dc}	V_{dc}	$-V_{dc}$	$(\frac{2}{3} + j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
tv_3	$\mathbf{V}(0,1,0)$	$-V_{dc}$	V_{dc}	$-V_{dc}$	$(-\frac{2}{3} + j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
tv_4	$\mathbf{V}(0,1,1)$	$-V_{dc}$	V_{dc}	V_{dc}	$-\frac{4}{3}V_{dc}$	$\frac{V_{dc}}{3}$
tv_5	$\mathbf{V}(0,0,1)$	$-V_{dc}$	$-V_{dc}$	V_{dc}	$(-\frac{2}{3} - j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
tv_6	$\mathbf{V}(1,0,1)$	V_{dc}	$-V_{dc}$	V_{dc}	$(\frac{2}{3} - j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
tv_7	$\mathbf{V}(1,1,1)$	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}

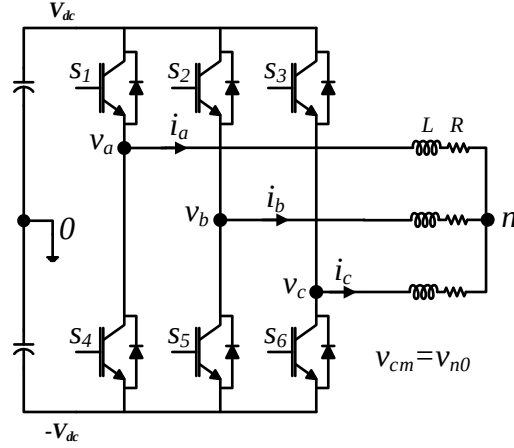


Figure 2.1 Three-phase voltage source inverter.

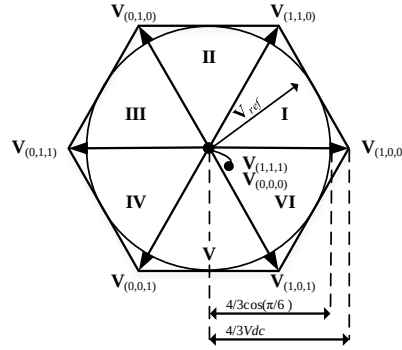


Figure 2.2 Eight stationary vectors in the complex plane for a VSI.

The reference vector $\mathbf{V}_{ref}$ is synthesized at each sampling period T_s using the two adjacent active vectors and the zero vectors. This leads to six equal sectors. Because the circular trajectory of $\mathbf{V}_{ref}$ in the complex plane corresponds to a sinusoidal three-phase voltage, the maximum achievable sinusoidal output voltage amplitude is $\leq \frac{2}{\sqrt{3}}V_{dc}$. Therefore, the modulation index MI can be defined as the per unit output voltage vector using V_{dc} as the base voltage $MI \in [0, \frac{2}{\sqrt{3}}]$.

For instance, when the trajectory of the reference voltage $\mathbf{V}_{ref}$ is passing through the first sector where $\theta \in [0, \frac{\pi}{3}]$, the following volt-seconds equality holds:

$$T_s \mathbf{V}_{ref} = t_{v1} \mathbf{V}_{(1,0,0)} + t_{v2} \mathbf{V}_{(1,1,0)} + t_{v0} \mathbf{V}_{(0,0,0)} + t_{v7} \mathbf{V}_{(1,1,1)} \quad (2.2)$$

$$T_s = t_{v1} + t_{v2} + t_{v0} + t_{v7}. \quad (2.3)$$

By equating the real part and the imaginary part in (2.2), the following dwell times can be obtained:

$$t_{v1} = \frac{3}{4}T_s MI [\cos(\theta) - \sin(\theta)] \quad (2.4)$$

$$t_{v2} = \frac{\sqrt{3}}{2}T_s MI \sin(\theta) \quad (2.5)$$

$$t_{v0} = t_{v7} = T_s - t_{v1} - t_{v2}. \quad (2.6)$$

The same rules can be applied for calculating the dwell times of the vectors for sectors 2 through 6 if the following modified θ_k is used:

$$\theta_k = \theta - (k - 1)\frac{\pi}{3} \quad (2.7)$$

where k is the number of the sector in which the $\mathbf{V}_{ref}$ resides.

2.2 Hybrid Space Vector Pulse With Modulation Synthesis

The method of hybrid space vector pulse width modulation synthesis (HSVPWMS) further subdivides each sector into three segments. In each segment, a group of active voltage vectors is selected to match the output reference volt-seconds and achieve minimal CMV amplitude and frequency. The location of the reference voltage vector can be defined in correspondence to the modulation index MI and its angle θ .

The total eighteen segments of the space vector hexagon are obtained based on their corresponding CMV. They can be categorized into: i) six odd segments that result in $\text{CMV} - \frac{V_{dc}}{3}$, ii) six even segments that result in $\text{CMV} \frac{V_{dc}}{3}$, and iii) six odd-even segments that result in $\text{CMV} \pm \frac{V_{dc}}{3}$.

To understand the navigation of the reference voltage through those segments, the author thoroughly explains the synthesis of the reference voltage vector via the first sector $\theta \in [0, \frac{\pi}{3})$ with

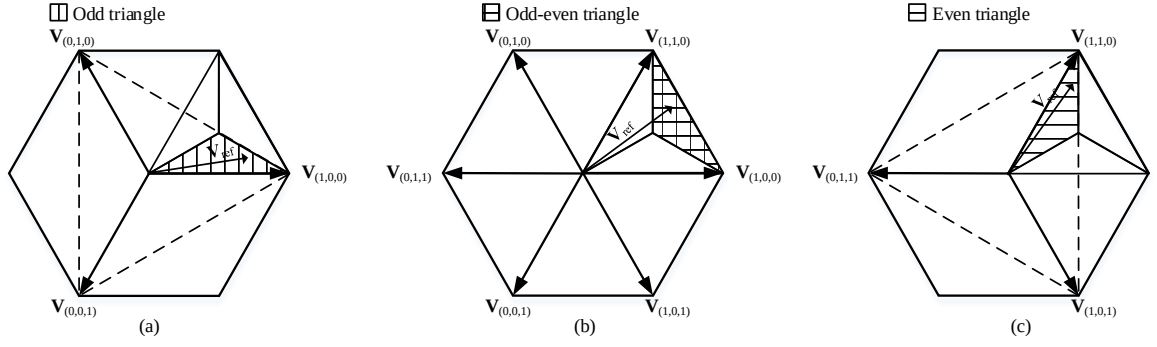


Figure 2.3 Sector I is divided into three segments: (a) odd triangle, (b) odd-even triangle, and (c) even triangle.

reference to Fig. 2.3.

The sector includes three segments (triangles). The reference vector in the bottom triangle (odd-triangle) can be synthesized using only the odd vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ as shown in Fig. 2.3 (a). The reference vector in the upper-right triangle (odd-even triangle) can be synthesized using the odd and even vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \dots, \mathbf{V}_{(1,0,1)}\}$ as shown Fig. 2.3 (b). The reference vector in the upper-left triangle (even triangle) can be synthesized using only the even vectors $\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$ as shown Fig. 2.3 (c).

The line dividing the odd triangle from the odd-even triangle can be parameterized as follows:

$$edge = \frac{2}{\sqrt{3}} \left(1 - \frac{\theta}{\pi/6}\right); \quad (2.8)$$

When the MI is greater than the value of $edge$, the reference voltage vector is in the odd triangle. Similar logic can be followed to identify all other segments.

The synthesis of the reference voltage vector in the odd triangle and even triangle is unique, whereas the synthesis for the reference voltage vector in the odd-even triangle can be realized using different groups of vectors. The groups are classified into four groups with each group producing similar harmonic content and switching losses. The four groups are delineated in the following subsections.

2.2.1 HSVPWMS I

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and the two voltage vectors of the neighboring states to match the output and reference volt-seconds as shown in Fig. 2.4 (b). For the odd triangle shown in Fig. 2.4 (a), the time intervals in which the inverter states $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref}T_s = \mathbf{V}_{(1,0,0)}t_{v1} + \mathbf{V}_{(0,1,0)}t_{v3} + \mathbf{V}_{(0,0,1)}t_{v5} \quad (2.9)$$

$$T_s = t_{v1} + t_{v3} + t_{v5}. \quad (2.10)$$

This leads to the following dwell times:

$$t_{v1} = \frac{T_s}{3} + \frac{T_s MI \cos(\theta)}{2} \quad (2.11)$$

$$t_{v3} = \frac{T_s}{3} - \frac{T_s MI \cos(\theta)}{4} + \frac{\sqrt{3}T_s MI \sin(\theta)}{4} \quad (2.12)$$

$$t_{v5} = \frac{T_s}{3} - \frac{T_s MI \cos(\theta)}{4} - \frac{\sqrt{3}T_s MI \sin(\theta)}{4}. \quad (2.13)$$

For the odd-even triangle shown in Fig. 2.4 (b), the time intervals in which the inverter states

$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)},$

$\mathbf{V}_{(0,1,0)}\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref}T_s = \mathbf{V}_{(1,0,1)}t_{v6} + \mathbf{V}_{(1,0,0)}t_{v1} + \mathbf{V}_{(1,1,0)}t_{v2} + \mathbf{V}_{(0,1,0)}t_{v3} \quad (2.14)$$

$$T_s = t_{v6} + t_{v1} + t_{v2} + t_{v3}. \quad (2.15)$$

To solve the algebraic equations, it is assumed t_{v6} is equal to t_{v3} . This leads to the following

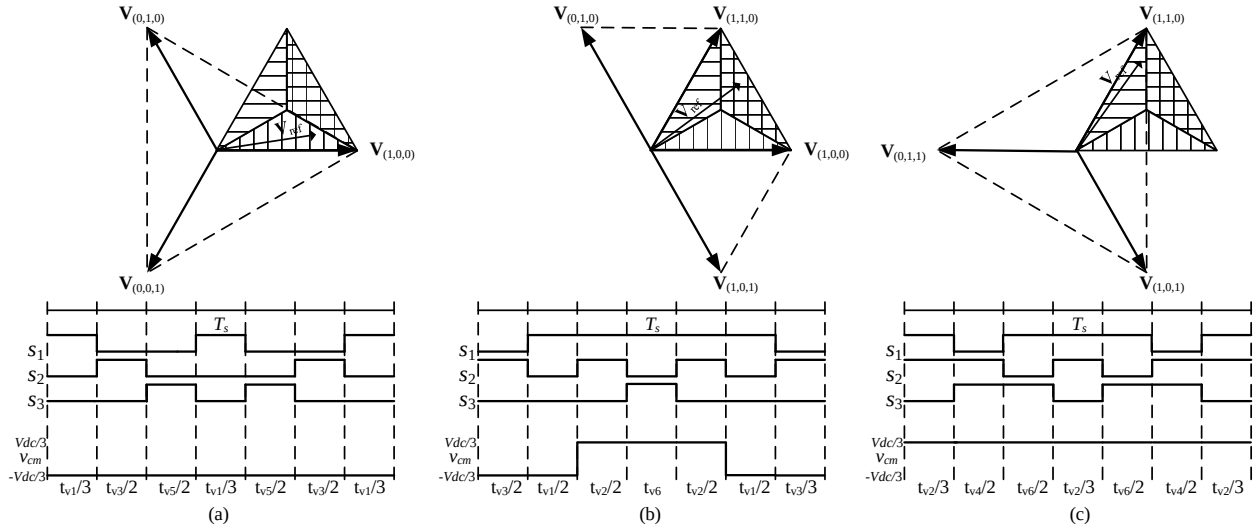


Figure 2.4 Vector synthesis for HSPWM I of (a) odd triangle, (b) odd-even triangle, and (c) even triangle.

dwell times:

$$t_{v1} = \frac{3T_s MI \cos(\theta)}{4} - \frac{\sqrt{3}T_s MI \sin(\theta)}{4} \quad (2.16)$$

$$t_{v2} = \frac{\sqrt{3}T_s MI \sin(\theta)}{2} \quad (2.17)$$

$$t_{v6} = t_{v3} = \frac{T_s}{2} - \frac{3T_s MI \cos(\theta)}{8} - \frac{\sqrt{3}T_s MI \sin(\theta)}{8}. \quad (2.18)$$

For the even triangle shown in Fig. 2.4 (c), the time intervals in which the inverter states $\{(\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)})\}$ are applied can be calculated by solving the following algebraic equations:

$$\mathbf{V}_{ref} T_s = \mathbf{V}_{(1,1,0)} t_{v2} + \mathbf{V}_{(0,1,1)} t_{v4} + \mathbf{V}_{(1,0,1)} t_{v6} \quad (2.19)$$

$$T_s = t_{v2} + t_{v4} + t_{v6}. \quad (2.20)$$

This leads to the following dwell times:

$$t_{v2} = \frac{T_s}{3} + \frac{T_s MI \cos(\theta)}{4} + \frac{\sqrt{3}T_s MI \sin(\theta)}{4} \quad (2.21)$$

$$t_{v4} = \frac{T_s}{3} - \frac{T_s MI \cos(\theta)}{2} \quad (2.22)$$

$$t_{v6} = \frac{T_s}{3} + \frac{T_s MI \cos(\theta)}{4} - \frac{\sqrt{3}T_s MI \sin(\theta)}{4}. \quad (2.23)$$

The similar calculation can be conducted for the other five sectors by employing the appropriate vectors as listed in Table 2.2.

Table 2.2 The vector combinations used in the three segments of each sector using HSVPWMS I.

Sector	Odd triangle	Odd-even triangle	Even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
II	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
III	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
IV	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
V	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
VI	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}\}$	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$

2.2.2 HSVPWMS II

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and one voltage vector of either neighboring state to match the output and reference volt-seconds as shown in Fig. 2.5. Table 2.3 shows the vector combinations used in the three segments of each sector for HSVPWMS II.

Table 2.3 The vector combinations used in the three segments of each sector using HSVPWMS II.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, (\mathbf{V}_{(0,1,0)} \vee \mathbf{V}_{(1,0,1)})\}$
II	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, (\mathbf{V}_{(0,1,1)} \vee \mathbf{V}_{(1,0,0)})\}$
III	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, (\mathbf{V}_{(0,0,1)} \vee \mathbf{V}_{(1,1,0)})\}$
IV	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, (\mathbf{V}_{(1,0,1)} \vee \mathbf{V}_{(0,1,0)})\}$
V	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, (\mathbf{V}_{(1,0,0)} \vee \mathbf{V}_{(0,1,1)})\}$
VI	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, (\mathbf{V}_{(1,1,0)} \vee \mathbf{V}_{(0,0,1)})\}$

2.2.3 HSVPWMS III

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and the two voltage vectors of the far states to match the output

and reference volt-seconds as shown in Fig. 2.6. Table 2.4 shows the vector combinations used in the three segments of each sector for HSVPWMS III.

Table 2.4 The vector combinations used in the three segments of each sector using HSVPWMS III.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}\}$
II	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$
III	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$
IV	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,0)}\}$
V	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,1,0)}\}$
VI	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}\}$

2.2.4 HSVPWMS IV

The voltage reference vector passing through the odd-even triangles can be synthesized by using the two adjacent voltage vectors and one voltage vectors of either far state to match the output and reference volt-seconds as shown in Fig. 2.7. Table 2.5 shows the vector combinations used in the three segments of each sector for HSVPWMS IV.

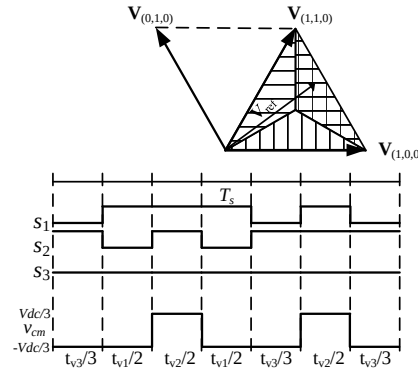


Figure 2.5 Vector synthesis of odd-even triangle for HSVPWMS II.

Table 2.5 The vector combinations used in the three segments of each sector using HSVPWMS IV.

Sector	Odd-even triangle
I	$\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, (\mathbf{V}_{(0,1,1)} \vee \mathbf{V}_{(0,0,1)})\}$
II	$\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, (\mathbf{V}_{(0,0,1)} \vee \mathbf{V}_{(1,0,1)})\}$
III	$\{\mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, (\mathbf{V}_{(1,0,1)} \vee \mathbf{V}_{(1,0,0)})\}$
IV	$\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, (\mathbf{V}_{(1,0,0)} \vee \mathbf{V}_{(1,1,0)})\}$
V	$\{\mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}, (\mathbf{V}_{(1,1,0)} \vee \mathbf{V}_{(0,1,0)})\}$
VI	$\{\mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,0,0)}, (\mathbf{V}_{(0,1,0)} \vee \mathbf{V}_{(0,1,1)})\}$

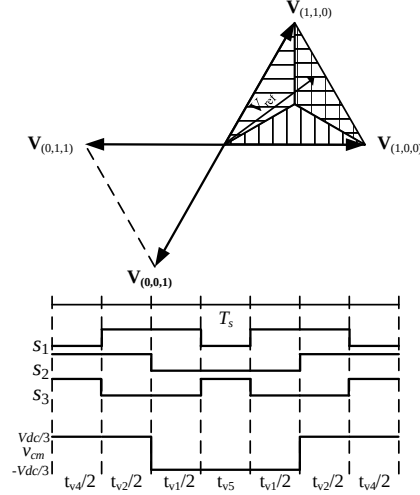


Figure 2.6 Vector synthesis of odd-even triangle for HSPWMS III.

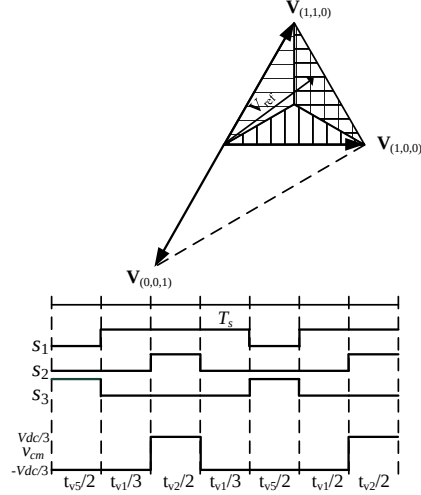


Figure 2.7 Vector synthesis of odd-even triangle for HSPWMS IV.

2.3 Dead-time Effect and Narrow CMV Pulse Avoidance

The implementation of only odd or only even vectors requires simultaneous switching of two converter legs. In practice, this could be challenging because of the dead-times and the differences in the gate delay [30]. The dead-time mismatch causes a narrow pulse in the CMV. The narrow pulse frequency increases as the switching frequency increases. To further assess the situation, consider Fig. 2.8. During the dead-times, the resulting CMV is no longer a function of the switching commands. Instead it is strictly dependent on the signs of the three-phase load currents. In this

case, the CMV $\in \{V_{dc}, \frac{V_{dc}}{3}, -\frac{V_{dc}}{3}, -V_{dc}\}$. Therefore, the effective switching state during the dead-times must be analyzed for each transition.

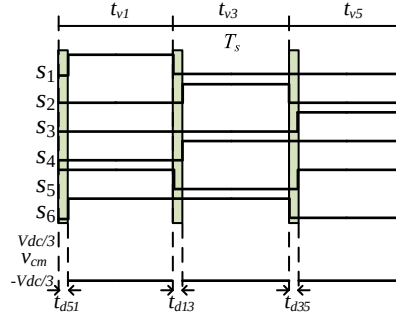


Figure 2.8 Dead-time effect on CMV. During the dead-times, the CMV is dependent on the sign of the three-phase load current, $\text{CMV} \in \{V_{dc}, \frac{V_{dc}}{3}, -\frac{V_{dc}}{3}, -V_{dc}\}$.

Consider these three examples:

Example 1

Suppose the transition from the odd vector $\mathbf{V}_{(1,0,0)}$ to the odd vector $\mathbf{V}_{(0,1,0)}$ is taking place while the three-phase load currents $i_a > 0$, $i_b < 0$, and $i_c > 0$. The effective switching state during the dead-time t_{d13} will be the same as the destination vector state $(0, 1, 0)$. This is because of the current polarities as shown in Fig. 2.9: i_a is positive and will flow through the freewheeling diode of S_4 when S_1 turns off; i_b is negative and will flow through the freewheeling diode of S_2 ; and i_c is positive and will flow through the freewheeling diode of S_6 . This is equivalent to connecting two of the load phases to the lower DC rail V_{dc} and only one phase to the upper DC rail V_{dc} . In this case, the resulting CMV during t_{d13} is as expected and equal to $-\frac{V_{dc}}{3}$.

Example 2

If the same transition occurs while the three-phase load currents $i_a > 0$, $i_b > 0$, and $i_c < 0$, the effective switching state during the dead-time t_{d13} will not be the same as the destination vector

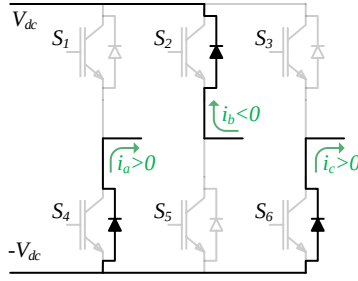


Figure 2.9 During t_{d13} and $i_a > 0$, $i_b < 0$, and $i_c > 0$, the CMV is equal to $-\frac{V_{dc}}{3}$.

state $(0, 1, 0)$. Instead it will be $(0, 0, 0)$, and the resulting CMV during t_{d13} will be equal to $-V_{dc}$ as shown in Fig 2.10.

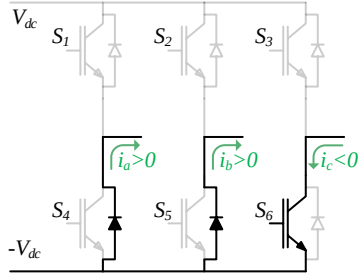


Figure 2.10 During t_{d13} and $i_a > 0$, $i_b > 0$, and $i_c < 0$, the CMV is equal to $-V_{dc}$.

Example 3

If the same transition occurs while the three-phase load currents $i_a < 0$, $i_b < 0$, and $i_c > 0$, the effective switching state at the dead-time t_{d13} will not be the same as the destination vector state $(0, 1, 0)$. Instead it will be $(1, 1, 0)$, and resulting CMV will be $\frac{V_{dc}}{3}$ as shown in Fig. 2.11.

By considering all of the possible intervals in which the three-phase load currents do not change sign, six current sectors can be defined as shown in Fig. 2.12. The calculations for the effective switching states during the other dead-times are performed in the same manner as illustrated in the examples and listed in Tables 2.6 and 2.7 for odd and even states, respectively. It is important to note that the effective switching state is the same as the effective switching state when the transition is reversed ($t_{dxy} = t_{dyx}$). For this reason, the calculations for this type of transition are

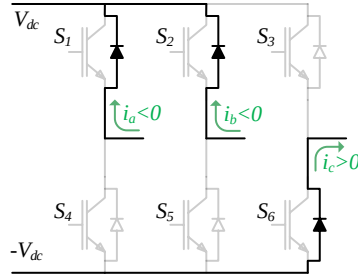


Figure 2.11 During t_{d13} and $i_a < 0$, $i_b < 0$, and $i_c > 0$, the CMV is equal to $\frac{V_{dc}}{3}$.

not included in the tables.

Table 2.6 Effective switching states in case of only odd modulation.

Sector	Dead-time	Eff. state (S1,S2,S3)	v_{cm}
S-I	t_{d13}	(0,0,0)	$-V_{dc}$
	t_{d35}	(0,1,0)	$-\frac{V_{dc}}{3}$
	t_{d51}	(0,1,0)	$-\frac{V_{dc}}{3}$
S-II	t_{d13}	(0,0,1)	$-\frac{V_{dc}}{3}$
	t_{d35}	(0,1,0)	$-\frac{V_{dc}}{3}$
	t_{d51}	(0,1,1)	$\frac{V_{dc}}{3}$
S-III	t_{d13}	(0,0,1)	$-\frac{V_{dc}}{3}$
	t_{d35}	(0,0,0)	$-V_{dc}$
	t_{d51}	(0,0,1)	$-\frac{V_{dc}}{3}$
S-IV	t_{d13}	(1,0,1)	$\frac{V_{dc}}{3}$
	t_{d35}	(1,0,0)	$-\frac{V_{dc}}{3}$
	t_{d51}	(0,0,1)	$-\frac{V_{dc}}{3}$
S-V	t_{d13}	(1,0,0)	$-\frac{V_{dc}}{3}$
	t_{d35}	(1,0,0)	$-\frac{V_{dc}}{3}$
	t_{d51}	(0,0,0)	$-V_{dc}$
S-VI	t_{d13}	(1,0,0)	$-\frac{V_{dc}}{3}$
	t_{d35}	(1,1,0)	$\frac{V_{dc}}{3}$
	t_{d51}	(0,1,0)	$-\frac{V_{dc}}{3}$

Table 2.7 Effective states in case of only even modulation.

Sector	Dead-time	Eff. state (S1,S2,S3)	v_{cm}
S-I	t_{d24}	(1,1,0)	$\frac{V_{dc}}{3}$
	t_{d46}	(0,1,0)	$-\frac{V_{dc}}{3}$
	t_{d62}	(0,1,1)	$\frac{V_{dc}}{3}$
S-II	t_{d24}	(1,1,1)	V_{dc}
	t_{d46}	(0,1,1)	$\frac{V_{dc}}{3}$
	t_{d62}	(0,1,1)	$\frac{V_{dc}}{3}$
S-III	t_{d24}	(1,0,1)	$\frac{V_{dc}}{3}$
	t_{d46}	(0,1,1)	$\frac{V_{dc}}{3}$
	t_{d62}	(0,0,1)	$-\frac{V_{dc}}{3}$
S-IV	t_{d24}	(1,0,1)	$\frac{V_{dc}}{3}$
	t_{d46}	(1,1,1)	V_{dc}
	t_{d62}	(1,0,1)	$\frac{V_{dc}}{3}$
S-V	t_{d24}	(1,0,0)	$-\frac{V_{dc}}{3}$
	t_{d46}	(1,1,0)	$\frac{V_{dc}}{3}$
	t_{d62}	(1,0,1)	$\frac{V_{dc}}{3}$
S-VI	t_{d24}	(1,1,0)	$\frac{V_{dc}}{3}$
	t_{d35}	(1,1,0)	$\frac{V_{dc}}{3}$
	t_{d62}	(1,1,1)	V_{dc}

It is evident from Tables 2.6 and 2.7 that the CMV is not limited to $|\frac{V_{dc}}{3}|$ even if only odd or only even states are used. Therefore, to avoid the unwanted CMV peaks ($|V_{dc}|$), the control algorithm must be modified to use only odd states in S-II, S-IV, and S-VI and only even states in S-I, S-III, and S-V. The current sectors are shown in Fig. 2.13(a).

It is important to note the connection between the current sectors {S-I to S-VI} and the power factor (PF). In machine drive applications the current space vector ($\mathbf{i}$) is lagging. This causes the current sectors to rotate clockwise and changes the feasible regions of using only odd or only even states. Fig. 2.13(b) shows the rotated current space vector when the $PF = 0.866$ lagging.

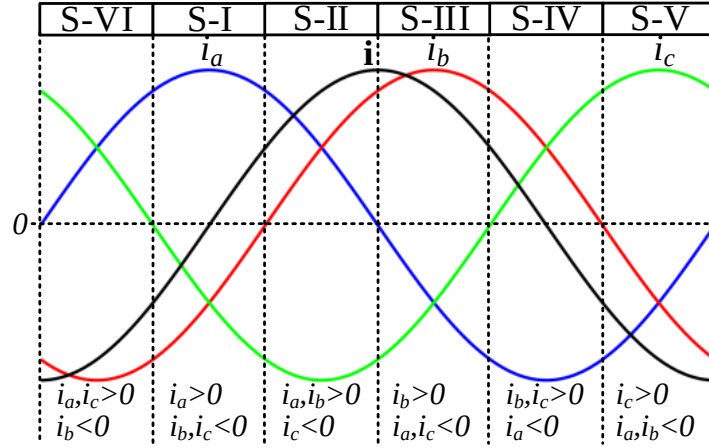


Figure 2.12 There are six regions in which the three-phase load currents do not change sign.

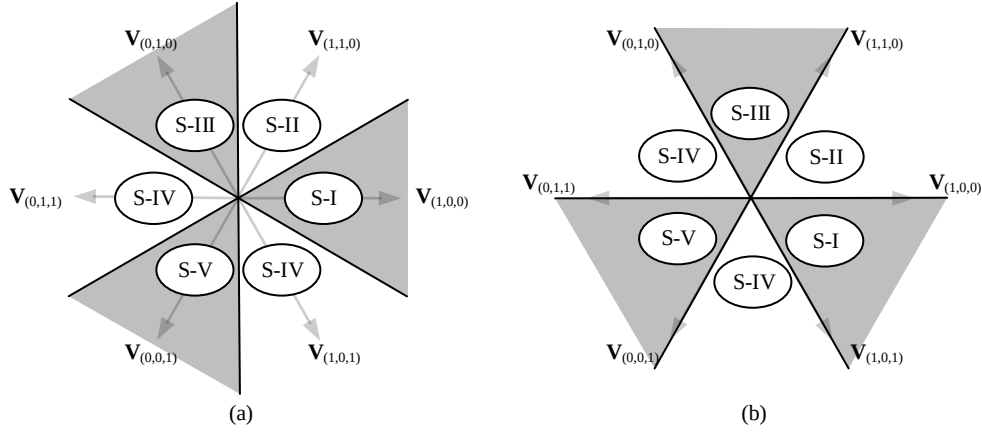


Figure 2.13 The current sectors (in which the three-phase load currents do not change sign) in relation to the voltage vectors when (a) $PF = 1$ and (b) $PF = 0.866$ lagging.

Modifying the control algorithm to avoid the peak CMV is not difficult as long as the load current signals are available in the loop. Fig. 2.14 shows the modified control block diagram.

The current sectors are determined by measuring the load currents and checking the sign of each phase current. Although this modification allows one to avoid the maximum CMV peaks, high $\frac{dv_{cm}}{dt}$ is still possible during some dead-times. Furthermore, the availability of only odd or only even vectors is linked to the PF . When the $PF = 1$, the current sectors are completely out of sync. Whereas if the $PF = 0.866$, the current sectors are completely in sync. To avoid this limitation, the authors propose a new commutation method in the next section. The new commutation method allows a complete decoupling of the effect of PF , and it avoids the narrow

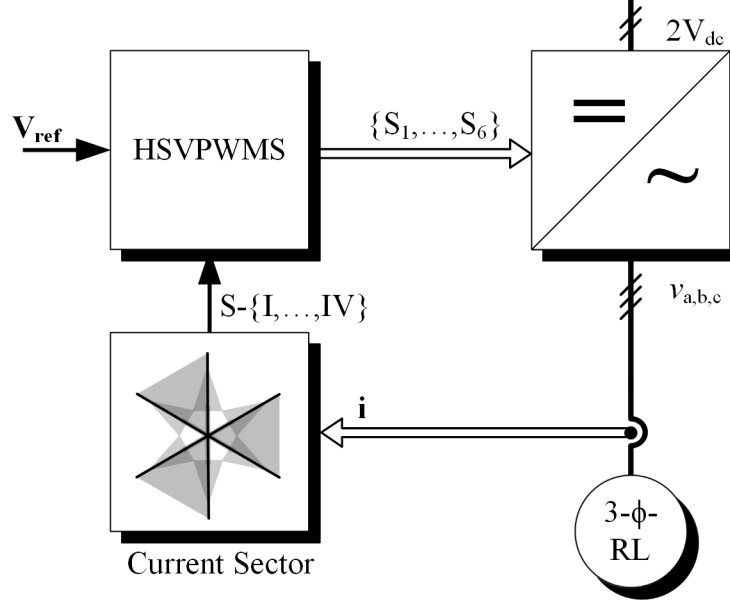


Figure 2.14 Modified control block diagram to account for the current sectors position.

CMV pulse during dead-time intervals.

2.4 Proposed commutation Algorithm

As shown in the previous section, by including the load current signals in the control loop, one can determine when it is safe to use only odd or only even vectors without causing peak CMV. However, there are unwanted transitions in the CMV from $\frac{V_{dc}}{3}$ to $-\frac{V_{dc}}{3}$ or vice versa during some dead-time intervals. As Tables 2.6 and 2.7 demonstrate, in each current sector there are two dead-time intervals in which no change in the CMV occurs. These two dead-times can be utilized to make a proper commutation sequence among the odd vectors or even vectors. Fig. 2.15 shows the commutation sequences that achieve no change in the CMV during the dead-time intervals. Furthermore, the rotation of the current sectors due to the PF will not affect the availability of only odd or only even vectors because in each current sector there are two safe sequences: one for only odd states and one for only even states. The safe sequences also allow to equalize switching losses per fundamental cycle among the IGBTs. Therefore, there is no unbalanced temperature distribution in inverter switches.

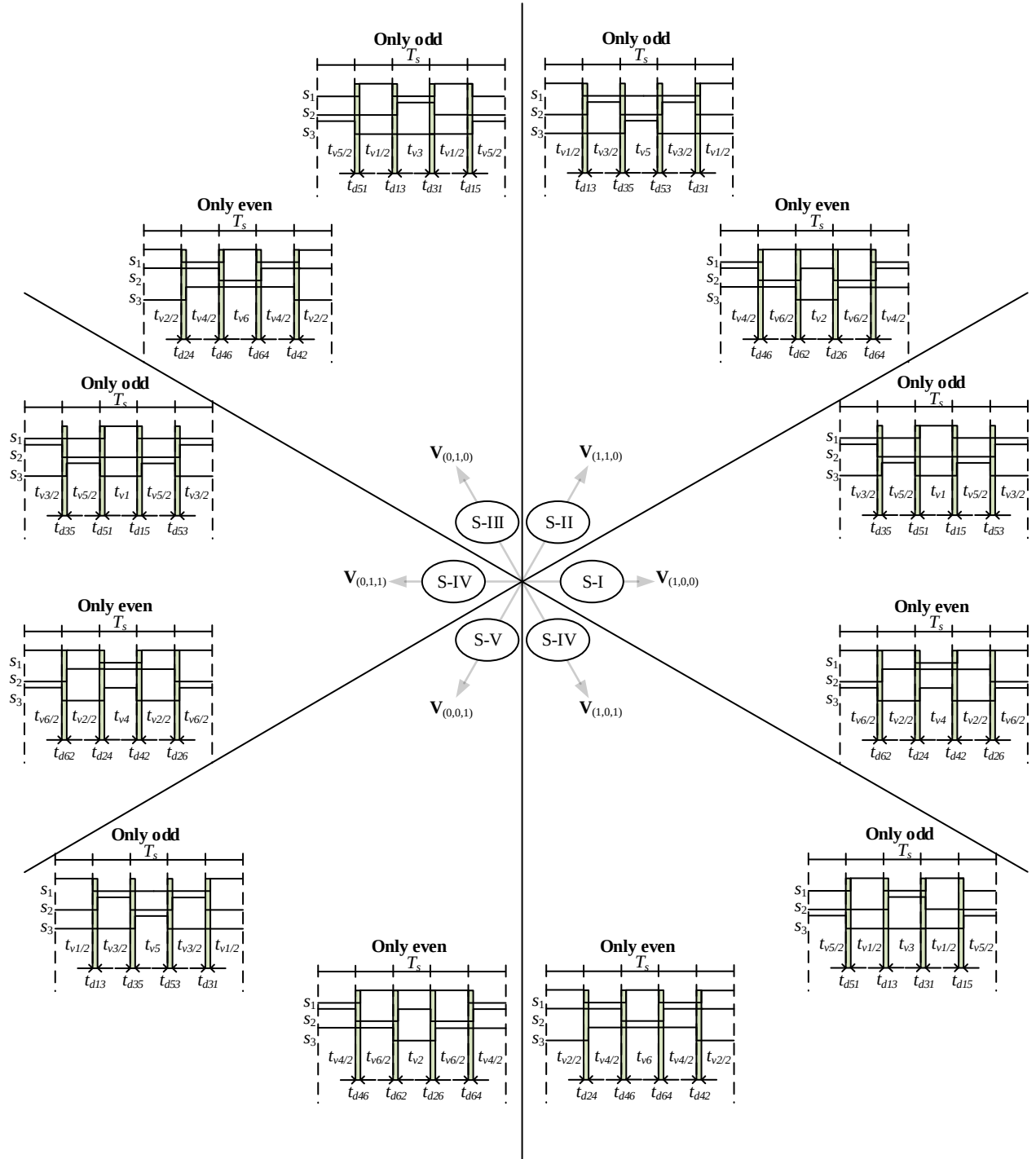


Figure 2.15 The commutation sequences that do not cause a change in CMV during dead-time intervals. Each current sector has two safe sequences: one for only odd and one for only even syntheses. This allows the use of only odd and only even vectors without any constraints imposed by the PF .

2.5 Performance Analysis

HSVPWMS methods utilize different voltage vectors with different possible sequences. Each synthesis and combination corresponds to a different number of commutations, output current quality, CMV characteristics, DC-link current harmonics, and switching losses. Therefore, to understand the full potential of each method, a fair comparison with the CMV reduction PWM methods in terms of CMV characteristics, HDF, DC-link current, and switching losses is presented next.

2.5.1 Common-mode Voltage Characteristics

Common-mode behavior for induction machines is mostly capacitive [41]. Therefore, it does not require an extensive high-frequency machine modeling to determine the relationship between CMV characteristics and the resulting CM current. Early studies showed that the parasitic machine capacitances can be measured [42] or calculated by finite element methods [43, 44]. A machine model for high frequencies is developed in [45] and shows that the CM current is directly proportional to the frequency of the CMV.

Fig. 2.16 shows the CMV and its spectrum for the conventional SVPWM. The amplitude of the CMV is V_{dc} and is high due to the use of zero vectors. Another fundamental component of the CMV at the PWM carrier frequency (f_c).

All of the other HSVPWMS methods have similar CMV waveforms for $MI \leq \frac{4}{3\sqrt{3}}$, where the main harmonic components are at $3f_1$ and $6f_1$, where f_1 is the system fundamental frequency (for instance 60 Hz). These two frequency components result in a very small common-mode current because the impedance is very high prior to the resonance region [41]. HSVPWMS I and HSVPWMS III have harmonic components around the carrier frequency f_c with an amplitude lower than that of the conventional SVPWM method. The f_c component increases as the MI increases as shown in Fig. 2.17 and Fig. 2.19. HSVPWMS II and HSVPWMS IV have high-frequency CMV components around $2f_c$ that increase as the MI increases. Most of the CMV harmonic compo-

nents are concentrated in the fundamental component $3f_1$ and base band harmonic $6f_1$ as shown in Fig. 2.18 and Fig. 2.20. Generally, HSVPWMS methods have a maximum CMV amplitude equal to $\frac{V_{dc}}{3}$, which is three times less than the regular SVPWM. More importantly, the amplitudes of CMV at high frequencies are reduced tremendously, especially at $MI \leq MI_{max}$. Therefore, the resulting CM current in the HSVPWMS method is significantly reduced as compared against the other methods..

Fig. 2.21 gives a clear representation of how the fundamental component of the CMV is behaving versus MI within the linear modulation region. The simulation parameters: DC-link voltage 60 V, carrier frequency $f_c = 5$ kHz, and system fundamental frequency $f_1 = 60$ Hz. It has been observed through multiple simulations that the characteristic of each harmonic is relatively constant to those parameters, therefore, the plots are given in terms of the DC-link voltage, fundamental frequency, and the carrier frequency. The high-frequency CMV of the regular SVPWM has a very high amplitude when the MI is low because of the high duty ratio of the zero vector. The suitable HSVPWMS can be selected based on the level of the MI and the characteristics of the machine common-mode impedance.

2.5.2 Harmonic Distortion Factor

In the motor winding $f_{sw}/f \geq 20$, the harmonic current is directly proportional to the harmonic flux. Therefore, the current quality can be studied by using only the information of the applied voltage vector independent of the load ratings. The concept of harmonic distortion factor introduced in [46] is further expanded to account for the transitions between different syntheses. The harmonic flux for the N th carrier cycle can be defined as [29]

$$\lambda_h(MI, \theta, V_{(.,.,.)}) = \int_{NT_s}^{(N+1)T_s} (V_{(.,.,.)} - V_{ref}) dt \quad (2.24)$$

where $V_{(.,.,.)}$ is the applied voltage vector during the sampling time NT_s . Normalizing the harmonic flux results in the harmonic flux voltage vector

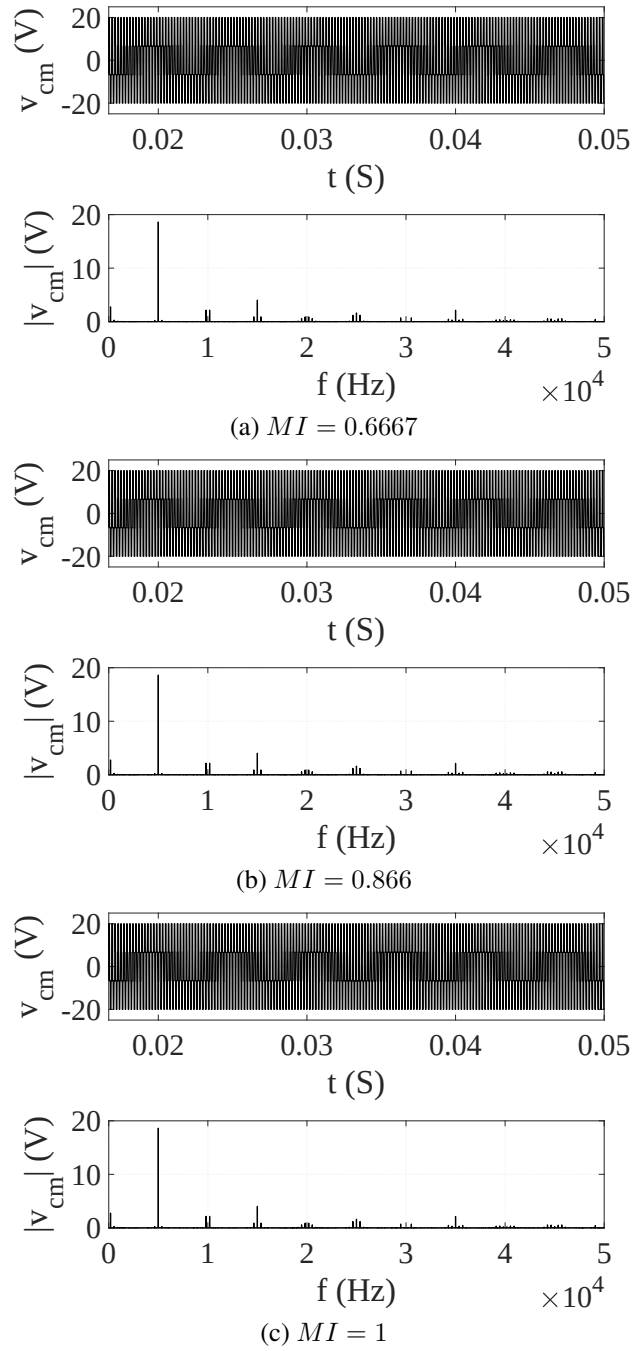


Figure 2.16 Common-mode voltage waveforms and their corresponding frequency spectrum using the regular SVPWM.

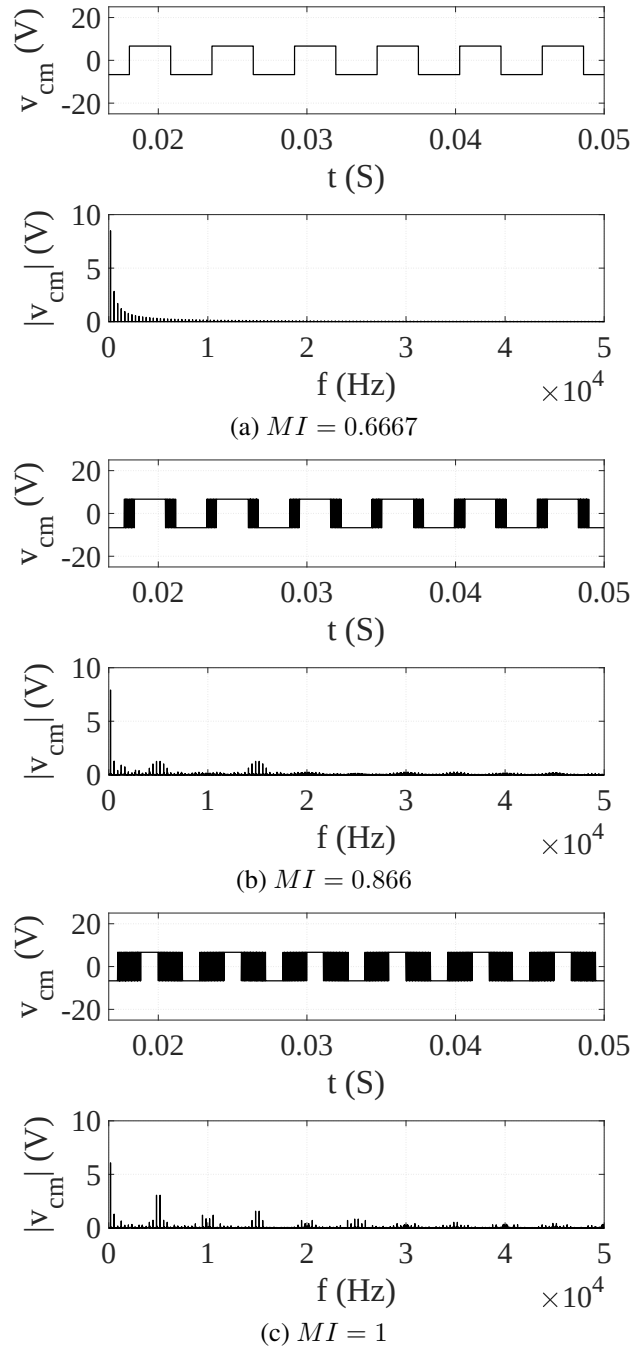


Figure 2.17 Common-mode voltage waveforms and their corresponding frequency spectrum using HSVPWMS I.

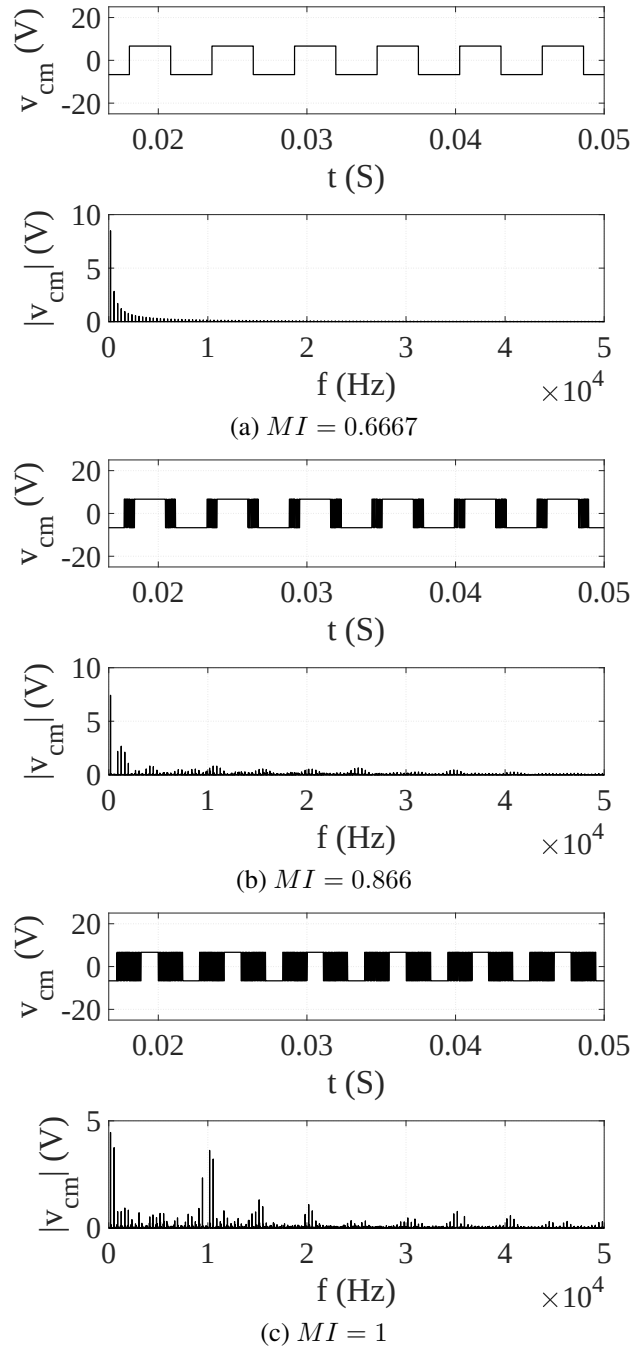


Figure 2.18 Common-mode voltage waveforms and their corresponding frequency spectrum using HSVPWMS II.

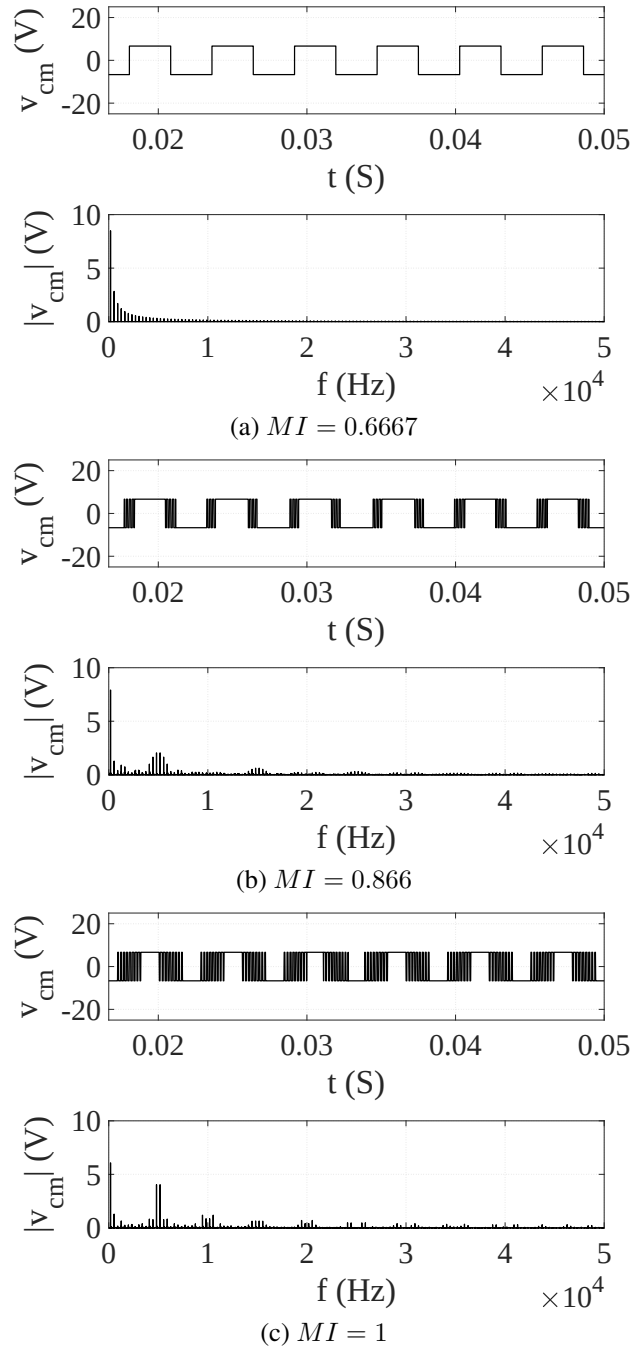


Figure 2.19 Common-mode voltage waveforms and their corresponding frequency spectrum using HSVPWMS III.

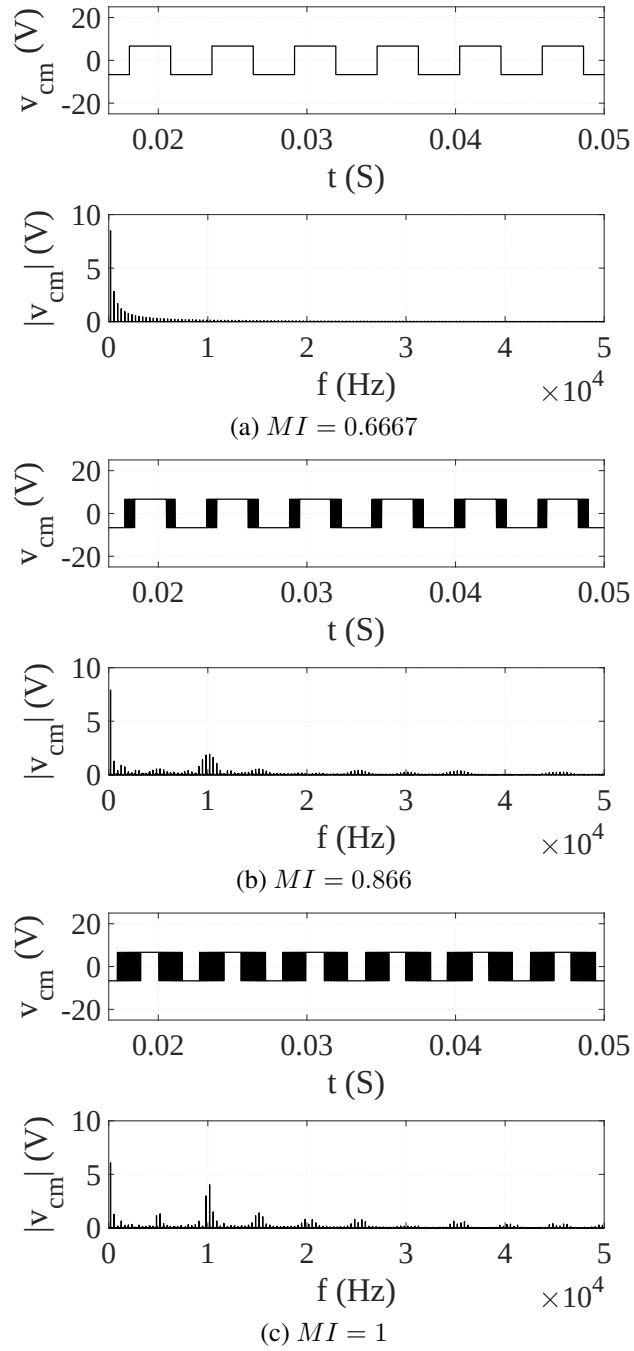


Figure 2.20 Common-mode voltage waveforms and their corresponding frequency spectrum using HSVPWMS IV.

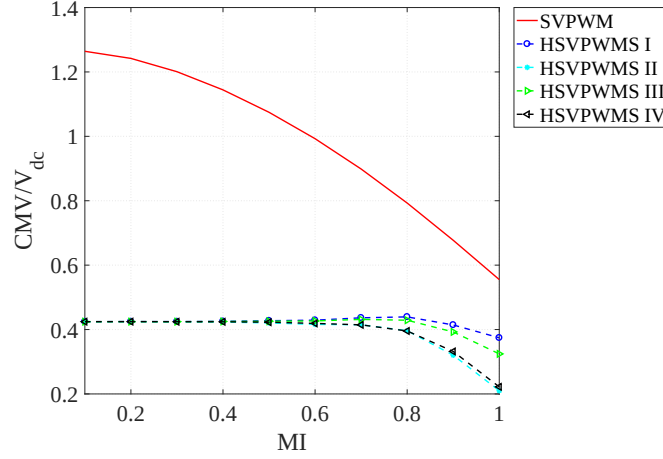


Figure 2.21 The fundamental component of the CMV. The fundamental frequency of the CMV in SVPWM is equal to $f_c = 5$ kHz. Whereas in HSVPWMS methods the frequency of the fundamental component is equal to $3f_1 = 180$ Hz.

$$\lambda_{hn} = \frac{\pi}{V_{dc}T_s} \lambda_h. \quad (2.25)$$

Each voltage utilization method results in a unique harmonic voltage vector trajectory. The normalized harmonic flux RMS value over a PWM (duty cycle δ of 0 to 1) is calculated as follows:

$$\lambda_{hn-rms}(MI, \theta) = K_f^2 \sqrt{\int_0^1 \lambda_{hn}^2 d\delta} \quad (2.26)$$

where K_f is the ratio of the switching per PWM cycle between the regular SVPWM and the HSVPWMS methods. In order to attain a fair comparison between HSVPWMS methods and the regular SVPWM method, all HSVPWMS methods are set to operate at the same switching frequency by dividing the carrier frequency of each method by K_f . Taking the average value of the RMS harmonic flux function over a full fundamental cycle results in the a harmonic distortion factor (HDF), which is a measure of the AC current ripple:

$$HDF = \frac{288}{\pi^2} \frac{1}{2\pi} \int_0^{2\pi} \lambda_{hn-rms} d\theta. \quad (2.27)$$

The hybrid harmonic distortion factor HDF_H is obtained by averaging the HDFs of each sequence based on the value of the modulation index as follows:

$$HDF_H = \begin{cases} HDF_{(\mathcal{O} \vee \mathcal{E})} & MI \leq \frac{4}{3\sqrt{3}} \\ M_p HDF_{(\mathcal{O} \vee \mathcal{E})} + (1 - M_p) HDF_{(\mathcal{E} \wedge \mathcal{O})} & MI > \frac{4}{3\sqrt{3}} \end{cases} \quad (2.28)$$

where M_p is the modulation parametric factor defined as

$$M_p = \frac{MI_{max} - MI}{\frac{2}{3\sqrt{3}}} \quad (2.29)$$

$HDF_{(\mathcal{O} \vee \mathcal{E})}$ is HDF calculated when only the odd vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ are applied or only the even vectors $\{\mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}\}$ are applied, depending on the location of the segments as described previously for each HSVPWMS. $HDF_{(\mathcal{O} \wedge \mathcal{E})}$ is HDF calculated when both odd and even vectors are applied $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(1,1,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,1,1)}, \mathbf{V}_{(0,0,1)}, \mathbf{V}_{(1,0,1)}\}$, depending on the selected group of vectors. When the MI is less than or equal to $\frac{4}{3\sqrt{3}}$, the HDF_H is identical to the HDF resulting from only odd vectors or only even vectors. When the MI is greater than $\frac{4}{3\sqrt{3}}$, the HDF_H is averaged based on the definition in (2.28). Fig. 2.22 shows the numerical results of HDF_H for all HSVPWMS along with the regular SVPWM. All the HSVPWMS methods present similar HDF in the region where $MI \leq \frac{4}{3\sqrt{3}}$. Although the HDF for HSVPWMS II is lower than the other hybrid methods, it presents higher CMV frequency as will be seen later in the results.

2.5.3 DC-Link Current Harmonics

The rms current on the DC side is important factor in determining the DC-link capacitor sizing [47]. To compare the behavior of the PWM methods, K_{dc} is defined in [29] as

$$K_{dc} = \frac{I_{in-h-rms}^2}{I_{1-rms}^2} \quad (2.30)$$

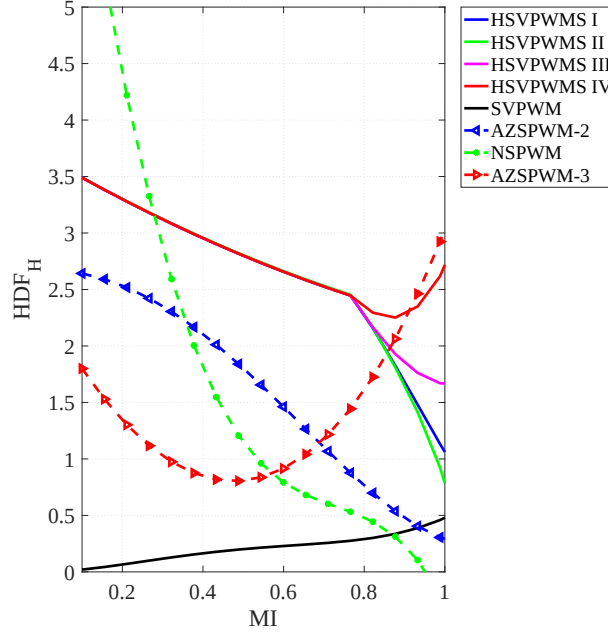
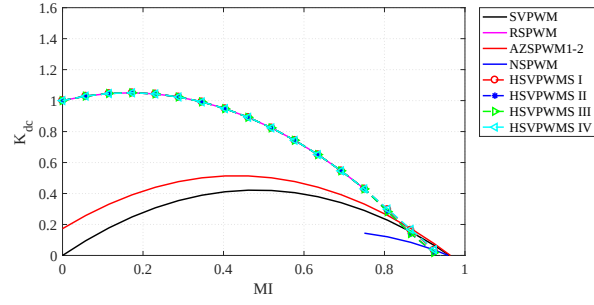


Figure 2.22 Harmonic distortion factor for the HSVPWMS methods compared with the conventional PWMS methods.

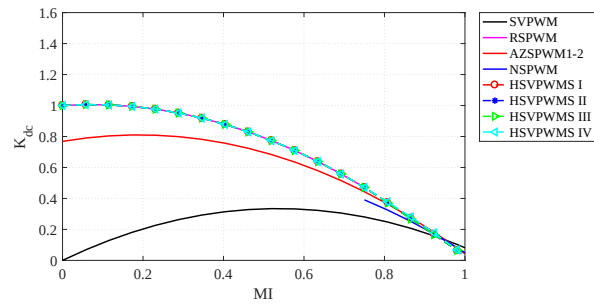
where $I_{in-h-rms}$ is the rms value of the DC-link current and I_{1-rms} is the fundamental component of the output rms current. The calculations for K_{dc} are performed numerically for different power factors. Fig. 2.23 (a) to (c) show K_{dc} for the HSVPWMS methods compared with the conventional SVPWM and CMV reduction methods. When the PF is high, K_{dc} for the hybrid methods is higher than the other methods. However, when operating at low PF , K_{dc} for the hybrid methods surpasses K_{dc} for all of the other CMV reduction methods. In general, K_{dc} for the all hybrid method is almost identical and decreases with decreasing the power factor.

2.5.4 Switching Losses

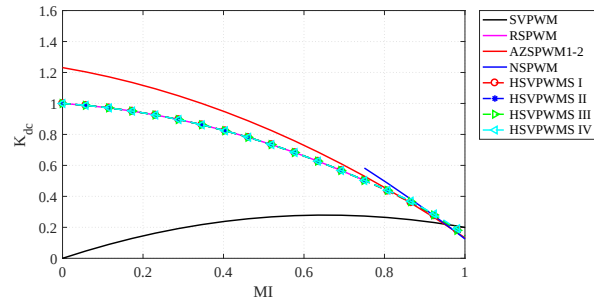
The switching losses for the VSI using HSVPWMS are calculated analytically by taking into account the effect of changing different vector syntheses over the switching frequency. The IGBT current and voltage do not abruptly change their values. Instead there is a transition interval in which both the current and voltage across the IGBT have values larger than zero [48, 50]. The



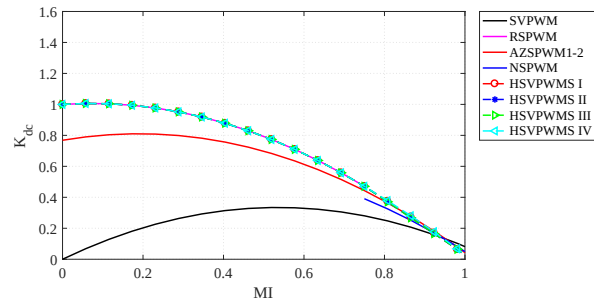
(a) $PF = 1$



(b) $PF = 0.8$



(c) $PF = 0.6$



(d) $PF = 0.4$

Figure 2.23 DC-link current ripple coefficient (K_{dc}) for various PWM methods.

average value of the switching losses can be calculated as follows:

$$P_{sw-IGBT} = f_s(MI) \left[\int_t^{t+t_r} i_C(t)v_{CE}(t)dt + \int_t^{t+t_f} i_C(t)v_{CE}(t)dt \right] \quad (2.31)$$

where f_s is the effective switching frequency that represents the number of switching instants for one IGBT in one fundamental frequency period, unlike the regular SVPWM. f_s in HSVPWMS is a function of the modulation index as shown in Table 2.8. i_C is the collector current, and v_{CE} is the voltage across the collector-emitter. t_r and t_f are the rising and falling times, respectively. The average switching losses per one IGBT can be integrate as follows: Equation (2.31) can be expanded by simple linear approximation of i_C and v_{CE} , except during turn off events, in which case i_C can be approximated as an exponentially decaying function as follows [48]

$$i_C(t) = I_L e^{-a(t-t_i)} \quad (2.32)$$

where t_i is the initial value of time in which the turn off event started and a is a constant that can be adjusted to achieve the best function approximation. To solve (2.32), it is assumed that at $t = t_i + t_f$, 95% of the collector current i_C vanishes. Therefore, a can be defined as a function of the falling time t_f as follows:

$$a = \frac{3}{t_f} \quad (2.33)$$

Therefore, the integral becomes

$$P_{sw-IGBT} = f_s(MI) \left[\int_0^{t_r} \frac{0}{t_r} i_C(2V_{dc} - \frac{t}{t_r} 2V_{dc})dt + \int_0^{t_f} I_L e^{-at} \frac{t}{t_f} 2V_{dc} dt \right] \quad (2.34)$$

$$P_{sw-IGBT} = f_s(MI) \left[\frac{1}{3} I_L V_{dc} t_r + \frac{2I_L V_{dc}}{t_f} \left(\frac{1 - e^{-at_f} (at_f + 1)}{a^2} \right) \right]. \quad (2.35)$$

Substituting (2.33) in (2.35) leads to

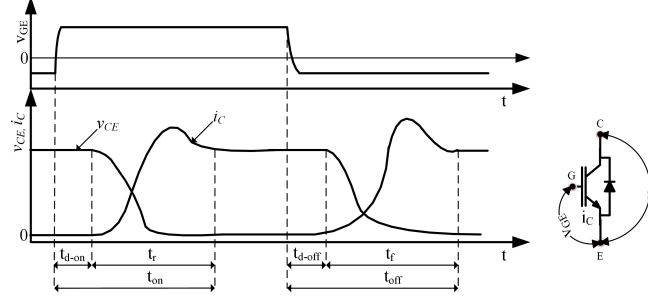


Figure 2.24 Switching on and off events for an IGBT.

Table 2.8 Effective switching frequency f_s defined as a function of the modulation index.

Modulation method	$f_s(MI) _{MI \leq \frac{4}{3\sqrt{3}}}$	$f_s(MI) _{MI > \frac{4}{3\sqrt{3}}}$
SVPWM	f_c	f_c
HSVPWM I	$2f_c$	$2M_p f_c + (1 - M_p) \frac{10}{6} f_c$
HSVPWM II	$2f_c$	$2M_p f_c + (1 - M_p) \frac{4}{3} f_c$
HSVPWM III	$2f_c$	$2M_p f_c + (1 - M_p) \frac{10}{6} f_s$
HSVPWM IV	$2f_c$	$2M_p f_c + (1 - M_p) \frac{3}{2} f_c$

$$P_{sw-IGBT} = f_s(MI) \left[\frac{1}{3} I_L V_{dc} t_r + \frac{9}{50} I_L V_{dc} t_f \right]. \quad (2.36)$$

The integration results leads to

$$P_{sw-IGBT} = f_s(MI) \left[\frac{1}{3} I_L V_{dc} t_r + \frac{9}{50} I_L V_{dc} t_f \right]. \quad (2.37)$$

The total switching losses also include the reverse recovery losses associated with the diode turn-off process:

$$P_{rr-D} = \frac{1}{2} f_s(MI) I_{rr} V_{dc} t_{rr} \quad (2.38)$$

where I_{rr} is the maximum value of the reverse recovery current, and t_{rr} is the reverse recovery time.

To obtain the effective switching frequency, the number of commutations per sampling time is counted as shown in the Table 2.8.

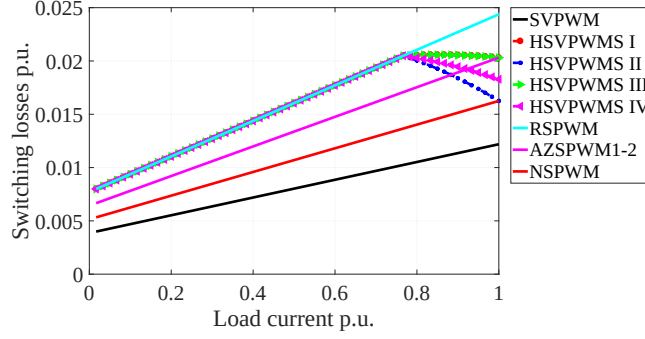


Figure 2.25 Switching losses for the HSPWMS methods compared with the conventional PWM methods.

2.6 Experimental results

The experimental work has been carried out using the following parameters and operating conditions: DC-link voltage 100 V carrier frequency $f_c = 5$ kHz and an RL load with 5Ω and 2 mH. The system consists of three inverter legs with each leg being realized by the IGBT module CM100DY-24A. The control algorithm is implemented using DSpace CP1103.

Fig. 2.26 shows the resulting CMV with $MI = 0.75$. The reference voltage vector is synthesized using only odd and only even states. This results in a square wave CMV with a frequency equal to $3f_1$ (three times the fundamental frequency of the system 180 Hz). Fig. 2.27 shows the FFT for the CMV with $MI = 0.75$. All of the CMV is concentrated at 180 Hz. The CMV frequency spectrum is the similar to the one in Fig. 2.27 at any $MI \in \{0, 0.766\}$.

Fig. 2.28 shows the CMV with $MI = 0.85$ for the proposed hybrid approach and several PWM methods. For the $MI > 0.766$, the reference voltage vector starts entering the odd-even region, leading to a CMV that fluctuates between the values of $\frac{V_{dc}}{3}$ and $-\frac{V_{dc}}{3}$. However, the CMV spectrum is still concentrated at 180 Hz frequency as shown in Fig. 2.29. The frequency spectrum for the conventional SVPWM and DPWM1 includes high amplitude CMV due to the use of the zero vector. This high amplitude is located at the carrier frequency (normally in kHz). The conventional CMV reduction PWM methods have lower CMV amplitudes, but they are still located at the carrier frequency. The main difference between the proposed method and the conventional CMV reduction methods is that the CMV frequency is decreased. A lower frequency CMV has

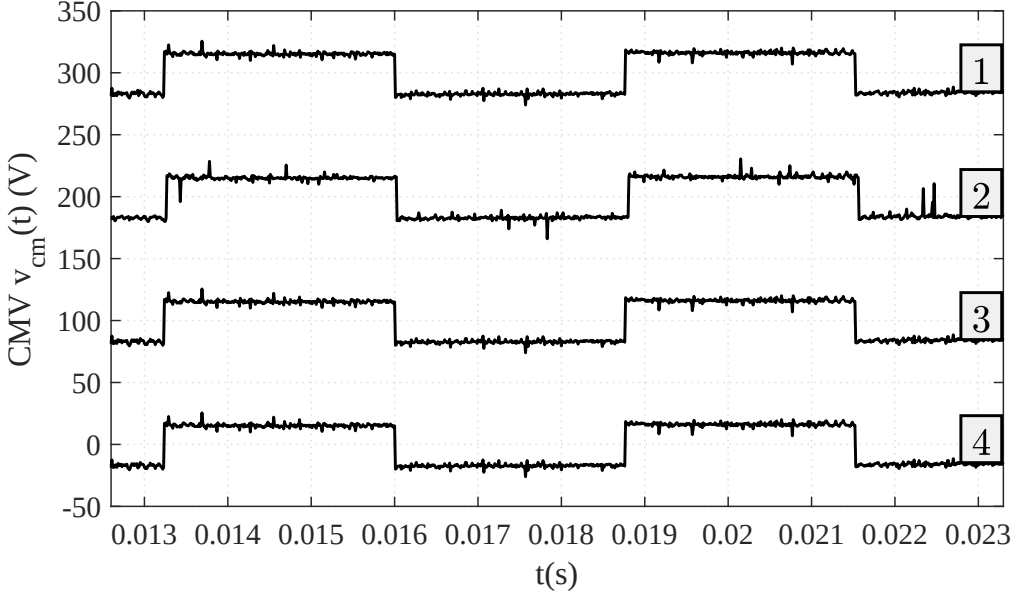


Figure 2.26 Experimental results for CMV at $MI = 0.75$ of 1 - HSVPWMS I, 2 - HSVPWMS II, 3 - HSVPWMS III, 4 - HSVPWMS IV.

two main advantages over a high frequency CMV. First, less CMV fluctuation corresponds to less EDM in the bearings. Second, a low frequency CMV can help meet the EMC standards because the amplitude limit for low frequencies is much higher than the amplitude limit for high frequencies.

Fig. 2.30 shows the CMV at $MI = 1$ for the proposed hybrid approach and several PWM methods. As the MI increases higher the implementation of only odd or only even synthesis decreases leading to high frequency CMV frequency components. However, the high frequency CMV components are still less than the ones resulting from the conventional CMV reduction methods as shown in Fig. 2.31.

Fig. 2.32 (a) and (b) show the load currents for the proposed methods along with the conventional PWM methods. Although the load is mostly resistive with $PF = 0.988$, current ripples resulting from the proposed hybrid methods are still comparable with the current ripples resulting from the conventional PWM methods. As the MI increases, the HDF of load currents for the proposed hybrid method improves because the reference voltage vector synthesis shifts from only odd and only even to odd-even.

Fig 2.33 (a) shows the CMV waveform without implementing the safe commutation algorithm.

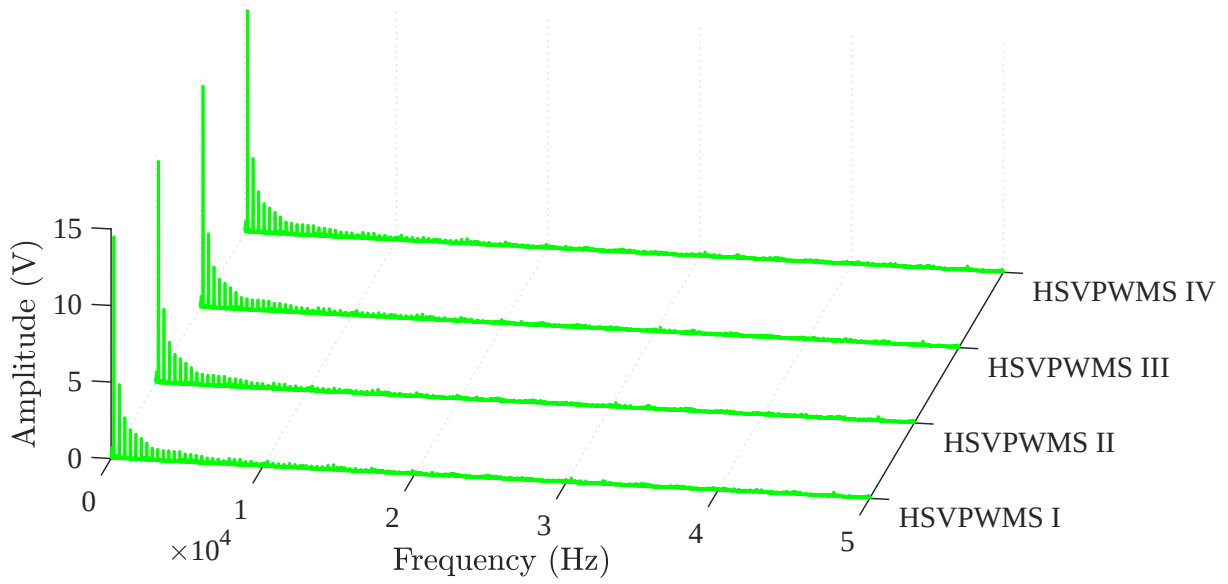


Figure 2.27 FFT of the CMV waveforms of 1 - HSVPWMS I, 2 - HSVPWMS II, 3 - HSVPWMS III, 4 - HSVPWMS IV.

There are two types of unwanted transitions during the dead-time intervals: Type 1, result in CMV equal to $|V_{dc}|$, and Type 2, result in CMV that changes sign from $\frac{V_{dc}}{3}$ to $-\frac{V_{dc}}{3}$ or vice versa. These unwanted CMV pulses can be fully avoided when the proposed commutation sequences is implemented as shown in Fig 2.33 (b).

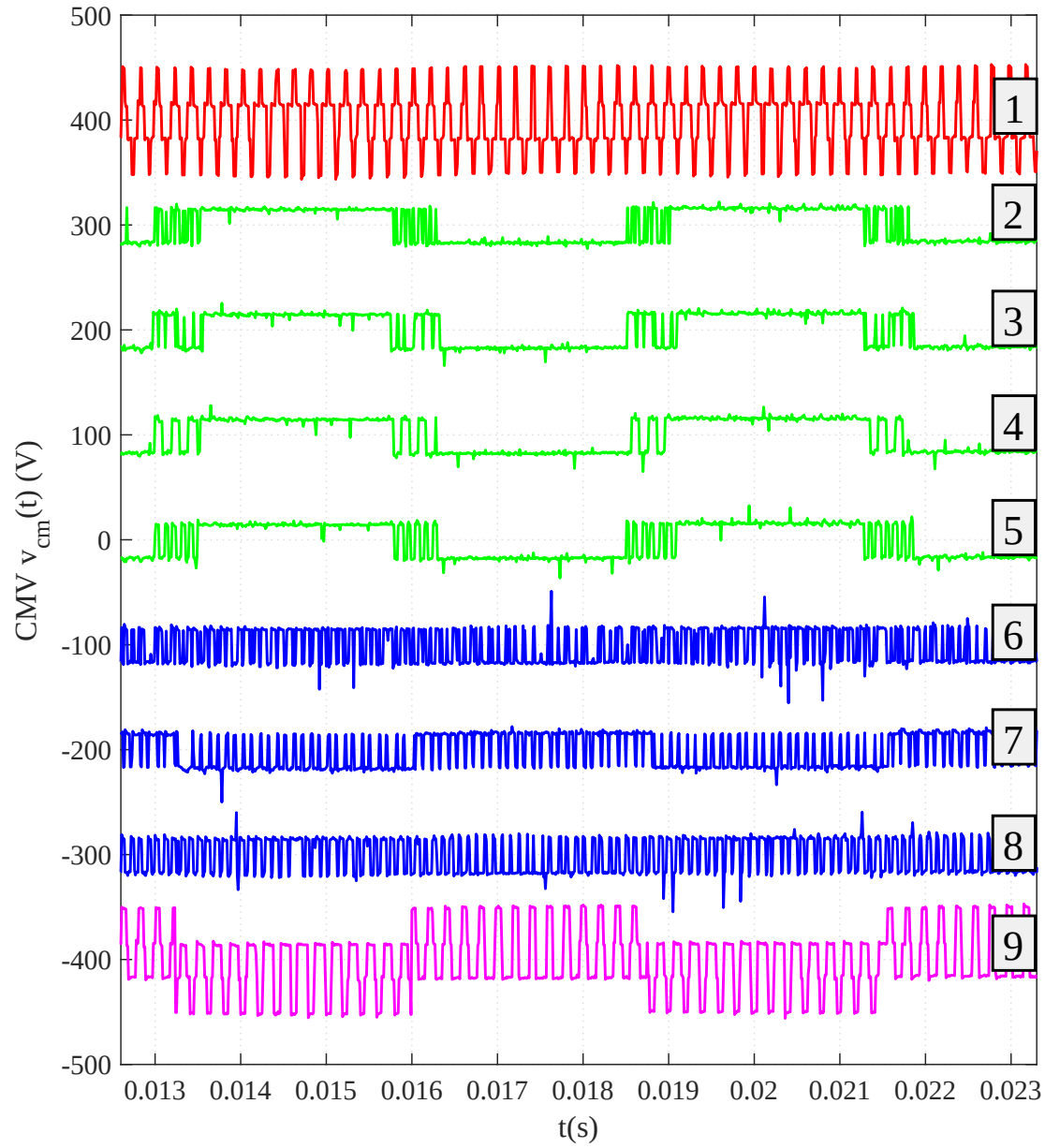


Figure 2.28 Experimental results of CMV waveforms at $MI = 0.85$ for 1 - SVPWM, 2 - HSVPWMS I, 3 - HSVPWMS II, 4 - HSVPWMS III, 5 - HSVPWMS IV, 6 - AZSPWM1-2, 7 - NSPWM, 8 - AZSPWM3, and 9 - DPWM1.

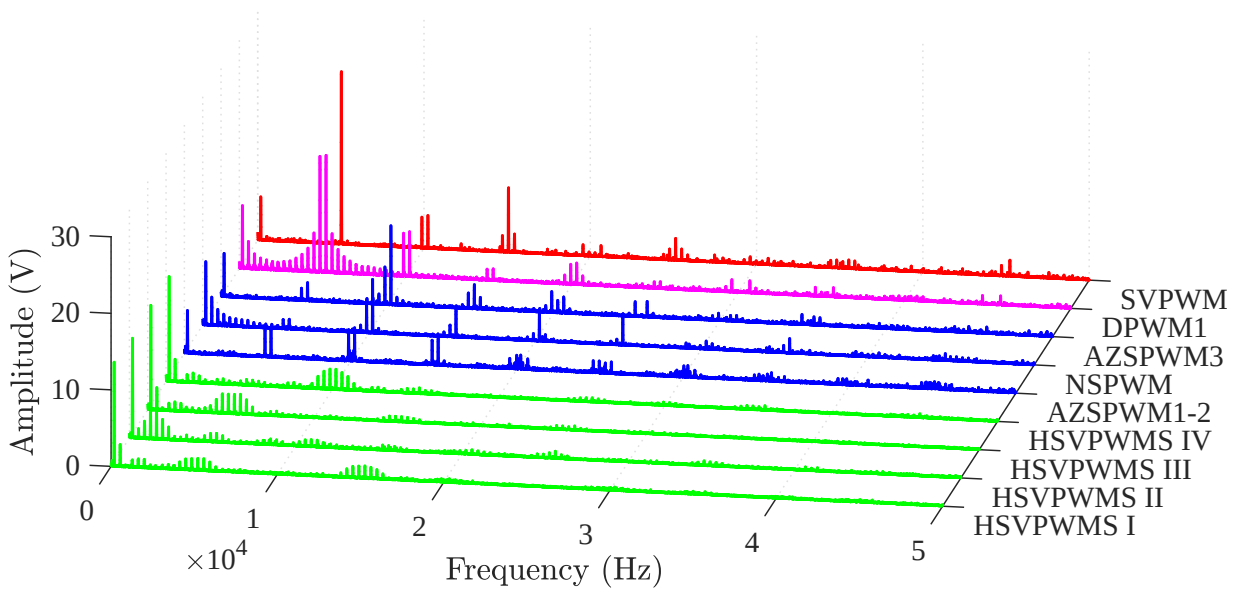


Figure 2.29 FFT of the CMV waveforms at $MI = 0.85$ for 1 - SVPWM, 2 - HSVPWMS I, 3 - HSVPWMS II, 4 - HSVPWMS III, 5 - HSVPWMS IV, 6 - AZSPWM1-2, 7 - NSPWM, 8 - AZSPWM3, and 9 - DPWM1.

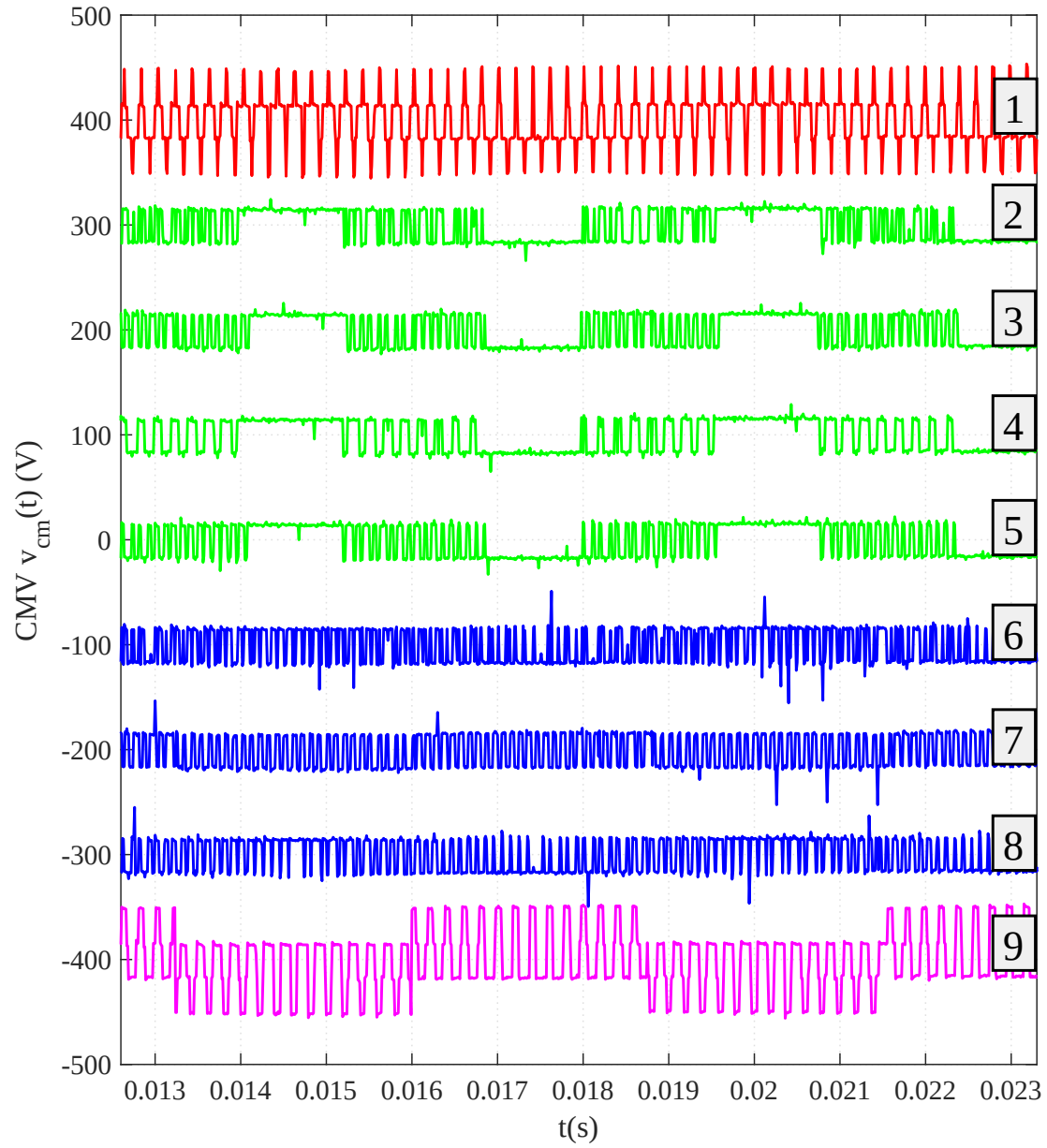


Figure 2.30 Experimental results of CMV waveforms at $MI = 1$ for 1 - SVPWM, 2 - HSVPWMS I, 3 - HSVPWMS II, 4 - HSVPWMS III, 5 - HSVPWMS IV, 6 - AZSPWM1-2, 7 - NSPWM, 8 - AZSPWM3, and 9 - DPWM1.

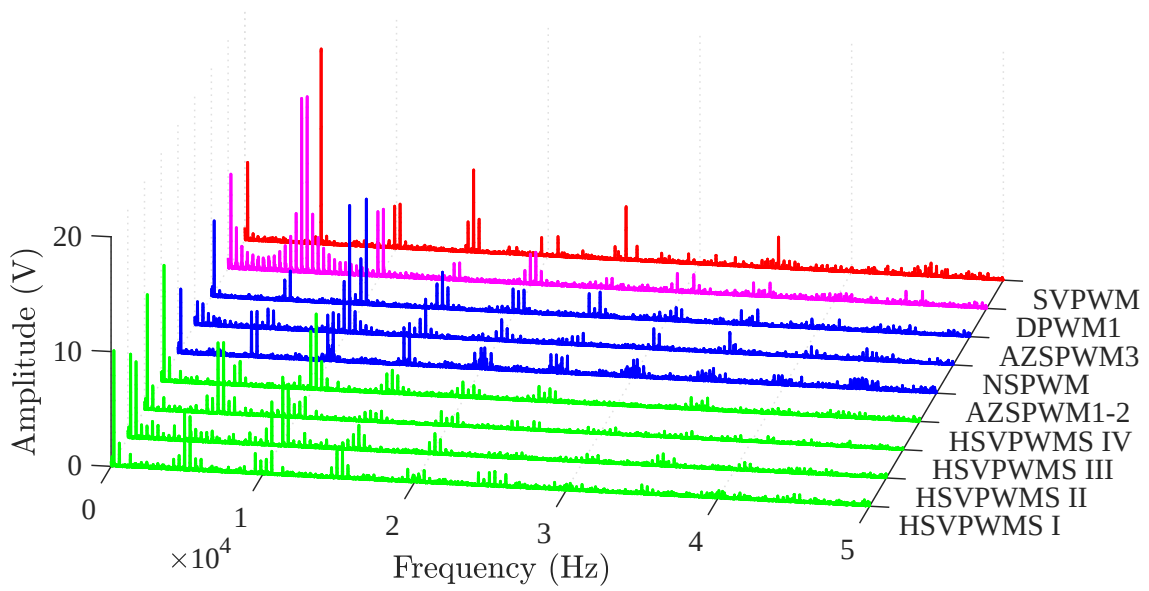
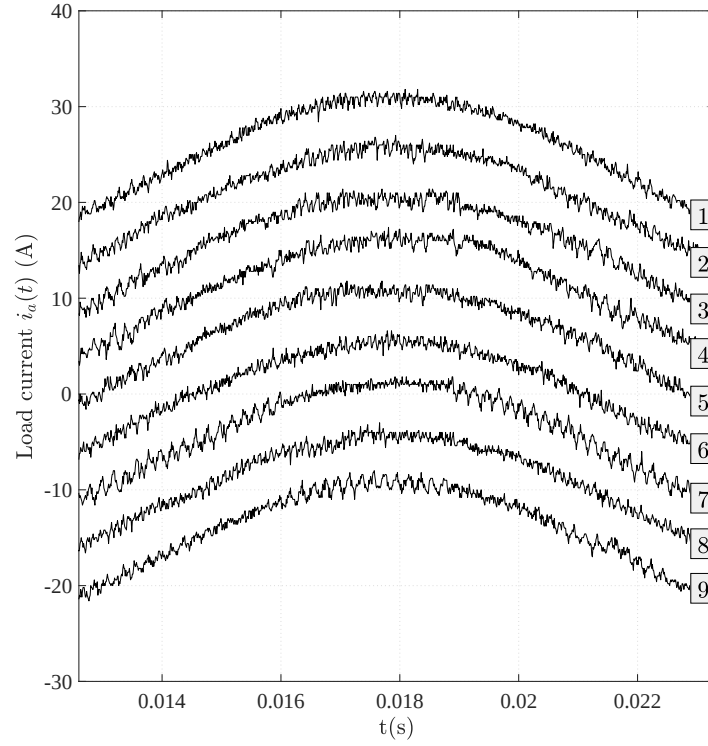
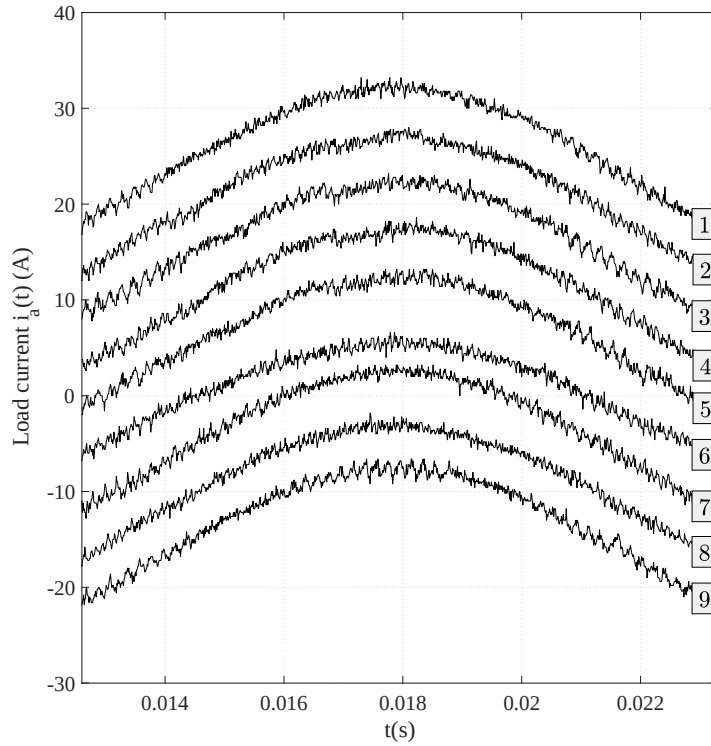


Figure 2.31 FFT of the CMV waveforms at $MI = 1$ for 1 - SVPWM, 2 - HSPWMS I, 3 - HSPWMS II, 4 - HSPWMS III, 5 - HSPWMS IV, 6 - AZSPWM1-2, 7 - NSPWM, 8 - AZSPWM3, and 9 - DPWM1.



(a)



(b)

Figure 2.32 Experimental results of the load current $i_a(t)$ at (a) $MI = 0.85$ and (b) $MI = 1$ for 1 - SVPWM+20A, 2 - HSVPWMS I+15A, 3 - HSVPWMS II+10A, 4 - HSVPWMS III+5A, 5 - HSVPWMS IV, 6 - AZSPWM1-2-5A, 7-NSPWM-10A, 8-AZSPWM3-15A, and 9-DPWM1-20A.

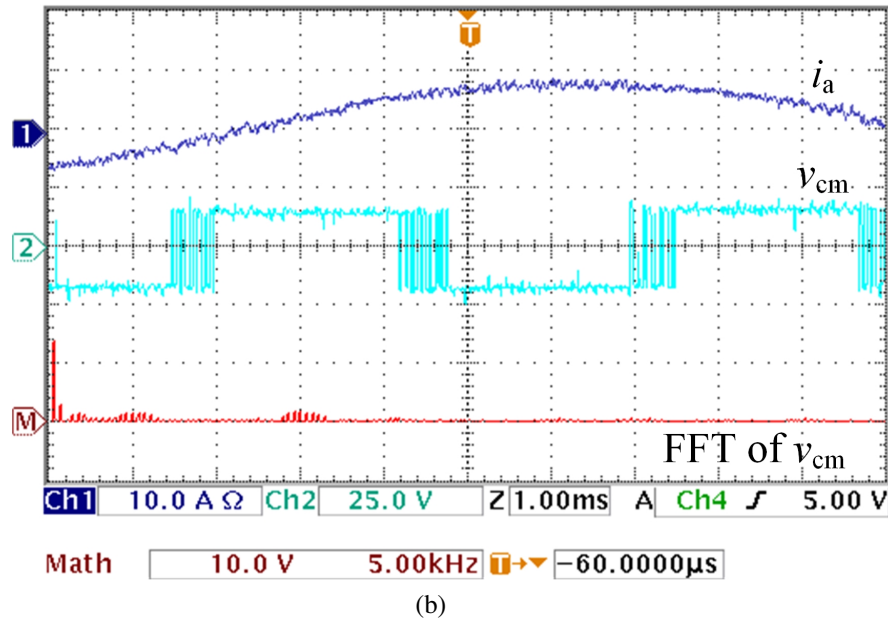
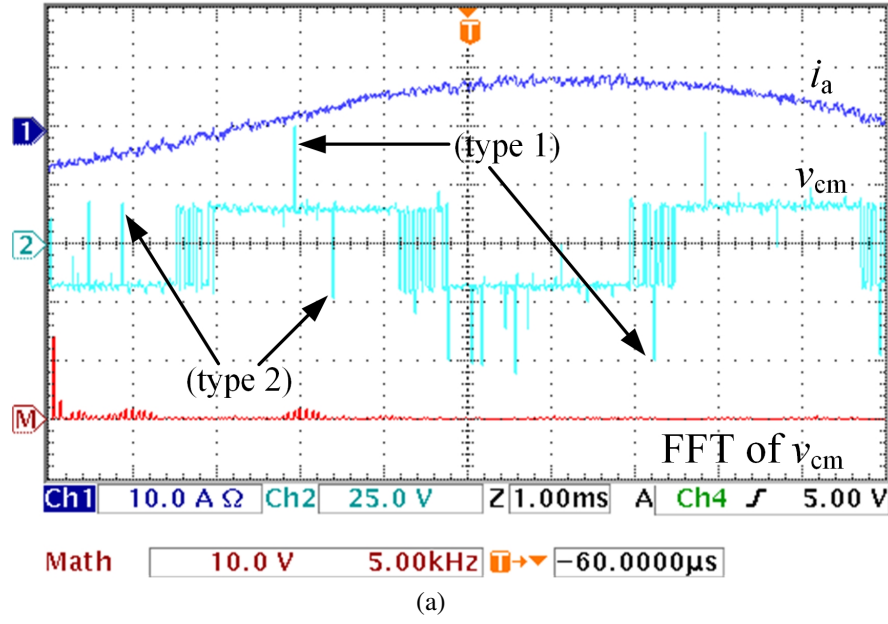


Figure 2.33 Experimental results of (a) the HSVPWMS II without implementing the safe commutation algorithm. During the dead-times the effective switching state could be one of the zero vectors $\mathbf{V}_{(0,0,0)}$ or $\mathbf{V}_{(1,1,1)}$ and the CMV will be similar to type 1, or it could be similar to type 2 when the effective switching state result in one of the odd or even vectors; (b) the HSVPWMS II with implementing the safe commutation algorithm, both type 1 and type 2 unwanted transitions are successfully avoided. $MI = 0.85$.

Chapter 3

Model Predictive Approach to Control the Amplitude and Frequency of CMV in VSI Drives

Ever since the invention of the IGBT increasing the switching frequency of the power converter has been a trend due to the reduction of the footprint and the increase of power density [1]. Recent development of wide-bandgap devices has equipped the power switches with even faster switching speed [3]. However, the increase in the switching frequency has generated several unwanted consequences, one of which is the high-frequency common-mode voltage (CMV) [4]. The high-frequency CMV can cause electromagnetic interference (EMI) that adversely affects the other components of the system [7]. The induced over-voltage stress to the winding insulation of the drives can also increase the shaft current [8]. In particular, the shaft current is the result of the fluctuation of the CMV, which is strictly related to the sequence of the inverter switching states [9]. Several studies presented in the literature discussed the methods of mitigating CMV effects. They can be classified into hardware solutions and algorithmic solutions. Before using the additional passive components, it is essential to provide proper earthing paths to allow the stray current to return to the inverter frame rather than through the machine bearings [51].

The hardware ones require either increasing the number of the inverter switches [11], passive components [16], or both [26]. The study in this chapter is mostly related to the algorithmic approaches that require no additional hardware.

On the other hand, algorithmic approaches can be implemented on the existing hardware and offer minimization of the CMV without any additional costs. The early attempt to reduce the CMV proposed in [9] uses only the odd or only the even voltage vectors. Utilizing only odd or even vector has several drawbacks, such as decreasing the linear region to $MI \leq \frac{4}{3\sqrt{3}}$, degrading the inverter efficiency by increasing the switching losses, and increasing the total harmonic distortion (THD). Later a number of CMV reduction methods were proposed such as the active zero states PWM (AZSPWM1-2 and AZSPWM3), remote state PWM (RSPWM1, RSPWM2, and RSPWM3) [29], and near-state PWM (NSPWM) [28]. In each one, several active voltage vectors are utilized to meet the voltage second requirements and avoid using the zero vectors. The non-zero switching vectors generate lower magnitude CMV but the conventional space vector PWM uses zero vectors as it helps in reducing the THD [32]. Although the latter methods utilize all of the linear region (except for NSPWM), the high frequency of the CMV remains an issue. The high common-mode $\frac{dv}{dt}$ causes electric discharge machining (EDM) across the bearing races. Furthermore, the CMV reduction methods assume ideal switches and fail when nonlinearities such as the dead-time and line-line voltage reversal are considered [34].

Recently, model predictive control (MPC) method has been developed as a simple and effective control technique for power converters without using PWM modulator [52]. The MPC method shows that it is very easy to implement all of the six-active-vector approaches and the three-active-vector approaches [53]. Also, it is possible to apply a restriction on the CMV by adding a penalty term in the objective function. However, those methods did not bring much improvement over the conventional PWM methods and did not fully demonstrate the capabilities of MPC methods. Instead, all of the proposed MPC CMV reduction methods were a direct translation to what previously proposed using PWM methods. None of the CMV reduction methods in the literature offer the ability to arbitrarily shape the frequency and the amplitude of the CMV.

In this chapter, a novel approach to control the amplitude and the frequency of the CMV, rather than minimizing it, is proposed. The control concept is based on modifying the existing MPC method such that CMV can be generated at any arbitrarily set frequency and with minimized amplitude. It is shown that the proposed algorithm allows arbitrarily adjusting the amplitude and the frequency of CMV while maintaining low load current THD. The ability to shape the spectrum of CMV makes it possible to use the high-frequency machine impedance as a filter and reduce the resulting common-mode current.

The proposed method can be considered as a generalization of the existing approaches that include the three-active-vector methods, when the CMV frequency is set to zero and the six-active-vector methods, when the CMV frequency is set to maximum. Therefore, the proposed method can offer optimal trade-off between the two control areas.

The rest of the chapter is organized as follows. Following the introduction, the conventional MPC common-mode reduction method are reviewed in Section 3.1. The proposed MPC method is presented in Section 3.2. The reduction of bearing current is presented in Section 3.3. Finally, the experimental results presented in Section 3.4.

3.1 Conventional Model Predictive Common-mode Reduction Methods

The model predictive controller for the three-phase inverter shown in Fig. 3.1 is dependent on accurate modeling of the load dynamics. For three-phase resistive-inductive (RL) load, the load voltage equation can be written in the space vector notation as follows:

$$\mathbf{v} = L \frac{d\mathbf{i}}{dt} + R\mathbf{i} \quad (3.1)$$

where $\mathbf{v}$ and $\mathbf{i}$ are the voltage vector and the current vector in the complex plane, respectively. L and R are the inductance and the resistance of the load, respectively. Replacing load current

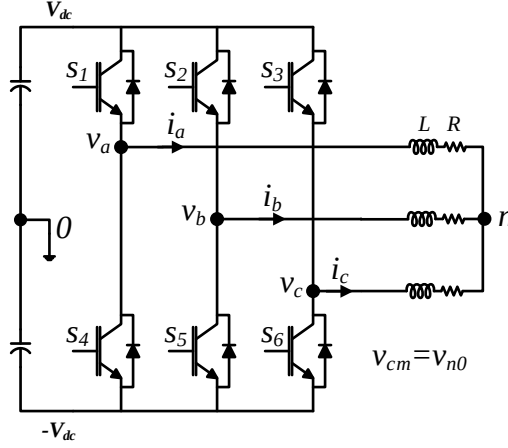


Figure 3.1 Three-phase voltage source inverter.

derivative $\frac{d\mathbf{i}}{dt}$ in (3.1) by Euler forward approximation results in the following discrete equation for the future load current

$$\mathbf{i}_{(k+1)} = \left(1 - \frac{RT_s}{L}\right)\mathbf{i}_{(k)} + \frac{T_s}{L}\mathbf{v}_{(k)} \quad (3.2)$$

where T_s is the sampling period, $\mathbf{i}(k+1)$ is the one step horizon predicted current. In some cases the second step horizon current $\mathbf{i}(k+2)$ is used to compensate the calculation delay. The objective of the model predictive controller is to minimize the error between the measured load current and command reference value through a proper formulation of the objective function. Which is typically in the form of mean square error between the current command and the predicted currents resulting from all the eight possible voltage vectors;

$$J = \left[\Re \mathbf{i}_{(k+N)}^* - \Re \mathbf{i}_{(k+N)}\right]^2 + \left[\Im \mathbf{i}_{(k+N)}^* - \Im \mathbf{i}_{(k+N)}\right]^2 \quad (3.3)$$

where $\mathbf{i}_{(k+N)}^*$ is the reference current and N is number of prediction horizon. In our case N is equal to one because the calculations delay is negligible for high sampling frequency. The voltage vector that minimize J is applied during the entire sampling period T_s can be obtained as follows:

$$\mathbf{v}_{(k+N)}^{opt} = \arg \min_{\mathbf{v}_{(.,.,.)}} \{J\} \quad (3.4)$$

where $\mathbf{v}_{(.,.,.)}$ is to be chosen from the eight available voltage vectors shown in Table 3.1.

Table 3.1 Voltage vectors and the corresponding differential-mode voltage $\mathbf{v}_{dm}$ and CMV v_{cm} amplitudes.

Voltage vector	v_{an}	v_{bn}	v_{cn}	$\mathbf{v}_{dm}$	v_{cm}
$\mathbf{V}_{(0,0,0)}$	$-V_{dc}$	$-V_{dc}$	$-V_{dc}$	0	$-V_{dc}$
$\mathbf{V}_{(1,0,0)}$	V_{dc}	$-V_{dc}$	$-V_{dc}$	$\frac{4}{3}V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,1,0)}$	V_{dc}	V_{dc}	$-V_{dc}$	$(\frac{2}{3} + j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,1,0)}$	$-V_{dc}$	V_{dc}	$-V_{dc}$	$(-\frac{2}{3} + j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,1,1)}$	$-V_{dc}$	V_{dc}	V_{dc}	$-\frac{4}{3}V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(0,0,1)}$	$-V_{dc}$	$-V_{dc}$	V_{dc}	$(-\frac{2}{3} - j\frac{2}{\sqrt{3}})V_{dc}$	$-\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,0,1)}$	V_{dc}	$-V_{dc}$	V_{dc}	$(\frac{2}{3} - j\frac{2}{\sqrt{3}})V_{dc}$	$\frac{V_{dc}}{3}$
$\mathbf{V}_{(1,1,1)}$	V_{dc}	V_{dc}	V_{dc}	0	V_{dc}

The CMV v_{cm} is defined as the voltage between the n and 0 in Fig. 3.1. It can be expressed in terms of the phase voltages as follows:

$$v_{cm} = v_{n0} = \frac{v_{an} + v_{bn} + v_{cn}}{3} \quad (3.5)$$

since we have a very good idea of what would be the phase voltages during each switching combination we can calculate all of the corresponding valued of the CMV using (3.5) as shown in Table. 3.1. The highest CMV $v_{cm} = \pm V_{dc}$ corresponds to the zero vectors when all of the three-phase loads are connected to either the upper or the lower DC-rail. Furthermore, there are three even voltage vectors that result in $v_{cm} = \frac{V_{dc}}{3}$ and three odd voltage vectors result in $v_{cm} = -\frac{V_{dc}}{3}$. In the conventional MPC method the choice of the voltage vector strictly depends on the objective function. Therefore, the CMV can potentially have any value from the ones shown in Table 3.1. To restrict this drawback various approaches have been presented in the literature. Fig. 3.2 shows the classification of model predictive CMV reduction methods. The authors briefly explain the merits and demerits of each approach. It is important to note that the point of interest here is the MPC methods and not the PWM method. The interested reader may check [28] for PWM CMV reduction methods analysis.

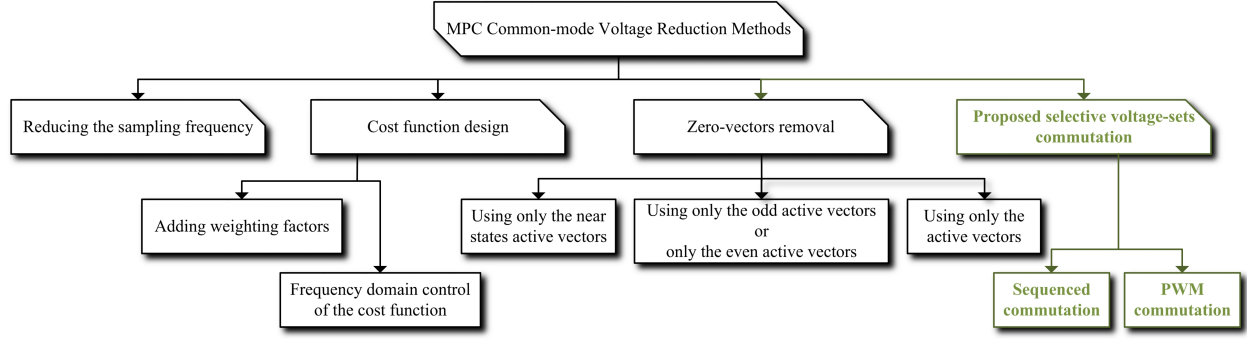


Figure 3.2 Model predictive CMV reduction methods diagram.

3.1.1 Reducing the Sampling Time

The maximum switching frequency of a converter controlled by MPC method is unknown parameter but it is upper bounded by the sampling frequency $f_{sw} \leq f_s/2$ where $f_s = \frac{1}{T_s}$. Observations from the hardware implementation show that the switching frequency of VSI with RL load is always between $\frac{1}{5} f_s$ and $\frac{1}{4} f_s$. Furthermore, results from [54] and [55] show that the area of the ultimate invariant set in which the error value converge to is inversely proportional to the sampling frequency. Therefore, reducing the sampling frequency f_s leads to more substantial current tracking error and reduced stability margin.

3.1.2 Cost Function Redesign (CFR-MPC)

One of many benefits of MPC is that the cost function can include all kinds of complex nonlinearities which makes the MPC method a multi-objective optimal control method. The design of the cost function can be blue divided into two subcategories:

3.1.2.1 Adding Weighting Factor

A secondary term can be added to the cost function to add another control objective beside the main control objective, which is in our case the current reference tracking. The dominance of the

secondary term or terms is adjusted via weighting factor λ as follows:

$$J_{\text{multi-obj.}} = \underbrace{J_{\text{single-obj.}}}_{\text{primery term}} + \underbrace{\lambda_1 J_{\text{single-obj.1}} + \dots + \lambda_n J_{\text{single-obj.n}}}_{\text{secondary terms}} \quad (3.6)$$

where $J_{\text{single-obj.1}}$ can be the predicted value of the CMV $|v_{cm} - v_{cm}^p|$ or $|v_{cm}^p|$ and λ_1 is the weighting factor. The first formulation for the secondary objective function restricts the change in CMV when making a control decision. As the value of λ increases the frequency of the CMV decreases with some sacrifice on the THD of the load current. The second formulation makes the MPC controller chose the vectors that correspond to a low CMV, immediately disregarding the use of the zero vectors. However the second formulation becomes unnecessary when λ increases since the CMV for all of the active vectors of the VSI is equal to $|\frac{V_{dc}}{3}|$. The reduction of CMV can also be achieved in less direct way by adding constrain on the switching frequency or the number of actuation [56]. In spite of using weighting factor is easy to implement, the stability of the converter is comprised. The weighting factor should be tested empirically by starting from zero and increasing it in a very small steps until the desired behavior is obtained. Furthermore, it has been shown that in most cases the control over the secondary term is not linearly related to the change in the weighting factor which makes the behavior of the inverter unpredictable [57].

3.1.2.2 Frequency Domain Control of the Cost Function

The cost function can be controlled by augmenting a filter to achieve additional degree of objective function. Although this was initially proposed to shape the load current spectrum [59] and control the thermal stress [60], they both used to control the switching frequency of the converter and hence controlling the CMV.

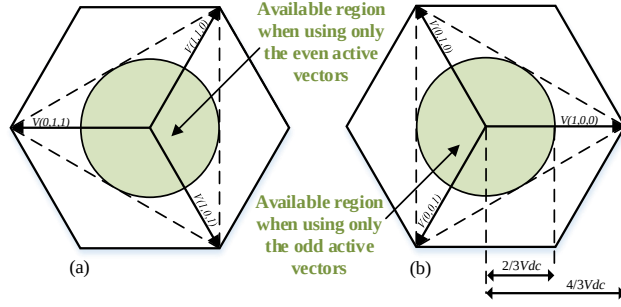


Figure 3.3 The highlighted region is the available linear region in: (a) using the even vectors only; (b) using the odd vectors only.

3.1.3 Zero-vectors Removal (6V-MPC)

As it has been shown that the zero-vectors $V_{(0,0,0)}$ and $V_{(1,1,1)}$ produce $-V_{dc}$ and V_{dc} CMV amplitudes, respectively. This is three time greater than the CMV amplitude produced when employing any of the other six active-vectors. There are few methods based on the zero-vector removal such as

3.1.3.1 Using Only the Active Vectors

Only the nonzero voltage vector can be used to minimize the current error [61]. This limit the CMV amplitude to $|\frac{V_{dc}}{3}|$.

3.1.3.2 Using Only the Odd or the even Active Vectors

Although, the previous method reduces the CMV to $|\frac{V_{dc}}{3}|$, it's switching frequency is relatively high due to the switching between the nonadjacent vectors [58]. The CMV can be a constant DC value if either only the odd or only the even active vectors are included in the finite-set of the objective function. However, this results in a significant reduction in the linear region to $MI \leq \frac{2}{3}$ as shown in Fig. 3.3.

The recently proposed zero-vector removal methods are all translation from what it have been proposed by Hava [28] using PWM. They do not fully exploit the effectiveness and abilities of the MPC method. Therefore, a new selective voltage-set MPC (SVS-MPC) method is proposed next.

3.2 Proposed Selective Voltage-sets Commutation MPC Method

The odd active vectors $\{\mathbf{V}_{(1,0,0)}, \mathbf{V}_{(0,1,0)}, \mathbf{V}_{(0,0,1)}\}$ produce CMV amplitude equal to $-\frac{V_{dc}}{3}$ and the even active vectors $\{\mathbf{V}_{(0,1,1)}, \mathbf{V}_{(1,0,1)}, \mathbf{V}_{(1,1,0)}\}$ produce CMV amplitude equal to $+\frac{V_{dc}}{3}$. Therefore, by selecting one of these two voltage set at a time, the concept of voltage-sets commutation can be realized. The selective voltage set MPC achieve control over the amplitude and the frequency of the CMV. Furthermore, the linear region can be extend such that the modulation index can be increased to maximum based on the rate of the commutation. The commutation between odd set to even set or even set to odd set can be easily implemented by defining three virtual voltage vectors as follows:

$$\mathbf{v}_x = h\mathbf{V}_{(1,0,0)} + (1-h)\mathbf{V}_{(0,1,1)} \quad (3.7)$$

$$\mathbf{v}_y = h\mathbf{V}_{(0,1,0)} + (1-h)\mathbf{V}_{(1,0,1)} \quad (3.8)$$

$$\mathbf{v}_z = h\mathbf{V}_{(0,0,1)} + (1-h)\mathbf{V}_{(1,1,0)} \quad (3.9)$$

where $\mathbf{v}_x, \mathbf{v}_y$, and $\mathbf{v}_z$ belong to the set of the active non zero vectors $\{V_{1,0,0}, V_{1,1,0}, \dots, V_{1,0,1}\}$. $h \in \{0, 1\}$ is a discrete-valued function of the CMV modulation signal. It can be either one or zero. When $h = 1$, only the odd active-vectors are used. When $h = 0$, only the even active-vectors are used. By only controlling h in (3.7), (3.8) and (3.9) the concept of commutation between the odd and the even vectors can be extended such that the entire linear region is available and the control over the frequency of the CMV is realized as shown in Fig. 3.4.

The load current predictive model block diagram is illustrated in Fig 3.5 and the means square error (MSE) objective function is illustrated in Fig 3.6. Note that the measured load current is transformed from abc to $\alpha\beta$ stationary reference frame using Clarke transformation. The algorithms as well have the flexibility to extrapolate the input reference current and increase the number of prediction horizon N .

1. Sequenced Commutation (SC): In which the commutation between odd and even vector occurs every n sampling times. Therefore, we can define the ratio between the odd vector

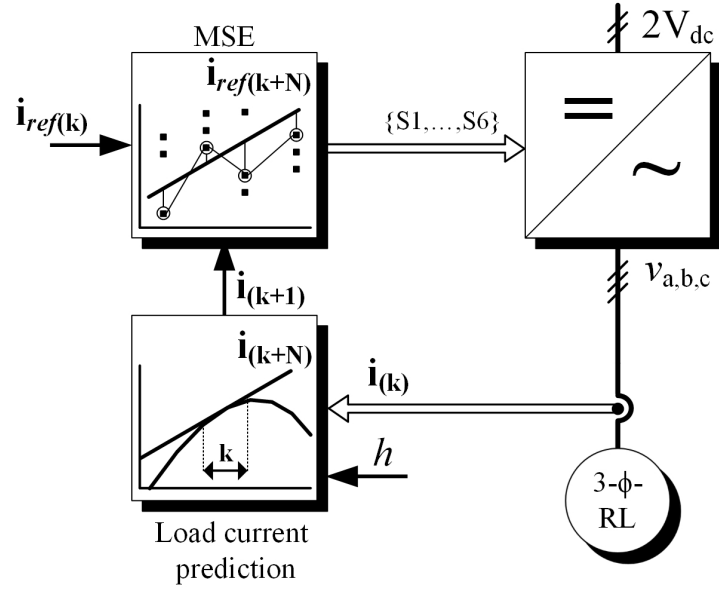


Figure 3.4 Control block diagram of the three-phase VSI with SVS-MPC controller.

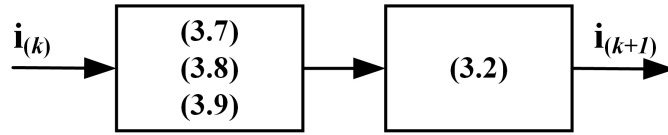


Figure 3.5 Load current prediction.

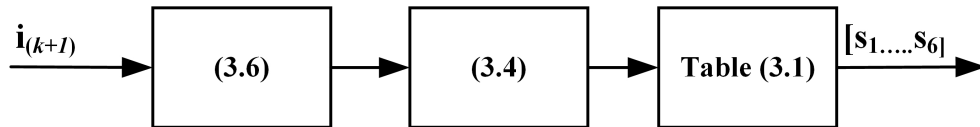


Figure 3.6 Objective function in a form of mean square error (MSE).

implementation and the even vectors implementation as

$$nT_s = n_oT_s + n_eT_s \quad (3.10)$$

$$D_{oe} = \frac{n_o}{n_o + n_e} \quad (3.11)$$

where $\{n_o, n_e \in \mathbb{N} : n_o, n_e \leq n\}$. In our case the realization is simplified by comparing triangular carrier with a constant number and D_{oe} is set to 50%. In contrary, when $D_{oe} = 100\%$ only the odd vectors are used and when $D_{oe} = 0\%$ only the even vectors are used.

2. Pulse Width Modulation Commutation (PWMC): In which the the frequency and amplitude of the CMV are modulated by using sinusoidal duty ratio D_{oe} .

A Simulink model for the system shown in Fig. 3.1 is built to simulate the two approaches. Fig. 3.7 shows the sequenced commutation approach when the system fundamental frequency is 60 Hz and the $MI = 0.9$. Although the sampling time for the MPC algorithm is set to $10 \mu s$ the CMV frequency spectrum is concentrated at the commutation frequency 5 kHz.

Fig. 3.10 shows the PWM approach when the system fundamental frequency is 60 and the $MI = 0.9$. The CMV is concentrated at the CMV carrier frequency 5 kHz. For the PWM method, the CMV amplitude at the carrier frequency can be changed based on the CMV reference level. At high modulation index the CMV reference amplitude should not exceed 0.45 in order to achieve acceptable load current THD. Fig. 3.9 shows the trade-off between the reference amplitude setting and the corresponding load current THD. As the reference amplitude increases the CMV at the corresponding frequency (60 Hz) increases with some sacrifice on the load current THD.

Decoupling the frequency of the CMV from the sampling frequency of the MPC method provides an extra degree of freedom to limit the bearing current. In the next section the bearing current for the proposed method will be compared with the ones from the conventional MPC methods.

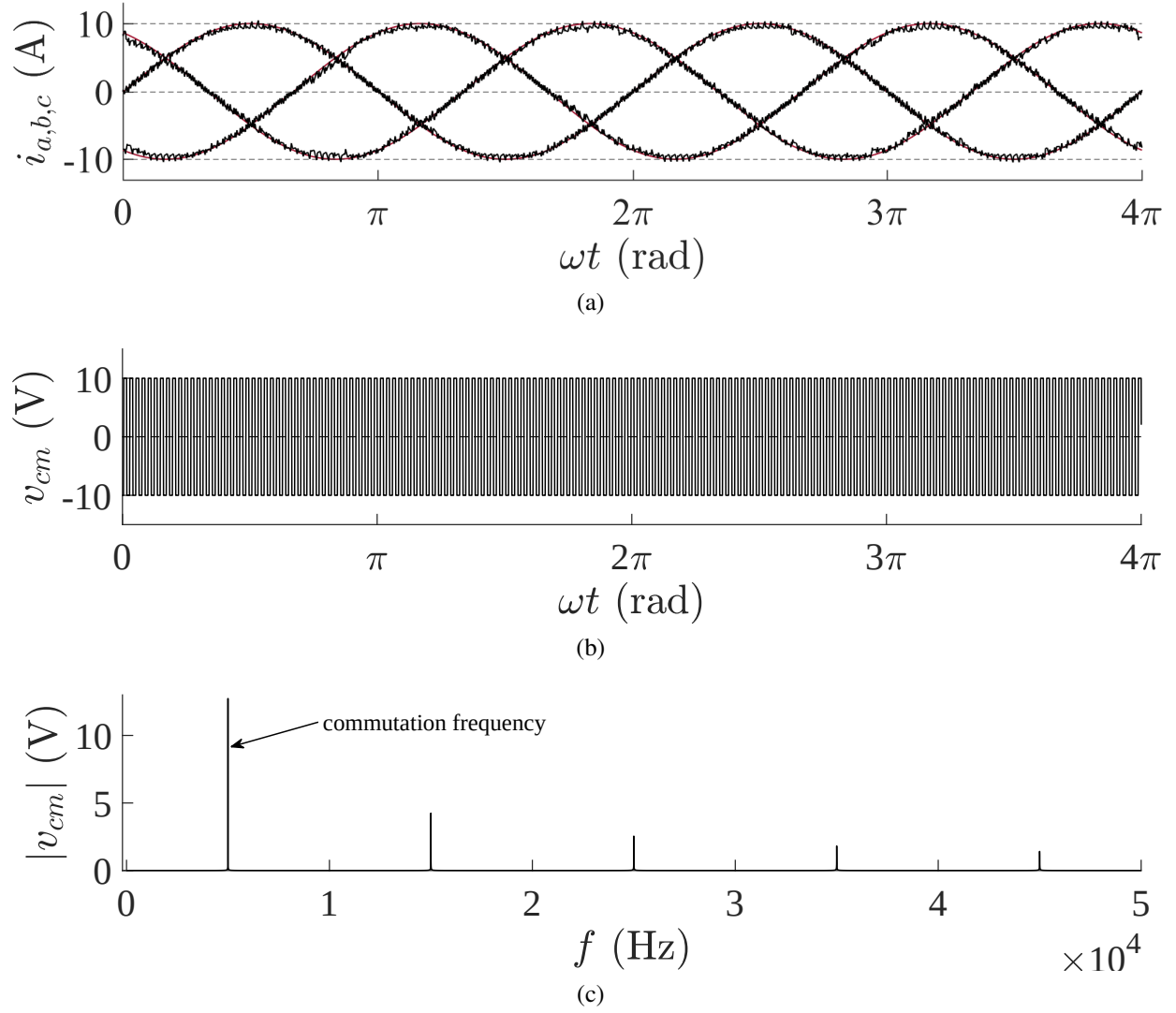


Figure 3.7 Simulation results of MPC-SC at 60 Hz fundamental frequency. $T_s = 10 \mu s$, $1/nT_s = 5$ kHz, $D_{oe} = 50\%$. Load current THD= 4.2%.

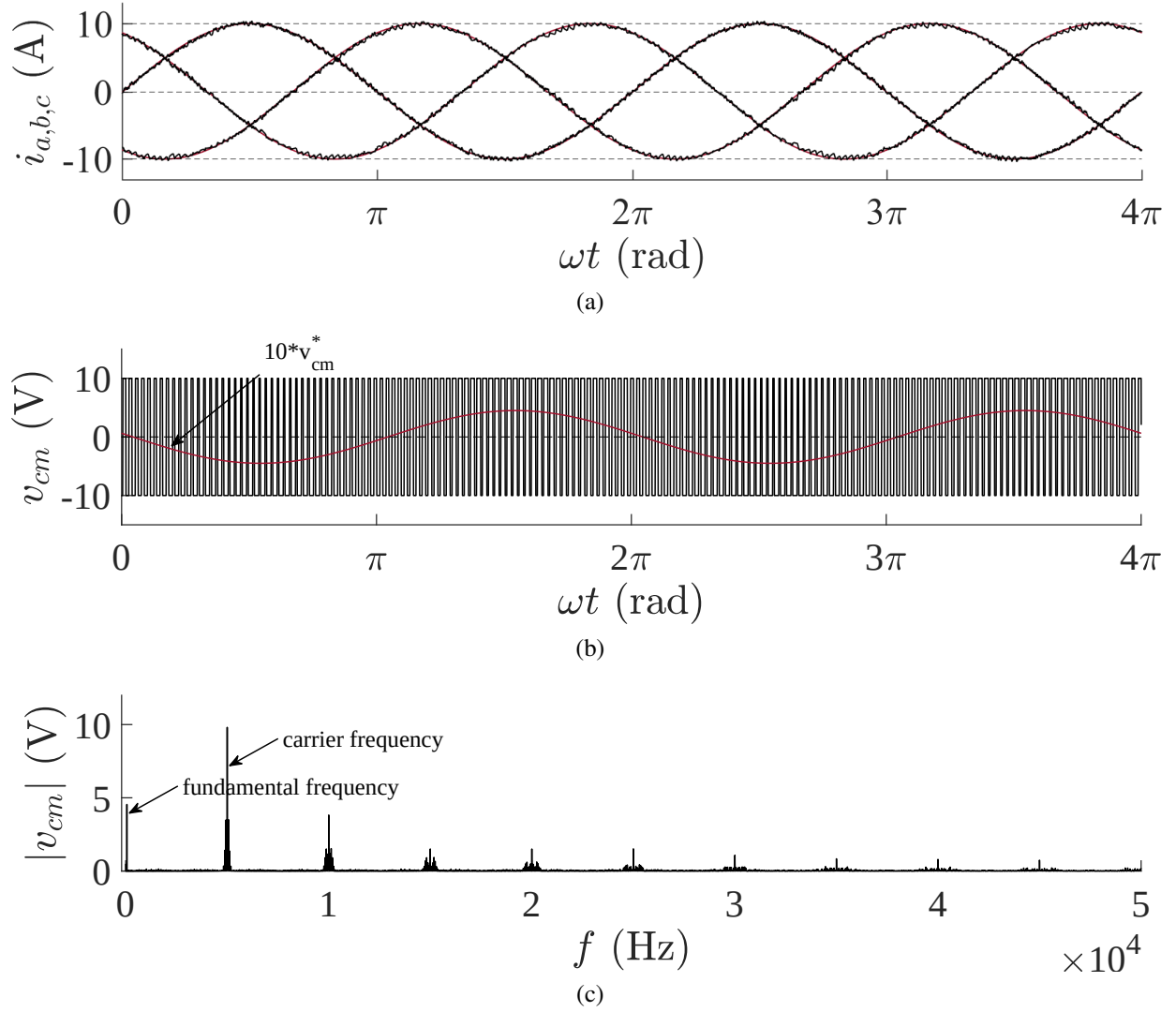


Figure 3.8 Simulation results of MPC-PWM at 60 Hz fundamental frequency. $T_s = 10 \mu s$, CMV reference amplitude = 0.45, CMV carrier frequency = 50 kHz. CMV carrier phase-shift = -8° . Load current THD = 4%.

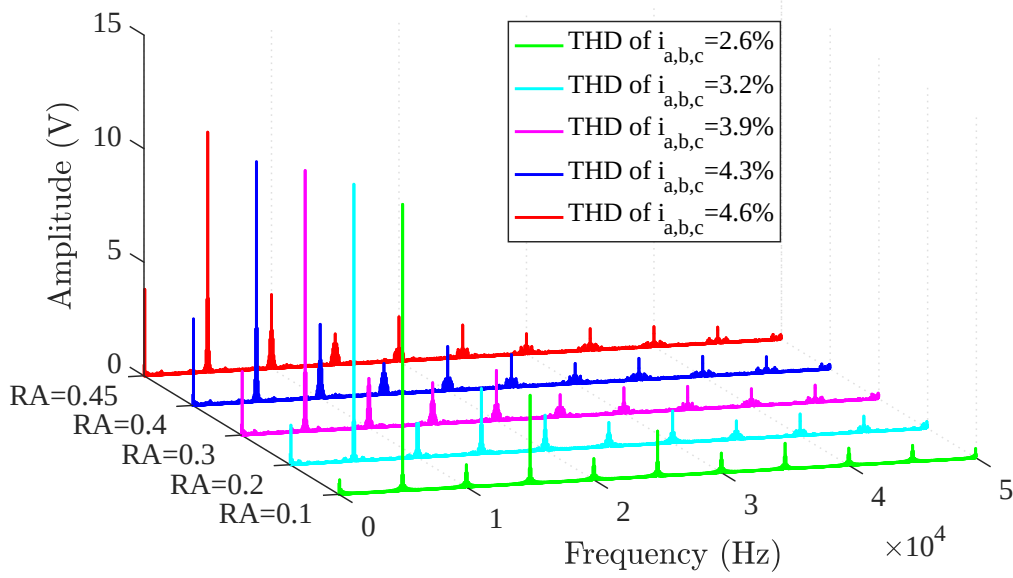


Figure 3.9 The trade-off between the reference amplitude (RA) and the THD of the load current. As the reference amplitude increases the CMV amplitude and the reference frequency increases with some sacrifice on the load current THD. $MI = 1$.

3.3 Bearing Current Reduction

The different bearing currents vary with the motor size and grounding configuration. Therefore, the mitigation technique have to be chosen for different drive specifications. Recent years have seen rising number of electric discharge machining (EDM) type of bearing failure in AC drive system, sometimes, the failure happens few months after start-up [51]. The source of the EDM current is the voltage induced over the bearing v_b which is the potential between the inner and the outer race of the bearing. The bearing voltage mirror the CMV at the motor terminal by a capacitive voltage divider

$$\frac{v_b}{v_{cm}} = \frac{C_{wr}}{C_{wr} + C_{rf} + 2C_b} = BVR \quad (3.12)$$

where C_{wr} is the stator winding-to-frame capacitance, C_{rf} is the rotor-to-frame capacitance, and C_b is the bearing capacitance as shown in Fig. 3.11. BVR is the bearing voltage ratio.

The electrically loaded lubrication film between the balls breaks down when a threshold voltage of $v_{b,th} \approx (5...30)$ V is reached. The exact break down voltage of the lubricant can only be

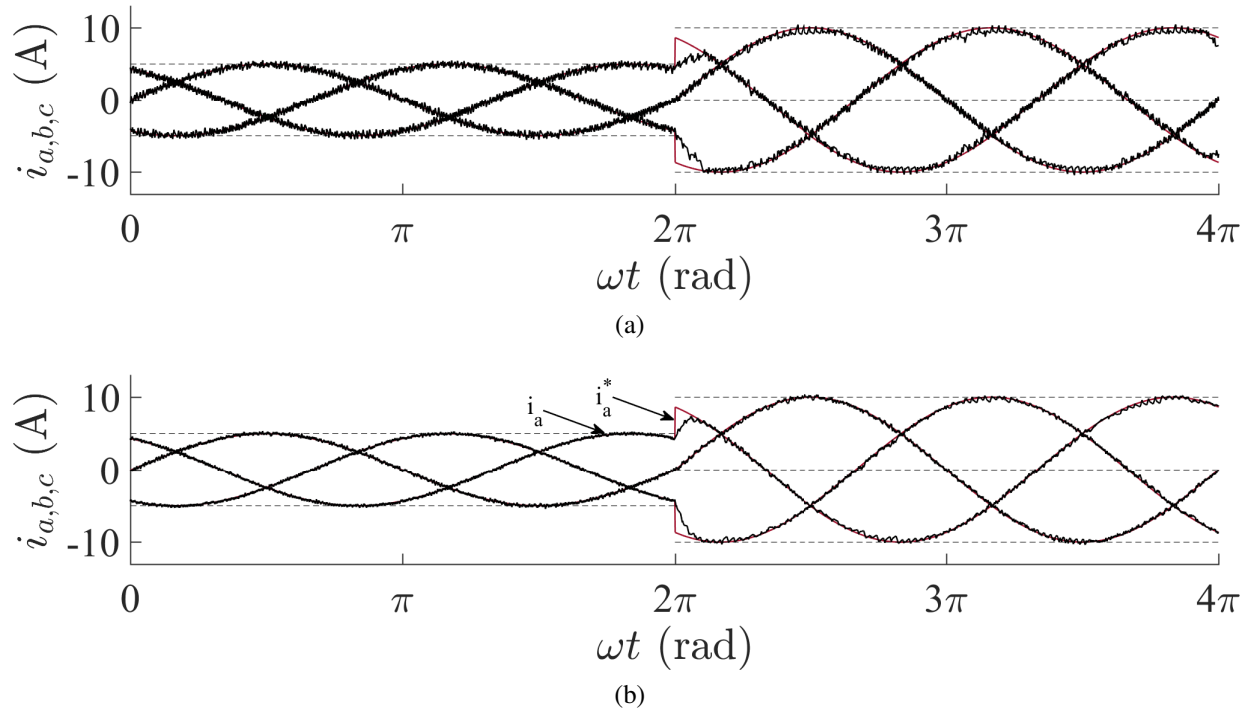


Figure 3.10 The transient behavior of the load current during a step change from 5 A ($MI = 0.45$) to 10 A ($MI = 0.9$) (a) MPC-SC and (b) MPC-PWMC.

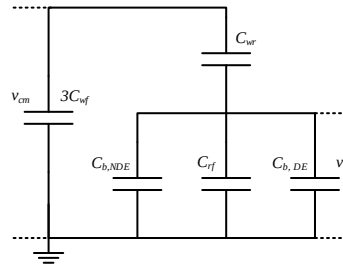


Figure 3.11 Equivalent circuit of the main capacitances of an induction machine or PM machine that are important in high frequencies.

estimated because it changes with the machine speed and the bearing temperature.

All the parasitic capacitances are assumed not to change with the operating conditions. Due to the fast switching, v_b build up repeatedly and discharge at $v_b \approx (5...15)$ V.

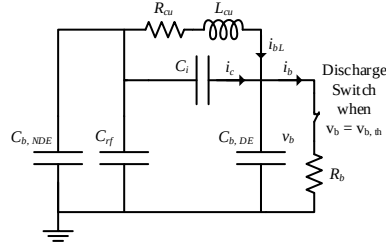


Figure 3.12 Equivalent circuit of EDM current discharge.

The process of calculating the bearing current discharge is well presented in ([62], section 7.4). Although the bearing current can not be measured, the current measured in the copper loop shown in Fig. 3.14 can be utilized indirectly to verify the simulation model. The high frequency machine model shown in Fig. 3.14 is used to calculate the bearing discharge current i_b . EDM bearing current does not occur with each switching instant, but when the lubricant film has been loaded [62]. Here we assume the worst case scenario by assuming that v_b reaches $v_{b,th}$ every CMV switching instant. Reducing the number of EDM discharges occurrence results in smaller average value of bearing current [63]. The average value of the bearing current can be reduced enormously by reducing the frequency of the CMV. Fig. 3.13 shows the bearing current resulting from the conventional MPC methods and the proposed selective voltage set methods. It is evident that because the selective voltage set methods can reduce the CMV frequency below $\frac{1}{2}f_s$, the resulting bearing charge is reduced and hence the number of the electric discharges.

Furthermore, there is an optimal common-mode frequency in which the minimum common-mode current can be achieved for high switching frequency setting. This could be a very attractive feature in high-frequency applications that utilize the wide-band-gap devices. Furthermore, new machine design objectives could be considered to increase the dip effect in the machine impedance so that a low admittance path can be provided to the CM current. One of the main differences between the proposed selective voltage set and the conventional CFR-MPC method is that the

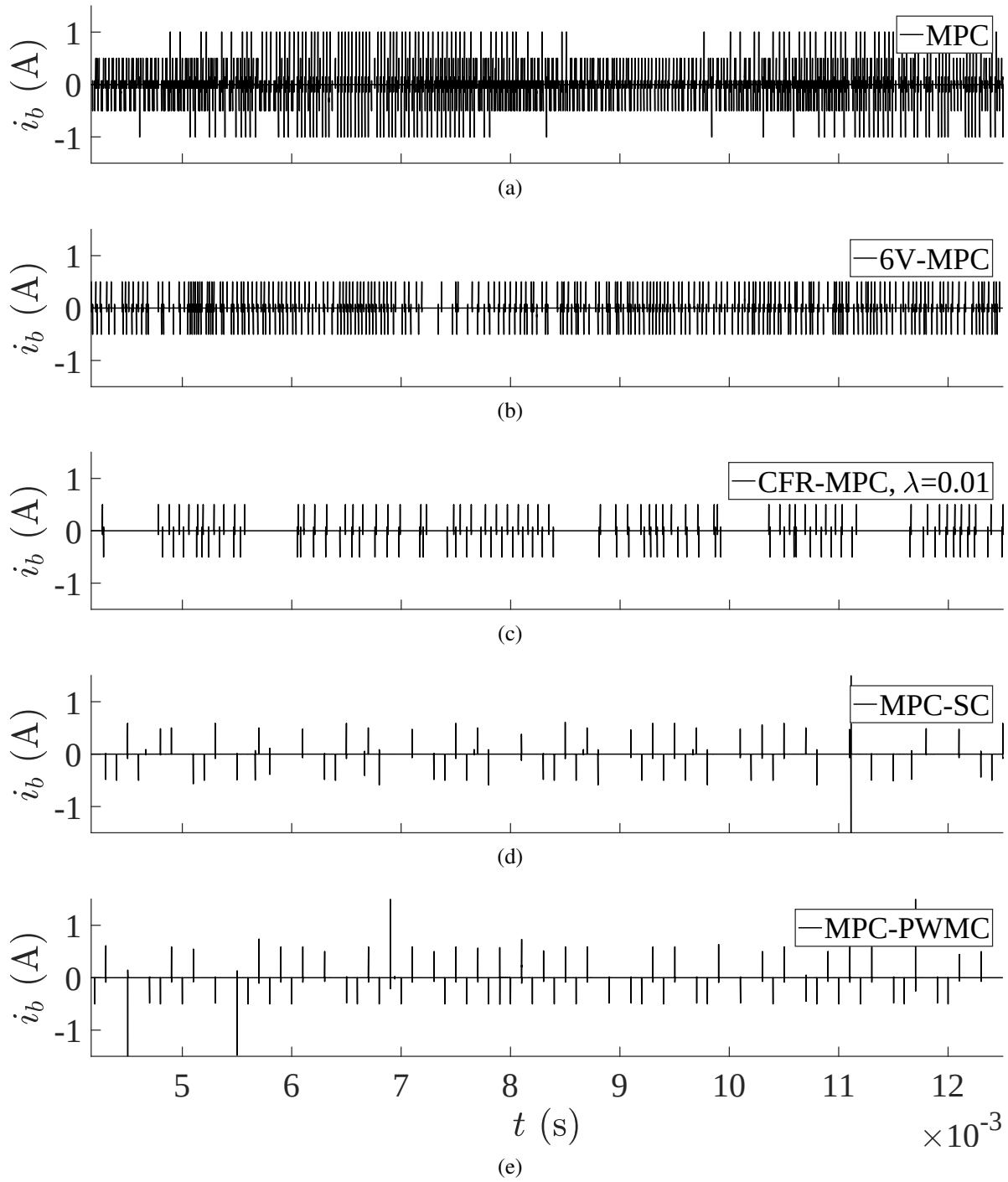


Figure 3.13 Comparison of bearing currents i_b of the conventional MPC methods and the proposed selective voltage set MPC methods. $V_{dc} = 250$ V, $f = 60$ Hz, and $MI = 0.9$.

later method is unable to control the frequency of the CMV. The frequency of the CMV can be only reduced by increasing the weighting factor in the objective function. This result in unpredictable behavior by the converter when the weighting factor increased above the limits. Fig. 3.14 shows that as the weighting factor increases the CMV frequency decreases and the THD of the load current increases. Increasing λ to 0.021 results in inferior current tracking performance. It is essential to calibrate the weighting factor range on the hardware itself. This uncertainty puts stringent limitations on the practical viability of this approach.

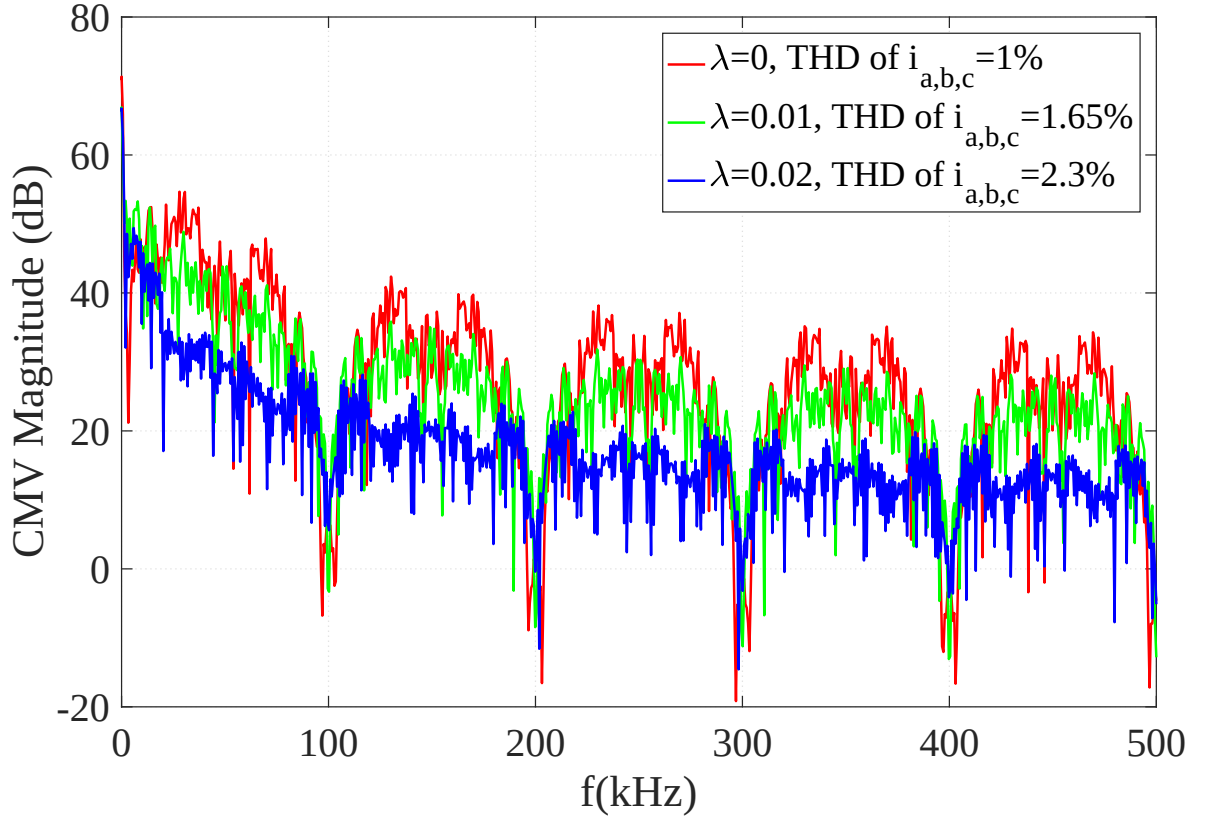


Figure 3.14 Frequency spectrum of CMV and the load current THD with changing the weighting factor λ .

3.4 Experimental Results

The experimental work to validate the simulation results has been carried out using the rated parameters and operating conditions. Fig. 3.15 shows the experimental setup. The system consists of

three inverter legs with each leg being realized with IGBT module CM100DY-24A. The control algorithm is implemented using DSpace CP1103. The CMV is measured as the voltage between the three-phase star connection and the center tap of the DC-link as shown in Fig. 3.1. The parameters used for the experiment are listed in table 3.2. First the experimental results for the conventional

Table 3.2 Experimental test parameters.

Parameter	Value
DC-link voltage	50 and 60 V
Load inductance	1 and 2 mH
Load resistance	2.5 and 5 Ω
Load current reference range	3 and 10 A
Sampling time	10 μ s

MPC method is shown in Fig. 3.16. The amplitude of the CMV is $|V_{dc}|$ with frequency spectrum ranges all across the sampling frequency spectrum. In our case the sampling time is 10 μ s, therefore, the frequency spectrum of the CMV is between (0, 50) kHz. The cost function redesign is presented in Fig. 3.17. The added weight ($\lambda=0.01$) in the cost function reduces the use of the zero vector, therefore, the amplitude of the CMV is lower than the one from the conventional MPC method. Fig. 3.18 shows the experimental results when both zero vectors are not used. In this case the amplitude of the CMV is reduced to $|\frac{V_{dc}}{3}|$. However, the frequency of the CMV still within the entire range of half the sampling frequency. None of the previously proposed methods can control the frequency of the CMV to reduce the number of current discharges in the bearing. The normal range of the DC-link voltage is large enough to accumulate charge across the bearing races. Therefore, it is not possible to reduce or limit the number of current discharges in the bearing using the previous methods.

On the other hand, the experimental results of sequenced commutation method when the fundamental frequency is 60 Hz are shown in Fig. 3.19(a) and (b), where the period of the CMV is set to 0.0033 s. The characteristic of the CMV is completely decoupled from the other operating conditions. The spectrum of the CMV shows that the CMV is concentrated at the chosen commutation frequency 3.3 kHz.

The experimental results of pulse width modulation commutation method when the fundamental frequency is 60 Hz are shown in Fig. 3.20(a) and (b), where reference waveform is 0.2, frequency 2 Hz, and the carrier frequency is 5 kHz. The characteristic of the CMV is completely decoupled from the other operating conditions. The spectrum of the CMV shows that the CMV is concentrated at the chosen carrier frequency 5 kHz.

The MPC-PWMC is more capable than the MPC-SC method in concentrating the frequency of the CMV at the carrier frequency. The simulations and experimental results show that MPC-SC and MPC-PWMC method produce similar current tracking performance. The THD of the load current can be further reduced when the commutation frequency is increased. The choice of which control method is better in implementation is solely dependent on the characteristic of the impedance of the machine. Generally, reducing the CMV frequency as minimum as it possible without sacrificing much of the load current quality is the goal. In a very high switching frequency applications the resonance dip in the frequency response of the machine impedance can be utilized as a filtering factor. The proposed method is the only method that allows to arbitrarily select the frequency of the common-mode voltage at any region below half the sampling frequency.

The implementation of only odd or only even vectors requires simultaneous switching of two converter legs. In practice, this could be challenging because of the dead-times and the differences in the gate delay [60]. The dead-time mismatch causes a narrow pulse in the CMV. The narrow pulse frequency increases as the switching frequency increases. During the dead-times, the resulting CMV is no longer a function of the switching commands. Instead, it is strictly dependent on the signs of the load currents. The interested reader may check [60] for examples and solutions for the dead-time problem when using only odd and only even. In this study the sampling time is set to $10\text{ }\mu\text{s}$, therefore, by observation, the switching frequency of the converter is approximately 15kHz. By increasing the dead time from $0.5\text{ }\mu\text{s}$ to $1\text{ }\mu\text{s}$ The effect of deadtime can be more evident as shown in Fig. 3.21 (a) and (b). The high peaks (V_{dc} and $-V_{dc}$) are occurring because at some deadtime intervals the zero vectors are activated.

The implementation of only odd or only even vectors requires simultaneous switching of two

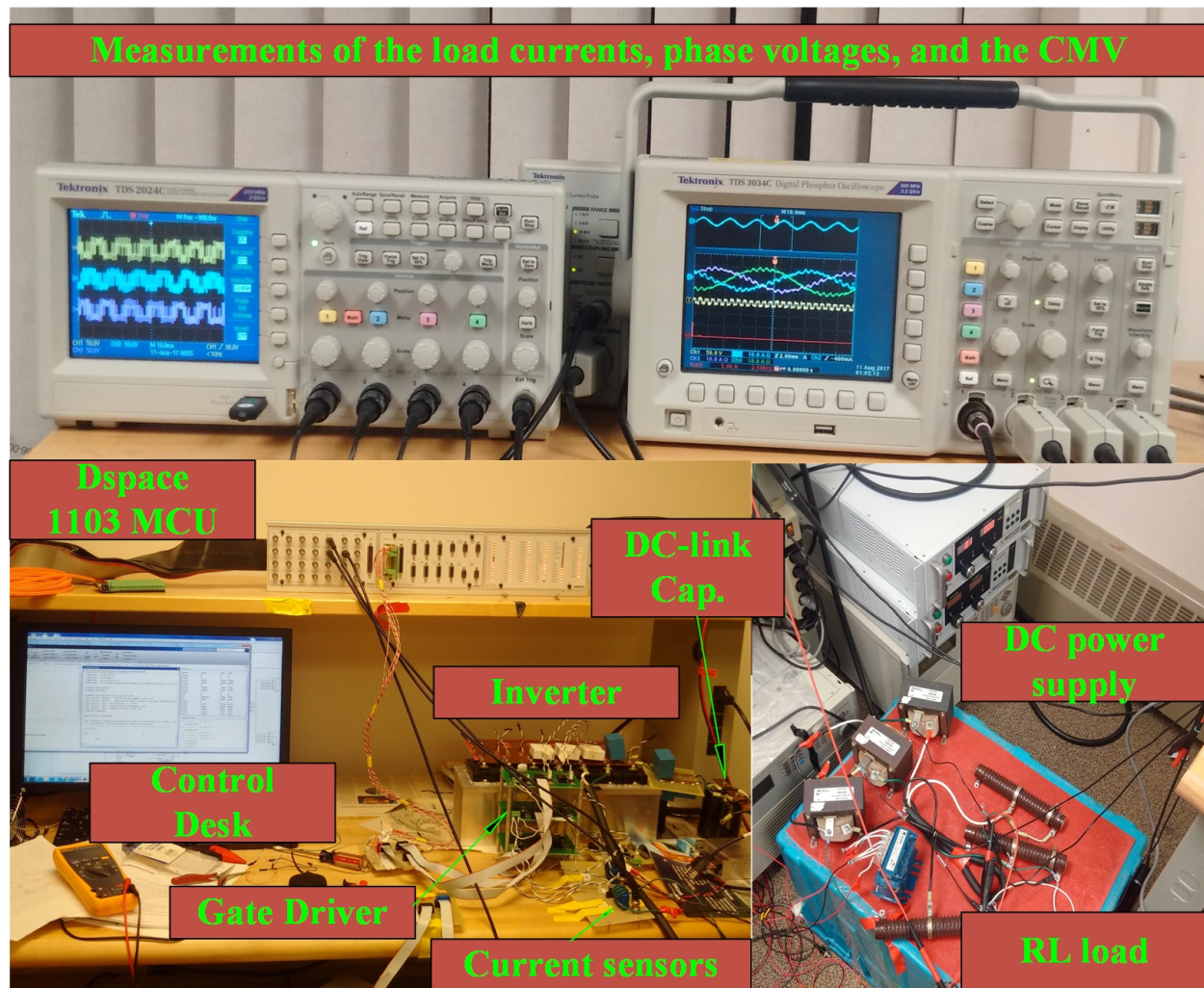


Figure 3.15 The experimental setup.

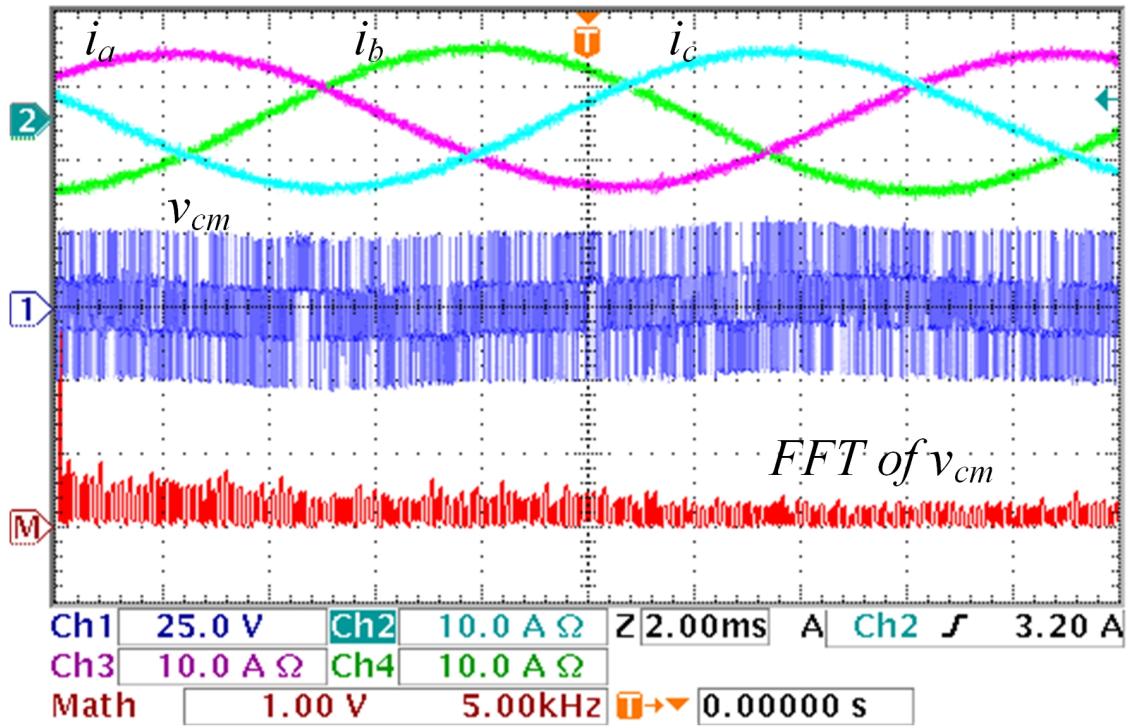


Figure 3.16 Experimental results of MPC method load current $i_{a,b,c}$, CMV v_{cm} , and FFT of CMV.

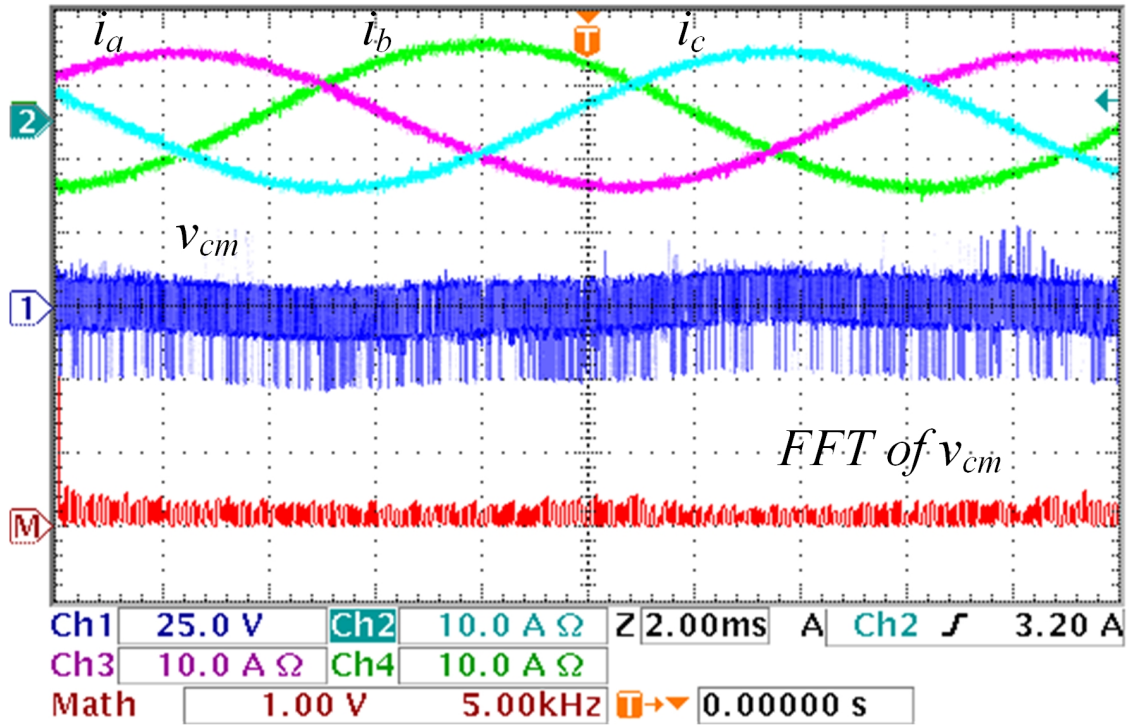


Figure 3.17 Experimental results of CFR-MPC method load current $i_{a,b,c}$, CMV v_{cm} , and FFT of CMV.

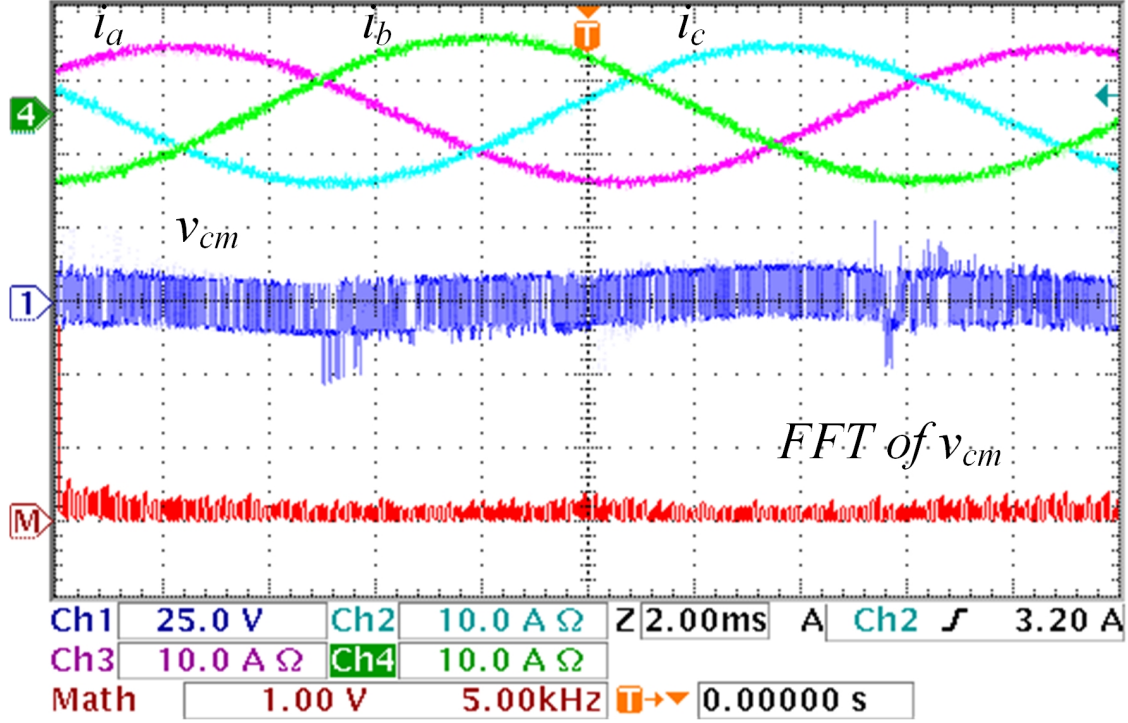
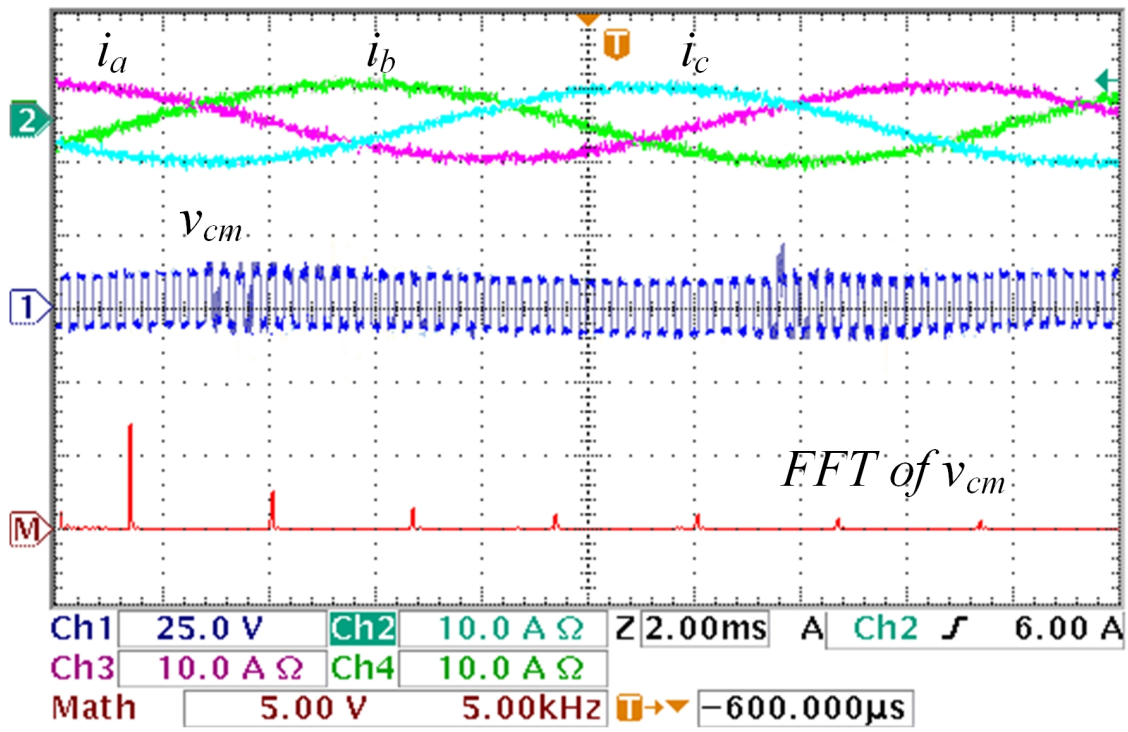
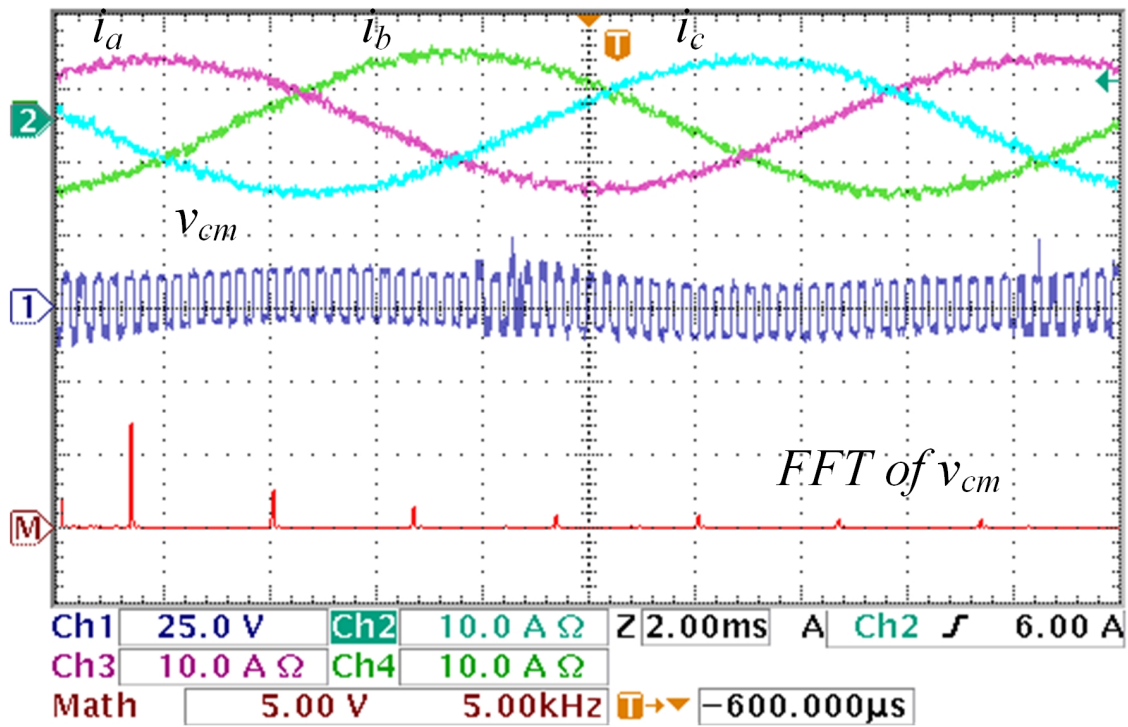


Figure 3.18 Experimental results of 6V-MPC method load current $i_{a,b,c}$, CMV v_{cm} , and FFT of CMV.

converter legs. In practice, this could be challenging because of the dead-times and the differences in the gate delay [60]. The dead-time mismatch causes a narrow pulse in the CMV. The narrow pulse frequency increases as the switching frequency increases. For instance, consider Fig. 2.8, during the dead-times, the resulting CMV is no longer a function of the switching commands. Instead, it is strictly dependent on the signs of the load currents. The interested reader may check [60] for examples and solutions for the dead-time problem when using only odd and only even. In this study the sampling time is set to $10\mu s$, therefore, by observation, the switching frequency of the converter is approximately 15kHz. The dead-time is reduced to less than 0.5μ to reduce the effect of short pulsed in the CMV.

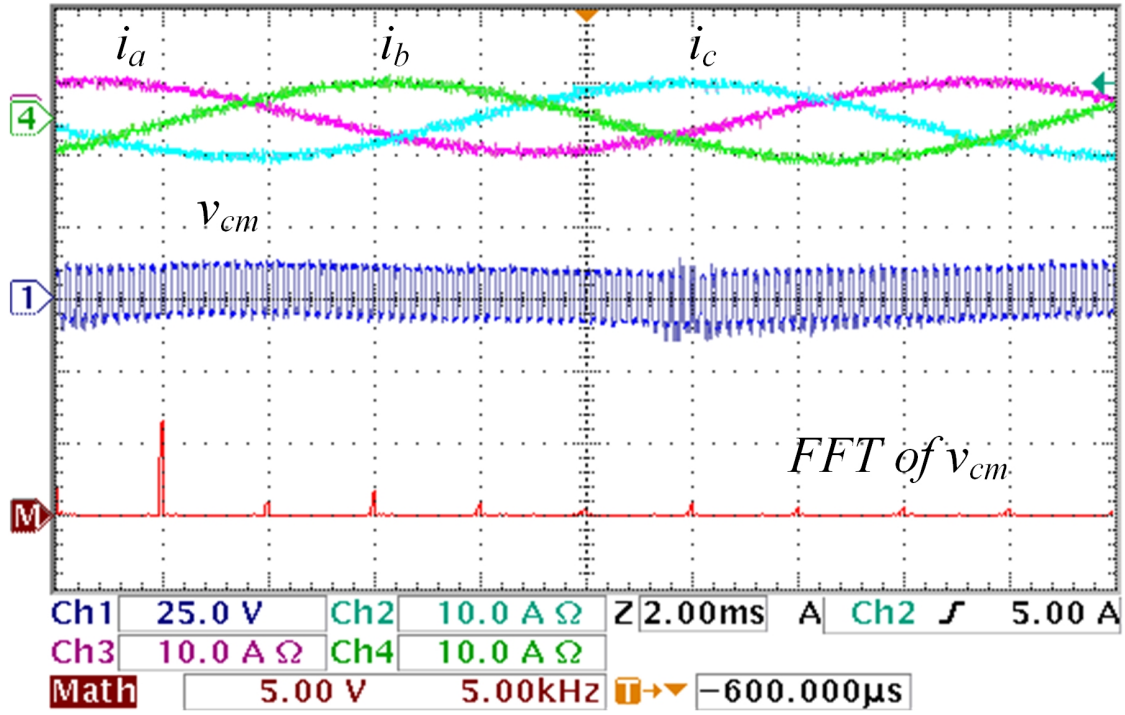


(a) $MI = 0.5$, $THD = 4.8\%$

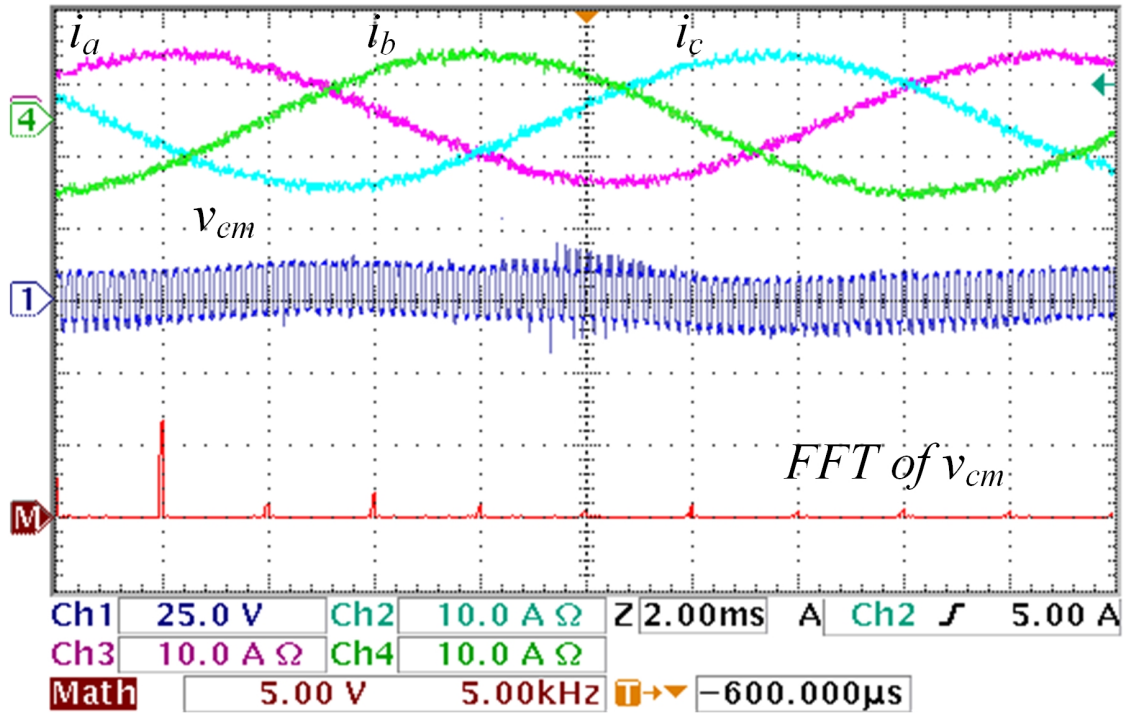


(b) $MI = 0.9$, $THD = 4\%$

Figure 3.19 Experimental results for the proposed MPC-SC method load current $i_{a,b,c}$, CMV v_{cm} , and FFT of CMV.

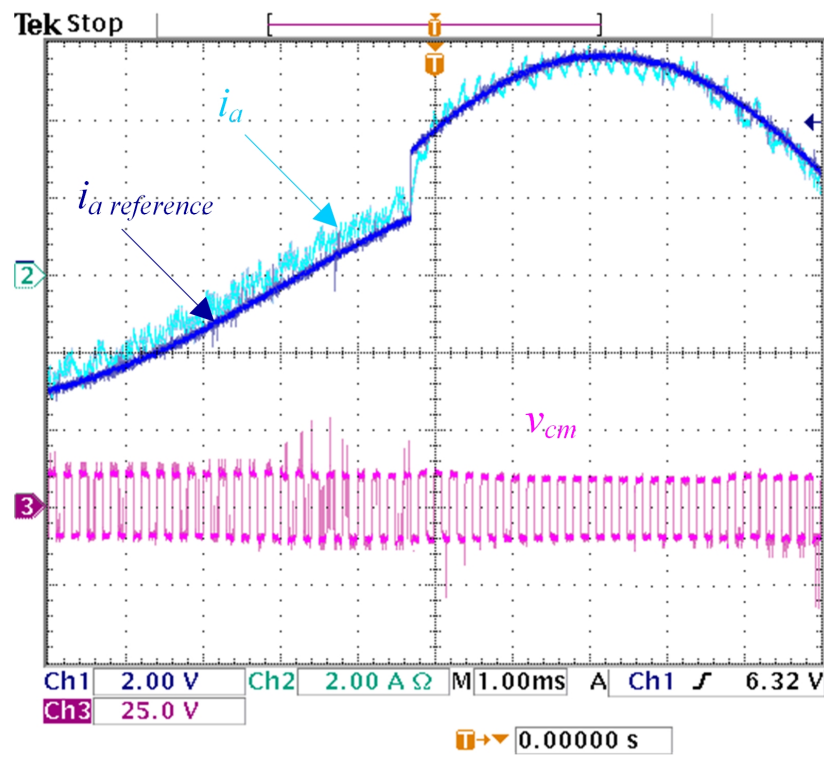


(a) $MI = 0.5$, $THD = 4.8\%$

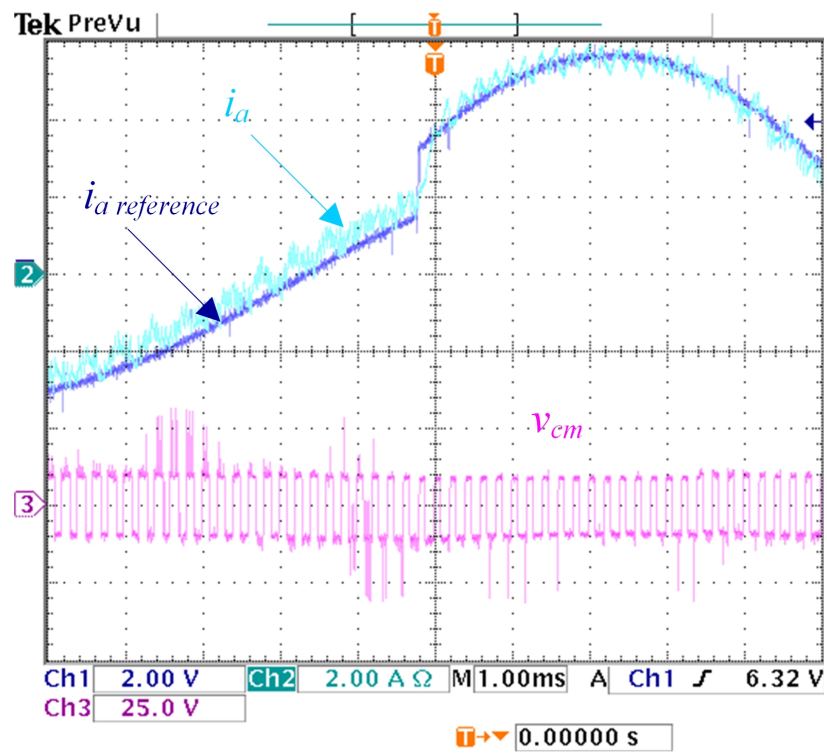


(b) $MI = 0.9$, $THD = 3.8\%$

Figure 3.20 Experimental results for the proposed MPC-PWMC method load current $i_{a,b,c}$, CMV v_{cm} , and FFT of CMV.



(a)



(b)

Figure 3.21 Load Current transient behaviour during a step change from 3 A to 6 A.

Chapter 4

Generalized Chudnovsky Algorithm for Real-time PWM Selective Harmonic Elimination/Modulation: Two-Level VSI Example

4.1 Introduction

The selective harmonic elimination (SHE) technique effectively reduces the low-order harmonic content of inverter output waveform and generates a high-quality spectrum through the elimination of specific low-order harmonics [64] [65]. Therefore, it has been applied in power electronic controllers extensively, and many related techniques have been proposed in recent years [66]- [70].

The traditional implementation of SHE is to use a lookup table and a modulator driven by a very slow control loop to ensure steady-state stability [71]. Offline SHE implementations share the crucial drawback: the switching angles could not be calculated in real-time and one has to rely on loading the optimal switching angles for each specific modulation index (M_i). During the transient state of a low switching-frequency drive, the low-frequency component of the reference

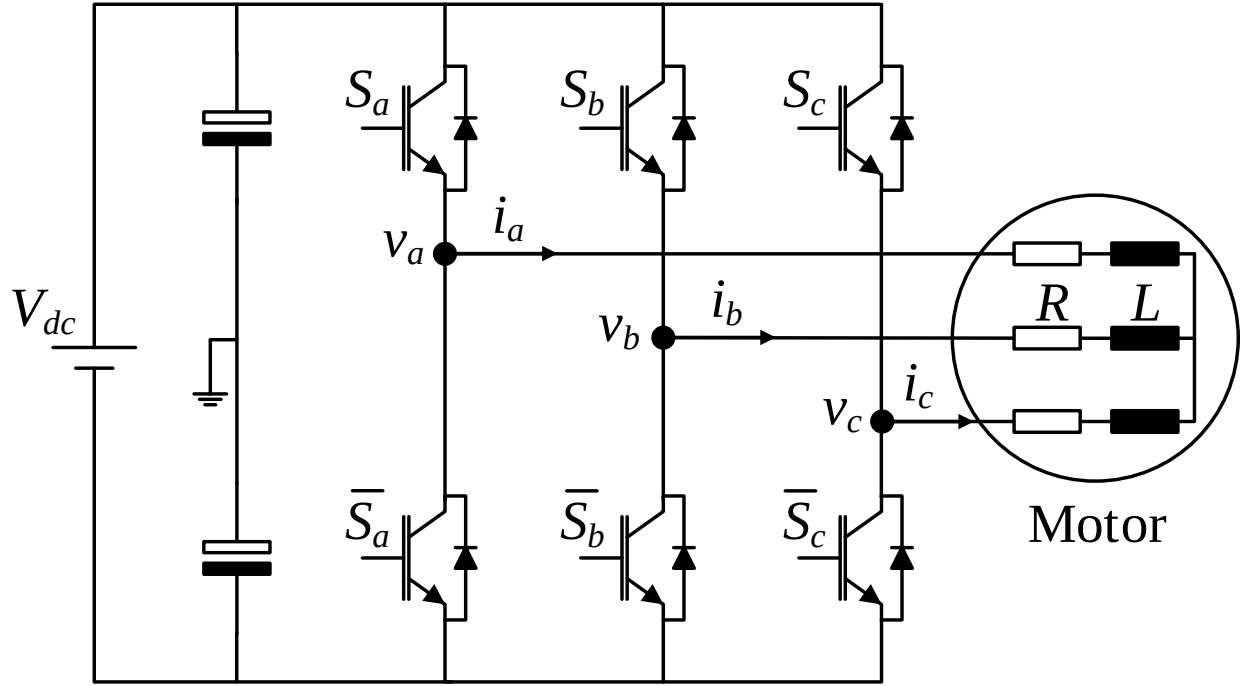


Figure 4.1 Two-level voltage source inverter drive.

voltage becomes nonsinusoidal [72]. The switching sequence will then be implemented with the optimal angles saved in the lookup table, which is only valid for steady-state conditions. The resulting current dynamic will be far from optimal. Furthermore, there are other sub-transient conditions such as changing the number of switching events per cycle and changing M_i , which will result in the sub-optimal current performance.

It is important to make the distinction between different types of real-time or online solutions of SHE. Some online SHE algorithms solve the optimization problem in the controller using an iterative process with guessed initial values. Although these methods reduce the memory requirement, they suffer from a poor dynamic performance that is typically inferior to the dynamic performance of the look-up table implementations. For instance, the supposedly real-time method in [73] is unable to perform rapid changes in M_i . It would take 58 ms to change M_i from 0.96 to 0.64. Furthermore, the presented implementation results in larger total harmonic distortion (THD) than the offline solution. Other methods also claim the real-time feature while the solution requires an initial guess and an indeterminate number of iterations [74]. In [75], the switching angles are

approximated using curve fitting of the offline solution. Then a carrier waveform is calculated by a cosine function based on the modulation depth. This approach requires saving the curve fitting coefficients for each modulation index. If 1% resolution is desired, it would require 100 polynomials to describe each switching angle. Not to mention that if the switching frequency is changed, a new set of equations is required for each angle. In [76], Chebyshev polynomials are used to convert a set of the transcendental equations into algebraic polynomials. Then the algebraic equations are rearranged through a change of variables to solve for the switching angles. However, the transformation of the transcendental equations is not systematic, and no generalization was given to simplify the process of transforming the transcendental equations to algebraic equations. The complexity of the derivation increases as the number of the selected harmonics increases. Furthermore, the set of the algebraic equations is solved using inverse cosine function, but the computational effort could be reduced by converting the set of the algebraic equations to a single polynomial. All these drawbacks with the strict operating requirements of high power industrial drives pose serious limitations on the practical viability of the existing approaches.

A new implementation of the real-time selective harmonic elimination (RTSHE) is proposed in this paper. The original contributions of the proposed RTSHE are the following:

- 1· Presenting the generalized Chudnovsky algorithm. The new algorithm allows modulating the selected harmonics rather than only eliminating them.
- 2· Presenting a new method of obtaining the values of the optimal switching angles from the polynomial in real-time without resorting to any iterations or guesses.

Preliminary results were published in [64] show that the real-time approach could be a suitable replacement for the conventional offline method. In this article, the authors expand the real-time algorithm to a generalized form without increasing the computational effort. The algorithm is demonstrated through the experiment of the two-level voltage source inverter (VSI) shown in Fig. 4.1. A comparison between the proposed RTSHE method and the conventional offline method is presented throughout the paper.

The rest of the paper is organized as follows: The proposed RTSHE method is presented in section II. The comparison between the proposed RTSHE and the conventional offline method is presented in section III. The selective harmonic modulation (RTSHM) method is presented in section IV. The experimental results are presented in section V. Finally, the conclusion is presented in section VI.

4.2 The Proposed Real-Time Selective Harmonic Elimination

The development of RTSHE starts from manipulating the transcendental equations. Owing to the symmetry of the PWM waveform, only odd harmonics exist. By chopping the PWM waveform n times per quarter cycle, the Fourier coefficients of the odd harmonics are given by

$$b_k = -\frac{4V_{dc}}{k\pi} \left[1 - 2 \sum_{i=1}^n (-1)^{i-1} \cos(k\alpha_i) \right], \quad (4.1)$$

where k is the harmonic order number $\{1, 3, 5, \dots\}$, n is the total number of the switching angles per quarter fundamental cycle, V_{dc} is the DC-link voltage, and α_i is the optimal switching angle. In SHE, the fundamental component ($k = 1$) is set to a desired amplitude, and the other selected odd harmonics are set to zero. This formulation of the optimization problem leads to the following set of transcendental equations:

$$\begin{aligned} 1 - 2 \cos(\alpha_1) + \dots + (-1)^n 2 \cos(\alpha_n) &= -\frac{\pi b_1}{4V_{dc}} \\ 1 - 2 \cos(3\alpha_1) + \dots + (-1)^n 2 \cos(3\alpha_n) &= -\frac{3\pi b_3}{4V_{dc}} \\ &\vdots \\ &\vdots \\ 1 - 2 \cos(k\alpha_1) + \dots + (-1)^n 2 \cos(k\alpha_n) &= -\frac{k\pi b_k}{4V_{dc}}. \end{aligned} \quad (4.2)$$

4.2.1 Converting the Transcendental Equations to Algebraic Equations

By using Chebyshev polynomials, the transcendental equations in (4.2) can be transformed to algebraic equations [77]- [78]. This can be achieved by letting $x_o = \cos(\alpha_o)$ and $x_e = -\cos(\alpha_e)$, where the subscripts o and e denote the odd and even numbers, respectively. This leads to the following set of algebraic polynomials:

$$\begin{aligned} x_1 + x_2 + \dots + x_n &= s_1 \\ x_1^3 + x_2^3 + \dots + x_n^3 &= s_3 \\ &\cdot \\ &\cdot \\ x_1^{2n-1} + x_2^{2n-1} + \dots + x_n^{2n-1} &= s_{2n-1}, \end{aligned} \quad (4.3)$$

where $x_1, x_2, \dots, x_n$, hold the solution of the switching angles α_1, α_2 , and α_n , respectively. $s_1, s_3, \dots, s_{2n-1}$ can be obtained using the proposed recursive algorithm:

$$T_{2n-1}(x)|_{(x^{2n-1}=s_{2n-1})} = \frac{1}{2} + \frac{\pi b_{2n-1}}{8V_{dc}}, \quad (4.4)$$

where $T_{2n-1}(x)$ is a Chebyshev polynomial of the first kind [80]. This can be found through the recursive formula

$$T_{n+1}(x) = 2xT_n(x) - T_{n-1}(x), \quad (4.5)$$

where $T_0(x) = 1$ and $T_1(x) = x$. For instance, if the desired fundamental component is set to a specific value b_1 and the rest of the odd harmonics are set to zero, the following values for s can be obtained:

$$\begin{aligned}
s_1 &= \frac{1}{2} \left[1 + \frac{\pi b_1}{4V_{dc}} \right] \\
s_3 &= \frac{1}{2} \left[1 + \frac{3}{4} \frac{\pi b_1}{4V_{dc}} \right] \\
&\cdot \\
&\cdot \\
s_{2n-1} &= \frac{1}{2} \left[1 + \frac{\pi b_1}{4^{n-1} 4V_{dc}} \binom{2n-1}{n-1} \right].
\end{aligned} \tag{4.6}$$

In the case of a three-level VSI such as the neutral point clamped (NPC) inverter or the single phase inverter [79], the following equation can be used to calculate s :

$$s_{2n-1} = \frac{\pi b_1}{4^{n-1} 4V_{dc}} \binom{2n-1}{n-1}. \tag{4.7}$$

The generalized formulas (4.6) and (4.7) circumvent the offline recursive derivation effort. The remarkable fact is that the definition of s becomes explicit, rather than recursive. One can now start the optimization problem from writing down the algebraic polynomials (4.3) directly, without going through the earlier steps.

4.2.2 Converting the Algebraic Equations to a Single Polynomial

The set of algebraic polynomials in (2) is a symmetric sum of powers. Therefore, it can be further reduced to the following form of the single polynomial using Newton's identities:

$$P(x) = p_0 x^n + p_1 x^{n-1} + \dots + p_n = 0, \tag{4.8}$$

where $p_0 = 1$, and p_1 to p_n can be obtained using the generalized version of Newton's identity first presented in [79]. If the series expansion for the desired polynomial is

$$P(x) = \prod_{i=1}^n (x - x_i), \quad (4.9)$$

then by algebraically manipulating the polynomial terms we get

$$P(x) = x^n \exp\left(-\sum_{m=1}^{\infty} \frac{s_m}{mx^m}\right), \quad (4.10)$$

where s_m is the power series representation of the polynomials in (4.3). As in [79], one can eliminate the multiplication x^n term by dividing (4.10) by $P(-x)$. This leads to the following expression:

$$P(x) = (-1)^n P(-x) G(1/x), \quad (4.11)$$

where

$$G(1/x) = \exp\left(V(1/x)\right) = \exp\left(-2 \sum_{m=1,3,5,\dots}^{\infty} \frac{s_m}{mx^m}\right). \quad (4.12)$$

It is possible to analytically express $G(1/x)$ using the generating function approximation:

$$G(x) = g_0 + g_1 x + g_2 x^2 + \dots = \sum_{n \geq 0} g_n x^n. \quad (4.13)$$

Generating functions are a single quantity that represents the whole sequence. They were introduced by De Moivre to solve a class of general recurrence problems [81]. We can recover the individual value of $g_1, g_2, \dots$ from $G(x)$ by assuming that the infinite sum (4.13) exists for some value of x . The exponential term $e^{V(1/x)}$ in (4.12) can also be represented by the following generating function:

$$V(x) = v_0 + v_1 x + v_2 x^2 + \dots = \sum_{n \geq 0} v_n x^n. \quad (4.14)$$

After calculating the values of (4.13) and (4.14), each x in the equation will be replaced by its reciprocal to match (4.12). The coefficients of $G(x)$ can be obtained by using the binomial theorem. However, Euler discovered an efficient method to obtain the power series powers [82]. Consider the following equation:

$$G(x) = e^{V(x)}. \quad (4.15)$$

By taking the derivative for both sides

$$\frac{dG(x)}{dx} = \frac{dV(x)}{dx} G(x), \quad (4.16)$$

expanding both sides

$$g_1 + 2g_2x + 3g_3x^2 + \dots = (v_1 + 2v_2x + 3v_3x^2 + \dots)(g_0 + g_1x + g_2x^2 + \dots), \quad (4.17)$$

rearranging the RHS

$$g_1 + 2g_2x + 3g_3x^2 + \dots = (v_1g_0) + (2v_2g_0 + v_1g_1)x + (3v_3g_0 + 2v_2g_1 + v_1g_2)x^2 + \dots, \quad (4.18)$$

and by equating the coefficients of the LHS with the RHS, we find that

$$g_n = \sum_{k=1}^n \frac{k}{n} v_k g_{n-k}, \quad (4.19)$$

where $g_0 = e^{v_0} = 1$. This leads to a simple real-time algorithm by which we can successively determine the coefficients of $G(x)$. To avoid the forbidden abstract way of presenting results, the authors provide the following non-trivial example.

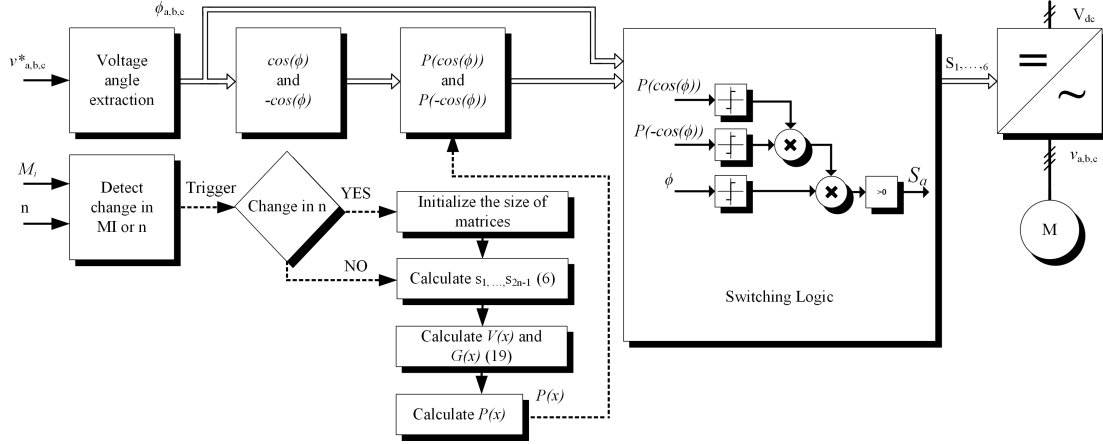


Figure 4.2 Illustration of obtaining the value of the optimal switching angles by solving the polynomial in real-time.

Example

Suppose that for a three-phase voltage source inverter, we are required to eliminate the first three odd harmonics 3rd, 5th, and 7th, and set the modulation index to $0.6283 = \frac{\pi b_1}{4V_{dc}}$. The DC-link voltage is 100V.

The first step is to calculate the value of s for each polynomial in (4.3) using the proposed generalized formula (4.6) as follows:

$$s_1 = \frac{1}{2} \left[1 + \frac{0.6283}{4^0} \binom{1}{0} \right] = 0.8141.$$

By plugging in (4.6) $n = 2$, $n = 3$, and $n = 4$, we can find that $s_3 = 0.7356$, $s_5 = 0.6963$, and $s_7 = 0.6718$, respectively. Now the symmetric power sum (4.3) can be written as

$$\begin{aligned} x_1 + x_2 + x_3 + x_4 &= 0.8141 \\ x_1^3 + x_2^3 + x_3^3 + x_4^3 &= 0.7356 \\ x_1^5 + x_2^5 + x_3^5 + x_4^5 &= 0.6963 \\ x_1^7 + x_2^7 + x_3^7 + x_4^7 &= 0.6718. \end{aligned} \tag{4.20}$$

The next step is to reduce the system of equation in (4.20) to a single polynomial of order 4 such that the roots of the polynomial are the values of x_1, x_2, x_3 , and x_4 in (4.20). Using the expression in (4.12) for $V(1/x)$, we can calculate the coefficients of the $V(x)$ series as follows:

$$V(1/x) = -2 \sum_{m=1,3,5,\dots}^{\infty} \frac{s_m}{mx^m}$$

$$\Rightarrow V(x) = -2 \sum_{m=1,3,5,\dots}^{\infty} \frac{s_m}{m} x^m,$$

where the term $-2 \frac{s_m}{m}$ is equal to the coefficient $v_{\frac{m+1}{2}}$ in the generating function (4.14). $s_2, s_4, \dots$ are set to zero, $v_0=0$. The calculations lead to the following vector:

$$v = [v_0, v_1, v_2, v_3, v_7, v_5, v_6, v_7, v_8]^T =$$

$$[0, -1.6283, 0, -0.4904, 0 - 0.2785, 0, -0.1919, 0]^T.$$

After obtaining $V(x)$, $e^{V(x)}$ can be calculated using (4.19), where $g_0 = e^{V(0)} = 1$,

$$g_1 = \sum_{k=1}^1 \frac{k}{1} v_k g_{1-k} = v_1 g_0 = v_1 = -1.6283,$$

$$g_2 = \sum_{k=1}^2 \frac{k}{2} v_k g_{2-k} =$$

$$\frac{1}{2} v_1 g_1 + \frac{2}{2} v_2 g_0 = \frac{1}{2} (-1.6283) * (-1.6283) + 0 = 1.3257.$$

By calculating all of the coefficients, one can obtain the following vector:

$$g = [g_0, g_1, g_2, g_3, g_7, g_5, g_6, g_7, g_8]^T =$$

$$[1, -1.6283, 1.3257, -1.2099, 1.0914,$$

$$-1.0240, 0.9525, -0.9067, 0.8570]^T.$$

Now we have all the elements to evaluate the single polynomial by expanding (4.11) and negating the coefficient of the same power from both sides. Note that $p_0 = 1$

$$P(x) = (-1)^n P(-x)G(1/x)$$

$$p_0x^4 + p_1x^3 + p_2x^2 + p_3x + p_4 =$$

$$(p_0x^4 - p_1x^3 + p_2x^2 - p_3x - p_4)(1 + g_1/x + g_2/x^2 + \dots + g_8/x^8).$$

This leads to the following trapezoidal system:

$$\begin{bmatrix} p_1 \\ p_2 \\ p_3 \\ p_4 \end{bmatrix} = \begin{bmatrix} g_4 & -g_3 & g_2 & -g_1 \\ g_5 & -g_4 & g_3 & -g_2 \\ g_6 & -g_5 & g_4 & -g_3 \\ g_7 & -g_6 & g_5 & -g_4 \end{bmatrix}^{-1} \begin{bmatrix} g_5 \\ g_6 \\ g_7 \\ g_8 \end{bmatrix} = \begin{bmatrix} -0.8142 \\ -0.6135 \\ 0.4342 \\ 0.0192 \end{bmatrix}.$$

The polynomial is

$$P(x) = x^4 - 0.8142x^3 - 0.6135x^2 + 0.4342x + 0.0192. \quad (4.21)$$

The same example can be solved using the script shown in Fig. 4.3.

Now we know how to calculate the polynomial, a novel technique of determining the switching angles from the single polynomial in real-time will be presented in the next section.

```

1      % computing s for four switching
2      % angles per quarter fundamental cycle
3      MI=0.6283; % Modulation Index
4      s1=(1+MI)/2; % s1
5      s2=(3*MI+4)/8; % s2
6      s3=(5*MI+8)/16; % s3
7      s4=(35*MI+64)/128; % s4
8      s=[s1; 0; s2; 0; s3; 0; s4; 0];
9      % computing v
10     n=4;
11     v=zeros(2*n+1,1);
12     v(1)=0;
13     for ii=1:n
14         x=(-2)*s(2*ii-1)/((2*ii)-1);
15         v(2*ii)=x;
16     end
17     g=zeros(2* n+1,1);
18     g(1)=1;
19     for ii=1:8
20         g_intial=zeros(2*n+1,1);
21         for k=1:ii
22             x=k*v(k+1)*g(ii+1-k);
23             g_intial(k+1)=x;
24         end
25         %g_intial
26         g(ii+1)=1/ii*sum(g_intial);
27     end
28     % Solving the Toeplitz system
29     gg=[g(5) -g(4) g(3) -g(2);...
30         g(6) -g(5) g(4) -g(3);...
31         g(7) -g(6) g(5) -g(4);...
32         g(8) -g(7) g(6) -g(5)];
33     r=[g(6) g(7) g(8) g(9)]';
34     p=inv(gg)*r % the polynomial coefficients

```

Figure 4.3 Matlab script solving the example.

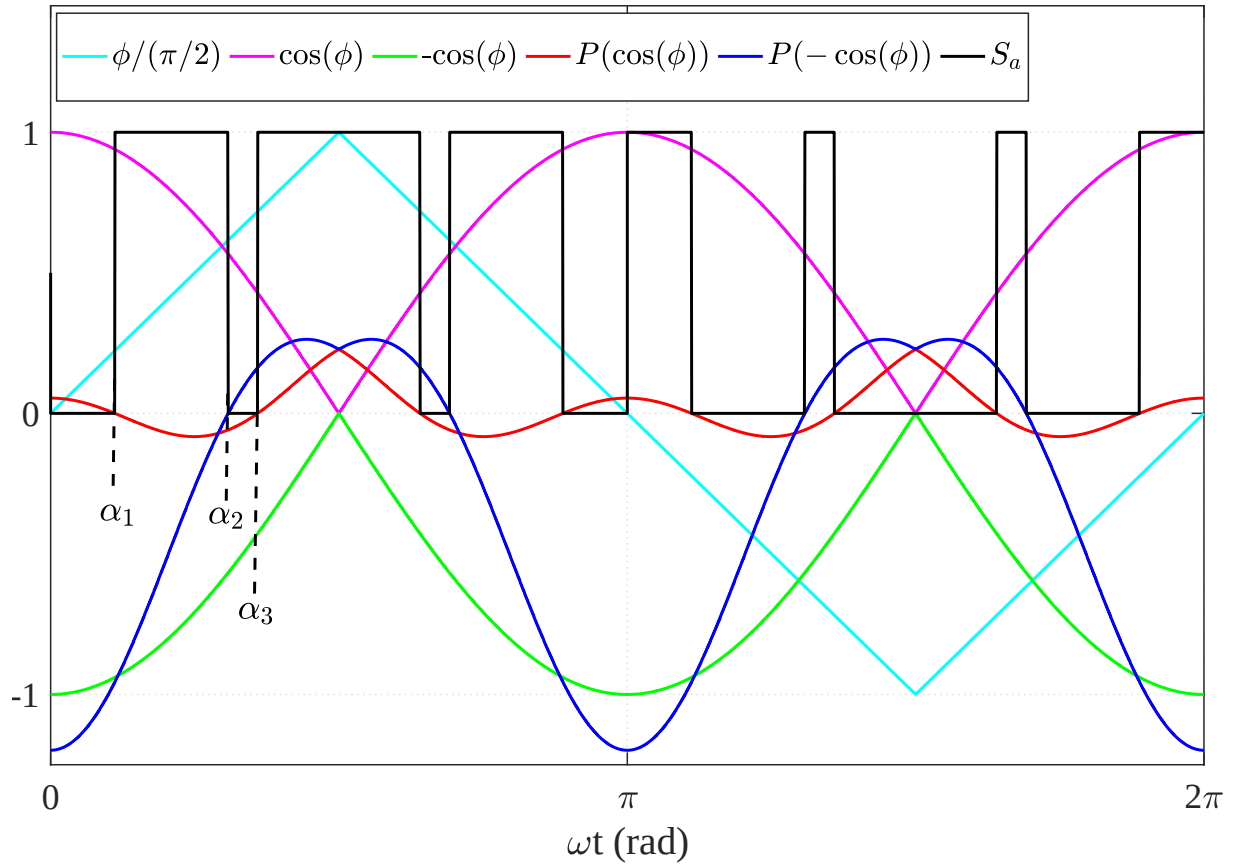


Figure 4.4 The zero crossing occurs at the optimal switching angle.

4.2.3 Obtaining the Optimal Switching Angles

The implementation of the RTSHE can be divided into two routines. A short routine is used when there is a change in the output voltage fundamental frequency, and a longer routine is used when there is a change in either the modulation index, or the number of switching events per fundamental cycle. Typically, under the steady-state conditions, the short routine will be executed. When there is a change in the modulation index, a subroutine to calculate the new polynomial coefficients is triggered as shown in Fig. 4.2.

First, the reference voltage angles of the three-phase reference voltage are extracted. Then the optimal switching angles are obtained by a simple substitution of $x = \cos(\phi)$ and $x = -\cos(\phi)$ in $P(x)$, where ϕ is the reference angle of the phase voltage. When the value of the polynomial is equal to zero, a root of the polynomial is detected as shown in Fig. 4.4. To extract the switching

command S_a in real-time, the authors present a technique similar to Descartes' sign rule as shown in the large square in Fig. 4.2.

The proposed technique allows for obtaining the actuation commands in real-time without the need to solve the roots of the polynomial, which cannot be done in determinate real-time.

There is no need to worry about sorting the optimal switching angles from lower value to larger value. The direct substitution produces the switching angles with the correct order. The solution of the polynomial does not require great computational effort as it is a direct substitution and does not involve an iterative process or initial guessing. Furthermore, the proposed algorithm is valid for multilevel inverters. The only thing that needs to be changed is to use (4.7) instead of (4.6) and rearrange the logic in Fig. 4.2 to provide the switching functions for all of the switches.

The straightforward evaluation of a polynomial using a floating point controller would follow this form: p_0x^n is calculated, then $p_1x^{n-1}, \dots, p_{n-2}x$, and finally all the terms are added. Such a process requires $2n - 1$ multiplications and n additions. To optimize this process, one can use Horner's rule to rearrange the computation of the polynomial. Horner's rule requires n multiplications and n additions [83]. Furthermore, there is no need to store the partial results since each quantity arising during the calculation can be used immediately after it has been computed. The computational effort can be further reduced by adaptation of the coefficients [83]. Since the leading coefficient in RTSHE polynomials has the largest value, the division by the leading coefficient will never lead to instability.

4.3 Comparison with the Offline Selective Harmonic Elimination

The traditional approach of implementing the selective harmonic elimination method is by solving the transcendental system of equations (4.2) using an iterative method. Since the solution needs to be evaluated for each possible modulation index, it is more convenient to solve for a limited number of modulation indices and extrapolate the values of the optimal switching angles between every

two solutions and store the data in the form of curve fitting polynomials. The interested reader may check [84] where the Newton-Raphson iterative method is used to solve the transcendental equations. As the number of selected harmonics increases, Newton's method becomes more sensitive to the initial conditions. For instance, to achieve convergence for six switching angles per quarter fundamental cycle, one needs to use the solution from the previous few steps instead of the most recent step. The uncertainty of the initial guess along with the indeterminate convergence time, if any, makes the real-time implementation of the transcendental equations an unattractive approach. Since the real-time selective harmonic elimination involves more mathematical processes, it is essential to check the numerical difference between the real-time solution and the solution obtained by offline calculation. Fig. 4.5 shows the numerical difference of the first three odd harmonic magnitudes of the real-time approach and the offline approach in both 60 Hz and 120 Hz fundamental frequencies. Fig. 4.6 shows similar results when eliminating the first six odd harmonics.

In Fig. 4.5, the value of the third harmonic in the offline approach is larger than the one from the real-time implementation. This is due to the inaccuracy of the curve fitting. It can be improved by creating a higher order polynomial to represent the curve. In our case, the order of the curve fitting polynomial is kept equal to the order of the univalent polynomial of the real-time implementation. The norm of residuals along with other error-contributing factors are quantified in Table I. Fig. 4.7 shows the total harmonic content divided by the fundamental component. This number does not change when n is increased from 4 to 6 to 8, ..., etc. The benefit of increasing n is that all of the harmonics concentration will be located to the right of the last eliminated harmonic. This results in harmonic content with higher frequency. Therefore, the current resulting from these harmonics will have less amplitude due to the inductive nature of the load impedance ($Z_L = 2\pi fL$). Furthermore, it is important to note that the total harmonic content is exactly the same as the one produced by the offline SHE.

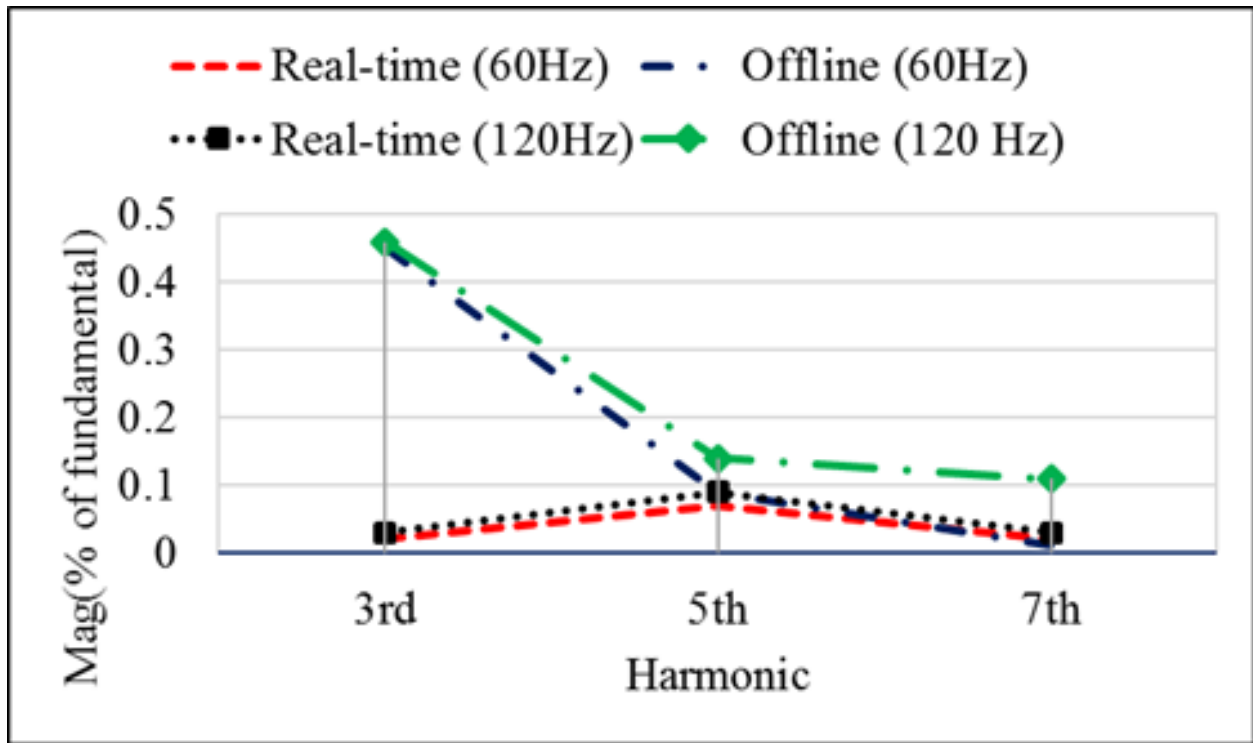


Figure 4.5 Numerical results show a comparison between the proposed real-time method and the conventional offline method eliminated harmonics magnitude when eliminating the first three odd harmonics. The results shown are in two fundamental frequencies 60 Hz and 120 Hz.

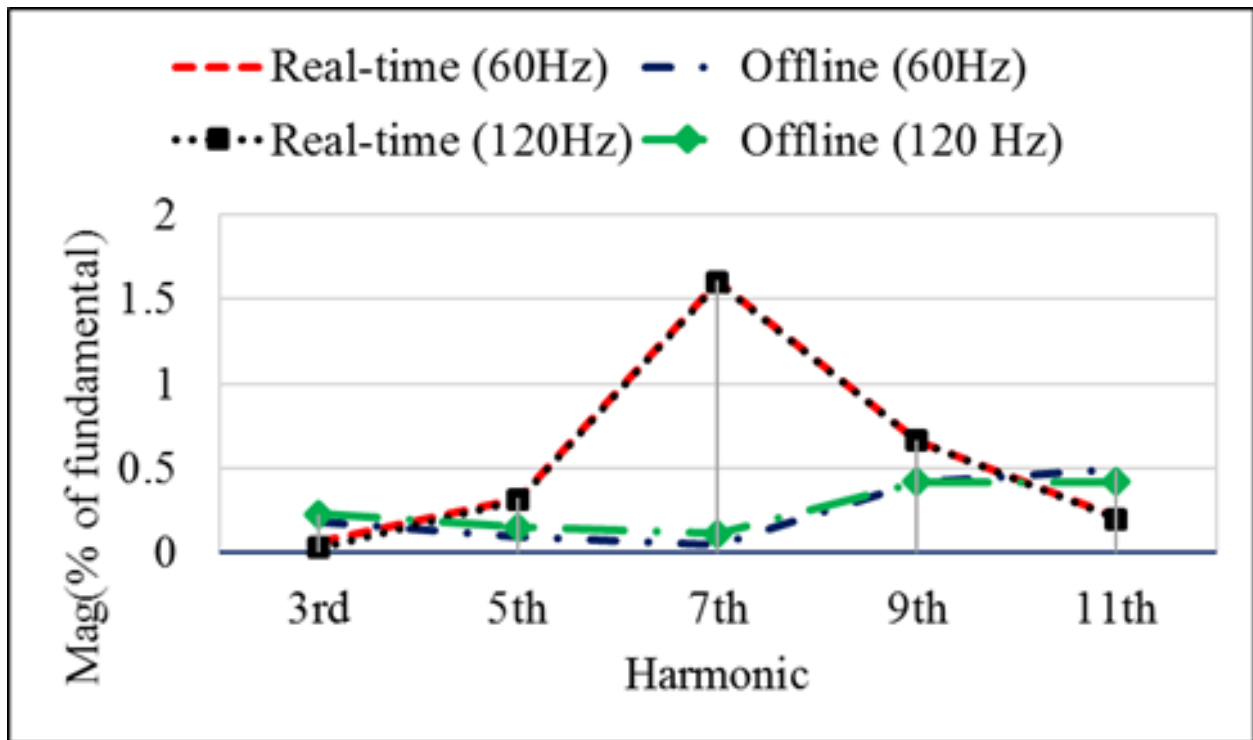


Figure 4.6 Numerical results show a comparison between the proposed real-time method and the conventional offline method eliminated harmonics magnitude when eliminating the first five odd harmonics. The results shown are in two fundamental frequencies 60 Hz and 120 Hz.

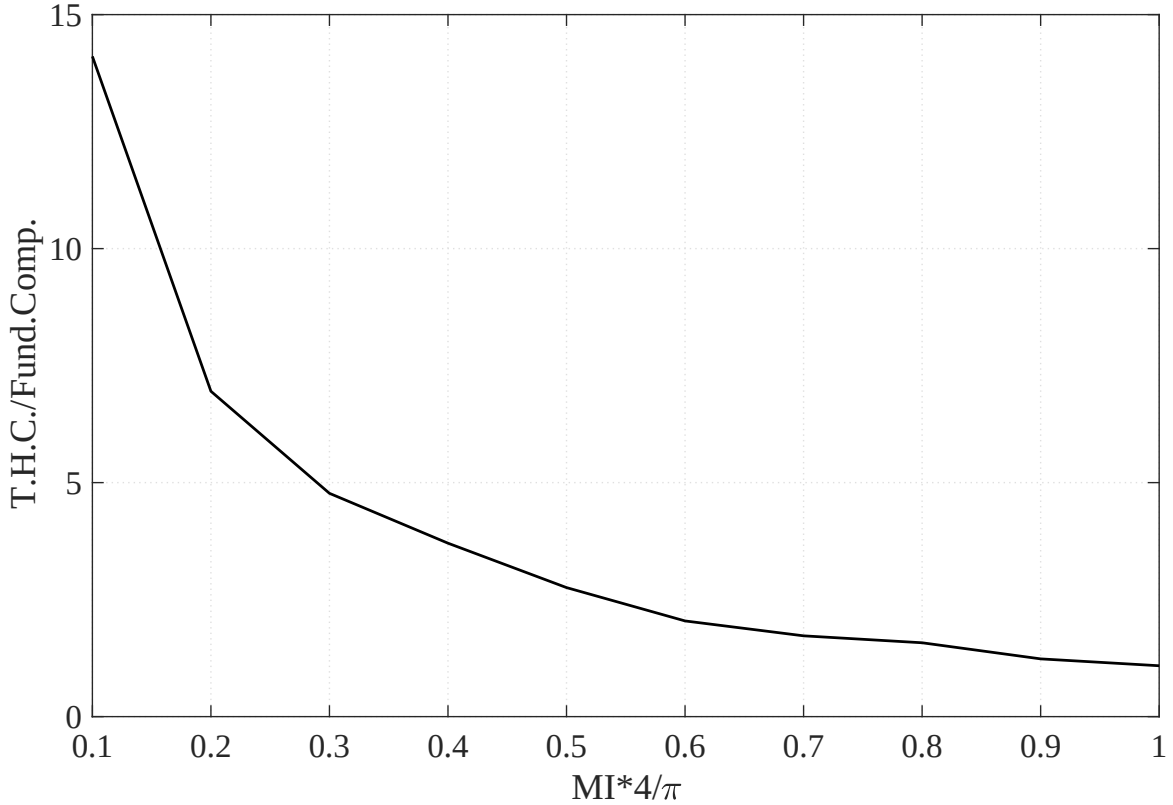


Figure 4.7 Total harmonic content divided by the fundamental component for both the offline SHE and the proposed real-time SHE. Note that this number does not change by changing the number of eliminated harmonics, instead, the harmonics get shifted to the right of the last eliminated harmonic and this result in a better load current performance. This is due to the fact that higher-frequency harmonics face higher impedance in an inductive load.

4.4 Selective Harmonic Modulation

So far the intent behind implementing the RTSHE is to achieve a desired modulation index and to eliminate the lower order harmonics. In this section, we show that the proposed RTSHE can be generalized such that the lower order harmonics can have any arbitrary value rather than zero. Hence the generalized method is called the real-time selective harmonic modulation RTSHM.

Starting from the system of algebraic polynomials in (4.3), $s_1, s_3, \dots, s_{2n-1}$ can be obtained using the proposed recursive algorithm:

$$T_{2n-1}(x)|_{(x^{2n-1}=s_{2n-1})} = \frac{1}{2} + \frac{n\pi b_{2n-1}}{8V_{dc}}. \quad (4.22)$$

To better understand the proposed algorithm, we apply it to the earlier example: for that matter the modulation index is kept at 0.6283 and the third harmonic $b_3 = 0.2$. The substitution of the Chebyshev's first polynomial ($T_1 = x$) in (4.22) yields

$$s_1 = \frac{1}{2} + \frac{\pi b_1}{8V_{dc}}.$$

Similarly, the substitution of Chebyshev's third polynomial ($T_3 = 4x^3 - 3x$) in (4.22) yields

$$4s_3 - 3s_1 = \frac{1}{2} + \frac{3\pi b_3}{8V_{dc}}$$

$$s_3 = \frac{3s_1}{4} + \frac{3\pi b_3}{32V_{dc}} + \frac{1}{8}$$

and

$$s_5 = \frac{5s_3}{4} - \frac{5s_1}{16} + \frac{5\pi b_5}{128V_{dc}} + \frac{1}{32}$$

$$s_7 = \frac{7s_1}{64} - \frac{7s_3}{8} + \frac{7s_5}{4} + \frac{7\pi b_7}{512V_{dc}} + \frac{1}{128}.$$

As it can be seen, the value of s in (4.6) is only dependent on the value of b_1 while in (4.22) it is dependent on the value of each harmonic including b_1 . Therefore, we can assign any value to any harmonic and the rest of the algorithm, remains unchanged. Note that if the modulation of several harmonics is needed to be implemented using the offline approach, with each modulated harmonic, the size of the look-up table will be doubled. This makes it impossible to solve and store within the limited memory of the microcontroller.

4.5 Experimental Results

Experimental tests have been performed to validate the efficacy of the proposed method. The three-phase, two-level voltage source inverter shown in Fig. 4.1 is used. The DC-link voltage is $V_{dc} = 100$ V. The motor is replaced with equivalent RL load $R = 5 \Omega$ and $L = 2$ mH.

The controller used in the experiment is dSPACE CP1103. The digital output pins were used to generate the switching signals. Therefore, the calculations of the algorithm are done by the dSPACE PowerPC PCC 750GX and Xilinx Spartan 6 FPGA.

The first test is conducted to investigate the effect of the sampling frequency on the accuracy of the generated switching signals. The RTSHE algorithm was set to calculate the new polynomial coefficients and substitute the value of the reference voltage angle into the new polynomial (long routine). Since the algorithm requires approximately $6 \mu s$, the fixed sampling time is set to $8 \mu s$. Fig. 4.8 and Fig. 4.9 show a comparison between the waveforms resulting from the real-time algorithm and the waveforms resulting from using the offline method. Note that the offline method uses a curve fitting polynomial to obtain the optimal switching angle. The order of the curve fitting polynomial is set to the same order as the polynomial in the real-time algorithm. The offline method requires approximately $4 \mu s$ turnaround time. For comparison, the fixed sampling frequency for the offline method is also set to $8 \mu s$. The experimental waveform shows that the value of the eliminated harmonics is still very close to zero. This is justifiable because at 60 Hz frequency, it takes 0.0167 s to complete one cycle. An update for the switching angle can be made by the controller every $8 \mu s$. This leads to 2087 updates per fundamental cycle. Therefore, the error of the generated switching angle cannot be larger than ± 0.172 degrees. Fig. 4.10 and Fig. 4.11 show similar results when the fundamental frequency is set to 120 Hz. In this case, the error of the switching angles of the real-time method is bounded by ± 0.345 degrees. Slight difference in the spectrum can be observed at the frequencies beyond the eliminated harmonics on the right side of the FFT window.

Fig. 4.12 and Fig. 4.13 show the steady-state performance of the proposed RTSHE method when the fundamental frequency is 60 Hz and 120 Hz, respectively, and the first eight odd harmonics are eliminated. It is clear from the FFT results that the first seven odd harmonics are successfully eliminated for both cases.

Fig. 4.14 shows the transient behavior of the RTSHE method when the switching frequency of the system is changed from 32 Hz to 16 Hz. Fig. 4.15 shows the transient behavior when M_i

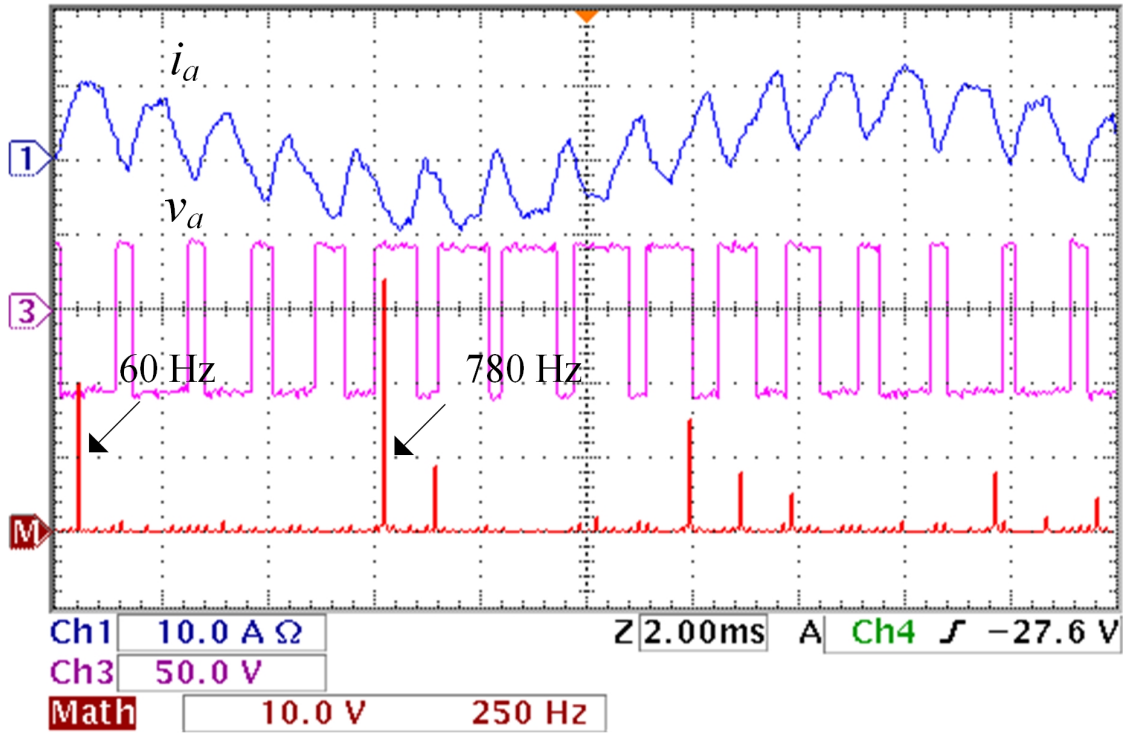


Figure 4.8 Experimental results of the line current i_a , line-neutral voltage v_a and the spectrum of v_a using the proposed real-time algorithm. The fundamental frequency is 60 Hz.

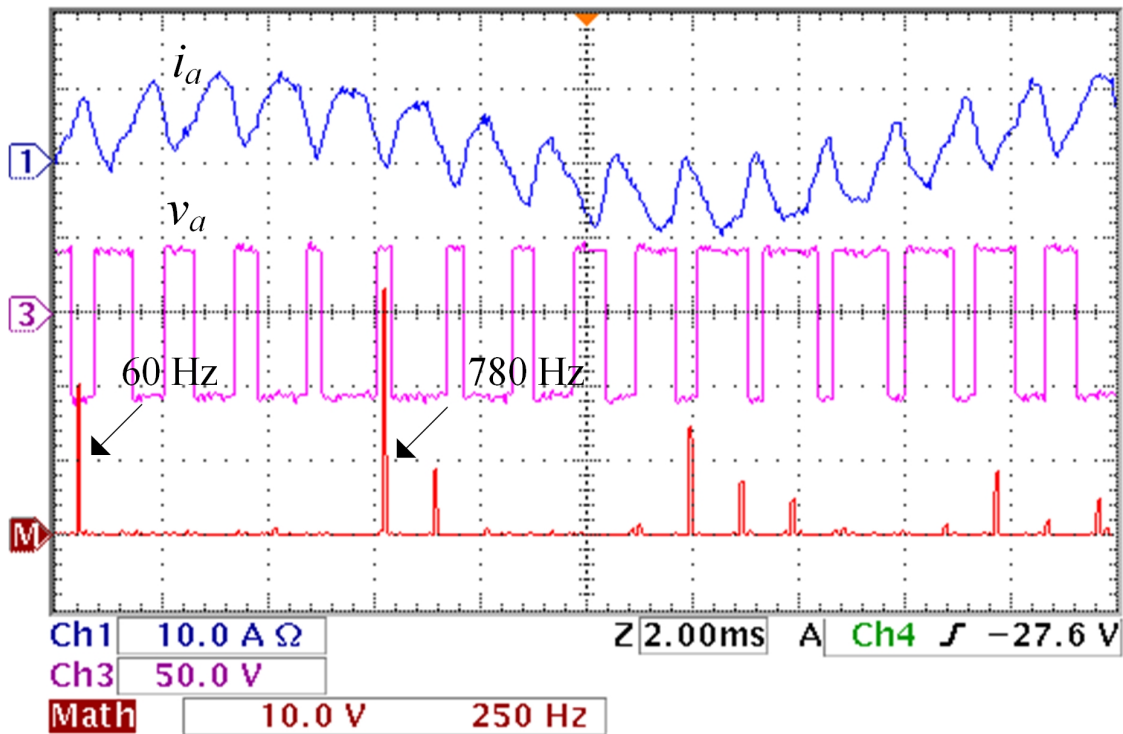


Figure 4.9 Experimental results of the line current i_a , line-neutral voltage v_a and the spectrum of v_a using the conventional offline method. The fundamental frequency is 60 Hz.

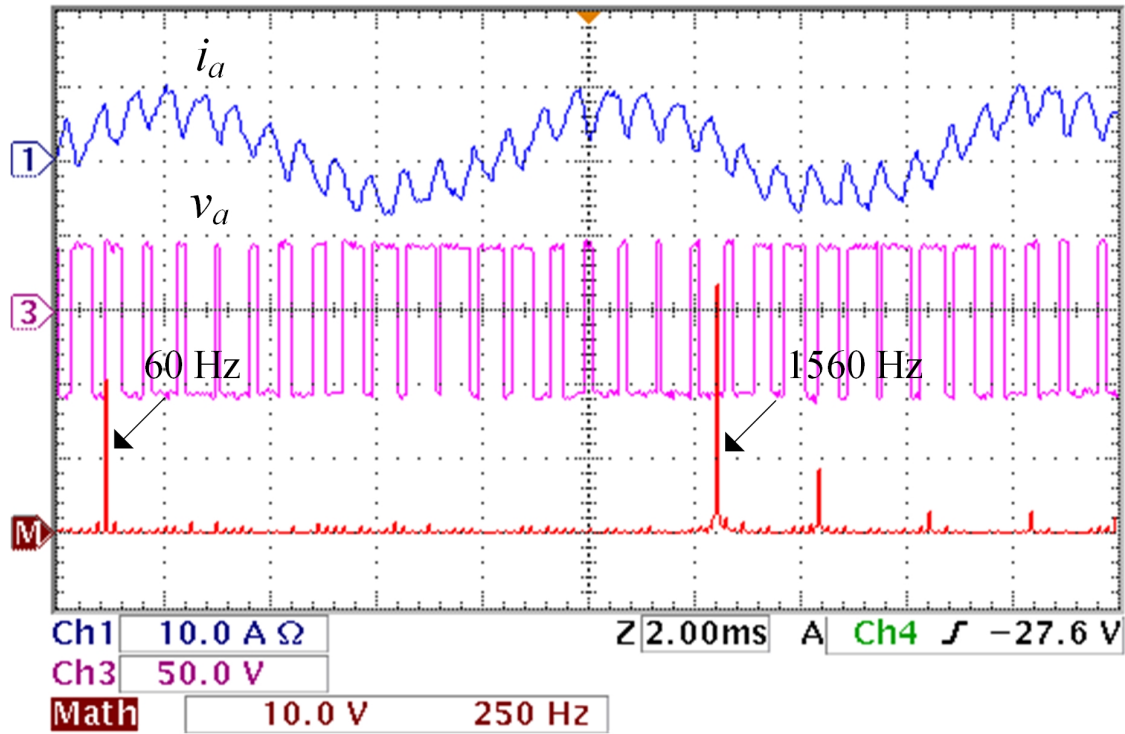


Figure 4.10 Experimental results of the line current i_a , line-neutral voltage v_a and the spectrum of v_a using the proposed real-time algorithm. The fundamental frequency is 120 Hz.

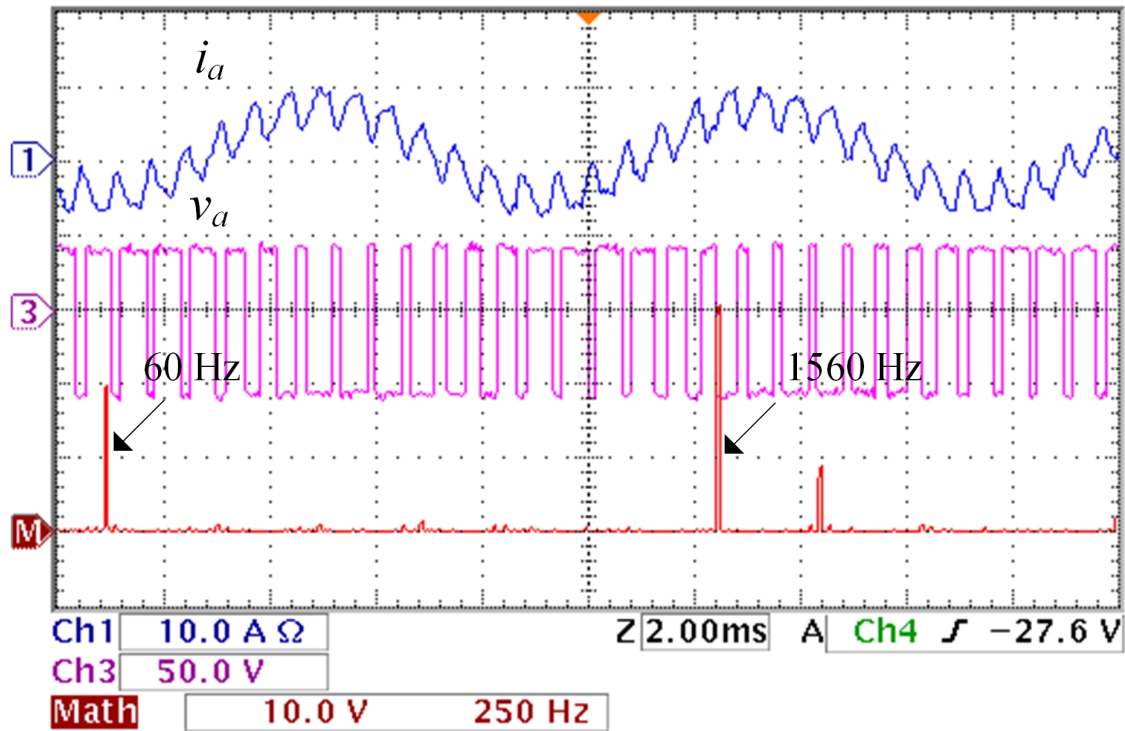


Figure 4.11 Experimental results of the line current i_a , line-neutral voltage v_a and the spectrum of v_a using the conventional offline method. The fundamental frequency is 120 Hz.

Table 4.1 Summary of the comparison between the conventional offline method and the proposed RTSHE.

Trade	Conventional Offline Method	Proposed RTSHE
Error Due Numerical Conv.	$\approx 10^{-15}$	$\approx 10^{-15}$
Error Due Implementation	Norm of residuals = 0.076104.	No implementation error
Error Due Sampling	0.08 degree and it is proportional to the fundamental frequency and n	0.172 degree and it is proportional to the fundamental frequency and n
Offline Complexity	Requires solving difficult mixed integer programming problem. Especially for n is large.	No offline solution required
Online Complexity	Minimal	The additional calculation almost double the turn around time compared to the offline method
Transient Behaviour	Standard, My suffer high current transient when transferring from a set of angles to another due to change in MI	Improved due to the high achievable MI precision
Ablity to Remove the Selected Harmonics	Able to remove the selected harmonic.	Able to remove the selected harmonic. THD is the same as the one from the offline method

is increased from 0.6 to 0.8. Fig. 4.16 shows the transient behavior when the inverter reduces the switching frequency and concurrently increases the fundamental frequency. This is very common in high power inverters when the high power GTOs are only able to switch at a rate less than 100 Hz. The load current shows a seamless transition in all of these cases. The concurrent change in the fundamental and switching frequencies is tested at random instants within the fundamental period to inspect any possible current spikes. As shown in Fig. 4.17, no current spike was ever observed. For comparison, the current transient behavior of the conventional offline method is shown in Fig. 4.18.

Fig. 4.19(a) to (c) demonstrate the ability to achieve control over the third harmonic without affecting the fundamental component of the phase voltage and the THD of the load current.

To further reduce the execution effort, the coefficients of the polynomial can be pre-calculated and hard-coded in the controller. To have the flexibility to operate at any M_i , the algorithm that calculates the polynomial coefficient needs to be executed by the controller in real-time. Note that this is required only when the M_i changes. The execution time of the control algorithm only takes $6 \mu s$, which leaves ample room to increase the system fundamental frequency while maintaining high-quality waveforms. Furthermore, the calculation of the polynomial and the actuation command extraction can be done by the external FPGA, especially when the order of the polynomial is large. Using an external FPGA allows parallel schemes for software realization, and based on the number of the available parallel units, the overall turnaround time can be further reduced [85].

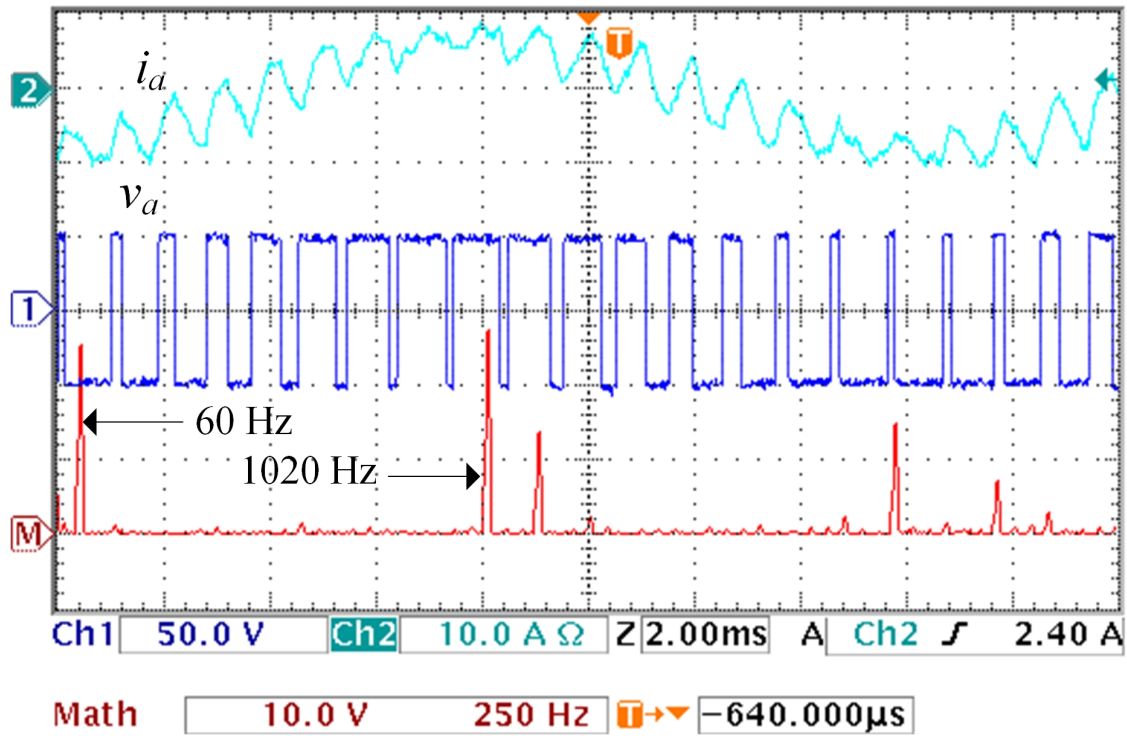


Figure 4.12 Experimental results of RTSHE load current i_a and the phase voltage v_a at a fundamental frequency of 60 Hz.

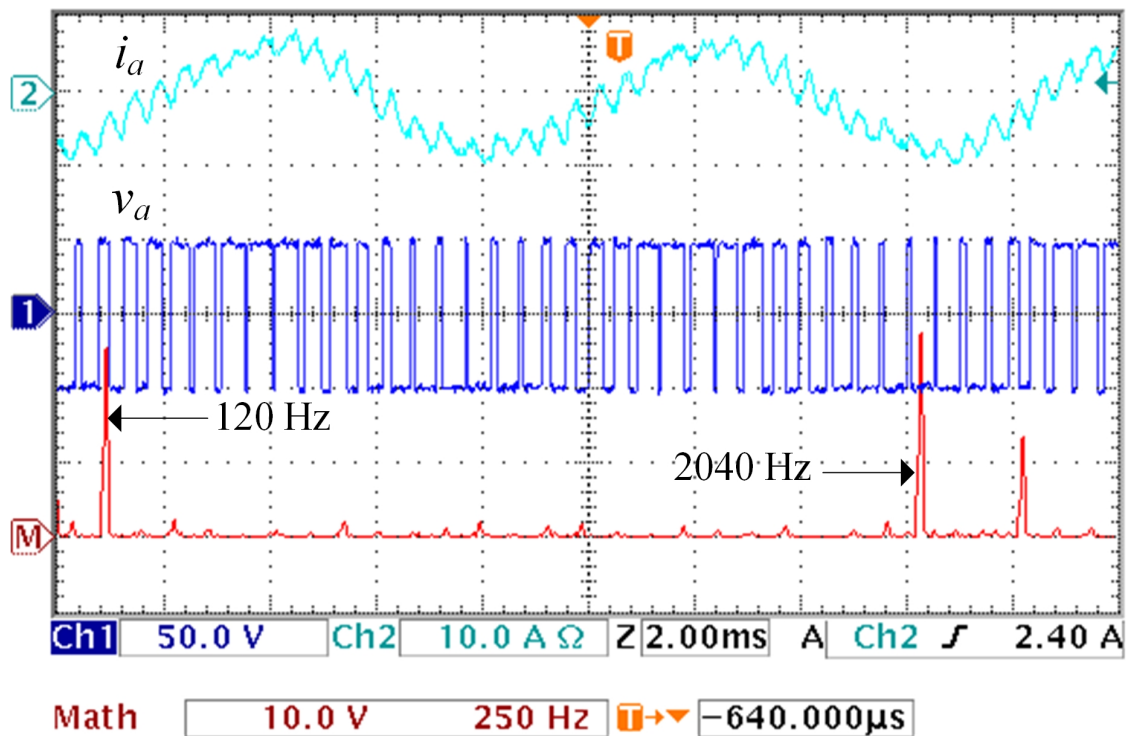


Figure 4.13 Experimental results of RTSHE load current i_a and the phase voltage v_a at a fundamental frequency of 120 Hz.

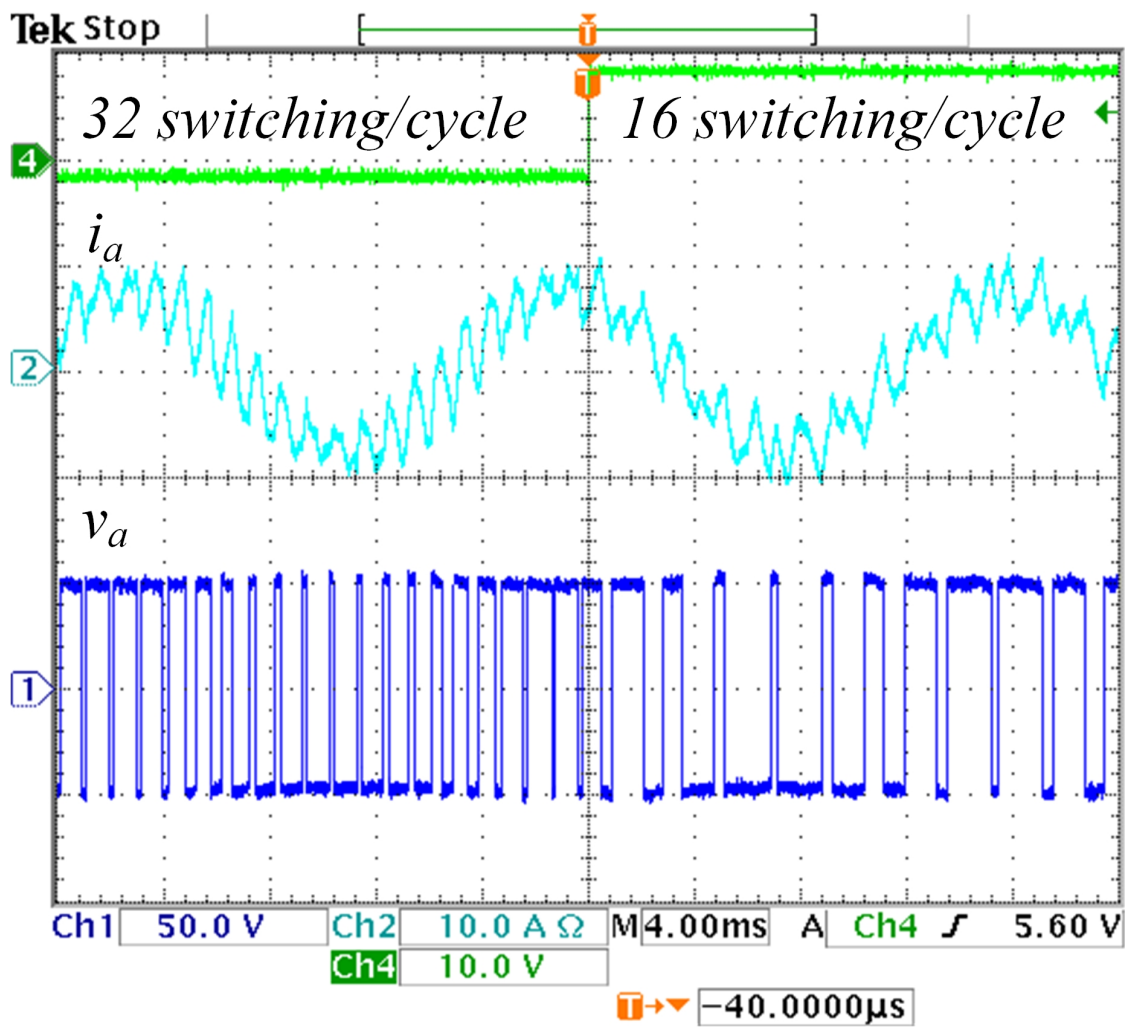


Figure 4.14 The transient behavior of the load current i_a and the phase voltage v_a when changing the switching frequency.

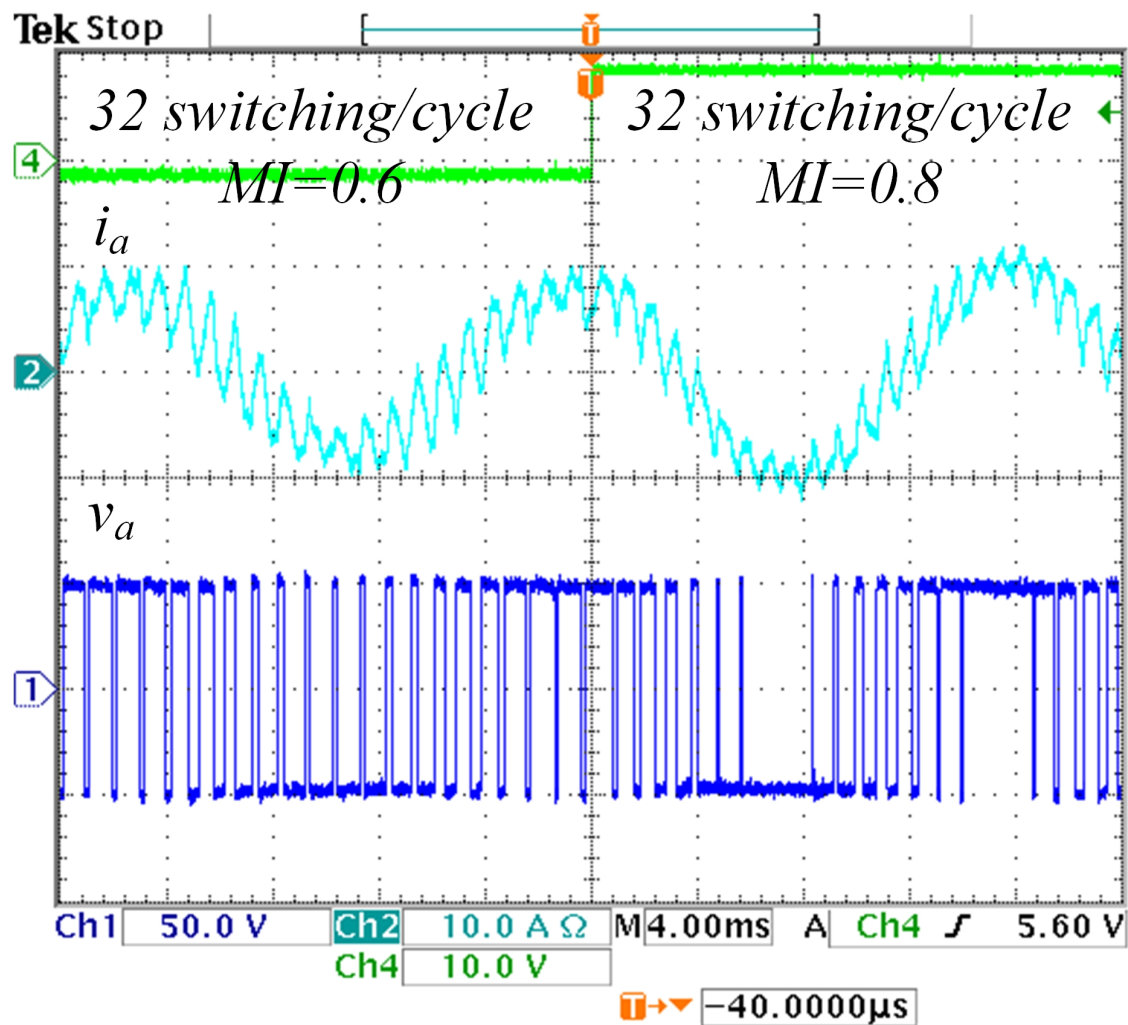


Figure 4.15 The transient behavior of the load current i_a and the phase voltage v_a when changing MI.

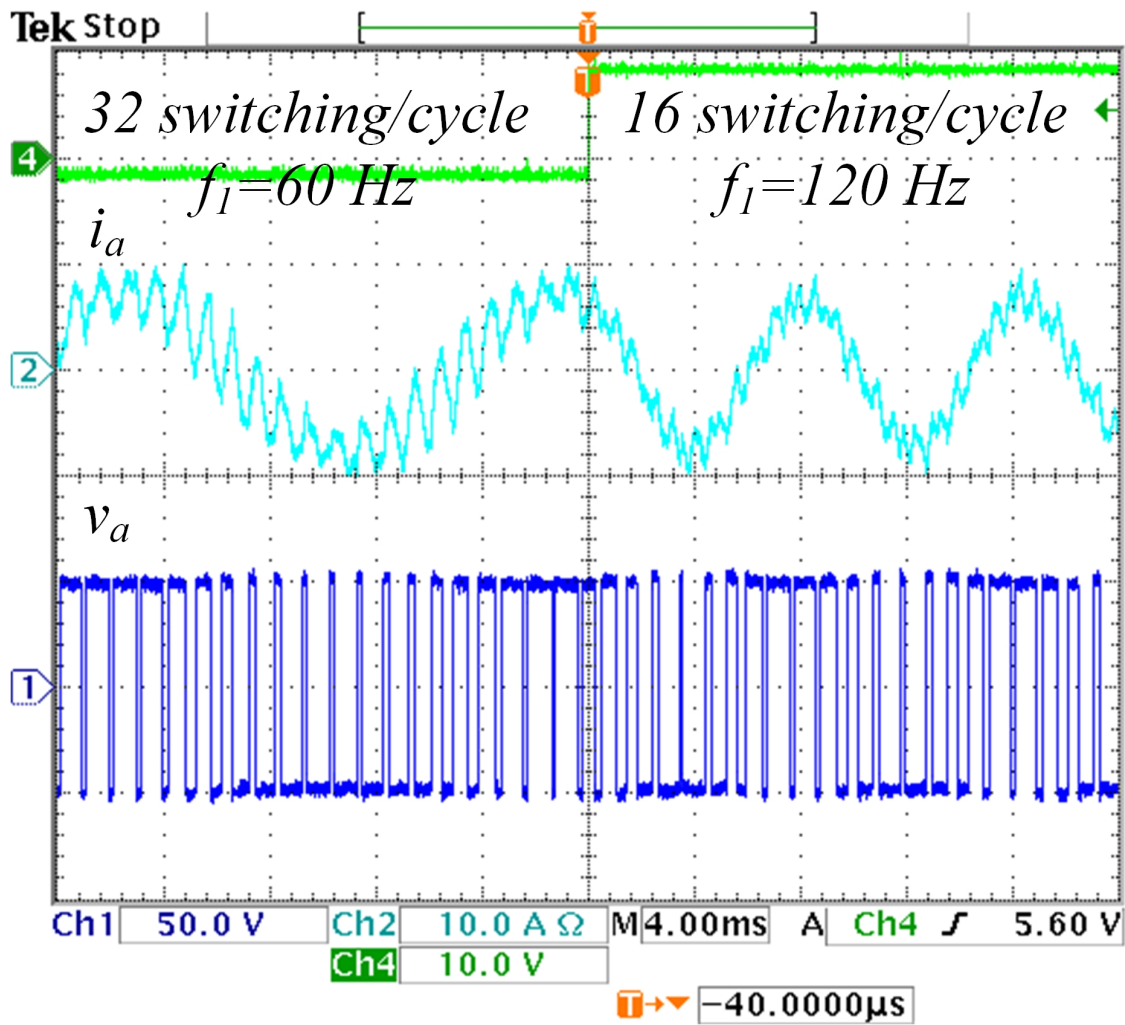


Figure 4.16 The transient behavior of the load current i_a and the phase voltage v_a when changing both fundamental and switching frequencies at the same instant.

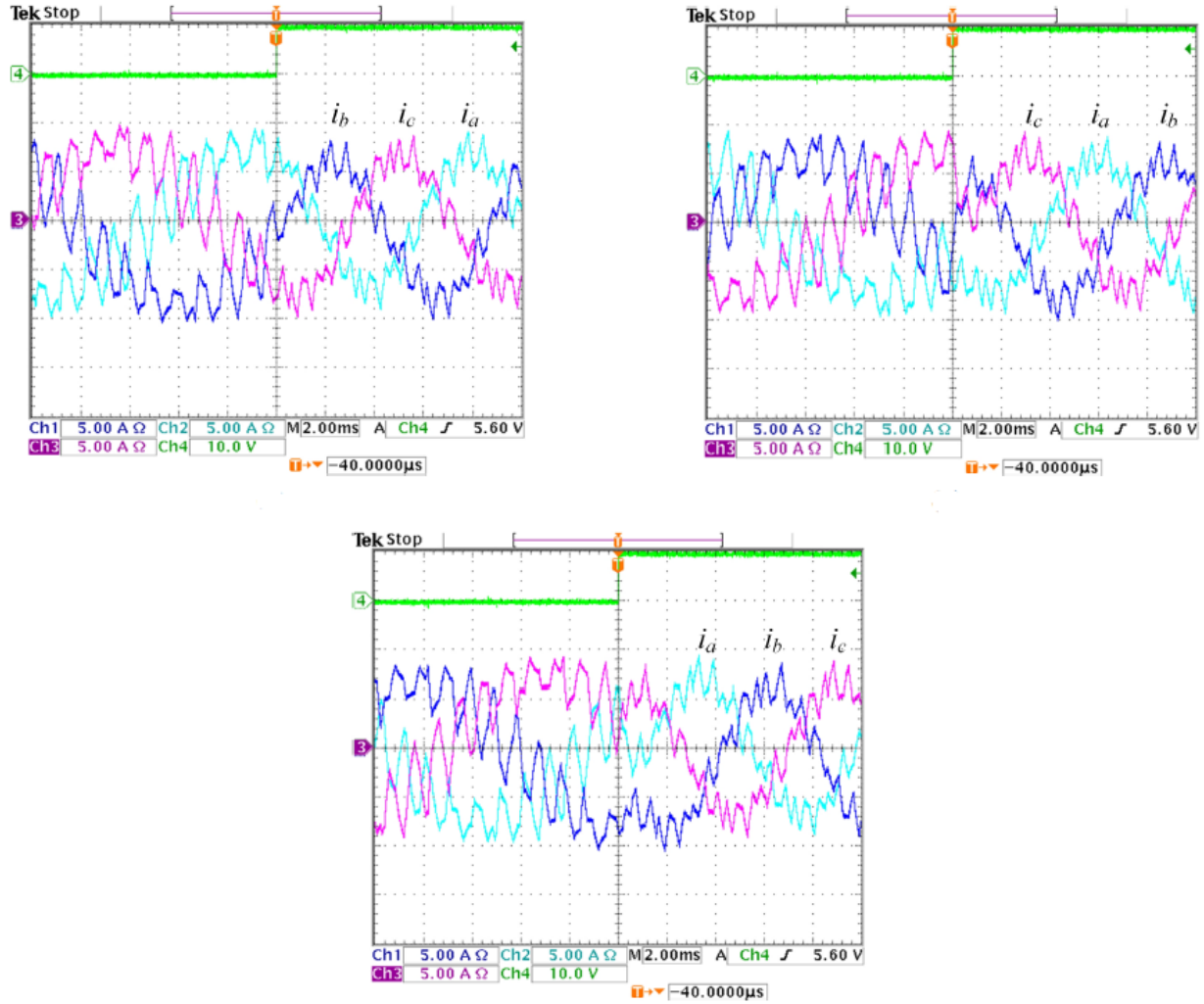


Figure 4.17 The transient behavior of the proposed RTSHE load currents i_a , i_b , and i_c when a concurrent change in the fundamental and switching frequencies are randomly requested. No current spike is detected.

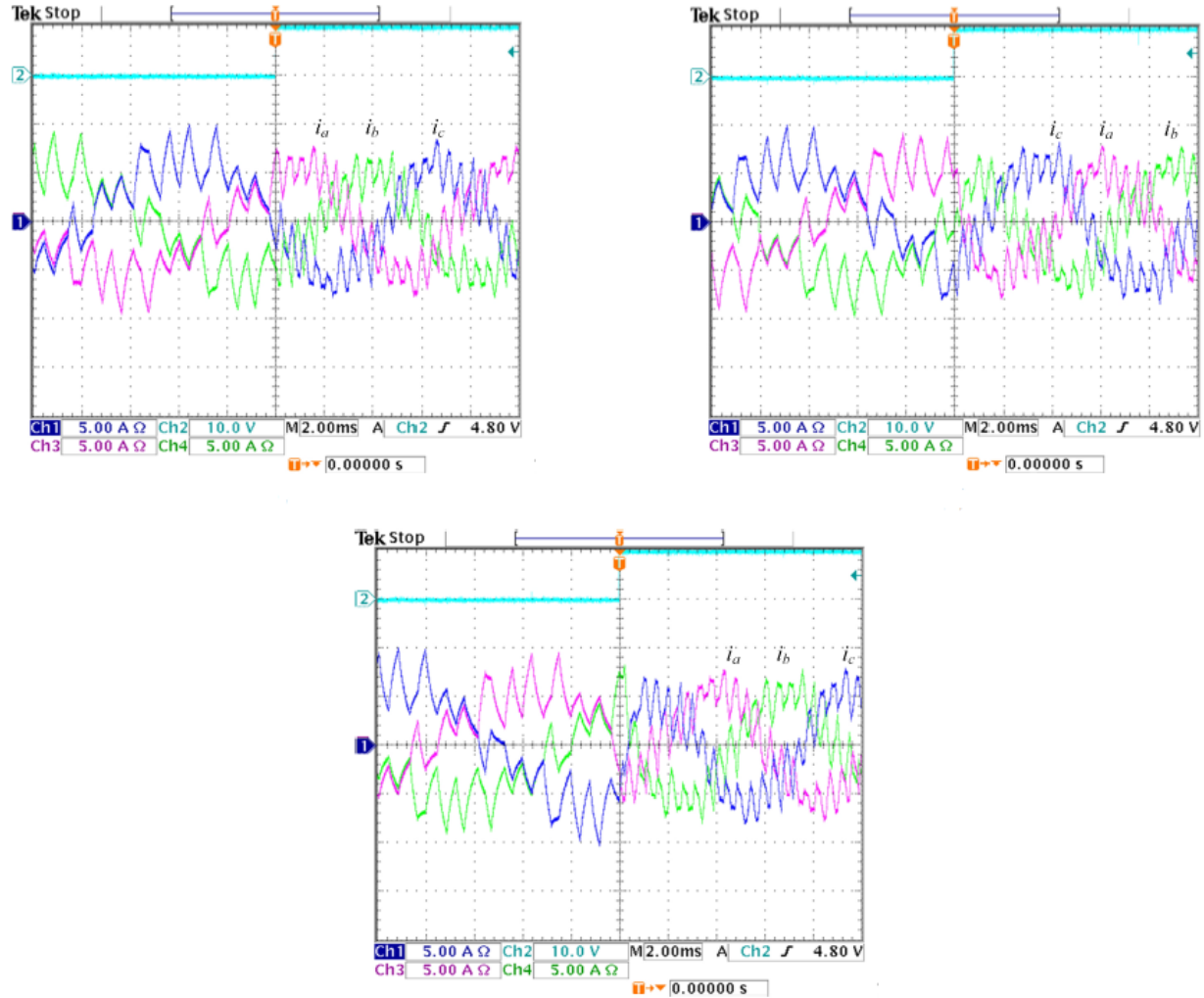
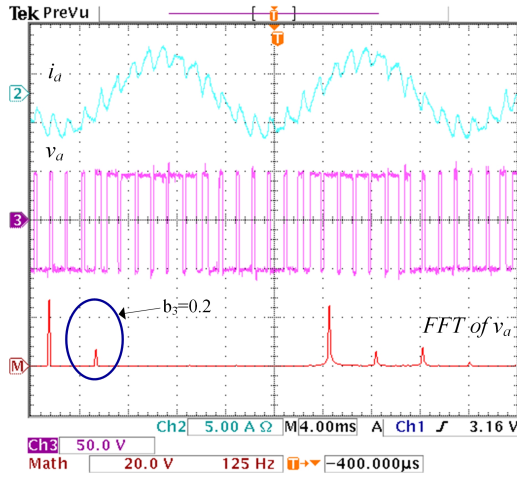
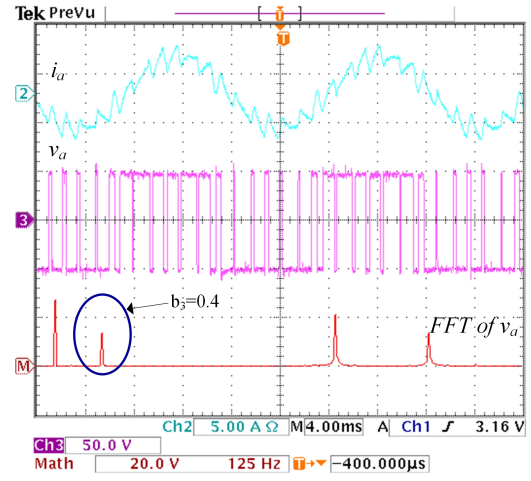


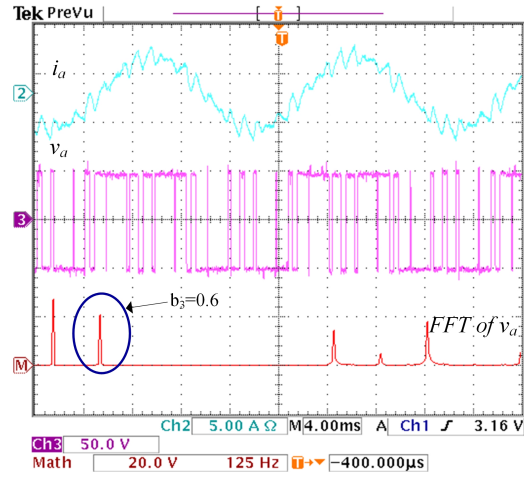
Figure 4.18 The transient behavior of the conventional offline SHE load currents i_a , i_b , and i_c when a concurrent change in the fundamental and switching frequencies are randomly requested.



(a)



(b)



(c)

Figure 4.19 The real-time controllability of the third harmonic: (a) $v_{b3} = \frac{\pi b_3}{4} * V_{dc}/2 = \frac{\pi 0.2}{4} * 50 = 7.855$ V, (b) $v_{b3} = \frac{\pi b_3}{4} * V_{dc}/2 = \frac{\pi 0.4}{4} * 50 = 15.71$ V, and (c) $v_{b3} = \frac{\pi b_3}{4} * V_{dc}/2 = \frac{\pi 0.6}{4} * 50 = 23.565$ V.

Chapter 5

Switched-Capacitor Voltage Boost

Converter for Electric and Hybrid Electric Vehicle Drives

5.1 Introduction

In May 2017, the International Monetary Fund (IMF) published a white paper regarding energy transition and the oil market beyond 2040. In the paper, the authors concluded that a fast adaptation scenario for electric vehicles is likely to happen. By 2042, around 93% (290 million) of all vehicles in the U.S. will be electric [86]. At that time, the internal combustion-based automakers that fail to transition to electric cars (EVs) will soon have a Kodak moment.

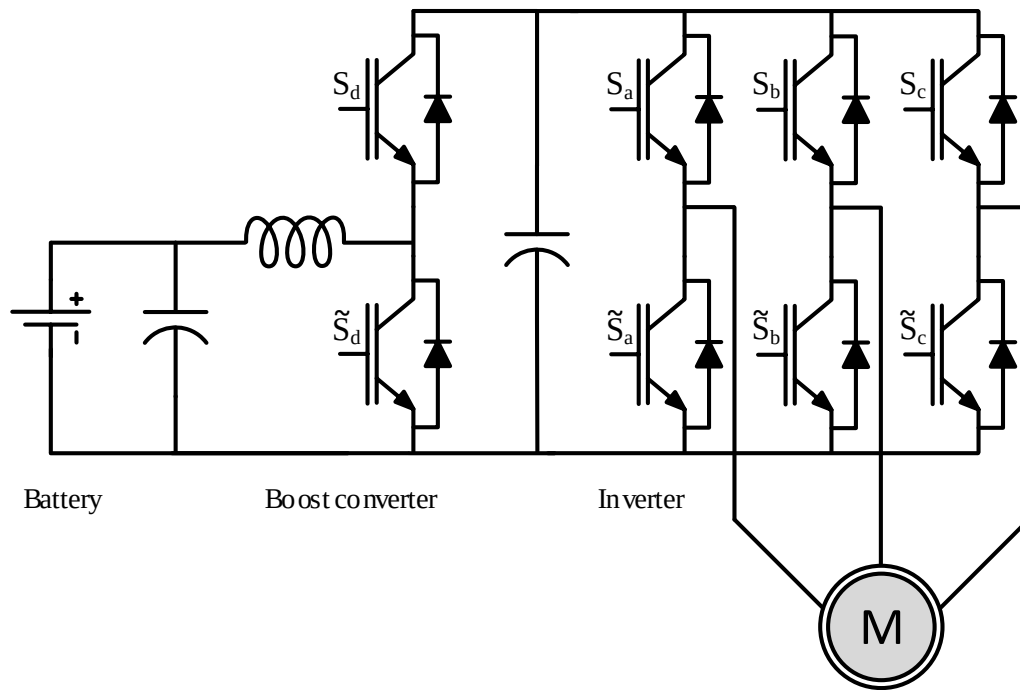
In ideal world, the fast adaptation of EVs depends on how fast the EVs will outperform the internal combustion-based cars in mileage and price. The potential development of EV technology falls broadly into three categories: battery chemistry, autonomous driving, and the power electronic units. With regard to the last category, one of the most critical power conversion units is the drive train. The improvement of the drive train results in size reduction, fast speed/torque dynamic, and better utilization of battery power. Most of the existing EVs utilize a two-level voltage source

inverter (VSI) with or without boost stage due to its reliability [87] [88]. The opportunities to improve the EV power train can be addressed by exploring the limitations of VSIs.

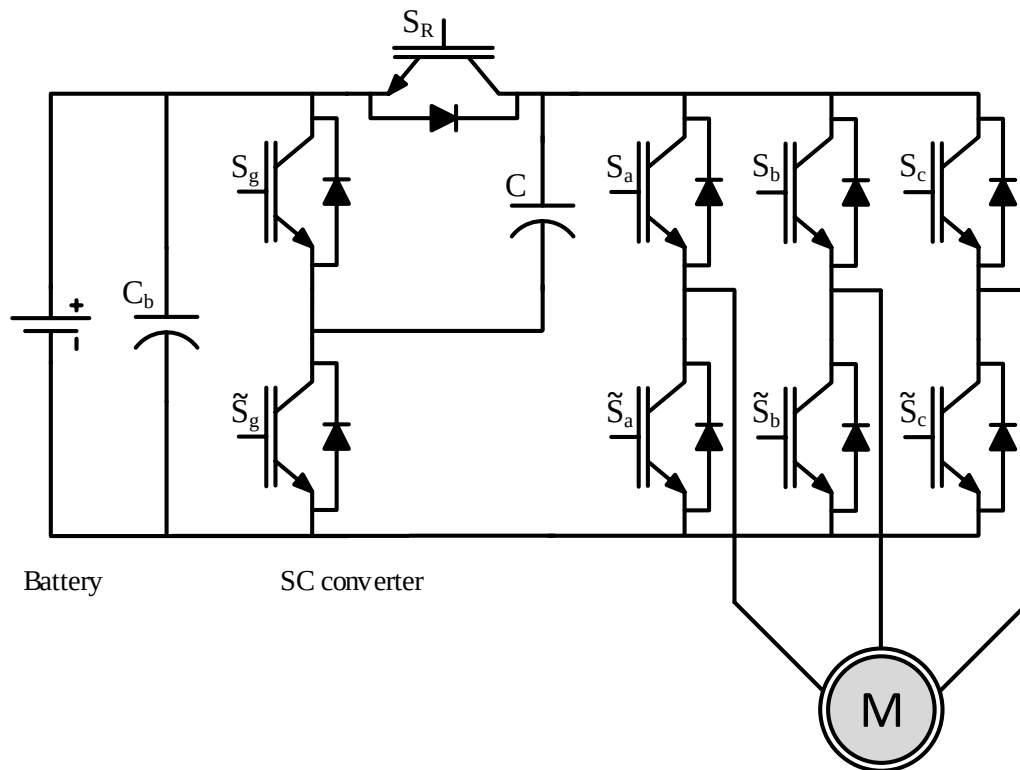
VSIs are inherently buck converters. Therefore, the dc-link voltage has to be higher than the dc or ac input voltage. For applications where the available dc voltage is limited, an additional dc-dc boost converter is needed to obtain the desirable ac voltage [89]. For the commercial traction electric drive system, two configurations are commonly used: the first one is a battery directly powering a two-level inverter; the second one is a battery connected to the inverter with an intermediate dc-dc boost stage as shown in Fig. 5.1(a) [90].

The first configuration of a battery directly connected to the dc-bus offers minimum stress on the inverter side, but it requires an expensive battery with a large number of cells in series to achieve the necessary dc-link voltage [91]. The series connection of battery cells poses a challenge in terms of the slow charge equalization speed [92]. Furthermore, the isolation of one faulty cell in the series connection leads to a voltage drop in the overall series connection. In this case, the entire series row of batteries needs to be disconnected from the dc-link to avoid a short circuit with other non-faulty series rows of cells. The first configuration is seen only in extended-range electric vehicles (with large batteries) such as Tesla (75 to 100 kWh) [93].

The second configuration shown in Fig. 5.1(a) is used in hybrid electric vehicles (HEVs) and plug-in HEVs (PHEVs) where the battery energy rating ranges from 5 to 50 kWh. While the current limit in the machine is dependent on its ability to dissipate the heat, the voltage limit is dependent on the dc-link voltage level. Therefore, using a dc-dc boost converter extends the constant torque region [94]. Owing to the superior current density characteristics of the SiC-MOSFET compared to the Si-IGBT, the current density of the 1200V SiC-MOSFET is similar to the current density of the lower-voltage 600V Si-IGBT [95]. This advantage leads to a reduction in semiconductor die area by a factor of two, and this is accomplished by utilizing high-voltage motors and SiC-MOSFETs [96]. Furthermore, the reduced current peak at a higher voltage leads to smaller peak losses by a factor of four [96]. Since power loss translates directly into cooling system capacity, a significant reduction in cooling system size and weight, as well as an improvement in EV range,



(a)



(b)

Figure 5.1 The schematics of (a) the conventional inverter-converter topology and of (b) the proposed switched-capacitor voltage boost converter.

can be achieved.

The conventional boost stage depicted in Fig. 5.1(a) is not quite perfect. The power rating of the dc-dc converter must match the battery pack power, leading to a proportionally large inductor. The inductor is a heavy and costly component. Furthermore, the inductor copper and core losses increase proportionally with the size of the inductor. When boosted by a high-voltage ratio, the boost converter must operate with a high duty cycle where the efficiency is relatively low [97]. The partial power efficiency is also reduced, because the ac losses (switching loss and ac magnetic loss) depend on voltage but are nearly independent of current. At high duty cycles, the rms current applied to the bus capacitor is also quite high, which impacts the size and cost of the capacitor [96].

To overcome the above limitations of the traditional drive trains, this paper presents the switched-capacitor voltage boost (SC) converter and its control methods. Fig. 5.1(b) shows one version of the proposed SC converter. It employs a switched-capacitor circuit with the inverter to form a unified circuit. The switched capacitor circuit is used to create a multi-leveled dc-link voltage. Therefore, the proposed switched-capacitor circuit differs from the conventional one by not having the reverse blocking diode at the load side or the large filtering capacitor. The regulation of the output current and voltage is realized by unified control of both the inverter and the switched-capacitor stages.

The rest of the paper is organized as follows: After the introduction, the space vector operating principle of the SC converter is presented in Section II. The design and analysis of the SC converter are presented in Section III. The carrier-based modulation of the SC converter is presented in Section IV. Finally, simulation results, prototype, experimental results, and the conclusion are presented in section V and VI.

5.2 Space Vector Pulse Width Modulation of SC Converter

The switched-capacitor circuit at Fig. 5.1 (b) can have two possible states: one when the capacitor is charging shown in Fig. 5.2 (a)

$$V_{bat} = v_{cap} = v_i, \quad (5.1)$$

and one when the capacitor is discharging shown in Fig. 5.2 (b)

$$V_{bat} = v_{cap}; \quad v_i = 2V_{bat}, \quad (5.2)$$

$$i_i = S_a i_a + S_b i_b + S_c i_c. \quad (5.3)$$

In addition to these options, the other phase legs feature the eight known inverter states. There are fourteen overall feasible states in the SC converter, and they are depicted in the space vector hexagon shown in Fig. 5.3. One can observe that the states of the SC converter resemble a four-level inverter with phase voltage possibilities $\{\pm V_{bat}, \pm 2V_{bat}\}$.

To derive the dwell time for each vector, a few assumptions are made. First, in each sector, the four adjacent active vectors and the two zero vectors are used to synthesize the reference voltage vector. Second, during the discharge time, the capacitor voltage is assumed to be constant and equal to the battery voltage. Therefore, the dwell time during the discharge time needs to be minimized to allow minimum voltage drop during the capacitor discharge.

Assume that the reference voltage vector $\mathbf{V}_{ref}$ can be synthesized using the following virtual vectors:

$$\mathbf{V}_{ref} T_s = \mathbf{V}_x t_x + \mathbf{V}_y t_y + \mathbf{V}_0 t_0 \quad (5.4)$$

where

$$\mathbf{V}_x t_x = \mathbf{V}_{11} t_{11} + \mathbf{V}_{12} t_{12} \quad (5.5)$$

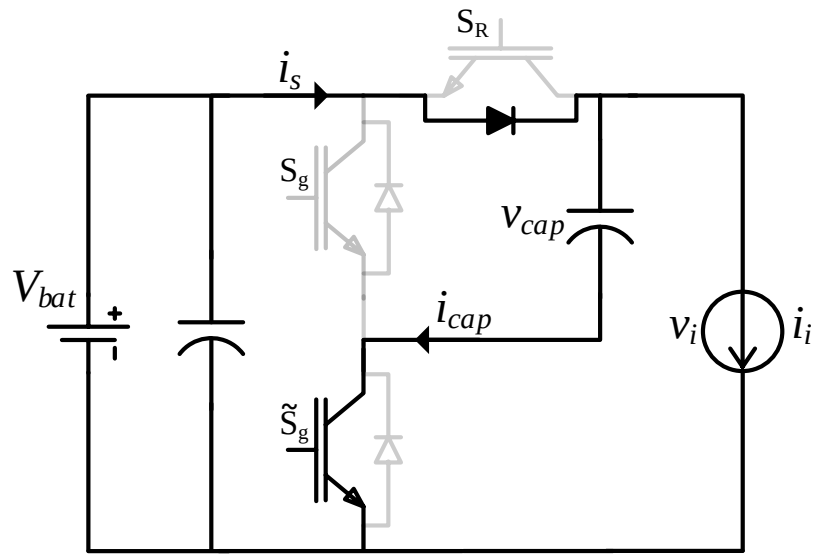
and

$$\mathbf{V}_y t_y = \mathbf{V}_{21} t_{21} + \mathbf{V}_{22} t_{22}. \quad (5.6)$$

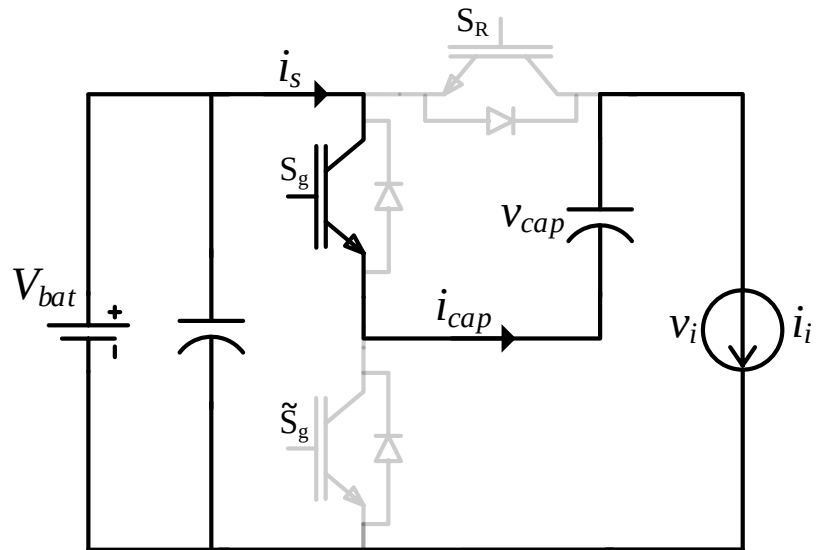
With some algebraic manipulation, the following dwell time for the four active vectors can be obtained:

$$t_{11} = (1 - A) t_x \quad (5.7)$$

$$t_{12} = A t_x \quad (5.8)$$



(a)



(b)

Figure 5.2 (a) Charging and (b) discharging equivalent circuits of SC converter.

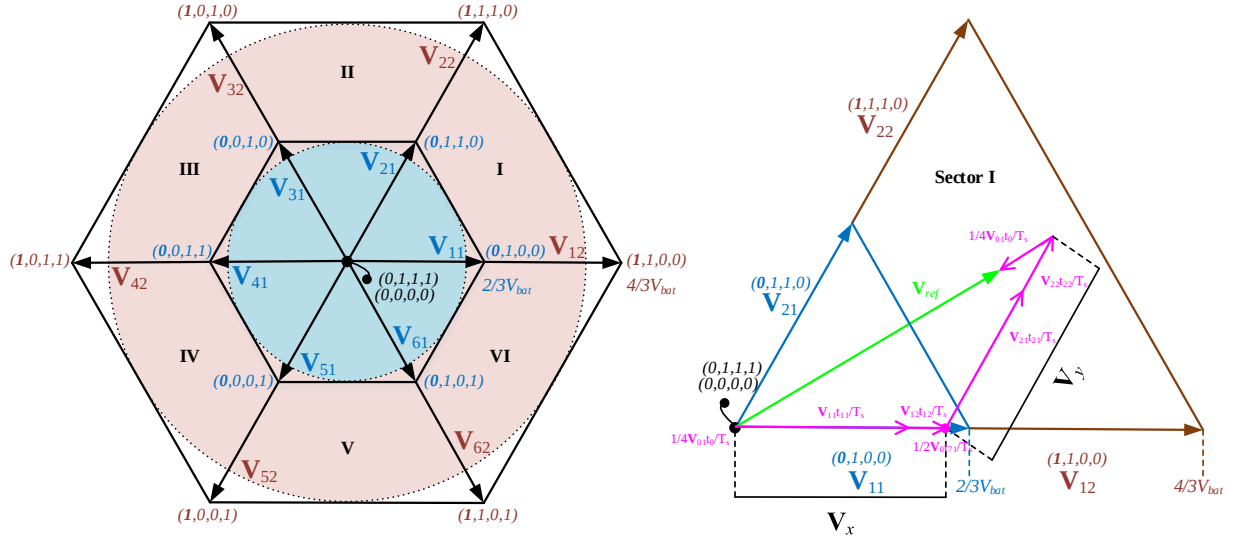


Figure 5.3 Space vector hexagon for SC converter with the annotated switching states in the order of (S_g, S_a, S_b, S_c) . The vector synthesis is a graphical representation of the algebraic summation and not the actual sequence in which the states are applied.

where

$$t_x = \sqrt{3}T_s M_i \sin\left(\frac{\pi}{3} - \theta\right) \quad (5.9)$$

and

$$t_{21} = (1 - A)t_y \quad (5.10)$$

$$t_{22} = At_y \quad (5.11)$$

where

$$t_y = \sqrt{3}T_s M_i \sin(\theta). \quad (5.12)$$

The factor $A \in [0, 1]$ is the boost factor and is expressed as follows:

$$A = \begin{cases} 0, & 0 \leq M_i \leq \frac{1}{\sqrt{3}} \\ \sqrt{3}M_i - 1, & \frac{1}{\sqrt{3}} < M_i \leq \frac{2}{\sqrt{3}} \end{cases} \quad (5.13)$$

where the modulation M_i is defined as

$$M_i = \frac{|\mathbf{V}_{ref}|}{V_{bat}}. \quad (5.14)$$

From this result, it is easy to see that when the modulation index $M_i \leq \frac{1}{\sqrt{3}}$, $t_{11} = t_x$, $t_{21} = t_y$ and $t_{12} = t_{22} = 0$. The capacitor is maintained in parallel with the dc source, and no discharge occurs at any time. The SC converter operation in this case is identical to the operation of a conventional two-level inverter. The authors refer to this operation mode as abstemious mode.

On the other hand, when $\frac{1}{\sqrt{3}} < M_i \leq \frac{2}{\sqrt{3}}$, then $0 < A \leq 1$, and the capacitor is charged and discharged with a rate proportional to the value of A . The authors refer to this operation mode as gluttonous mode.

When $M_i = \frac{2}{\sqrt{3}}$, $t_{11} = t_{21} = 0$, $t_{12} = t_x$, $t_{22} = t_y$. In this case, the capacitors are only charged during the zero vector implementation. Therefore, the six-step operation cannot be performed in the gluttonous mode, and the minimum zero vector time must be ensured to maintain the capacitor charge level.

The same rules in (5.9) and (5.12) can be applied for calculating the dwell times of the vectors in sectors II to VI if modified θ_k for the k th sector is used instead of θ used in the calculations.

$$\theta_k = \theta - (k - 1)\frac{\pi}{3}. \quad (5.15)$$

The space vector sequence should assure that the load line voltage has the quarter-wave symmetry to reduce the even harmonics in their spectra. To reduce the switching frequency, it is also necessary to execute the switching sequence in such a way that the transition from one to the next is performed by switching only one inverter leg at a time. For instance, if the reference vector falls in sector I, the switching sequence is shown in Fig. 5.4. The capacitor discharge intervals are placed in the middle of the active vectors intervals to maintain the switching of only one inverter leg at a time. The zero vector time is distributed at the beginning, the middle, and the end of the sampling period T_s . This placement has the particular advantage of limiting the capacitor charging

current as we show in the following sections.

5.3 Analysis of the Capacitor Voltage Ripple and the Charging Current Using SVPWM

The capacitor connection with the source and inverter falls into one of the following two configurations: the pre-discharge state and the discharge state. In the pre-discharge state as shown in Fig. 5.2(a), the capacitor is charged with voltage equal to

$$V_{cap} = V_{bat} - (V_D + V_p) = V_{dc} \quad (5.16)$$

where V_D is the forward voltage drop across the diode. V_p refers to the summation of the parasitic voltages drop along the charging path, including the voltage drop across the series resistance of the capacitor and the on-resistance of the switch. For simplicity's sake, we will refer to the fully charged capacitor as V_{dc} , where $V_{dc} \approx V_{bat}$.

In the discharge state, the capacitor is discharged to the load as shown in Fig. 5.2(b). During this time, the capacitor is connected in series with the source and the load. Therefore,

$$i_{cap} = i_s = i_i = S_a i_a + S_b i_b + S_c i_c. \quad (5.17)$$

The voltage drop in the capacitor voltage is a function of the capacitor size and the discharge time,

$$\Delta v_{cap} = \frac{i_{cap} t_{dch}}{C}, \quad (5.18)$$

where t_{dch} is the discharge time. During the discharge time the capacitor becomes in series with the source, $i_{cap} = i_i$, and

$$\Delta v_{cap} = v_{cap}(k) - v_{cap}(k+1) = \frac{i_i t_{dch}}{C}, \quad (5.19)$$

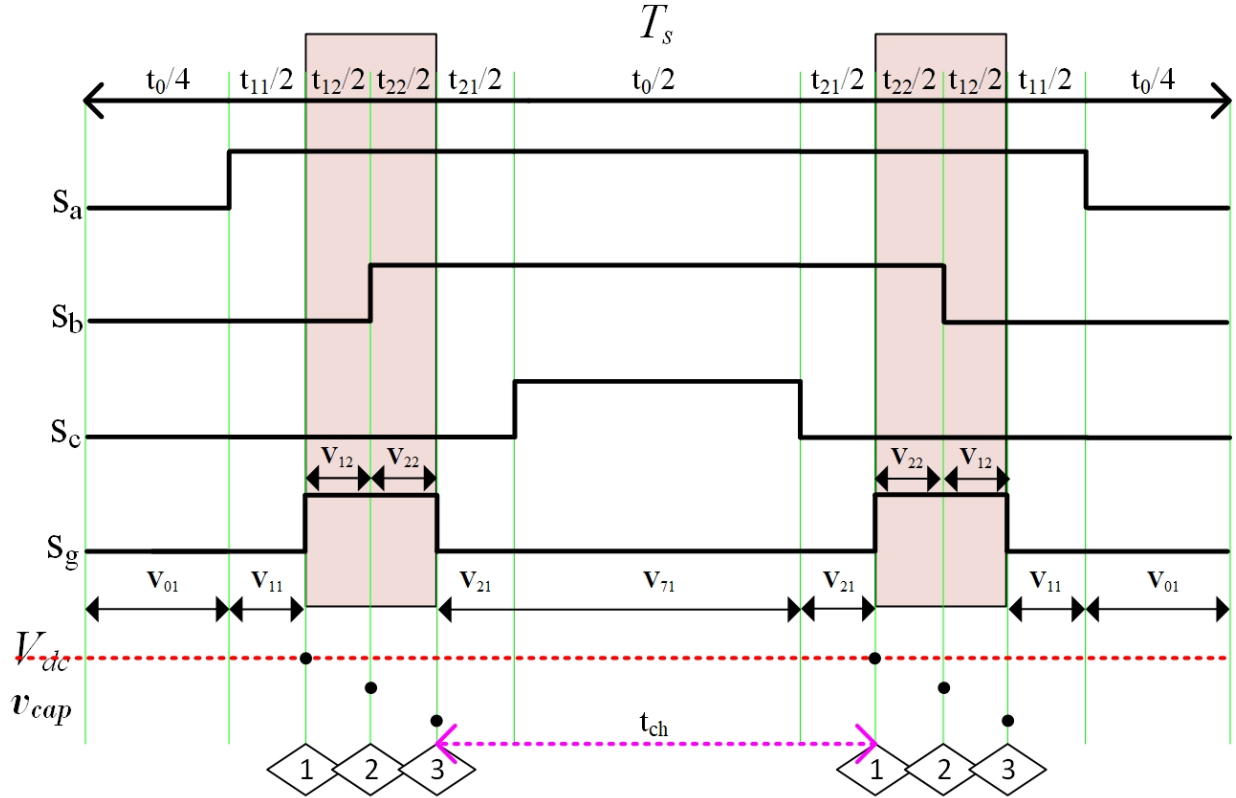


Figure 5.4 Illustration of the switching sequence of SVPWM in sector I.

To estimate the charging current of the capacitor, we must consider the sequence in which the capacitor is charged and discharged with respect to the inverter states.

Consider the switching sequence in Fig. 5.4. The capacitor is discharged in two separate intervals per sampling time T_s . The first interval produces V_{12} and V_{22} and the second interval produces V_{22} and V_{12} . First, we assume that equation (5.16) holds, and therefore, before every discharge state, $v_{cap(1)} = V_{dc}$. Using (5.19), the capacitor voltage at point 2 $v_{cap(2)}$ can be predicted as follows:

$$v_{cap2} = V_{dc} - \frac{i_a t_{12}}{2C}. \quad (5.20)$$

Similarly, the capacitor voltage at point 3 v_{cap3} can be expressed as

$$v_{cap3} = V_{dc} - \frac{i_a A t_x}{2C} + \frac{i_c A t_y}{2C}. \quad (5.21)$$

Note that

$$\begin{aligned} i_a &= I_a \cos(\theta - \phi) \\ i_b &= I_b \cos(\theta - \phi + \frac{2\pi}{3}) \\ i_c &= I_c \cos(\theta - \phi - \frac{2\pi}{3}) \end{aligned} \quad (5.22)$$

where i_a , i_b and i_c are phase shifted from the reference voltage by ϕ , which is the power factor angle. $I_a = I_b = I_c = I$ are the phase currents amplitudes. Note that t_x and t_y are functions of the modulation index M_i and the angle θ as expressed in (5.9) and (5.12), respectively.

For any assigned value of the modulation index, the capacitor voltage drop in the first discharge interval shown in Fig. 5.4 is

$$\Delta V = V_{dc} - v_{cap3} = \frac{A}{2C} \left(t_x i_a - t_y i_c \right) \quad (5.23)$$

and the maximum value of ΔV (ΔV_{max}) can be obtained by taking the gradient of (5.23) with respect to θ ,

$$\frac{\partial \Delta V}{\partial \theta} = \frac{\sqrt{3} M_i T_s I}{C} \left(\cos(2\theta - \phi - \frac{\pi}{3}) + \cos(2\theta - \phi - \frac{2\pi}{3}) \right). \quad (5.24)$$

Note that there exists an angle $\hat{\theta} \in \{0, \frac{\pi}{3}\}$ that causes maximum ΔV and makes the gradient equal zero

$$\frac{\partial \Delta V}{\partial \theta} = 0 = \cos(2\hat{\theta} - \phi - \frac{\pi}{3}) + \cos(2\hat{\theta} - \phi - \frac{2\pi}{3}). \quad (5.25)$$

By using the following identity

$$\cos(x - y) + \cos(x + y) = 2 \cos(x) \cos(y), \quad (5.26)$$

equation (5.25) can be expressed as

$$\cos(2\hat{\theta} - \phi - \frac{\pi}{2} + \frac{\pi}{6}) + \cos(2\hat{\theta} - \phi - \frac{\pi}{2} - \frac{\pi}{6}) = 2 \cos(2\hat{\theta} - \phi - \frac{\pi}{2}) \cos(\pi/6). \quad (5.27)$$

Obviously, $\cos(\pi/6) \neq 0$; therefore, $\cos(2\theta - \phi - \frac{\pi}{2}) = 0$. This leads to the following conditions:

$$\begin{aligned} 2\hat{\theta} - \phi - \frac{\pi}{2} &= \frac{\pi}{2} \\ 2\hat{\theta} - \phi - \frac{\pi}{2} &= -\frac{\pi}{2}, \end{aligned} \quad (5.28)$$

and θ that causes maximum ΔV is one of the two solutions

$$\hat{\theta} = \begin{cases} \frac{\pi+\phi}{2}, & 0 > \phi \geq -\frac{\pi}{2} \\ \frac{\phi}{2}, & 0 \leq \phi \leq \frac{\pi}{2}. \end{cases} \quad (5.29)$$

The formulation of the angle $\hat{\theta}$ gives the insight that for any power factor PF from 0 to 1, the angle that causes maximum ΔV always lies between 0° and 45° of sector I.

The maximum voltage drop using the pattern in Fig. 5.4 can be expressed as

$$\begin{aligned} \Delta V|_{\theta=\frac{\phi}{2}} &= \Delta V_{max} = \frac{A}{2C} \left(t_x i_a - t_y i_c \right) \\ &= \frac{A}{2C} \sqrt{3} T_s M_i I \left[\sin\left(\frac{\pi}{3} - \frac{\phi}{2}\right) \cos\left(\frac{\phi}{2}\right) - \sin\left(\frac{\phi}{2}\right) \cos\left(\frac{\phi}{2} - \phi - \frac{2\pi}{3}\right) \right]. \end{aligned} \quad (5.30)$$

So far it has been shown that the maximum voltage drop location within the sector is solely dependent on the power factor PF of the load. However, the power factor PF does not affect the value of the maximum voltage drop ΔV_{max} as shown in Fig. 5.5. As a consequence, the final expression of ΔV_{max} can be described in the following compact form:

$$\Delta V_{max} = \frac{3AM_i I}{4C f_{sw}}. \quad (5.31)$$

To complete the analysis, we must make sure that the capacitor reaches $\approx V_{dc}$ voltage during the charging time. This can be understood by obtaining the minimum charging time location within the sector and its value dependency. Consider t_{ch} indicated in Fig. 5.4. The charging time t_{ch} is a function of M_i and A :

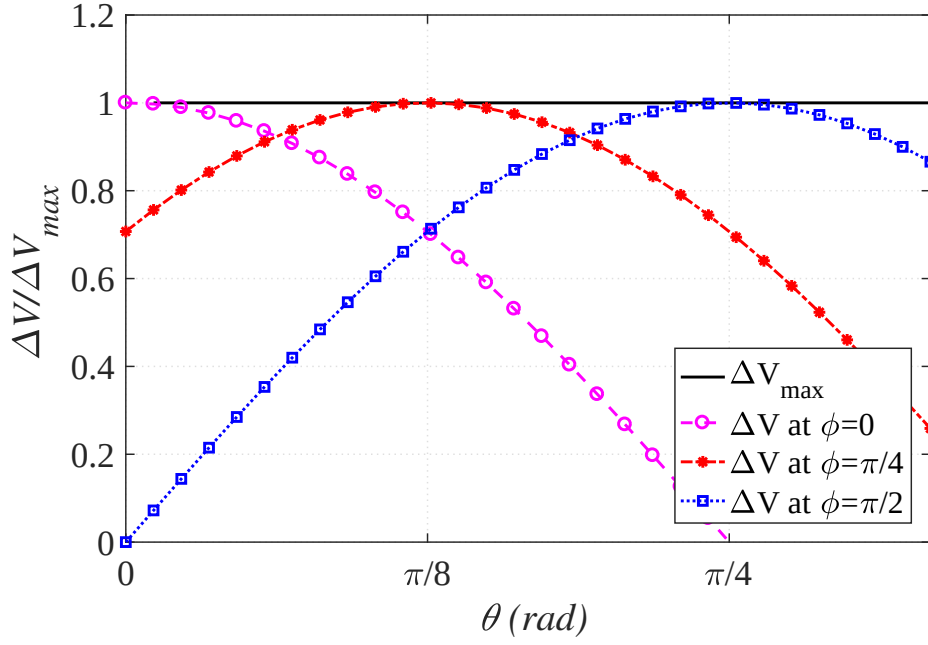


Figure 5.5 The relationship between the location of ΔV_{max} and the power factor angle ϕ . ϕ does not change the value of ΔV_{max} ; it only changes the location within the sector in which ΔV_{max} occurs.

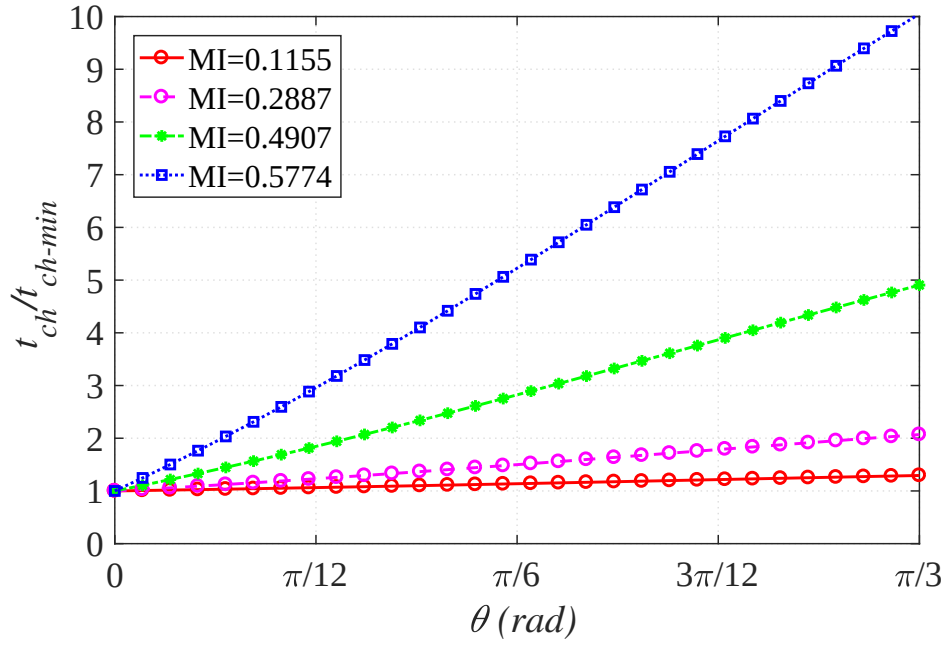


Figure 5.6 The charging time t_{ch} with respect to the minimum charging time t_{ch-min} with different values of M_i , $A = 0.3$.

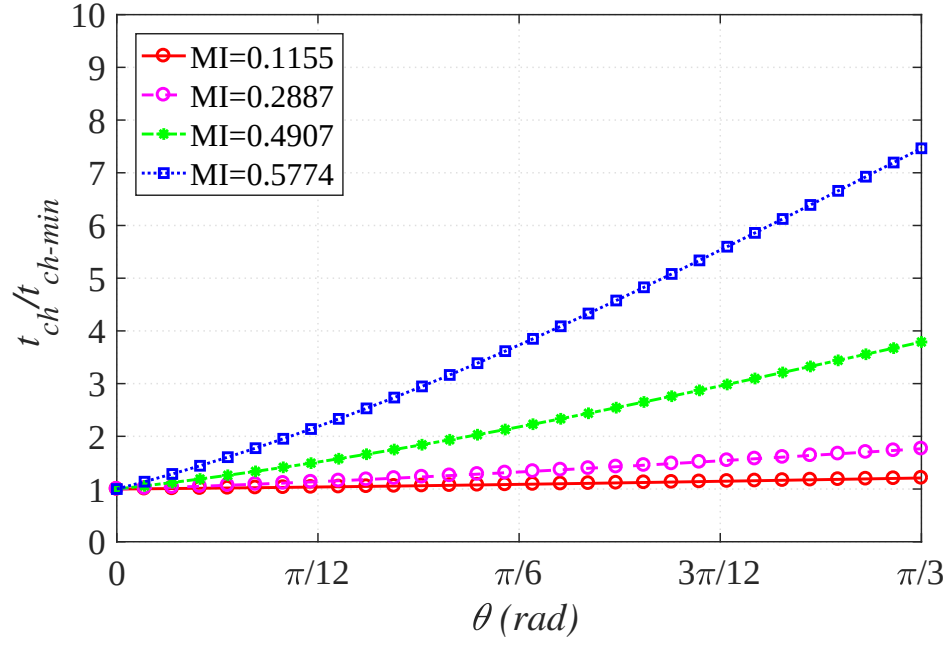


Figure 5.7 The charging time t_{ch} with respect to the minimum charging time t_{ch-min} with different values of M_i , $A = 0.5$.

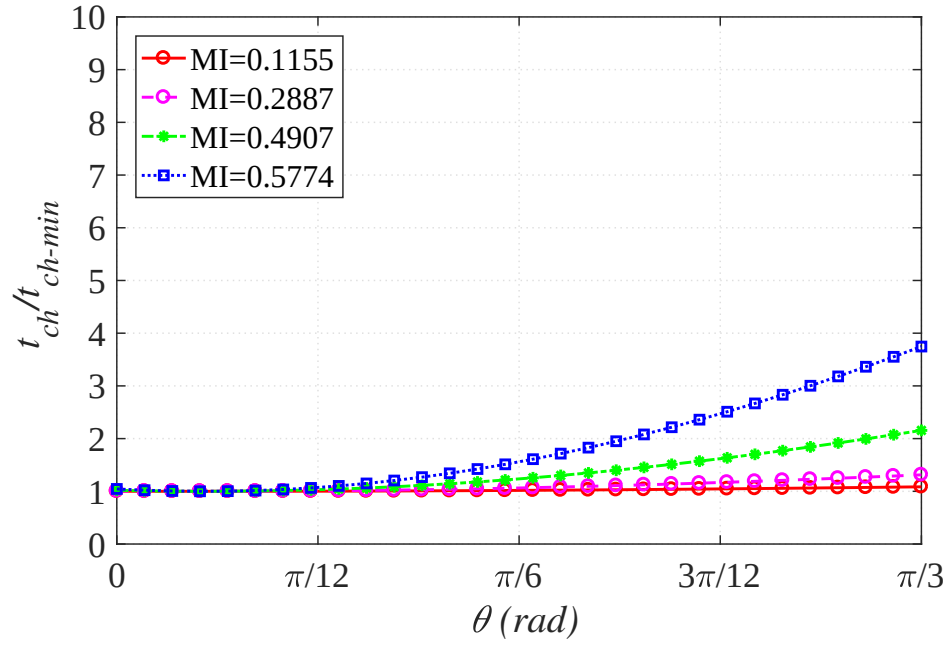


Figure 5.8 The charging time t_{ch} with respect to the minimum charging time t_{ch-min} with different values of M_i , $A = 0.8$.

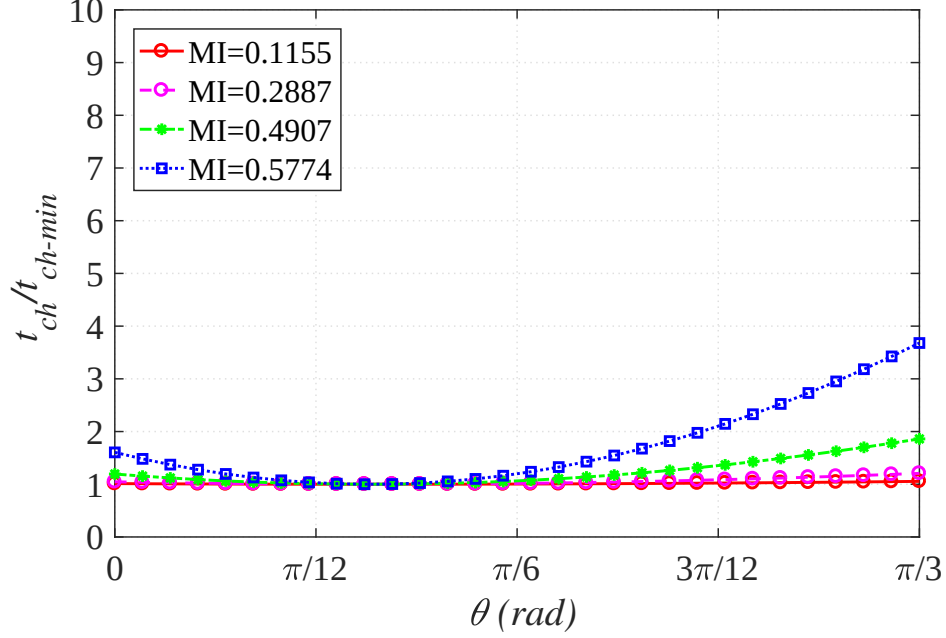


Figure 5.9 The charging time t_{ch} with respect to the minimum charging time t_{ch-min} with different values of M_i , $A = 0.9$.

$$\begin{aligned}
 t_{ch} &= \frac{t_0}{2} + (1 - A)t_y \\
 &= \frac{T_s}{2} - \sqrt{3}T_s M_i \left[\frac{1}{2} \sin\left(\frac{\pi}{3} - \theta\right) - \left(\frac{1}{2} - A\right) \sin(\theta) \right].
 \end{aligned} \tag{5.32}$$

Taking the gradient for (5.32) and equating it to zero results in the angle $\hat{\theta}$ at which the minimum charging time is experienced t_{ch-min}

$$\frac{\partial t_{ch}}{\partial \theta} = 0 = \cos\left(\frac{\pi}{3} - \hat{\theta}\right) - \left(A - \frac{1}{2}\right) \cos(\hat{\theta}). \tag{5.33}$$

The optimal angle is determined to be

$$\hat{\theta} = \tan^{-1} \left(\frac{4A - 3}{\sqrt{3}} \right). \tag{5.34}$$

Note that the angle $\hat{\theta}$ lies in sector I only when $\frac{3}{4} \leq A \leq 1$. When $0 \leq A < \frac{3}{4}$, the resulting angle is negative, and it does not reside in sector I. However, a small segment of a sinusoidal

function has a linear behavior. It is observed that $\hat{\theta} = 0$ when $0 \leq A < \frac{3}{4}$. Therefore, the general description for $\hat{\theta}$ is

$$\hat{\theta} = \begin{cases} 0, & 0 \leq A < \frac{3}{4} \\ \tan^{-1}\left(\frac{4A-3}{\sqrt{3}}\right), & \frac{3}{4} \leq A \leq 1. \end{cases} \quad (5.35)$$

As a result, the minimum charging time t_{ch-min} is expressed as follows:

$$t_{ch-min} = \begin{cases} \frac{1}{2}T_s(1 - \frac{3}{2}M_i), & 0 \leq A < \frac{3}{4} \\ \frac{T_s}{2} - \sqrt{3}T_sM_i \\ \left[\frac{1}{2} \sin\left(\frac{\pi}{3} - \tan^{-1}\left(\frac{4A-3}{\sqrt{3}}\right)\right) - \right. \\ \left. \left(\frac{1}{2} - A\right) \sin\left(\tan^{-1}\left(\frac{4A-3}{\sqrt{3}}\right)\right) \right], & \frac{3}{4} \leq A \leq 1. \end{cases} \quad (5.36)$$

Because of the symmetry of the sector, the other charging intervals have a similar expression for t_{ch-min} . In order for the capacitor to retain the full voltage after each charging period, the following condition must be met:

$$t_{ch-min} \geq RC \ln\left(\frac{V_{dc} - V_{cap}}{\frac{3}{4C}AT_sM_iI}\right). \quad (5.37)$$

Under these conditions, the maximum charging current amplitude passing through the diode of S_R and the IGBT of $\tilde{S}_g$ can be estimated as:

$$I_{charging-max} = \frac{3AM_iI}{4RCf_{sw}} \quad (5.38)$$

where R is the resistance along the charging path including the on-resistance of the switches and the ESR of the switched-capacitor. The power losses resulting from the additional resistance must be very small and can be estimated as follow:

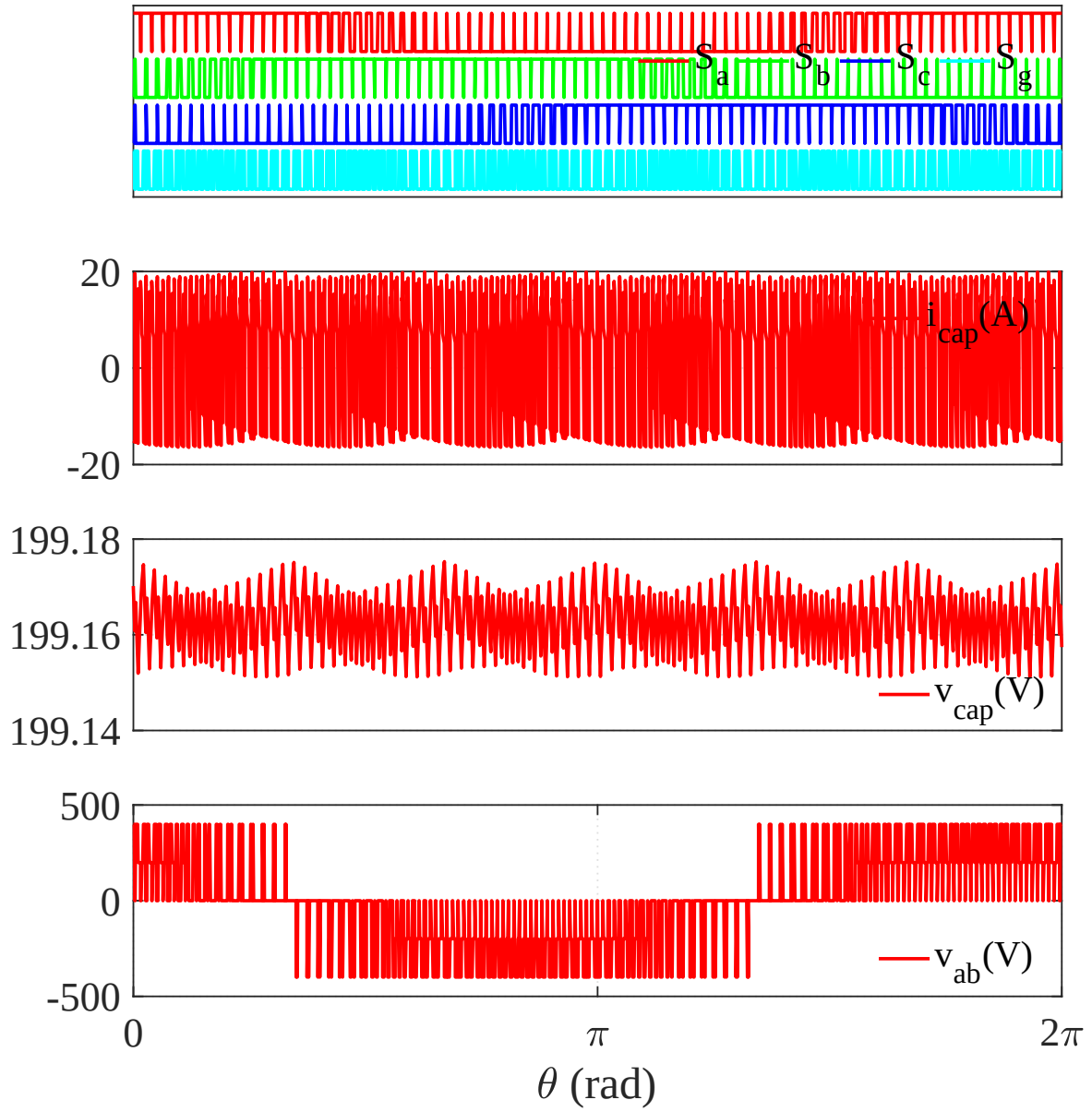


Figure 5.10 Simulation results of one fundamental cycle showing the behavior of the charging current i_{cap} with respect to the instantaneous voltage drop across the capacitor v_{cap} .

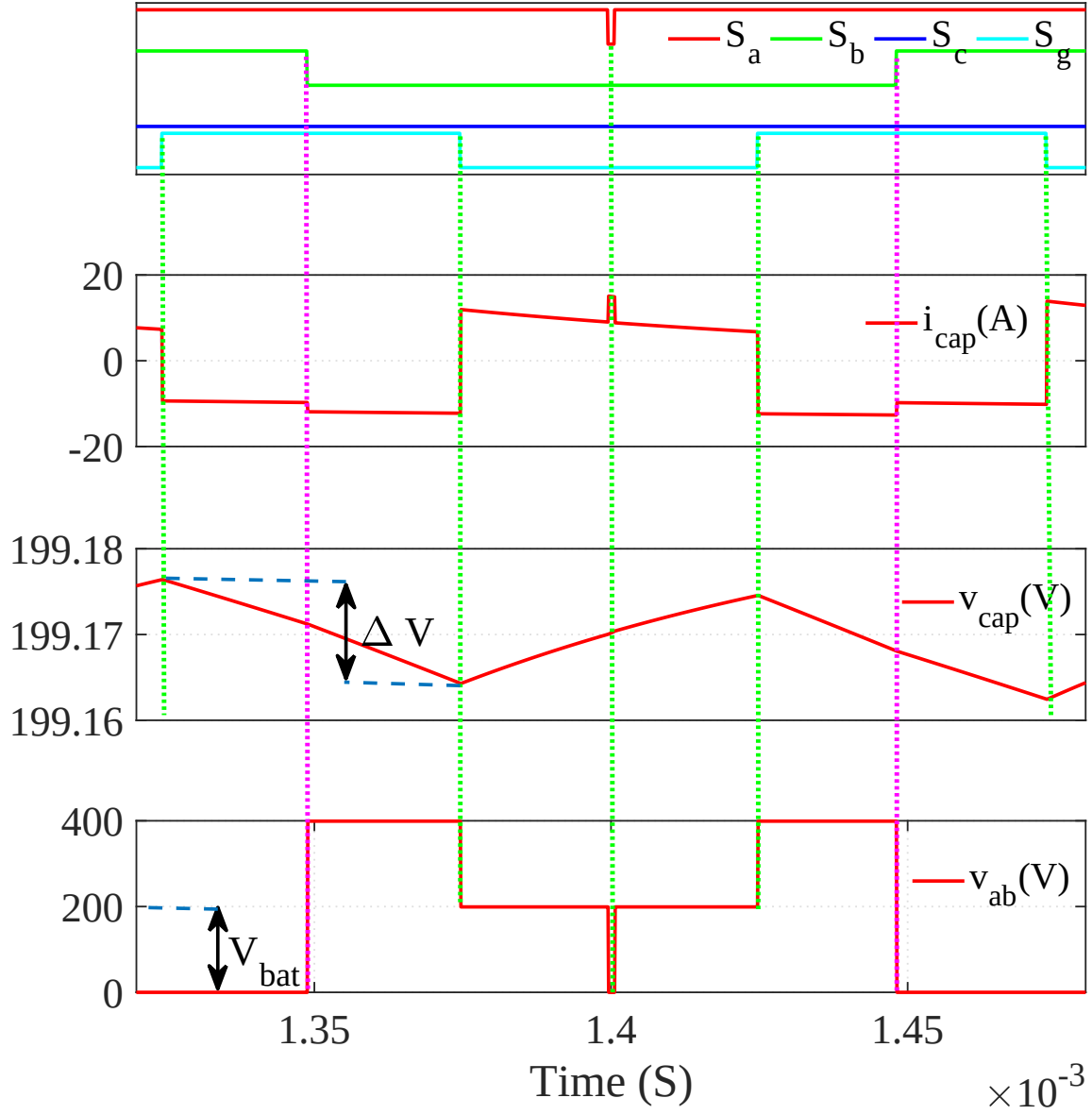


Figure 5.11 (Zoom in of Fig. 5.10); Simulation results of the charging current showing that when the $\Delta V \approx 0.02$ V the charging current $i_{cap} = \frac{\Delta V}{R} \approx 18$ A; given that the series resistance in the simulation model is set to $R = 0.0011 \Omega$.

$$P_{R-losses} = \frac{1}{R} \left(\frac{3AM_i I}{4Cf_{sw}} \right)^2. \quad (5.39)$$

The presented guidelines allow better understanding of the charging current and how the selection of the switching frequency, the capacitor size, M_i , and A will determine the current rating of the switched-capacitor half-bridge. Fig. 5.6 to Fig. 5.9 show the normalized charging time in different values of M_i and A . Note that the expressions of ΔV_{max} and t_{ch-min} for the second t_{ch} interval is the mirror image of the one shown in Fig. 5.6 to Fig. 5.9.

Fig. 5.10 shows the simulation results of one fundamental cycle. The capacitor voltage v_{cap} experiences the maximum voltage drop ΔV_{max} when the angle within the sector is near 10° when the power factor of the load is 0.93. This observation is well supporting the analytic analysis of the of the maximum voltage drop location within the sector shown in Fig. 5.5.

Fig. 5.11 shows a zoom-in of Fig. 5.10 to one sampling period. As it can be seen, the charging current is a function of the voltage drop across the capacitor in the previous discharging event and the series resistance of the charging path. The total on-resistance of the diode and the lower switch is set to 0.0011Ω . Increasing the series resistance will limit the charging current, but it will also lead to an increase in conduction losses. Therefore, the viable solution to limit the charging current is to limit the voltage drop occurring in the discharge period. This can be done by either increasing the switching frequency or increasing the capacitor size or both as indicated by (5.31).

5.4 Carrier-based Modulation of SC Converter

The generation of the switching function for the SC converter can be further simplified by adopting the carrier-based method. The carrier-based method gives the exact switching sequence obtained by the SVPWM. In fact, the carrier waveforms are directly derived from the dwell times developed in Section II. To generate the switching signals, five modulation waveforms are derived from the dwell times. The first three v_a^* , v_b^* , and v_c^* are used to modulate the three phase legs of the inverter a , b , and c , respectively, and it is dependent on M_i . The last two are used to modulate

Table 5.1 The generation of the reference waveforms from the dwell times in each sector.

Sector	v_a^*	v_b^*	v_c^*	v_l^*	v_h^*
I	$t_x + t_y + \frac{t_0}{2}$	$t_y + \frac{t_0}{2}$	$\frac{t_0}{2}$	$t_{11} + \frac{t_0}{2}$	$t_x + t_{22} + \frac{t_0}{2}$
II	$t_x + \frac{t_0}{2}$	$t_x + t_y + \frac{t_0}{2}$	$\frac{t_0}{2}$	$t_{21} + \frac{t_0}{2}$	$t_y + t_{12} + \frac{t_0}{2}$
III	$\frac{t_0}{2}$	$t_x + t_y + \frac{t_0}{2}$	$t_y + \frac{t_0}{2}$	$t_{11} + \frac{t_0}{2}$	$t_x + t_{22} + \frac{t_0}{2}$
IV	$\frac{t_0}{2}$	$t_x + \frac{t_0}{2}$	$t_x + t_y + \frac{t_0}{2}$	$t_{21} + \frac{t_0}{2}$	$t_y + t_{12} + \frac{t_0}{2}$
V	$t_y + \frac{t_0}{2}$	$\frac{t_0}{2}$	$t_x + t_y + \frac{t_0}{2}$	$t_{11} + \frac{t_0}{2}$	$t_x + t_{22} + \frac{t_0}{2}$
VI	$t_x + t_y + \frac{t_0}{2}$	$\frac{t_0}{2}$	$t_x + \frac{t_0}{2}$	$t_{21} + \frac{t_0}{2}$	$t_y + t_{12} + \frac{t_0}{2}$

the switching capacitor leg, and it is dependent on both M_i and A . The equations to obtain those reference waveforms are listed in Table 5.1.

Fig. 5.12 to Fig. 5.15 show how the reference signals behave as A changes from 0 to 0.75, where M_i in the figures is maximum (0.5774). If M_i is reduced, then the envelope of v_a^* , v_b^* , and v_c^* will be reduced with the same shape being maintained. After calculating the five reference waveforms, the simplified control diagram shown in Fig. 5.16 can be used to generate the switching signals. The reference waveform can be either calculated or stored in a sine look-up table for minimum computational effort. In our case, the logic block diagram shown in Fig. 5.16 is implemented using an FPGA.

5.5 Simulation Results, Experimental Test, and Hardware Design

To verify the proposed design equation and control, a simulation model of the SC converter is built using Saber RD simulation software. Fig. 5.1(b) shows the circuit configuration and Fig. 5.17 and 5.18 show the simulation waveform in various operating regions. The battery voltage is set to 200 V. RL load is used with $R_{load} = 10 \Omega$ and $L = 10$ mH. The switching frequency of the inverter legs is set to 10 kHz, and the switching frequency of the SC leg is set to 20kHz. The switched-capacitor is 9000 μ F. The total series resistance along the charging path shown in Fig 5.2(a) is

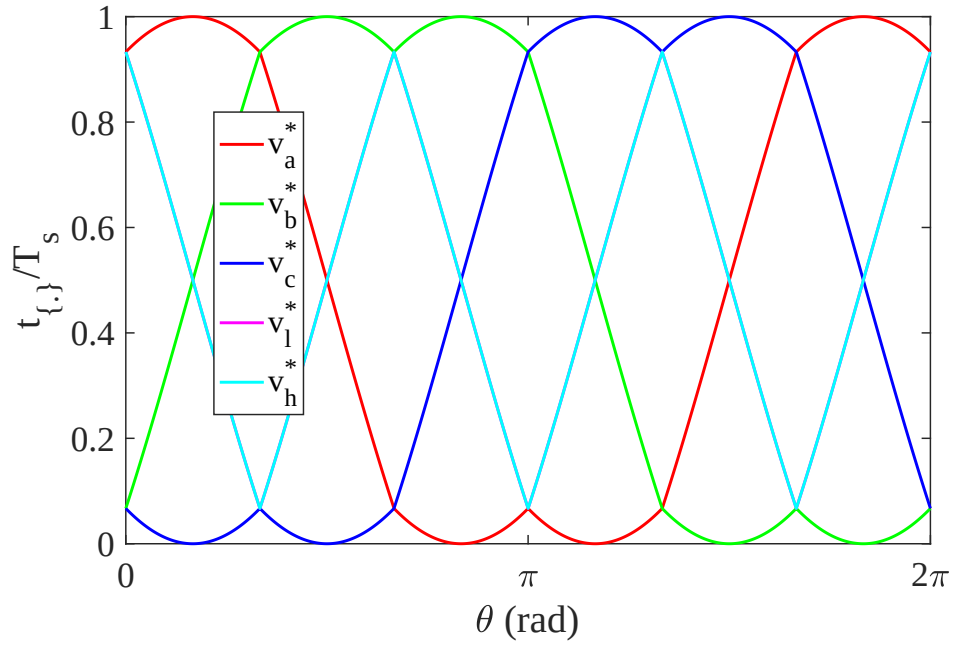


Figure 5.12 The reference waveforms synthesized from the SVPWM algorithm, $M_i = 0.5774$, $A = 0$.

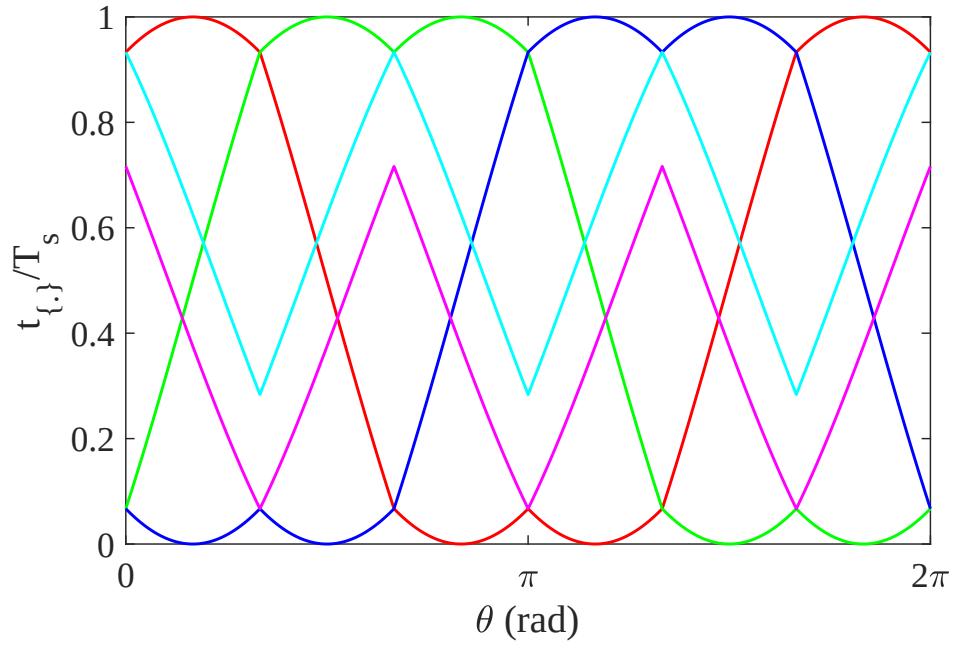


Figure 5.13 The reference waveforms synthesized from the SVPWM algorithm, $M_i = 0.5774$, $A = 0.25$.

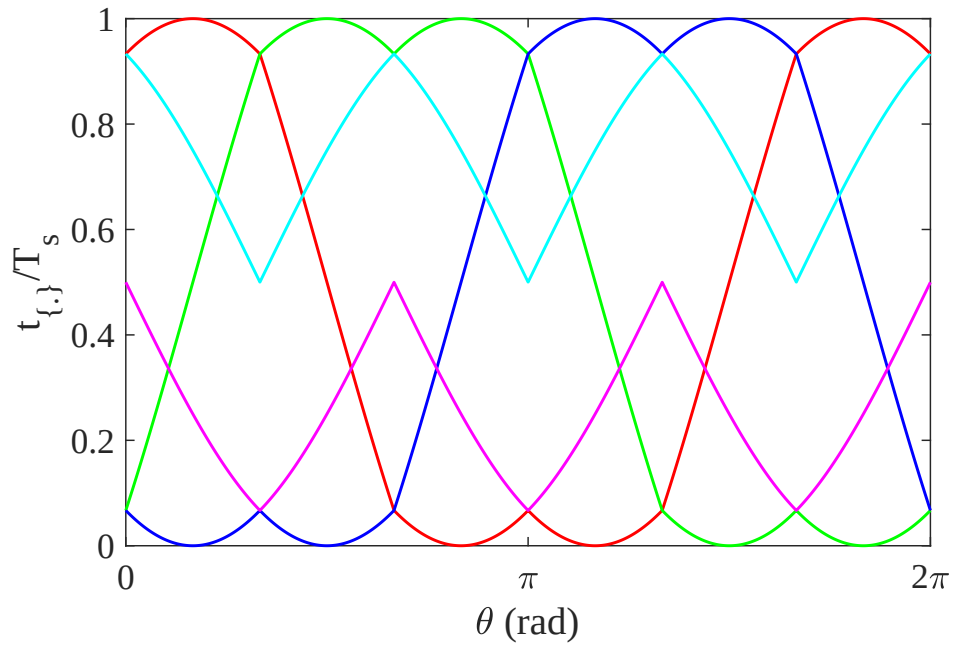


Figure 5.14 The reference waveforms synthesized from the SVPWM algorithm, $M_i = 0.5774$, $A = 0.5$.

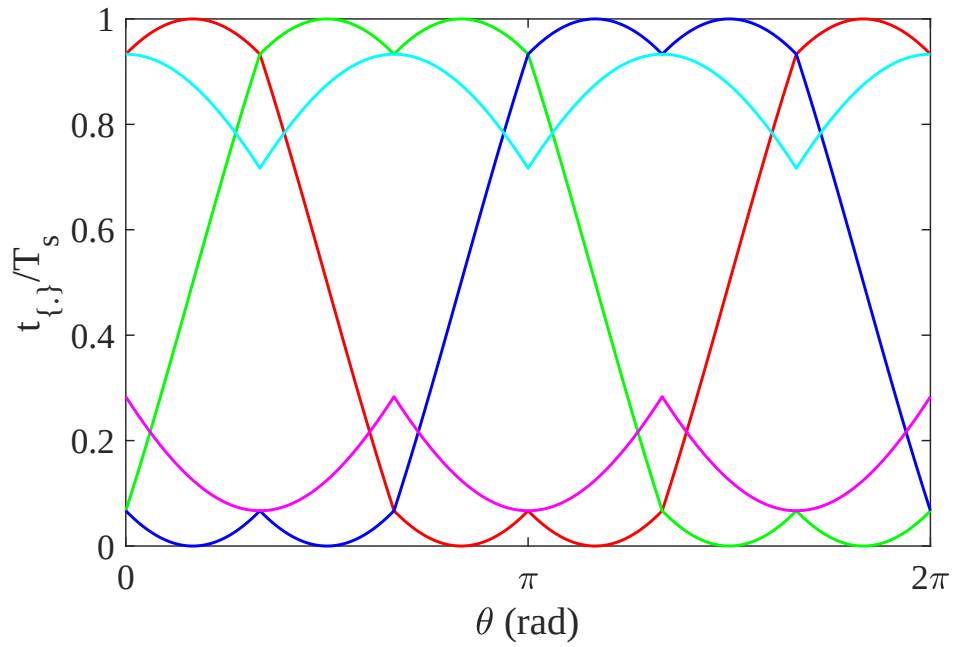


Figure 5.15 The reference waveforms synthesized from the SVPWM algorithm, $M_i = 0.5774$, $A = 0.75$.

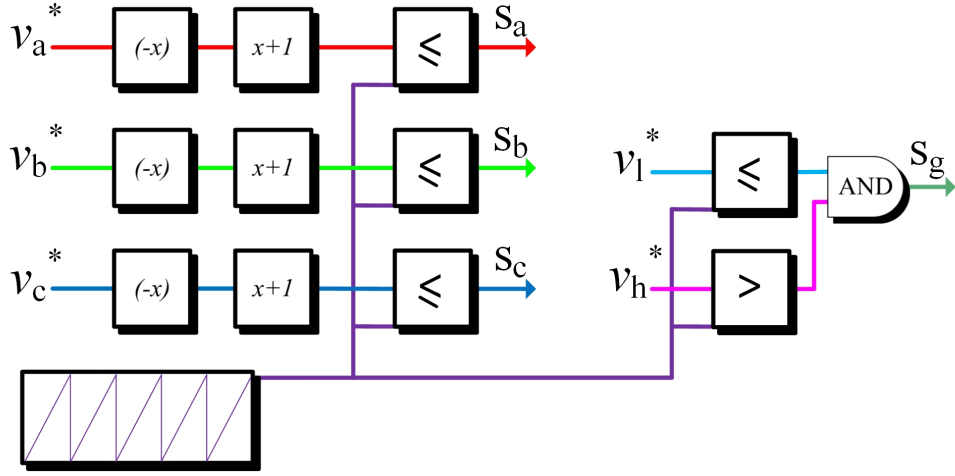


Figure 5.16 The carrier-based modulation of the SC converter.

0.25Ω , which serves to limit the charging current of the capacitor.

Fig. 5.17 shows the result when $M_i = 0.5$ and $A = 0$. The converter is operating in the abstemious mode, and the operation is identical to the one of two-level VSI. The diode in S_R and the IGBT in $\tilde{S}_g$ experience continuous conduction. However, the current flowing through the IGBT in $\tilde{S}_g$ is negligible in the steady-state operation, and it does not contribute to increasing the conduction losses. Fig. 5.18 shows the simulation results when $A = 0.5$ $M_i = 0.5$. The converter is operating in the gluttonous mode. The capacitor voltage is fluctuating between 200 V and 400 V during the charging and discharging intervals, respectively.

In the abstemious mode, the inverter switches have voltage stress equal V_{dc} instead of $2V_{dc}$, a feature that is unavailable to inverters with non-adjustable dc-link voltage. For instance, if the conventional VSI is fed by 400 V dc-link voltage, then the voltage stress across the switches is always 400 V regardless of the value of the MI . Whereas an equivalent system of SC converter will have a dc-link voltage equal to 200 V and the voltage stress across the switches during all of the abstemious mode is only 200. The voltage stress becomes 400 V only when the inverter is operating in the gluttonous region. This cut the voltage stress of the switches to half in half of the operating region of the SC converter. Furthermore, the PWM operation under very low modulation index presents maximum total harmonic distortion (THD). Therefore, by operating

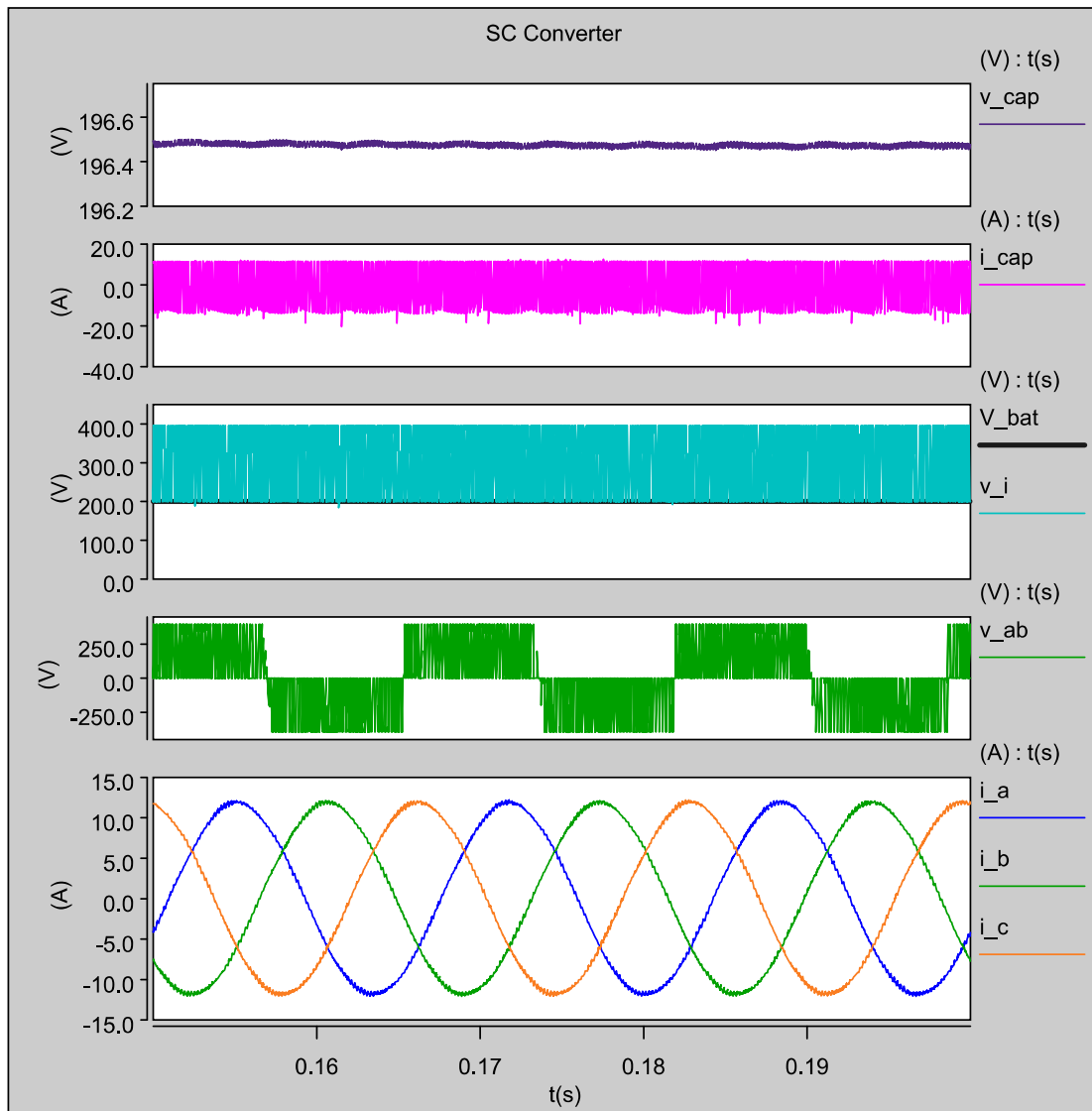


Figure 5.17 The carrier-based modulation of the SC converter. Abstemious mode, $M_i = 0.5$ and $A = 0$.

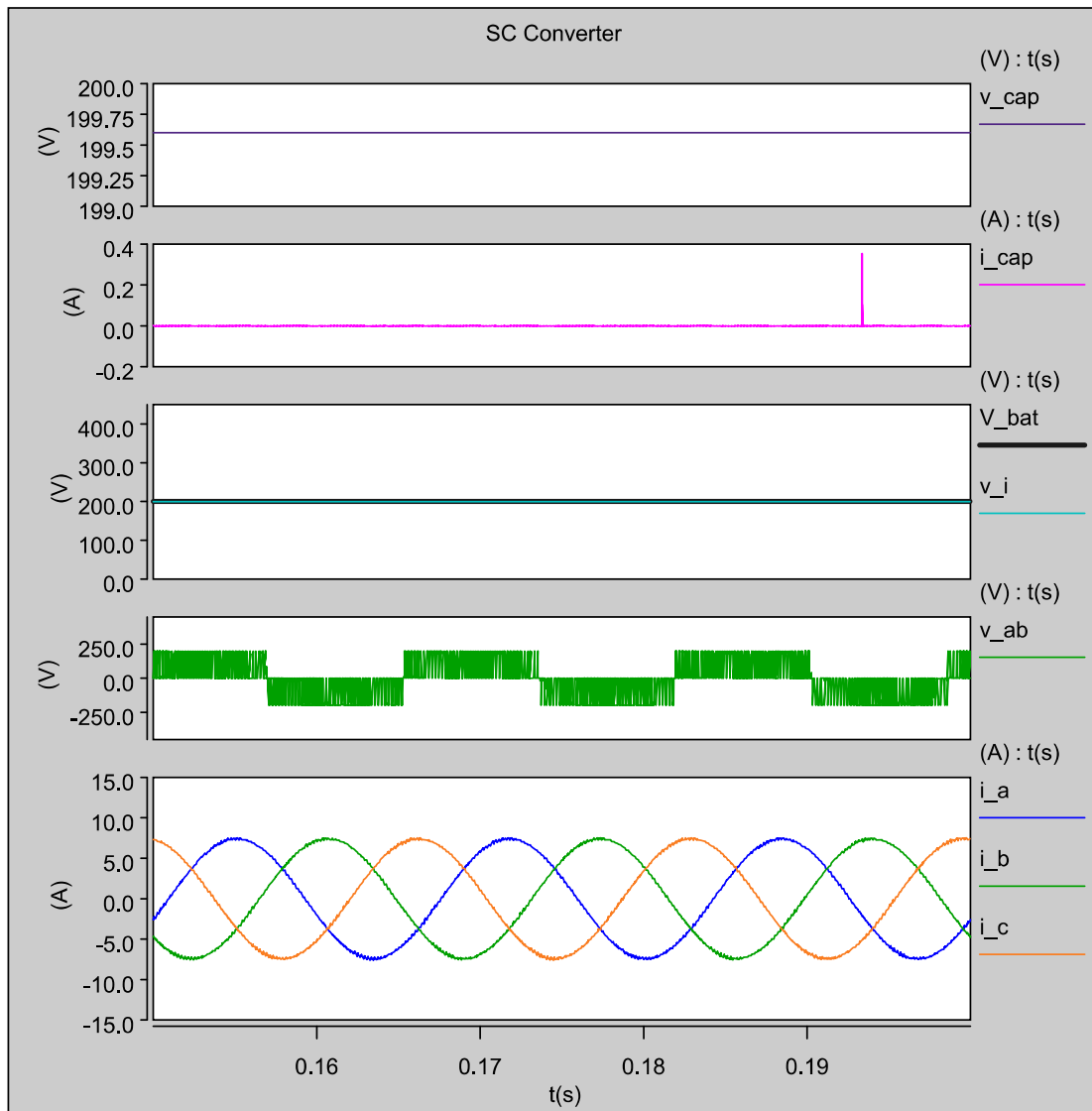


Figure 5.18 The carrier-based modulation of the SC converter. Gluttonous mode, $M_i = 0.5$ and $A = 0.5$.

in the abstemious mode, the converter M_i remains at the higher area of the linear region and the reduction in THD can reach 60% lower than the THD of an equivalent fixed dc-link inverter system. The experimental results show that the THD of the SC converter is within less than 3% across the entire operating region. Fig. 5.19 Fig. 5.20 show the dc-link design of the SC converter. Note that laminated copper strips can be used instead of the narrow strips to further minimize the loop inductance.

Fig. 5.21 shows the experimental prototype. Fig. 5.23 shows the experimental results when the battery voltage is 100V, the maximum dc-link voltage seen by the inverter bridge is 200 V, the operating switching frequency is set to 10 kHz, the switched-capacitor used is 9000 μ F. In Fig. 5.22, $M_i = 0.5774$, and $A = 0$. The converter in this case is operating in the abstemious mode. The switched capacitor becomes in parallel with the dc-link capacitor and the current flowing through the IGBT in $\tilde{S}_g$ is near zero.

Fig. 5.24 Fig. 5.25 show the experimental results when the battery voltage is raised to 200 V, the dc-link voltage seen by the inverter bridge is 400V, the operating switching frequency is set to 20 kHz, $M_i = 0.5$, and $A = 0.5$.

Fig. 5.26 shows the experimental results focusing on the switching transient of the charging current and the output line voltage. The top image shows the switching function sent by the FPGA. It is essential to know that the charging current is dangerous only at the charging period, right when S_g turns off. The negative peaks of the charging current occur when the capacitor is in a series configuration with the input battery source. In this case, the capacitor current is equal to the inverter input current.

Fig. 5.27 shows the load current waveform when the switching frequency of the converter is only 1 kHz. Thanks to the large size of the switched-capacitor, the charging current is still within the design limit of the converter. The significance of being able to operate at low switching frequency is to achieve high efficiency or the possibility of implementing low-frequency optimal PWM.

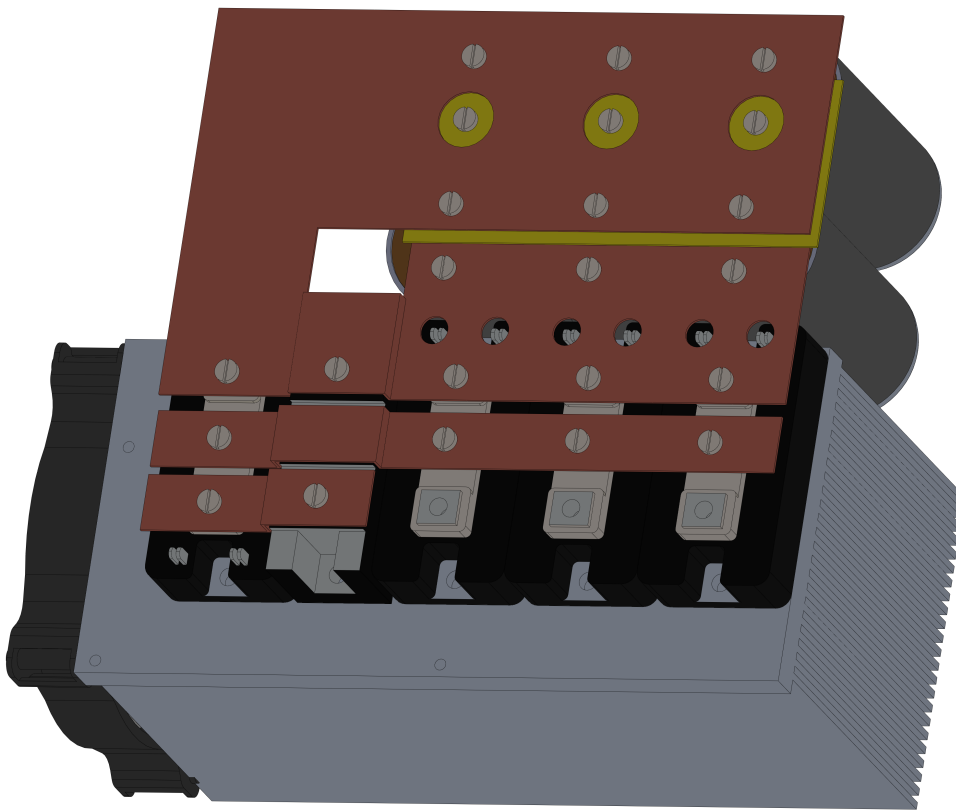


Figure 5.19 Isometric view of the SC converter layout.

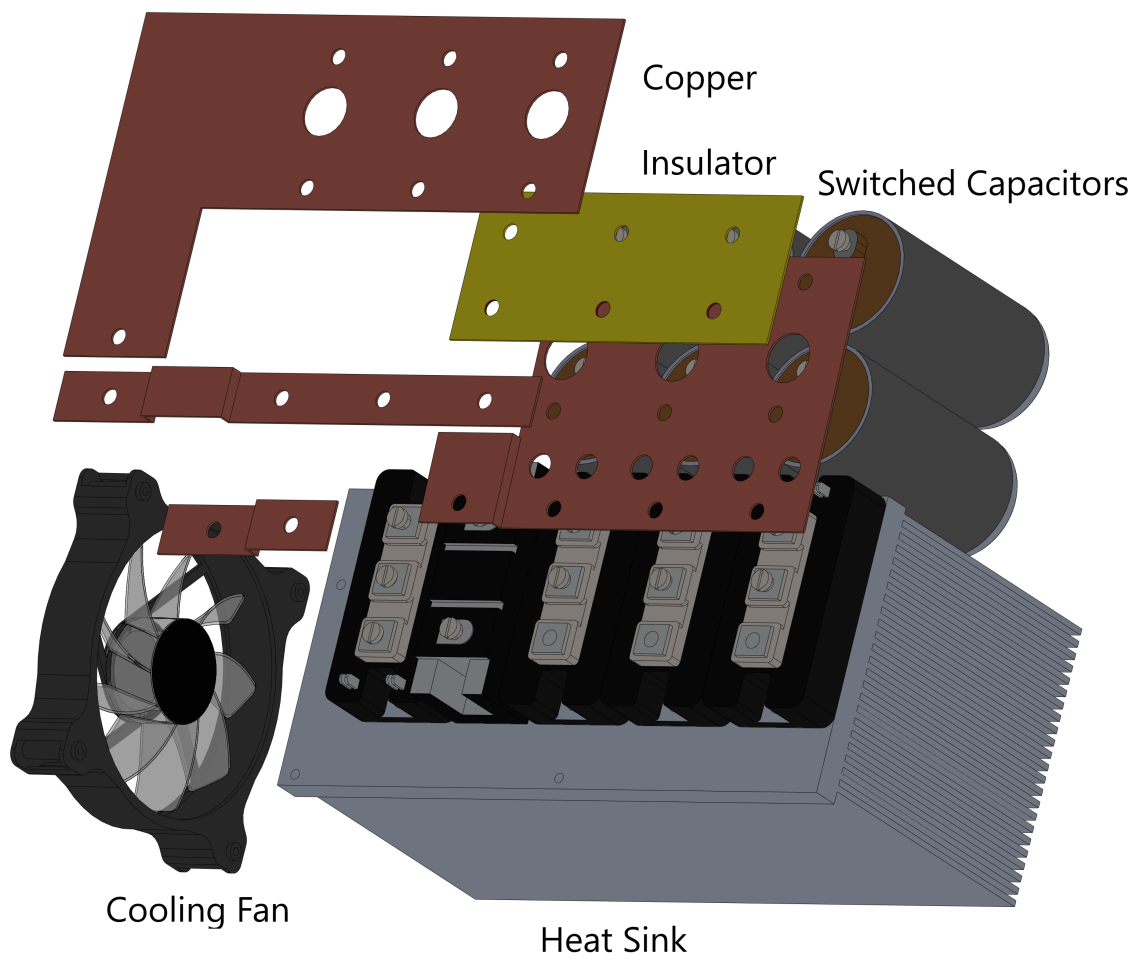


Figure 5.20 Exploded view of the SC converter layout.

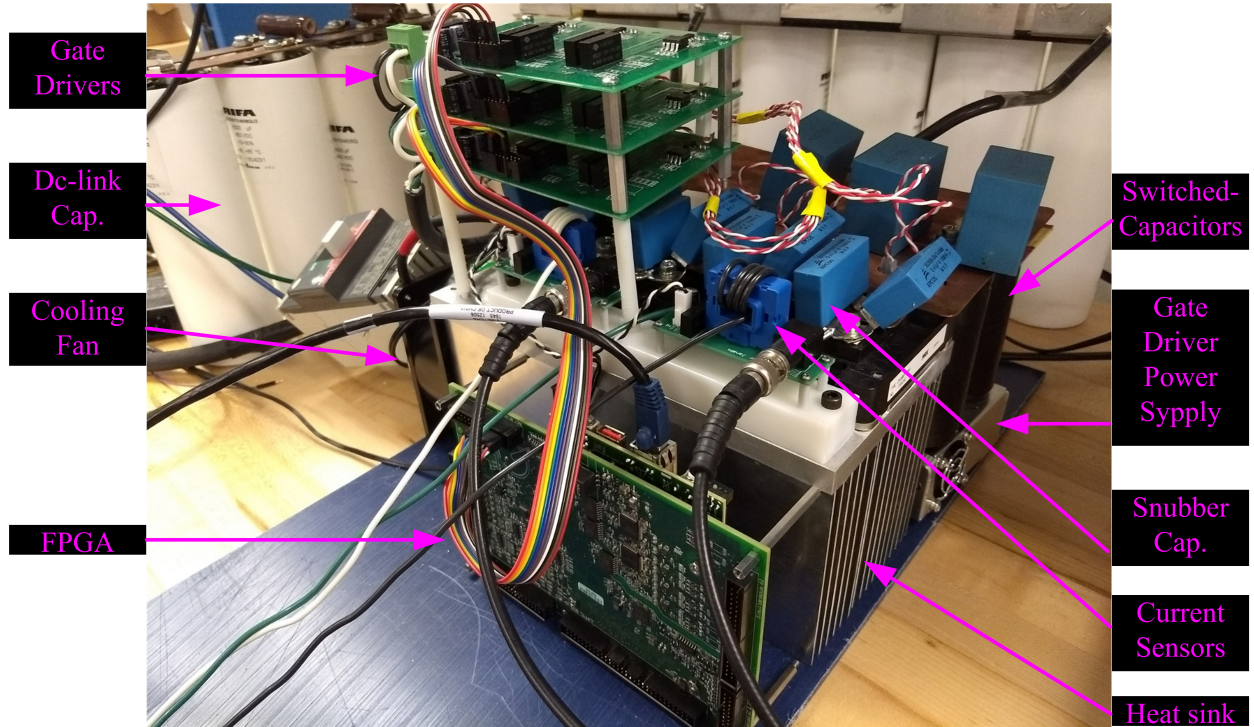


Figure 5.21 Exploded view of the SC converter layout.

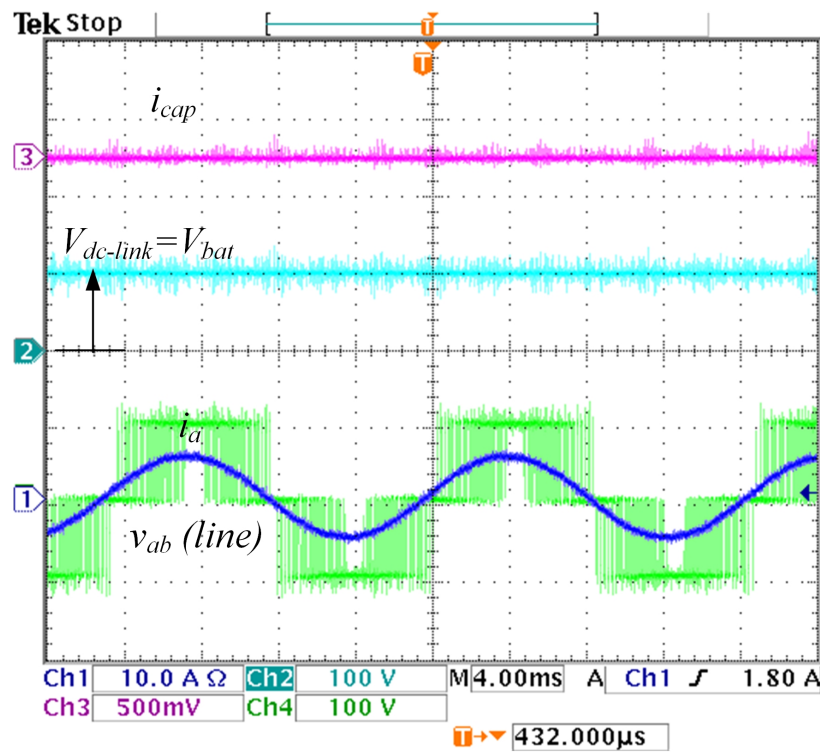


Figure 5.22 Experimental results of (a) abtstemious mode, $M_i = 0.5$ and $A = 0$.

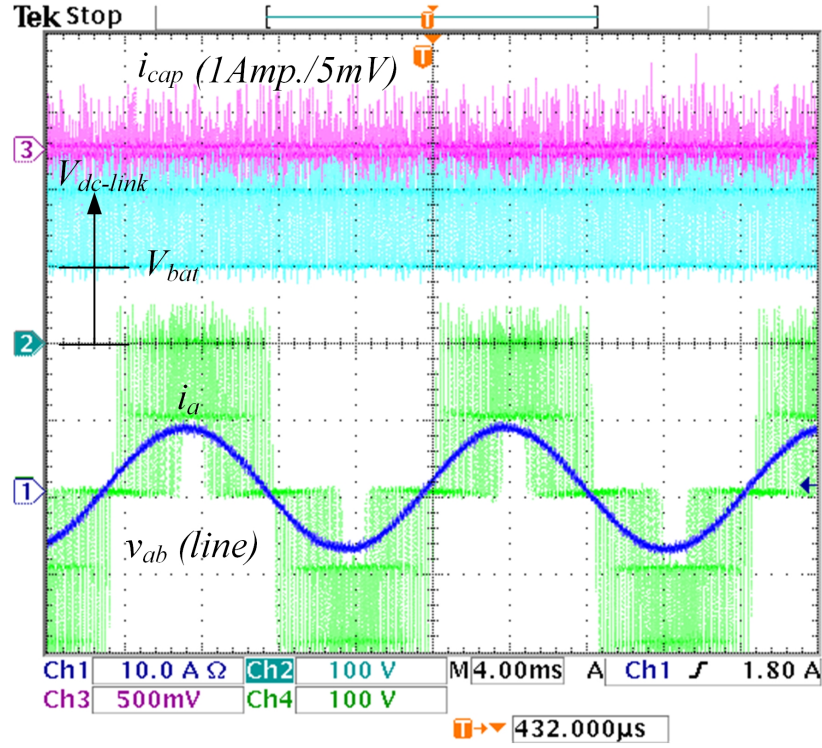


Figure 5.23 Experimental results of gluttonous mode, $M_i = 0.5774$ and $A = 0.5$.

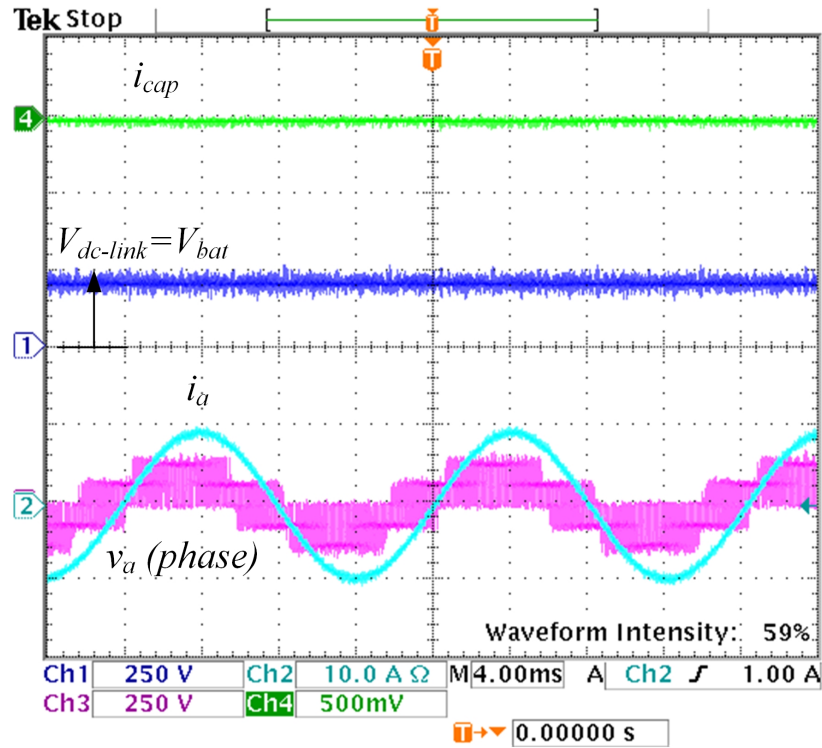


Figure 5.24 Experimental results of abstemious mode, $M_i = 0.5$ and $A = 0$.

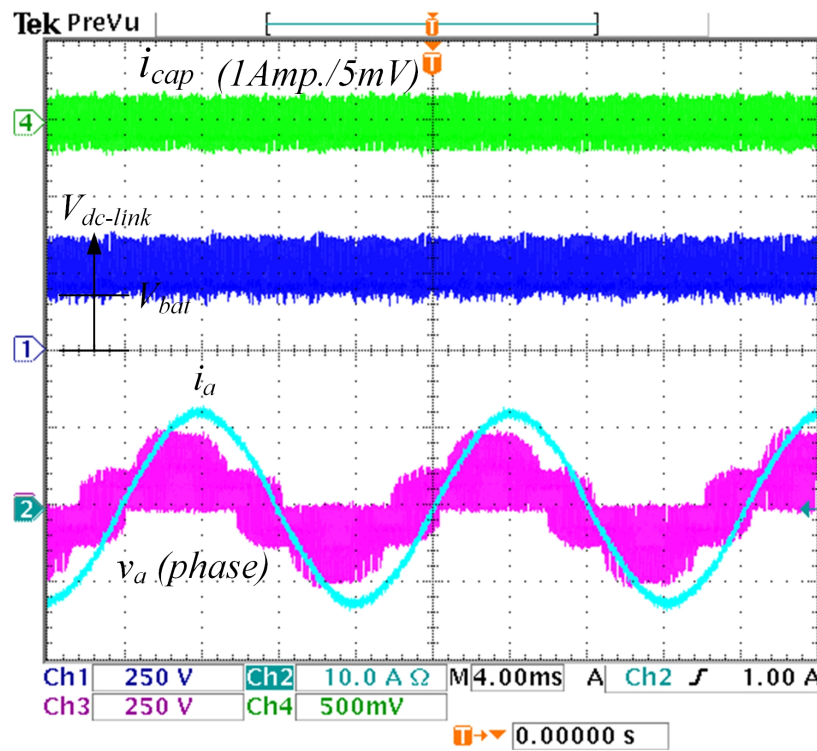


Figure 5.25 Experimental results of gluttonous mode, $M_i = 0.5774$ and $A = 0.5$.

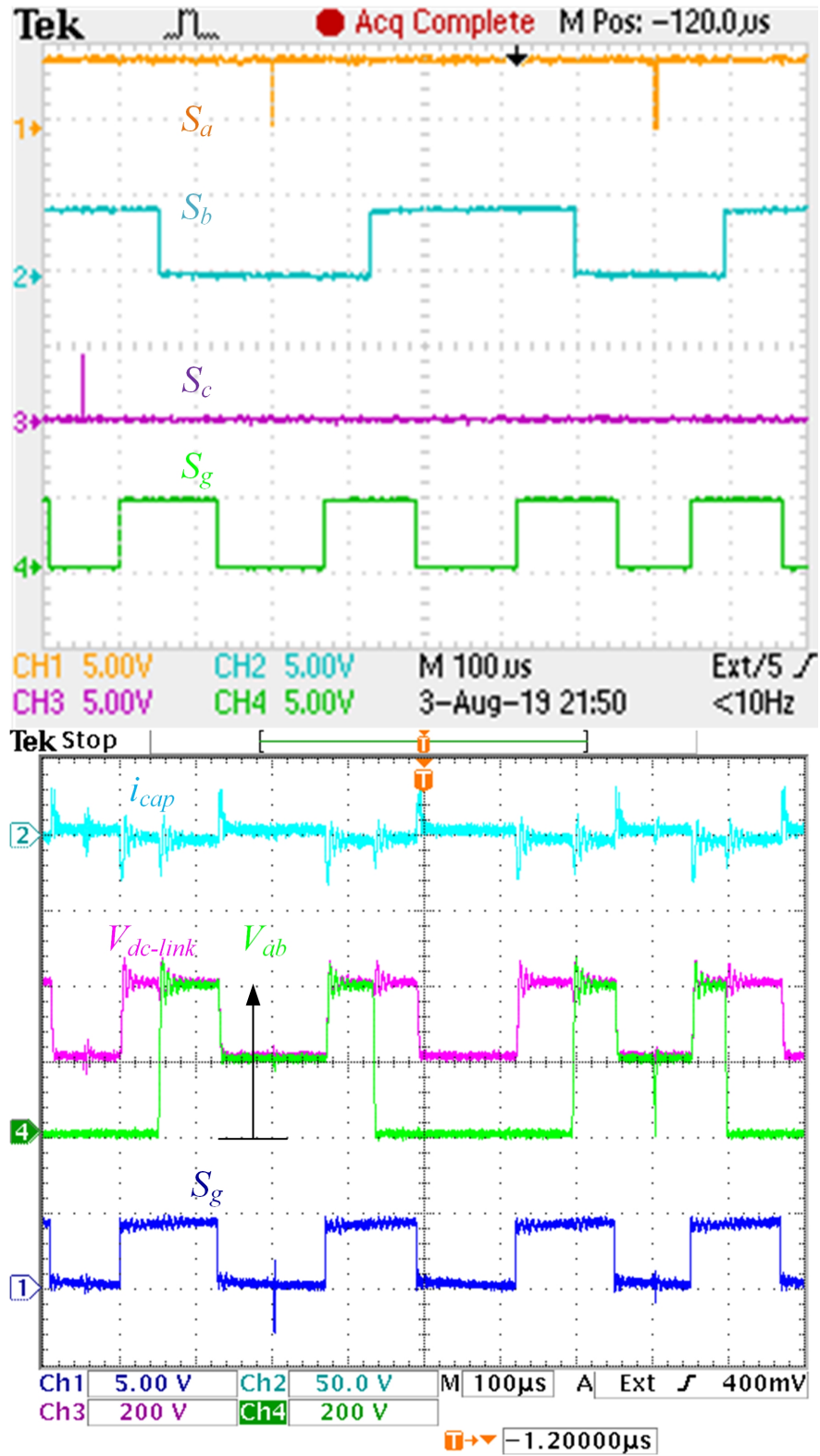


Figure 5.26 Experimental results showing the charging current with respect to the switching functions of the SC converter. (Ch2: 1 A/V).

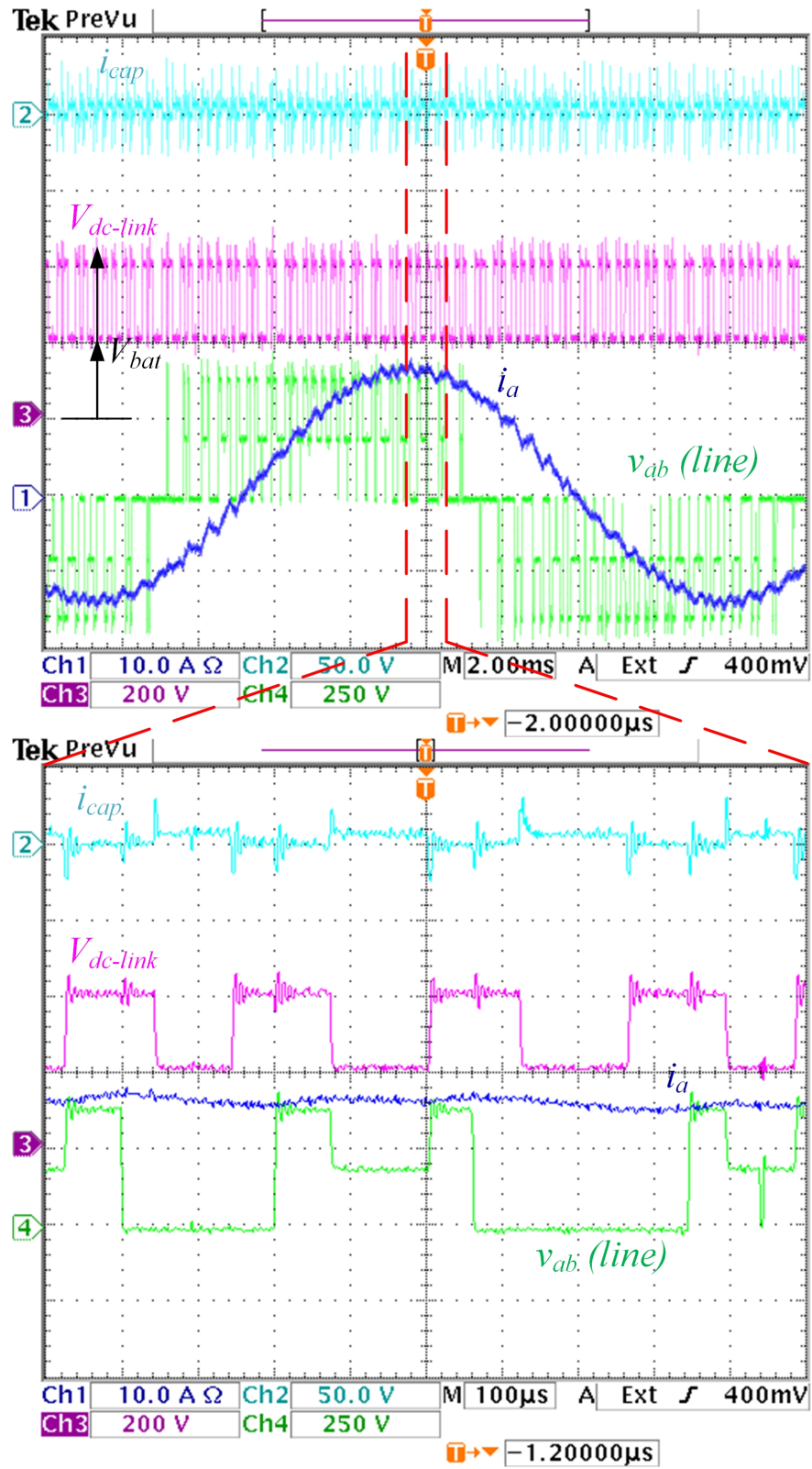


Figure 5.27 Experimental results showing the switching transient of the SC converter at 1 kHz switching frequency. (Ch2: 1 A/V).

Chapter 6

Conclusions and Future Work

In first chapter, a set of new HSVPWMS control methods are proposed to minimize the amplitude and frequency of the CMV. A detailed comparison shows the relative performance of the conventional PWM methods and the proposed HSVPWMS methods in terms of CMV characteristics, HDF, switching losses, and DC ripples. The conventional PWM methods have a CMV harmonic component with high frequency equal to the carrier frequency f_c . The new HSVPWMS method proposed in the chapter limits the CMV amplitude to $\frac{V_{dc}}{3}$ and concentrates the CMV harmonics to a low frequency equal to three times the fundamental frequency $3f_1$. A new commutation algorithm that avoids nonlinear behavior during dead-time intervals is proposed. The performance of the proposed HSVPWMS algorithms has been verified via simulations and validated by laboratory experiments. The new HSVPWMS method can potentially enable converters to operate at a very high switching frequency using the newly emerging wide bandgap devices while effectively mitigating the adverse CMV effects associated with conventional high-frequency PWM schemes.

In second chapter, an MPC-based control method is proposed to fully control the amplitude and the frequency of the CMV. Two approaches were implemented to govern the commutation between odd and even voltage vectors to shape the characteristic of the CMV. The first one is sequenced commutation (SC) and the second one is pulse width modulation commutation (PWMC) method. Both of which can cover all the linear region with full modulation index. The previously proposed

methods are summarized and compared with the proposed method. The ability to fully control the CMV frequency allows us to minimize the resulting shaft current without reducing the switching frequency of the system. A high frequency machine model to investigate the bearing current is presented.

The proposed method gives an extra degree of freedom over the CMV and shows that all of the previously proposed methods are special cases of the proposed method. This additional control freedom can potentially enable MPC controlled converters to operate at a very high sampling frequency without having the CMV effects associated with conventional MPC methods. The MPC-PWMC is more capable than MPC-SC method in concentrating the frequency of the CMV at the carrier frequency. The simulations and experimental results show that MPC-SC and MPC-PWMC methods produce similar current tracking performance. The THD of the load current can be further reduced when the commutation frequency is increased.

In this third chapter, a new real-time SHE implementation method is presented. By the transformation of variables, the transcendental equations of the optimization problem are converted to a set of algebraic equations using Chebyshev polynomials. Then the set of algebraic equations is reduced to a single univalent polynomial using generalized Newton's identities. The roots of this polynomial hold the values of the switching angles. The switching angles are calculated in real-time by simple substitution of the reference phase. The original contributions of the proposed RTSHE/M are the following:

- 1- Presenting the generalized Chudnovsky algorithm. The new algorithm allows modulating the selected harmonics rather than only eliminating them. In the near future, this feature will be utilized for the wireless energy transfer of the multi-receiver case.
- 2- Presenting a new method of obtaining the values of the optimal switching angles from the polynomial in real-time without resorting to any iterations or guesses. This enabled the implementation in the microcontroller with a determinate execution time.

The proposed method requires minimal computational effort by the controller because it is not

an iterative process and does not involve any guessing of initial conditions. Hardware experiments show the superior dynamic performance of the proposed method during a change in the modulation index, switching frequency, and both switching and fundamental frequencies. The proposed method has the efficacy to be a viable replacement for the offline approach and the existing online approaches.

The last chapter has presented a new switched-capacitor power converter (SC) for implementing dc-ac and ac-dc power conversion. The SC converter employs a switched-capacitor circuit augmented with the main converter circuit to the power source, thus providing unique features that cannot be attained by the traditional VSI or boost VSI. One of these unique features is doubling the area of the linear modulation region.

The SC converter eliminates the need for the cumbersome and costly inductor to boost the voltage. Instead, it relies on only the capacitors to achieve voltage boost, which allows higher power density.

The formulation of the maximum voltage drop across the capacitor and the minimum charging current are analytically derived. The analytical results provide a clear insight into the design elements that affect the behavior of the charging current, thus allowing the operation at higher power.

The carrier-based modulation method for the new SC converter is derived from the SVPWM and employs the exact switching sequence of the SVPWM method with minimal computational effort.

The analytic derivations, simulation, and experimental results have validated the operating principle and modulation methods of the proposed converter. The SC converter can boost or buck voltage, minimize component count, increase power density, and reduce cost.

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