ADDITIVE MANUFACTURING FOR RAPID PROTOTYPING OF MM-WAVE CIRCUITS

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ABSTRACT

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Additive manufacturing (AM) has recently attracted significant interest to meet the need of next generation of wireless systems, and the growing demand for customization and rapid prototyping of electronic systems. In addition, AM is being investigated to supplement and in some cases replace traditional microelectronic fabrication techniques. This is to lessen the ecological impact of electronics manufacturing as well as to reduce cleanroom facility costs. This research work focuses on the use of AM for the design and fabrication of microwave and millimeter wave components and systems, leading to heterogeneous integration. For systems integration, two major challenges to tackle are: (1) rapid printing of conductive regions with high precision and high conductivity; (2) selective deposition of dielectrics with varying geometries surrounding active and passive components. In this work, printing of both conductors and dielectrics was carried out using aerosol jet printing (AJP). AJP allows for high resolution printing ($\sim$10 μm) at a large standoff distance ($\sim$10 mm). Silver (Ag) based inks were investigated to achieve high conductivity and polymers (benzocyclobutene, BCB and Polyimide, PI) as low-loss dielectric materials.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

An approach to fabrication of fine resolution printed circuit components with rapid annealing of conductive materials and rapid fabrication of thick film dielectric substrates is presented in this thesis. These techniques for rapid processing include hardware design and processing of materials, which are described in detail. Sample circuits are fabricated and measured with results shown along with simulation data. Radio Frequency (RF) ranges up to millimeter-wave (MMW) circuit fabrication are the primary motivation for this work.

1.1.1 Motivation

Interest in Additive Manufacturing (AM) techniques for the fabrication of electronic devices has increased greatly in recent years. Coupled with a desire to fabricate devices with green or eco-friendly materials: research has focused heavily on reduction of waste during the fabrication of electronic devices and packaging. Historical fabrication methods included many caustic, hazardous materials, and expensive equipment. By moving away from traditional subtractive manufacturing, the requirements for masking techniques, lithography equipment, evaporation and sputter deposition machinery, and etching chemicals or chambers is drastically reduced. By using AM methods to fabricate electronic devices, virtually no waste can be achieved by building up work pieces with the precise amount of materials required on-demand. AM techniques also allow for far fewer pieces of equipment, such as 3D printing to replace injection molding equipment or inkjet and aerosol jet printers to replace photoresist mask alignment and developing equipment for patterning of materials [2].

1.1.2 Review of Additive Manufacturing

Most common practices for fabrication of printed circuit boards (PCBs) involve placement of a pattern onto conductive materials clad to either side of a dielectric or insulating material. The conductors are systematically removed to leave a desired pattern forming the electrical pathways for devices and components that make up a circuit. This process can involve toxic chemicals, expensive equipment or laboratory time invoking many steps to yield a patterned material on a substrate or wafer. With the use of AM techniques, portions of a circuit or even the entire substrate can be fabricated from the ground up using basic materials. This is where 3D printing has gained most traction in the past decade, as plastic components can be fabricated layer by layer to create a physical part that can be touched and used with very few steps and materials required [3, 4, 5, 6, 7]. This is the power behind additive manufacturing; a single machine has the potential to fabricate most or all an electronic circuit for use by a consumer, requiring less laboratory space and less material waste to create similar products in comparison to traditional manufacturing methods. Relating to the first example of PCB fabrication, a conductive ink may be deposited in the exact final pattern and thickness designed by the user with 3D printing. Once processed, this conductive layer can be used in the same way a PCB fabricated with pattern, developing, etching, and plating steps used by subtractive methods but realized in one or two steps with far less waste, equipment, or laboratory space.

1.1.3 Review of Aerosol Jet Printing

Aerosol jet printing (AJP) has gained a lot of traction within the AM fabrication world in the recent decade. Offered commercially through Optomec, research and development of new AM processes have created new methods for the deposition of conductive, dielectric, magnetic, and semiconducting materials on-demand without the requirement for pattern and etching processes. Virtually an entire laboratory of expensive and specialized equipment can be replaced by a printer and few supporting equipment for processing of the deposited materials. Fine resolution patterns can be created on the fly with little programming skills required by using an AJP. This makes AJP

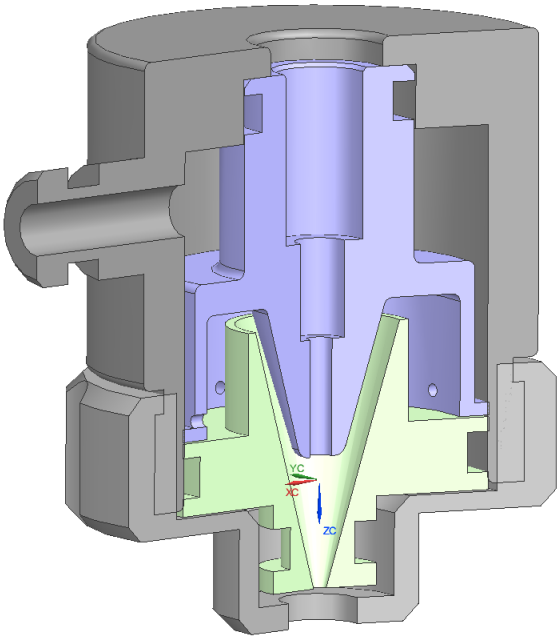

Figure 1.1: Cutaway view of Optomec 5x print head.

highly desirable for RF circuit prototyping and fabrication, as very small features ranging from 10 μm to 100 μm can be easily reproduced. Material characterization and processing of the deposited films is the most challenging aspect in relation to the use of AJP for electronic circuit fabrication. A lot of focus and attention have been in this particular area recently. This thesis makes use of the advantages of AJP and draws best practice for how to overcome some of the challenges involved with rapid processing of these materials for RF and MMW circuits.

Figure 1.1 demonstrates the 3D structure of the print head used in the Optomec AJP process. Atomizers containing liquid inks form an aerosol mist which then route to the print head. This mix of aerosolized particle mist and nitrogen from the atomizer is introduced into the print head through the top inlet. A sheath gas of nitrogen is also inserted into the body of the assembly (shown on the left). This sheath gas defines the size of the feature to be printed by exerting pressure on the mist stream in the lower funnel chamber before exiting through a print nozzle to be installed at the bottom of the head. The print nozzle (not shown in the figure) can range from 100 μm to 300 μm exit orifices in steps of 50 μm. These various nozzle tips allow for intermediate ranges of orifice sizes between the neighboring size. The smallest nozzle yields the smallest feature size,

and the largest nozzle yields the largest feature size. Increasing the flow rate of the ink or the sheath gas may drastically increase or reduce the feature size and deposited thickness according to experimental procedures.

1.2 Conductive Materials

1.2.1 Overview

Conductors are a valued component when it comes to deciding the fabrication of a PCB. Cost of materials and ease of fabrication are often the key deciding factors when metal is being considered. Choices of metal conductors for circuits can vary between Gold (Au), Silver (Ag), Copper (Cu), Tin (Sn), Titanium (Ti), and Aluminum (Al), for most common applications. Copper is a soft, malleable, ductile metal that has been historically chosen for use by the electronics industry for its low cost in comparison to its rarer, high conductivity relatives such as silver. Copper is often used for most printed circuit interconnects or traces found on substrates. When passivated for protection from oxidation, copper can be used for high current and low resistance of PCB conductors. More valuable conductors are often much thinner and used either as oxidation protection or for high conductivity applications. For environments where oxidation or exposure to atmospheric conditions cannot be avoided, other conductive materials such as gold may be used as a plated layer on top of nickel and copper to protect underlying surfaces, or as a complete replacement for the conductor as a whole.

1.2.2 Traditional Fabrication Methods

There are various methods for application of conductive metals onto substrates for the basis of conductive paths or traces. Common techniques used for large scale fabrication of conductors involve either deposition of metals at a molecular scale or the adhesion of large films or sheets of metals to a board surface. While these methods of conductor application are additive in nature, they also require subtractive methods in order to pattern and remove unwanted materials to leave the desired conductive features on the substrate. These methods have been tried and true for decades

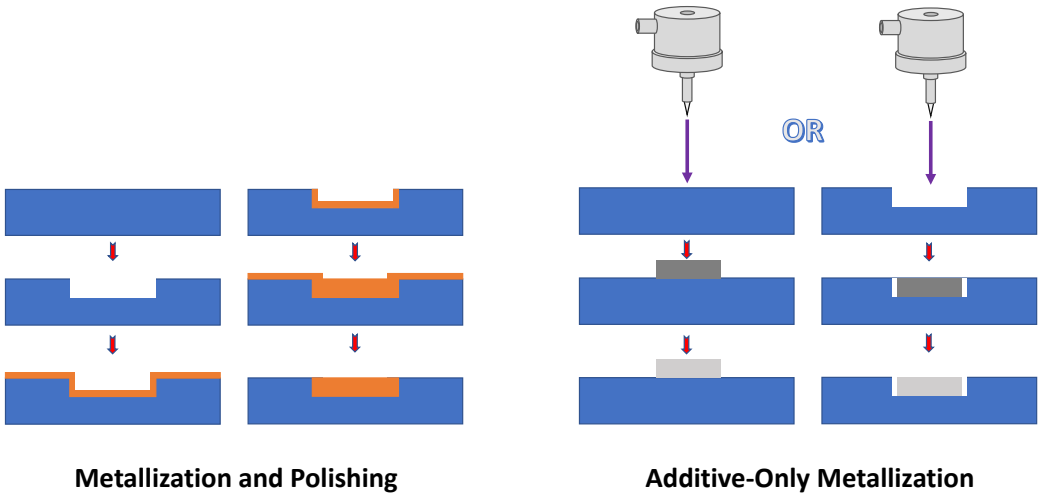

Figure 1.2: Left: mechanical polishing of unwanted metal layers must be performed, alongside pattern and etch lithography to reach desired metal patterns. Right: AM methods allow for the final metal pattern to be achieved in the first steps, without removal of unwanted material.

and have high levels of repeat-ability and predictable outcomes. However, the downside to such methods is the cost of equipment, materials, waste, and chemicals required for the entire process. Green or eco-friendly solutions are difficult to achieve with a subtractive process. See Fig. 1.2 for illustration of traditional methods and additive methods proposed below.

1.2.3 Additive Manufacturing Conductors

A desire to remove the subtractive process completely from printed circuit fabrication has been expanding with the introduction of 3D printing. Rapid prototyping of designs with short turnaround time and lowered cost is highly desired. In order for additive manufacturing circuit fabrication to be practical, it must be highly comparable and cost-competitive with traditional methods. For high frequency operations, conductors must be low ohmic resistance, maintain controllable impedance matching, and have minimal electrical noise [8]. Pattern and etch lithography processes have yielded consistent and accurate fine resolutions of conductors for decades. In recent years, technologies such as injket and aerosol-jet printing have become popular due to relative low-cost of

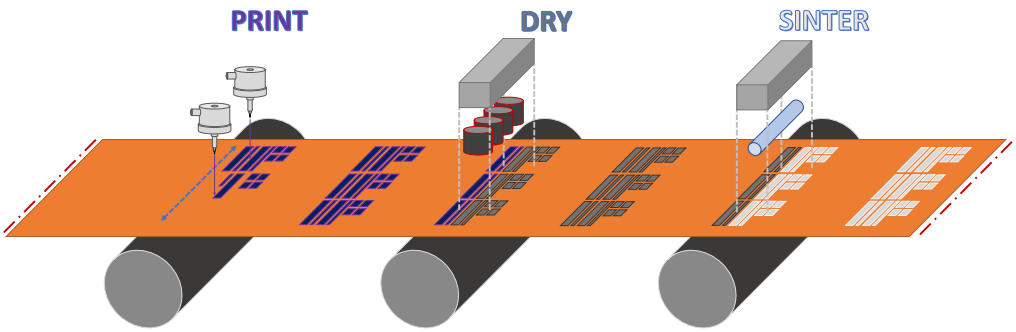

Figure 1.3: Proposed Reel to Reel fabrication using AJP and flash sintering for conductive traces.

materials and post-processing required. These two printing techniques have been the at the front of attention, as they can fabricate fine resolution circuit components with precision in the micron (μm) range on nearly any surface.

The leading challenge brought forth by AM conductor fabrication is the nature of the materials being used. In comparison to traditional methods, AM conductive materials have the unique challenge of requiring processing steps to form high conductivity films after being deposited. The most common technique for printing conductive materials is in the form of a nanoparticle (NP) ink or nanoink. These inks are formed of conductive molecules on the scale of nanometers to fractions of a micrometers, suspended in a dispersion of liquid to prevent clumping and oxidation. In order for this ink to become conductive on a scale comparable to sputtered, plated, or rolled films of metal (known as "bulk" conductivity) they must be annealed or sintered to form conductive networks of molecules. This process can have many different approaches with varied outcomes and results, which are discussed within. The desire for AM conductive materials is to be a successful replacement or substitute to a compatible process for use in large scale processing. In Chapter 1, literature review of various types are compared and contrasted, and an optical flash sintering

system is described in detail for conductive silver nanoinks deposited by AJP. Ultimately, this allows for a reel-to-reel fabrication method to be integrated using AJP and flash sintering. Printing, drying, and sintering steps can be performed with individual machines connected via rollers as the substrate is fed through them. A brief description of this process can be seen in Fig. 1.3.

1.3 Dielectric Materials

1.3.1 Overview

Dielectric materials are the second critical component for circuit fabrication. Substrates for nearly all printed circuits are formed using dielectric compounds. For RF circuits, dielectric substrates with low loss and high performance characteristics are chosen for each specific application. Both rigid and flexible substrates can be fabricated with the use of polymers, hydrocarbons, elastomers, fibers, glasses, and even ceramics. One of the most common substrates used for electronic circuits is woven fiberglass board such as FR4 [8]. While common substrates may be inexpensive to mass produce and have many uses, they are not always the best choice for RF applications. As technology has advanced and frequency requirements for communication have pushed past microwaves and into millimeter-wave frequencies, dielectric substrates with much lower losses have been required to meet performance demands. While many RF substrates are designed with particular uses in mind, the application may dictate which materials are appropriate. As with other fabrication processes, both subtractive and additive manufacturing methods have been developed to meed those needs.

1.3.2 Applications

Using the 3D printing approach with AJP described in this thesis allows for rapid design and development of thick film dielectrics, and new fundamental applications can be achieved with ease. Relative to traditional processes, AM has the potential to reduce processing time of dielectrics from weeks or days to hours or less with few or single steps [9]. With AM, various thickness films may be created, allowing for step structures and ramps to interconnect and route around chips

with different thicknesses and material properties. Interconnection distance between chips can be reduced to the absolute minimum on the same z-plane. Active and passive devices can be placed into embedded cavities, and heterogeneous integration of hybrid RF and MMW circuits can be achieved with minimal number of steps and vastly reduced processing time [10].

1.3.2.1 Different chip thickness

Active and passive devices of various technologies range from ceramics, organics, and metal films, to semiconductors of varying elements and alloys. Each of these technologies may vastly differ in x and y dimensions as well as z-thickness when placed and processed on boards. Many traditional hybridized circuits comprise of a combination of etched distributed-elements, surface mount devices (SMD), bare die, chip capacitors, resistors, inductors and baluns. In order to interconnect these devices, a mix of microstrip traces or waveguides and transitions weave and route through a board plane or multiple planes using vias in order to make connections to devices with rigid connectors or pads with wirebonded leads. This mix of technologies allow for an engineer to pick and place components on demand from many different manufacturers and subset families within those groups. By using a substrate as a carrier plane of either planar or non-planar z-height, devices may be attached or glued in place ahead of interconnection. The challenge introduced with mixing of technologies is the interconnect, which can be improved with 3D printing. By placing components onto a carrier substrate and then printing dielectric filling in moats, valleys, and dams around the parts, 3D printed interconnects may be formed to make the electrical connection hybridization. For these various devices with vast ranges of z-height, AM allows for material agnosticism.

1.3.2.2 Minimal Interconnect Losses

One major challenge when utilizing a hybrid circuit design with multiple thickness chips is the format used for interconnection. Wirebonding of two chips with a large difference in z-height or added x and y distance between chips will increase the parasitic properties of the wirebond such as series inductance and resistance. One solution is to use dielectric embedding of chips or

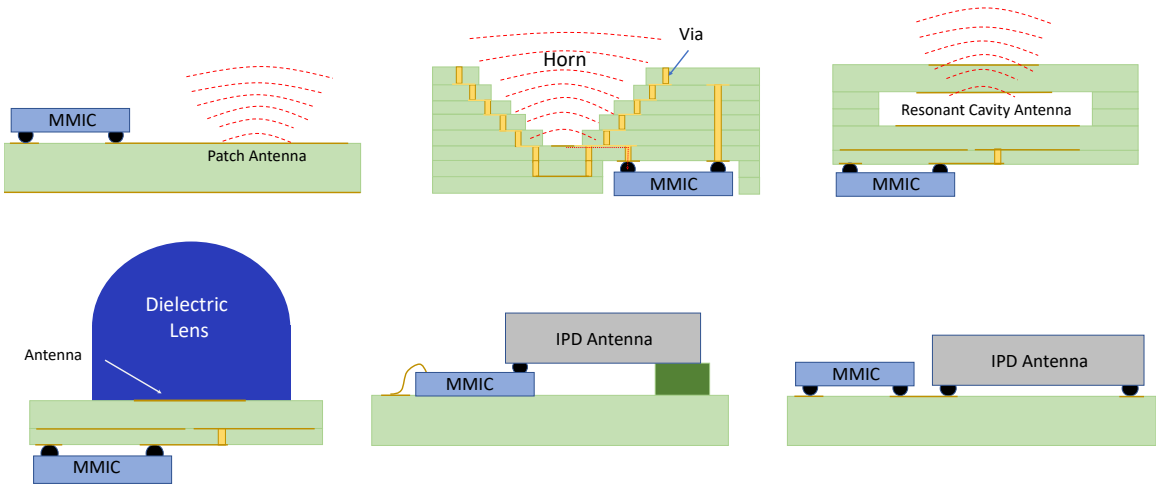

Figure 1.4: Various embedded and integrated MMIC circuits formed as integral active MMW systems.

dielectric ramps to bridge connections for 3D printed conductive interconnects. By allowing for devices to be placed closely together with minimal x, y, and z distancing, the minimal interconnect loss can be achieved for DC and RF circuits. Allowing for custom 3D printed shapes, routes, and materials to be used increases the fabrication efficiency and robustness as well as reducing potential interconnect loss over traditional connections. AM processing removes the difficulty in mask alignment required for hybrid designs that are not one-off fabrications; as component placement machines have certain tolerances, 3D printing greatly reduces the requirement for such tolerances with tailored deposition.

1.3.2.3 Embedded Actives

Embedding of devices in dielectric materials allows for improved hybrid designs of mixed technologies. Embedded actives as well as passive biasing components allow for systems to become packaged into the substrate rather than sitting exposed on the surface of a card. While card and panel technologies are heavily used and popular for RF circuits, the implementation of hybrid

components sourced from various manufacturers increases the challenge of hybrid circuits without fully packaged devices. Embedding active devices into a self-package improves reliability and robustness of the system and reduces the difficulty of designing hybrid circuits. This concept was heavily used in the 1990s by companies such as General Electric for the High Density Interconnect (HDE) fabrication assembly [8, 11]. Embedding of active devices also allows for self-packaging in ways which were challenging before, but now would allow for integration of active components with 3D structures. One such structure is a monolithic microwave integrated circuit (MMIC) embedded in a horn antenna (see Fig. 1.4).

1.3.2.4 Heterogeneous Integration

Heterogeneous integration has traditionally been a wafer level technology involving many difficult steps and requiring expensive masking techniques [1, 12, 13]. With the use of 3D printing on substrates and wafer surfaces, this type of close device integration can be achieved without the tedious masking, liftoff, coating, and oxide growing processes used in wafer fabrication to develop membranes, bridges, and layer interconnects. Instead, by using 3D printing, devices can be closely placed either with automation or manually for one-off designs. These placed components can vary in distance between as well as z-height differences and still be interconnected, integrated, and packaged in similar manors with far less steps and less expensive equipment. The application of this in the future could allow for integration of microelectromechanical systems (MEMS), surface mount or 3D printed transistors, and both packaged and unpackaged devices within the same vicinity to be housed on a carrier substrate or even non-planar surfaces. These technology improvements allow for a direct chip integration regardless of thickness and size without the complications included with wafer level fabrication. Various methods of achieving high density interconnected devices have been shown by industry for RF MEMS devices and other small footprint circuits which require integration of varied technology chips. Benzocylobutene (BCB) polymers have been used for the packaging of such devices for RF MEMS [14]. While traditional wafer level fabrication requires large masking areas in order to develop only a small number of delicate membrane struc-

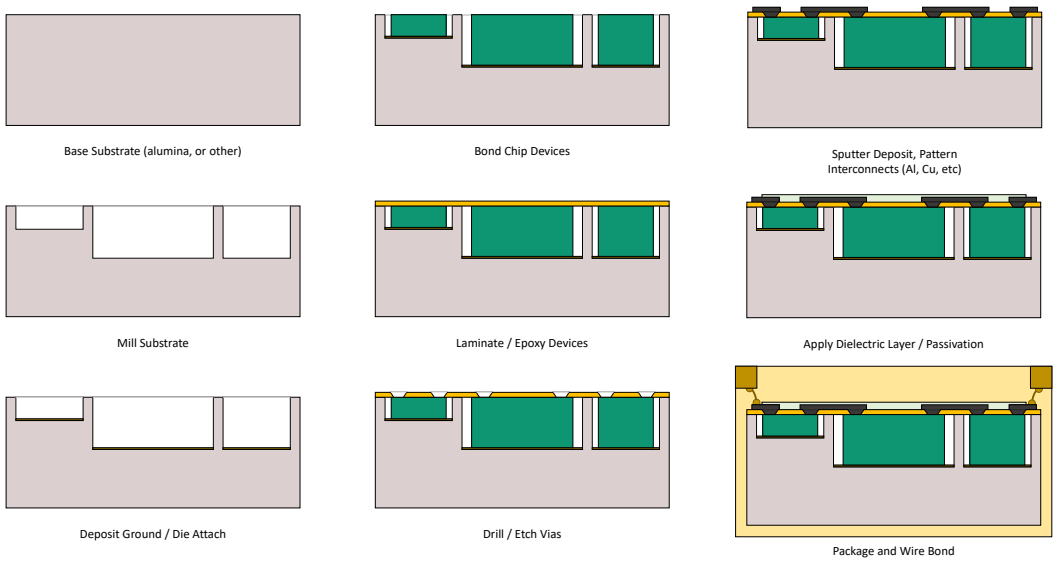

Figure 1.5: Diagram of GE High Density Interconnect fabrication technique used in the 1990s [1].

tures, similar fabrication can be done utilizing a dam and fill method with a lift off step on substrate of choice.

1.3.3 High Density Integration Techniques

Traditional methods for achieving these desired properties was lead by research and fabrication techniques utilized by high density integration [1]. Shown in Fig. 1.5. The main challenges sought to overcome here include the proximity of chip placement, varied chip heights on a single carrier, depositing as many layers with 3D printing as possible, and tailoring dielectric material to vary across the substrate as needed for each chip.

1) In order to significantly reduce proximity of chip placement, cells can be fabricated surrounding chips or sets of chips with minimal distancing allowing for the shortest possible interconnection between devices. One early method for this type of multichip module (MCM) fabrication was the chip first and chip last approach to interconnects [15, 16]. Chip first places the device face up and then involves the fabrication of interconnects on the face of the chips. Demonstration of this process is shown in Fig. 1.6

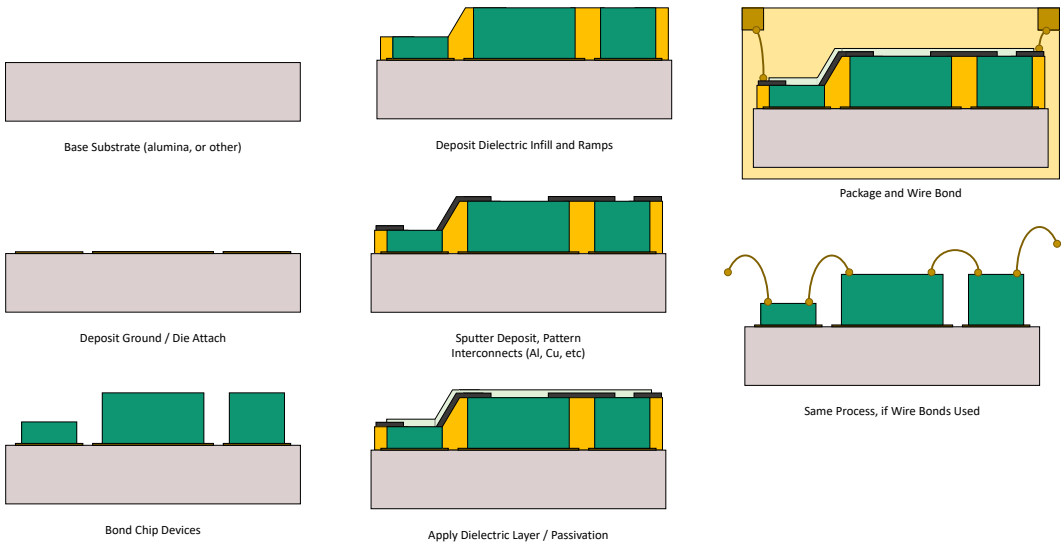

Figure 1.6: Diagram of Chip First/Chip Last fabrication technique used to encapsulate devices on substrate surfaces.

Using AM techniques, the dielectric walls to form as bridges for interconnects can be selectively printed around the chips in order to form rigid support. This allows for a tailored package on the carrier with the best choice dielectric materials to interface with the chip technology being used. Shown in Fig. 1.7 is another example of chip first approach, in which active components are embedded in a cavity formed on the substrate surface.

2) To overcome the varying heights of chips on the same carrier board, different methods have been used to approach this issue. Dielectric ramps, bumps, and bridges have been 3D printed from one height to another in order to gap the distance between chips. These methods incur a few parasitic losses similarly to wire bonding, but often with far less negative effects. The most desired approach would involve having the face of two chips at the same height and minimum proximity placement. To do this, the best approach taken by this thesis was to fabricate chips together in a custom tailored package starting with the chips face down on a release agent and building the package around them. This method allowed for closest chip placement with both faces at level heights to create the shortest possible distance between chips. Shown in Fig. 1.8 is one solution to

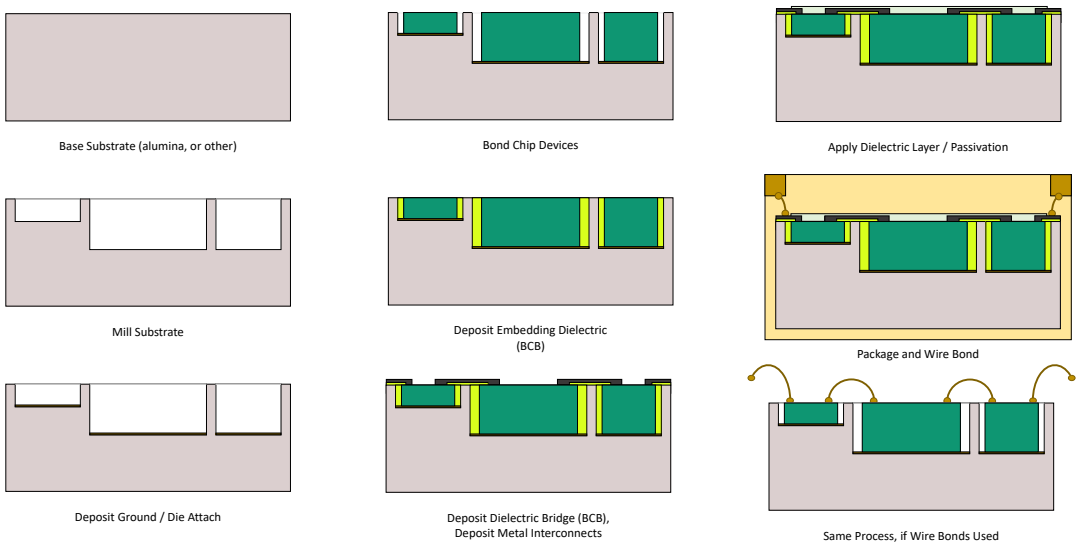

Figure 1.7: Diagram of Embedded Devices fabrication technique used to encapsulate devices embedded in cavities etched into substrate surfaces.

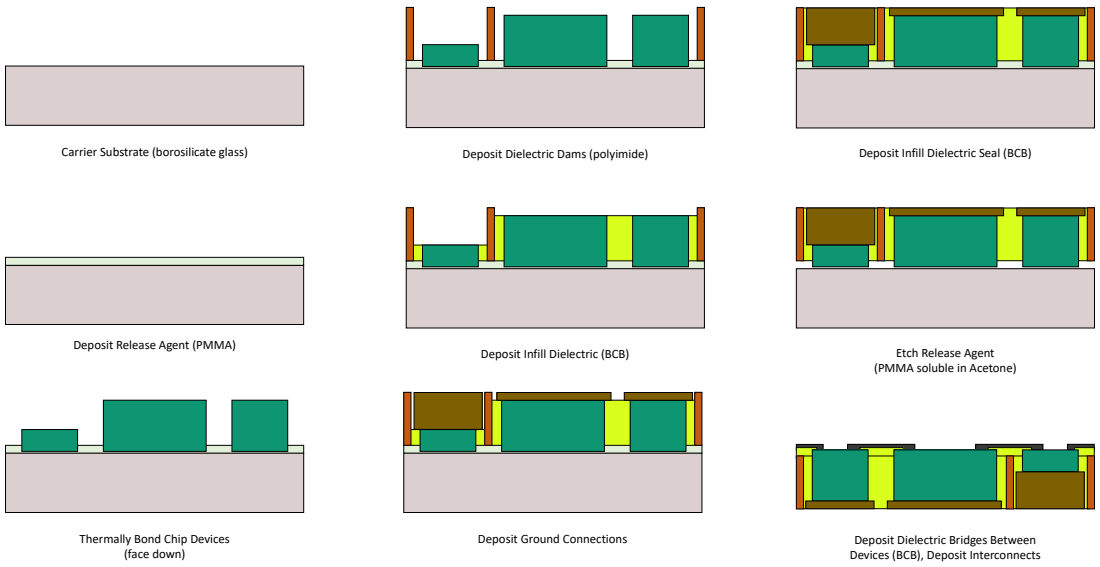

Figure 1.8: Diagram of Substrate-Less fabrication technique used in this research to print packages with fully AM processes.

this problem best described as a substrate-less approach.

3) For active devices with different heights, the substrate-less packaging can be utilized to

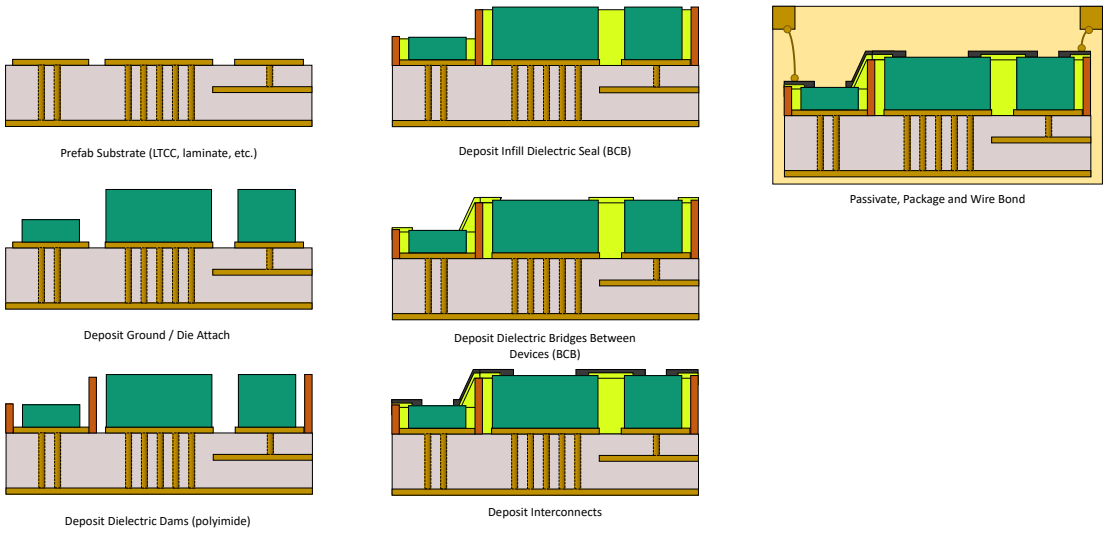

Figure 1.9: Diagram of Substrate-Less on PCB fabrication technique as compliment to Chip Last fabrication approach.

deposit or 3D print all of the materials on the bottom face of the chips (excluding heat sinking materials at this time). The complexity of fabricating a conductive heatsink microns at a time to overcome height differences of more than 10 μm was not undertaken in this work. Conductive plugs of metal could be placed on the contacts used for heatsinking in order to transfer heat (and current if not electrically isolated) away from the chip and to the same z-plane as the entire tailored package [14]. Shown in Fig. 1.9 is another form for substrate-less approach which resembles the chip first approach to MCM fabrication on the surface of a substrate. The major difference here is that substrate-less allows for self-packaged systems of devices with various thicknesses and technologies directly onto a PCB if desired.

4) By utilizing cells of dams with infilled dielectric materials, the dielectric can be varied across the carrier board to allow for multiple substrates tailored for a truly hybridized, highly dense integration. With chip technology that may require flexibility in its surrounding dielectric well, a rigid polymer with vastly different coefficient of thermal expansion (CTE) will likely cause delamination or cracking of printed interconnects as well as the dielectric fill around the chip. In order

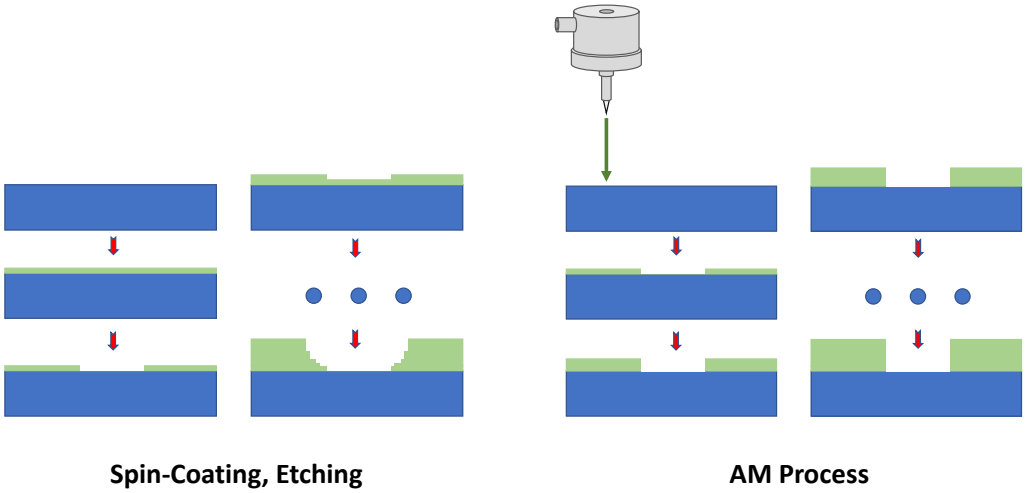

Figure 1.10: Left: dielectric material is spin-coated and processed one layer at a time, involving patterning and etching. Right: AM processes allows for final dimensions to be fabricated in as few steps as needed.

to avoid this issue, CTE matching and mechanical requirements can be met around each device uniquely and then interconnected to the neighboring cell. This process easily allows for hybridization that would have been made impractical with traditional methods due to cost or complexity to fabricate multiple dielectric thick films on a single board.

1.3.4 Coating Substrates

One very common method for dielectric film fabrication used for decades in the semiconductor industry is the spin coating and patterning process. This process involves the application of dielectric materials (often polymers) onto a carrier substrate via a high speed spinner and then processed to remove areas where the dielectric is unnecessary. This process has been used to fabricate many structures from simple RF elements to complex MEMS circuits. But, the process is complex and requires the use of specialized equipment and often very hazardous chemical processes. In most cases, thin films of dielectric material are fabricated with ease in this process and then patterned with fine resolution to achieve the detail required for the circuit. What is extremely challenging is

the fabrication of small, fine featured details, with thick films. The fabrication of thick films (tens to hundreds of microns) for polymer materials is very time consuming as it may require many steps to achieve desired thickness of films in only certain areas of a circuit, or incur planarity issues as the z-height increases over many layers. See Fig. 1.10 for illustration of traditional methods and additive methods proposed below.

1.3.5 AM Techniques

Because traditional methods make fine resolution thick film dielectrics challenging, new approaches with fully additive manufacturing methods are key to solving problems in the electronics packaging and RF communication communities. By eliminating the need to process a circuit with harmful chemicals and expensive equipment, rapid fabrication can be achieved with relatively few steps. The technique approached within and discussed in detail involves the use of a dam and fill process. This dam and filling process or selective dielectric deposition allows for creative and unique designs where non-uniform thickness of dielectrics throughout a printed circuit may be achieved with ease. Components that require encapsulation or potting can be surrounded with a dielectric dam material and then filled with the desired polymer or epoxy at virtually any thickness and shape. This allows for devices of dissimilar heights to be placed directly next to one another with shortest possible interconnects and even fully packaged hybrid systems on a substrate. Chapter 3 describes in detail how this dam and fill process is performed using AJP 3D printing for rapid fabrication of thick film dielectrics and chip scale packaging (CSP) to achieve highly dense integration of hybrid circuit components.

CHAPTER 2

STREAMLINING CONDUCTORS USING AJP

2.1 Introduction

Recently there has been significant research focus towards the design of high functional density electronic systems, especially for 5G applications. In parallel, to address accurate, high-quality, fine-resolution circuit geometry requirements: increased research into additive manufacturing (AM) printing techniques, such as Aerosol Jet Printing (AJP), has emerged. The issues are complicated by low-loss flexible substrates, such as liquid crystal polymers (LCP), which are commonly used in the design of high frequency circuits and systems. These substrates cannot be taken through high sintering temperature processes that are commonly required for silver nanoinks. To avoid permanent damage, it is essential that the sintering temperature remains below the glass transition temperature (T_g) of the substrates. Recent work on LCP substrates has demonstrated 10 - 20% bulk silver (Ag) conductivity by using low-temperature thermal sintering techniques. This paper investigates the use of a rapid ultra-violet (UV) flash annealing technique to achieve high conductivity of Ag on LCP for use in high frequency circuits while maintaining the integrity of the substrate. Results are compared against thermally sintered films. The resulting conductivity was studied as a function of UV exposure time and energy, printed film thickness, surface roughness of the substrate, and multilayer deposition.

2.2 Applications

Additive Manufacturing (AM), often referred to as 3D printing, is a process of building parts layer by layer rather than using traditional molding or subtractive lithographic methods. It is revolutionizing how critical parts get manufactured and enables rapid prototyping, reduced waste, quick-turn custom designs, rework adjustments, and parts can be printed as they are packaged into a single unit. Recent advances in higher print resolution, the ability to print multiple materials, and

the ability to print combinations of low and high-temperature materials open up the opportunity to design and manufacture next generation electronic systems without long and expensive cycle times [17, 5, 18, 19]. High density features and geometric structures that cannot be fabricated conventionally have now become realizable using AM technologies. Among the many printing technologies, Aerosol Jet Printing (AJP) and inkjet printing are commonly applied to deposit structures requiring fine line resolutions (10 - 100 μm). The range of inks (conductive, dielectric, magnetic, and mixtures) that have been printed to achieve desired electrical properties has rapidly increased in recent years with many more options under development.

Inks comprised of conductive nanoparticles (NPs) have been printed using a range of techniques [20, 21, 22]. One major obstacle to overcome has been the realized conductivity of printed metals on polymers and plastics that have low temperature limits or undesirably rough surface morphologies. NP-based conductive inks consist of metal particles of raw elements such as silver (Ag) which are smaller than 0.1 μm. They are suspended in a solvent, and the particles are often coated with organic stabilizing agents and encapsulants. Metallic NPs provide a reduced melting temperature compared to their bulk material forms [23, 24, 25, 26]. However, the organic coatings hinders lowering of this temperature [27]. These organics must be removed by sintering. The metallic NPs become more tightly packed after sintering which enhances conductivity by minimizing the contact resistance between the NPs. Conventionally, an oven is used to sinter printed Ag inks. The ink and the substrate may be exposed to temperatures as high as 200 to 300 °C to achieve high conductivity. However, many substrates, such as liquid crystal polymer (LCP), cannot withstand such high temperatures without a change in their physical state or being irreparably damaged. Low thermal budget processing of metal inks would enable access to these high frequency substrate materials for a range of microwave and millimeter wave applications.

To meet the challenge of low temperature processing, different approaches to sintering Ag nanoparticles (AgNP) have been investigated over the last decade [27, 28, 29, 24]. These include curing using lasers [30], intense pulse light (IPL) [31, 32, 33, 22, 21, 34], plasmas [29], [35], microwaves [27, 23, 36, 37], as well as electrical [24] or chemical [38] methods. All techniques are

capable of sintering at a relatively low processing temperature that is compatible with common flex substrates. Among these processes, the IPL, also called broadband-UV (ultra-violet) sintering, allows for sintering over a large area and can be incorporated with existing printing process equipment, especially AJP [21, 22]. IPL uses a Xenon arc-discharge lamp as a source of high intensity energy directed at a printed surface to achieve high conductivity on substrates. Photothermal processes in metal particles (thermoplasmonics) plays an important role in the sintering of nanoparticles [39, 40, 41, 26]. It has been shown that the magnitude of photonic heating depends on the shape and density of deposited nanoparticles [39, 42]. Using optical flash techniques, the resulting conductivities for silver inks have been reported up to 25 MS/m [33, 22, 43, 44, 31].

IPL has mainly been investigated in the fabrication of low-frequency circuits, and little or no work has been reported for the fabrication of circuits operating at radio-frequencies (RF) or higher frequencies. In this paper, we investigate the use of UV flash annealing to achieve high conductivity Ag structures on LCP for use in high frequency circuits within the LCP thermal tolerances. Ultimately, IPL can be integrated with AJP machines to meet the needs of multi-material (conductors and dielectrics) deposition for rapid prototyping.

2.3 Experimental Setup

2.3.1 Aerosol Jet Printing

AJP has gained significant interest as an accurate alternative to photolithography for RF circuits, integration, and packaging. Circuits that cannot be realized or are impracticable using mainstream coarse-feature AM methods are potentially feasible with the use of AJP, e.g., printing on non-planar structures [45]. An Optomec 5-axis AJP was used in this work. It is equipped with two types of atomizers, an ultrasonic atomizer for low viscosity inks and a pneumatic atomizer for higher viscosity inks [46, 20]. Inks consisting of NPs dispersed in solvents are placed into an atomizer to be aerosolized into an inert carrier gas (nitrogen). This aerosol combination of nitrogen and atomized particles are then transported via tubing to the print head and jet nozzle. In the print head, a sheath gas (nitrogen) flow rate is varied to change the shape and force of the carried aerosol

stream through the jet print nozzle. Features as small as 10 μm and as large as 100 μm may be printed using various nozzle sizes and AJP operating conditions [47].

The AgNP ink in this work was Clariant Prelect TPS 50G2, with an average NP diameter of 30 to 50 nm (as listed by the manufacturer). It is comprised of a silver colloid of 50 wt. %, with 10 - 20 wt. % of ethanediol (ethylene glycol) in H_2O. The ink was further diluted before printing with deionized (DI) water by volume with ratio of water:ink::3:1. The dilution was done to decrease viscosity from 15 cP (centipoise) closer to the viscosity of water for the ease of atomization in the ultrasonic atomizer. According to the manufacturer, the ink can be diluted with either DI water or ethanediol. We chose water due to a lower boiling point as well as ease of cleaning which is important for robust AJP operation.

After printing, all samples were dried in an inert−gas oven for 1 hour at 110 °C with nitrogen included to allow drying with reduced oxidation of the specimen. Samples were allowed to cool down for 60 min before removing from the oven at 40 °C or less. Drying was done to allow for proper evaporation of solvents to reduce the likelihood of cracks and delamination of films [48, 49, 50, 51]. All samples were stored in a vacuum desiccator to limit moisture and oxygen intake prior to the next step in processing.

2.3.2 Flash Sintering System

A simple optical flash sintering system was assembled using components purchasable through common suppliers. It consists of a high voltage DC power supply, a capacitor bank allowing for 1000 J or greater, a germicidal Xenon (Xe) flash lamp, a 10 kV auto-transformer to trigger the arc lamp. Fig. 2.1 illustrates the flash sintering system setup.

The process for exposing a specimen for UV flash sintering was maintained with the following control parameters: constant flash distance (h) no greater than 35 mm, single flash exposure, and consistent energy discharged. Irradiation energy was measured to be the same for each sample using a Coherent FieldMaxII digital power/energy meter. With a 2 inch diameter filter, the exposure measured 1.120 J at a 90-degree angle from various distances in front of the Xe lamp. Distances

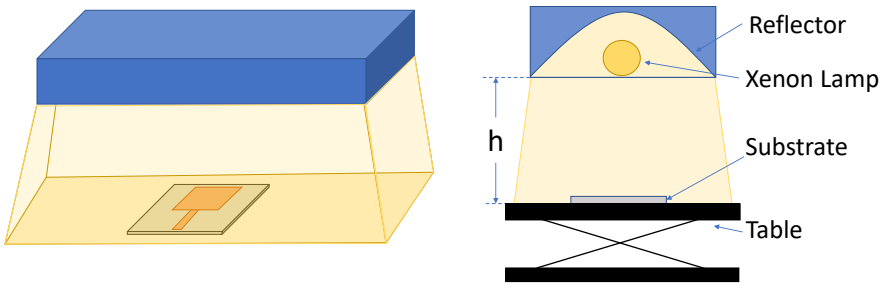

Figure 2.1: Illustration of the flash sintering system.

further than 35 mm did not yield conductive samples. Repeatable measurements were made this way, giving an estimated minimum amount of energy that is applied to a specimen during a single flash. Because of the inability to measure a direct exposure to a power meter, it is unknown how high of a dose of energy a sample receives. Other studies have shown that the pulse time and peak power are important controls for thermal dosing [40, 52, 41]. Here, the peak power was fixed and the dosage was controlled by varying the distance between the sample and the lamp. During the discharge of the capacitor bank, roughly 1800 J is released through the flash system. It is currently unknown how efficient the system is at delivering power to the specimen versus the energy lost due to the various components of the system.

2.3.3 Thermal Sintering

As a comparison to flash sintering, thermal sintering of the samples was also carried out and reported in this paper. Thermal sintering has been the most widely used method to achieve good conductivity from AgNP inks regardless of a deposition technique. Thermal sintering can take place with simple equipment such as a hotplate, convection oven [53], inert-gas oven, or vacuum oven [54]. Here, an inert-gas oven was used for thermal sintering of samples. A Yamato DN411IE Inert Gas Forced Convection Oven was used to sinter AgNP ink samples at 190 °C for 5 hours with a flow rate of 5 SCCM nitrogen mixed to limit oxidation of samples. Experiments showed warping and heavy discoloration of the LCP substrate with prolonged exposure to temperatures above 190 °C.

2.3.4 DC Measurements

A Lucas Labs Pro4 four-point probe designed for wafer resistivity measurements using a Keithley 2400 source meter was used for rapid and accurate measurement of conductive samples. The probe pin pitch is 1.588 mm, allowing for a square specimen of 5 mm x 5 mm minimum size to be measured. This type of resistivity structure was chosen to efficiently print many samples with the AJP. Step height and average thickness of a sample were determined using an AEP NanoMap 500 stylus contact surface profiler. The average thickness and known area of the square allow for the resistivity (ρ) of the sample to be calculated from the measured voltage and current on the probe station. For accurate thickness measurements, similar samples were also printed on smooth glass substrates under the same AJP print conditions. Resistivity (ρ) can be calculated for a square film of known thickness (t) where the meter output of V/I is seen as resistance (R): $\rho = R * t$. In order to remove the effects of the film shape and distance between the probes used, a correction factor (CF) is multiplied by the resulting value of ρ. The conductivity (σ) of a sample is the reciprocal of its resistivity.

In order to verify measurement accuracy, the same resistivity geometries were patterned and etched out of copper clad LCP. Measurements of these geometries verified the correct CF to be used in the 5 mm square samples. Measured conductivity of the 10 mm x 10 mm etched copper standards with this correction factor were between 93 - 98% of the value for bulk annealed copper. With the process used by Rogers Corp. to manufacture the copper, this measurement is reasonable. For verification, a measurement was also taken of a photolithographically etched copper specimen in order to calibrate the measurements made using the same 5 mm x 5 mm squares.

Several papers cited here use different resistivity values of bulk Ag. This thesis uses a value from a NIST standard document, a measured total resistivity of bulk silver to be 1.466×10^{-8} Ω/m at room temperature [55]. The conductivity of bulk silver is then described as 68.21 MS/m throughout this thesis. Where possible, conductivity comparisons are referred to in Siemens/meter rather than by percentage (%Ag) of bulk conductivity to limit confusion when comparing with other published measurements using different bulk standards.

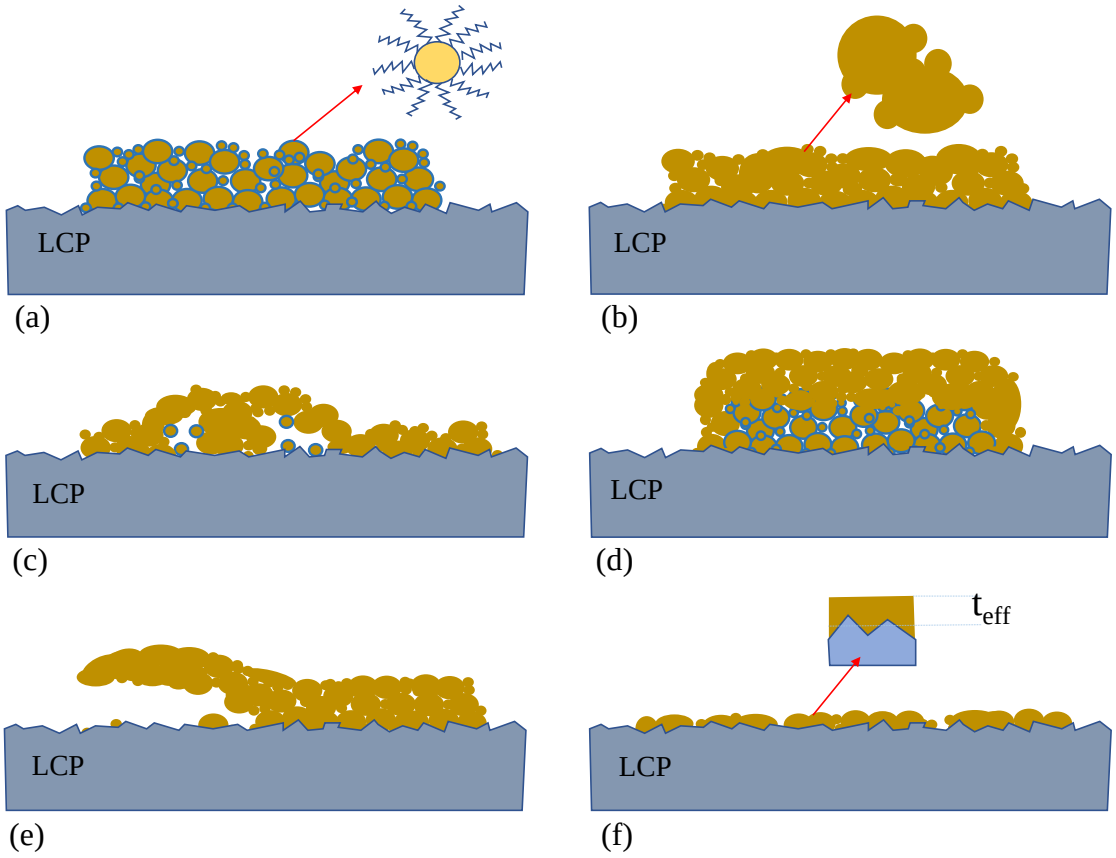

Figure 2.2: Illustration of the flash sintering symptoms. (a) As deposited Ag ink. (b) Fully sintered film. (c) Sintered particles with air-pockets. (d) Sintered outer-layer of particles with wet defects below. (e) delamination of Ag film from substrate. (f) Thin Ag film on rough surface.

In order to make accurate conductivity measurements of the AJP Ag films on LCP substrates, similar DC structures were printed on both smooth borosilicate glass and LCP substrates in the same AJP print session. Films were determined to have poor adhesion to the glass substrate. However, the minimal surface roughness of glass allows for accurate measurement of film thickness. Based on film thickness from glass substrates and four-point probe measurements from LCP substrates the conductivity of the film was calculated.

2.4 Measured Results: Physical Properties and Conductivity

Figure 2.2 shows an illustration of physical properties of the films observed with and without drying steps taken with AJP AgNP ink. Fig. 2.3 shows microscope images of the various results. Films prior to sintering show a darker appearance in color and may exhibit a sheen on the surface

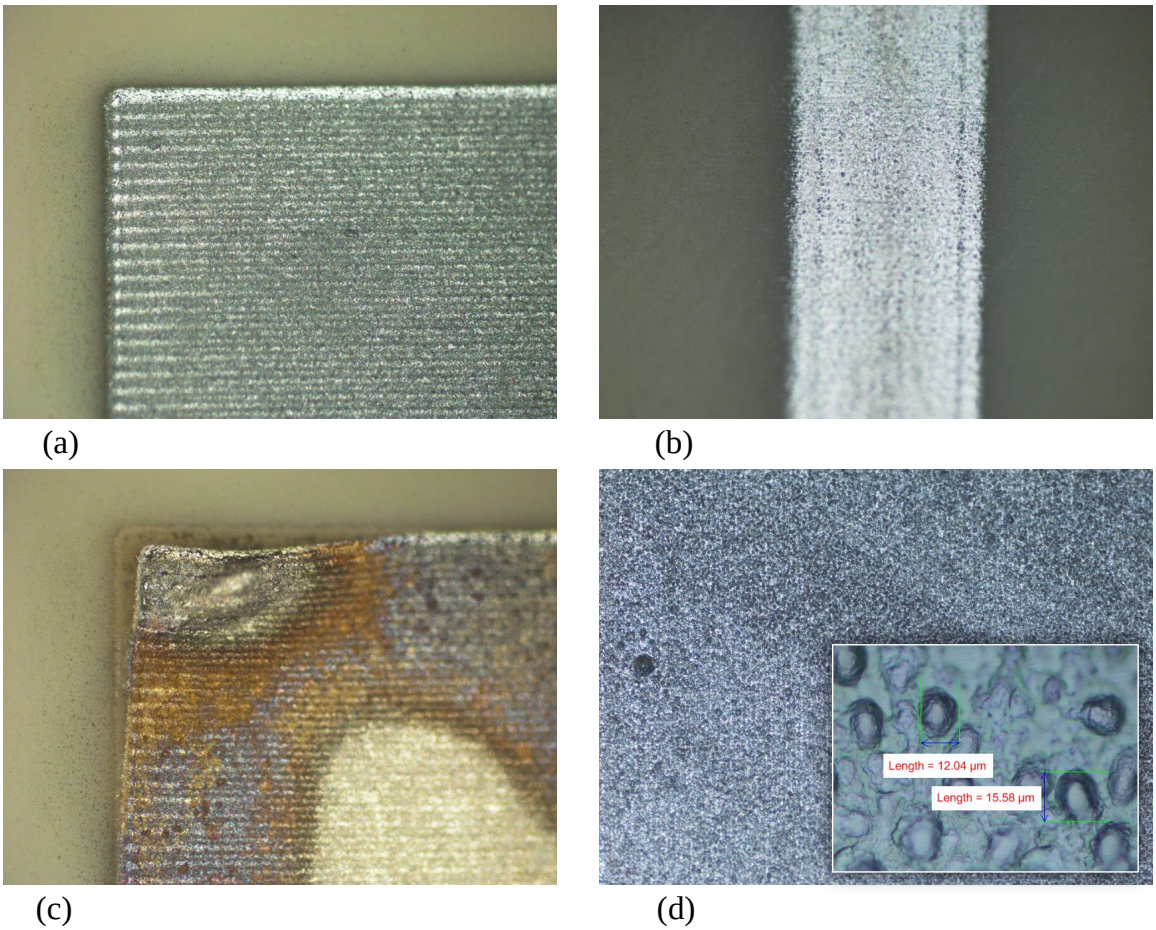

Figure 2.3: (a) Wet AJP Ag ink. (b) Flash UV sintered AJP Ag ink. (c) Delamination of Ag ink under flash UV sintered layers. (d) Bubbles formed under Ag ink during flash UV sintering.

(Fig. 2.3a). AgNP ink that has been properly sintered shows a condensed pattern of particles that are more tightly bunched together and become more reflective (Fig. 2.3b). Delamination can occur with features that did not adhere well to the substrate. This occurs when the deposited film is not sufficiently dried before exposing to UV flashes. Local blisters can also occur when the film is not properly dried, and this leads to darker oxidized spots due to super-heat (Fig. 2.3c). Stress delamination can occur on some corners and small features such as transmission lines, where there may be less surface contact area between the Ag film and the substrate. Other defects as a result of inadequate drying are bubbles and blisters formed between printed layers, leading to a “popcorn effect" (Fig. 2.3d). Proper drying of the AgNP ink requires the reduction of the solvent from the ink in order to promote adhesion and reduce defects in the fabricated circuit. This step is not fully

necessary for oven sintering when a slow ramp in temperature is done (10 °C/min.). However, to be consistent in comparison of results between oven and UV flash sintering, a drying step was carried out to remove moisture from the ink for both techniques. To avoid oxidation of silver film, all drying was carried out in nitrogen atmosphere.

Both the DC and RF measurements were performed on films sintered using the two techniques, flash and thermal. To minimize any variation in film deposition using AJP, all samples were deposited under similar conditions and all samples were dried under similar conditions. Both DC measurements and physical analysis was carried out on films that were flash sintered.

2.4.1 Flash Sintering

Key parameters that were determined to affect the properties of the films are surface roughness of the substrate, thickness of the deposited film and optical exposure power. These parameters were studied and are discussed below.

2.4.1.1 Exposure and Film Thickness

Sintering of films under UV flash was carried out for film thicknesses ranging between 0.5 μm to 5 μm. The samples were initially placed 45 mm in distance from the lamp. Once dried, the printed Ag sample was exposed directly to UV in the optical flash system a single exposure at a time. From the first measurements it was determined that the optimal thickness for flash power penetration was approximately 1 μm with 2 μm as the absolute maximum for the Clariant AgNP ink. Thicker films (delta of $>$1.5 μm) had poor adhesion to the substrate and also led to poor conductivity. This was determined to be due to poor penetration of the UV light into the film. Fig. 2.5 shows the Scanning Electron Microscope (SEM) images of 1 μm thick silver films on a silicon (Si) substrate before and after flash UV exposure. SEM images show that thin films of AgNP ink can become discontinuous after flash UV exposure and some areas even ablate if adhesion is poor. Table 2.1 lists the measured conductivity of silver films deposited in layers on LCP. Each layer was treated (exposed) with single or multiple flashes. The sample was allowed to cool down

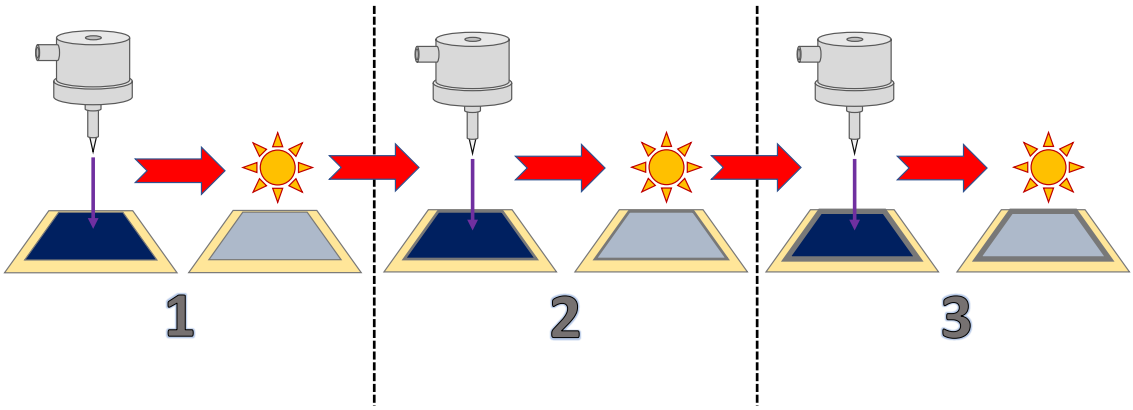

Figure 2.4: Demonstrated process to achieve highly conductive samples of AgNP ink. Printing and sintering is repeated with thin layers until desired thickness and conductivity is achieved.

to room temperature between the flashes. It can be noted that the conductivity does not improve significantly as a function of number of flashes, however repeating the flash and print process did increase conductivity (see Fig. 2.4).

Since the sintering of nanoparticles is closely tied to the magnitude of photonic heating which depends on the shapes and densities of deposited nanoparticles [39, 42], it is reasonable that thicker films saturate in response to further flashes. This happens as the thin sintered layer loses its thermoplasmonic interaction and less heat is generated during flashes, the light does not penetrate deeper to further heat the film. To overcome this challenge, the power in the first flash can be increased or the film thickness can be limited based on the available power. Increasing the initial pulse is also limited by the damage threshold of the sample.

It was also noted that thin films on LCP substrate had poor effective conductivity, see Table 2.1. LCP has an average roughness of 0.5 μm and peaks of 1 μm. This leads to variation in film thickness across the substrate as depicted in Fig. 2.2. To achieve thicker conductive films, to meet the challenge of surface roughness and thermoplasmonic effect, a multi-layer deposition technique

Table 2.1: Correlation of DC conductivity versus number of flash exposures on AJP deposited AgNP specimen.

Layer	Exposure	Thick. (μm)	σ (MS/m)	% Bulk (Ag)
1	1	0.889	0.17	0.25
2	1	1.247	0.44	0.65
2	2	1.247	1.24	1.81
3	1	1.969	1.75	2.56
3	2	1.969	1.84	2.7
3	3	1.969	4.96	7.27
4	1	2.436	6.93	10.16
4	2	2.436	7.12	10.44
4	3	2.436	8.03	11.77

was followed. Here, each layer was dried and flash sintered before the deposition of the next layer. The surface morphology of the final AgNP ink deposit layer was measured to be less influenced by the surface of the substrate, and instead solely by the deposition pattern and layering done by the AJP. Layers following the same printing pattern and flow rates exhibit a “corn row" effect with consistent peaks and valleys in the final layers. In order to overcome this effect, 90-degree rotations in print patterns were also made to reduce overall surface roughness and achieve planarity in the final layers of samples. Average surface roughness $<$0.3 μm was achieved consistently on LCP substrates for two or more layers.

The distance from the flash tube to the surface of sample was highly critical for the preferred amount of energy transferred. Too close to the conductive ink and the particles ablated from the substrate (Fig. 2.5, right). Too far from the conductive ink, and single or double exposures did not induce enough energy to sinter the NPs. In order to fix the distance from the flash tube, an adjustable table was placed in the exposure drawer of the flash system with a height determined by successive experimental data. Starting from 45 mm, an optimal distance of 35 mm was determined to provide good conductivity with a limited number of flashes. Table 2.2 shows the measured conductivity of films exposed under this optimal setup, and this distance was used in all subsequent experiments. With these refined and optimized parameters, the highest conductivity of the samples

Table 2.2: Optimal exposure distance and number of flashes for conductivity.

Layer	Exposure	Thick. (μm)	σ (MS/m)	% Bulk (Ag)
1	1	1.312	7.5	11.04
1	2	1.312	8.2	11.96
2	1	2.239	3.4	5.04
2	2	2.239	13.2	19.36
2	3	2.239	12.5	18.36

Note: Effect of surface roughness is not accounted in these calculations.

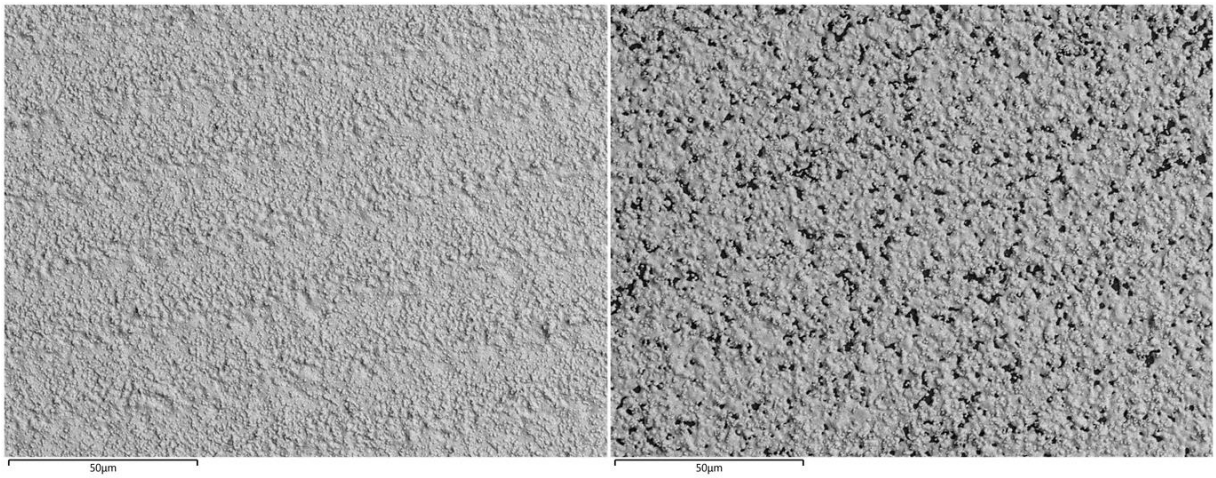

Figure 2.5: SEM images of as-printed (left) and UV Flash Sintered (right) AJP Silver NPs on Si.

measured to date was 1.48x10^7 S/m (roughly 21% bulk Ag, Table 2.3).

The total amount of energy that a AgNP film can be exposed to has its limitations. Too few exposures yielded poor conductivity, while too many exposures lead to high resistivity due to ablation, cracking, or delamination. For example, the conductivity of a 2 μm layer (delta of 0.927 μm atop the first layer) of AgNP ink on LCP (Table 2.2) was found to be 3.44 MS/m (5% bulk Ag) with a single flash exposure. After a second exposure it measured 13.2 MS/m (20% bulk Ag). Additionally, a third flash damaged the film, forming microcracks, and the conductivity reduced to 12.55 MS/m (19% bulk Ag). The number of exposures before damage occurs depends on thickness of the conductive ink as well as the substrate characteristics.

With optimized flash sintering, the brief period of exposure to high intensity energy the damage to the substrate material can be minimized. This reduced exposure time is especially helpful for

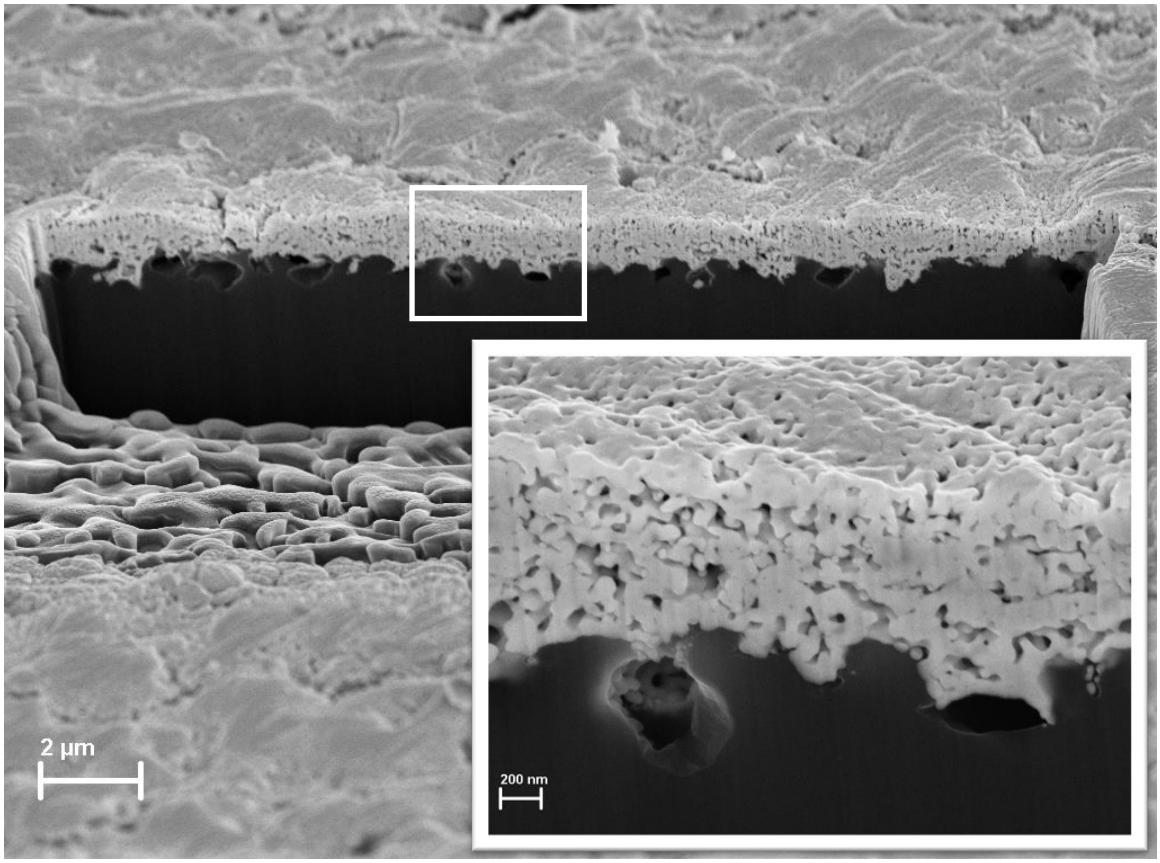

Figure 2.6: Cross-section SEM image of UV Flash Sintered AgNP ink (light grey) on LCP (dark grey).

materials that have strong absorption bands in the UV spectral region. Here, no damage to LCP substrate was noted under multiple flashes. Using a Carl Zeiss Auriga dual column Focused Ion Beam (FIB) – Secondary Electron Microscope (SEM), cross-sectional image of the sintered film was taken, see Figure 2.6 and 2.7. Such images allows for much better understanding of the underlying layers of Ag nanoparticles [56, 57, 58]. It can be noted that the film is uniformly sintered in depth. Also, the sintered film is porous, which leads to reduced conductivity. Also, the deposited film is self-planarizing on the LCP substrate. Figure 2.6 shows a closeup view of sintered Ag cluster. It shows that the nanoparticles are fused together in a tight arrangement. The porosity is only present between these large clusters.

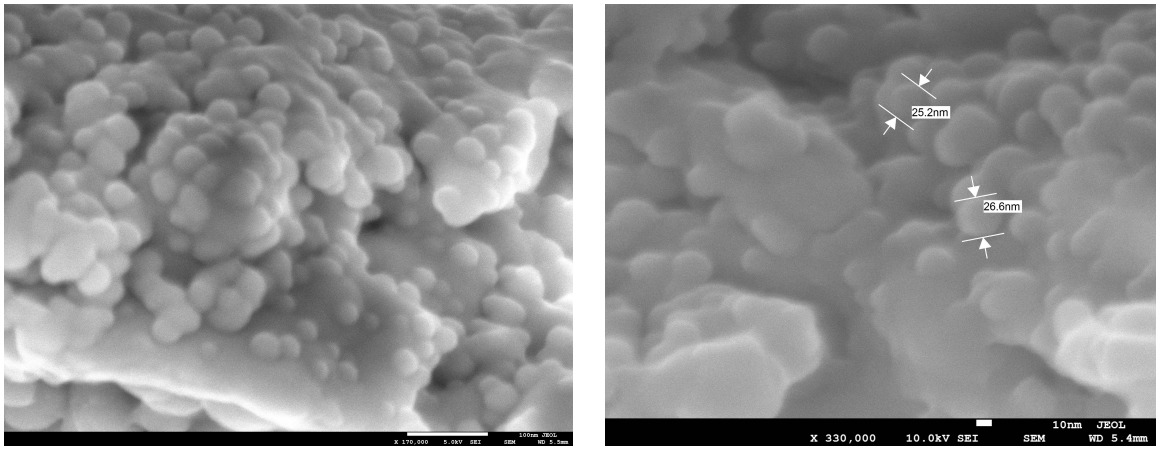

Figure 2.7: SEM images of AgNPs sintered into tight clusters with average 30 nm diameters (left: X 170,000, right: X 330,000).

2.4.1.2 Surface Roughness and Conductivity

As seen in Figure 2.6, LCP has a large surface roughness. Although this roughness helps improve the mechanical adhesion of the Ag particles to the substrate, it is detrimental to the effective conductivity of the film. Conductivity of the silver film is expected to be higher if this roughness is accounted for in the calculations. For example, the first exposure showed 5.04% bulk Ag with 2.24 μm of thickness; it will be 6.5% bulk Ag when the thickness is adjusted to 1.74 μm due to surface roughness. Similarly, the measured 18.36% bulk Ag will be closer to 23.6% bulk Ag. More accurate step-height and conductivity measurements can be obtained if the ratio of metal thickness to surface roughness of the substrate is large. This was not practical, as aerosol-jet printing deposits only a few microns at a time of ink, having a ratio on average of 3:1 or 4:1 aspect. The estimated conductivity of the optical flash sintered AgNP ink is expected to be greater than 30% bulk Ag conductivity if effective thickness is reduced by 0.5 μm, which is due to surface roughness. After FIB analysis, it was determined that the profiler estimate of the AgNP film thickness introduces an unknown that can only be solved with a cross-section measurement.

Table 2.3: Comparison of DC conductivity against reported results.

Reference	Sintering Method	Substrate	$\sigma(MS/m)$
[53]	Oven (300 °C)	Polyimide	25.0
This Work	Oven (190 °C)	LCP	15.4
[47]	Oven	LCP	12.0
[45]	Hotplate (180 °C)	Resin	10.0
[59]	Photonic (N-IR)	Paper	25.0
[31]	Optical Flash	Polyimide	20.0
[44]	Optical Flash	Glass	17.9
This Work	Optical Flash	LCP	14.8
[43]	Photonic (N-IR)	Paper	10.0
[22]	Optical Flash	PET	9.4
[33]	Optical Flash	PET	6.5
[24]	Electrical (DC)	Photopaper	37.0
[37]	μ-wave	PEN	16.9
[35]	Plasma (Ar/SF6)	Resin [60]	5.1
[27]	μ-wave	Polyimide	3.3
[30]	Laser	PEN	3.3

2.4.2 Thermal Sintering

Thermal sintering of the AgNP ink was chosen as the best comparison between commonly used techniques and this optical UV flash sintering method. High conductivity yields can be achieved with high temperatures on a hotplate or in an oven [61]. Because of the desire to use a low loss RF substrate for this comparison, an inert-gas oven was used for the experiment. By using an inert-gas such as nitrogen in the oven for sintering, oxidation was reduced for 5 hour exposure to the 190 °C temperature environment. The temperature chosen was also due to the low glass transition temperature (T_g) of the LCP substrate [62, 63], which exhibited warping and discoloration at temperatures greater than 200 °C. Rogers Corp. lists the melting point for ULTRALAM 3850HT substrate at 330 °C, which we maintained with substantial margin. After thermal sintering, the specimen were gently cleaned using a hi-polymer eraser to polish the sintered silver and remove

any oxidation from the conductive films. They were then rinsed with isopropyl alcohol to remove any polymer and organic debris. Polishing the films also verified that the silver nanoparticles adhered well to the substrate surfaces.

Thermal sintered AJP Ag ink showed to have a similar surface morphology to what was measured with flash sintered samples. Surface roughness and thickness per printed layer were also similar using the same printing parameters. The specimen measured 2.0 μm thickness with conductivity of 15.4 MS/m (22.5% bulk Ag), and a possible effective conductivity of 30% bulk Ag with 0.5 μm thickness removed due to surface roughness of the LCP. Figure 2.8 shows FIB milled SEM image of the thermal sintered samples. Thermal sintered films show less porosity than the flash sintered films, this in turn leads to higher measured conductivity. By having a comparable surface roughness and DC conductivity to the flash sintered samples, the thermal sintering method was shown to be a good experimental control for this process. The same processes were repeated for RF structures to demonstrate the differences and advantages between the two.

2.5 Measured Results: RF Circuits

In the literature, a range of high frequency circuits fabricated using different AgNP inks as well as different substrate types has been reported. Table 2.4 lists several high frequency circuits fabricated using AgNPs and their results. The most common sintering method was found to be thermal, with a variety of substrates ranging from Liquid Crystal Polymers (LCP) [20, 47] and Polyimide (PI) [61], to Polyethylene terephthalate (PET) [54], and Pyrex glass [64]. For thermally sintered AgNPs on LCP and PI, the highest frequencies ranged upwards of 210 GHz with maximum insertion losses of 25 dB for filters [20], and insertion losses of 0.366 dB/mm for coplanar waveguide (CPW) transmission lines [61]. For Xe broadband flash sintering, the only publication known at this time used a spraying technique to deposit AgNPs onto PET substrates [22]. The authors of that publication fabricated a 5 GHz coplanar antenna spraying the film with 4 layers which shown a mean thickness of less than 1 μm. These publications set a baseline for expressing this method of optical UV flash sintering of AgNPs deposited by AJP for fine resolution on LCP

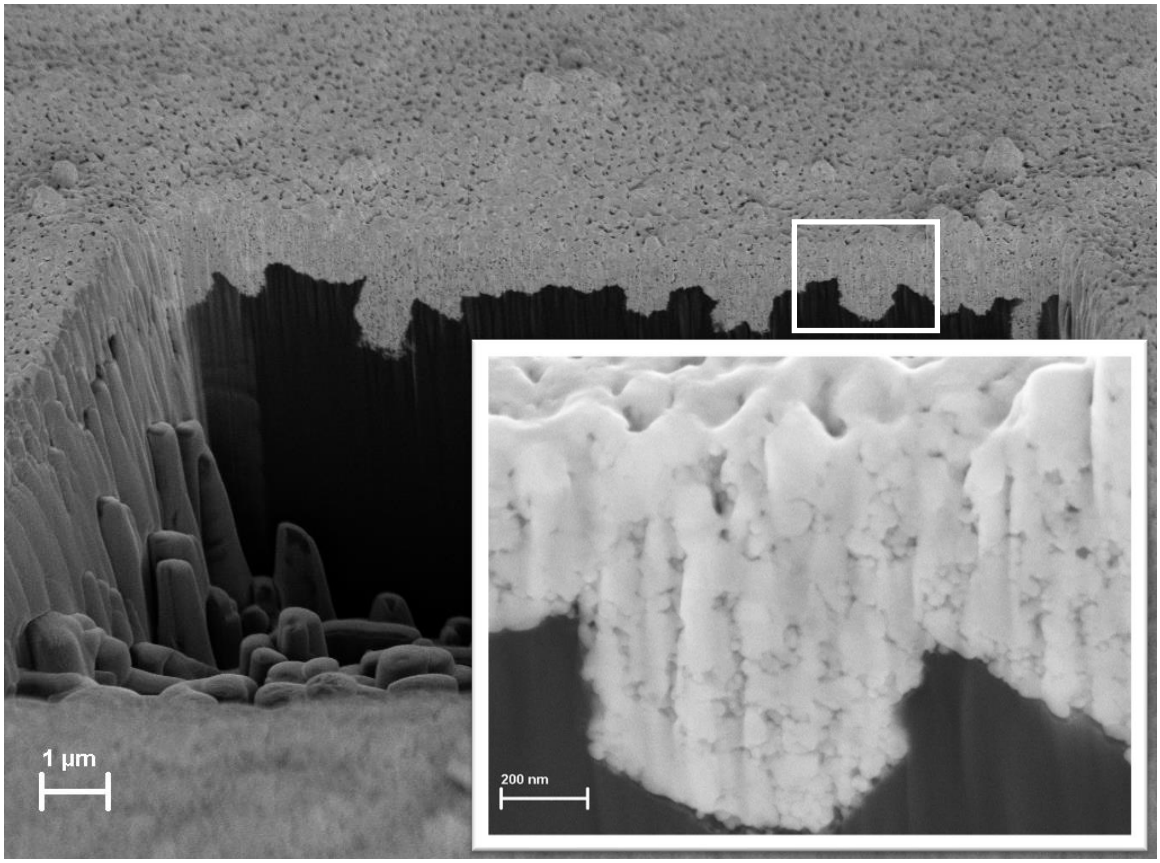

Figure 2.8: FIB cross-section SEM image of Thermal (Oven) Sintered AgNP ink (light grey) on LCP (dark grey).

RF substrates. The frequencies chosen demonstrate useful applications in 5G technologies and mm-wave RF circuits.

In order to draw a direct comparison between traditional oven sintering and the optical flash method described in this thesis, microstrip transmission lines were fabricated on LCP substrates. The sample set for optical flash exposure required twice as many print sessions to achieve the same thickness as the thermal sample set. Once dried and after a second sintering was performed, both sets were measured using a Keysight N5227A PNA Microwave Network Analyzer from 1 GHz to 67 GHz (Fig. 2.9). The AJP fabricated transmission lines were 240 μm width by 34 mm length on 4 mil LCP with a copper ground plane. The measured S-Parameters show a reasonable amount of loss to be expected for a long length transmission line with roughly 20% bulk Ag. Dividing the measured S-Parameters by 34 mm, Table 2.4 shows that at 40 GHz the transmission line had an

Table 2.4: RF Structures using AgNPs

Ref.	Deposited	Sintering	Substrate	Ink Formulation	Insertion Loss
Transmission Lines					
This work	AJP	Xe (broad)	LCP	PRELECT TPS 50	0.11 dB/mm @ 40 GHz 0.16 dB/mm @ 60 GHz
[64]	Inkjet	Bake	Pyrex	CCI-300 Cabot	0.162 dB/mm @ 10 GHz 0.265 dB/mm @ 20 GHz
[61]	AJP	Bake 140 °C	LCP Kapton	PRELECT TPS 50	0.366 dB/mm @ 110 GHz 0.546 dB/mm @ 110 GHz
Other RF Circuits: Antennas and Filters					
This work	AJP	Xe (broad)	LCP	PRELECT TPS 50	-11.62 dB @ 16.3 GHz Patch, Gain: 6.69 dBi
[35]	AJP	Ar Plasma	VeroWhite [60]	PRELECT TPS 50	-14.6 dB @ 25.8 GHz Quasi-Yagi-Uda
[54]	Inkjet	Bake 120 °C	PET	Novele IJ-220	-35.49 dB @ 2.49 GHz Multi-band antenna
[22]	Spray	Xe (broad)	PET	Lab made (TGME)	-27 dB @ 5 GHz Patch, Gain: 3.3 dBi
[20]	AJP	Bake 160 °C	LCP	PRELECT TPS 50	-25 dB @ 210 GHz THz Band-stop filter
[45]	AJP	Bake 168 °C	FormLabs	PRELECT TPS 50	-10 dB @ 140 GHz THz Curved Lens filter

insertion loss of 0.11 dB/mm and 0.16 dB/mm at 60 GHz. This demonstrates the comparison of the oven and flash-sintering methods for the same AJP circuits, which yielded very similar results.

Three patch antennas were also fabricated using the optical UV Flash sintering technique as well as three using the oven sintering method described in the above section. While the data showed repeatability for each, the data sets were reduced to one patch of each method to prevent crowding of data in the figure. The patch antennas were measured on a PNA to demonstrate S_{11} at the center frequency from the range of 14 GHz to 17 GHz. The main focus of Fig. 2.11 was to compare how the two sintering methods effected the RF parameters of AJP printed silver nanoparticle ink on LCP substrates which radiate power.

The patch antennas were also fabricated using 4 mil thickness LCP sheets with 17.5 μm copper cladding on the back for ground plane. This design was consistent with the transmission line fabrication. The antenna was designed using Ansoft HFSS simulation software. The antennas were simulated having a resonant frequency of 16 GHz, while using 25% bulk conductivity for the

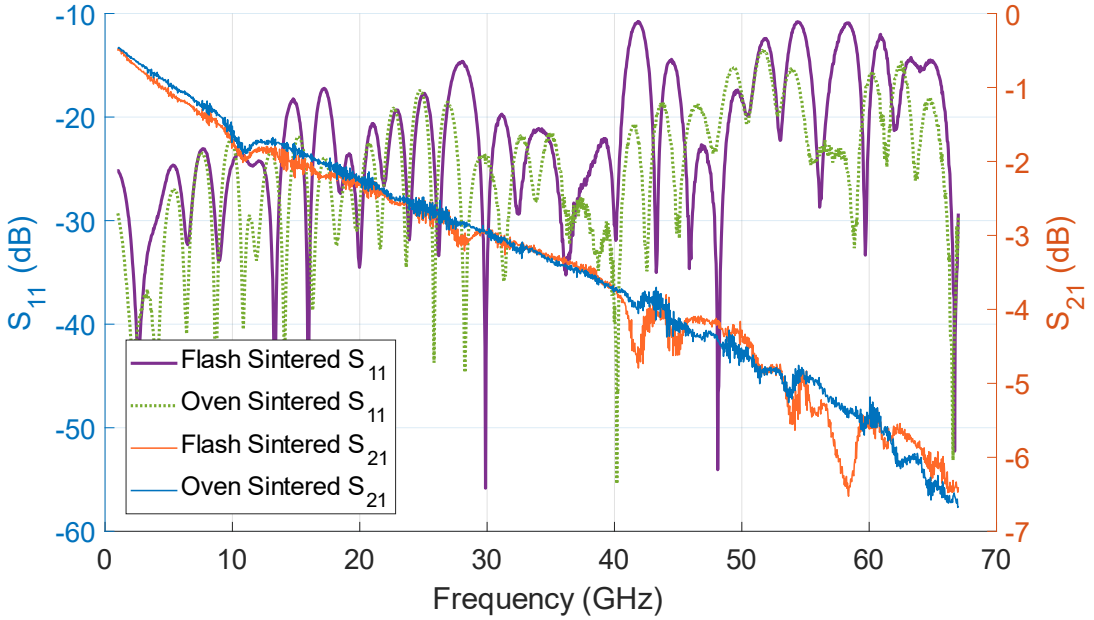

Figure 2.9: 34 mm long microstrip transmission line printed on LCP. S-parameters shown for both the UV and oven sintered samples.

Figure 2.10: Connectorized Ag transmission line on LCP.

printed transmission feed line and patch of antenna. As with the transmission lines, two sets of antennas were fabricated with the Optomec AJP in order to draw a comparison between sintering methods. Using a Satimo Starlab near field measurement system, results of the antenna showed a gain of 6.69 dBi for a single patch antenna which was flash sintered, see Fig. 2.12 and 2.13. Measured S_{11} parameters show that the frequency was 16.3 GHz rather than the designed 16 GHz. This was accounted for in simulation due to a reduced size of the patch antenna parameters by 50 μm on each side. The oven sintered antennas had similar results as the flash UV sintered antennas.

Simulation was adapted to best fit the measured results using a finite conductivity boundary

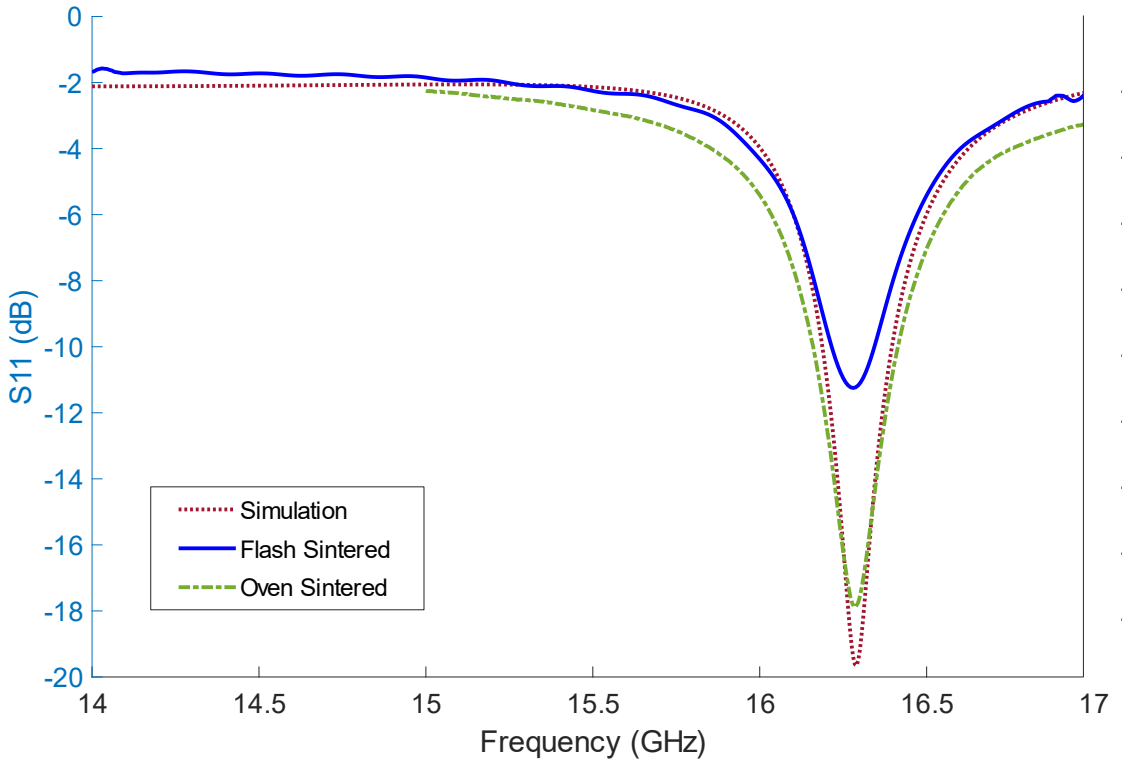

Figure 2.11: S-Parameters of patch antenna sintering comparison.

with 14.8 MS/m (21.7% bulk Ag) and a surface roughness of 800 nm for the patch antenna and feedline, with an overall reduced dimension of 50 μm on each feature. To further increase accuracy of the simulation, an impedance boundary was added for the surface area of the pin contact from the connector (Southwest 1092-01A-6 2.92 mm Female End Launch Connector, Fig. 2.10) using 1 Ω of series resistance to show the effects of pin contact resistance to the printed Ag.

These two additively manufactured circuits demonstrate the usefulness of optical UV flash sintering for RF circuits which require fine patterning on low-loss substrates. This work shows that RF circuits can be fabricated using a combination of AJP and flash sintering without damaging the substrate or reducing its integrity.

2.6 Discussion

A flash sintering technique along with aerosol printing was demonstrated for rapid prototyping of RF circuits. Further studies are needed to determine the optimal power transfer into the

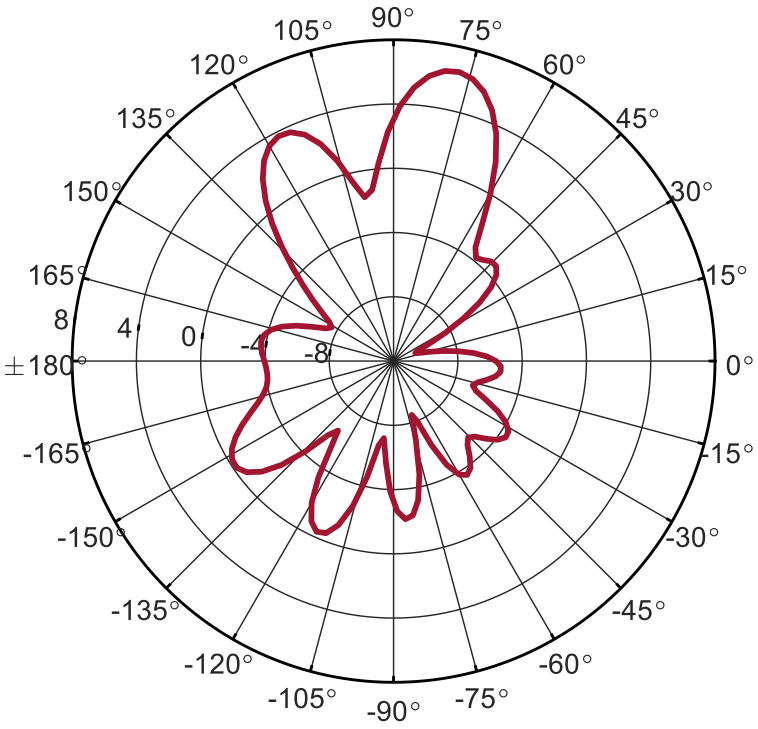

Figure 2.12: Polar pattern of UV sample patch with gain 6.69dBi.

silver film. In particular, it is believed that the power absorption by non-sintered film is higher as compared to partially or fully sintered films due to change in optical absorption properties. While currently unable to investigate the occurrence of the densification process and related photonic heat changes, other studies have shown that particle size and temperature induced by photonic sintering are directly related [65, 39]. In addition, the porosity of sintered film was not fully considered in this work. FIB milled cross-sections of both thermal and UV flash sintering show that the limitation of AgNP ink conductivity can be related to factors of surface roughness, porosity, and particle size. If porosity and surface roughness of the substrate are to be considered in conductivity, the estimated conductivity of the sample is greater than 30% of bulk silver conductivity. Porosity in the films appeared to range from 50 to 200 nm in some areas of measured samples. Bimodal or trimodal particle distribution can potentially be used to reduce porosity. Porosity in the film leads to lower conductivity and also degrades RF performance. Parameters such as porosity and spectral response are closely coupled to the ink nanocompositions and will require unique process

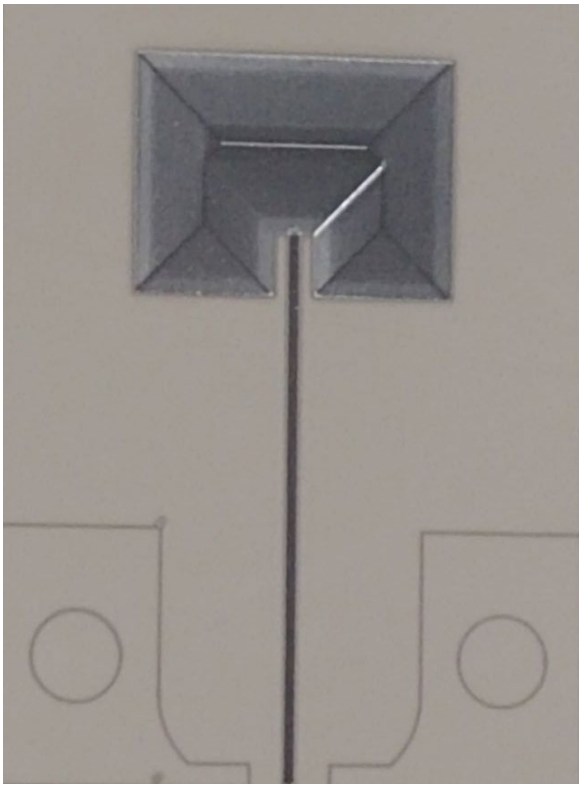

Figure 2.13: UV sintered AJP printed antenna on an LCP substrate.

developments to optimize conductivity versus thermal loading and damage thresholds. It was also determined that the surface roughness of the substrates effects the conductivity calculations. Better models should be used to calculate the conductivity of deposited films that accounts for substrate surface roughness and the porosity of the deposited film. In conclusion, flash sintering of AgNPs is a process which can be further improved and optimized as potential processes for reel-to-reel and other manufacturing techniques to improve circuit fabrication in the future. In brief, detailed material analysis needs to be carried out to further understand the properties of silver ink deposited and sintered using the flash technique.

2.7 Conclusion

A direct comparison between optical (UV) flash and thermal sintering of AJP AgNP inks was made. The advantage of flash sintering is that it is rapid and it can be incorporated as integral part of the AJP system. Similar conductive values and RF performance can be achieved between the two

techniques. DC conductivity values were shown to be comparable for both techniques: 22.5% bulk Ag for thermal sintering, and 21.7% bulk Ag for flash sintering. The flash technique is compatible with sintering of thin layers ($<$1.5 μm thick), and multiple layers have to deposited and sintered to achieve a desired thickness. The primary advantage of thermal sintering is that it allows for processing of many layers ($>$10 μm thick) simultaneously. However, the process time is long ($\sim$1 hr) and the process temperature is high, and thus not compatible with low temperature substrates. The flash technique does not affect the properties of the substrate, which LCP was studied here. Transmission lines operating up to 67 GHz and a patch antenna with center frequency of 16.3 GHz was demonstrated with good RF characteristics.

CHAPTER 3

THICK DIELECTRICS USING AJP

3.1 Introduction

High functional density is highly desired for the next generation of electronics systems. Heterogeneous integration of many semiconductor technologies are needed to meet the need of high functional density systems, esp. microwave and millimeter wave systems. In the open literature, any approaches have been demonstrated to meet the need of heterogeneous integration [66, 67, 68, 69, 70]. This includes integration of different semiconductor technologies on a single chip or a common substrate. For RF systems, a range of semiconductor technologies are needed including Silicon (Si), InP, GaAs, GaN, SiC, etc. bringing all these on a single chip is very challenging and cost prohibitive [67]. Thus, integration on a common substrate is attractive [70].

Along with different semiconductor technologies, many passive elements are needed in the design of a RF system. For example, the RF front-end design requires passive elements such as filters, antennas, directional couplers, etc. These passive elements have to be placed in close proximity to the active elements (e.g., amplifiers, oscillators, switches and detectors). In a typical RF system, the majority of the area ($\sim$90%) is occupied by the passive elements. Thus, it is not economical to carry out RF system integration on a chip and integration on substrates is desired [71, 10]. Apart from component needs, there are many other challenges that needs to be tackled to design a truly high functional density system.

The mechanical compatibility of dielectric materials used for substrates is often a large challenge to meet when it comes to high density fabrication. In an RF system, there is often an intermix of technologies for each device in the RF signal chain. This intermixing of material differences and physical size differences (such as height or shape) requires materials for encapsulation, filling, dielectric bridging, and interconnect supports to be uniquely tailored to the application at hand. Different substrate chemistry supports different expansions and contractions of materials under

thermal stress, leading to difficulties in fabrication approaches.

For RF circuits, often choices of dielectric materials can be made by finding the desired permittivity, loss tangent, and thermal capacity. Material choice for substrates can have many factors not limited to: coefficient of thermal expansion (CTE), heatsinking methods, external DC biasing components, environmental requirements (moisture intake, chemical resistance, thermal shock, flexibility), and material adhesion. CTE mismatch in a hybrid circuit is a very real occurrence, not just with differing technologies being integrated, but also where material interfaces occur with 3D printed components, ramps, interconnects, and packages. As temperatures increase during fabrication steps or during environmental interactions, differing CTE properties will expand or contract, causing breaks in 3D printed sections of circuits.

Finding the appropriate intermediate materials for dielectric substrates can also cause difficulty with dispensing the raw materials to develop the high density circuit. Most commonly this difficulty is found in the viscosity of the material precursor or uncured polymer resin. The difficulty with using low viscosity materials which may have other highly desired properties becomes how to dispense large quantities in short periods of time with high resolution. This is challenging, as spin coating fabrication process often used on wafer level packaging will only yield very thin films after many processing steps. 3D printing becomes the obvious choice for low viscosity materials, but the resolution capability is lost with spillage of the material as it flows easily without constraint. In order to overcome this challenge, a dam and fill process can be utilized for fabrication of thick film dielectrics tailored with high resolution to a vast number of substrates and surfaces.

To meet all of the above challenges, here a new process is introduced, referred to as a dam and fill process. The dam and fill process can take advantage of minimal spacing between components, and allow for endless design potential. One major advantage of fabricating the substrate around the devices is that the substrate can be formed on a carrier surface for shape, and then later removed by using a release agent. This substrate-less fabrication step allows for planar, level interconnects between devices of differing technologies and thickness. All supporting components such as DC bias networks can be tightly bound to the active device and form a unique package that is easily

fabricated for custom applications. By utilizing these methods, high density interconnects can be achieved more easily with minimal space placement of devices. Shortest distance interconnects allow for the elimination of parasitic losses introduced through wire bond interconnects. This method allows for the custom tailoring of dielectrics to all surrounding materials regardless of the viscosity of the dielectric. Benzocylcobutene was utilized here due to its highly desired properties, of which low viscosity has caused problems with accurately dispensing before utilization of this method. Designs also permit the tailoring of dielectric to the metal interconnects and contacts being used, or for integration with other dielectrics with various thermal processing requirements.

3.2 Overview

Selective dielectric deposition using a dam and filling process utilizing additive manufacturing (AM) is presented in this thesis. It is used here for the design of millimeter wave (MMW) circuits. For this process, Aerosol jet printing (AJP) is utilized for the building of dams and filling with polyimide and benzocyclobutene (BCB), respectively. Dielectric islands with different thicknesses and high aspect ratios can readily be deposited with good print resolution. Fully AM printed patch antenna (center frequency = 94.08 GHz) was demonstrated on these dielectric structures using silver conductive ink also deposited using AJP. Embedded circuits are discussed with a demonstrated 0 dB attenuator die placed in liquid crystal polymer (LCP) cavity filled with BCB. Building upon each of these circuit fabrication techniques, a unique substrate-less packaging approach was demonstrated with the use of lift-off post processing to form a self-packaged chip-to-chip system. Details of design, fabrication, and measurement are presented and discussed. This process is attractive where a mix and match of substrates are desired in the design of high density MMW packages.

3.2.1 High Density Heterogeneous Integration

Wireless systems are growing exponentially to support larger and more diverse applications ranging from sensor networks for smart integration to telemedicine and distributed data storage. From a

systems integration point of view, it is economical to build large systems out of smaller functions. This technique leads to the construction of a variety of products both rapidly and economically [71]. These smaller functional components can be separately designed, fabricated and tested, and packaged. Heterogeneous Integration will be the key technology direction to meet the future challenges of MMW circuits and systems of 5G and 6G communication.

Packaging techniques that allow the integration of active and passive devices with arbitrary location and rotation are needed to meet the need of the next generation of RF systems. Additive manufacturing (AM) provides the flexibility to meet this challenge. Recently, AM has attracted the interest of RF circuit and systems designers [5, 72, 73, 74, 6]. Among the many AM technologies, AJP is attractive as it allows fine line printing on planar and non-planar surfaces from a large stand off distance from the surface and offers tailored alignment [47].

Fine line resolution is necessary for the fabrication of MMW circuits. One of the major challenges with AJP is that there is a trade-off between resolution and material deposition speed. AJP is commonly used in the deposition of thin films with high resolution printing or on non-planar surfaces which traditional printing methods are incompatible. Many layers are deposited to achieve thicker films and this requires long processing time [75]. Here, we propose a new processing technique that allows the deposition of thick dielectric regions, and an approach to embed active devices within the dielectric to meet the need for high functional density RF systems.

3.2.2 Dielectric filling (Chip Scale Packaging)

Fig. 3.1 shows this approach for selective dielectric deposition using a dam and filling process utilizing AJP. AJP is used for both building of the dam and filling with polyimide (PI) and benzocyclobutene (BCB), respectively. Dam and fill encapsulation is commonly employed in chip scale packaging (CSP) [76, 77, 78, 79, 80]. Benefits of this process include package miniaturization, planar surfaces, rapid prototyping, and use of a common tool for packaging of different chip sizes. This process allows the use of low viscosity liquids that can readily flow around the chips and minimizes the formation of voids. Damming provides a barrier that keeps the dispensed low

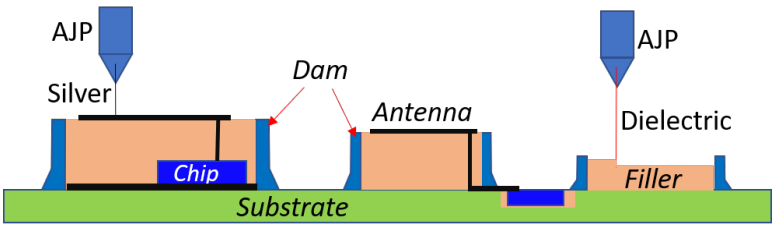

Figure 3.1: Selective dielectric deposition using a dam and filling process.

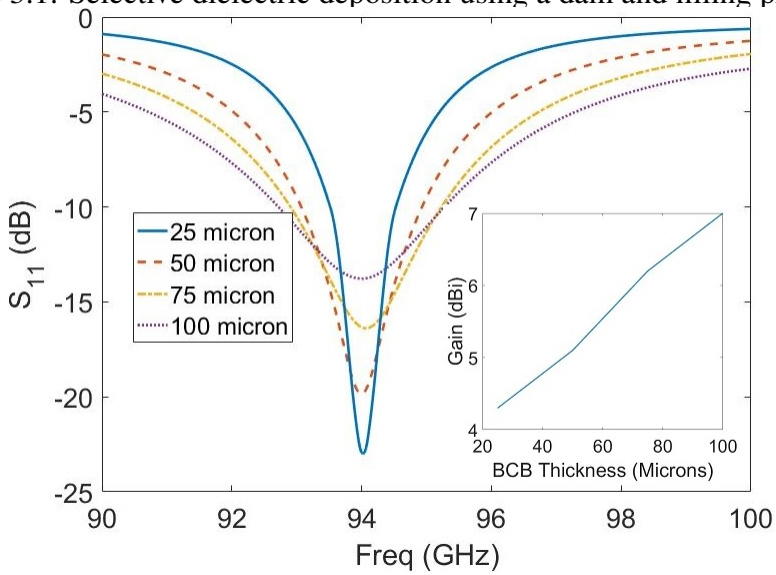

Figure 3.2: Simulation of 94 GHz patch antenna on BCB with thickness from 25 to 100 μm. Superimposed gain at resonance.

viscosity fill liquid in a bounded region. This process was adopted here to package the chip and to form dielectric islands that can be used to form passive MMW circuits. The flow rate can be significantly increased during the filling process, and thick fills can be printed and cured in one session.

This technique allows the design of novel RF circuits and systems, and provides a significant benefit in antenna design. As an example, Fig. 3.2 shows the simulated results of a W-band patch antenna on different thickness BCB. From scattering parameters, it can be noted that the gain and bandwidth of the antenna can readily be tailored using dielectric thickness [81].

3.2.3 Thick Structures with varying heights

Utilizing the dielectric filling method, structures of thick dielectric films can be fabricated with varying heights on the same substrate. This allows for custom tailored films without the use of tedious, complex, and expensive mask techniques to build thick substrate and 3D structures with dielectric materials. One major benefit of this process is that it can be used to fabricate thick dielectric films for antenna substrates to allow for improved gain or tailored multi-dielectrics. Antennas built upon thick dielectric have better efficiency and higher gain than with thin or a base substrate.

Another application would allow for complex geometric structures with step profiles to form waveguides, low-loss air cavities, and horn antennas with the substrate materials being 3D printed [82, 83]. Such devices shown in Fig. 1.4 could be fabricated with much less difficulty by printing stepped dams of dielectric material and filling them with low-loss dielectric in layers, allowing for more control and custom processing of individual layers and sections of the board rather than an entire layer of LTCC fabricated at a time.

3.3 Dam Process

Polyimide (PI) is commonly used in many electronic devices as a robust dielectric layer. However, polyimide has a high moisture absorption rate which increases the risk of delamination during thermal processing, and was therefore used as a barrier material rather than a fill material [8]. The high viscosity of PI ink allows for ease of fabrication of 3D structures. With the use of a 100 °C heated platen, the drying time is significantly reduced during printing. The deposited film quickly dries and allows further build up of layers to form dam structures for containing of lower viscosity materials.

Premixed Sigma Aldrich Poly(pyromellitic dianhydride-co-4,4'-oxydianiline) polyamic acid (PAA) dissolved in N-Methyl-2-Pyrrolidone (NMP) was used. The material was further diluted by weight to achieve between 5 - 7% of PAA to NMP. Using 300 μm size AJP nozzle, feature widths of 50 μm and 400 - 500 nm thickness per layer were created. For fine features, the use of a 200 μm size print nozzle was able to yield 30 μm widths with 600 - 700 nm thickness per layer.

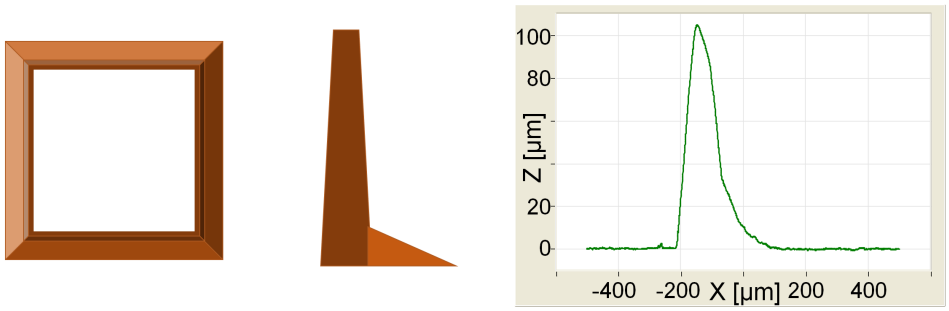

Figure 3.3: (a) Top-down view of dam; (b) Cross-section view of brim and wall; (c) 2D scanned profile of the dam wall.

3D printing using Fused Deposition Modeling (FDM) utilizes a "brim" printed to the base of an item to enhance mechanical properties and improve adhesion. Similarly, a brim was used here to improve adhesion and to support a high-aspect ratio walled dam. Fig. 3.3 demonstrates the resulting cross-section and top-down views of a printed dam. An example profile of a dam is also shown in Fig. 3.4.

Support structures are often removed from 3D printed parts; here, this structure is made an integral part of the final design and not removed. The dam was constructed with a 50 μm line width feature and supported by printing a brim outside with a 5:1 aspect ratio. Fig. 3.3(a) illustrates how the printing of a dam with 1 feature width should have 5 feature widths at the base to form the brim. The brim was printed with multiple layers to form a gradual slope. Printing the brim and the wall in a single print session significantly improved the adhesion of the PI layers to each other. Without the brim, samples showed good structural integrity during printing but would break due to stress induced during the curing of the fill material.

3.3.1 Filling Process

B-staged bisbenzocylobutene (DVS-bis-BCB; BCB), Cyclotene 3022-35 from DOW Chemicals, was selected due to its low viscosity of 15 cP at room temperature. The dielectric constant of 2.65 and a dissipation factor (DF) of 0.0008 - 0.002 are highly desired for RF and MMW circuits [84, 85, 86, 87]. BCB also has good chemical and mechanical properties [88], which can be used

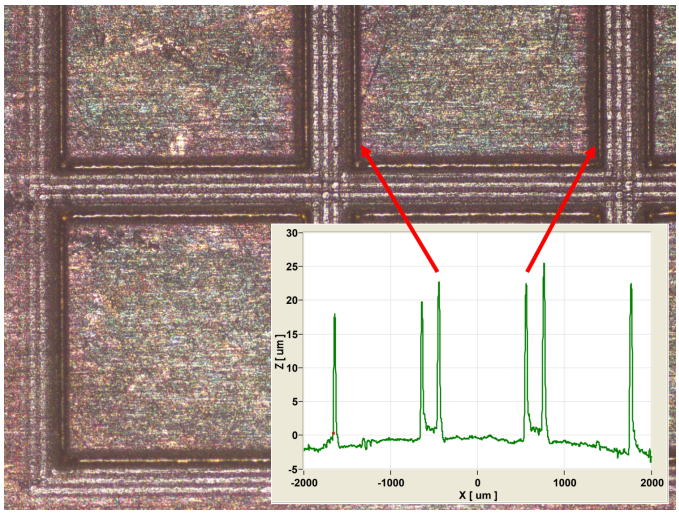

Figure 3.4: Fabricated cells for varied height dielectric dams, no fill material placement in this step.

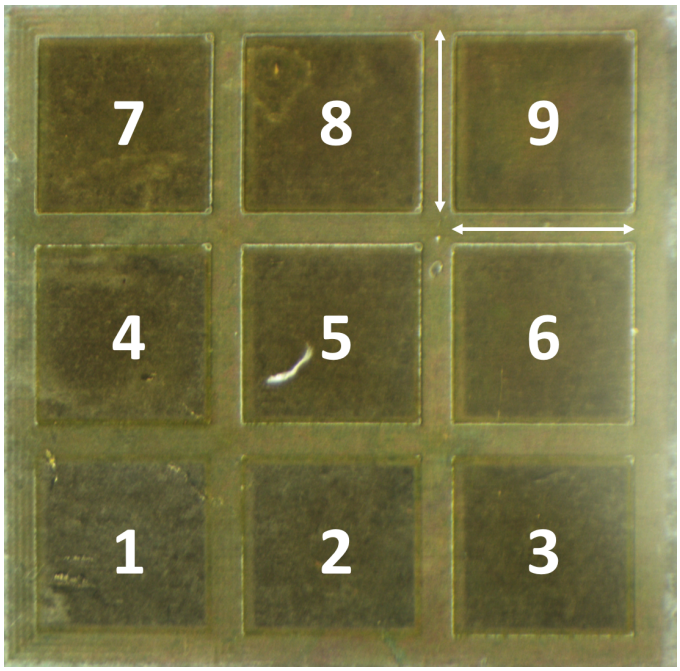

Figure 3.5: Dielectric array with varying BCB thickness, 5 μm to 45 μm (1 - 9 layers)

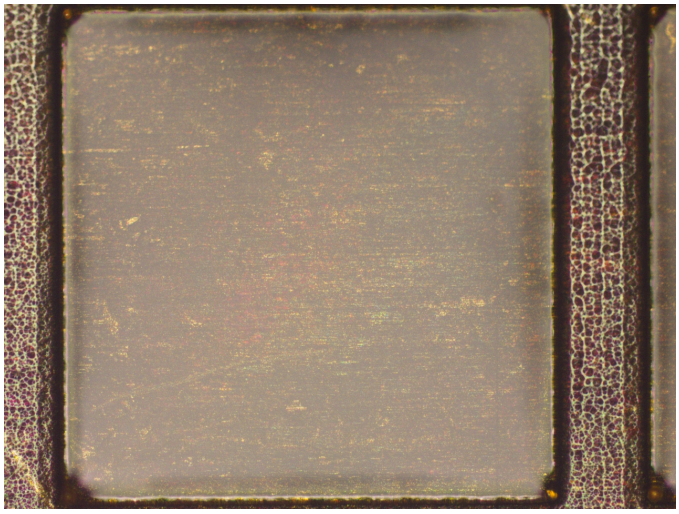

Figure 3.6: 3 mm x 3 mm Dielectric dam fill with 45 μm BCB thickness.

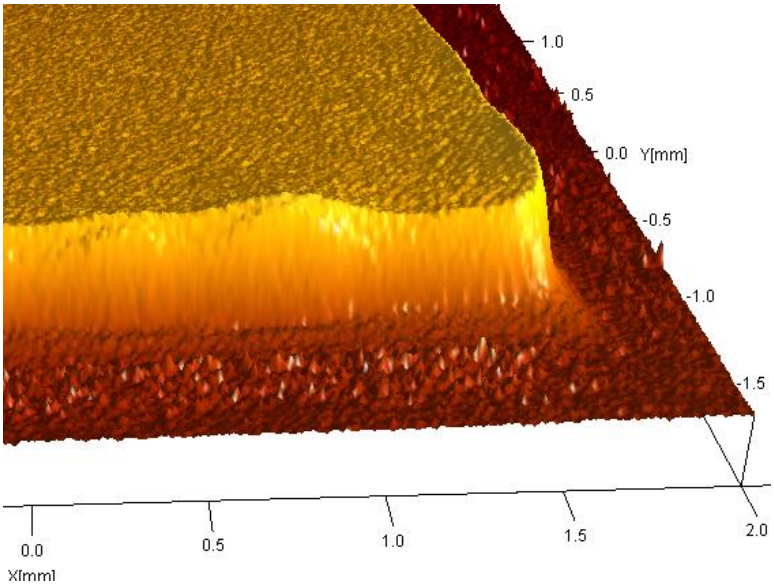

Figure 3.7: 3D profile of an example structure.

for encapsulation or passivation, and to form air bridges in planar inductors.

BCB was printed with the platen heated to 50 °C to remove some solvent from the ink. BCB was printed with a 200 μm nozzle yielding 5 μm thick layers per pass after curing. Multiple layers were first deposited and then dried in one step on a hotplate in the atmosphere set to 100 °C for 10 minutes. Soft cure was performed at 200 °C for 5 hours in an inert gas oven with nitrogen. A hard cure was done at 250 °C for 3 hours under the same conditions. BCB flows during soft cure leading to self planarization [89]. In contrast, self planarization is difficult to achieve using AJP printed PI films [87]. Fig. 3.5 shows an array of BCB filled dielectrics with heights ranging from

5 μm to 45 μmm, increasing by 5 μm per layer.

3.4 Conductor Deposition

Silver nanoparticle (AgNP) ink from Clariant has been commonly used in the fabrication of RF circuits using AJP [90, 35, 20, 61, 47, 91]. PRELECT TPS 50G2 ink is an AgNP dispersed in water with a 50 wt% of silver colloid. Ink preparation for printing in the UA consisted of dilution below 10 cP using a 3:1 ratio of deionized water (DI) to Ag ink by volume (25% AgNP to 75% DI). Using a small 150 μm size nozzle, feature sizes of 20 - 30 μm and 1 - 2 μm thickness can readily be attained. The silver structures were deposited on the dielectrics after curing. Thermal sintering of the deposited silver was performed at 180 °C for 5 hours in a nitrogen based oven. For the RF structures, 2.5 μm thick silver features for transmission lines, ground pads, and patch antenna were printed.

3.4.1 Substrate processing

A 1 mm thick copper (Cu) sheet coated with 600 nm of sputtered titanium (Ti) was used. Ti coating ensures good adhesion between the deposited layer and the substrate, and also Ti minimizes the oxidation of Cu. The filler material, BCB, shows good adhesion to metal surfaces such as copper (Cu) and titanium (Ti) often used as contacts for many electronics [84].

Optomec 5x Aerosol Jet five-axis printer with two atomizers was used. The pneumatic atomizer is designed for material handling of various viscosity, upwards of 1000 cP. The ultrasonic atomizer (UA) is designed for materials of low viscosity up to roughly 15 cP. The aerosol mist is directed to the print head and print jet nozzle to be focused and deposited onto the desired substrate surface (see Fig. 1.1).

3.5 Dielectric Property Verification

The very first application of BCB before printing with the Optomec 5x printer was to spin coat a film onto an RF substrate and measure the dielectric constant. This was done using a laminated

4-mil thickness LCP with copper cladding etched on one side to form a ring resonant structure at 14 GHz. By measuring the ring resonator with and without BCB film deposited on top, the difference between the resonant frequency shift and the scattering parameters allowed for a rough extrapolation of the dielectric constant of the BCB. This was done for verification purposes to ensure that the material purchased would behave as expected through the thermal curing profiles used in the subsequent experimental data. A dielectric constant of roughly 2.6 was determined, and with the use of literature published for frequencies upwards of 60 GHz it was decided to use 2.65 for all future simulation and designs using BCB.

3.6 RF Circuits

To demonstrate the effectiveness of this dam and fill process, two simple RF structures were chosen for fabrication operating in the MMW frequency bands: (1) embedded devices and (2) W-band patch antenna. With success of the process, more RF structures were fabricated, including the aforementioned substrate-less package demonstrated here. RF structures were probed using a Ground-Signal-Ground (GSG) probe (120 μm pitch) on an MPI TS150-THZ probe station and measured using the Keysight N5227 vector network analyzer (VNA \ PNA).

3.6.1 Embedded Devices

As illustrated in Fig. 3.1, chips can be embedded directly into the fill material or embedded in a cavity formed in the substrate. The second technique is demonstrated here using a liquid crystal polymer (LCP) substrate. The cavity was formed in LCP with Cu backing using a wet-etch process [92]. A Mini-Circuits KAT-0-D+ transmission line on GaAs die with gold (Au) contacts (0 dB attenuator) was mounted in the cavity using conductive epoxy. The edge between the chip and the LCP was filled with BCB using AJP, allowing a short and smooth transition. Granular polymethyl methacrylate (PMMA) suspended in solvent was printed on top of the chip faces in order to create a resist mask for the BCB printing to reduce overspray dielectric coating the contact pads. PMMA

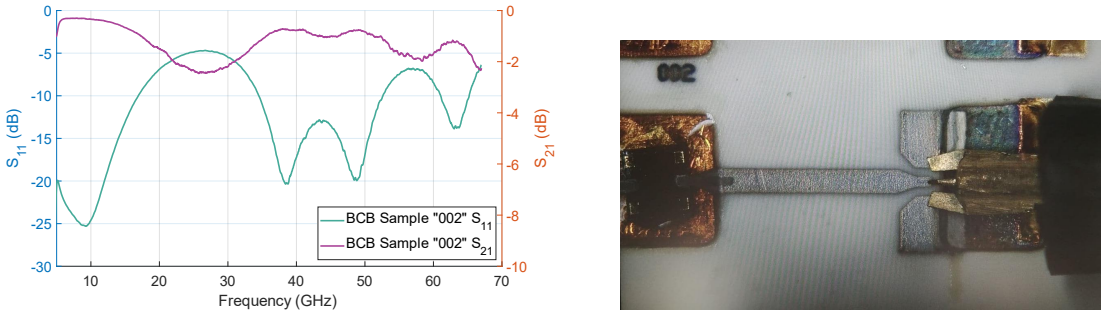

Figure 3.8: (a) S-Parameters of embedded 0 dB GaAs single chip in BCB with interconnection to LCP. (b) Photo image of the measured circuit.

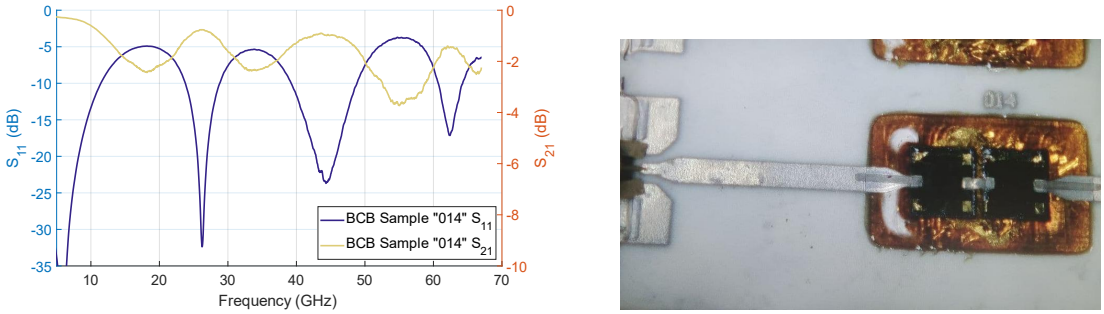

Figure 3.9: (a) S-Parameters of embedded 0 dB GaAs 215 μm chip-to-chip separation in BCB with interconnection to LCP. (b) Photo image of the measured circuit.

was later removed using acetone before printing conductive traces with the AJP.

Three embedded RF circuits were demonstrated: (1) substrate to embedded chip transition, (2) substrate to embedded chip-to-chip, (3) substrate to dielectric transition. The first circuit was performed in order to achieve transition from substrate to device and back to the substrate for measurement using a microstrip transmission line (Fig. 3.8). This demonstrated the basic function of 3D printed interconnect over a BCB infilled cavity, with the second circuit demonstrating the previous interconnect with an additional chip-to-chip interconnect for hybrid circuits (Fig. 3.9). The third circuit was to demonstrate the losses associated with impedance mismatch if matching is not taken into account for the transition period across varying dielectric constants (Fig. 3.10). This loss shows up in the scattering parameters where the return loss is above -10 dB for S_{11} and S_{22}, which can be seen in the figures.

A 50 Ω transmission line was printed across the structure as shown in Fig. 3.11 that can be probed using a GSG probe. Fig. 3.11 also shows the measured S-parameter. This data includes the

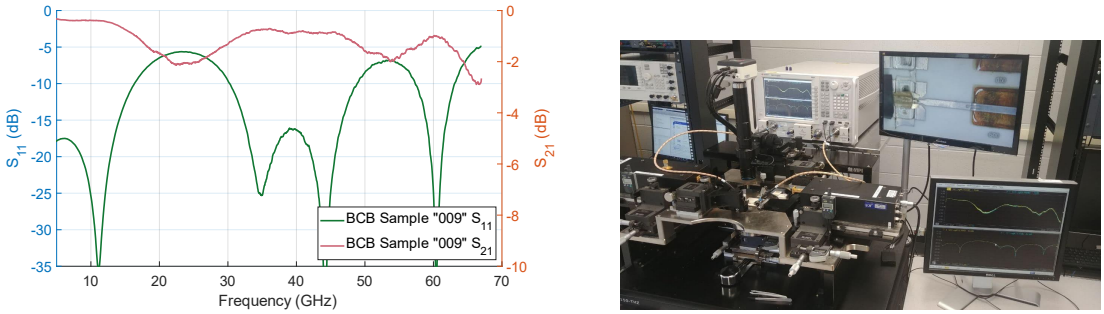

Figure 3.10: (a) S-Parameters of 2 mm BCB fill with transmission line interconnection to LCP. (b) Photo image of measurement setup for GSG probe station.

effect of the microstrip transmission line on LCP. Results show that low-loss transition can readily be designed using this fill process.

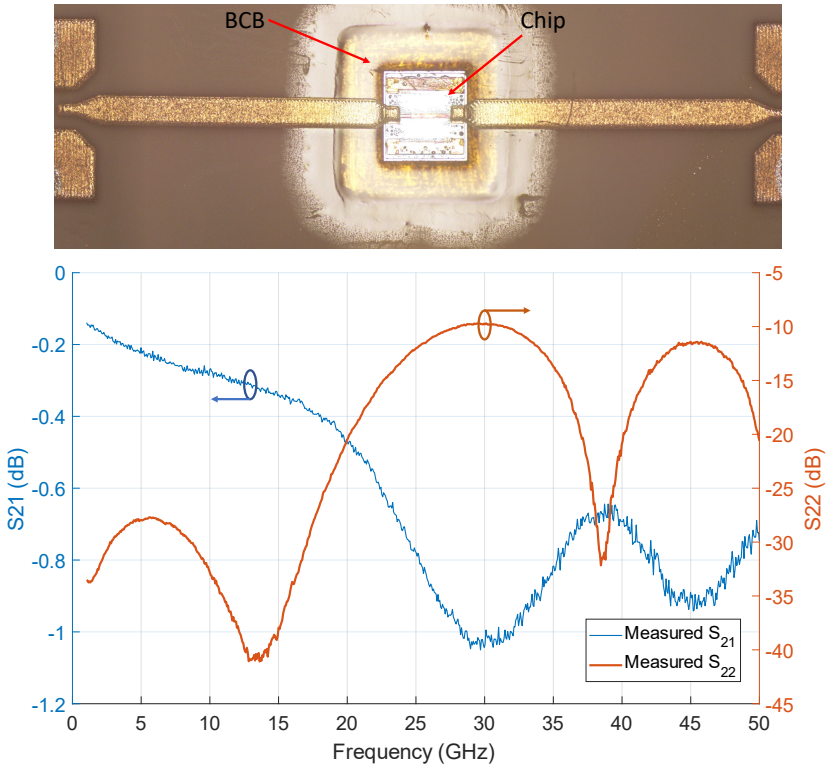

Figure 3.11: Measured S-Parameters of embedded chip in a cavity.

Of the demonstrated embedded devices, various parameters were modified to show how custom tailoring of the fabrication process can be made to fit geometry challenges that a 3D printed AM process is well suited to solve. For manual chip placement that is not precise, transmission lines and interconnects can printed with offset angles or curves allowing for pinpoint accuracy on

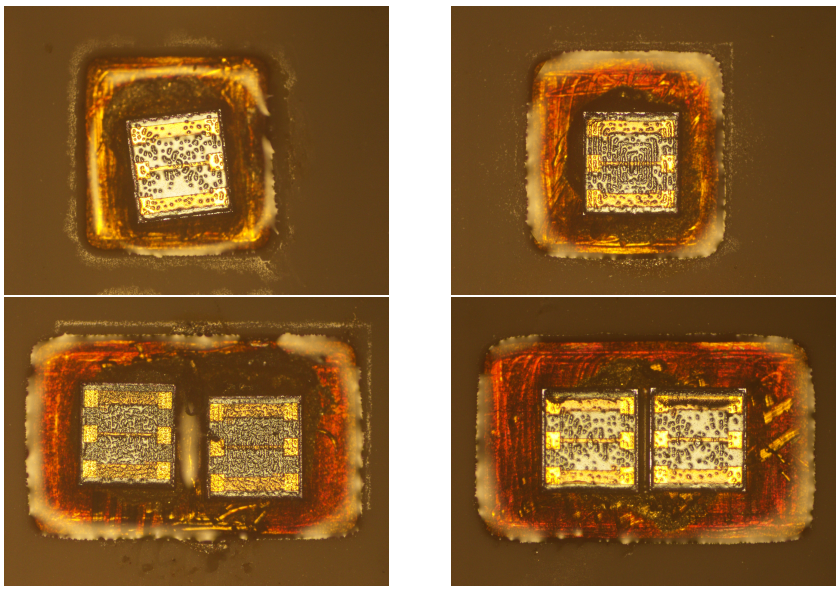

Figure 3.12: Microscope photo images of manual placement chips before removal of protective PMMA film and printing of AgNP interconnects. Left show purposefully offset angles, while right show careful alignment and appropriate distancing of chips.

the finished product (Fig. 3.12). While this is similar to one of the benefits of wire bonded interconnects, the ability to print the interconnect and the transmission line trace to the device from its termination point with custom tailoring allows for a higher yield from the fabrication steps without concerns for errors such as mask misalignment. Chips were also placed at varied distances to show the losses associated from creating a metal interconnect without proper impedance matching over three distances between the RF chips (Fig. 3.13 shows the gap distance varied between two chips and the S-Parameters differing for each distance). Some tolerance in fabrication processed can lead to lowered yields, which this process helps to improve those statistics by tailoring custom interconnects to misaligned chips. The loss in decibels is shown by the calculation:

$$LOSS = 1 - [mag(S_{11})^2 + mag(S_{12})^2]$$

3.6.2 Patch Antenna

A 94 GHz patch antenna was fabricated on a 65 μm thick film of BCB having PI dam on a 1 mm thick Ti coated Cu substrate. Figs. 3.15 and 3.16 show the profile of the dielectrics and the picture of the patch antenna. The feed point of the GSG launch was optimized to be as close to the width of the 50 Ω transmission line. The signal is fed into the transmission line through a 120 μm

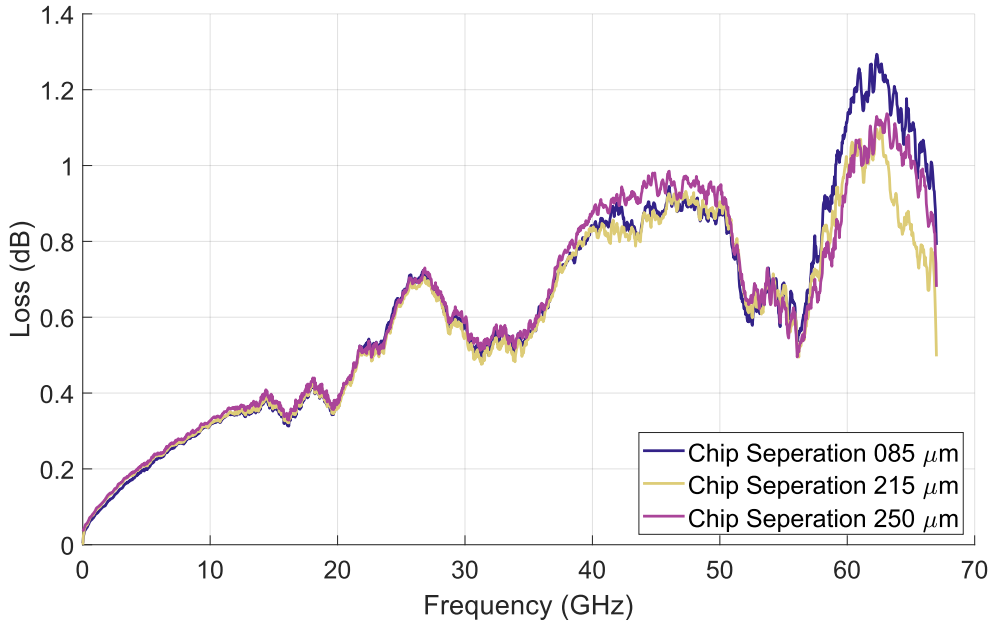

Figure 3.13: Losses: Chip Spacing over DC - 67 GHz. Distance between the chips were varied from 85 to 250 μm.

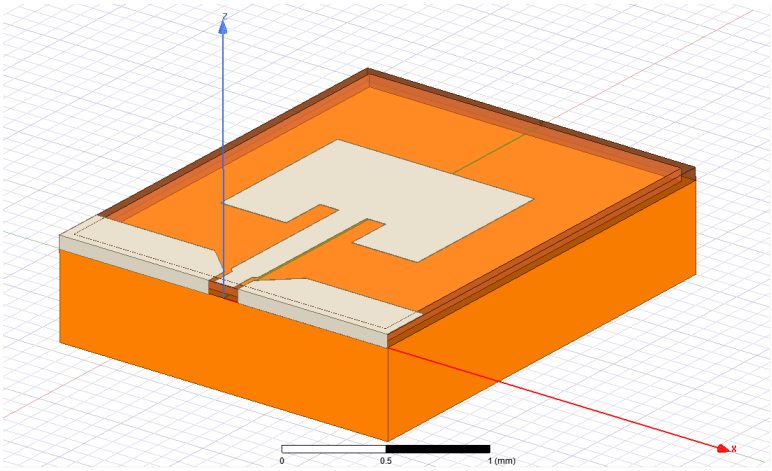

Figure 3.14: Patch antenna 3D model exported from HFSS simulation.

pitch GSG probe. The filling step was performed in 3 print and cure steps to precisely control the resulting thickness. Fig. 3.15 shows that the BCB dielectric may not be perfectly flat after printing and is dictated by the planarization of the sample in the oven during curing.

Rather than forming vias, to achieve good connection, the grounds of the GSG pad were connected along the PI wall by printing at a 30° angle on the tilted platen of the Optomec 5x (Fig. 3.17).

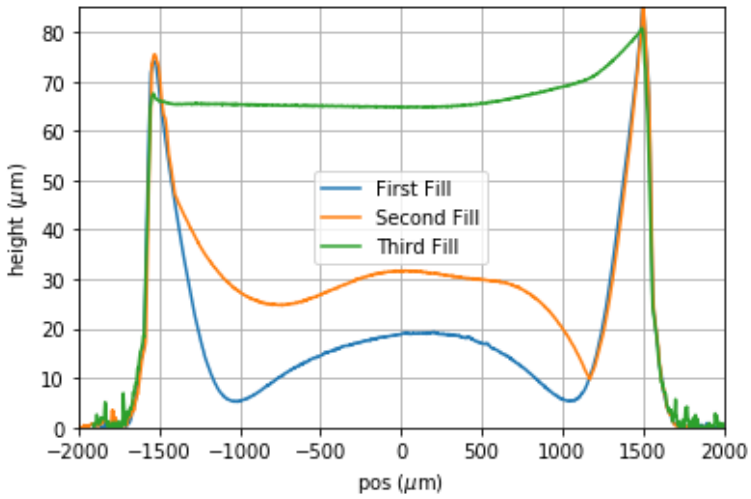

Figure 3.15: Left: 2D Profile of the dam with multiple fillings; Right: Printed Ag patch antenna on filled BCB.

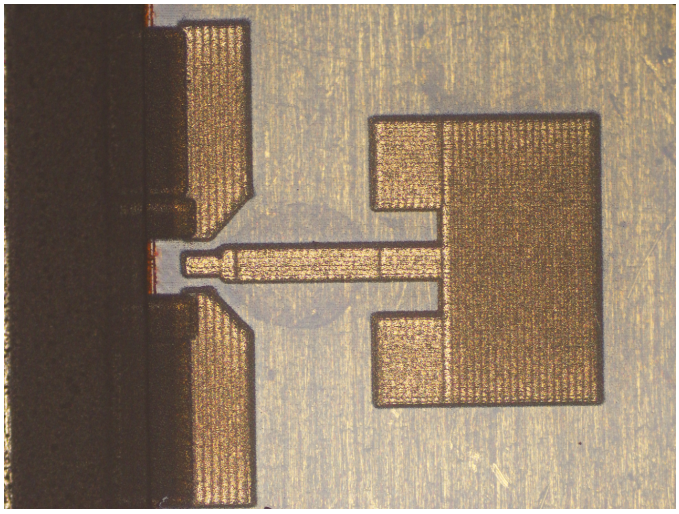

Figure 3.16: Left: 2D Profile of the dam with multiple fillings; Right: Printed Ag patch antenna on filled BCB.

Fig. 3.18 shows the measured S_{11} of the patch antenna. It has a return loss of 22 dB at 94.08 GHz, and the simulated gain is 4.8 dBi. Simulation results are also included in the figure. It was determined by simulation parameters that there is approximately 2 Ω of contact resistance between the GSG probe and the pad. Simulation results of the antenna including a 2 Ω series resistance is also shown in the figure. The VNA measurement and simulation results match closely. These results show that the proposed process can be used to design MMW patch antennas with good performance.

Multi-layered circuits: by using process compatible materials in this circuit which can with-

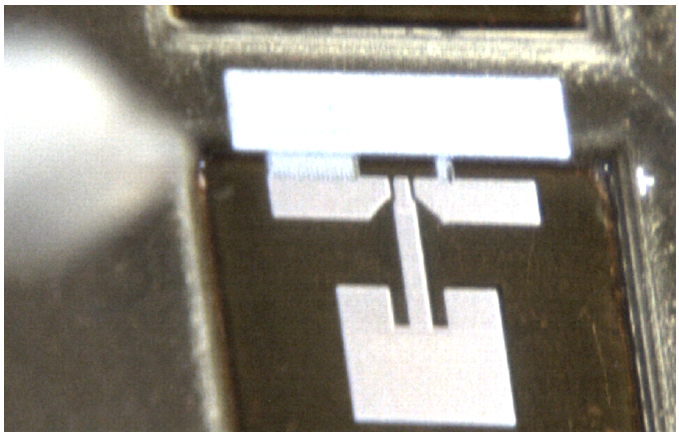

Figure 3.17: Process Camera capture of 30-degree angle printing on Patch Antenna ground connection using Ag ink.

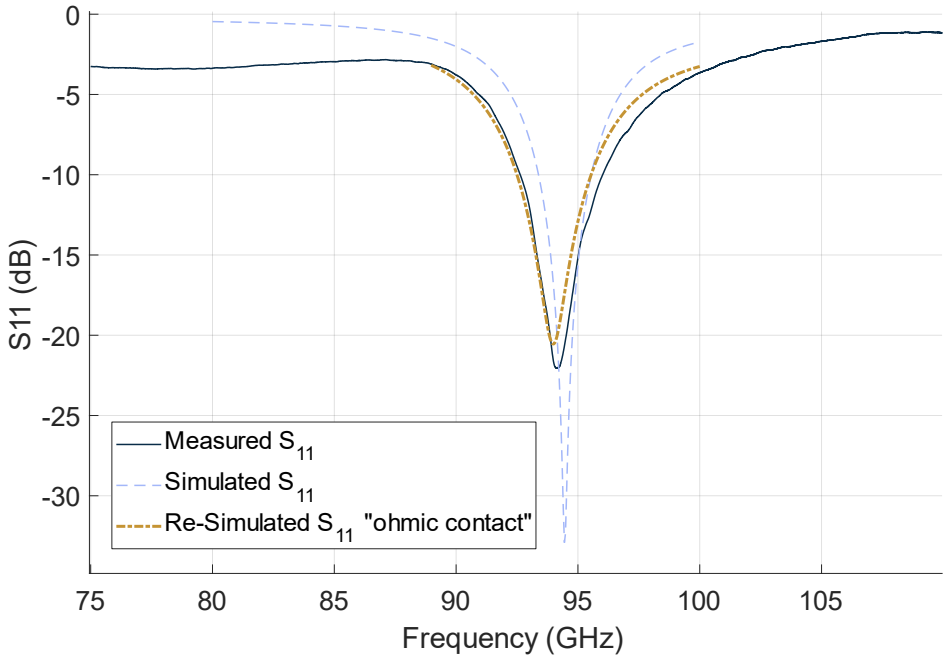

Figure 3.18: Measured and simulated S_{11} of the patch antenna, including a re-simulation with series resistance added for probe to silver contact.

stand thermal cycling and multiple AJP depositions, multiple layers are fully achievable to allow for designs such as focused antennas, capacitive coupled conductors, and dielectric lenses. The previously discussed patch antenna can be loaded with a dielectric on the patch to change the resonant frequency of the antenna and improve the gain characteristics or directionality of the antenna. With the novelty of 3D printing a barrier to dam the dielectric material only where it is needed, a resonator was formed atop of the 94.3 GHz patch antenna. Simulation in HFSS of a

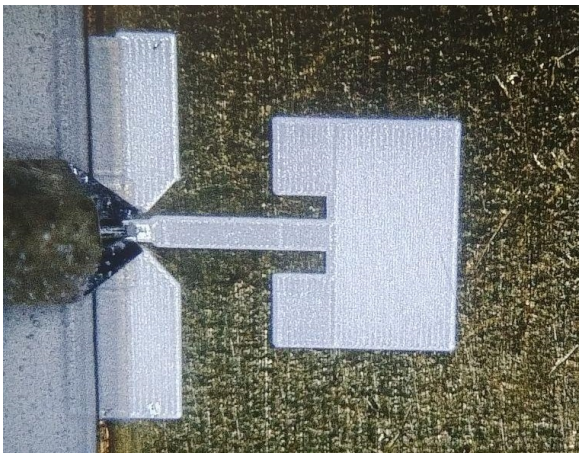

Figure 3.19: Measuring the patch antenna on the PNA

domed lens of BCB shifted the resonant frequency downward in frequency to 89.46 GHz. This not only changes the gain pattern of the antenna, but also allows for the ability to miniaturize lower frequency antennas with the same footprint of very small antennas.

3.6.3 Substrate-less Packaging

The final demonstrated RF circuit involved the use of the substrate-less 3D printed package approach. This self-packaging 3D printing method using the dam and fill steps described above, with an additional lift-off process included (See Fig. 3.20). Polymethyl methacrylate (PMMA) was used as the release material as it easily dissolves under acetone solution. PMMA was first printed onto a carrier substrate of borosilicate glass, with the film measuring 5 μm. This thickness was required in order to form adequate seal to the die structures. GaAs devices were placed face down onto the PMMA film and placed on a hotplate at 160 °C until the devices sunk into the PMMA and allowed for a seal around the passivation layer and contact pads. This sealing step is important to prevent the flow of low-viscosity materials onto the face of the die. Once component placement was achieved, the same dam and fill process used for the other RF circuits was repeated around the chips on the PMMA film. Ag ink was printed onto the back side of the chips to connect the ground plane of both chips and the BCB package. Acetone was used to dissolve the PMMA layer and allow for the package to float off of the glass substrate leaving only the packaged chips. This

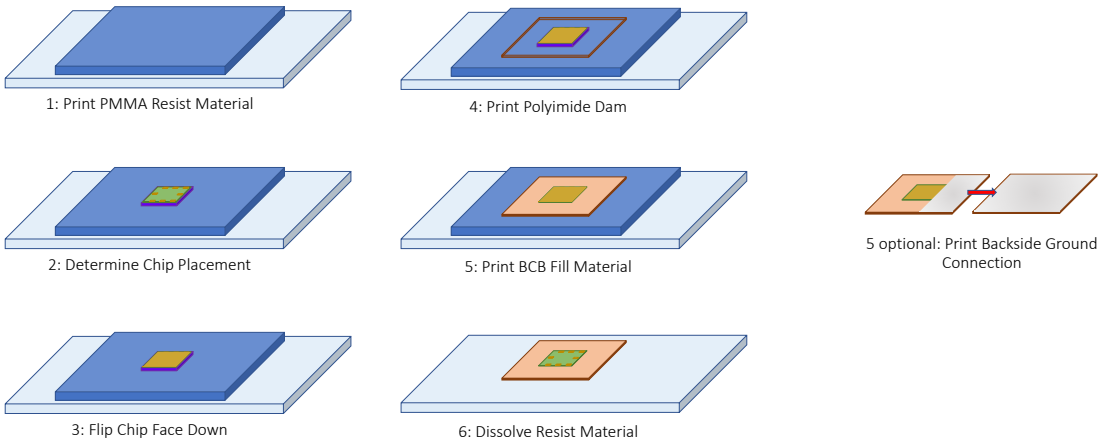

Figure 3.20: Fabrication steps used to make a substrateless package for bare die chip devices.

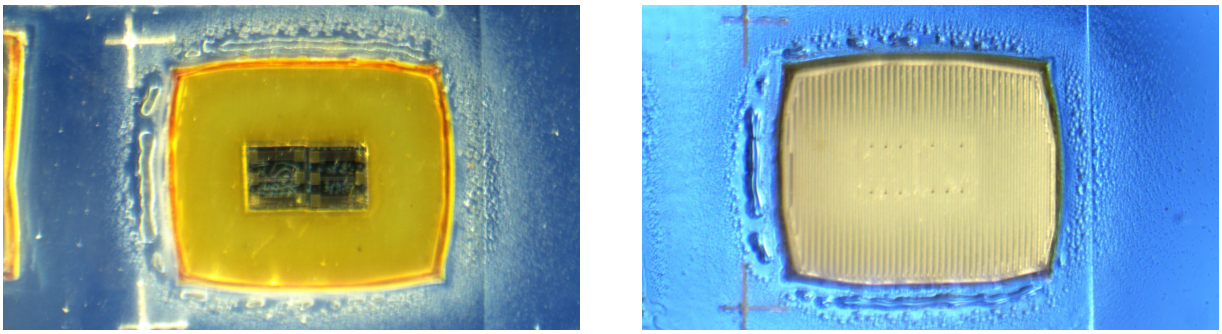

Figure 3.21: Fabricated substrateless package. Left: face side of the dice. Right: ground plane printed on back with AgNP ink.

package with BCB and PI structure allowed for ease of handling and was placed face up on a board to process the interconnect. One final BCB layer was printed on the edge of the two chips to fill a small 5 μm valley leftover from processing. Then, Ag ink was printed to connect the two chips and measurement was taken to demonstrate a fully AM package which can now be attached to any surface and used as a hybrid component for RF circuitry.

By utilizing this process, the absolute minimum distance between two devices was shown with a planar face surface regardless of the semiconductor technology being used. Both chips were GaAs with a thickness of 100 μm for ease of demonstration. This process would allow for varied

thickness dice, as the devices are placed face-down onto the lift-off material prior to dielectric printing. This insures that the faces of the dice are both level and at the absolute minimum distance for the printed interconnect that the device design allows. This process utilized standard chips designed for wire bond interconnects without an impedance match tailored to 3D printed metal traces. This impedance mismatch is the largest obstacle to the process, and future devices could be designed with wideband transitions for printed interconnects as the intended fabrication step for hybridized applications.

The printed package has overall dimensions of 2.5 mm x 3.5 mm and physical separation between the devices of 23 μm. Shown in Figure 3.22, the package allows for the minimum distance between the interconnect pads of these chips. Each chip has a passivation layer and exposed street of 15 μm as part of the manufacturing process. This leaves the pads inset by roughly 25 μm from the edge of the die. Because these chips were designed to be probed and wirebonded, the pads are sized to the requirements of those tools and thus the structure itself is not fully matched from one side to the other. The pads are larger than the width of a 50 Ω transmission line, causing a low impedance at the pad, and the transmission line on the GaAs substrate is thinner, corresponding to a high impedance in the middle of the die. This limits the high frequency capability of the device, and impedance matching to overcome this was not part of this demonstrated work. With loss due to impedance mismatch as a concern, the loss of the circuit was calculated for this package as well, and is shown in Fig. 3.23. The loss remained below 1 dB through the designed frequency range for the chip, keeping in mind that this is 2 chips connected together. Loss increased above 50 GHz, which is beyond the rating of the attenuator chip.

3.7 Results

High density integration of devices on a chip-scale level are highly desired by many electronics manufacturers. Recently, the common use for high density fabrication was utilized heavily by MEMS and multilayer PCB manufacturing [8]. RF and MMW circuits can also benefit from rapid production techniques for high density integration and interconnects with RF substrates and 3D

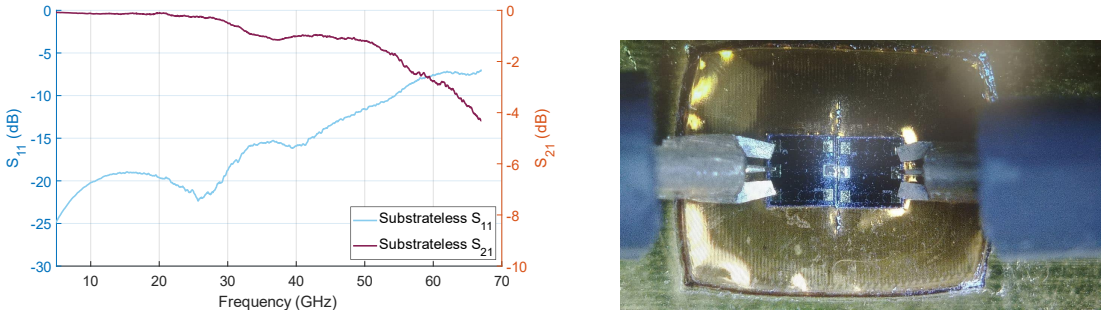

Figure 3.22: (a) S-Parameters of substrate-less BCB package containing two devices. (b) Photo image of the measurement.

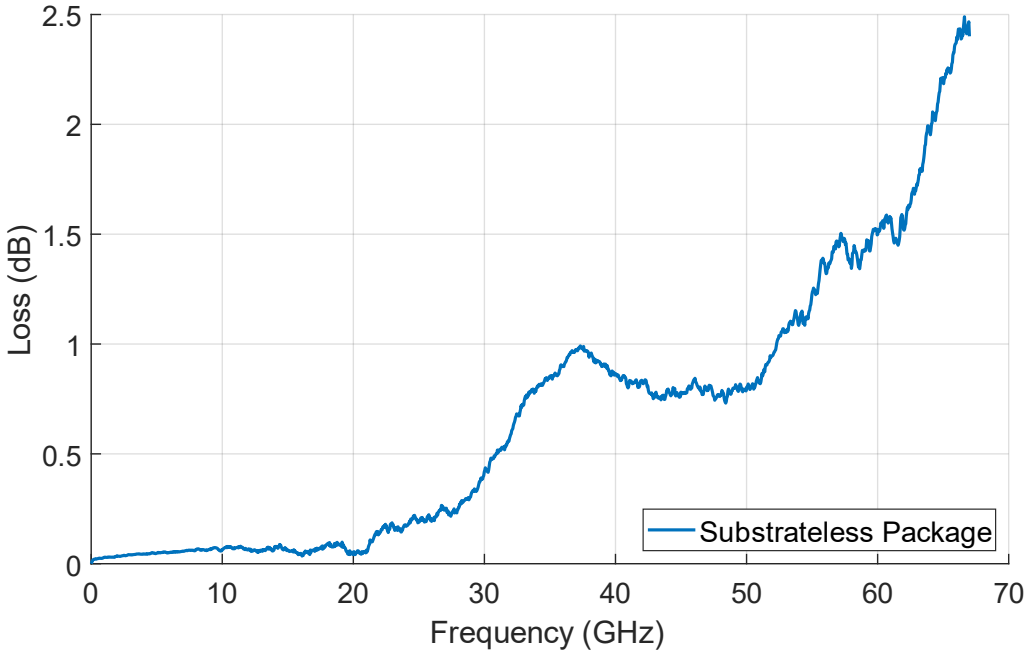

Figure 3.23: Losses: Substrate-less package over DC - 67 GHz. Distance between the chips were 23 μm [77 μm pad-to-pad spacing].

printing. With MMW circuit design, the substrates must be carefully chosen in order to meet requirements for signal integrity, environmental compatibility, and mechanical compatibility with varied fabrication technologies (such as GaAS, SiN, GaN, SiC, etc.). As the envelope for frequency and physical size limitations of devices continues to be pushed, the production methods also must be pushed past limitations in order to meet increasing demands.

3.8 Future Work

This work discussed the applications which can be utilized today in hybrid RF and MMW circuits, and also introduced a few future concepts that can be improved upon in following research. The major benefit to all of the above methods leads majorly to the tailored design of shapes both planar and non-planar on substrates or self-packaged substrates. Mentioned prior, substrate based hollow waveguides and waveguided antennas can be fabricated using the substrate or a 3D printed substrate built upon itself using low-loss dielectric materials. While this process has been shown with LTCC, it can be redesigned with any low-viscosity dielectric with desired loss parameters for the chosen frequency band, making the process much more versatile for application-specific designs.

3.9 Conclusion

A new dam and fill process to selectively deposit dielectric patches with varying dimensions on a common substrate using AJP was demonstrated for additive manufacturing. This process has many advantages: 1) rapid deposition of dielectrics with varying geometries using AJP, 2) allows the use of materials that readily flow during deposition, drying or curing, 3) allows for embedding (self-packaging) of chips and other components, 4) allows self-planarization of dielectrics, 5) allows for the design of complex RF circuits. A millimeter wave embedded 0 dB attenuator and a W-band patch antenna were demonstrated, with improvements leading to a substrate-less design package using this process. This process allows for many high density MMW circuits to be fabricated with ease using AJP.

CHAPTER 4

CONCLUSIONS

4.1 Conclusions

In this thesis, two major approaches have been developed and discussed for rapid additive manufacturing of microwave and millimeter-wave RF circuits utilizing AJP 3D printing. Both high conductivity Ag circuits and self-packaging processes have been demonstrated with current and future applications in order to meet the demand of high speed communications and component manufacturing.

In Chapter 2, optical UV flash sintering was demonstrated as a viable alternative to thermal baking of silver nanoparticle ink in order to achieve high conductivity required for RF applications. Traditional thermal methods as well as other novel processes were compared to this sintering technique at both DC ohmic performance and for microwave applications using a microstrip patch antenna based on LCP substrate technology. The combination of multiple print and sinter steps were shown to achieve the high conductivity for microwave applications using AJP 3D printed Ag. SEM cross-sectional measurements were made to show that this multilayered approach solves issues of delamination and deformation of conductive inks with thick single layer sintering.

In Chapter 3, a new approach to fabricating AJP thick film dielectric films and self-packaged chips was shown in order to drastically reduce the difficulty and time required to form chip scale packages. This dam and fill process was used to demonstrate multiple cell selective dielectric deposition on a carrier substrate with BCB material thickness spanning 5 μm to 45 μm within a 1 cm x 1 cm area. This process was used to fabricate a W-band patch antenna on BCB printed using AJP for both dielectric and Ag conductor. To show the novelty of packaging, embedded circuits were fabricated to introduce selective dielectric deposition as a viable addition to hybrid circuit design. Finally, a self-packaged chip was demonstrated with a substrate-less process involving a release agent in order to produce the absolute minimal spacing between two RF chips for 3D

printed interconnection and packaging with low loss.

This work demonstrates how chip scale packaging and rapid prototyping can take advantage of additive manufacturing using aerosol-jet printing for reel-to-reel compatible applications and reduced laboratory expenses for future works. Commercially available materials were used in order to demonstrate relatively inexpensive fabrication with common choice conductive and dielectric inks.

4.1.1 Limitations Overcome

Thermal processing limitations for both conductive and dielectric materials are a major issue for most additive manufacturing goals. Low temperature substrates are often used in RF circuits, and thus material compatible processes must be chosen within those limits. For conductive inks, optical UV flash sintering allows for the single or multiple doses of high energy transfer to the nanomaterials with little damage to the delicate substrates. This is a major improvement over low conductivity achievable by only room temperature drying and sintering of conductive nanoparticles. Dielectric materials printed using AM processes may also struggle with compatibility of other materials during thermal cycling. Traditional methods of achieving thick dielectric films requires many layers of wet resin and drying or curing steps to build layers. This repeated thermal cycling cause stress to the carrier and other sections of the fabricated item. By reducing thermal cycling to a single or a few cure steps with thick deposition of resin in a single print session, the thermal stress is reduced with the side effect of drastic reduction of processing time. Hybrid circuits can be formed with multiple technologies and various z-heights with few limitations seen by traditional fabrication methods.

4.1.2 Future Work

Many opportunities were explored in the work that lead up to this thesis topic. Several techniques were tried and noted for potential future application. Noted in the Appendix section are methods for room temperature sintering of Ag nanoparticle ink using select-able color spectrum LEDs for

plastics and other low temperature materials. This short term project involved use of UV, full spectrum white, near-infrared and infrared 100 W light-emitting diodes to help determine which spectrum band from 300 nm to 900 nm would cause energy absorption in the silver inks. No direct conclusion was made from this work, but it has potential for future expansion if plastics are a desired material for additive manufacturing.

Another area of future work is custom tailoring of dielectric geometries on top of patch antennas useful either for gain focusing or frequency selection. An experimental BCB lens was printed on top of a W-band patch antenna in order to observe the effect of resonance frequency shift. Simulation and preliminary data shown a reduction in the resonance of the antenna and proved that this method can be further improved upon. It was mentioned chapter 3, but it was not explored in depth.

Finally, simulation and first experimental fabrication of a hybrid chip on board process was created to utilize a wide-band transition of microstrip to chip with 3D printed coaxial via was explored. This topic was only explored briefly as it was too application specific to be included in the thesis work.

The high resolution and speed of fabrication which can be achieved using AJP 3D printing can allow for increasingly reduced size for printed circuits and reduced loss for interconnection of bare die components. Packaging improvements will continue to be made as further exploration into these areas increase. Complete hybridized RF circuits can be realized within hours of computer aided design. By expanding the topics demonstrated in this work, many difficult to achieve circuits can be fabricated with reduced time, cost, and waste in comparison to traditional methods. Reel to reel printing of conductive materials and sintering can potentially include the use of AJP for fine resolution features and optical UV flash sintering for high conductivity required for microwave and millimeter-wave technologies.

APPENDIX

APPENDIX

A.1 Extra Information

A.1.1 Dielectric Verification

Verification of dielectric constants for BCB were performed for laboratory processing used in Chapter 3. This verification was performed using measurements of an unloaded ring resonator structure on LCP, followed by dielectric loading with BCB, curing processes, and further measurement to determine the shift in resonant frequency and extrapolate the dielectric constant from scattering parameters.

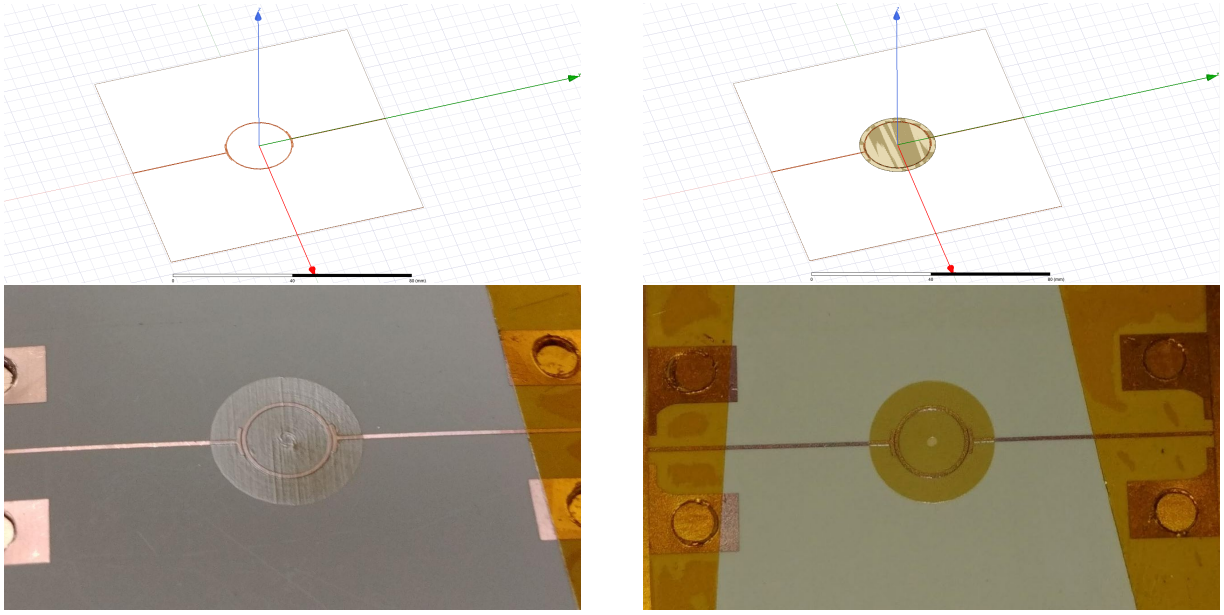

Figure A.1.1: Dielectric Verification using 14 GHz unloaded and loaded ring resonator on etched LCP.

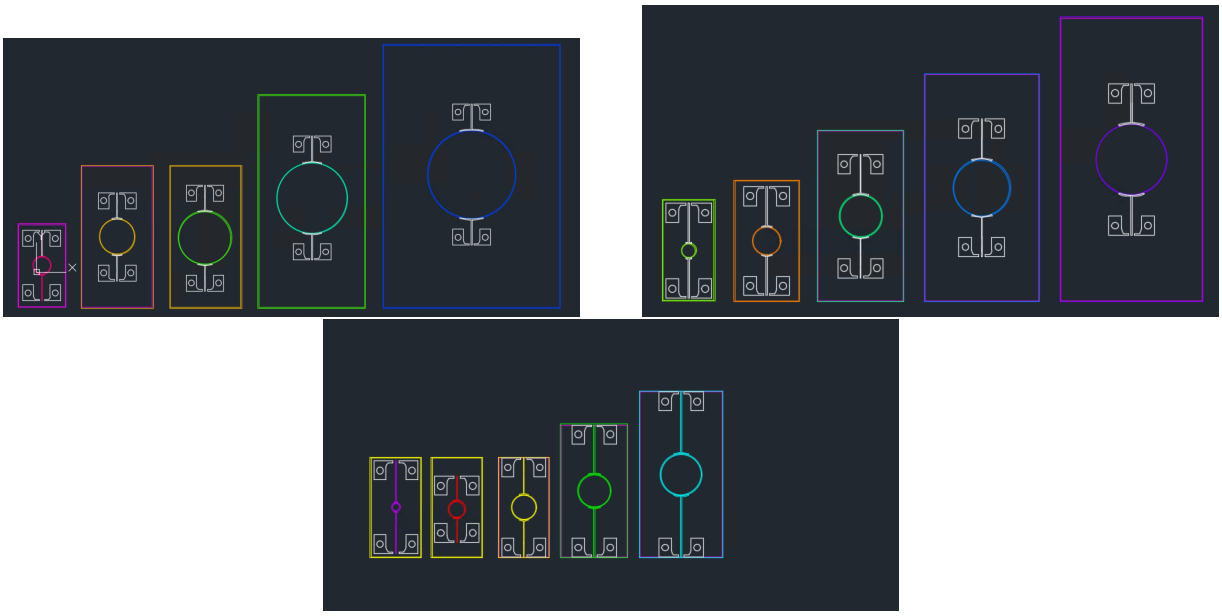

Figure A.1.2: Set of 10, 15, 25 GHz ring resonators on 4 MIL thickness LCP. Measured with no surface dielectric loading and then after dielectric loading to determine dielectric permittivity of printed BCB films.

A.1.2 Substrateless Package Prototypes

First prototypes for proof of concept to show substrate-less packaging involved a single die. This chip was placed face-side down onto a film of PMMA which was previously printed with AJP onto a borosilicate slide. The chip was placed by hand, and allowed demonstration of the AJP process to custom tailor a printing pattern regardless of the placement orientation. Photos shown were taken from the reverse side of the slide through various steps of the process. Melting of the PMMA allowed to form a hermetic-like seal around the top and side edges of the die to prevent dielectric filling to flow onto the top surface and cover traces or contact pads. A pattern was designed for the desired size of the PI dam, and then printed to the same height as the device. BCB was then printed to infill the dam structure and curing was performed as discussed in Chapter 3. The structural experiment lead to the design of a two-device interconnection described and measured in Chapter 3.

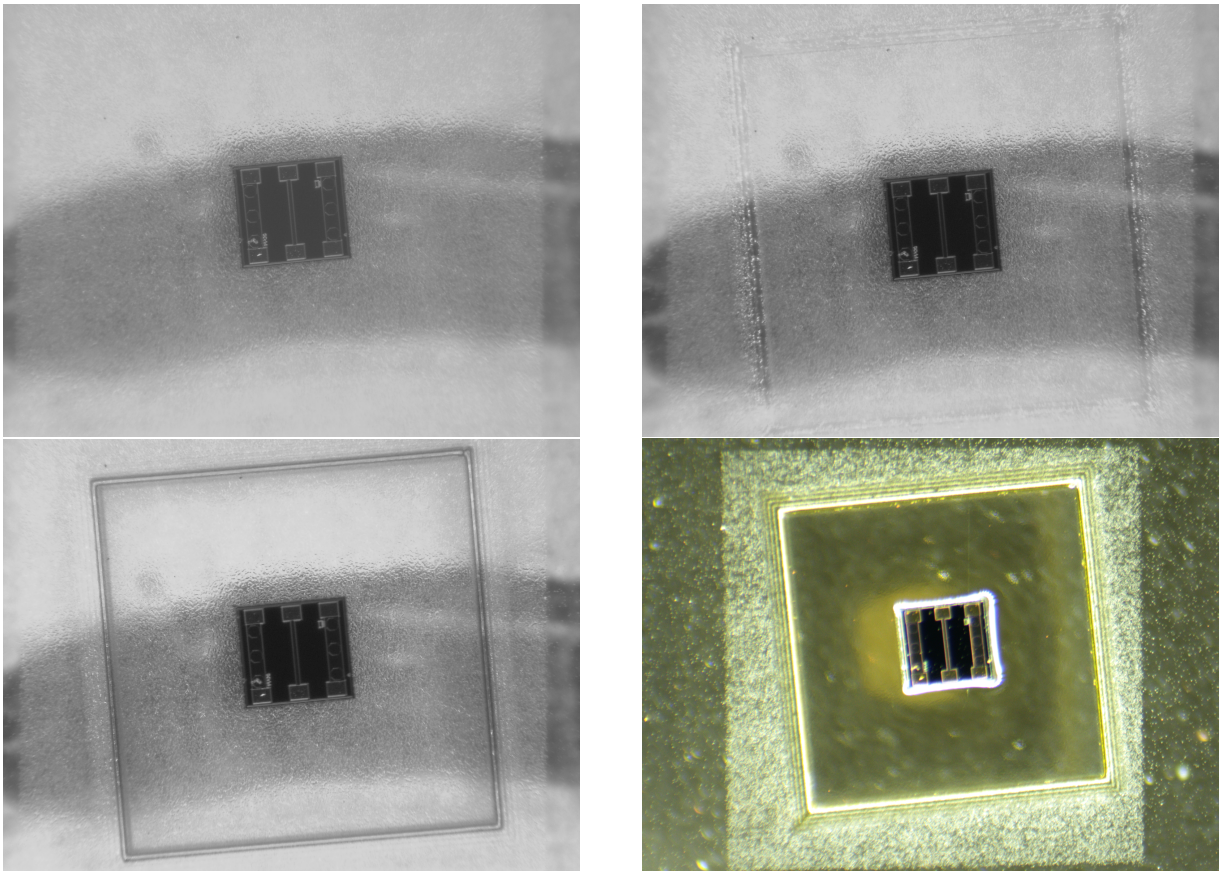

Figure A.1.3: First Prototype of Liftoff Process

A.2 Future Work

Specific wavelengths of concentrated light may be particularly useful in the curing of materials or sintering of nanoparticles. Selecting filters for the wavelength may be challenging, so a selectable wavelength system was built utilizing 100W LED lamps of various wavelengths including 395mn, 425nm, 440nm, 660nm, 730nm, 850nm, 940nm, and a broad spectrum 380-840nm white LED. For materials that absorb these wavelengths, it is possible to use photonic sintering at the specific wavelength. Early experiments shown that AgNP inks react to various selected LEDs, but it is yet unknown how thick of a film can be dried or sintered with this system.

A.2.1 Ag Sintering With Broad Spectrum LEDs

Figure A.2.4: Photograph of LED Sintering Device

A.2.2 BCB Patch Antenna with Dielectric Lens

Two improvements to the dielectric dam antenna presented in Section VII B. can be explored further with tailored shapes printed in conjunction with the patch antenna. First, dielectric dams can be printed on the surface of the patch conductor to allow focusing and shaping of the beam pattern. Second, multiple layered dielectric and conductors can be utilized to fabricate reflectors below the patch antenna in order to increase gain and directivity of the antenna.

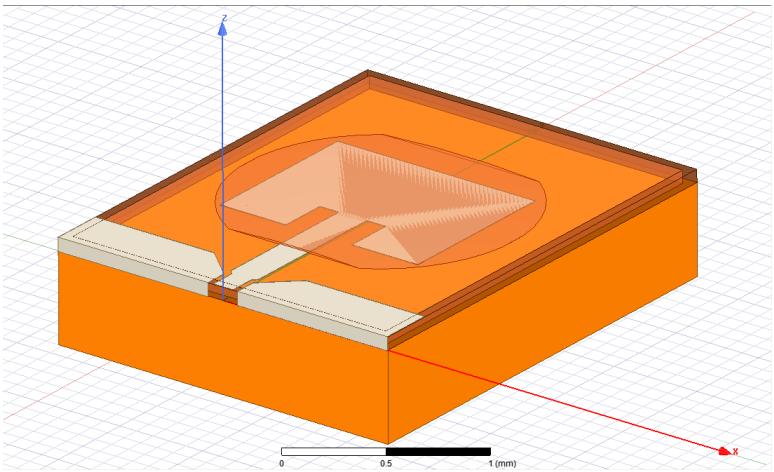

Figure A.2.5: Patch with BCB lens 3D model from HFSS simulation

The first of the two described was explored briefly, where the same dam and fill method with PI and BCB were used to form a simple dielectric micro-lens as a proof-of-concept. Fig. A.2.7 shows that the micro-lens had feature height as much as 50 μm over the distance of nearly 2 mm. Fine tuning of parameters could allow for frequency shifting and direction changes to the gain pattern of the antenna.

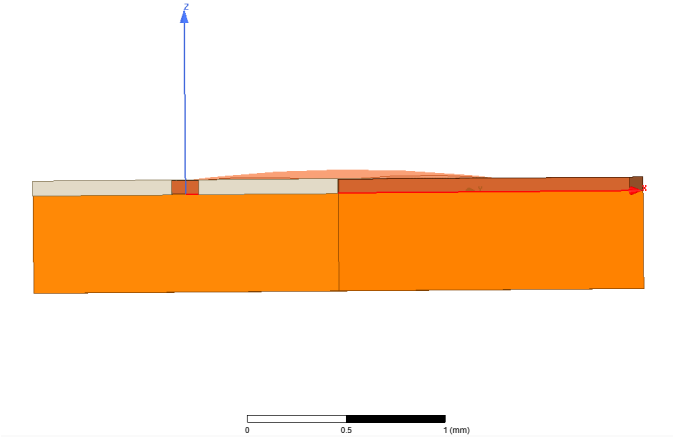

Figure A.2.6: Patch With 50 μm Dielectric Lens 3D model from HFSS simulation

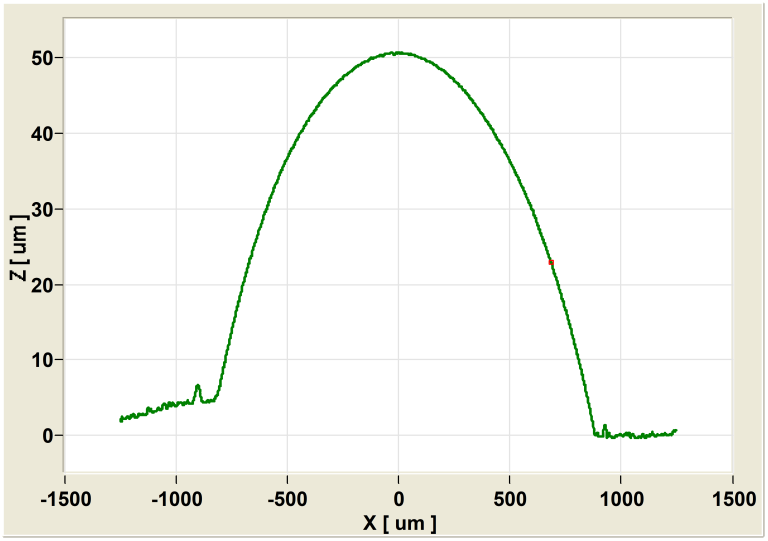

Figure A.2.7: Profile of BCB lens printed on top of patch antenna.

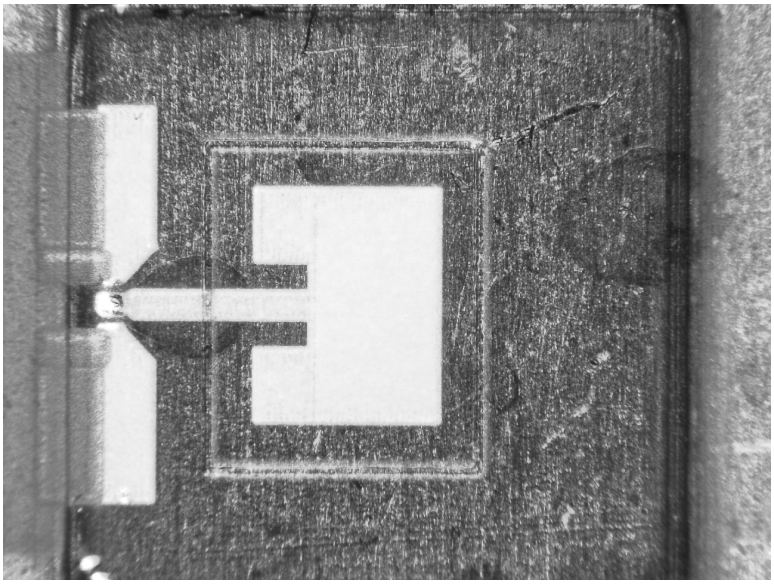

Figure A.2.8: Lens Barrier Fabrication.

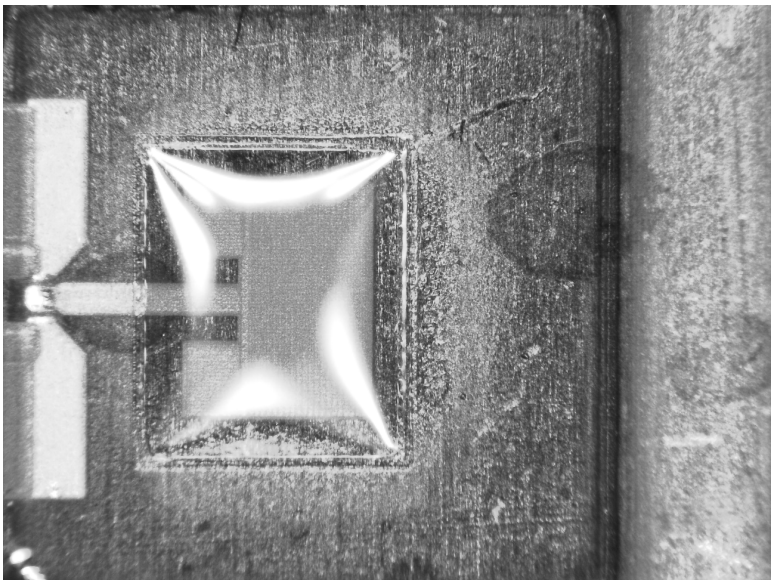

Figure A.2.9: Lens Dielectric Fabrication.

A.2.3 3D Printed Coaxial Interconnection

First proposed before the dam and fill process had been utilized for packaging of a chip on a surface substrate, a chip to microstrip transmission line transition circuit was explored. The goal of this experiment was to perform a coaxial via interconnect from two different z-heights on a substrate using AJP. The 0 dB attenutator chip would be placed onto a printed ground pad and die attach section, followed by the 3D printed structure of a via and coaxial ring. This demonstrated the potential of high aspect ratio AgNP with AJP, but proved to be challenging. The BCB dielectric dam shown in the 3D render from HFSS was the first design of a dam and fill thick dielectric film as part of this research. As the goal was experimental, the application was ultimately not used, but instead lead to further research into the dam and fill process for self packaging of chips and interconnections as described in Chapter 3.

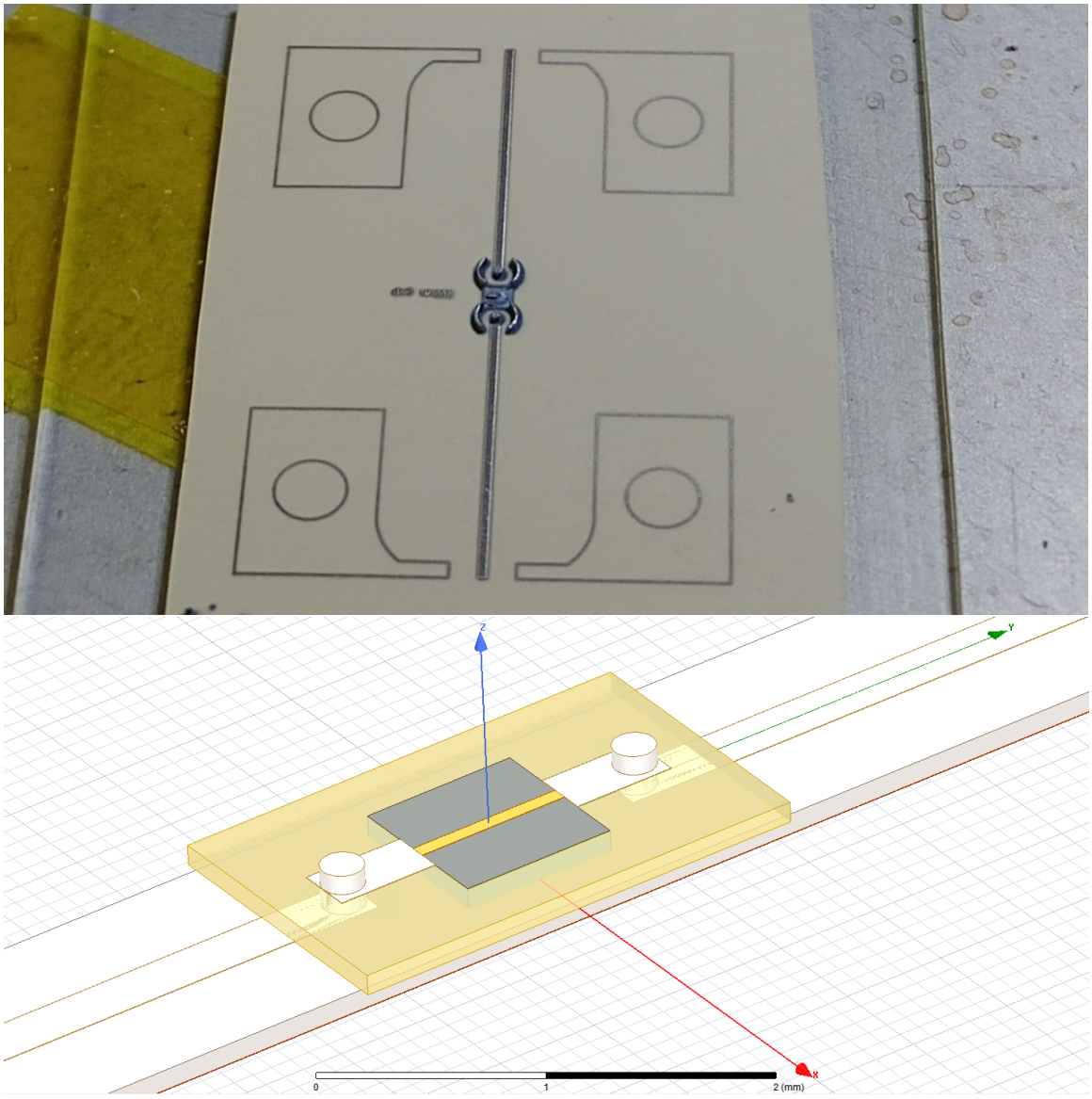

Figure A.2.10: 3D render of Coaxial Chip Interconnection

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