TRANSMITTER DESIGNS FOR SUB-6 GHZ AND MILLIMETER WAVE BANDS

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ABSTRACT

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The rapid growth data streaming demand in modern communication systems makes unprecedented challenges for wireless service providers. Along with the growth data streaming demand, the steady development of wireless application causes an issue of wireless coexistence with limited frequency spectrum. Therefore, the energy and spectrum efficient transmitters with higher data rate, small die area, and low integration cost are demanded for the modern communication systems.

The fifth generation mobile network emerges as a promising revolution in mobile communications with higher data rates. In 5G mobile network, two kind of frequency bands, sub-6 GHz bands and millimeter-wave bands above 24 GHz, are classified. Due to the densely packed spectrum in sub-6 GHz bands, the transmitter designs have focused on improving spectral efficiency with frequency-localized waveforms such as Orthogonal Frequency Division Multiplexing. However, the OFDM signal has a major drawback of high peak-to-average-ratio, which results in degraded power efficiency of the transmitter. On the other hand, to support higher data rate, mm-wave bands can support bandwidths up to 2 GHz without aggregating bands together. However, at mm-wave bands, the maximum range to sustain reliable wireless links is decreased due the increasing pass loss. Fortunately, the phased array techniques, which have been used for defense and satellite applications for many years, enables the directive communications could be a promising solution to overcome the challenges.

The objective of this dissertation is to present novel topologies for transmitter designs, which are suitable for modern communication systems in both sub-6 GHz and mm-wave bands. For sub-6 GHz bands, an efficient quadrature digital power amplifier as a standalone transmitter has been proposed. The proposed transmitter employs complex-domain Doherty and dual-supply Class-G to achieve up to four efficiency peaks and excellent system efficiency at power back-off. For mm-wave bands, an 18–50-GHz mm-wave transmitter has been proposed. The proposed mm-wave transmitter is designed for low power consumption, a small area, and supports emerging multibeam communications and directional sensing with an increased number of phased array elements from 18–50 GHz.

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KEY TO ABBREVIATIONS

OFDM	Orthogonal Frequency Division Multiplexing
PAPR	High Peak-to-Average Ratio
PBO	Power Back-off
OOB	Out-of-Band
PA	Power Amplifier
SE	System Efficiency
SCPA	Switched-Capacitor Power Amplification
CDD	Complex-Domain Doherty
PVT	Process-, Voltage-, and Temperature
DPD	Digital Predistortion
QAM	Quadrature Amplitude Modulation
DPA	Digital Power Amplifier
P_{OUT}	Output Power
LINC	Linear Amplifier with Nonlinear Components
SCS	Signal Component Separator
CORDIC	Coordinate Rotation Digital Computer
VMD	Voltage Mode Doherty
RF	Radio Frequency
XFMR	Transformer
P_{SC}	Power Dissipation
LO	Local Oscillator

AUX	Auxiliary
DCW	Digital Control Word
LUT	Look-Up Table
EVM	Error Vector Magnitude
SCPI	Standard Commands for Programmable Instruments
2DLUT	Two-Dimensional Look-Up Table
AUX	Auxiliary
LSB	Least Significant Bit
CW	Continuous-Wave
RFIC	Radio Frequency integrated circuit
P_{SC}	Power Dissipation
CG	Common Gate
CS	Common Source
DA	Driving Amplifier
V2I	Voltage-to-Current
RLC	Resistor-Capacitor-Inductor
KCL	Kirchhoff's Current Law
SOI	Silicon-On-Insulator
P1dB	1-dB Compressed Point
OIP3	Output Third Order Intercept Point
BGA	Ball Grid Array
Psat	Saturated Output Power

1 INTRODUCTION

1.1 Wireless Communication and Frequency Bands

Since the existence of human interactions, human beings have discovered various ways to communicate with each other through the combination of gestures, symbols, and primitive language. In addition to face-to-face language-based communication, humans have also continued to look for effective and reliable communication approaches over long distances. One example of long-distance communication is the use of a heliograph. Ancient civilizations used a heliograph to reflect the light of the sun to alarm allies of invasion.

Over the past hundred years, long-distance communication through radio waves has been proved as a reliable method. The first wireless telegraphy system, which adapted the radio waves, was invented by Guglielmo Marconi. Human society has benefited from the great convenience of the first wireless system since its inventions, which has led to the highly divided radio frequency spectrum for a huge number of applications [1]. The raid frequency bands and applications include extremely low frequency for seismic studies (ELF, 3Hz to 3 kHz), very low frequency for submarines communication (VLF, 3 kHz to 30 kHz), low frequency for radio frequency identification (RFID) (LF, 30 kHz to 300 kHz), the medium frequency for AM radio transmission (MF, 300 kHz to 3 MHz), high frequency for near field communication (NFC) (HF, 3 MHz and 30 MHz), very high frequency for analog TV broadcasting and FM radio broadcasting (VHF, 30 MHz to 300 MHz), ultra-high frequency for GPS navigation systems, satellites, pagers, Wi-Fi, Bluetooth, and most importantly GSM, CDMA, and LTE mobile transmission, (UHF, 300 MHz to 3 GHz), super high frequency for Wi-Fi (sub-6GHz channel), microwave ovens and mobile networks (SHF, 3 GHz to 30 GHz), and extremely high frequency for 5G technology for future

transmission networks (EHF, 30 GHz, and 300 GHz). The summary of the radio frequency bands and applications are shown in Figure 1-1.

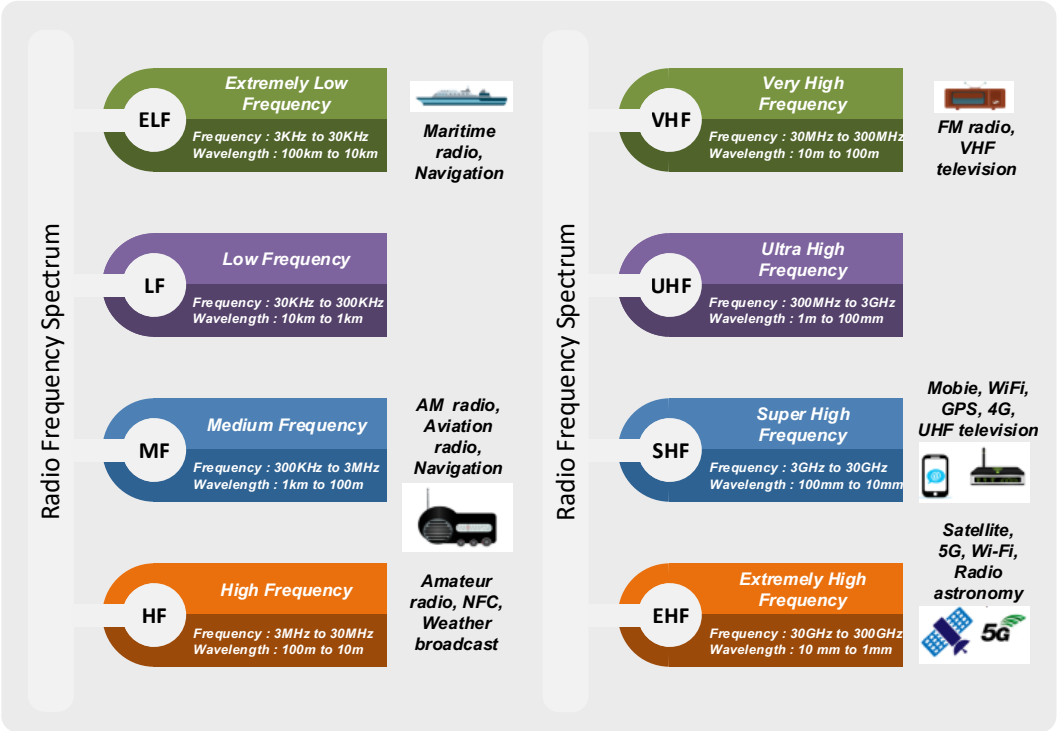


Figure 1-1 Frequency Bands and Applications

1.2 Transmitter Designs for Cutting-Edge Wireless Communication System

In modern society, the development of wireless communication technology has covered various applications ranging from smart phones to computers, laptops, tablets to Bluetooth technology. Moreover, wireless network users' dramatic growth urges the development of wireless communication technology to support more data-hungry services. For example, the 5G network adapted in cellular phones aims to achieve average download speeds of around 1Gbps and is expected to soon replace the 4G LTE connection. For the 5G network, the considered spectrum is given into two parts:

1. FR1: 410 MHz - 7125 MHz

2. FR2: 24250 MHz - 52600 MHz

Transmitter designs in each of the bands experience different challenges to meet 5G high-speed (1-10 Gbps) requirements.

1.2.1 Transmitter Designs for Wireless System in Millimeter-Wave Bands

The 5G network is the first system where frequencies higher than 6 GHz are considered. The motivation behind new spectrum portions is due to the difficulty of finding new frequency bands below sub-6GHz because of the coexistence of several wireless applications. mm-wave bands with significant amounts of unused or moderately used bandwidths as shown in Figure 1-2 [2] emerged as a suitable alternative to the current sub-6GHz bands. The use of mm-wave in the 5G network has shown evidenced to be a promising solution for the spectrum shortage within sub-6GHz bands of the current 4G LTE connection. Therefore, intensive research of designing new millimeter wave components operated beyond 6-GHz band has been conducted.

One key challenge in implementing a mm-wave wireless system is the maximum range to sustain reliable wireless links. According to Friis path loss equation, when the antenna gains are equal, the path loss increases with the square of the carrier frequency. Fortunately, the small dimension of the antenna, which is inversely proportional to the carrier frequency, allows high degree integration with other elements such as passive components and filters. Moreover, the

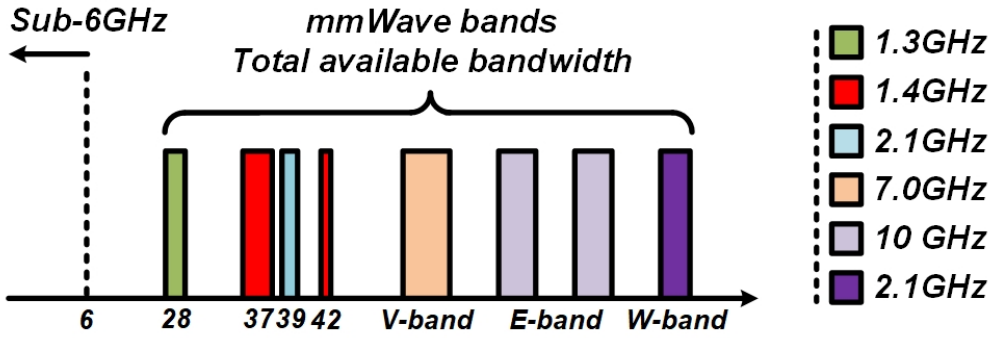


Figure 1-2 Mm-Wave Bands Total Available Bandwidth.

phased array technology, which can scan or switch the propagating beam, can be implemented in mm-wave wireless communication systems to overcome this challenge. Therefore, with an increased number of phased array elements, the transmitter designs with low power consumption and small area are required to supports emerging multibeam communications and directional sensing.

1.2.2 Transmitter Designs for Wireless System in Sub-6-GHz Bands

Due to the challenges of maintaining reliability for long-distance communication in mm-wave wireless systems, another trend of research has focused on improving spectral efficiency for densely packed spectrum in sub-6GHz bands. Higher data-rate of transmissions can be guaranteed by frequency-localized waveforms such as Orthogonal Frequency Division Multiplexing (OFDM). However, one of the most serious problems of the OFDM signal is the high peak-to-average ratio (PAPR). When the large PAPR signal passes through power amplifiers in transmitters, it introduces degradation in the linearity performance. The signal also reduces the overall system efficiency due to the power back-off (PBO) operation. Moreover, due to the tightly packed spectrum, the maximum level of out-of-band (OOB) power emissions becomes increasingly strict for wideband applications at sub-6-GHz bands.

The power amplifier (PA) is often the most power-hungry block in modern transceivers and is frequently operated in large PBO region with large PAPR signals. The overall system efficiency (SE) in the transceiver chain is significantly degraded, which leads to a shorter battery

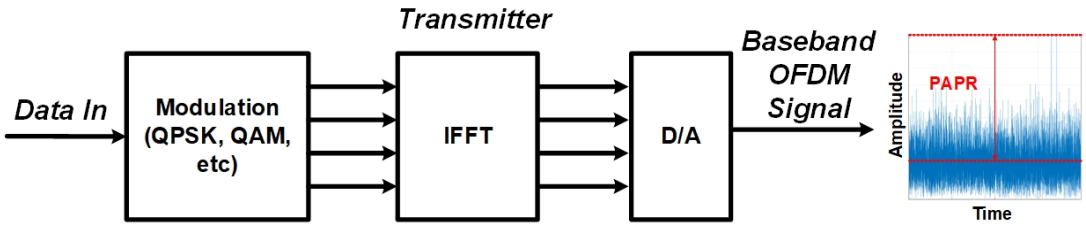


Figure 1-3 Orthogonal Frequency Division Multiplexing (OFDM).

life of mobile devices. Therefore, the transmitter and PA architectures with enhanced SE at PBO have been widely investigated.

1.3 Objectives and Organization of the Dissertation

This dissertation aims to explore the research opportunities for improving transmitter and PA designs in both sub-6-GHz and mm-wave bands. For sub-6-GHz bands, the research focus is to build the transmitter and PA, which is suitable for frequency-localized and high PAPR signals under densely packed sub-6-GHz bands with improved power efficiency. For mm-wave bands, the research is supported by Defense Advanced Research Project Agency (DARPA). The targeted application for this research is to build a wide-frequency range transmitter with low power and a small area to expand the usage of phased arrays in mm-wave for Department of Defense (DoD) systems.

Chapter 2 presents the comparison between transconductance-based conventional PA, switch-based conventional PA, and the digitally modulated switched-capacitor power amplification (SCPA). It is concluded that the SCPA provides a very efficient way of fast RF signal modulation and smaller chip area. Moreover, the digital circuits can be scaled with the CMOS technology progress with less dependency on the process-, voltage-, and temperature-variations.

Chapter 3 presents an efficient quadrature digital power amplifier as a standalone transmitter. A complex-domain Doherty (CDD) demonstrates the Doherty operation in a complex-domain with two vectors in different angles. It achieves high efficiency when two vectors have in-phase components in the complex domain by introducing an additional efficiency peak. The proposed SCPA employs CDD and dual-supply Class-G to achieve up to four efficiency peaks and excellent

SE at PBO. One of the ideal additional efficiency peaks is associated with the CDD at 6-dB PBO and two additional peaks are associated with the Class-G at 2.5-dB and 12-dB PBO.

Chapter 4 presents an 18–50-GHz mm-wave transmitter. The proposed mm-wave transmitter is designed for compact size and low-power consumption, and it is suitable for an element-level digital phased array system. A stacked double balanced active mixer mitigates the requirement for bulky inductors between transmitter building blocks so that the whole transmitter can be implemented within a limited area well within the array spacing to allow area for other functions.

Chapter 5 summarizes the theme and contribution of this thesis and Chapter 6 summarizes the future work on this topic.

2 CATEGORIES OF POWER AMPLIFIER

Since the 1980's, there has been a development of telecommunication generation(G) to the present day 4G and upcoming 5G in development progress. Other than the smartphone, there are many other mobile devices using wireless communication, such as laptops, iPad, and so on. Recent research focuses on wireless communication systems with applications in both mm-wave and sub-6-GHz bands. Modern wireless communication systems require RF transceivers with very low power consumption and increased energy efficiency to extend life for battery-powered devices. Thus, it is critical to improving the efficiency of the RF PA in the modern communication system, since it is one of the most power consuming blocks in mobile devices. The conventional power amplifiers, shown in Figure 2-1, with transconductance-based and switch-based architecture and digitally modulated power amplifier (DPA) are discussed in the following sections.

2.1 Transconductance-based Conventional Power Amplifier

Transconductance-based power amplifier, shown in Figure 2-1, is a standard small-signal amplifier conventional power amplifier. There are four types of transconductance-based power amplifiers, class A, class B, class AB, and class C amplifiers.

The class A amplifier, which biased the output stage transistor operates in the linear portion of its characteristic curves, achieves the highest linearity over all the transconductance-based

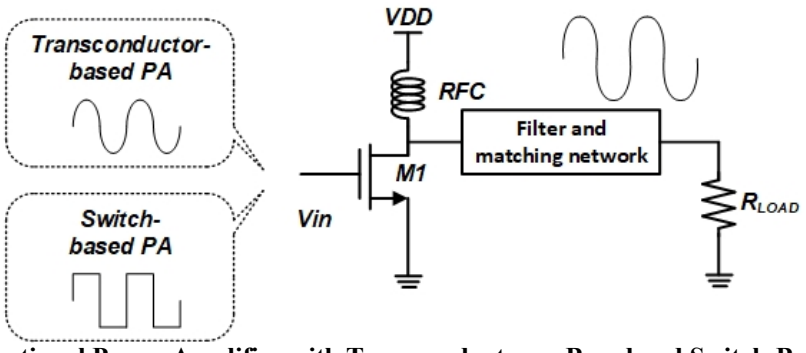


Figure 2-1 Conventional Power Amplifier with Transconductance-Based and Switch-Based Architecture.

amplifiers. However, in exchange for the highest linearity, the efficiency has to be compromised due to the power consumption from static bias current [3]. The drain current consists of DC current I_D and small-signal current i_0 which can be described as

$$i_D = I_D + i_0 \sin \omega_0 t \tag{1}$$

If RFC is large enough, all small-signal current is flowing to output, resulting in output small-signal voltage:

$$v_{out} = -i_0 R_{out} \sin \omega_0 t \tag{2}$$

where R_{out} is output resistance. The output power can be derived as

$$P_{out} = 0.5 \times \frac{v_0^{\,2}}{R_{out}} \tag{3}$$

since all other harmonic components except fundamental frequency (ω_0) are filtered out through the tank tuned at ω_0. The static power consumption of the amplifier circuit is

$$P_{DC} = I_D * V_{DD} = i_0 * V_{DD} \tag{4}$$

The overall efficiency can be calculated from the ratio of output power, P_{out} and DC power consumption, P_{DC}.

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\frac{v_o^{\,2}}{2R_{out}}}{io * VDD} = \frac{i_0 * R_{out}}{2V_{DD}} = \frac{v_0}{2V_{DD}} \tag{5}$$

The theoretical maximum efficiency is 50% since the maximum output voltage swing can be the same as the supply voltages. The efficiency will be lower if the loss of the output matching network is considered.

Compared to the class A amplifier, the transistor of the class B amplifier is biased such that the quiescent current is small or nearly zero. The higher efficiency is achieved since the transistor of the class B amplifier only conducts for half cycle. Thus, the fraction of the cycle of both non-

zero transistor current and the non-zero drain voltage is reduced. The ideal class B power amplifier has 50% of conduction angle, and the drain current can be described as

$$i_D = \begin{cases} i_0 \sin \omega_0 t, \ for \ \ i_D > 0 \\ 0 \qquad\quad , otherwise \end{cases} \tag{6}$$

The maximum efficiency is

$$\eta = \frac{P_{out}}{P_{DC}} = \frac{\pi}{4} \approx 0.785 \tag{7}$$

The class B amplifier suffers from severe linearity issues because of the substantial variation in the transistor bias current [4]. The class AB amplifier is the compromised solution, which has a conduction angle between 180º and 360 º and shows better linearity than class B and better efficiency than class A amplifier.

The class C amplifier, which has a conduction angle of less than 180 º, has enhanced efficiency with less output power. The ideal maximum efficiency of the class C amplifier is 100%.

2.2 Switch-based Conventional Power Amplifier

Instead of using a transistor as transconductor, switch-based amplifier shown in Figure 2-1 such as class D and class E amplifiers uses transistors as a switch. Recalling from the discussion of the transconductance-based power amplifiers, there is power consumption with simultaneous non-zero current and non-zero voltage in the transistor. If the product of voltage and current in the transistor becomes zero, there is no loss in the transistor and the efficiency will be 100% [3]. The trade-off is fixed output power since the operation of the switch-based power amplifier is based on the switch, instead of transconductance generating output power changing with the input signal.

Class E amplifier is one type of switching amplifier widely used in RF transmitters due to its high efficiency and power capability. The transistor M1 switches current into the output load, R_{out}, through a matching network. The product of voltage and current at the drain of the transistor

is ideally zero, thereby achieving theoretical efficiency of 100%. Class E amplifier delivers constant high output power with the use of switches instead of the transconductance.

2.3 Digitally Modulated Power Amplifier

Digital-friendly PA design takes advantage of state-of-the-art nano-scale CMOS process technology for high integration, fast processing speed, and robustness to process-, voltage-, and temperature (PVT) variation.

2.3.1 Digitally Modulated Power Amplifier

The cell-based structure is one of the major architectures due to no supply modulation and delta-sigma modulation [5] is required and can achieve wider bandwidth. As shown in Figure 2-2 [6]–[10], the cell-based structure controls the current flowing into the output load. The output voltage is proportional to the number of cells turned on. The signal distortion of the cell-based architecture can also be alleviated since the envelope and phase are modulated together in the same unit power amplifiers.

Maintaining good linearity at high output power is a challenge in the conventional DPA based on linear PA [11]. Most of the previously reported DPA show non-linear output power with amplitude control, as depicted in Figure 2-2. Cell-based DPA could be understood as a digital-to-

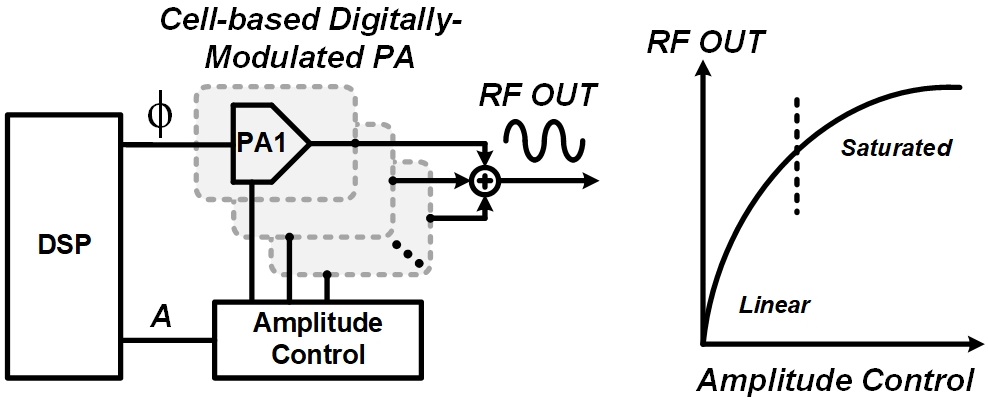


Figure 2-2 Digital RF Transmitter Based on Cells.

RF power converter since it converts digital signals to RF signals. The number of turned-on cells modulates the output impedance and output amplitude as in the design of the current-steering DAC. Each cell needs a higher impedance in order to achieve better linearity. Moreover, at higher output power, the output swing is large which causes the resistance variation. Therefore, most DPA with high output power requires additional resolution and another linearization technique, such as digital predistortion (DPD).

2.3.2 Switched-Capacitor Power Amplifier

The newly invented SCPA [12], as shown in Figure 2-3(a), has been widely investigated among the DPA architecture. Instead of switching current from the inductor as in a typical switching amplifier, it switches voltage applied to the capacitor. There are advantages to using the capacitor as a signal processing device. The capacitor occupies a small area in the CMOS process and can be easily split into small capacitors with high accuracy. By splitting the capacitors, the output amplitude can be controlled by the number of signals applied to the capacitance array. The concept of a digitally modulated SCPA is depicted in Figure 2-3(a). It is noted that effective

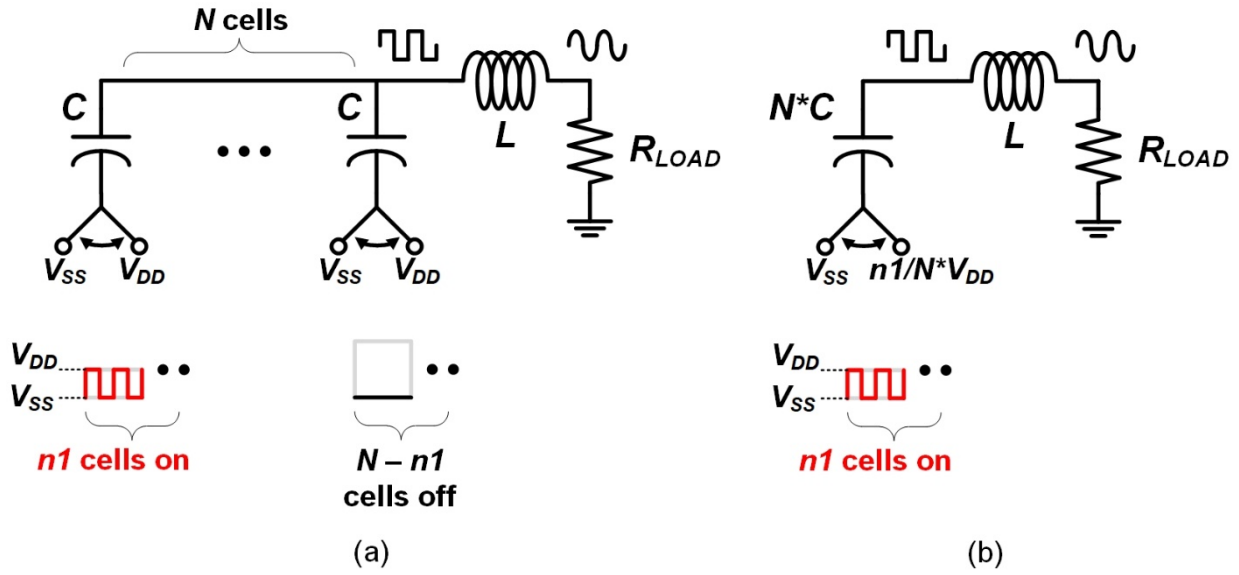


Figure 2-3 (a) Switched Capacitor power Amplifier (SCPA) (b) Equivalent Circuit of SCPA.

capacitance looking into the capacitor array is the same as the capacitance before split since all the capacitors are still connected to V_{DD} or V_{SS}, which is AC ground. As a result, LC resonance is maintained with split capacitors, regardless of the number of split capacitors switching between V_{DD} and V_{SS}.

The switched-capacitor circuit can provide high linearity since the matching between unit capacitors can be very accurate. The switched-capacitor circuit can be simplified with the equivalent circuit, as shown in Figure 2-3(b). From the perspective of linearity, it is the same with a capacitor switching between $n1/N*V_{DD}$ and V_{SS}, where n is the number of switching unit capacitors and N is the total number of unit capacitors.

2.3.2.1 Efficiency of Switched-Capacitor Power Amplifier

The ideal drain efficiency of the SCPA is 100%. However, the drain efficiency is degraded for the following reasons [12]: First, the power is dissipated in the output matching network due to the limited quality factor of the passive device. Second, the power dissipation is caused by the parasitic resistance and capacitance of output stage switches. Third, the power dissipates in the inverter chain, which is needed to drive the output switches. Lastly, the power loss is caused by the phase difference between the voltage and current at output switches. All the aforementioned efficiency degradation factors affect the whole efficiency. The last factor affects the efficiency degradation curve by different output power levels as described as follows: The effective impedance Zin seen from the operating switches of SCPA is modeled as in Figure 2-4. Zin is the

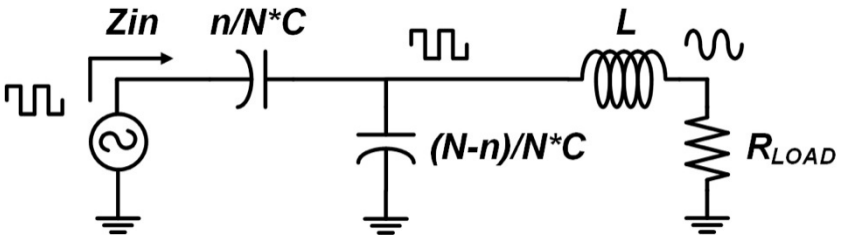


Figure 2-4 SCPA Model Seen from Operating Switches.

combined impedance of switching series capacitors, the disabled shunt capacitors, and the output matching network including output load. Zin can be derived as the following equation.

$$Zin = \frac{1}{j\omega \frac{n}{N} C} + \frac{1}{\frac{1}{R + j\omega L} + j\omega \frac{N-n}{N} C} \tag{8}$$

C is the total capacitance of the capacitor array. N is the total number of unit capacitors and n is the number of switching unit capacitors. The effective impedance is purely resistive when n is equal to N for full output power, which means 0º phase shift is achieved between voltage and current. As the number of switching unit capacitors decreases, Zin becomes more capacitive, making more phase shifts of current provided by the source. The amount of phase shift is also affected by the quality factor of the matching network. The phase shift can be minimized with a higher quality factor of the output matching network. In a qualitative explanation, the lower shunt capacitance, (N-n)/N*C, exists with the higher quality factor of the matching network, keeping Zin less capacitive. Also, there is more inductance in the matching network, which leads to more inductive impedance and less capacitive.

2.3.2.2 Conventional Class-G Switched-Capacitor Power Amplifier

A Class-G architecture with multiple supply voltages shows further improvement in the power efficiency of the transmitters. A conventional Class-G architecture uses a lower supply voltage to generate the lower output power levels and a higher supply voltage to generate higher power levels to achieve improved efficiency. By introducing multiple supply voltages, additional efficiency peaks can be generated in the PBO region. In the SCPA architecture, implementing the Class-G stage only requires additional switches connected to the additional supply voltages [13]. The SCPA with class-G architecture with ideal switch toggle between V_{DD}- V_{SS} or V_{DD2}- V_{SS} is shown in

Figure 2-5. However, as shown in Figure 2-6(a), due to the non-smoothing transition between two supply voltages, the efficiency is a discontinuity and is not improved compared to the original SCPA efficiency curve without the class-G scheme at the normalized voltage output from 0.5 to 1.

2.3.2.3 Enhanced Class-G Switched-Capacitor Power Amplifier

In the class-G SCPA amplifier, both supply voltages can simultaneously provide a higher and more continuous efficiency curve. Thus, the enhanced Class-G architecture [13] was proposed to improve the efficiency in the range of normalized Vout between 0.5 and 1. The comparison of the efficiency between conventional and enhanced Class-G architecture is shown in Figure 2-6(b).

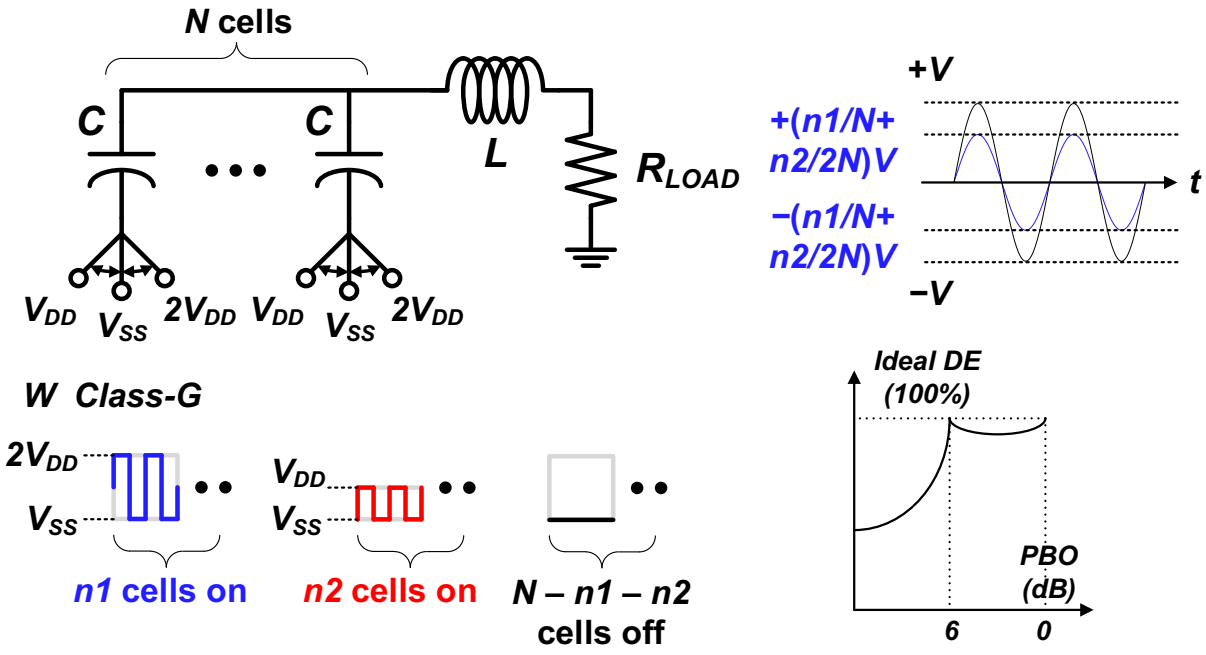


Figure 2-5 Class-G SCPA Architecture with Additional Switches.

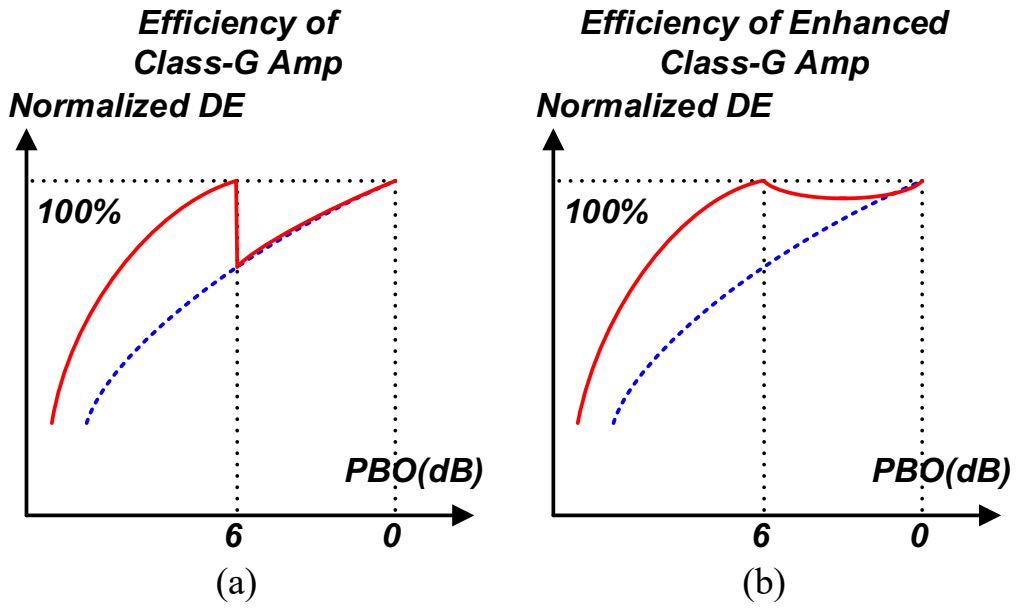


Figure 2-6 Efficiency versus Different Output Voltage of (a) Class-G SCPA (b) Enhanced Class-G SCPA.

3 A QUADRAUTRE CLASS-G COMPLEX-DOMAIN DOHERTY DIGITAL TRANSMITTER

3.1 Transmitter and Power Amplifier Architecture

Spectrally efficient and information-dense modulation, such as 1024 quadrature amplitude modulation (QAM) with OFDM, is widely used for modern communication standards to support the exponentially growing demand for a high data rate. However, such modulation schemes often result in a large PAPR for a transmitted signal. Therefore, the PA is frequently operated in a deep PBO region with degraded efficiency. Since the PA is the most power-hungry block in a transceiver chain, the overall SE of the transmitter is significantly degraded, which leads to shorter battery life in mobile devices. For enhanced SE at PBO, transmitter and PA architectures have been widely investigated, such as outphasing [14]–[19] and Doherty [20]–[24]. On the other hand, digital transmitters or digital PAs (DPAs) [12]–[13], [22]–[41] have been actively investigated recently. These DPAs provide simple architectures by incorporating the functionality of a digital-to-analog converter (DAC), mixer, driving amplifier, and PA into a single block, further enhancing the SE and reducing the power consumption of transmitters and PAs.

Conventional or digital transmitter architectures can be configured to combine different signals to increase output power (P_{OUT}), to enhance efficiency, or to express signals in the complex domain in different ways, such as simple power combining, outphasing, Doherty, and quadrature architectures, as shown in Figure 3-1.

3.1.1 Outphasing Architecture

The outphasing architectures, known as "linear amplifier with nonlinear components" (LINC), provide an amplitude modulation by combining two vectors from highly efficient switching PAs, such as Class-D, Class-E, or Class-F PAs. In the outphasing architecture, shown in Figure 3-1 (a), a signal component separator (SCS) generates two sinewave signals of constant envelopes with different phases, $\phi + \theta$ and $\phi - \theta$. The two constant-amplitude vectors generated by two sub-PAs, PA1 and PA2, are summed through a power-combing network, and the combined output amplitude is controlled by the outphasing angle (±θ), as shown in Figure 3-1(a). Therefore, the outphasing architecture requires phase modulators to change the phase angle of each vector in each PA. With phase modulators and an SCS, the outphasing architecture incurs increased complexity

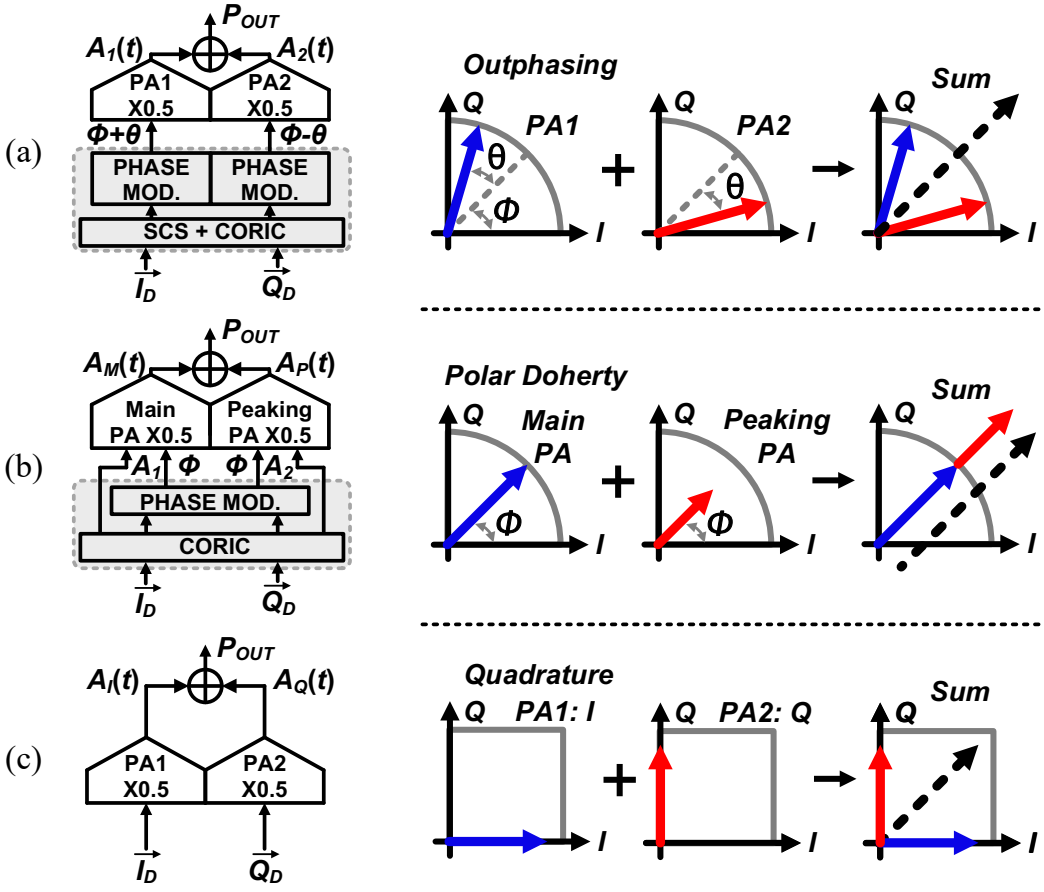


Figure 3-1 Transmitters Based on (a) Outphasing, (b) Polar Doherty, and (c) Quadrature Architectures. Solid and Dashed Arrows Indicate the Output Vectors of the Sub-PAs and the Combined PA, respectively.

and power consumption in the digital [14][15] or analog domain [16][17]. The increased complexity and power consumption make the outphasing system less attractive compared to the Doherty architecture which can operate on a modulated RF input signal directly.

3.1.2 Doherty Architecture

A typical Doherty architecture, composed of main and peaking PAs, demonstrates a significantly enhanced efficiency at PBO by creating an additional efficiency peak and a smooth efficiency transition between the efficiency peaks. Furthermore, the DPA-based polar architecture [12][13], [29]–[38] in Doherty configuration [22]–[24] can utilize switch-mode PAs for improved peak e fficiency. The DPA-based polar Doherty architecture also provides a unique advantage of precise control over the gain and turning-on point of the peaking PA. It leads to a fundamentally improved

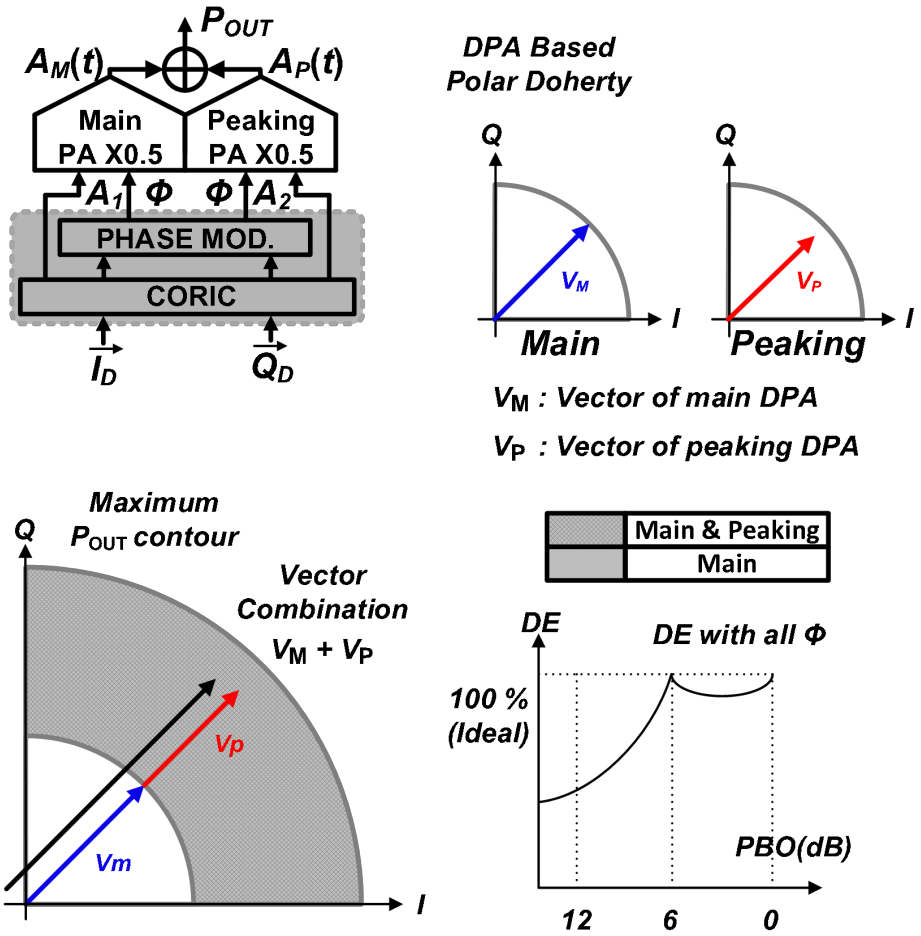


Figure 3-2 DPA-based Polar Doherty Architecture.

Doherty operation [22]. For a DPA-based polar Doherty architecture, shown in Figure 3-1 (b), two sub-PAs, the main and peaking PAs, generate vectors with the same phase and different amplitudes for an impedance modulation. The DPA-based polar Doherty architecture also requires a complex system with a coordinate rotation digital computer (CORDIC) and a wideband phase modulator.

The DPA-based polar Doherty architecture uses the same phase output vectors V_M and V_P and the operation in the complex domain is demonstrated in Figure 3-2. The area marked with a diagonal grid exhibits the high-power region, 0-6-dB PBO, where both main and peaking PAs are turned on. The white area depicts the low-power region, below 6-dB PBO, where only the main PA is turned on. The DPA-based polar Doherty architecture demonstrates one additional efficiency peak at 6-dB PBO as shown in Figure 3-2.

3.1.3 Quadrature Architecture

Compared to the DPA-based outphasing and polar Doherty architectures, a conventional quadrature DPA provides a simple system without any requirement for an SCS, CORDIC, or phase modulator. A conventional quadrature DPA with two sub-PAs, PA1 and PA2, generates P_{OUT} by combining two orthogonal in-phase (I) and quadrature (Q) vectors, as shown in Figure 3-1(c). However, P_{OUT} and efficiency are limited due to the orthogonal I and Q vector combination. Also, efficiency enhancement at PBO through load modulation cannot be achieved because two sub-PAs deliver orthogonal signals without any in-phase components.

3.2 Quadrature Complex-Domain Doherty Architecture

In the proposed quadrature CDD DPA, each sub-PA expresses the whole complex domain as a quadrature DPA to achieve load and phase modulation. The two sub-PAs can be configured to generate signals with different amplitudes as in the polar Doherty architecture and also to generate

signals with different phases as in the outphasing or quadrature architecture at the same time. The output signals of the main and peaking DPAs are coupled with XFMR in voltage mode Doherty (VMD) configuration [24]. The in-phase components of the two sub-PAs provide an efficiency peak at PBO in the complex domain, and the out-of-phase components provide a phase modulation without any dedicated phase modulators. Therefore, the proposed quadrature CDD DPA, as a standalone quadrature transmitter with efficiency enhancement at PBO, provides a simple architecture, small area, wide bandwidth, and high average efficiency. In addition, the Class-G technique [13],[23]–**Error! Reference source not found.** with multiple supply voltages can be a pplied to the proposed quadrature CDD DPA for further PBO efficiency enhancement.

3.2.1 Quadrature Complex-Domain Doherty Operation

The proposed CDD DPA consists of main and peaking quadrature DPAs, as shown in Figure 3-3. A quadrature architecture has the advantage of simple hardware and can more easily support wide bandwidth. In the conventional quadrature DPA, the sup-PAs are designated for each I and Q vector, which are combined in the radio frequency (RF) domain. For higher P_{OUT} and efficiency, IQ-combined unit vectors [25] are employed in the proposed CDD DPA. The IQ-combined unit vectors, generated from combing 25%-duty-cycle I and Q unit vectors, deliver maximum P_{OUT} at 45°/135°/225°/315° [25]. Unlike the conventional quadrature DPA, all the unit cells in the main and peaking DPAs can be assigned to the same IQ-combined unit vector simultaneously as shown in Figure 3-3 because there are no dedicated unit cells for I and Q signals. As a result, P_{OUT} of each main and peaking quadrature DPA is larger than that of the conventional quadrature DPA with dedicated I and Q. The maximum POUT and efficiency of the CDD DPA are significantly higher improved.

Each output vector of the main and peaking DPAs is represented as V_M and V_P, respectively. Since the main and peaking DPAs in the CDD DPA have a quadrature architecture, V_M and V_P are not limited to the same amplitude or phase as in the conventional outphasing or polar Doherty architecture, as shown in Figure 3-3. The output vectors with different amplitudes and phases are combined using a transformer (XFMR) power combiner to provide a high P_{OUT} and enhanced efficiency in the complex domain through load modulation and phase modulation.

The operation principle of the CDD DPA and an example of the V_M and V_P combination in the complex domain are depicted in Figure 3-3. The phase difference between V_M and V_P is represented as Φ in Figure 3-3. When $\Phi = 0$, V_M and V_P have equal phase of 45°, as in the polar Doherty architecture. The load modulation and ideal efficiency curve with a seamless transition

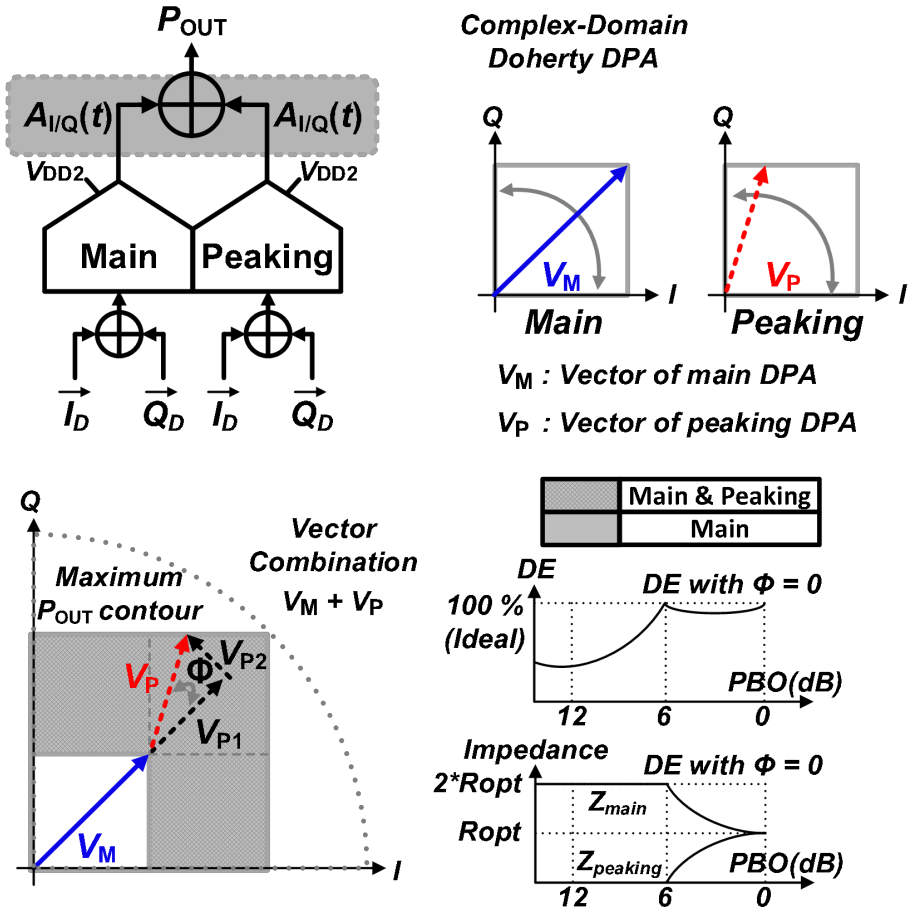


Figure 3-3 Quadrature CDD DPA Configuration and the Ideal Drain Efficiency with Load Modulation.

between the efficiency peaks of the CDD DPA at 45° are depicted in Figure 3-3. When $\Phi \neq 0$, V_{P} can be decomposed into two vectors, V_{P1} and V_{P2} which represent in-phase and 90° out-of-phase components relative to V_{M}, respectively. Here, V_{P1} relates to the load modulation for Doherty operation, while V_{P2} controls the phase of the output vector for the quadrature modulation. Therefore, the proposed CDD DPA enables Doherty operation with load modulation in the complex domain for enhanced efficiency and also achieves quadrature operation for phase modulation without any phase modulators. The load modulation of the proposed CDD DPA in the complex domain is detailed in Section II-B. The operation regions of the main and peaking DPAs in the complex domain are depicted in Figure 3-3. The operation region of each main and peaking DPA is represented by the square area, as in conventional quadrature DPAs. With an XFMR power combiner, the square operation area in the constellation map of the CDD DPA is extended to the high power region marked with a diagonal grid by 6 dB.

A triangular area in the first quadrant shown in Figure 3-5 is selected as an example to explain the vector combination. In the first quadrant, V_{M}, V_{P}, and the combination of V_{M} and V_{P} can deliver the maximum P_{OUT} at 45° with the IQ-combined unit vectors and can have phase

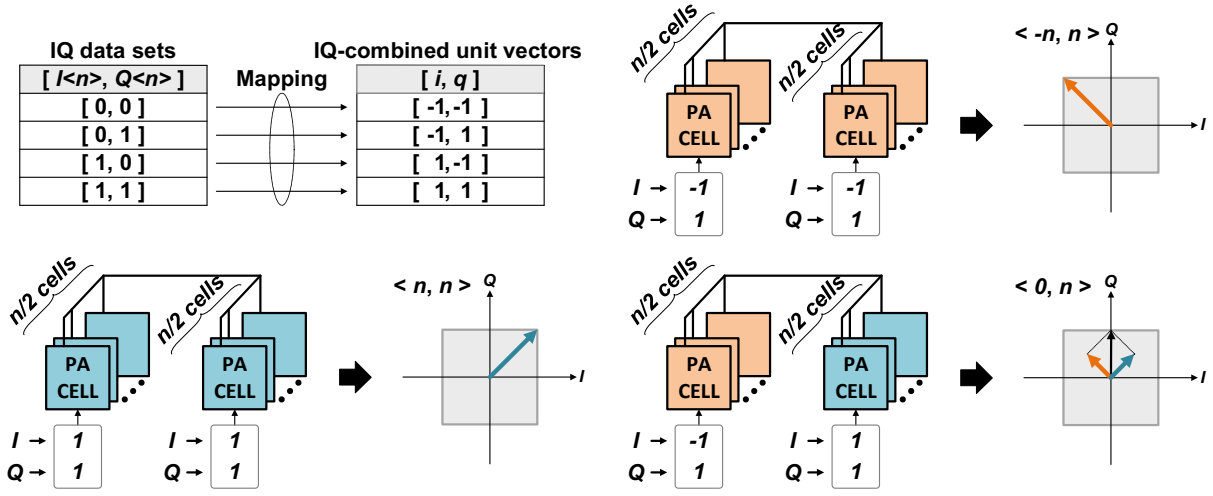


Figure 3-4 IQ-Combined Unit Vector.

rotation from 0° to 90°. The triangular area is segmented into three regions (Regions I, II, and III) according to the combination of V_M and V_P. The same segmentation can be applied to the remaining triangular area in the first quadrant and the other three quadrants as well. For region I, only V_M is considered because only the main DPA is turned on. For region II, the main DPA transmits V_M at 45° with the maximum P_{OUT}, while the peaking DPA delivers V_P at an angle between 45° and 90° to express the whole region II. For region III, V_M transmits P_{OUT} at a phase angle between 45° and 90°, while V_P shows a fixed 90° phase angle in the first quadrant.

3.2.2 Load Modulation in Complex-Domain Doherty Architecture

The conventional Doherty PA combines the main and peaking PA outputs using a λ/4 impedance inverter. However, the impedance inverter imposes limitations in bandwidth and chip area on the

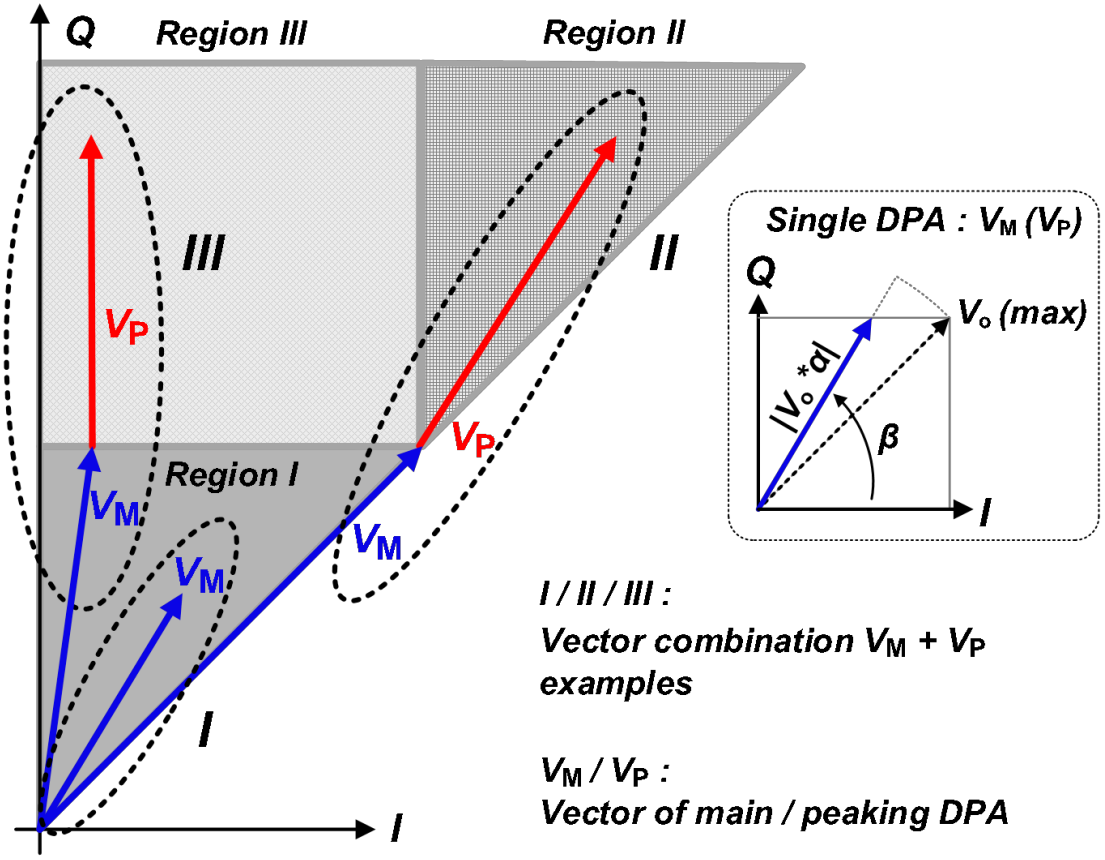


Figure 3-5 Vector Combination of the Quadrature CDD DPA.

conventional Doherty PA in low-GHz applications. On the other hand, the CDD DPA with XFMR eliminates the bulky transmission line for the impedance inverter while achieving a wide bandwidth and high PBO efficiency [11]. A simplified model, shown in Figure 3-6(a), is used to calculate the load impedance seen by the main and peaking DPAs in the CDD DPA. The output voltages of the two DPAs, V_{M} and V_{P}, are connected to a common load resistance R_{L} and can be written as

$$V_M = V_o * \alpha_1 * (cos\beta_1 + jsin\beta_1) \tag{1}$$

$$V_P = V_o * \alpha_2 * (cos\beta_2 + jsin\beta_2). \tag{2}$$

where V_{o} represents the maximum voltage that can be delivered by each DPA, as shown in Figure 3-5. α_1 (α_2) and β_1 (β_2) represent the amplitude and phase modulation factors of V_{M} (V_{P}), respectively, where $0 \leq \alpha_1$ (α_2) ≤ 1 and $0 \leq \beta_1$ (β_2) $\leq \pi/2$ in the first quadrant. In the polar Doherty architecture, V_{M} and V_{P} have equal phase, and the load is modulated based on the amplitude ratio between V_{M} and V_{P}, as shown in Figure 3-6 (b). In the outphasing architecture, V_{M} and V_{P} have equal amplitude, and the load is modulated depending on the phase difference between the two vectors θ, as shown in Figure 3-6 (c). In the CDD DPA, both the amplitude and the phase

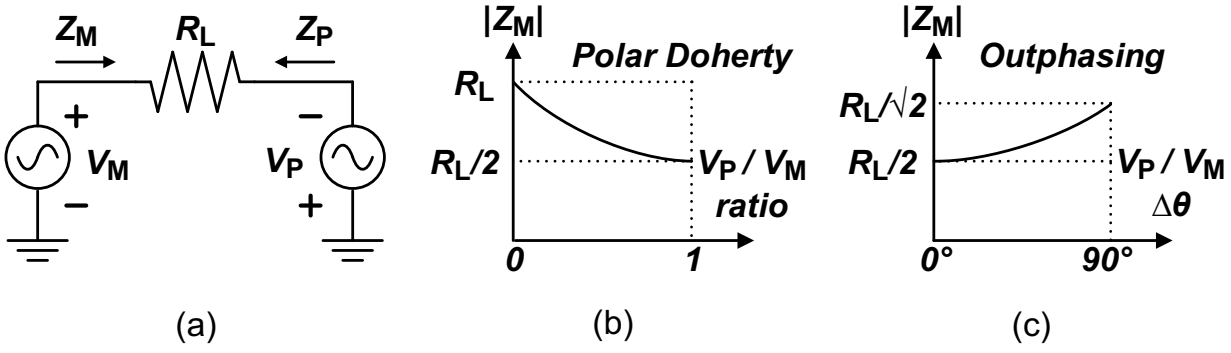


Figure 3-6 (a) Schematic Used to Calculate the Load Impedance Seen by the Main PA in (b) Polar Doherty (c) Outphasing Architecture.

of V_{M} and V_{P} can be varied independently. To analyze the load modulation in the CDD DPA, the triangular area introduced in Figure 3-5 is used. The general form of Z_{M} and Z_{P} can be written as

$$Z_{\mathrm{M}} = R_{\mathrm{L}} \frac{1}{1+V_{\mathrm{P}}/V_{\mathrm{M}}} = R_{\mathrm{L}} \frac{1}{1+\frac{\alpha_2}{\alpha_1} * e^{j(\beta_2-\beta_1)}} \tag{3}$$

$$Z_{\mathrm{P}} = R_{\mathrm{L}} \frac{1}{1+V_{\mathrm{M}}/V_{\mathrm{P}}} = R_{\mathrm{L}} \frac{1}{1+\frac{\alpha_1}{\alpha_2} * e^{j(\beta_1-\beta_2)}}. \tag{4}$$

In region I, since the peaking DPA is turned off, the load impedance seen by the main DPA is R_{L}. In region II, while the main DPA transmits the maximum output voltage, the peaking DPA modulates the amplitude and phase of the combined output voltage. Therefore, Z_{M} and Z_{P} are modulated with the amplitude and phase of the peaking DPA. For Z_{M} and Z_{P} in region II, α_1 is

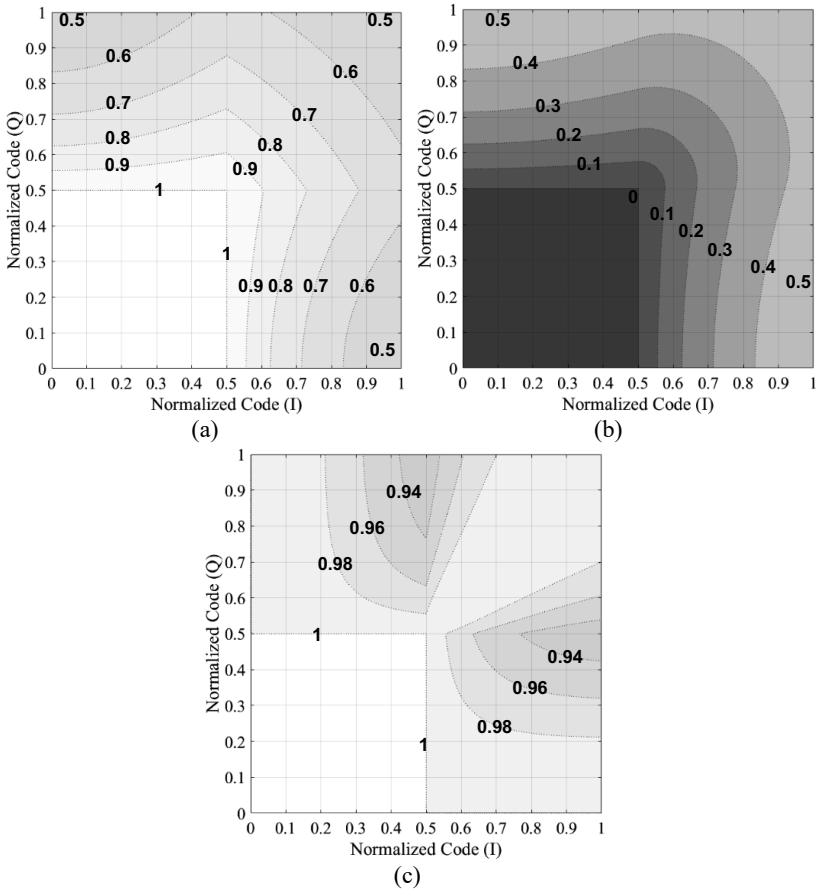


Figure 3-7 Normalized Absolute Impedance Seen by the (a) Main and (b) Peaking DPAs. (c) Normalized Efficiency of the CDD Technique with Different Vector Combinations.

equal to one, and $e^{j(\beta_1-\beta_2)}$and $e^{j(\beta_2-\beta_1)}$ are associated with the phase difference between the two DPA vectors. In region III, the amplitude and phase of the main DPA are changed to represent the boundary with region III. The amplitude of the peaking DPA is changed while the phase is maintained at 90° in the first quadrant. For Z_{M} and Z_{P}, both $\alpha_1$and α_2 change according to the amplitude modulation of the main and peaking DPAs. Also, β_1 changes according to the phase modulation of the main DPA while β_2 is fixed at 90°. The normalized absolute values of complex load impedance in the complex domain seen by the main and peaking DPAs are illustrated in Figure 3-7 (a) and (b), respectively. With the calculated load impedance seen by both DPAs, the output power, $P_{\mathrm{OUT\_M}}$ and $P_{\mathrm{OUT\_P}}$, and the efficiency, η_{M} and η_{P}, of both DPAs are expressed as follows:

$$P_{\mathrm{OUT\_M}} = |{V_{\mathrm{M}}}^2|/{Z_{\mathrm{M}}}^* \tag{5}$$

$$P_{\mathrm{OUT\_P}} = |{V_{\mathrm{P}}}^2|/{Z_{\mathrm{P}}}^* \tag{6}$$

$$\eta_{\mathrm{M}} = \frac{Re|Z_{\mathrm{M}}|}{|Z_{\mathrm{M}}|} * \eta_{\mathrm{M\_DPA\_PBO}} \tag{7}$$

$$\eta_{\mathrm{P}} = \frac{Re|Z_{\mathrm{P}}|}{|Z_{\mathrm{P}}|} * \eta_{\mathrm{P\_DPA\_PBO}} \tag{8}$$

where ${Z_{\mathrm{M}}}^*$ and ${Z_{\mathrm{P}}}^*$ are the complex conjugate of the load impedance seen by the main and peaking DPAs. The imaginary parts of the output power $P_{\mathrm{OUT\_M}}$ and $P_{\mathrm{OUT\_P}}$ cancel each other out in all combination cases of V_{M} and V_{P}. The efficiency of each DPA is degraded due to the imaginary impedance seen by each DPA and the PBO operation, as shown in (6). The efficiency characteristics of the main and peaking DPAs at PBO are expressed as $\eta_{\mathrm{M\_DPA\_PBO}}$ and $\eta_{\mathrm{P\_DPA\_PBO}}$, respectively. The two-dimensional normalized efficiency of the CDD technique is illustrated in

Figure 3-7 (c). The efficiency degradation due to the imaginary impedance is more dominant with a larger phase difference between V_M and V_P.

3.2.3 Quadrature Class-G Complex-Domain Doherty Architecture

The Class-G technique can be applied with the CDD to create additional efficiency peaks at PBO. The proposed quadrature Class-G CDD DPA further improves the average efficiency by adding three additional efficiency peaks at PBO and preserves the advantages of simple architecture as a quadrature transmitter. Figure 3-8 illustrates the operation region in the complex domain of the proposed quadrature Class-G CDD DPA. The high- and low-power regions associated with the CDD operation shown in Figure 3-3 are represented with and without a diagonal grid, respectively, in Figure 3-8. Also, the grey-shaded area depicts the Class-G operation

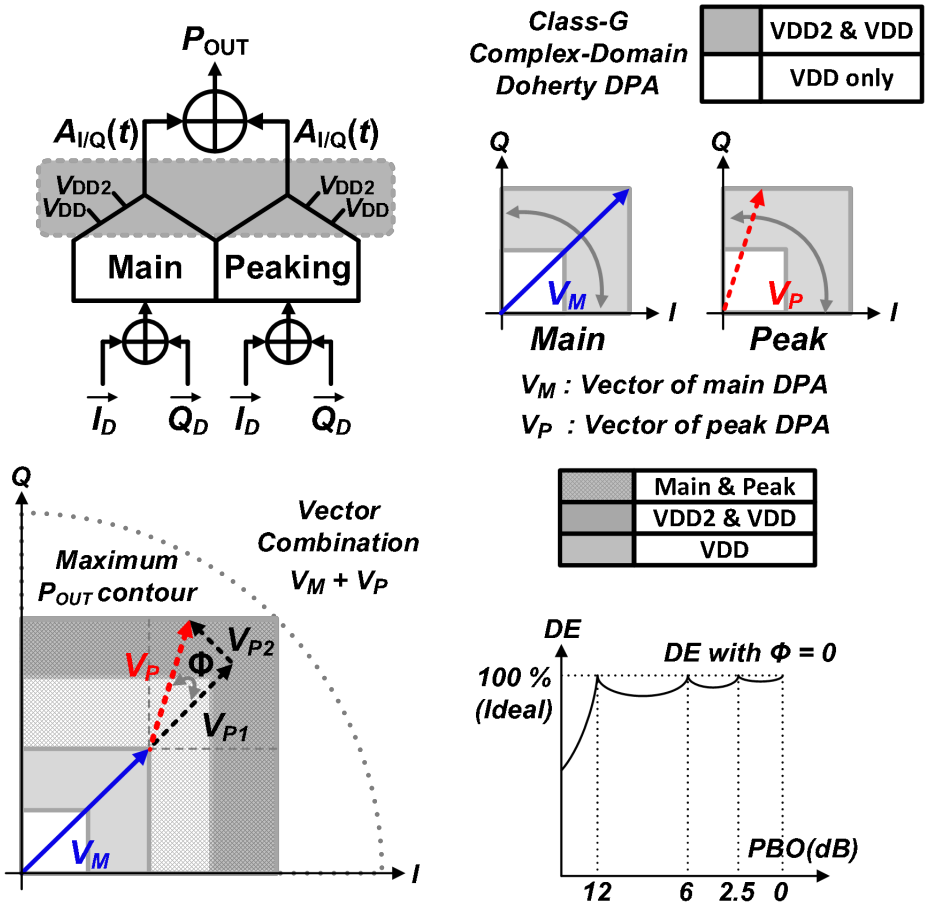


Figure 3-8 Quadrature Class-G CDD DPA Configuration and the Ideal Drain Efficiency.

regions with the supply voltages of both V_{DD} and V_{DD2}, assuming $V_{DD2} = 2V_{DD}$, while the white area represents the normal operation regions with only one supply voltage of V_{DD}. The ideal efficiency curve of the DPA with CDD, Class-G, and seamless transitions between the efficiency peaks at 45° is shown in Figure 3-8. Two additional efficiency peaks at 2.5-dB and 12-dB PBO and another efficiency peak at 6-dB PBO are added, associated with the Class-G and CDD operations, respectively.

3.3 Output Power and Efficiency of Quadrature Complex-Domain Doherty Switched-Capacitor Power Amplifier

The classical Doherty PA architecture combines the main and peak PA outputs by a λ/4 impedance inverter as shown in Figure 3-9(a). A new Doherty amplifier architecture [24] realized by two voltage-mode polar PAs demonstrates an efficient XFMR power combining as illustrated in Figure 3-9(b). The turning-on point of the peak PA and the gain relationship between the two PAs are the keys to achieve the desired operation of the classical Doherty PA. A variety of techniques have been employed to improve the performance of the classical Doherty PA, such as asymmetric power splitting and dynamic biasing. However, most of the techniques require dedicated design for accurate input splitting design or bias selection. The turning-on

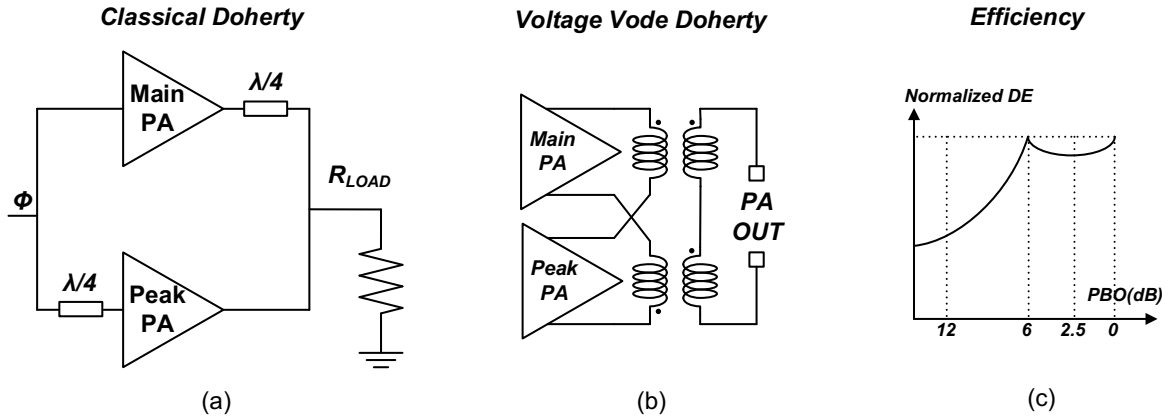


Figure 3-9 (a) Classical Doherty (a) Voltage Mode Doherty (c) Normalized Drain Efficiency Power Amplifier

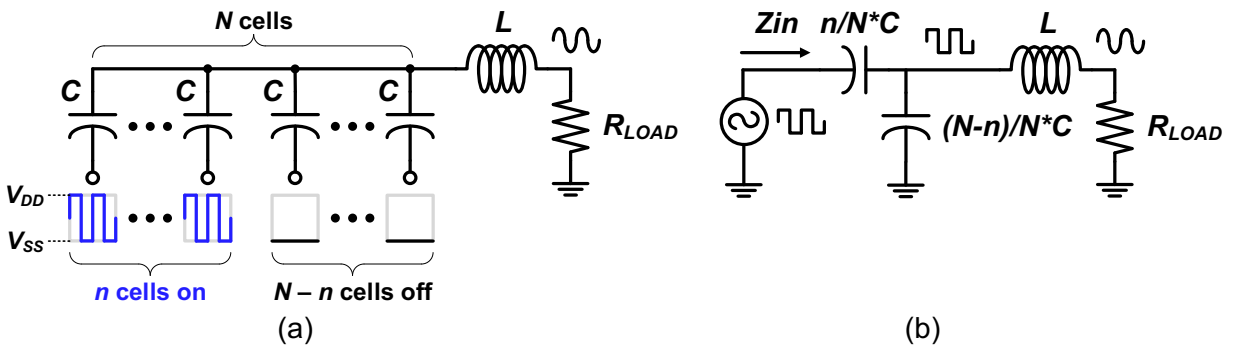


Figure 3-10 (a) Schematic and (b) Equivalent Circuit of Basic SCPA Architecture.

point of the peaking PA and the gain relationship between the main and peak PAs are the keys to achieving the desired operation of the classical Doherty PA. The digital Doherty PA architecture consisted of two DPAs [12]–[13], [22]–[41], is developed to improve the pe rformance of classical Doherty PA architecture [21]. The digital Doherty PA architecture can precisely control the gain relationship between the two PAs and the turning-on point of the peaking PA. It leads to a fundamentally improved Doherty operation and enhanced PBO efficiency [21]. Among DPA architectures, the SCPA [12]–[13], [24]–[30], [39]–[41] has been ex tensively investigated due to its high energy efficiency and excellent linearity. Compared to a quadrature SCPA with dedicated I/Q cells sharing a capacitor top plate, a quadrature IQ-cell-shared SCPA [25]–**Error! Reference source not found.**, [40]– [41] with 50% duty-cycle IQ-c ombined unit vectors based on 25% duty-cycle I/Q vectors provides an increased P_{OUT} and efficiency. Therefore, the quadrature IQ-cell-shared SCPA is chosen as a base architecture for each sub-PA in the CDD DPA. Figure 3-10 shows an equivalent circuit of the SCPA with a capacitor array, an inductor L, and an output resistance R_{OPT} connected in series, which is used to calculate the P_{OUT} and ideal drain efficiency. The number of capacitors switched at RF (*On*) and unswitched (*Off*) in the capacitor array is depicted as a bar chart in Figure 3-11, Figure 3-12, and Figure 3-14. Square waves with a 90° phase difference on top of the bar chart indicate IQ-combined vectors A and B, respectively.

3.3.1 Quadrature IQ-Cell-Shared SCPA

As shown in Figure 3-11 (a), a quadrature IQ-cell-shared SCPA generates output vectors by combining two orthogonal vectors, A and B, as in a conventional quadrature SCPA [39]. Therefore, the output voltage and P_{OUT} can be calculated as follows [26]:

$$|V_{OUT}| = \frac{2}{\pi}\sqrt{\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2}\, V_{DD} \tag{9}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{4}{\pi}\left[\left(\frac{a}{N}\right)^2 + \left(\frac{b}{N}\right)^2\right]\frac{{V_{DD}}^2}{R_{opt}} \tag{10}$$

$$Q_{\mathrm{LOAD}} = \frac{2\pi f L}{R_{\mathrm{OPT}}} = \frac{1}{2\pi f C_{\mathrm{TOT}} R_{\mathrm{OPT}}} \tag{11}$$

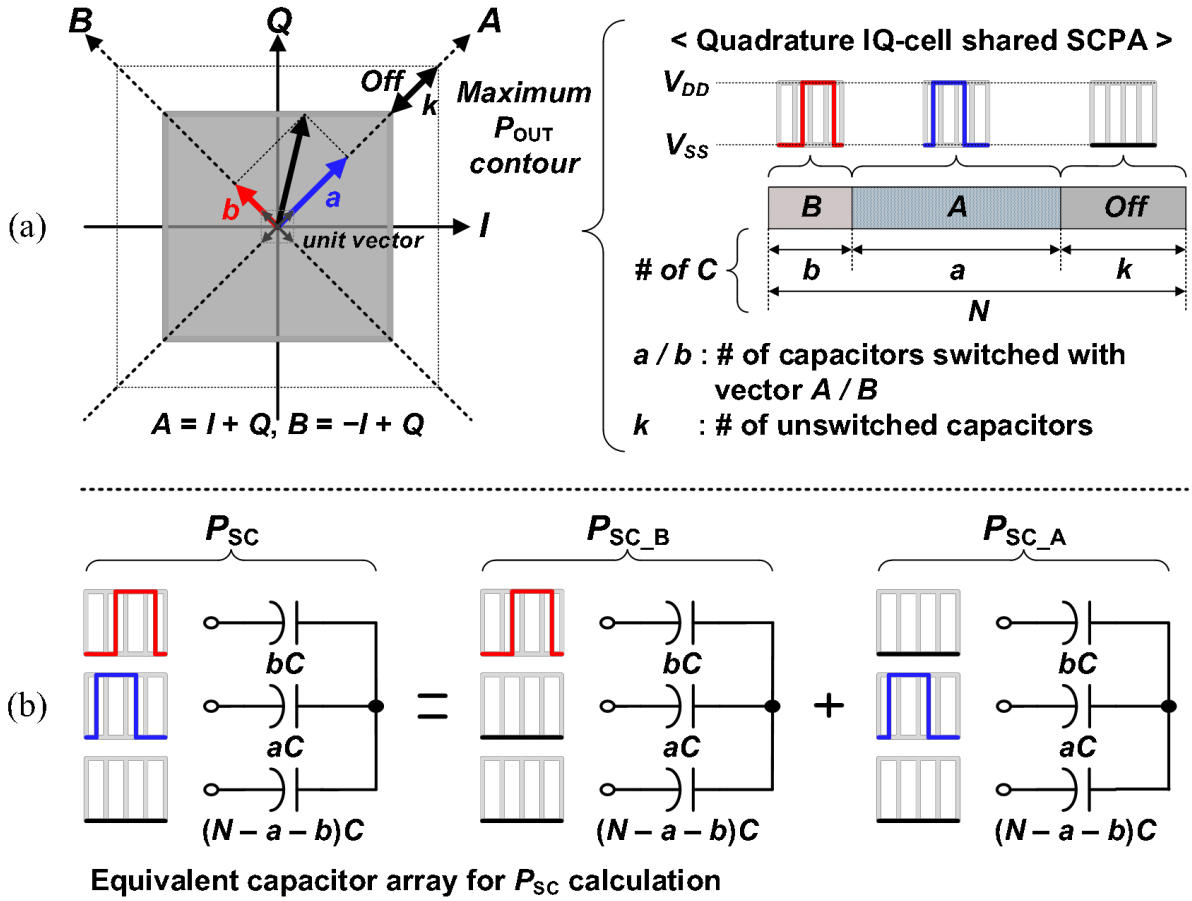


Figure 3-11 (a) Quadrature IQ-cell-shared SCPA Operation and (b) the Equivalent Circuit for Total Dynamic Power Dissipation (P_{SC}) Calculation in the Capacitor Array.

where N is the total number of capacitors in the capacitor array, Q_{LOAD} is the loaded quality factor of the output matching network, and a and b are the numbers of capacitors switched between V_{DD} and V_{SS}, representing vectors A and B, respectively. The Q_{LOAD} is assumed to be two in the efficiency calculation. Unlike the conventional quadrature SCPA architecture with dedicated I and Q cells, a and b are not limited to $N/2$, as shown in Figure 3-11 (a), and the relationship among a, b, and N is given by $0 \leq a + b \leq N$. The total dynamic power dissipation (P_{SC}) in the capacitor array can be calculated as the sum of each P_{SC} for vectors A and B, $P_{\mathrm{SC\_A}}$ and $P_{\mathrm{SC\_B}}$, respectively, from the equivalent circuit shown in Figure 3-11 (b). P_{SC} is given by [26]:

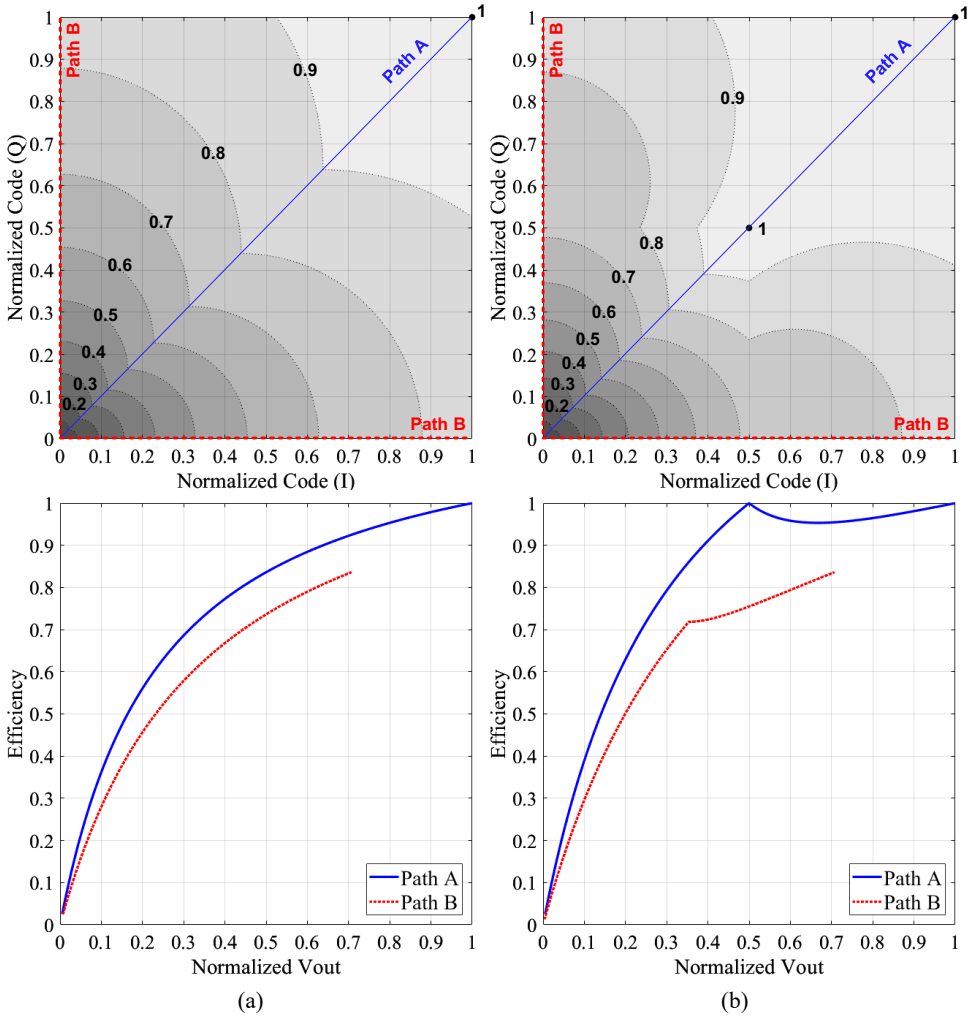


Figure 3-12 Theoretical 2-D Drain Efficiency Map in Quadrant I of (a) Quadrature IQ-cell-shared SCPA and (b) Quadrature CDD IQ-cell-shared SCPA.

$$P_{SC} = P_{SC\_A} + P_{SC\_B} \tag{12}$$

$$P_{SC\_A} = \frac{a(N-a)}{N^2} C_{TOT} {V_{DD}}^2 f \tag{13}$$

$$P_{SC\_B} = \frac{b(N-b)}{N^2} C_{TOT} {V_{DD}}^2 f. \tag{14}$$

The quadrature IQ-cell-shared SCPA is analyzed in a pair coupled through an ideal power combiner to fairly compare the efficiency to that of other CDD DPAs introduced in Section 3.3. The maximum P_{OUT} of the quadrature IQ-cell-shared SCPA in a pair is the same as that of the CDD DPAs with efficiency enhancement techniques in Sections 3.3.2 and 3.3.3, and the ideal drain efficiency is illustrated in Figure 3-12 (a).

3.3.2 Quadrature Complex-Domain Doherty IQ-Cell-Shared SCPA

The proposed CDD DPA can be configured with two quadrature IQ-cell-shared main and peaking SCPAs. The bar charts in Figure 3-13 depict the number of capacitors switched with

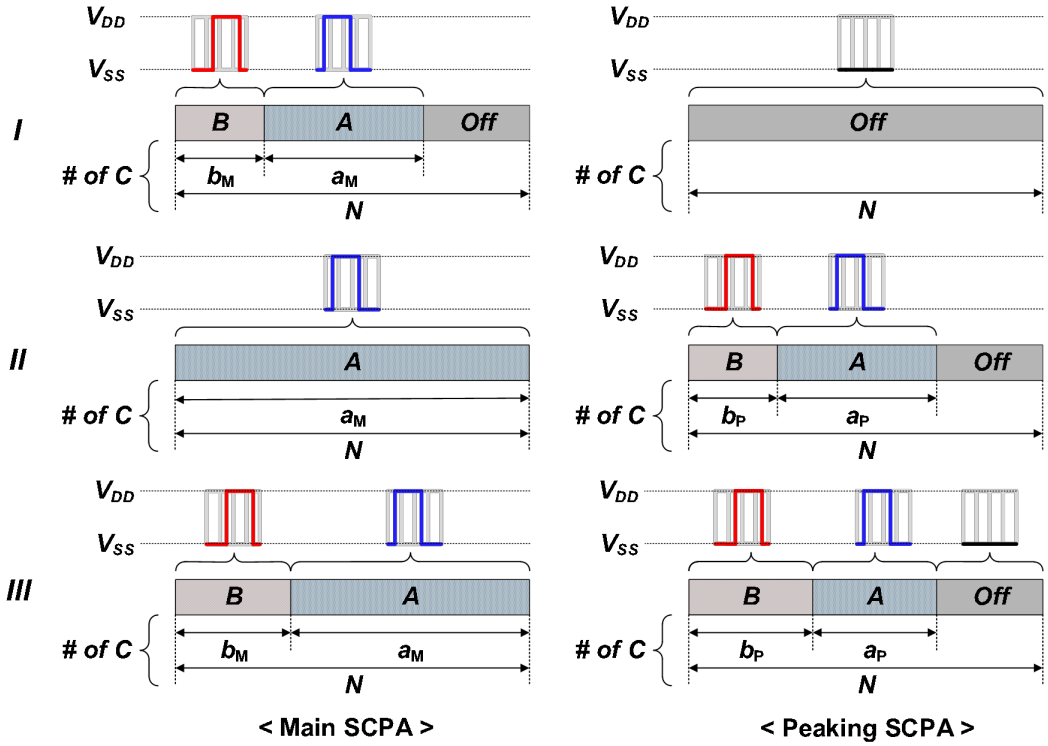


Figure 3-13 Vector Components in Quadrature CDD IQ-cell-shared SCPA in Three Different Regions.

vectors A and B in each main and peaking SCPA. a_{M} (b_{M}) and a_{P} (b_{P}) represent the capacitors switched with vector A (B) in the main and peaking SCPAs, respectively, and V_{M} and V_{P} indicate the sum of vectors A and B in each SCPA. Since the main (peaking) SCPA uses the IQ-combined unit vectors, as shown in Figure 3-11 (a), if all the capacitors are switched with vector A only (a_{M} (a_{P}) $= N$), the output vector V_{M} (V_{P}) is at a 45° angle to the I-axis in the IQ plane. If the numbers of capacitors switched with vectors A and B are equal (a_{M} (a_{P}) $= b_{\mathrm{M}}$ (b_{P}) $= N/2$), the output vector V_{M} (V_{P}) is along the Q-axis in the IQ plane. The same triangular area segmented into three regions in the first quadrant shown in Figure 3-5 is used for P_{OUT} and efficiency analysis of the CDD DPA employing quadrature IQ-cell-shared SCPAs.

In region I, because only the main SCPA operates, P_{OUT} and P_{SC} can be expressed in the same manner as in (9)–(14). For regions II and III, the output voltage and P_{OUT} can be calculated by replacing a and b in equations (9)–(10) with $a_{\mathrm{M}} + a_{\mathrm{P}}$ and $b_{\mathrm{M}} + b_{\mathrm{P}}$, respectively, and expressed as follows:

$$|V_{OUT}| = \frac{2}{\pi}\sqrt{\left(\frac{a_M+a_P}{N}\right)^2 + \left(\frac{b_M+b_P}{N}\right)^2}\,V_{DD} \tag{14}$$

$$P_{OUT} = \frac{1}{2}\frac{|V_{OUT}|^2}{R_{OPT}} = \frac{4}{\pi}\left[\left(\frac{a_M+a_P}{N}\right)^2 + \left(\frac{b_M+b_P}{N}\right)^2\right]\frac{{V_{DD}}^2}{R_{opt}}. \tag{15}$$

In region II, the peaking SCPA operates for high P_{OUT}, and all the capacitors in the main SCPA are switched with vector A. In the proposed CDD DPA, V_{M} is at 45°, and V_{P} varies between 45° and 90° to express the whole region II, as shown in Fig. 3. Only the peaking SCPA dissipates dynamic power in the capacitor array because all the capacitors in the main SCPA are only switched with the same vector A. P_{SC} can also be obtained from (12)–(14).

In region III, V_{M} varies between 45° and 90°, as shown in Figure 3-5, and all the capacitors in the main SCPA are switched with a combination of vectors A and B. The relationship among a_{M}, b_{M}, and N for the main SCPA is given by $a_{\mathrm{M}} + b_{\mathrm{M}} = N$ and $a_{\mathrm{M}} \geq b_{\mathrm{M}}$. For the peaking SCPA, V_{P} is maintained at 90°, and the relationship among a_{P}, b_{P}, and N for the peaking SCPA is given by $a_{\mathrm{P}} + b_{\mathrm{P}} \leq N$ and $a_{\mathrm{P}} = b_{\mathrm{P}}$. From the relationships among $a_{\mathrm{M}}, a_{\mathrm{P}}, b_{\mathrm{M}}, b_{\mathrm{P}}$, and N, the P_{SC} of each main and peaking SCPA can be calculated separately from (12)–(14). The total P_{SC} can be obtained as follows:

$$P_{SC} = P_{SC\_A_M} + P_{SC\_B_M} + P_{SC\_A_P} + P_{SC\_B_P} \tag{16}$$

where $P_{\mathrm{SC\_A_M}}$ ($P_{\mathrm{SC\_A_P}}$) and $P_{\mathrm{SC\_B_M}}$ ($P_{\mathrm{SC\_B_P}}$) are P_{SC} for vectors A and B, respectively, in the main (peaking) SCPA. For the first quadrant, the ideal drain efficiency is depicted in Figure 3-12 (b).

3.3.3 Complex-Domain Doherty with Quadrature IQ-cell Shared SCPA

An enhanced-efficiency Class-G technique provides an SCPA with additional efficiency peaks and seamless transitions in both efficiency and linearity characteristics [13]. In the Class-G SCPA, the output vectors with an amplitude of V_{DD2} in the SCPA cell need to be distributed to the *Off* cells to minimize P_{SC} in the capacitor array and to enhance efficiency [13].

An example of the vector distribution from the switched to the unswitched capacitors in the main and peaking SCPA is illustrated with arrows and square waves in Figure 3-14. The same analytical method for the three regions in the first quadrant (Figure 3-5) is used to calculate P_{OUT} and the efficiency of the quadrature Class-G CDD IQ-cell-shared SCPA. The number of capacitors switched with vectors A and B with an amplitude of V_{DD2} in the main (peaking) SCPA is defined as a_{M} (a_{P}) and b_{M} (b_{P}), respectively, and the number of unswitched capacitors is defined as k. α and β represent the number of *Off* cells that receive the distributed vectors A and B, respectively,

and the number of capacitors switched with vectors A and B with an amplitude of V_{DD} after the distribution is2α and 2β, correspondingly. The vector distribution is applied to the main SCPA in region I and the peaking SCPA in regions II and III. The relationship among a_{M} (a_{P}), b_{M} (b_{P}), α, β, k, and N in the SCPA is as follows: In region I (region II), when $k < N/2$, the relationship among a_{M} (a_{P}), b_{M} (b_{P}), α, β, and k is $0 \le \alpha \le a_{\mathrm{M}}$ (a_{P}), $0 \le \beta \le b_{\mathrm{M}}$ (b_{P}), and $\alpha + \beta = k$. The amplitude of vectors A and B of the main (peaking) SCPA after vector distribution are $(a_{\mathrm{M}} - \alpha)V_{\mathrm{DD2}} + 2\alpha V_{\mathrm{DD}}$ ($(a_{\mathrm{P}} - \alpha)V_{\mathrm{DD2}} + 2\alpha V_{\mathrm{DD}}$) and $(b_{\mathrm{M}} - \beta)V_{\mathrm{DD2}} + 2\beta V_{\mathrm{DD}}$ ($(b_{\mathrm{P}} - \beta)V_{\mathrm{DD2}} + 2\beta V_{\mathrm{DD}}$). When $k \ge N/2$, all the switched capacitors with vectors A and B with an amplitude of V_{DD2} distribute vectors with an amplitude of V_{DD} to the unswitched capacitors. Therefore, the amplitudes of the vectors A and B after the distribution are $2\alpha V_{\mathrm{DD}}$ and $2\beta V_{\mathrm{DD}}$, respectively. In region III, the relationship among a_{P}, b_{P}, α, β, k, and N in region II can still be applied with additional constraints, $a_{\mathrm{P}} = b_{\mathrm{P}}$ and $\alpha = \beta$, because the numbers of capacitors switched with vectors A and B in the peaking SCPA are equal.

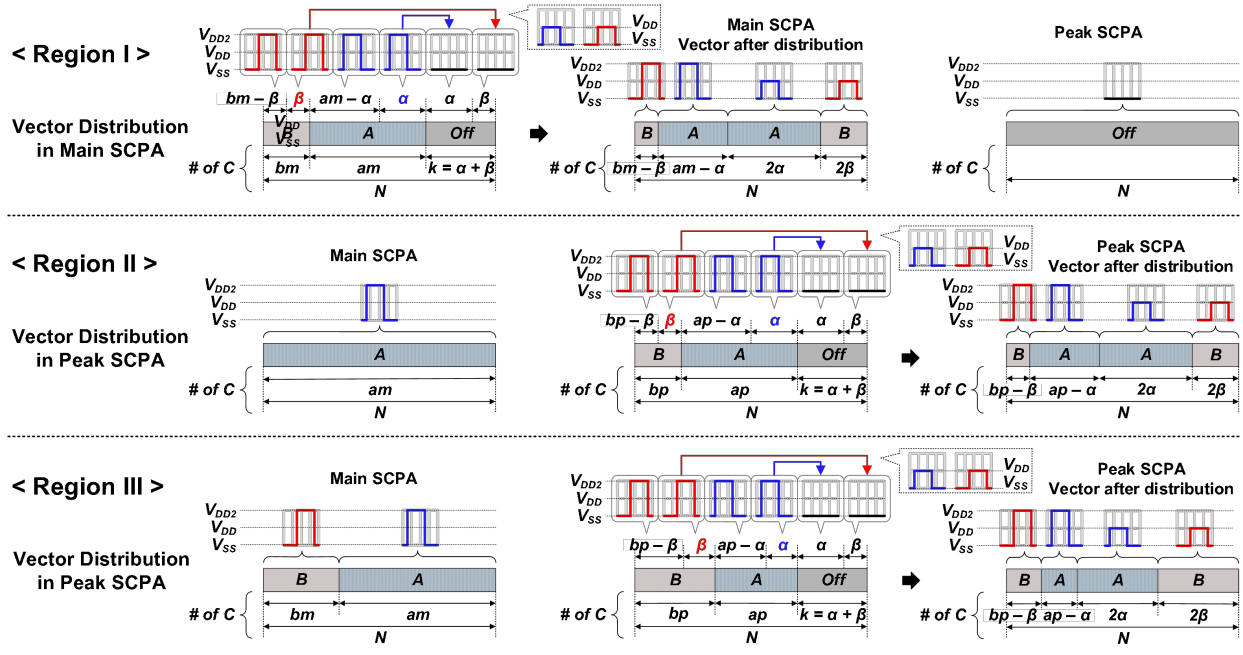


Figure 3-14 Example of Vector Distribution in Quadrature Class-G CDD IQ-cell-shared SCPA.

The output voltage and P_{OUT} can be obtained from (15)–(16) by replacing V_{DD} with V_{DD2} because the vector distribution does not change P_{OUT}. The total P_{SC} is obtained by summing the P_{SC} of each main and peaking SCPA, as in Section III-B. For the main and peaking SCPAs without vector distribution, P_{SC} can be calculated from (12)–(14). On the other hand, with vector distribution, there are two different supply voltages, V_{DD2} and V_{DD}, applied to the capacitors. Therefore, the power consumption for each capacitor switched between V_{DD2} and V_{SS} (P_{SC_A1}, P_{SC_B1}), switched between V_{DD} and V_{SS} (P_{SC_A2}, P_{SC_B2}), and unswitched (P_{SC_A3}, P_{SC_B3}) needs to be calculated separately. In region I (II and III), with the vector distribution in the main (peaking) SCPA and $k < N/2$, P_{SC} of the main (peaking) SCPA, $P_{SC\_A_M} + P_{SC\_B_M}$ ($P_{SC\_A_P} + P_{SC\_B_P}$), can be obtained as follows [26]:

$$P_{SC\_A_M} + P_{SC\_B_M} = \left(P_{SC\_A1} + P_{SC\_A2} + P_{SC\_A3}\right) + \left(P_{SC\_B1} + P_{SC\_B2} + P_{SC\_B3}\right) \tag{17}$$

$$P_{SC\_A_M} = \left[\frac{4(a_M-\alpha)}{N}\left(\frac{N-a_M}{N}\right)^2 + \frac{2\alpha}{N}\left(\frac{N-2a_M}{N}\right)^2 + \frac{b_M+\beta}{N}\left(\frac{2a_M}{N}\right)^2\right] C_{TOT}{V_{DD}}^2 f \tag{18}$$

$$P_{SC\_B_M} = \left[\frac{4(b_M-\beta)}{N}\left(\frac{N-b_M}{N}\right)^2 + \frac{2\beta}{N}\left(\frac{N-2b_M}{N}\right)^2 + \frac{a_M+\alpha}{N}\left(\frac{2b_M}{N}\right)^2\right] C_{TOT}{V_{DD}}^2 f. \tag{19}$$

$P_{SC\_A_P}$ and $P_{SC\_B_P}$ in regions II and III can be calculated by replacing a_M and b_M with a_P and b_P in equations (18)–(19). When $k \geq N/2$, after the vector distribution, the capacitors in the capacitor array are switched only with an amplitude of V_{DD}. Therefore, the P_{SC} can be calculated by replacing a and b with a_M (a_P) and b_M (b_P) in (12)–(14), respectively. The total P_{SC} is obtained from (16), and the ideal drain efficiency characteristics in the first quadrant and entire region are illustrated in Figure 3-15.

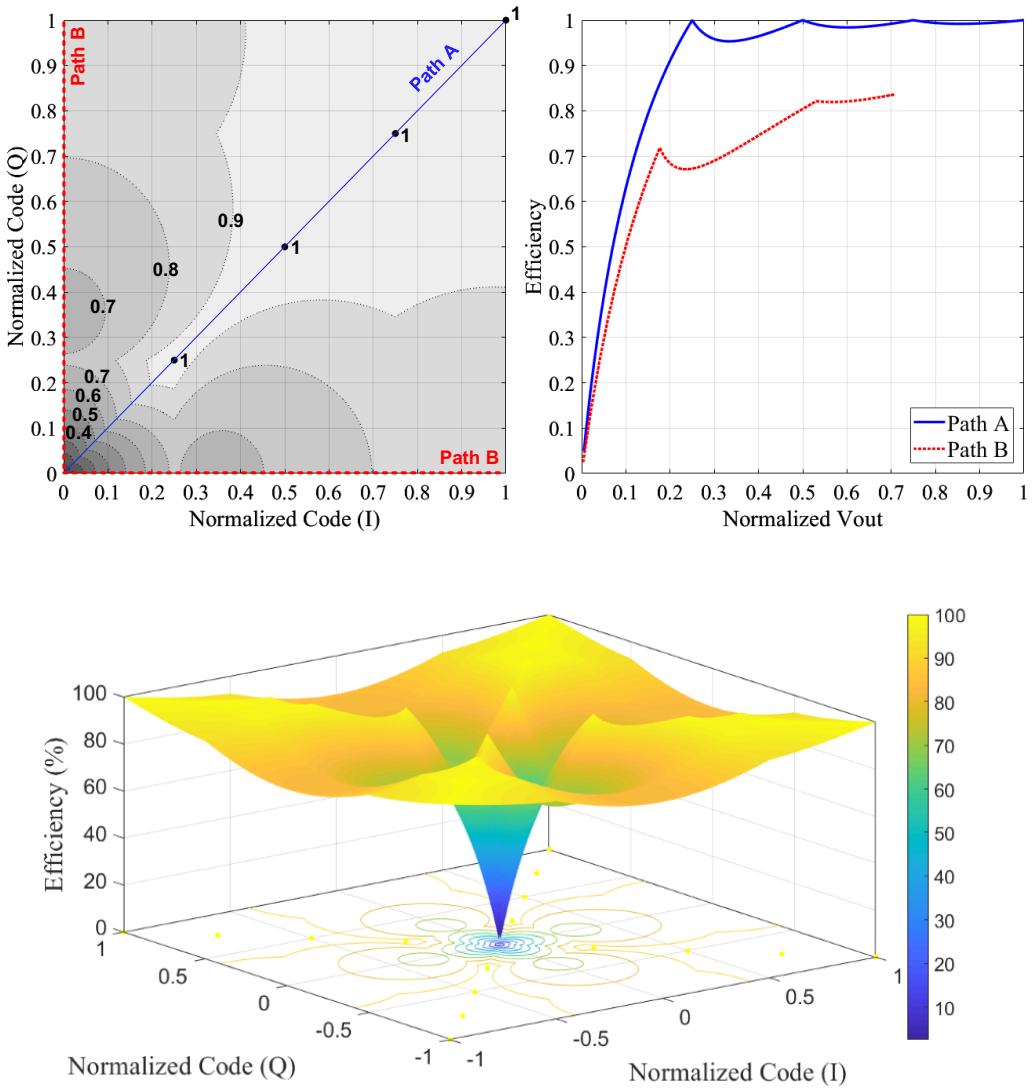


Figure 3-15 Theoretical Efficiency of the Quadrature Class-G CDD IQ-cell-shared SCPA: (a) 2-D Map in Quadrant I and (b) Entire 3-D Map.

3.4 Experiment Results

3.4.1 Prototype Implementation

3.4.1.1 Top Level Block Diagram

The proposed 12b quadrature Class-G CDD IQ-cell-shared SCPA, shown in Figure 3-16, converts an input digital I/Q data to an RF signal as a standalone quadrature transmitter without a phase modulator and a CORDIC. Each 11b quadrature IQ-cell-shared Class-G main and peaking SCPA is a complete quadrature digital transmitter with a dedicated decoder. The most significant

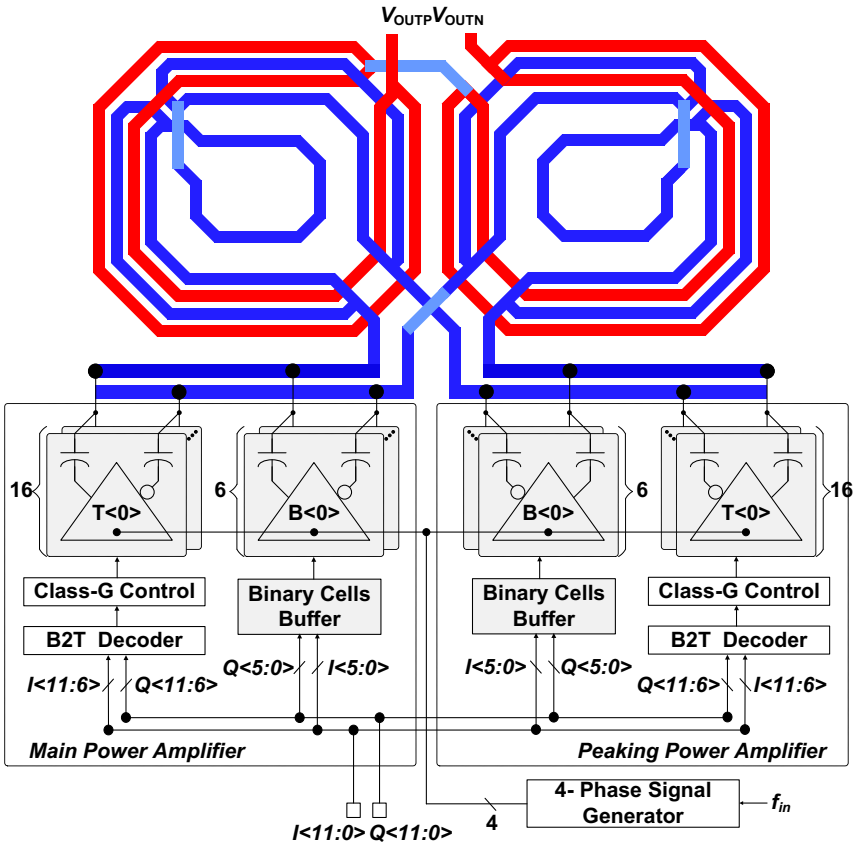


Figure 3-16 Block Diagram of the Quadrature Class-G CDD IQ-cell-shared SCPA.

bit of the I/Q data is assigned to the control of the main and peaking SCPAs, and the following 5 and 6 bits are allocated to the unary and binary cells of each SCPA, respectively.

The operation of the proposed quadrature Class-G CDD IQ-cell-shared SCPA is illustrated in Figure 3-17. The operating cells of each main and peaking SCPA are represented as triangles

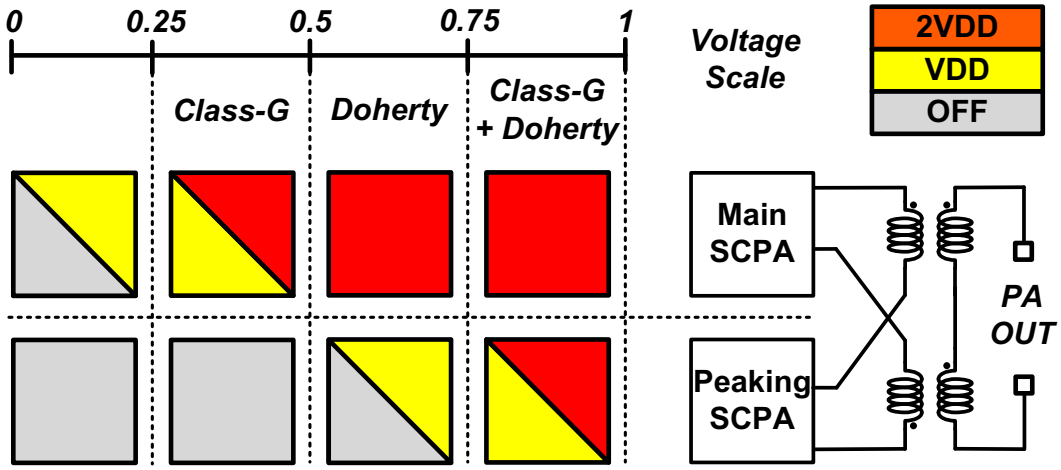


Figure 3-17 Quadrature Class-G CDD IQ-cell-shared SCPA Operation at 0-/2.5-/6-/12-dB PBO.

and rectangles, demonstrating the gradual increment of the output signal in proportion to the number of operating cells. For PBO lower than 6 dB, only the main SCPA operates, and the peaking SCPA is turned off. The peaking SCPA only operates after all the cells in the main SCPA are turned on for high P_{OUT} and enhanced efficiency through the Doherty operation for 0–6-dB PBO. For Class-G operation, each main and peaking SCPA can operate with both V_{DD} and V_{DD2} simultaneously because each SCPA cell connected to the switched-capacitor array inherently provides DC blocking function.

The main and peaking SCPAs are integrated with a power-combining XFMR. The XFMR is designed to cancel out the capacitance of the SCPA capacitor array at the resonance frequency while providing power combining and impedance conversion for high P_{OUT}. To enhance the efficiency at PBO for SCPA, the phase difference of voltage and current at output switches should be minimized. The amount of phase difference and efficiency at PBO is affected by the quality factor of the matching network and can be explained as follows: The loaded impedance, *Zin*, which can be modeled with the equivalent circuit as shown in Figure 3-10, varies with the number of switching unit capacitors in the SCPA. With the higher quality factor of the matching network, the smaller shunt capacitance keeps *Zin* less capacitive, provides less phase difference between the switching voltage and current and leads to an improved efficiency. The power consumption in the switched capacitor array can be minimized by employing smaller capacitance with a higher network quality factor. For the matching network in the prototype SCPA, the internal inductor structure within the XFMR is added to provide extra inductance and to reduce the capacitance in the capacitor array for a higher network quality factor and enhanced efficiency at PBO.

25% duty-cycle four-phase local oscillator (LO) signals are distributed globally and used to generate the 50% duty-cycle IQ-combined unit vectors in the quadrature SCPA [25]. In each

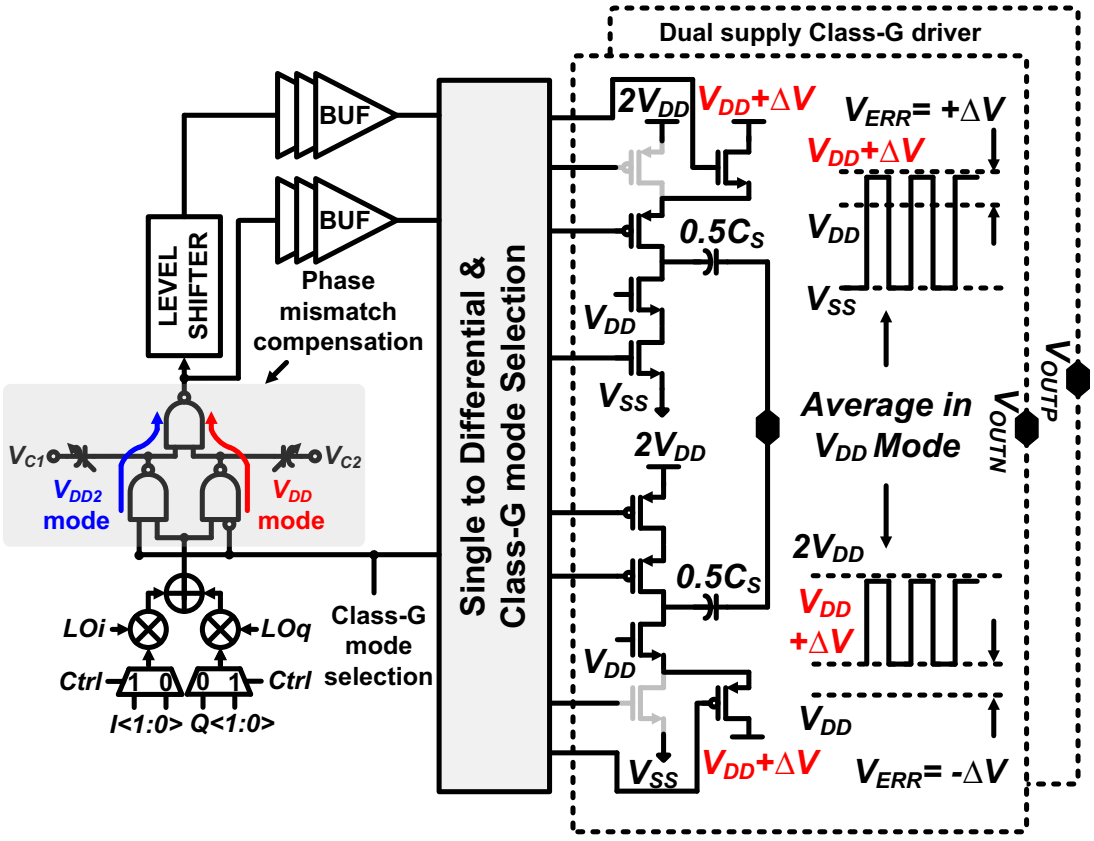


Figure 3-18 Dual-supply Class-G Switch with Supply Voltage and Phase Mismatch Compensation Scheme [26].

quadrature SCPA, there are 16 unary and 6 binary SCPA cells. For 5 unary bits, the 16 unary SCPA cells are integrated with dual-supply voltages. Each of the SCPA unary cells can process two input I/Q datasets for the dual-supply-voltage Class-G operation, as shown in Figure 3-18 [26]. The unary cells deliver the signal with an amplitude of V_{DD2} (V_{DD}) when two (one) input I/Q datasets are selected. Since there is only one I/Q mixer in the SCPA cell, if the two I/Q datasets for an SCPA unary cell are different, one of the I/Q datasets is transferred to an auxiliary (AUX) cell to conserve the amplitude and phase information [26].

3.4.1.2 Decoder Design

The peak SCPA is operated after all the cells in the main SCPA are turned on to guarantee the Doherty property. An example of a 6-bit IQ-cell shared CDD SCPA consists of 4-bit unary and 2-bit binary is shown in Figure 3-19. Since each main and peak SCPA is an IQ-cell shared SCPA,

the I and Q are combined in the digital domain to generate IQ-combined unit vectors. The IQ-combined unit vectors are represented by [i,q] where both i and q are ±1, and the mapping to the IQ data sets [I<n>, Q<n>] is shown in Fig. x. There are four SCPA unary cells, two binary cells, and one binary cell with auxiliary input (BAUX) in both SCPAs. Each of the SCPA unary cells can process two input IQ data sets for the Class-G operation and only has one IQ mixer. The unary cells deliver the signal with an amplitude of V_{DD2} (V_{DD}) when two (one) input IQ data sets are selected. Since there is only one IQ mixer in the SCPA cell, if the two IQ data sets to a SCPA unary cell are different, one of the IQ data is transferred to the cell with AUX input to conserve the amplitude and phase information.

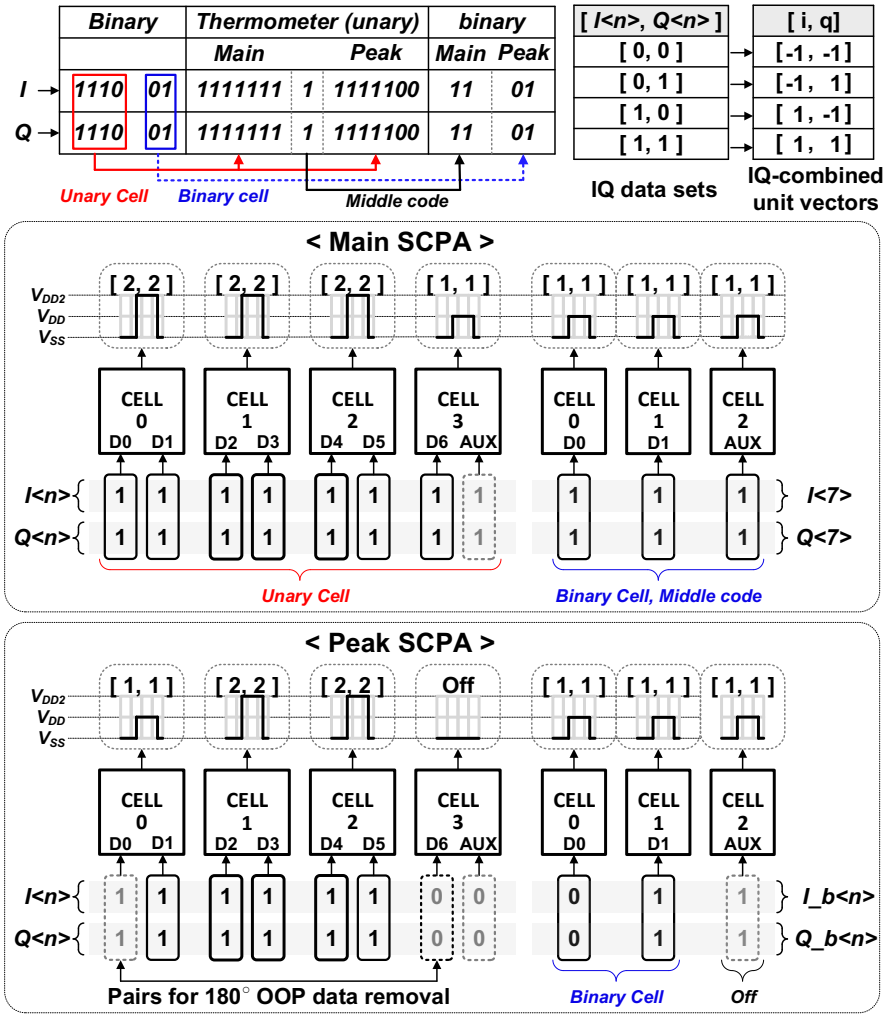


Figure 3-19 Decoder Design.

An example in Figure 3-19 shows the operation of the proposed CDD SCPA between 0-6dB PBO. Below 6dB PBO, only the main PA is turned on, and the transmitter operates as a single IQ-cell shared Class-G SCPA. The input four bits for each unary of I and Q are decoded into 15-bit thermometer codes of *I/Q*<14:0>, and the main and peak SCPAs operate with the I/Q<6:0> and I/Q<14:8>, respectively. Since all unary cells in the main SCPA have two or one identical IQ data sets, all cells are turned on and deliver the signal with [1, 1] IQ data set. In the peak SCPA, one unary cell is turned off because of the 180° OOP IQ data sets, [1, 1] and [0, 0]. The example shows the 180° OOP IQ data removal operation applies in the peak SCPA first until all the cells are turned off while keeping all the cells in the main SCPA are turned on to conserve the Doherty property. Since the 15-bit of the thermometer codes cannot be divided equally to the main and peak SCPAs, the 8th pair of the thermometer code, *I/Q*<7> is implemented as follows: The binary and BAUX cells deliver the signal with an amplitude of V_{DD}. With the same IQ data set, the output vector summation is equal to the unary cell with an amplitude of V_{DD}. Therefore, the 8th pair of the thermometer code, *I/Q*<7>, can be implemented by assigning the *I/Q*<7> to the binary and BAUX cells. Below 6dB PBO, only the main PA is turned on, and the binary bits are assigned to the binary cells in the main SCPA. For 0-6dB PBO, as in Figure 3-19, *I/Q*<7> are assigned to the binary and BAUX cells in the main SCPA. Since all the cells are turned on in the main SCPA, the binary bits are assigned to the binary cells in the peak SCPA.

3.4.1.3 Linearization Techniques

For excellent linearity, each SCPA incorporates inherently linear Class-G techniques to generate an amplitude of $V_{DD2}/2$ instead of V_{DD} for the V_{DD} (low-power) mode through the mixed usage of V_{DD2} and V_{DD}. The dual-supply Class-G switch with such linearization technique is shown in Figure 3-18 [26]. Any voltage mismatch in V_{DD2} and V_{DD} is canceled out by splitting switch cells

and summing outputs at the capacitor array. This significantly reduces the mismatch between V_{DD} and V_{DD2} for Class-G operation while maximizing efficiency by employing multiple supply voltages for multiple efficiency peaks. Class-G operation with two different supply voltages can also result in phase mismatch due to the different signal paths between the V_{DD2} and V_{DD} modes. A phase mismatch compensation technique is implemented in the signal path to align the phases in two different signal paths with two different supply-voltage domains, as shown in Figure 3-18 [26].

3.4.1.4 Die Micrograph

The prototype quadrature Class-G CDD DPA is fabricated in a 65-nm CMOS process, and it occupies 1.07×0.845 mm^2, as shown in Figure 3-20. It comprises main and peaking SCPAs, an LVDS receiver, a four-phase LO signal generator, a power-combining XFMR, and bonding pads. The chip is mounted and wirebonded to PCB for measurement.

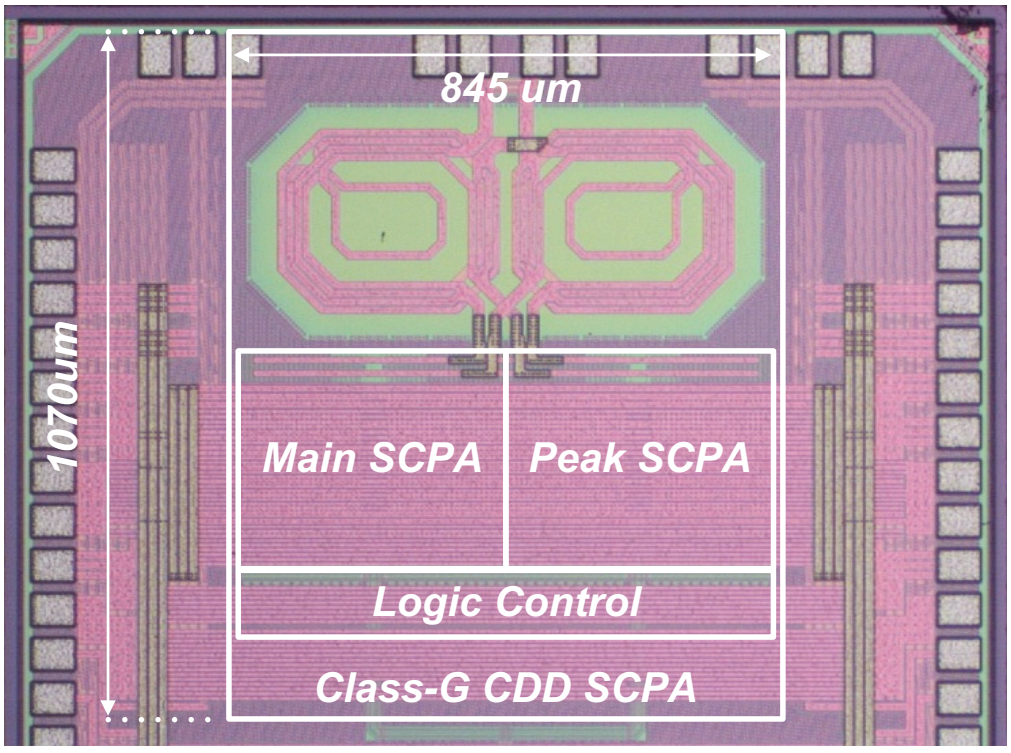


Figure 3-20 Die Micrograph.

3.4.2 Measurement and Simulation Results

3.4.2.1 Digital Predistortion Algorithm

Most DPD techniques as shown in Figure 3-21 can generally be classified into two categories: memoryless or memory DPD. In memoryless DPD, the output sample is only a nonlinear function of the current input sample. The memoryless DPD can be easily implemented with lower hardware complexity, however, its performance often degrades as signal bandwidth increases. While the signal bandwidth increases, the output sample is not only the nonlinear function of the current input sample but also relates to some finite number of previous samples. Therefore, the memory DPD has been introduced to improve performance over memoryless DPD for wideband signals with the penalty of added computational complexity. The Memoryless DPD was used for the measurement of the CDD DPA.

Before generating the memoryless DPD, the phase mismatch between the binary and unary cells and between two different signal paths with two different supply-voltage domains should be adjusted first. Same I and Q digital control word (DCW) has been applied to CDD DPA. Ideally, the constellation should be aligned along the 45° angle. However, due to the phase mismatch, the

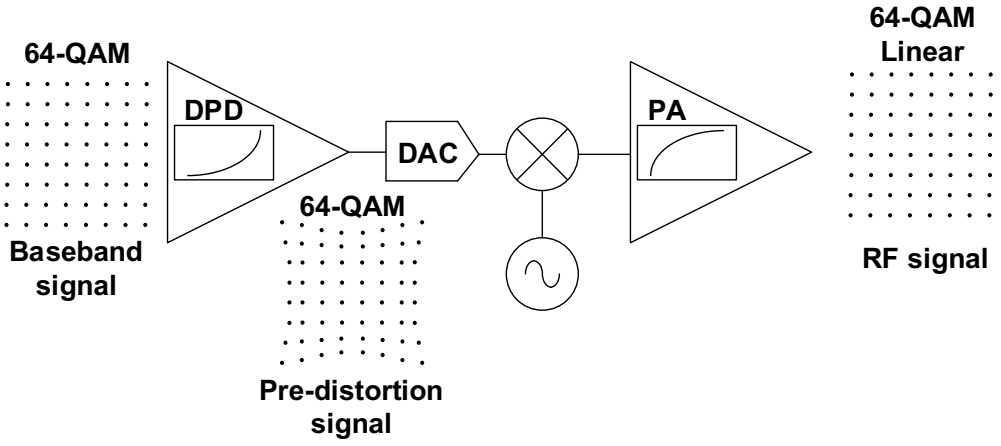


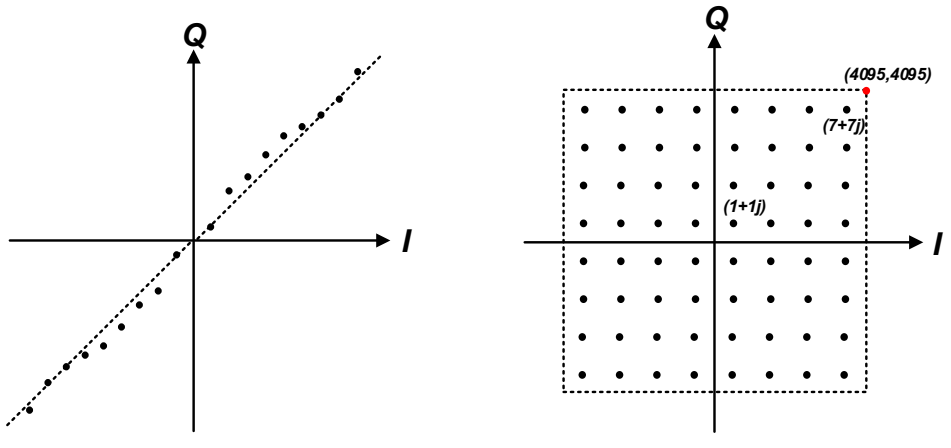
Figure 3-21 Digital Predistortion Techniques.

observed constellation could be offset from the 45° angle as shown in Figure 3-22 (a). The varactor control calibration on chip has been used to adjust the phase mismatch manually.

After adjusting the phase mismatch, the static nonlinearity of the CDD DPA has been measured. The permissible values of the 12b I and Q DCW are used to generate a set of uniformly spaced 32 × 32 points to represent 1024-QAM constellation without DPD. The point corresponding to DCW (+4095, +4095), which represents the peak output power in the first quadrant is used as the reference to generate the ideal 1024-QAM constellation. Figure 3-22 (b) shows an example of a 64-QAM constellation with the DCW (+4095, +4095) as reference.

An example shown in Figure 3-23 (a) demonstrates the measured static nonlinearity of the CDD DPA. The 1024-QAM is measured instead of 64-QAM in the real measurement. Four adjacent points in the constellation are grouped together as shown in Figure 3-23 (b) to calculate the interpolation function. If the I and Q input set, (I_{in}, Q_{in}) is closer to the constellation set of (A_1, A_2), the predistorted I input can be determined as follow:

$$I_{DPD} = I_{in} + \Delta X_1 + \frac{\Delta X_2 - \Delta X_1}{A_{2\_X} - A_{1\_X}} * (I_{in} - A_{1\_X}) \tag{20}$$



(a) (b)

Figure 3-22 An Example of Uniformly Spaced 8 × 8 Points to Represent 64-QAM Constellation without DPD.

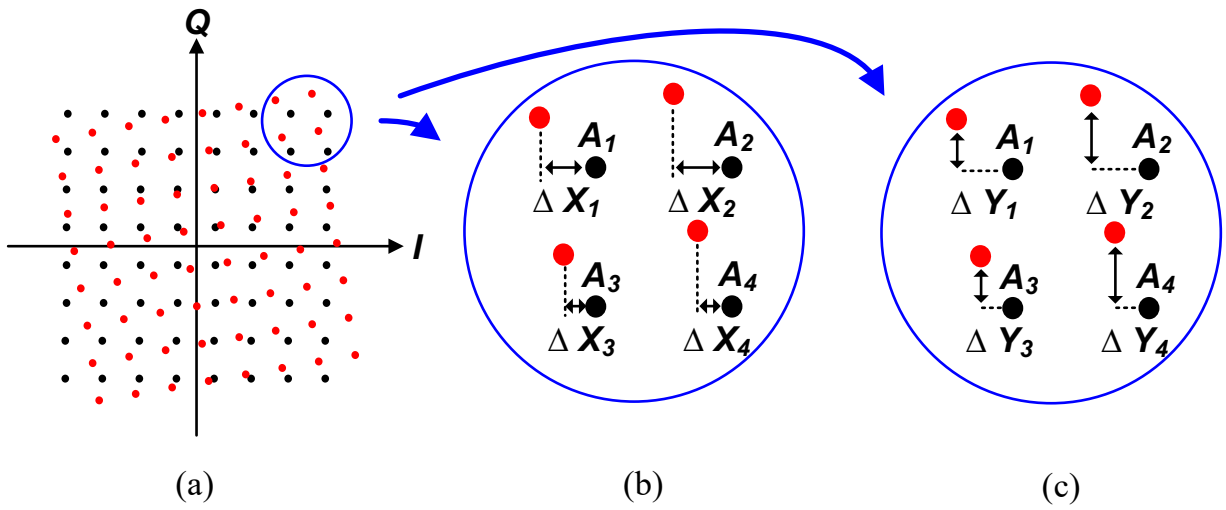


Figure 3-23 (a) Static Nonlinearity of the CDD DPA. (b) Four Adjacent Points in the Constellation Are Grouped Together to Calculate the Interpolation Function.

Linear interpolation is used instead of cubic interpolation since there is no significant difference in performance improvement between linear and cubic interpolation for large LUT numbers [42]. On the other hand, if (I_{in}, Q_{in}) is closer to the constellation set of (A_3, A_4), the same equations can be used to determine the predistorted I input by replacing ΔX_1 and ΔX_2 with ΔX_3 and ΔX_4. The same calculation methods as shown in Figure 3-23 (c) can be used to determine the predistorted Q input as follow:

$$Q_{DPD} = Q_{in} + \Delta Y_1 + \frac{\Delta Y_2 - \Delta Y_1}{A_{2\_Y} - A_{1\_Y}} * (Q_{in} - A_{1\_Y}) \tag{21}$$

The complete measurement setup is shown in **Error! Reference source not found.**. The I and Q DCW are provided through the back-panel of the AWG, which can provide up to 13b of digital inputs of both I and Q. The 1024-QAM constellation has been captured through the PathWave vector signal analysis of Keysight (89600 VSA). The measured constellation has been used to generate the predistorted look-up table (LUT) from (20)–(21) through Matlab. Then, the predistorted single-carrier 1024-QAM and 1024-QAM OFDM signals are applied to the CDD

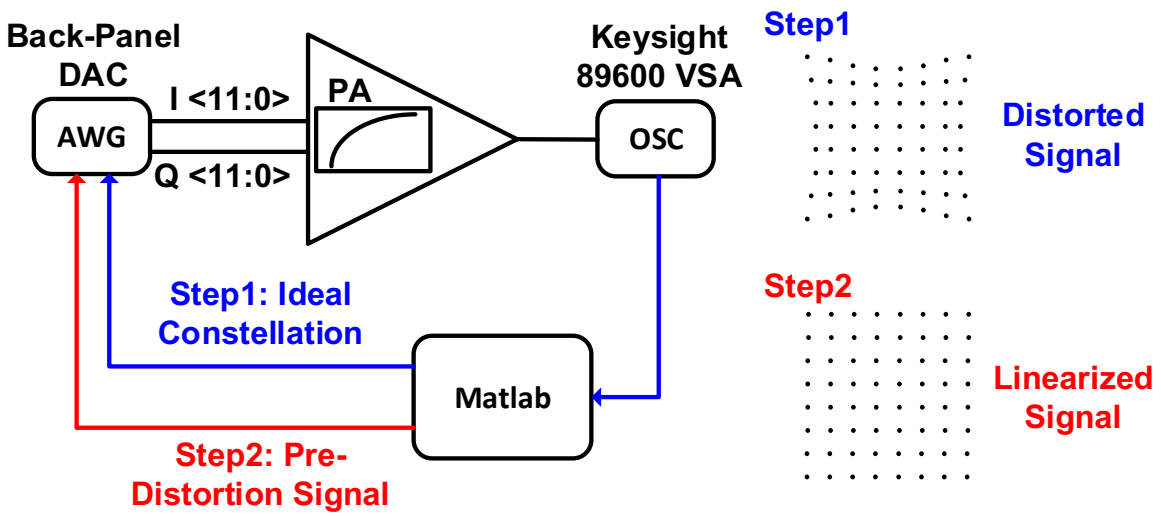


Figure 3-24 Measurement Setup of CDD DPA.

DPA to improve the measured error vector magnitude (EVM). All the measurements of the CDD DPA have been automated through the standard commands for programmable instruments (SCPI).

The static nonlinearity of the CDD DPA may vary with different operating conditions and PBO region. Therefore, the LUTs must be periodically updated to maintain a good EVM performance. Compared to the cubic interpolation, the computational complexity is significantly reduced with linear interpolation. The EVM improves with the increasing size of LUT. However, the EVM improvement is negligible for the LUT size beyond 32 × 32. At different PBO region, the static nonlinearity of the CDD DPA can be remeasured to generate updated LUT to improve the EVM performance with the penalty of computational complexity. The measured data with the implemented DPD algorithm has been shown in the following section.

3.4.2.2 Measurement with Digital Predistortion Algorithm

The measured EVM versus P_{OUT} for a 40-MHz (20-MHz) single-carrier 1024-QAM signal with a 6.8-dB PAPR at 2.2 GHz with and without DPD are shown in Figure 3-25. A 32×32-point two-dimensional LUT (2D-LUT) based DPD is adopted with linear interpolation for the least significant bits (LSBs). After DPD, for a 40-MHz (20-MHz) single-carrier 1024-QAM signal, the

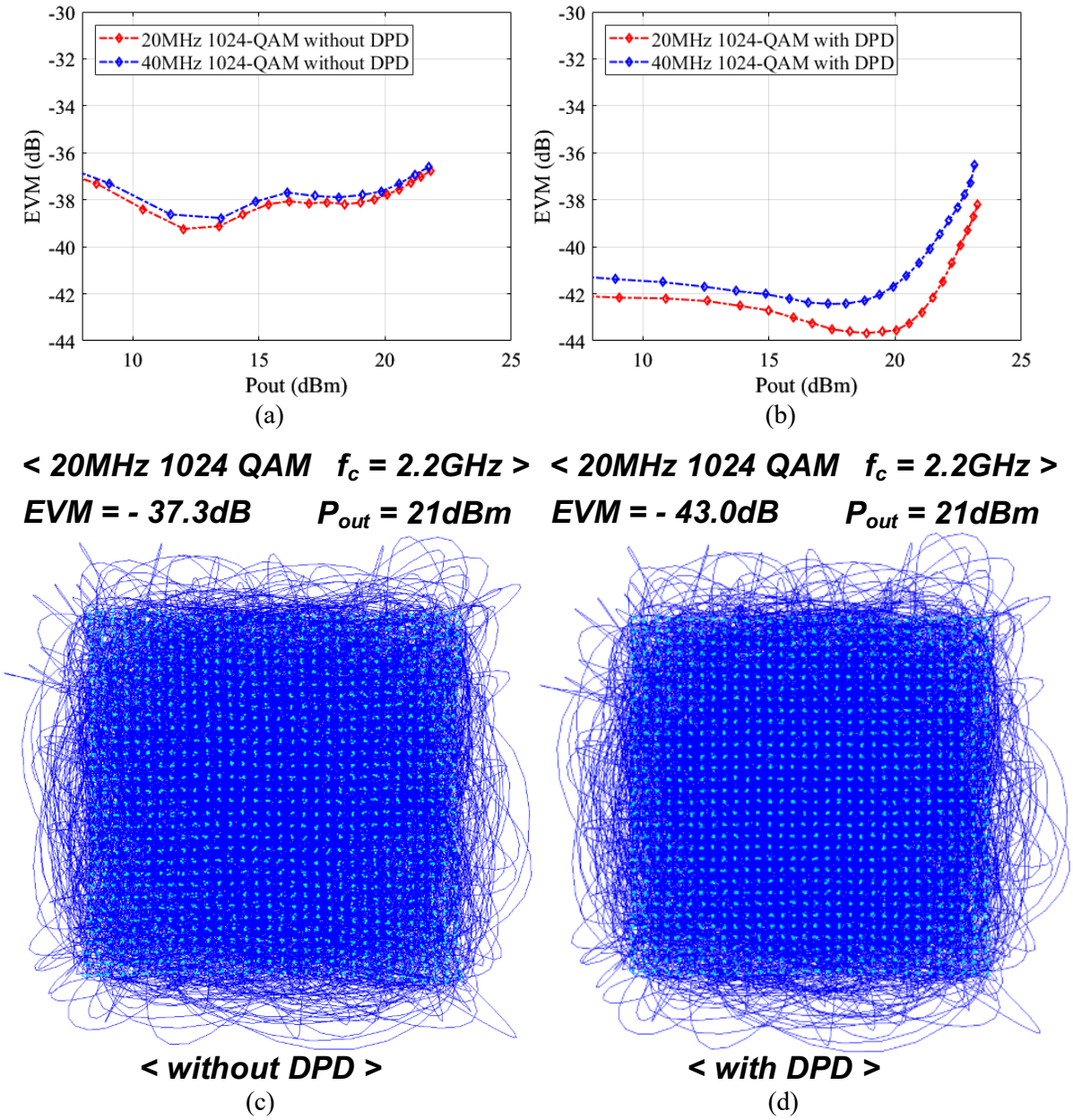


Figure 3-25 EVM vs. P_{OUT} for A 40-MHz (20-MHz) Single-carrier 1024-QAM Signal with 6.8-dB PAPR at 2.2GHz (a) without and (b) with DPD. Constellation for A 20-MHz Single-carrier 1024-QAM Signal at A P_{OUT} of 21-dBm (c) without and (d) with DPD.

measured EVM is -40.7 dB (-43.0 dB) at 21-dBm P_{OUT} [Figure 3-25 (b)], and the EVM floor is -42.4 dB (-43.6 dB) at a P_{OUT} of 17.3 dBm (18.8 dBm). The quadrature Class-G CDD DPA demonstrates 18.4% SE for a 20-MHz single-carrier 1024-QAM signal at 2.2 GHz at 21-dBm P_{OUT}. The measured constellations without and with DPD are depicted in Figure 3-25 (c) and (d), respectively. The EVM versus P_{OUT} for an IEEE 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM

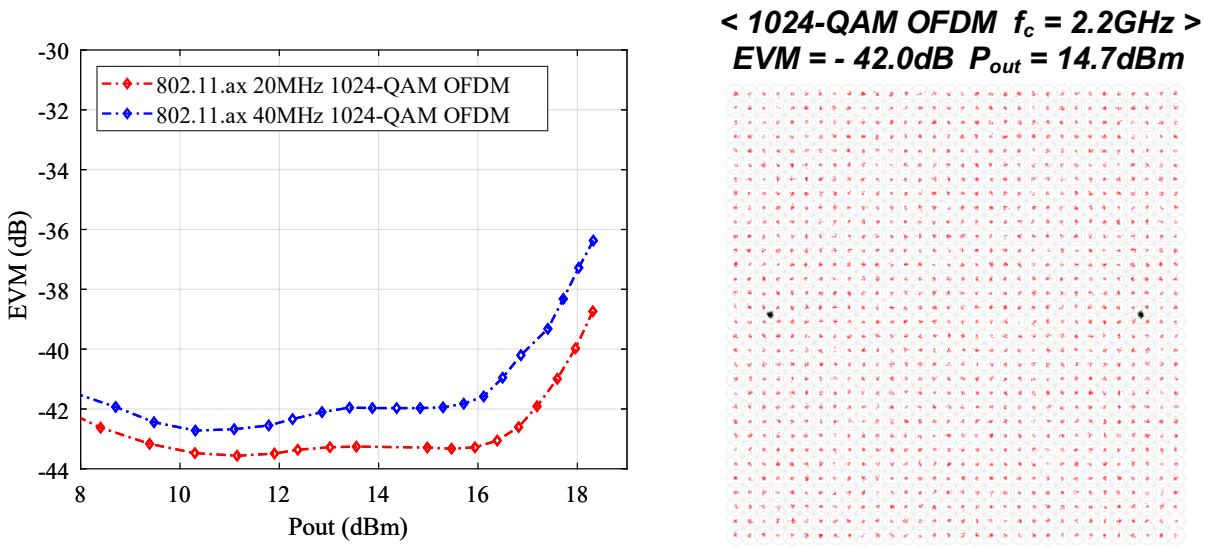


Figure 3-26 (a) EVM vs. P_{OUT} and (b) Constellation for An IEEE 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM Signal with A 13.1-dB (12.4-dB) PAPR at 2.2GHz with DPD.

signal with a 13.1-dB (12.4-dB) PAPR at 2.2 GHz with DPD is shown in Figure 3-27(a). The prototype achieves an EVM of better than -40 dB over a more-than-10-dB (12-dB) P_{OUT} range with DPD. The measured EVM is -42.0 dB (-43.3 dB) at 14.7-dBm (15.4-dBm) P_{OUT} [Figure 3-27 (a)], and the measured constellation with DPD at 14.7-dBm P_{OUT} is shown in Figure 3-27 (b). Figure 3-26 depicts the spectrum for an IEEE 802.11ax 40-MHz (20-MHz) signal with and without DPD.

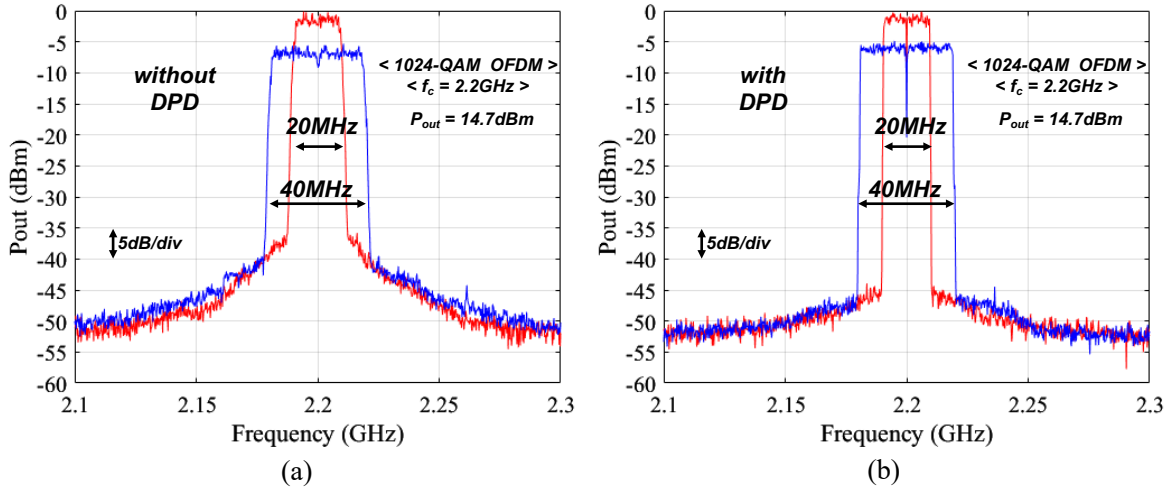


Figure 3-27 Spectrum for An IEEE 802.11ax 40-MHz (20-MHz) 1024-QAM OFDM Signal with a 13.1-dB (12.4-dB) PAPR (a) without and (b) with DPD.

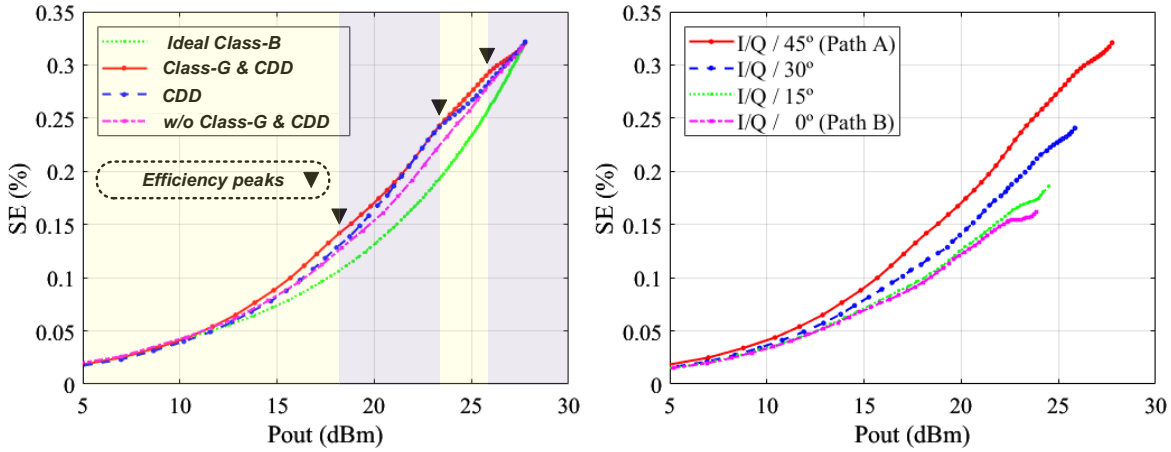


Figure 3-28 SE vs. P_{OUT} Measured with A 2.2-GHz CW Signal (a) for Different Operating Modes at 45° and (b) for the Class-G CDD Mode at Different Angles.

Figure 3-28 shows SE versus P_{OUT} measured with a 2.2-GHz continuous-wave (CW) signal for different operating modes at 45° and for the Class-G CDD mode at different angles. The measured SE of the quadrature Class-G CDD DPA reflects the total power consumption for the conversion of baseband I/Q bits to high-power RF signals. The peak SE of the proposed quadrature Class-G CDD DPA is 32.1% at 27.8-dBm P_{OUT}. The SE measured with Doherty and Class-G operations is compared with other SCPA operation modes without Doherty and/or Class-G and clearly exhibits efficiency enhancement with three additional efficiency peaks at PBO.

The simulated power consumption breakdown of the proposed quadrature Class-G CDD DPA is shown for 0, 6, and 12-dB PBOs in Figure 3-29. The breakdown includes the power consumption for dual-supply Class-G switches, logic gates and buffers to drive the switches, and a four-phase LO signal generator. At peak output power, power consumption is dominated by the dual-supply Class-G switches, while it is occupied by the logic gates and buffers at deep PBO in a 65-nm CMOS process. Therefore, the efficiency at PBO can be significantly enhanced in an advanced CMOS process with more dominant efficiency peaks because the switching performance can be drastically improved and the power consumption in digital circuits can be significantly reduced.

3.5 Conclusion

A quadrature Class-G CDD DPA is introduced, and a detailed theoretical analysis is provided. The proposed CDD technique achieves load modulation with high efficiency and phase modulation through Doherty operation in the complex domain. A prototype of 12b CDD DPA based on quadrature main and peaking Class-G SCPAs is implemented in a 65-nm CMOS process. The prototype demonstrates high efficiency at PBO with three additional efficiency peaks associated with the Class-G and CDD techniques. It also achieves excellent EVM of <-40 dB over >10 dB P_{OUT} for an IEEE 802.11ax 40-MHz signal. A comparison with the state of the art is shown in **Error! Reference source not found.**.

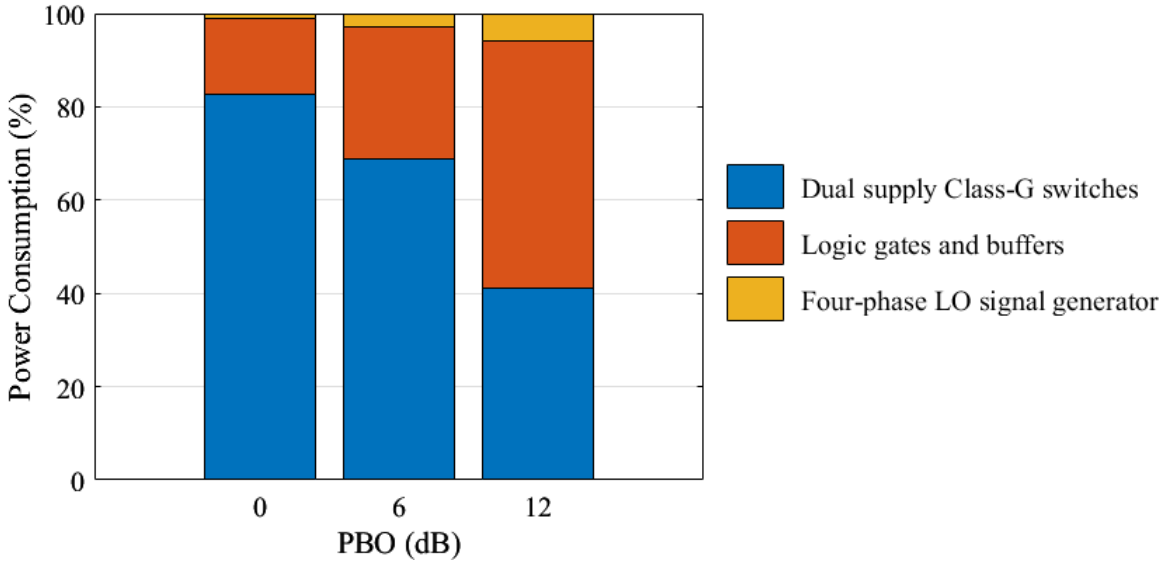


Figure 3-29 Simulated Power Consumption Breakdown of the Proposed Quadrature Class-G CDD DPA.

Table 3-1 Performance Comparison with the State of the Art

Reference	JSSC 2017 [24] V. Vorapipat	RFIC 2018 [25] S. W. Yoo	JSSC 2016 [39] W. Yuan	JSSC 2017 [40] H. D. Jin	This work		
Architecture (SCPA)	Polar Class-G VMD	Quadrature Class-G IQ-cell-shared	Quadrature Class-G	Quadrature IQ-cell-shared	Quadrature Class-G CDD		
Process (nm)	45	65	65	28	65		
Supply (V)	2.4/1.2	2.5/1.2	2.4/1.2	1.1	2.55/1.25		
Resolution	9 (5+4)	11 (6+5)	7 (5+2)	6 (5+1)	12 (1+5+6)		
Freq. (GHz)	3.5	2.2	2.0	0.8	2.2		
Peak Power (dBm)	25.3	30.1	20.5	13.9	27.8		
Peak SE (%)	30.4	37.0	20.0	40.4	32.1		
Modulation	10MHz 32 Carrier 1024-QAM	20MHz Single-Carrier 256-QAM	10MHz LTE 64-QAM	10MHz LTE 16-QAM	20MHz Single-Carrier 1024-QAM	20MHz 802.11ax OFDM 1024-QAM	40MHz 802.11ax OFDM 1024-QAM
Output Power (dBm)	14.8	22.5	14.5	6.97	21.0	15.4	14.7
PAPR (dB)	10.5	7.6	6.0†	6.9	6.8	12.4	13.1
Avg. SE (%)	18.0‡	18.3	12.2	29.1	18.4	9.3	7.9
EVM (DPD, dB)	-40.3	-40.3	-28.9	-26.0*	-43.0	-43.3	-42.0

‡ Power consumption of PA only excluding CORDIC and phase modulator.
† Estimated from the peak/output power.
* Measured without DPD.

4 An 18–50-GHz Transmitter Front-End for a Digital Phased Array System

Phased array technology has steadily evolved since it was first invented in the early 1900s. Compared to the early antenna arrays with mechanical rotation to steer the beams, the development of electronic steering in phased arrays enables more rapid and versatile scanning. Therefore, since the 1970s, phased array technology has been extensively used in RF applications [42][44], such as radar and communication systems.

Phased arrays can be categorized into three categories: passive, active, and digital. In passive and active phased arrays, beamforming is performed by digitally controlled analog phase shifters or time delay. Digital phased arrays [45][46], shown in Fig. 1, have a transceiver employed in each element at the sub-array or element level, and beam steering is performed using digital summations across the arrays. The digital phased arrays offer several significant advantages over passive and

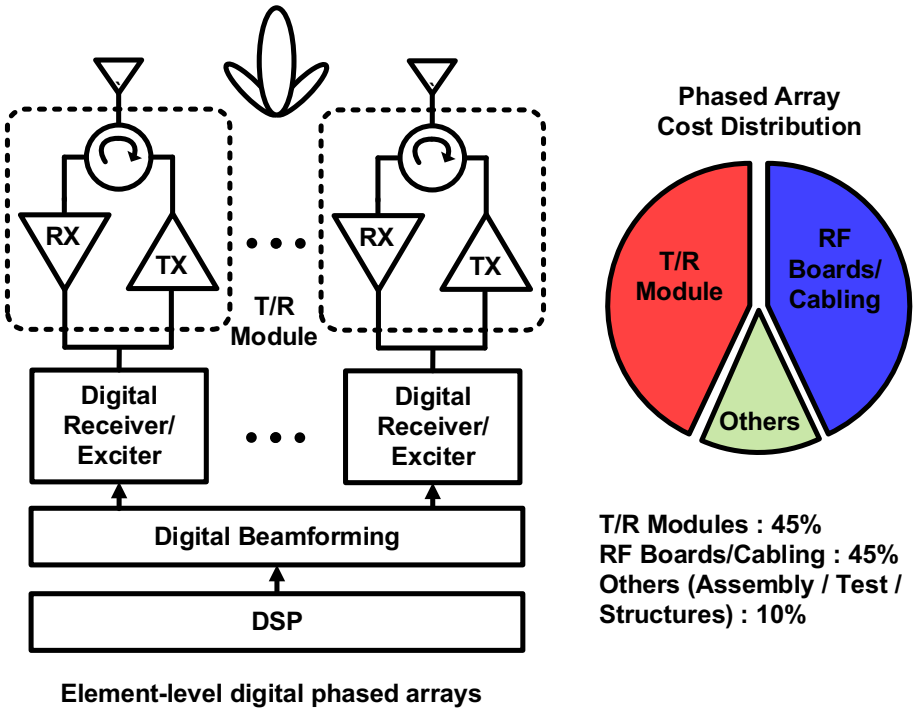


Figure 4-1 Element-level Digital Phased Arrays and the Cost Distribution of the Phased Arrays [47].

active phased arrays: wideband signal reception and transmission, flexible and precise beamforming and nulling, and multiple simultaneous beams with low sidelobes over the full scan volume. However, each element requires data converters and front-end transmit and receive (T/R) modules, which increase the hardware complexity, cost, and power consumption of the total phased array system. Due to the high implementation cost, the application of phased arrays has primarily been focused on military applications. The advanced manufacturing of silicon RF integrated circuits (RFICs) paves the way to significantly reduced implementation costs and extensive use of phased arrays. The T/R module cost, which drives half of the phased array cost [47] as shown in Figure 4-1, has been reduced drastically by leveraging volume production pricing of the advanced manufacturing technology. Moreover, multiple elements of large arrays can be integrated into a single sub-array chip, and the complexity and cost of the digital controls can be significantly reduced in advanced CMOS processes.

The physical size of the system in integrated phased arrays is dominated by the size of the antennas and the spacing between the antennas. Compact integration of antennas with the T/R module has become feasible in mm-wave communication as the antenna size and pitch decreased with an increase in frequency. In this work, the proposed mm-wave transmitter offers wide-frequency range operation, low power consumption, a small area, and supports emerging multibeam communications and directional sensing with an increased number of phased array elements from 18–50 GHz. The prototype covers the Q/Ka/K bands for most commercial and military applications.

4.1 System Specifications

Table 4-1 Specifications of Required 18-50 GHz Transmitter

Metrics	Specifications
Frequency Range	18 – 50 GHz
Transmitter 1-dB Compression point	-3.5 dB
Transmitter Baseband Input Power	-20 dBm
Transmitter DAC Interface Impedance (Differential)	1000 ohm
Transmitter Output Third Order Intercept Point	8 dBm
Baseband Filter Passband	DC-100 MHz
Baseband Filter Passband Ripple	1.5 dB
Baseband Filter Stopband Attenuation	-60dBc @ 700 MHz
Max DC Power Consumption	72 mW
Max Chip Area	550 x 850 um^2
LO/RF Input Impedance	100 ohm
LO Input Power (Differential)	0 dBm

This project is part of DARPA mm-wave Digital Arrays (MIDAS) program [48] and the required specifications of the desired receiver are given in Table 4-1.

4.2 System Design

A block diagram of the proposed transmitter is shown in Figure 4-2. In-phase (I) and quadrature (Q) signals generated from two DACs are amplified and filtered by the Sallen–Key filters with tunable gain and frequency response. The cascaded Sallen–Key filters provide higher-order rejection for the aliasing tones from the DACs and moderate gain to mitigate the gain required for the following mixer and stacked common gate (CG) driving amplifier (DA) stages. Voltage-to-

current (V2I) converters with the current mirror topology followed by the active mixer provide tunable gain controls and better linearity. The stacked mixer is composed of CG DA and two double balanced active mixers, whose currents are summed directly at the output. The stacked double balanced active mixer provides wide frequency operation, improved linearity, reduced chip size, and robust device reliability. The voltage swing across the mixer and the stacked CG DA is carefully designed to avoid reliability issues. The LO driver followed by the coupled line coupler is designed to generate the in-phase and quadrature LO signals from a single LO signal with excellent amplitude and phase balance over a broad frequency range of 18–50 GHz.

4.3 Differential Quadrature Coupler

For a small power consumption of the LO distribution in a phased array system, a single-phase LO signal is distributed instead of in-phase and quadrature LO signals in a conventional transmitter as shown in Figure 4-5.

There are two main categories for a quadrature LO generator: quadrature generators based on transmission lines and lump components.

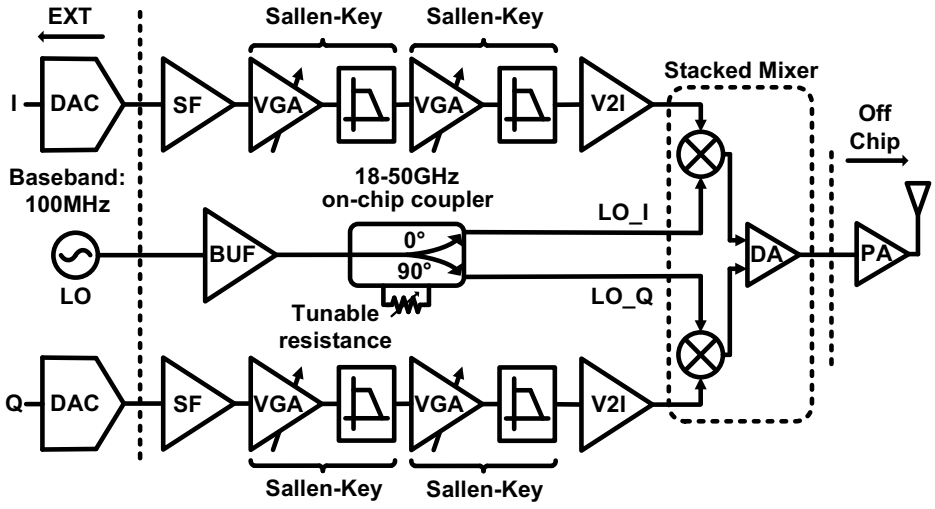


Figure 4-2 Block Diagram of the Proposed 18–50-GHz Transmitter.

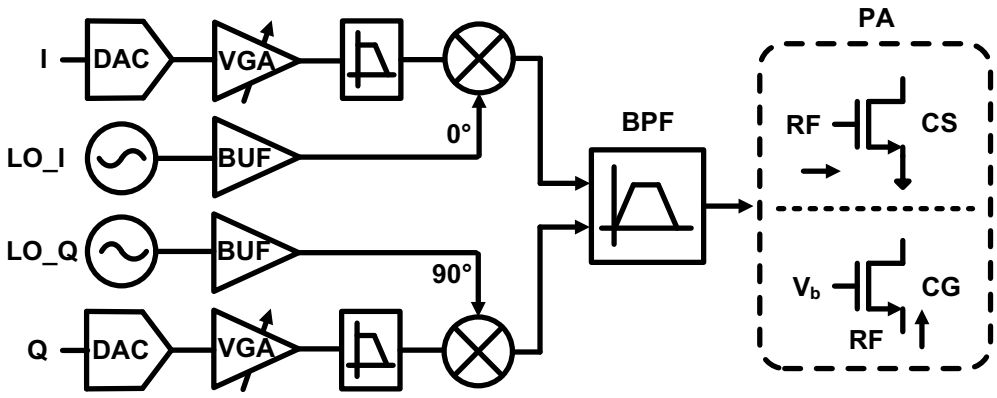


Figure 4-3 Block Diagram of the Conventional Transmitter Architecture.

4.3.1 Quadrature Generators Based on Lump Components

Basic circuit elements such as resistors, capacitors, and inductors can realize the quadrature generators. These basic circuit elements, which lead to compact and inexpensive quadrature generator designs, can be easily implemented in advanced CMOS processes. However, the designs with lumped components have large losses and significant central frequency shifts due to the PVT variation. There are two main topologies for quadrature generators based on lump components, poly-phase filter (PPF) and quadrature all-pass filter (QAF). Both PPF and QAF use a combination of the low-pass filter (LPF) and high-pass filter (HPF) to generate adequate phase shift between the output signals.

Figure 4-4 shows an example of simplified first order PPF. The transfer function of LPF and HPF can be expressed as follows:

$$H_{LPF}(j\omega) = \frac{1}{1+j\omega RC} \tag{1}$$

$$H_{HPF}(j\omega) = \frac{j\omega RC}{1+j\omega RC} \tag{2}$$

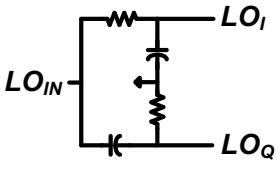


Figure 4-4 Simplified First Order PPF.

The phase can be approximated as follows:

$$\theta_{LPF}(j\omega) = -\tan^{-1}(\omega RC) \tag{3}$$

$$\theta_{LPF}(j\omega) = \frac{\pi}{2} - \tan^{-1}(\omega RC) \tag{4}$$

If the resistance and capacitance values are chosen as $RC = \frac{1}{\omega}$, ω is the desired radial frequency of the input signal, the phase difference between the LPF and HPF is equal to 90°. The attenuation is equal in both paths. Due to the wide phase variation over PVT, more robust designs can be achieved with higher order PPF.

4.3.2 Quadrature Generators Based on Transmission Lines

For a quadrature LO generator based on two quarter-wave coupled transmission lines, the chip area is the main limitation at lower frequencies. For mm-wave communication applications, a compact quarter-wave coupled line coupler structure can be achieved with excellent phase and amplitude imbalance for quadrature signals generation. The coupling effect can be achieved by edge-side or broadside coupling. The simplified single-ended operations for edge-side and broadside coupling are illustrated in Figure 4-5(a) and Figure 4-5(b), respectively.

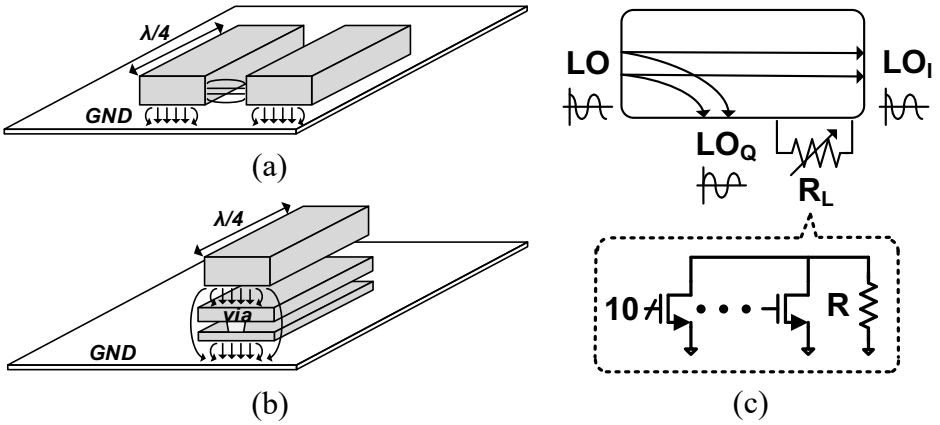


Figure 4-5 Coupled Line Coupler: (a) Edge and (b) Broadside Coupler Based on Two Quarter-wave Coupled Transmission Lines. (c) Coupler with Tunable Resistance.

4.3.2.1 Edge-side Coupling

Edge-side coupling can be simply designed as shown in Figure 4-5(a). However, the different modal velocities of even- and odd-modes lead to poor isolation, which worsens the directivity of the coupler. By placing the capacitors between the input and output ports, the performance of the edge-side coupler can be improved, but still suffers from reliability issues due to the PVT variation.

4.3.2.2 Broadside Coupling

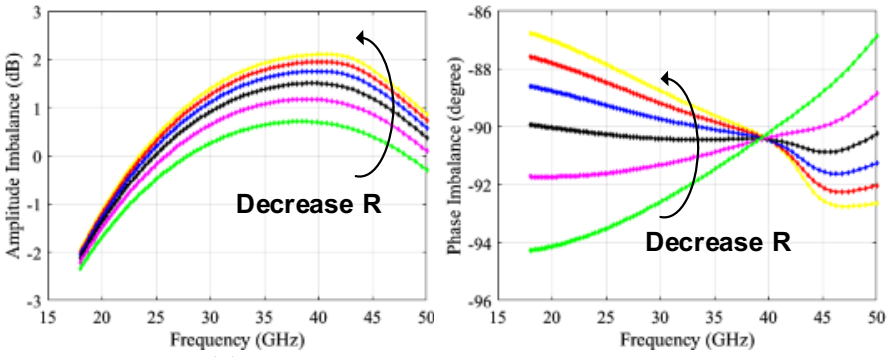
The coupling ratio between two broadside coupled metal layers shown in Fig be obtained as follows:

$$k = \frac{Z_{0e} - Z_{0o}}{Z_{0e} + Z_{0o}} \tag{5}$$

The Z_{0e} and Z_{0o} are even- and odd-modes impedances of the coupled lines. The chip area can be saved by its vertical stacks between coupled lines. The width of the two coupled transmission lines can be chosen differently to mitigate the difference of the distributed capacitance from the two coupled lines to the ground.

4.3.3 Coupler Implementation and Simulation Results

A differential broadside coupler is implemented to generate differential LO signals locally and save the chip area with its vertical stacks between coupled lines. By over-coupling the broadside coupler, a wideband response can be achieved by selecting the specific metal layers in a process. The UA and C2 metal layers are selected in the GlobalFoundries 45-nm SOI CMOS process. By stacking all the lower metal layers, the loss due to the thickness of the C2 metal layer can be reduced. Figure 4-6 presents the simulated frequency response of the 18–50-GHz broadside coupler, which is folded to fit the chip area requirement. The phase imbalance can be tuned for a



(a) (b)

Figure 4-6 Simulated (a) Amplitude and (b) Phase Imbalance of the 18–50-GHz Broadside Coupler with Tunable Resistances.

specific frequency with tunable resistance at the isolation port as shown in Figure 4-5(c), which also provides robustness against process variation.

4.4 LO Driver

A square wave is desired for the LO waveform to ensure abrupt switching and hence maximum conversion gain. However, at mm-wave frequencies, the LO signal is usually a sinusoidal waveform. As the sinusoids change gradually, the ON- and OFF-switching of the mixer transistors take time, resulting in reduced conversion gain at mm-wave frequencies. With low LO amplitude, the mixer transistors are all ON, which produces no differential component at the output. Therefore, high LO amplitude is required to minimize the ON- and OFF-switching time, resulting in improved conversion gain and isolation. The LO driver is implemented between the LO input and the mixer to increase the LO signal and provides the input matching at the same time.

4.4.1 Common-Source with Resistive Input Matching

One straightforward approach to provide input matching is using parallel resistance at the input port of a common source (CS) amplifier as shown in Figure 4-7. The simplest architecture reduces the complexity of the LO driver with the drawbacks of an attenuated input signal ahead of the transistor M_1 and higher noise figure.

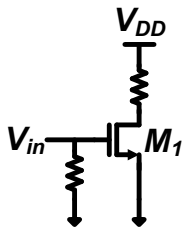


Figure 4-7 Common Source Amplifier with Resistive Input Matching.

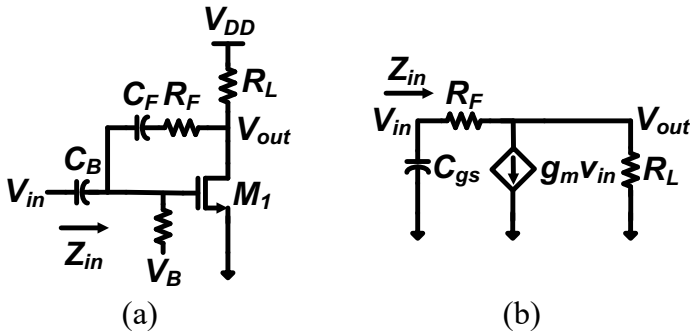
4.4.2 Common-Source with Resistive-Feedback Input Matching

The simplified resistive-feedback amplifier is shown in Figure 4-8(a). M_1 represents the transconductance device, which can be implemented with a single or cascode transistors. The shunt-shunt feedback is realized by the R_F resistor and the R_L represents the load impedance. The voltage bias is provided through R_B along with the DC block capacitances, C_F and C_B. The equivalent small-signal model of the transimpedance amplifier is shown in Figure 4-8(b), where g_m and C_{gs} represents the transconductance of M_1 and the capacitance to ground at the gate of M_1, respectively.

4.4.2.1 Voltage Gain

The voltage gain of the amplifier can be derived by using the small-signal model in Figure 4-8(b).

$$A = \frac{V_{out}}{V_{in}} = -\left(g_m - \frac{1}{R_F}\right) \times (R_L \,||\, R_F) \tag{5}$$



(a) (b)

Figure 4-8 Simplified (a) Schematic and (b) Small-signal Model of the Resistive-feedback Amplifier.

4.4.2.2 *Input Impedance Matching*

The input impedance Z_{in} can be obtained as follow:

$$Z_{in} = \frac{R_f + R_L}{1 + g_{m1}R_L} \,||\, \frac{1}{sC_{gs1}} \tag{6}$$

The input impedance is determined by the open-loop gain and the resistance values of RF and RL, which can be easily controlled.

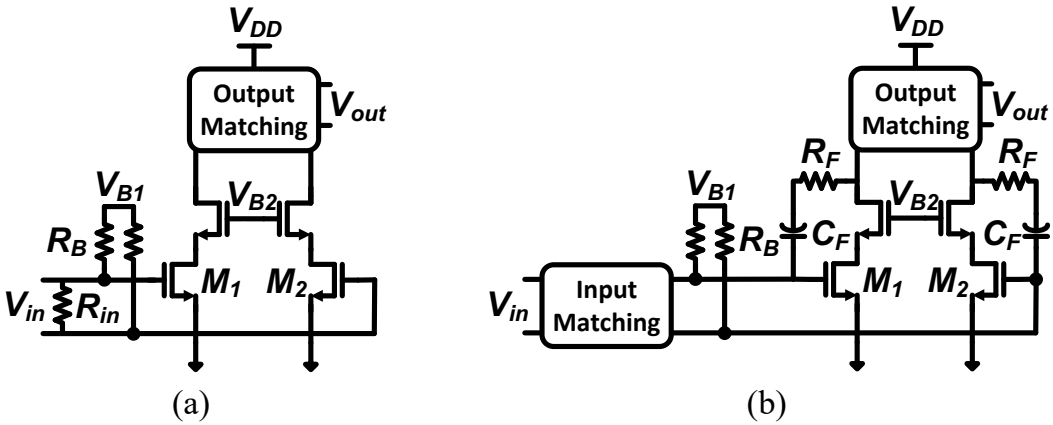


Figure 4-9 Common Source Architectures of (a) Resistive and (b) Resistive-Feedback Input Matching.

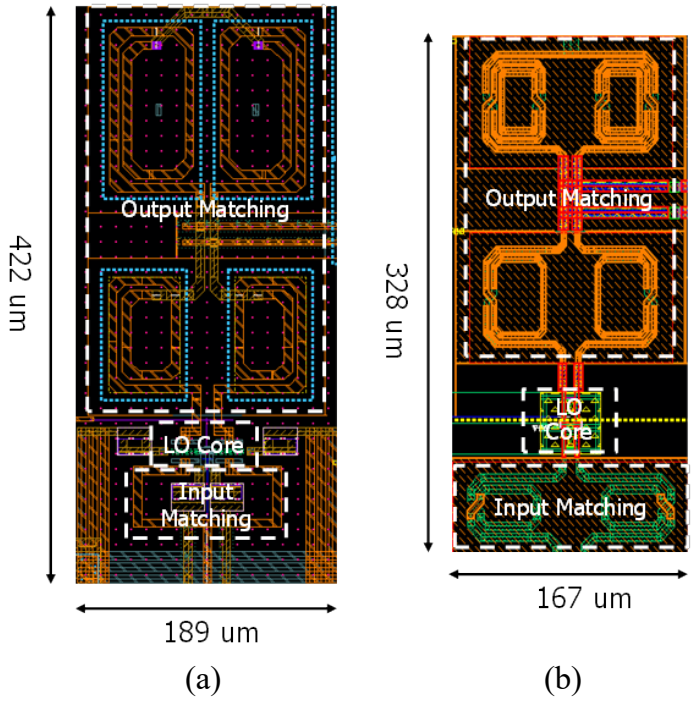


Figure 4-10 Common Source Architectures of (a) Resistive and (b) Resistive-Feedback Input Matching Layout.

4.4.3 LO Driver Schematic and Simulation Results

The LO drivers are implemented in the 45-nm and 12-nm SOI processes with common source architecture of resistive and resistive-feedback input matching, respectively. The schematics and layout of the two different architectures are shown in Figure 4-9 and Figure 4-10.

4.5 Cascaded Sallen-Key Filters

The baseband amplifier is required to provide a moderate gain to mitigate the gain required of the following stages of the mixers and the PA and at the same time the filtering to remove the aliasing tones from the DACs. Two second-order LPF is cascaded to achieve the filtering requirement of the transmitter.

4.5.1 Basic Second-Order Low-Pass Filter

The second-order LPF can be achieved by cascaded two RC networks, R_1 and C_1 and R_2 and C_2. The transfer function can be obtained as follow:

$$\frac{V_{out}}{V_{in}} = \frac{1}{S^2(R1C2R2C1)+S(R1C2+R2C1+R1C1)+1} \tag{7}$$

With equal R and C, the Q is equal to 1/3. The maximum value of Q, which is equal to 1/2, can be achieved when the second RC network is much larger than the first one. However, most filters require Qs larger than 1/2.

4.5.2 Sallen-Key Filter with Positive Feedback

Other than cascaded two first order RC LPF, the second-order topology can be used to achieve sharper roll-off. Second-order topologies such as passive resistor-capacitor-inductor (RLC) filters and active filters provide complex-conjugate poles, which allows the designer to optimize a filter for a particular application. The inductance value in the RLC filter becomes extremely large at a

lower frequency and occupies a large chip area. On the other hand, the active filter is implemented with an operational amplifier (op-amp) in combination with some resistors and capacitors, which provides an RLC-like filter response at a lower frequency. Therefore, a shunt capacitor C_1, a positive feedback capacitor C_F, two series resistors R_1 and R_2, and a negative feedback resistor R_F are integrated with the fully differential baseband amplifiers to create a modified version of Sallen-Key filter as shown in Figure 4-11 (a). An additional LPF is added to the output of the baseband amplifier to increase the order of filtering. Two Sallen-Key filters are cascaded to provide a sharper roll-off.

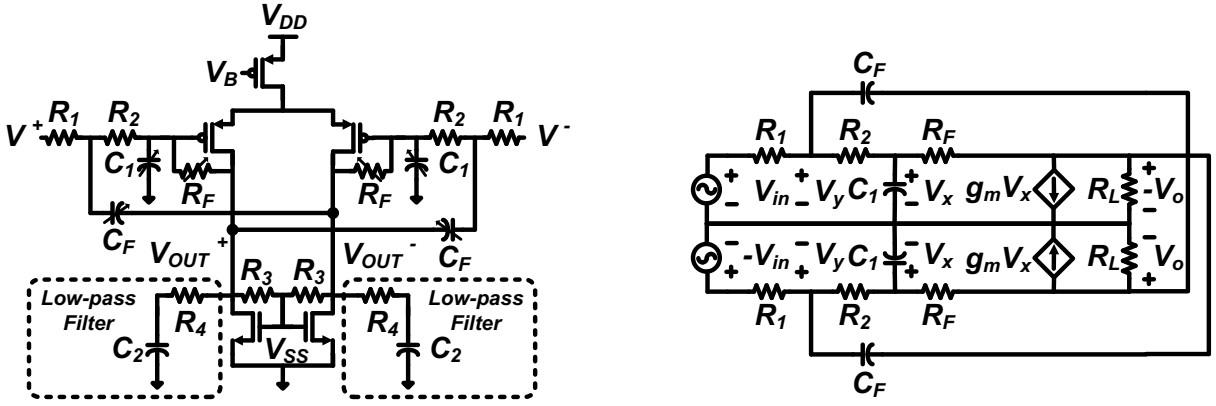
To understand how the modified version of Sallen-Key filter can generate complex poles to provide RLC-like filter response at a lower frequency, a simplified small-signal model as shown in Figure 4-11 (b) can be used to obtain the transfer function as follows:

$$\frac{V_x+V_{out}}{R_F} = g_m V_x - \frac{V_{out}}{R_L} \tag{8}$$

If $R_L \gg R_F$ and $g_m R_F \gg 1$, the output voltage can be obtained as:

$$V_{out} = g_m R_F V_x \tag{9}$$

By using the Kirchhoff's current law (KCL), the voltage V_x and V_y can be found as follows:



(a) (b)

Figure 4-11 (a) Schematic and (b) Simplified Small-signal Model of Modified Sallen-Key Filter.

$$\frac{V_y - V_x}{R_2} = V_x S C_1 + \frac{V_x + V_{out}}{R_F} \tag{10}$$

$$\frac{V_y - V_{in}}{R_1} + \frac{V_y - V_x}{R_2} + (V_1 - V_{out}) S C_F = 0 \tag{11}$$

By organizing the above equation in standard second-order LPF format:

$$\frac{V_{out}}{V_{in}} = g_m R_F \times \frac{1}{S^2 C_1 C_F R_1 R_2 + S(g_m C_F R_1 (R_2 - R_F) + C_1 R_1 + C_1 R_2) + (g_m R_2 + g_m R_1 - \frac{R_1}{R_2})} \tag{12}$$

At lower frequencies, the gain can be approximated as:

$$\frac{V_{out}}{V_{in}} = \frac{g_m R_F}{g_m R_2 + g_m R_1 - \frac{R_1}{R_2}} \tag{13}$$

The Q of the modified Sallen-Key can be obtained as follow:

$$Q = \frac{\sqrt{C_1 C_F R_1 R_2} \times \sqrt{(g_m R_2 + g_m R_1 - R_1/R_2)}}{g_m C_F R_1 (R_2 - R_F) + C_1 R_1 + C_1 R_2} \tag{14}$$

By selecting the values of g_m, C_F, R_1, R_2, and R_F, the Q can be achieved much higher value than 1/2 of the cascaded second-order RC LPF.

4.5.2.1 Digital Control

The gain and the filter response of the cascaded Sallen-Key filters can be varied due to the process variations. Therefore, the capacitor and resistance banks are added to mitigate the process variations as shown in Figure 4-11 (a).

4.5.2.2 Gain and Filter Response of Cascaded Sallen-Key Filters

Adjustable voltage gain and the filter response have been plotted across 0-1 GHz frequency as shown in Figure 4-12. The cascaded architecture demonstrates 9-dB to -2-dB voltage gain controls, ±200MHz filter tuning range, and 0.7-dB gain ripple for the default setting.

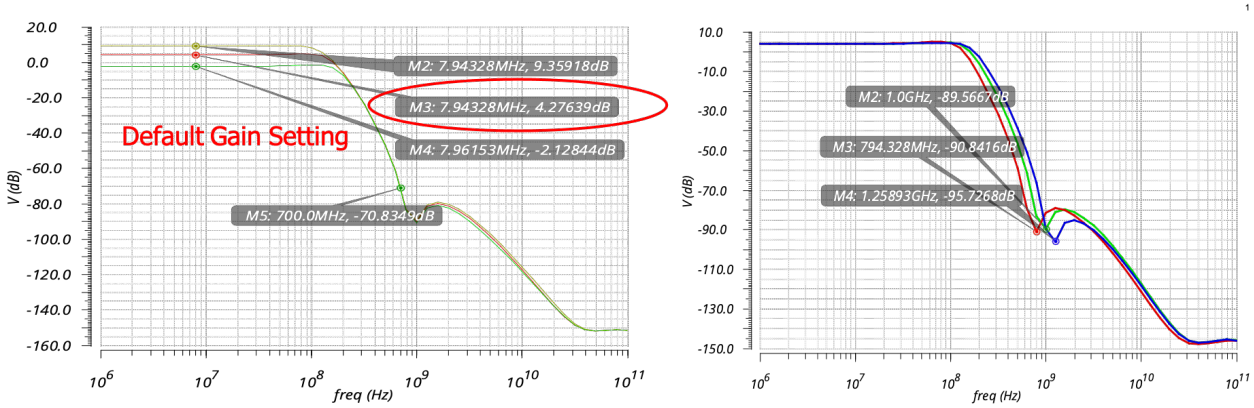


Figure 4-12 (a) Voltage Gain and (b) Filter Response of the Modified Sallen-Key Filter.

4.6 Stacked Double Balanced Active Mixer with Current Mirror Topology

A conventional transmitter comprised of DACs, baseband amplifiers, mixers, and the PA is shown in Figure 4-3. The basic CS topology depicted in Figure 4-3 is widely used in the PA design. For narrow bandwidth applications, a single LC tunning network is implemented at the output of the mixer before the DA or PA stage. However, the LC tuning network significantly reduces the bandwidth. Multiple LC tunning networks for different bands can be employed to achieve wide-frequency range operation. However, the inductors in the LC tunning network occupy a large area and limit the performance for a large frequency range. The area restriction is critical for phased

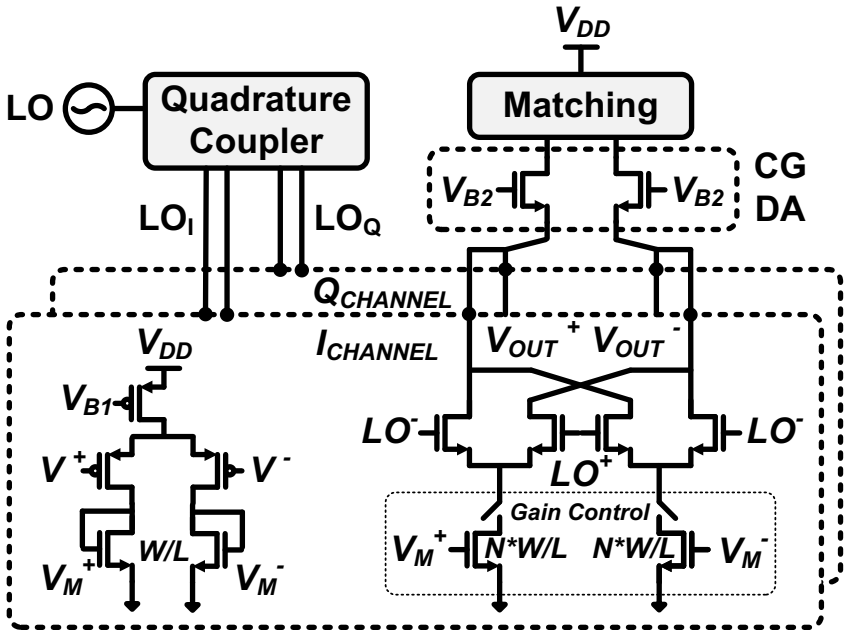


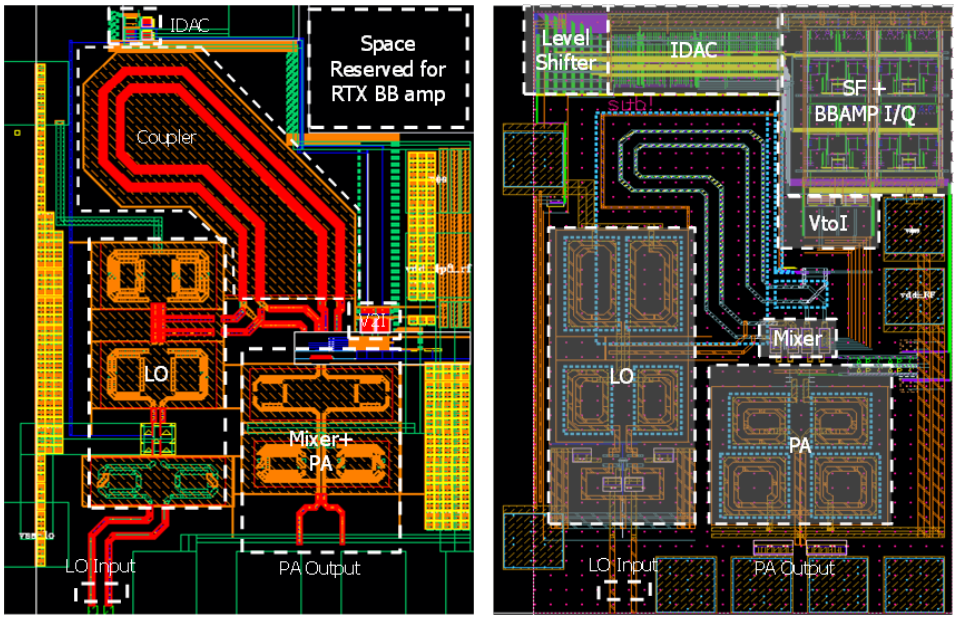
Figure 4-13 Stacked Double Balanced Mixer Architecture with Current Mirror Topology.

array applications with small area requirements. Therefore, a transmitter with multiple LC tunning networks is not suitable for the wide-frequency range applications in the digital phased array system with increased numbers of elements. Compared to the CS topology, the CG topology has an intrinsic wideband performance and good linearity [49]. The CG topology can be implemented to remove interstage LC matching due to its advantages of adjustable and small input impedance. Therefore, additional stacked CG transistors are added on top of the double balanced active mixer without the most critical and area-hungry inductors as shown in Figure 4-13. The current of the double balanced active mixer can be reused by the CG DA, which decreases the total power consumption. Moreover, the low input impedance of the stacked devices reduces the voltage swing at the mixer output and improves the linearity. In principle, with proper bias and transistor sizing, voltage swing can be distributed across the mixer core and the stacked transistors to enhance linearity and reliability. For the thin device in a 45-nm silicon-on-insulator (SOI) CMOS process, the drain-to-source and drain-to-gate voltage swing are constrained below 2.5 V [50]. Moreover, floating-body transistors in the SOI process do not suffer from the body effect and are particularly suitable for the stacking technique when it is compared to the bulk CMOS process.

The conventional double balanced active mixer is known for its good LO-to-RF isolation. The conventional double balanced active mixer requires three stacked transistors, which require a higher voltage supply for the available voltage headroom to achieve high conversion gain and good linearity with the increased bias current. A current mirror topology, which amplifies the converted current from the V2I converter, is stacked with the mixer core as shown in Figure 4-13. The three-bit tunable gain of the current mirror is provided through the switch control of the current mirror transistors as shown in Figure 4-13.

4.7 Layout

The layout of complete transmitter is shown in Figure 4-14 (a) and (b) for 12-nm and 45-nm SOI CMOS processes, respectively. Each layout occupies a chip area of 0.55×0.85 mm^2 and includes an LO driver, a quadrature coupler, input buffers, V2I converters, stacked mixers, an output matching network, and pads. The cascaded modified Sallen-Key filters only show in the 45-nm process since the filters are designed by the cooperated company in the 12-nm process.



(a) (b)

Figure 4-14 Chip Layout of Complete transmitter in the (a) 12-nm and (b) 45-nm CMOS SOI Processes.

4.8 System Simulation Results

4.8.1 P1dB and OIP3

Simulation environment of the transmitter in the 12-nm process:

- A LO driver, a quadrature coupler, input buffers, V2I converters, stacked mixers, and an output matching network.
- IF Frequency: 1 GHz

- RF Frequency: 18 - 50 GHz

Simulation environment of the transmitter in the 45-nm process:

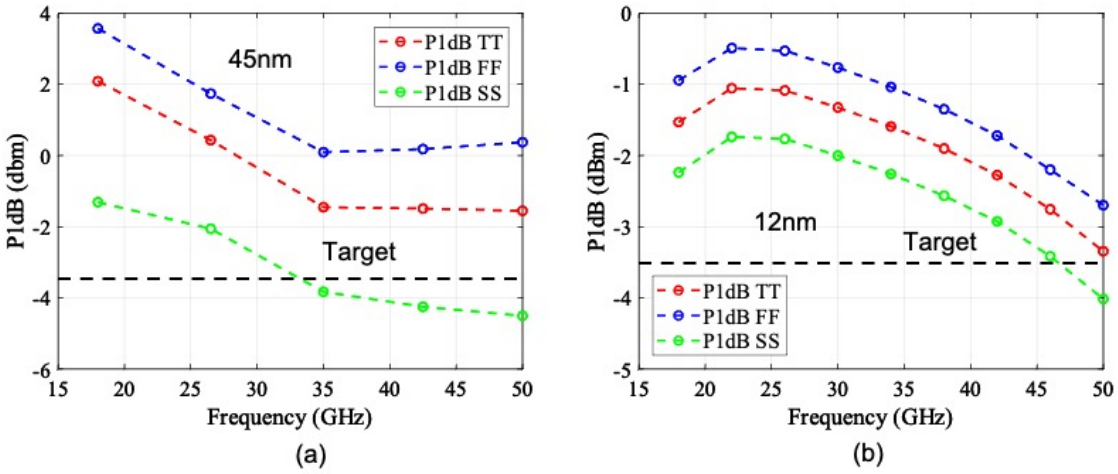
- Cascaded Sallen-Key filters, LO driver, a quadrature coupler, input buffers, V2I converters, stacked mixers, and an output matching network.
- IF Frequency: 100 MHz
- RF Frequency: 18 - 50 GHz

Error! Reference source not found. demonstrates the output 1-dB compressed point (P1dB) o f the transmitter in the 45-nm and 12-nm processes, respectively.

4.8.2 DC Power Consumption

The transmitter consumes 48.8 mW total (I+Q) in the 12-nm process, which only includes the LO driver, a quadrature coupler, V2I converters, stacked mixers, and an output matching network.

- LO Driver: 1.4 V supply with 12.4 mA (17.4 mW)



- V2I and Stacked Mixers: 1.8 V supply with 17.1 mA (31.4 mW)

Figure 4-15 Simulated P1dB of the transmitter in (a) 45-nm and (b) 12-nm processes.

Transmitter consumes 68 mW total (I+Q) in the 45-nm process, which includes Cascaded Sallen-Key filters, LO driver, a quadrature coupler, input buffers, V2I converters, stacked mixers, and an output matching network.

- LO Driver: 1.2 V supply with 14.5 mA (17.4 mW)
- V2I and Stacked Mixers: 1.8 V supply with 18 mA (32.4 mW)
- Cascaded BB Amplifier (I+Q): 1.8 V supply with 7.1 mA (12.8 mW)
- Misc. circuits (I+Q): 1.8 V supply with 3.2 mA (5.8 mW)

4.9 Measurement Results

Only the transmitter chip of the 45-nm SOI CMOS process was measured at the time of writing this thesis, therefore the measurement results of the transmitter chip of the 45-nm SOI CMOS process are presented below.

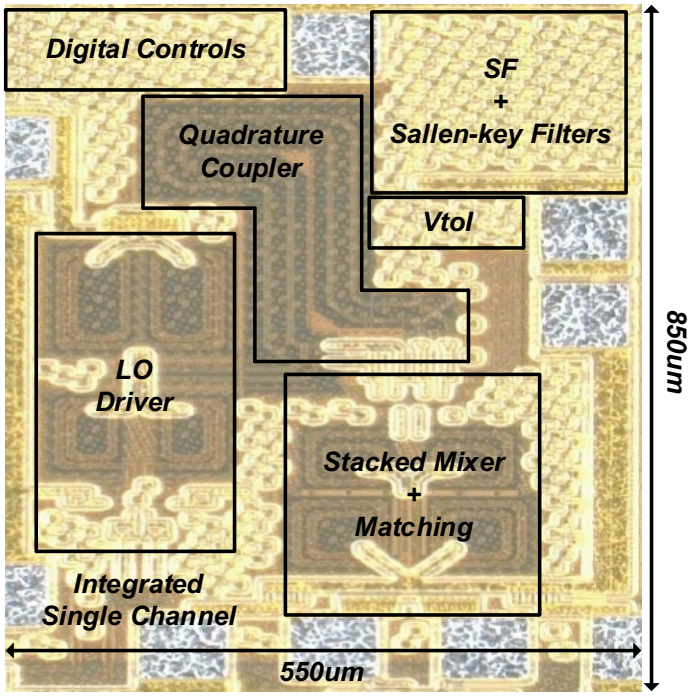


Figure 4-16 The Chip Micrograph of the Integrated Single Channel in the 45-nm Process.

A prototype of the wide-frequency range transmitter, fabricated in a 45-nm SOI CMOS process, has two different versions, a single-channel breakout for the integration with the phased array system and a standalone breakout circuit. For the standalone breakout, the LO and the baseband signals are provided externally through the probes, while those two signals are generated locally in the integrated single channel. Due to pads used for ball grid array (BGA) interconnects in the integrated single channel, the quadrature coupler, and the output matching of the LO driver have been slightly modified from the standalone version. Each prototype occupies a chip area of 0.55×0.85 mm^2 and includes an LO driver, a quadrature coupler, input buffers, cascaded Sallen-Key filters, V2I converters, stacked active mixers, an output matching network, and pads. The chip micrograph of the integrated single channel is shown in Figure 4-16.

The filter response of the cascaded Sallen-Key filters is measured across 0–100-MHz frequency for each standalone breakout and integrated single channel prototype as shown in Figure 4-17. The measured filter response exhibits 20-dB suppression at 300 MHz in the standalone breakout, and

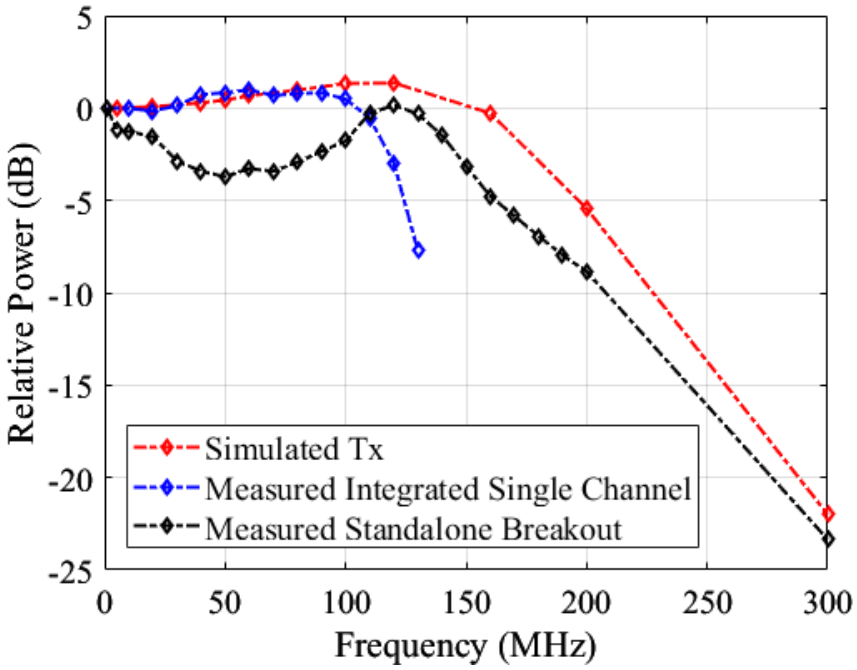


Figure 4-17 Filter Response of the Cascaded Sallen-Key Filters.

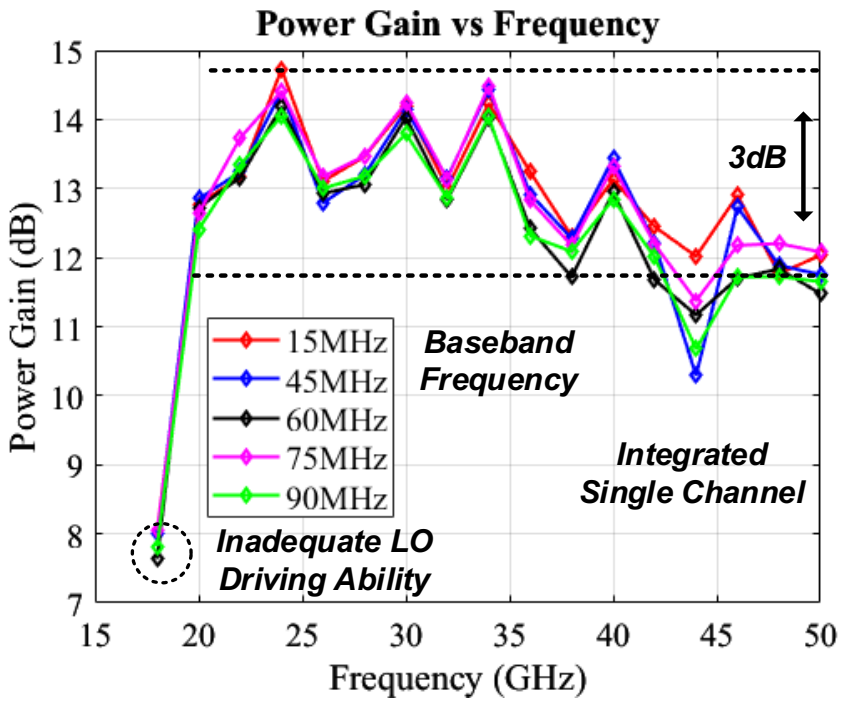


Figure 4-18 The Power Gain Versus Different Baseband and RF Frequencies.

the in-band ripple is due to the impedance mismatch. The in-band flatness is verified by the measurement with the integrated single channel. The roll-off of the filter response is sharper in the integrated single channel due to the digital interpolator LPF.

Figure 4-18 shows the measured power gain of the integrated single channel from the output of a single DAC with 2000Ω differential input impedance to the output of the transmitter with a 100Ω differential load impedance. The power gain is measured with different RF frequencies of 18–50 GHz and the maximum power gain is 14.8 dB. The prototype shows excellent gain flatness except for the minor degradation around 18 GHz and 44 GHz. The 3-dB gain flatness over the frequency range of interest is highlighted with two dashed lines as shown in Fig. 10. The fluctuation in gain comes from the LO signal distribution using a quadrature coupled-line coupler.

In the integrated single channel, the power gain has roll-off at 18 GHz due to the inadequate LO driving ability. Figure 4-19 shows the measured output power versus input power in the standalone breakout with adequate LO driving ability at 18 GHz. The standalone breakout demonstrates a

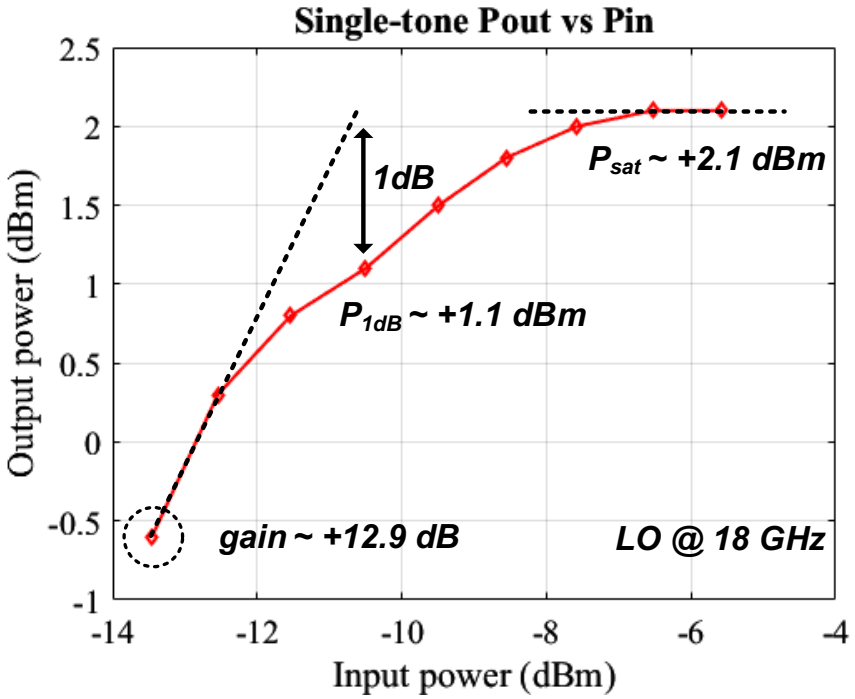


Figure 4-19 Output Power Versus Different Input Power of the Standalone Breakout.

12.9-dB power gain, an output P1dB of 1.1 dBm, and a saturated output power (Psat) of 2.1 dBm at 18 GHz. An indirect comparison to the state-of-the-art transmitters is shown in **Error! R eference source not found.**, as there are key differences in critical specifications among those cited and this work.

4.10 Summary

An 18–50-GHz mm-wave transmitter is introduced. The prototype achieves wide-frequency range operation, compact size, and low-power consumption of the transmitter in the digital phased arrays. The measurement results demonstrate the very wide-frequency range that covers the 18–50-GHz frequency range with excellent gain flatness.

Table 4-2 Performance Comparison with the State of the Art

	ESSCIRC 2005 [51]	ESSCIRC 2010 [52]	**This work**	
Supply (V)	3.3	2.5 / 3.5	1.2 / 1.8	
Process (nm)	130	130	45	
LO/RF Freq. (GHz)	16 - 26	35 - 67	18 - 50	
Fractional BW	0.6	0.66	1.06	
Baseband Freq. (MHz)	-	-	0 - 100	
P1dB (dBm)	-1* @ 24 GHz	3.75* @ 60 GHz	1.1 @ 18 GHz	
Psat (dBm)	1.6* @ 24 GHz	10.7 @ 60 GHz	2.1 @ 18 GHz	
Power gain (dB)	17*	>25	>10	
Power Consumption (mW)	168‡	462‡	55.7	
Suppression (dB)	-	-	>20 @ 300 MHz	
Power Breakdown (%)	-	-	LO driver	25.5
			Stacked mixer	47.3
			Cascaded filters	18.7
			Others	8.5
Area (mm^2)	0.528‡	0.79‡	0.4675†	

† Includes the pads for BGA interconnects.
‡ Bi-phase modulator without I/Q baseband amplifiers and quadrature coupler.
* Estimated from graph.

5 CONCLUSION

The exponential increase of wireless devices along with the newly developed wireless standards such as 5G, Wi-Fi 6 and Bluetooth 5.0 inevitably come with ever-growing bandwidth usage. In addition, the worldwide-available 2.4 GHz spectrum is already overwhelmed with technologies such as Wi-Fi, Zigbee, and Bluetooth. Therefore, the energy and spectrum efficient transmitters with higher data rate, small die area, and low integration cost are required for the rapid growth of data streaming demand in modern communication. The work in this dissertation aims to demonstrate the design and potential of energy and spectrum efficient transmitters in both sub-6 GHz and mm-wave bands. An efficient quadrature digital power amplifier as a standalone transmitter for the sub-6 GHz application employs CDD and dual-supply Class-G to achieve up to four efficiency peaks and excellent SE at PBO. The proposed transmitter achieves excellent linearity and the efficiency at PBO is expected to be significantly enhanced in an advanced CMOS process. Besides the transmitter for the sub-6 GHz application, an 18–50-GHz mm-wave transmitter has been proposed. The proposed mm-wave transmitter is designed for compact size and low-power consumption. Compact integration of antennas with the T/R module has become feasible in mm-wave communication as the antenna size and pitch decrease with an increase in frequency, and the proposed mm-wave transmitter has a huge potential in this regard.

6 FUTURE WORK

The proposed CDD SCPA architecture achieves excellent linearity and the efficiency at PBO can be a promising solution for the sub-6 GHz application. The proposed CDD SCPA architecture supports the OFDM signal up to 40MHz. With advanced CMOS processes, the signal bandwidth can be improved with better CMOS switches performance to support higher signal bandwidth up to 160MHz of IEEE 802.11ax standard. With higher signal bandwidth, the PAs can display significant memory effects, which are not satisfactorily linearized using the LUT approach of DPD. The memory polynomial model will be a good candidate for compensating the memory effects. The feasibility of SCPA at mm-wave bands shows promising results based on the preliminary research. The switching operation of the SCPA driving stage is limited by the switching frequency and the f_T of the CMOS devices.

Compared to the application for sub-6 GHz bands, the efficiency and the output power are further degraded at mm-wave bands. The efficiency boost techniques at PBO applied at sub-6GHz can be implemented at mm-wave bands to compensate for the further decreased system efficiency. The passive devices for output matching networks will shrink significantly, which leads to a compact design of SCPA in mm-wave bands.

The DPA architecture implemented with SCPA has great potential in both sub-6GHz and mm-wave bands, which can have a revolutionary impact on state-of-art communication systems.

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