IMPROVING THE PERFORMANCE OF PASSIVE COMPONENTS OF THE POWER ELECTRONICS AT HIGH SWITCHING FREQUENCY

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ABSTRACT

IMPROVING THE PERFORMANCE OF PASSIVE COMPONENTS OF THE POWER ELECTRONICS AT HIGH SWITCHING FREQUENCY

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Power converters have an important role in modern electric and electronic systems due to different voltage and power level requirements. Magnetic components are considered to be essential elements of the power converters. Storing the energy, filtering the signal, and transferring the energy are the main tasks of the magnetic components in the power converters. With developing the technology of power switches, the power converter can be operated at high frequencies. However, the magnetic components are suffering from their parasitic capacitance at high frequencies. Modeling the parasitic capacitance of the magnetic components is crucial to design power converters at high frequency. To date, the researches that have been conducted to modeling the parasitic capacitance have mainly targeted the low power applications with very high frequencies and high power with multi-layer transformers. Consequently, there remains a blank in the body of knowledge regarding modeling the parasitic capacitance of a single-layer inductor with a magnetic core at medium power. The relation between the number of turns and the parasitic capacitance of the single-layer inductors with the magnetic core should be considered. Moreover, improving the magnetic components by reducing the parasitic capacitance is essential. By using the technique of reducing the parasitic capacitance, the resonant frequency of the magnetic components can be shifted to a higher frequency besides improving the impedance of the inductor. Therefore, this dissertation contributes in four main parts: (1) Modeling the parasitic capacitance of a single-layer inductor with a magnetic core. (2) Reducing the parasitic capacitance using the technique of magnetic coupling. (3) Selecting the appropriate range of high operating frequency for power converter applications. (4) Estimating the parasitic capacitance of interleaved coupled two-phase inductors.

For the first part, a new approach to determining the total parasitic capacitance of a single-layer inductor with the magnetic core at a medium frequency range that is below the first resonant

frequency is presented in this research. The proposed analytical approach can obtain the parasitic capacitance between the winding and core based on the physical structure of the inductor. The analytical approach depends on approximating the rod wire shape to a square shape. The total equivalent parasitic capacitance is derived. The results are verified by finite element analysis and experimental measurements using impedance network analyzer.

The second part of this research presents a technique for improving the performance of an inductor at high frequencies through mitigating effects caused by the parasitic capacitance. This technique adds a small capacitor to the coupled windings of the inductor to reduce the parasitic capacitance of the inductor. The relationship between the parasitic capacitance, magnetic coupling coefficient, and the small capacitor is introduced. The method to size the reduction capacitor is detailed in this research. The results of applying this technique show an improvement in the inductance impedance by 40 dB and shifting the resonant frequency to a higher frequency when $k = 0.97$. The experimental results validated the effectiveness of the proposed technique.

Moreover, a new methodology to properly select the highest operating frequency for the magnetic components in power electronics devices is presented in this research. Several parameters of the magnetic components such as the resonant frequency and the losses of the magnetic core are taken under consideration. The results of this methodology prove the maintaining the efficiency with reducing the volume of the magnetic core by 70%.

Finally, the parasitic capacitance of the interleaved two-phase coupled-inductors is introduced in this research. Besides estimating the parasitic capacitance, the method of determining the size of the interleaved two-phase coupled inductors of boost converter is explained. The result shows the reduction of the size of the two-phase coupled inductors by using the proposed selecting suitable high operating frequency methodology. Moreover, the efficiency of the interleaved coupled inductors boost converter is maintained with reducing the volume by 60% and increasing the operating frequency by doubling the frequency.

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This dissertation is dedicated to my beloved father, Lafi Faheem Alshaabani, my beloved mother, Fatima Salem Alrashidi, and my beloved brothers and sisters.

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CHAPTER 1

INTRODUCTION

In this chapter, the main aspects of improving the magnetic components are presented. For power electronic systems, different methods can be applied to improve efficiency [3–10]. Besides improving the efficiency of magnetic components, an overview of downsizing techniques of the size of the magnetic components is introduced. The research scope and summary of contributions are presented.

1.1 Motivation and Challenge

The main objectives of power converters are to have high efficiency and to also reduce the size of converters. Reducing the size of the converter can be achieved by coupling the magnetic components and/or increasing the switching frequency [3, 5, 8–10]. By coupling the magnetic components, the losses of conductors and magnetic materials are decreased, besides reducing the size of converters [4, 8–10]. The switching frequency of power converters is the main aspect of reducing the size of magnetic components and devices of the converters [3, 5, 8]. However, by reducing the volume of power converters at high frequencies, the efficiency and performance of power electronic systems are reduced [11–17]. One of the main reasons for reducing the efficiency of power converters at high frequency is the effects of parasites of magnetic components [11, 12, 14, 15, 17–22].

Magnetic components of power converters such as inductors, choke inductors, interleaved coupled inductors, and transformers have parasitic elements that appear at high frequency [14, 17, 18]. There are two types of parasites of magnetic components, they are parasitic capacitance and parasitic resistance. Conductor and magnetic losses, eddy and proximity currents cause the parasitic resistance. The parasitic capacitance can be caused by capacitances between turn-to-turn, layer-to-layer, and winding-to-core [14, 17, 18, 21, 22]. Because of the parasitic capacitance of magnetic components, the efficiency of the power converter is reduced at high frequency. Also, it is the reason why the magnetic components have a resonant frequency, which will cause

electromagnetic interference [18]. Therefore, this research aims to model the parasitic capacitance of magnetic components in order to avoid operating and designing the power converters at the resonant frequency and also around it.

The modeling of the parasitic capacitance of magnetic components has been a major and challenging research area for decades, and is considered in the following classification [12, 14, 15, 17–22]:

- Single-layer inductors with conductive core for applications of very high frequencies such as EMI filters.
- Single-layer inductors with air-core at high frequency.
- Multi-layers inductors with high frequency.
- High frequency transformer applications.

To improve the modeling and calculations of the parasitic capacitance of magnetic components, the operating frequency of power converters should be divided in specific categories. There are three ranges of frequency that can be applied to power converters, they are : low frequency range (the parasitic capacitance does not affect the inductor behavior), medium frequency range (the characteristic of an inductor starts to get affected until the frequency reaches the first resonant frequency), and high frequency range (frequencies above the first resonant frequency such as radio frequency and EMI filter applications). The existing methods of modeling the parasitic capacitance for the single-layer inductors with magnetic core have some issues that do not work properly for the power converter with medium power range and medium frequency range. Some issues of existing methods of modeling the parasitic capacitance for single-layer inductors with magnetic core are the methods have no relationship between the number of turns and the parasitic capacitance while the experiment and simulation results show a relationship between them. Another issue of the existing methods of parasitic capacitance is the distance between turns and the core are not included. Because of the quick developments of switching frequency technology for medium and high power

converters, this research focuses on medium frequency range with medium power range to model the parasitic capacitance. The modeling of parasitic capacitance of this research concentrates on the single-layer inductors with magnetic core.

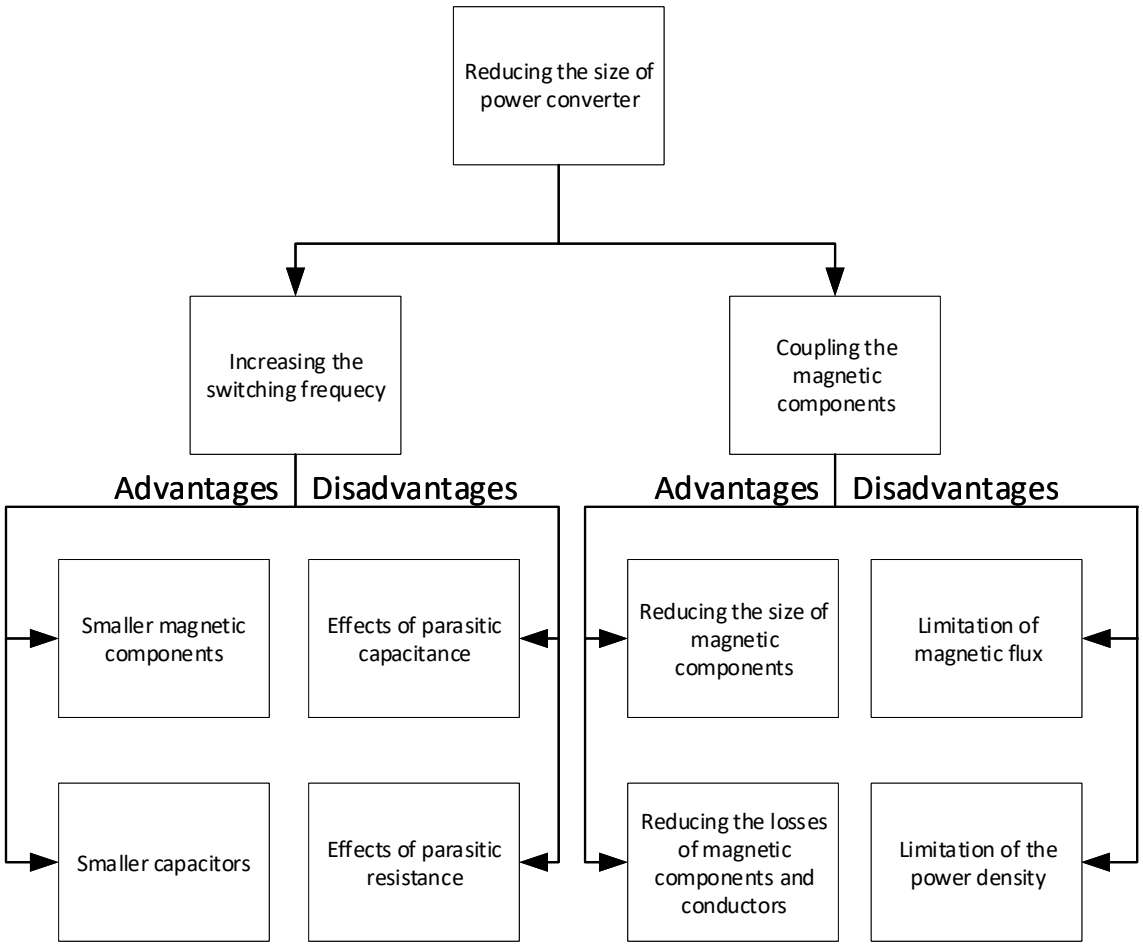


Figure 1.1: A flowchart of methods to reduce the size of magnetic components.

Figure 1.1 shows the flowchart of the methods for reducing the size and volume of power electronic systems. The flowchart presents the main advantages and disadvantages of each method of reducing the size of power converters.

Another objective of power converters in high frequency is improving the efficiency of power converters. It is essential to improve the efficiency of the magnetic components in the power converter. There are two ways to improve the performance of magnetic components. The magnetic components can be improved by reducing the losses of their material [3, 12, 23–25]. Another

method to improve the efficiency is by reducing the parasitic capacitance of magnetic components [11, 26–31].

Reducing the parasitic capacitance of magnetic components has been a challenging area for decades [11, 26–31]. The techniques of reducing the parasitic capacitance are applied based on the applications [28]. Improving the method of reducing the parasitic capacitance is essential for power converter applications.

There are two main methods of reducing the parasitic capacitance. Using the mutual capacitance between two inductors can be applied to reduce the parasitic capacitance of inductors [27, 28]. Another method of reducing the parasitic capacitance is by utilizing the mutual inductance. Using the mutual inductance with adding a small capacitor can generate a negative capacitance [26, 28, 30–33]. The negative capacitance can reduce the parasitic capacitance of the coupled inductors. Estimating the appropriate value of the small capacitor is an essential topic to reduce the parasitic capacitance. This research focuses on estimating the value of the small capacitor when the coupled inductors are not perfectly coupled $k \neq 1$ to reduce the parasitic capacitance by generating the negative capacitance.

The estimating of the parasitic capacitance for the magnetic components can lead to the design of the power converter with reducing the total size of the converter. By selecting the appropriate speed of the switching frequency based on estimating the parasitic capacitance value with considering the resonant frequency of the magnetic components, The capacitor value and the number of turns of the magnetic components of the power converter can be reduced with increasing the switching frequency. The losses of the magnetic components are reduced through decreasing the number of turns of the magnetic components which yields to improve the efficiency of the power converter. As a result of improving the magnetic components of power converters at high frequency, the power converter should be designed to achieve a smaller size with maintaining the efficiency. To maintain the performance with reducing the size of the power converter for medium power applications, the two methods of reducing the size of the converter can be applied.

Recently, many researches focused on the applications of electric vehicles to improve the

efficiency and to reduce the size of the power converters [4, 7–10, 34–37]. One of the major issues in the electric vehicle is the volume of the electric power-train [4, 7, 38, 39]. The effective technique to reduce the volume and size of the electric power-train is downsizing the DC-DC converter that is located between the storage unit and motor inverter [4, 7, 38–40]. The DC-DC boost converter can be applied in different topologies as shown in Figure 1.2. The effective topology that can reduce the total size of the DC-DC converter is the multi-phase boost converter with interleaved coupled inductors [4]. However, reducing the size of the multi-phase boost converter by coupling the inductors can be downsized more by considering the estimating value of the parasitic capacitance to operate it at a specific frequency. It is essential to estimate the parasitic capacitance based on the proposed method of determining the parasitic capacitance for medium power and medium frequency range, which concentrates on the single-layer inductors with a magnetic core, while all the existing methods of determining the parasitic capacitance for single-layer inductors with a magnetic core focus on low power application with high frequency. Moreover, the existing methods of determining the parasitic capacitance for single-layer inductors with a magnetic core have the main disadvantage that is there is no relationship between the parasitic capacitance and the number of turns, even if the experiment and simulation results show the relationship between the number of turns and the parasitic capacitance as presented in [12, 41, 42]. Also, the relationship between the parasitic capacitance and the distance between turns and a core is not included in the existing methods of determining the parasitic capacitance of the single-layer inductors with the magnetic core while the proposed method has a relation between the parasitic capacitance and the distance between turns and the core. For these reasons, estimating the parasitic capacitance of multi-phase inductors is essential and considered in this research by using the proposed method of determining the parasitic capacitance for single-layer inductors with a magnetic core.

As a result, the DC-DC interleaved boost converter will be designed based on the proposed estimating of the parasitic capacitance of the inductors with increasing the switching frequency. By increasing the switching frequency, the size of other components of the power converter will be reduced such as output capacitors, footprint of the printed circuit board which leads to saving the

board space, and the magnetic components.

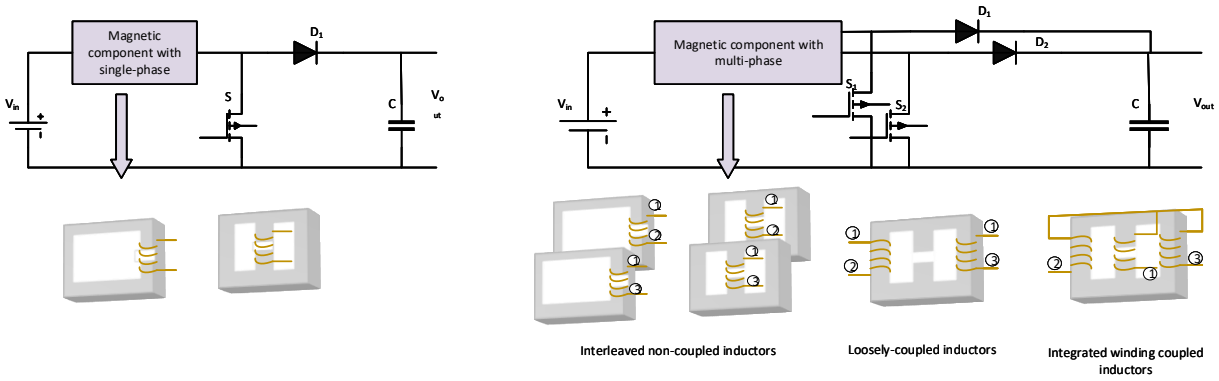


Figure 1.2: Different topologies of DC-DC boost converter.

1.2 Problem Statement

As the technology of power switches develops, the power converter can operate at higher frequencies. These high frequencies create the likelihood of unwanted parasites such as parasitic capacitance in the magnetic components. It is imperative to model the parasitic capacitance to improve performance. For example, the parasitic capacitance can be reduced by using the proposed methods which leads to enhanced performance.

To reduce the size along with improving the performance of the power converter at high frequencies, a new methodology of selecting a proper high operating frequency is required. By properly selecting the suitable high operating frequency, the total volume of the power converter can be downsized while maintaining the efficiency. It is important to model and design the power converter and magnetic components in the early stages of designing to prevent cataclysmic ramifications in the converter.

1.3 Objective

The objective of this research is to minimize the losses of the magnetic components of the DC-DC power converter and to downsize the magnetic components by estimating and reducing the parasitic capacitance. Moreover, the DC-DC power converter can have a smaller size with

maintaining efficiency by selecting a suitable high operating frequency.

1.4 Research Scope and Contributions

The purpose of this research is to present a new approach of modeling the parasitic capacitance of magnetic components, the technique of reducing the parasitic capacitance of magnetic components, the new methodology of properly selecting a high operating frequency, and reducing the size of the interleaved boost converter with two-phase coupled inductors based on the modeling of the parasitic capacitance. The outcome of this work is to improve the performance of the power converter with reducing its total size. Improving the performance of the power converter can be done by selecting the proper high operating frequency which yields to reducing the number of turns, a magnetic core size of the magnetic components, the DC link input capacitor and output capacitor, and saving the board space. Then the losses of the magnetic components are reduced. Moreover, reducing the size of the total power converter can be done by reducing the magnetic core volume and the output capacitor value. The power converter should be designed based on estimating the value of the parasitic capacitance to select the appropriate switching frequency speed. The contributions of this research can be summarized in the following:

- Generalizing the frequency response of magnetic components based on the impedance of parasitic capacitance.
- Proposing a novel method to estimate the parasitic capacitance of power converters. To the best knowledge of the author, this is the first approach of modeling the parasitic capacitance of single-layer inductors for medium power.
- Generalizing the overall parameters affecting the parasitic capacitance of the magnetic components.
- Proposing a new technique of reducing the parasitic capacitance to estimate the generated negative capacitance based on the magnetic coupling coefficient.

- Proposing a new methodology of properly selecting a high operating frequency for the power converter which can offer reducing the magnetic components volume with maintaining the performance. To the best knowledge of the author, this is the first methodology of selecting the suitable high operating frequency with maintaining the efficiency.

- Estimating the parasitic capacitance of multi-phase inductors to design the power converter with coupling the magnetic components at high frequency.

1.5 Research Organization

The rest of this research is organized as follows. In chapter 2, overview of the magnetic components is presented. The existing methods of determining the parasitic capacitance for single-layer inductor with magnetic core is shown in chapter 3. The new modeling of the parasitic capacitance for single-layer inductor with magnetic core is introduced in chapter 4. The investigating of the overall parameters affecting the parasitic capacitance of magnetic components is introduced in chapter 5. In chapter 6, the techniques of reducing the parasitic capacitance are presented. The new technique of reducing the parasitic capacitance by using the mutual inductance is shown in chapter 7. In chapter 8, the new methodology of properly selecting the operating frequency of magnetic components for power converter is presented. The interleaved two-phase coupled-inductors boost converter with estimating the parasitic capacitance is shown in chapter 9. Finally, the conclusion and the future work are presented in chapter 10.

CHAPTER 2

MAGNETIC COMPONENTS IN POWER CONVERTER

In this chapter, The overall magnetic core materials for power electronic systems is presented. Different shapes of magnetic core with their applications are introduced.

2.1 Overview about the Magnetic Components

Magnetic components in power electronics have different shapes and materials based on the desired application. The magnetic components contain two parts, are the coil of winding and the magnetic core or air-core. The magnetic core is a piece of magnetic material that has magnetic permeability. The magnetic permeability is an important feature to select the appropriate core type [3, 5, 25]. The magnetic core can be made from two main material types, are ferromagnetic metal and ferrimagnetic compounds. Each type of magnetic material and shape has advantages and disadvantages which can be applied for certain applications with specific frequencies and watts.

Based on the desired application, the magnetic core shape is selected. The magnetic core has several shapes, is designed based on the reduced losses of eddy currents and hysteresis besides the magnetic permeability, usage of power, and frequency limit [1, 25]. Figure 2.1 shows several different designs of magnetic core [1, 25]. Some magnetic core designs can work with most power electronics applications such as toroid, E-I, and U-I cores.

2.1.1 Toroid Core

Toroid core or choke inductor is used widely in electric and electronic systems. In the power electronic systems, the inductor and transformer with toroid core are essential parts.

Toroid magnetic core is mainly applied for broadband transformers, common mode chokes, converter and inverter transformers, noise filters, pulse transformers. However, the power used for toroid should be at a low power and it can work with high frequency. Figure 2.2 shows inductor and transformer with toroid magnetic core.

(a) Toroid core.

(b) U-R core.

(c) RS/DS core.

(d) U-I core.

(e) Pot core.

(f) ETD core.

(g) E-I core.

(h) RM core.

Figure 2.1: Several designs of magnetic core

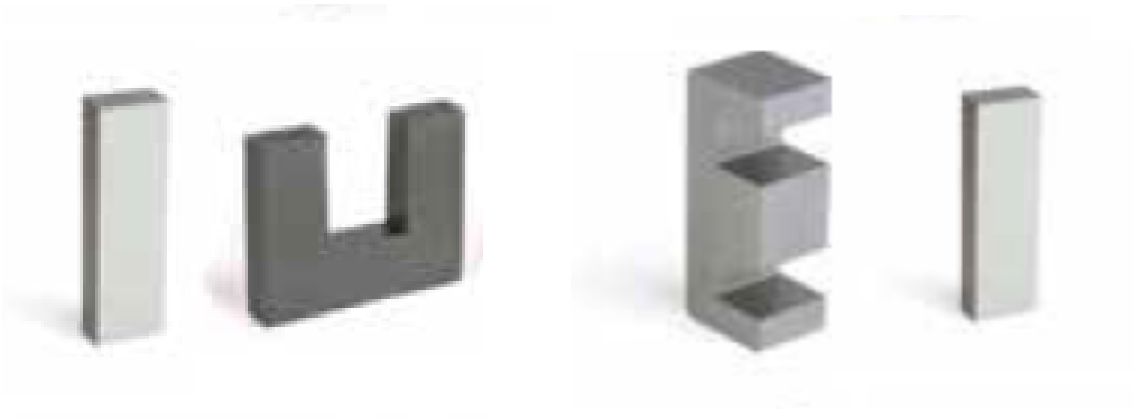
Figure 2.2: Toroid core [1].

2.1.2 U-I Core & E-I Core

The other important magnetic core designs are E-I and U-I cores. The two types of the magnetic core are used widely in electrical, electronics, and power electronic systems. The main advantage of these magnetic core shapes is having a high saturation level besides low losses [2]. The main applications for E-I magnetic core are the interleaved converter for an electric vehicle, differential mode, power and telecoms inductors, as well as the power converter and inverter transformer. The power transformer applications are ideally using U-I magnetic core. Also, the U-I core is applied for high-frequency transformer applications in power electronics such as dc-dc converter with high frequency [2]. Figure **??** depicts two types of magnetic cores which are E-I core and U-I core.

2.1.3 Magnetic Core Selected

The main focus of this research is to improve the magnetic component efficiency in power converters. For this reason, three types of magnetic components are studied. Toroid core is chosen for canceling the parasitic capacitance to improve the converter with single-phase and high frequency. Other types of the magnetic core, which are E-I core and U-I core, are selected to study and model the parasitic capacitance for a single-layer inductor. The reason for modeling this type of magnetic core



(a) U-I core [1].

(b) E-I core [1].

Figure 2.3: Two-different shapes of magnetic core.

is because no paper has been modeled for this type of magnetic component, besides the increasing use of magnetic geometry with wide-bandgap technology.

CHAPTER 3

EXISTING METHODS OF DETERMINING THE PARASITIC CAPACITANCE FOR SINGLE LAYER INDUCTORS

Inductors with a single layer are widely used in many applications. They can be used at any level of frequency range. However, the frequency response of inductors with magnetic core are different from the response of inductors with air core at high frequency. [13, 15, 17, 19, 22, 43]. The inductors with air core are mainly applied with high frequency applications while the inductors with magnetic core are preferred to be applied in low and medium frequency [13, 16, 18, 19, 21]. There are many researches on modeling the parasitic capacitance of single layer inductors with air-core [13, 19, 22, 43]. However, There exists a few models that consider modeling the parasitic capacitance of single layer inductors with magnetic core [15, 17, 22, 43, 44].

The parasitic capacitance of single layer inductors with a magnetic core are modeled for applications with high frequency (HF) and low power such as EMI filter, RF filter, and common-mode choke filter. It is important to study the techniques of modeling the parasitic capacitance for single layer inductors with a magnetic core at HF in order to determine a new approach of modeling the parasitic capacitance in medium frequency and medium power range.

The existing techniques of estimating the parasitic capacitance of single layer inductors with magnetic core focus on the parasitic capacitance between turns and the parasitic capacitance between turns and a core [15, 17, 22, 43, 44]. Most of these techniques are using toroid core to determine the parasitic capacitance. The distinguished methods of determining the parasitic capacitance of single layer inductors with magnetic core are presented in the following.

3.1 Basic cells method to determining the parasitic capacitance

Massarini and Marian, the authors of "Self-Capacitance of Inductors", are the first scientists who made a method to predict the parasitic capacitance of inductors [17, 43]. This method depends on the direction of the electric field lines. By applying the basic cells method as shown in Figure

3.1, the parasitic capacitance can be determined by a function of a few parameters.

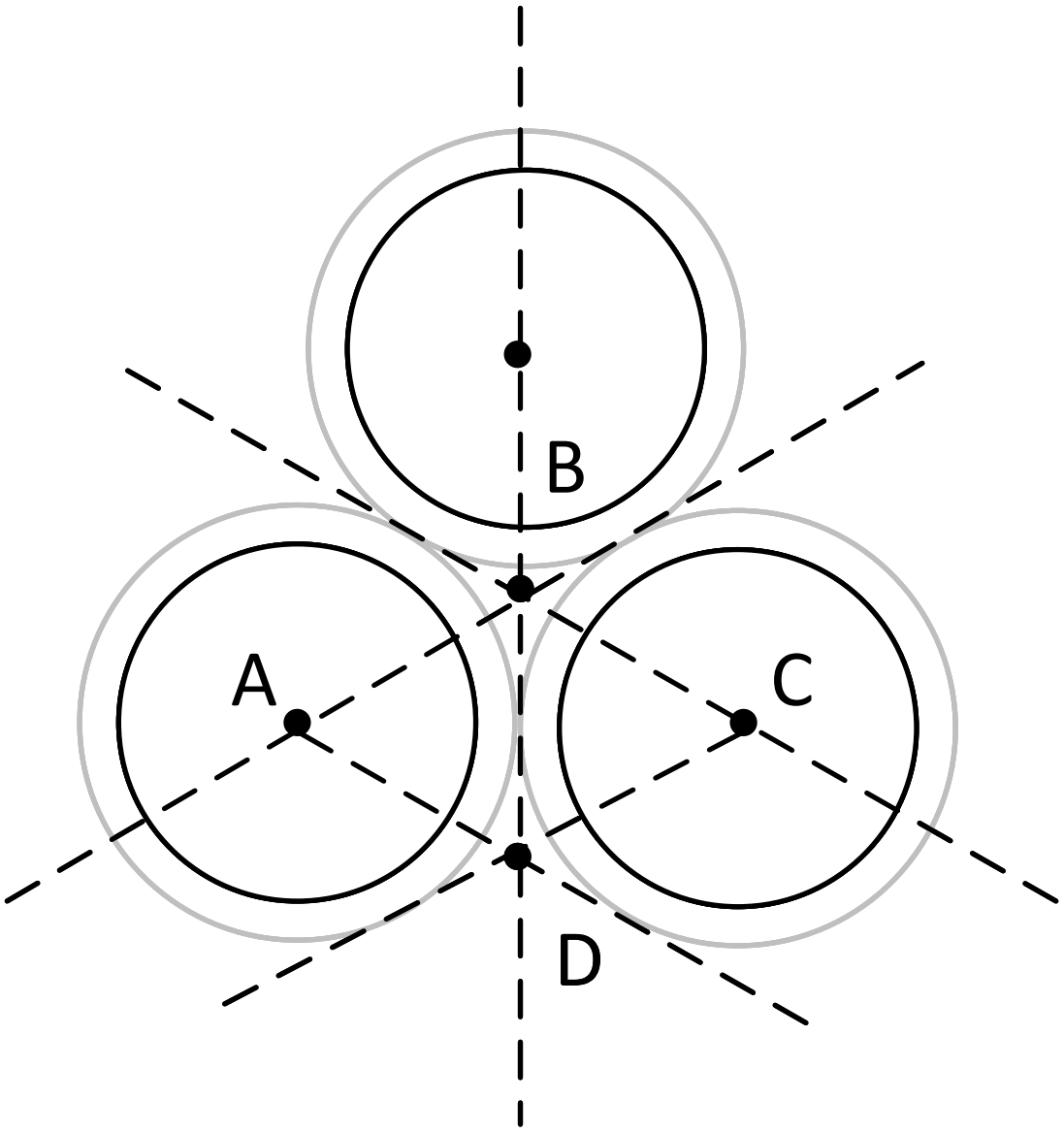


Figure 3.1: The basic cells method.

This paper provides an approximated model to determine the parasitic capacitance. This model depends on the angle of electric field lines between adjacent turns. The turn-to-turn capacitance is

represented by C_{tt}. C_{tt} can be determined as following.

$$\begin{aligned} C_{tt} &= \epsilon_o l_t \int_0^{\frac{\pi}{6}} \frac{1}{1+\frac{1}{\epsilon_r}\ln\frac{D_o}{D_c}-\cos\theta} \\ &= \epsilon_o l_t \frac{2\epsilon_r \arctan\left[\frac{\left(-1+\sqrt{3}\right)\left(2\epsilon_r+\ln\frac{D_o}{D_c}\right)}{\left(1+\sqrt{3}\right)\sqrt{\ln\frac{D_o}{D_c}\left(2\epsilon_r+\ln\frac{D_o}{D_c}\right)}}\right]}{\sqrt{2\epsilon_r \ln\frac{D_o}{D_c}+\left(\ln\frac{D_o}{D_c}\right)^2}} \end{aligned} \tag{3.1}$$

where the diameter of the conductor with and without the coating are represented by D_o and D_c, respectively. The length of a turn is l_t. The angle between two adjacent turns, which is represented by θ, is shown in figure3.2. Since the path lengths of the lines of the electric field between the turn and a core in the air gap are one half of the path lengths between two adjacent turns in the air gap, the parasitic capacitance between a turn and core can be approximated. The parasitic capacitance between a turn and core is denoted as C_{tc}.

$$C_{tc} = 2C_{tt} \tag{3.2}$$

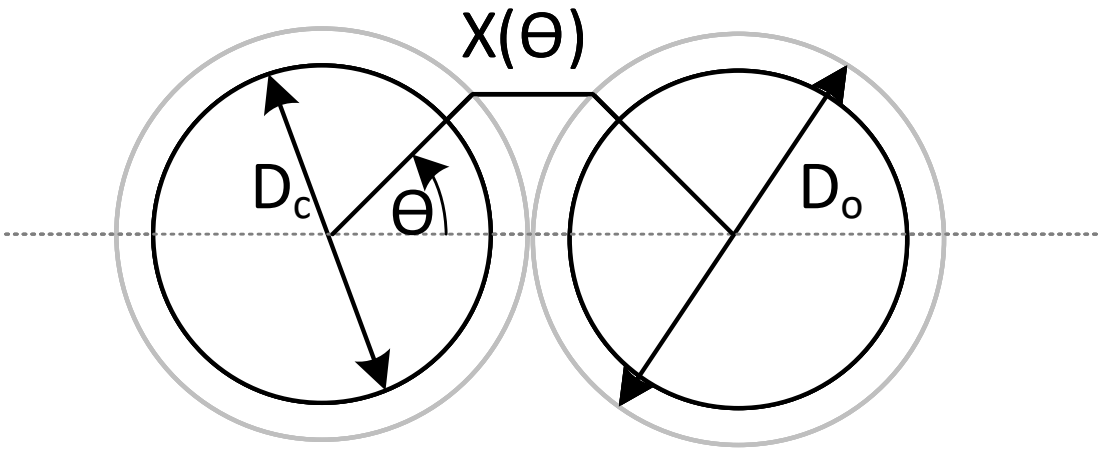


Figure 3.2: The electric field line between two turns.

For a single-layer coil with a conductive core, the total parasitic capacitance can be approximated

based on the number of turns. If the number of turns are even and less than 10 turns, the parasitic capacitance can be determined as follows

$$C_s(n_{even}) = \frac{C_{tt}C_s(n_{even}-2)}{2C_s(n_{even}-2)+C_{tt}} + C_{tt} \tag{3.3}$$

where C_s is the total parasitic capacitance. The even number of turns can be represented by n_{even} while the odd number of turns is n_{odd}. The total parasitic capacitance of an inductor with odd number of turns that is less than 10 turns is expressed as follows.

$$C_s(n_{odd}) = \frac{C_{tt}C_s(n_{odd}-2)}{2C_s(n_{odd}-2)+C_{tt}} + C_{tt} \tag{3.4}$$

The total parasitic capacitance of any number of turns can be calculated. The following equation is to calculate the total parasitic capacitance.

$$C_s(n) = \frac{C_t t}{2+\frac{C_{tt}}{C_s(n-2)}} + C_{tt} \tag{3.5}$$

The equation of calculating the total parasitic capacitance, which is represented in (3.5), becomes a convergent value after 10 turns. Therefore, the total parasitic capacitance can be as a constant value of inductors with more than 10 turns. The parasitic capacitance can be approximated as following.

$$C_s \cong 1.366C_{tt}, \quad for\ n \geq 10 \tag{3.6}$$

3.1.1 Advantages and Disadvantages

The new method of determining the parasitic capacitance of single-layer inductors with a magnetic core has several advantages as well as disadvantages. The following points represent the advantages of this method.

- This paper is considered to be the first analytical method that focuses on determining the parasitic capacitance.

- The analytical method is applied to applications with high frequency.
- A few parameters can determine the parasitic capacitance.
- The accuracy of this method's result is good compared with the experimental's.

While there are advantages in this method, there are disadvantages as well. The following points summarize the drawbacks of this method.

- This method can not estimate the parasitic capacitance of applications with frequencies lower than the first resonant frequency.
- The space between turns can not be increased in this method.
- There is no distance included between turns and core.
- The parasitic capacitance of any inductors is constant when the number of turns goes over 10 turns.
- There is no relationship between the number of turns and the parasitic capacitance.

3.2 Modeling the Parasitic Capacitance of Common-Mode Choke

The paper for modeling the parasitic capacitance of common-mode choke is proposed in [15]. This model is an extension to the method of estimating the parasitic capacitance with high frequency applications in [17, 43]. The contribution of this model is to calculate the parasitic capacitance of common-mode choke when there is distance between turns and between a turn to core.

The proposed model is based on determining the electric field lines between turns as well as between a turn and core. Figure 3.3 shows the electric filed lines between turns. The electric filed lines can be approximated as a circular arc, where the end of the circular arc is perpendicular to the surface of a conductor. In order to calculate the capacitance between turns and between a turn to core, three different regions are analyzed that are known as the inner, outer, and lateral regions. The inner and outer regions have different arc lengths between turns that are δ_{in} and δ_o, respectively.

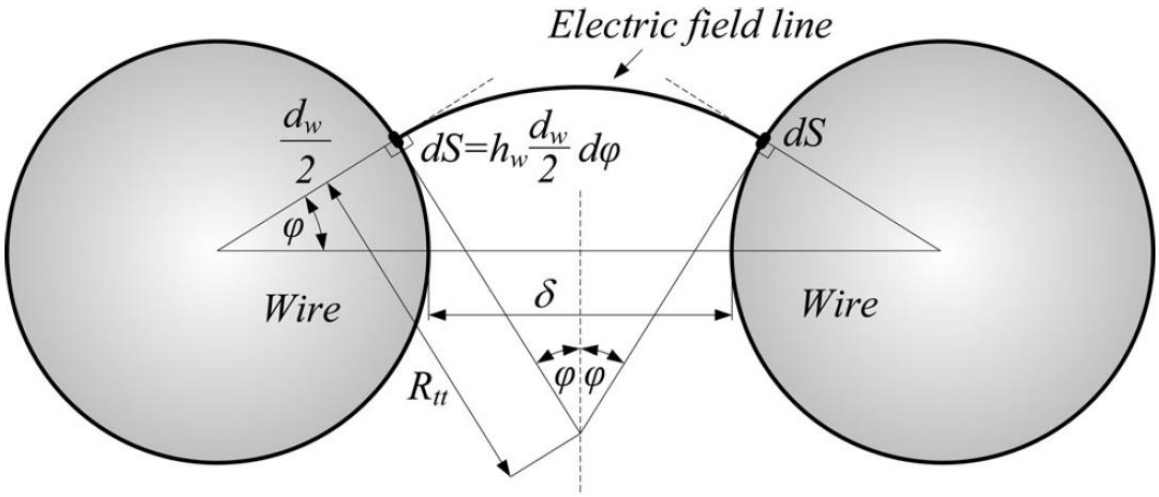


Figure 3.3: The electric filed lines between turns.

The radius of the inner and outer arc of the electric field lines are R_{ttin} and R_{ttout}. R_{ttin} can be determined as following.

$$R_{ttin} = \left[\frac{\delta_i n}{2} + \frac{d_w}{2}(1-\cos\theta)\right]\frac{1}{\sin\theta} \tag{3.7}$$

where the bare conductor diameter is denoted by d_w. θ is the angle of the electric field line. The radius formula can be expressed as a function of θ. Therefore, the turn-to-turn capacitance of the inner region C_{ttin} can be expressed as shown.

$$C_{ttin} = \epsilon_o h_w \frac{d_w}{2}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{\sin\theta d\theta}{\theta\left[\delta_{in} + d_w(1-\cos\theta)\right]} \tag{3.8}$$

where

$$h_w = h_{cpl} + 2w_s + d_w \tag{3.9}$$

The conductor length in either inner or outer region of the core is represented by h_w where h_{cpl} is the core height with plastic case. The distance between the conductor surface and the core plastic is w_s as shown in figure 3.4. The turn-to-turn capacitance of the outer region C_{tto} is following the same procedure of the capacitance between turns of the inner region.

$$C_{tto} = \epsilon_o h_w \frac{d_w}{2}\int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{\sin\theta d\theta}{\theta\left[\delta_{o} + d_w(1-\cos\theta)\right]} \tag{3.10}$$

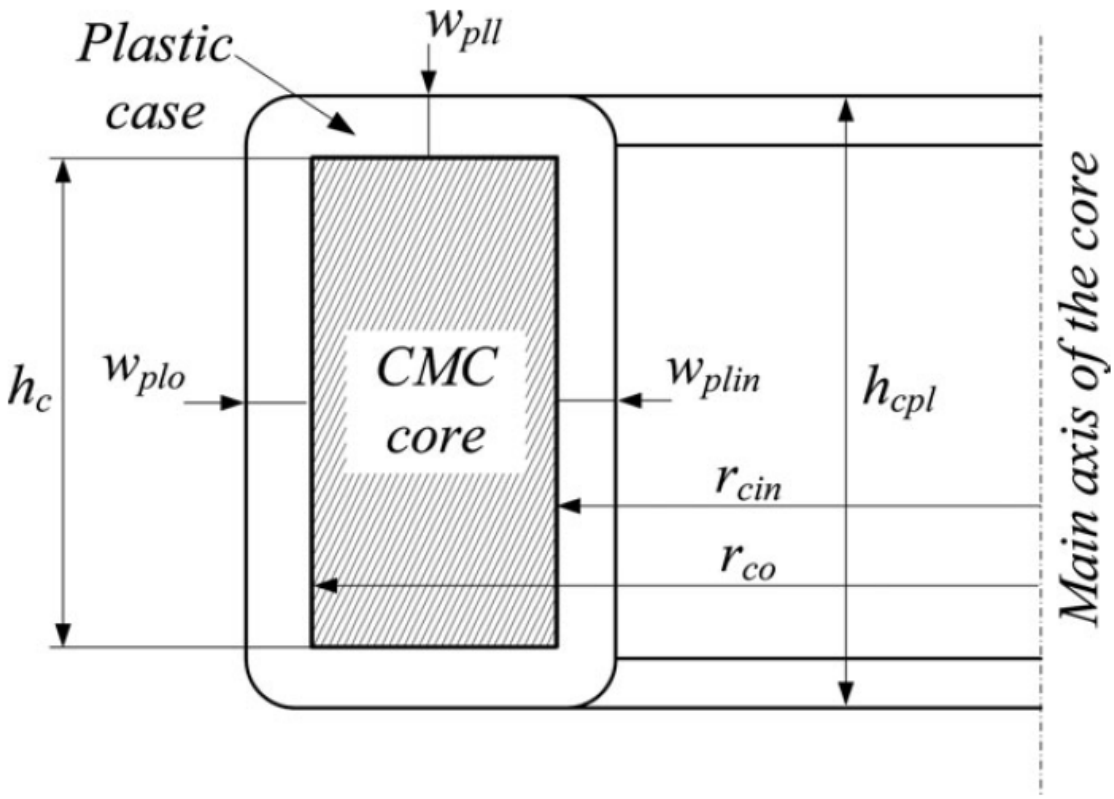


Figure 3.4: The cross section of the core geometry.

The last region of turn-to-turn capacitance is the lateral region. The capacitance in the lateral region is denoted as C_{ttl}. It can be determined as followed.

$$C_{ttl} = \epsilon_o \frac{d_w}{2} \int_{r_{in}}^{r_o} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{\sin\theta d\theta dr}{\theta\left[\frac{\delta_o - \delta_{in}}{r_o - r_{in}}(r - r_{in}) + \delta_{in} + d_w(1 - \cos\theta)\right]} \tag{3.11}$$

where the definitions of δ_o, δ_{in}, r_o, and r_{in} are shown in figure 3.5. The total parasitic capacitance of turn to turn can be determined as followed.

$$C_{tt} = C_{ttin} + C_{tto} + 2C_{ttl} \tag{3.12}$$

The capacitance between a turn and core has a similar way of calculating the capacitance between turns. Figure 3.6 shows the electric filed line between a turn and core. The capacitance

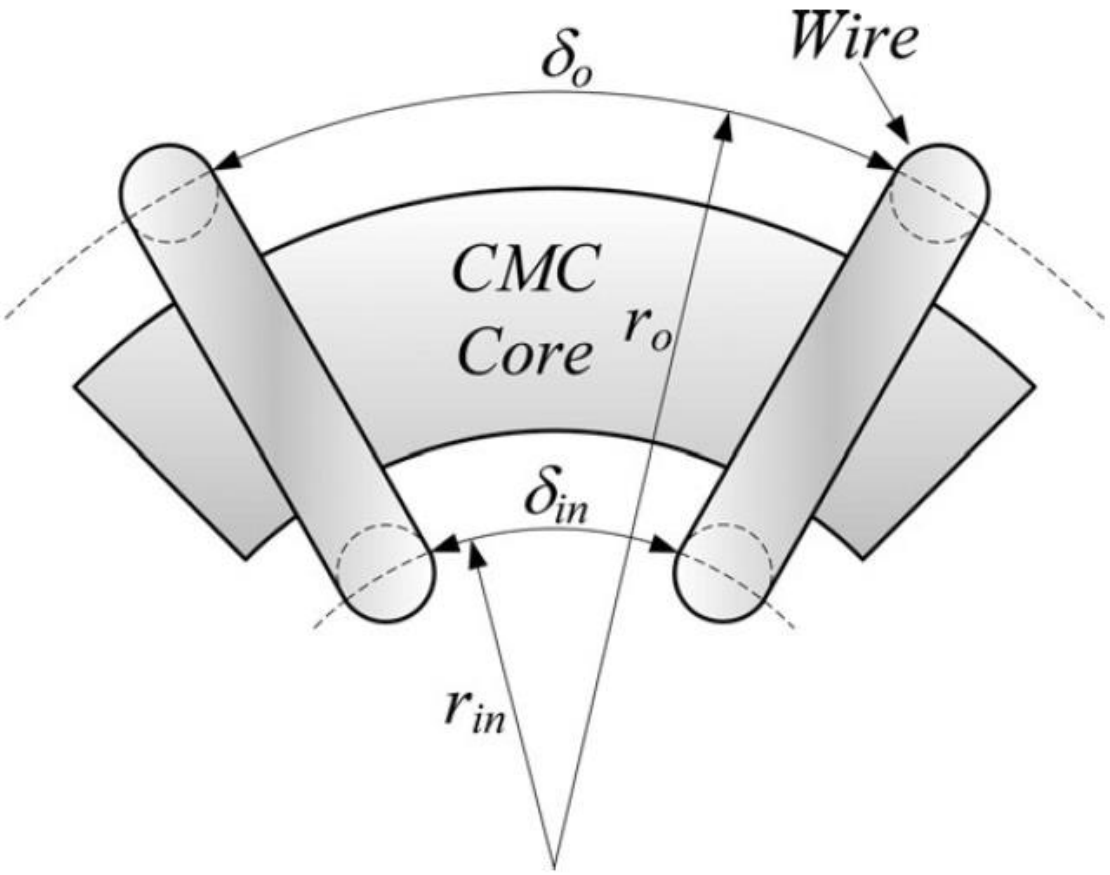


Figure 3.5: The electric field lines of lateral region.

between a turn and core of the inner region is represented by C_{tcin}. C_{tcin} can be determined as following.

$$C_{tcin} = \epsilon_o h_w \frac{d_w}{2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{d\theta}{\left(\theta \left[\delta_c + \left(\frac{d_w}{2}\right)(1-\cos\theta)\right] / \sin\theta\right) + \frac{w_{plin}}{\epsilon_{rpl}}} \tag{3.13}$$

where the width of the core plastic case for the inner region is w_{plin}. The relative permittivity of the plastic case is ϵ_{rpln}. Similarly, the capacitance between a turn and core for the outer region can be determined as followed.

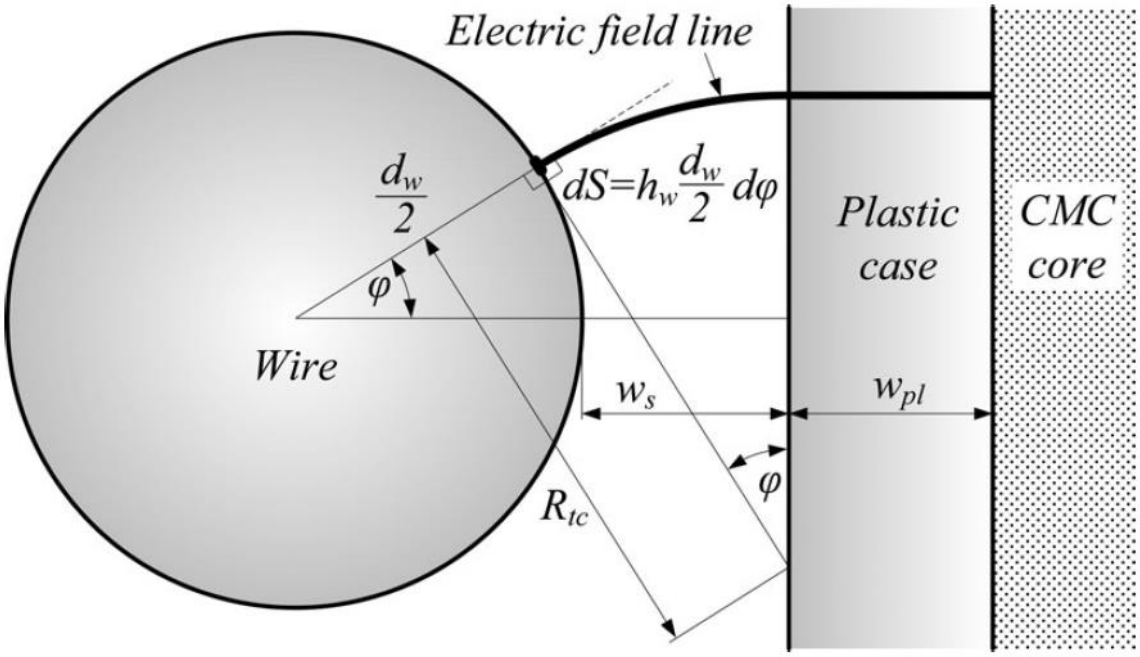


Figure 3.6: The electric field lines between turn and core.

$$C_{tco} = \epsilon_o h_w \frac{d_w}{2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{d\theta}{\left(\theta\left[w_s + \left(\frac{d_w}{2}\right)(1-\cos\theta)\right]/\sin\theta\right) + \frac{w_{plo}}{\epsilon_{rpl}}} \tag{3.14}$$

where the width of the core plastic case for the outer region is w_{plo}. For the lateral region, the capacitance between a turn and core can be determined as followed.

$$C_{tcl} = \epsilon_o (r_o - r_{in}) \frac{d_w}{2} \int_{-\frac{\pi}{2}}^{\frac{\pi}{2}} \frac{d\theta}{\left(\theta\left[w_s + \left(\frac{d_w}{2}\right)(1-\cos\theta)\right]/\sin\theta\right) + \frac{w_{pll}}{\epsilon_{rpl}}} \tag{3.15}$$

where the length of conductor h_w can be represented as the expression for the difference between r_o and r_{in}. The width of the core plastic case for the lateral region is w_{pll}. The total capacitance between a turn and core can be found as a sum of the turn to core capacitances in all regions.

$$C_{tc} = C_{tcin} + C_{tco} + 2C_{tcl} \tag{3.16}$$

3.2.1 Advantages and Disadvantages

Modeling the parasitic capacitance of common-mode choke of single-layer inductors with a magnetic core has several advantages as well as disadvantages. The following points represent the advantages of this method.

- This paper focuses on determining the parasitic capacitance of common-mode choke.
- The analytical method is applied for applications with high frequency.
- The model includes three different regions to calculate the capacitance between turns and between a turn and a core.
- The model depends on the electric filed lines in order to calculate the capacitance.
- The distance between turns and between a turn and a core can be applied in this model.

While there are advantages in this method, there are disadvantages as well. The following points summarize the drawbacks of this method.

- This method can not estimate the parasitic capacitance of applications with frequencies lower than the first resonant frequency.
- The complexity of this model is high.
- This model does not include the total capacitance of the winding.
- There is no relationship between the number of turns and the parasitic capacitance.

3.3 Modeling the Parasitic Capacitance by Using the Finite Element Method

A new model of the parasitic capacitance of inductors with high frequency applications is proposed in [22]. The purpose of this method is to calculate the capacitance between adjacent turns and nonadjacent turns. Figure 3.7 shows the lamped capacitance network of high frequency applications.

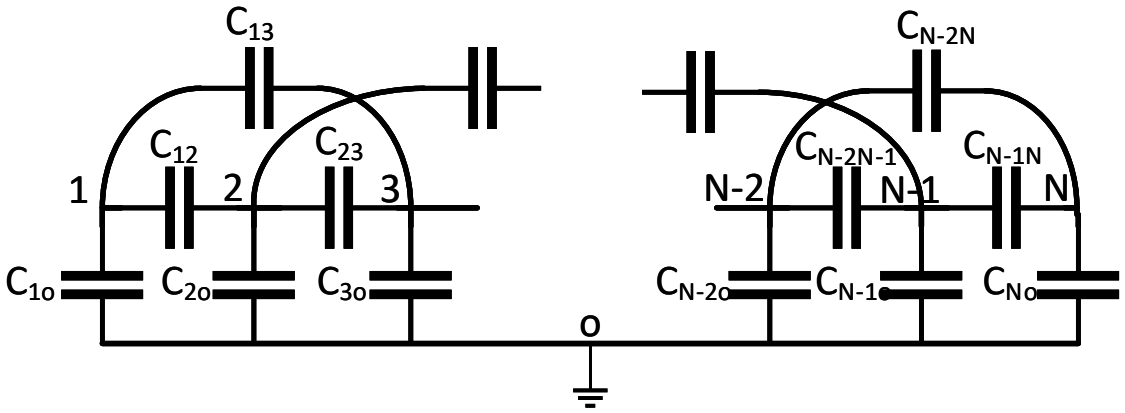


Figure 3.7: The lamped capacitance network.

The distributed capacitance of an inductor, which is shown in figure 3.7, presents node-to-node capacitance elements. Each node of the capacitance network represents a turn. The capacitance C_{ij} is the capacitance between the turns i and j, each are different than the other. The capacitance between the turn and the ground can be denoted by C_{io}. Each node has a voltage and a current. The node voltages, node currents, and node-to-node capacitance have a relationship. The relationship can be represented by a square admittance matrix, as shown next.

$$\begin{pmatrix} I_1 \\ I_2 \\ \vdots \\ I_N \end{pmatrix} = \begin{pmatrix} Y_{11} & Y_{12} & \dots & Y_{1N} \\ Y_{21} & Y_{22} & \dots & Y_{2N} \\ \vdots & \dots & \dots & \vdots \\ Y_{N1} & Y_{N2} & \dots & Y_{NN} \end{pmatrix} * \begin{pmatrix} V_1 \\ V_2 \\ \vdots \\ V_N \end{pmatrix} \tag{3.17}$$

where the current, voltage, and admittance can be represented by I_i, V_j, and Y_{ij}, respectively. (3.17) shows a general expression about the capacitive couplings among conductors. The parasitic

capacitance of an inductor can be determined by eliminating all intermediate nodes between its two terminals. The matrix in equation (3.17) is reduced to vectors and matrices as shown next.

$$\begin{aligned} \left(V_x\right) &= \begin{pmatrix} V_1 \\ V_x \end{pmatrix} \\ \left(V_y\right) &= \begin{pmatrix} V_2 \\ \vdots \\ V_{N-1} \end{pmatrix} \end{aligned} \tag{3.18}$$

where the node voltages can be divided to two vectors V_x and V_y. The node current, which are I_x and I_y, is represented by two vectors.

$$\begin{aligned} \left(I_x\right) &= \begin{pmatrix} I_1 \\ I_x \end{pmatrix} \\ \left(I_y\right) &= \begin{pmatrix} I_2 \\ \vdots \\ I_{N-1} \end{pmatrix} \end{aligned} \tag{3.19}$$

The admittance matrix is reduced to four different matrices. The reduction is based on the node place at the inductor.

$$
\begin{aligned}
\left(Y_{xx}\right) &= \begin{pmatrix} Y_{11} & Y_{1N} \\ Y_{N1} & Y_{NN} \end{pmatrix} \\
\left(Y_{xy}\right) &= \begin{pmatrix} Y_{12} & \dots & Y_{1N-1} \\ Y_{N2} & \dots & Y_{NN-1} \end{pmatrix} \\
\left(Y_{yx}\right) &= \begin{pmatrix} Y_{21} & Y_{2N} \\ \vdots & \vdots \\ Y_{N-11} & Y_{N-1N} \end{pmatrix} \\
\left(Y_{yy}\right) &= \begin{pmatrix} Y_{22} & \dots & Y_{2N-1} \\ \vdots & \vdots & \vdots \\ Y_{N-12} & \dots & Y_{N-1N-1} \end{pmatrix}
\end{aligned}
\tag{3.20}
$$

The nondiagonal admittance in the Y_x that is presented in (3.21) is equal to $-j\omega C_{1N}$.

$$
Y_x = Y_{xx} - Y_{xy} Y_{yy}^{-1} Y_{yx} \tag{3.21}
$$

Therefore, by assuming $I_y = 0$, the voltage vectors can be determined. Hence, the lumped parasitic capacitance of the inductor can be estimated easily.

3.3.1 Advantages and Disadvantages

The new model of determining the parasitic capacitance of single-layer inductors with a magnetic core has several advantages as well as disadvantages. The following points represent the advantages of this method.

- This paper focuses on determining the parasitic capacitance of inductors with radio frequency circuit.
- The analytical method is applied for applications with high frequency.
- The model is verified by a 2D electrostatic model with finite element method.

- The model includes adjacent and nonadjacent turns capacitance.

While there are advantages in this method, there are disadvantages as well. The following points summarize the drawbacks of this method.

- This method can not estimate the parasitic capacitance of applications with frequencies lower than first resonant frequency.
- The method of using this model is complex.
- There is no relationship between the number of turns and the parasitic capacitance.

CHAPTER 4

MODELING THE PARASITIC CAPACITANCE OF MAGNETIC COMPONENTS

4.1 Introduction

Magnetic components such as inductors, interleave coupled inductors, and transformers are important parts of electric and electronic systems [20]. Magnetic components have inherent parasitics that affect their performance when frequency increases. In fact, the parasitic elements of magnetic components can play a significant role on the modern electrical system. The magnetic components have two types of parasitics which are resistance and capacitance parasitics. The winding resistance and core losses constitute the parasitic resistance while the parasitic capacitance is caused by the inter-turn, inter-layer, and winding-to-core capacitances. [11, 17, 26, 43]. The parasitic elements of an inductor can be represented by the models as shown in figure 4.1. The commonly adopted model in figure 4.1(a) consists of the parasitic resistance R_s is in series with inductance while the parasitic capacitance C_p is in parallel with the series connected R_s and L. Figure 4.1(b) represents an inductor model with parallel parasitic resistance R_p and parallel parasitic capacitance [12, 27, 32, 43, 45].

The impedance of an inductor increases when the frequency increases. Because of the recent development of switching frequency, the efficiency of power electronics applications can be affected and reduced based on the range of frequency [16, 43]. Figure 4.2 shows the characteristic of the inductor impedance when the frequency increases. The frequencies range of an inductor in power electronics applications can be divided into three categories: low frequency range in which the parasitic capacitance does not affect the inductor behavior, medium frequency range when the characteristic of an inductor start to be affected by frequency which appears below first resonant frequency, and high frequency range which is the range of frequencies above the first resonant frequency such as radio frequency and EMI filter applications.

The parasitic capacitance over medium frequency range is different than the parasitic capacitance

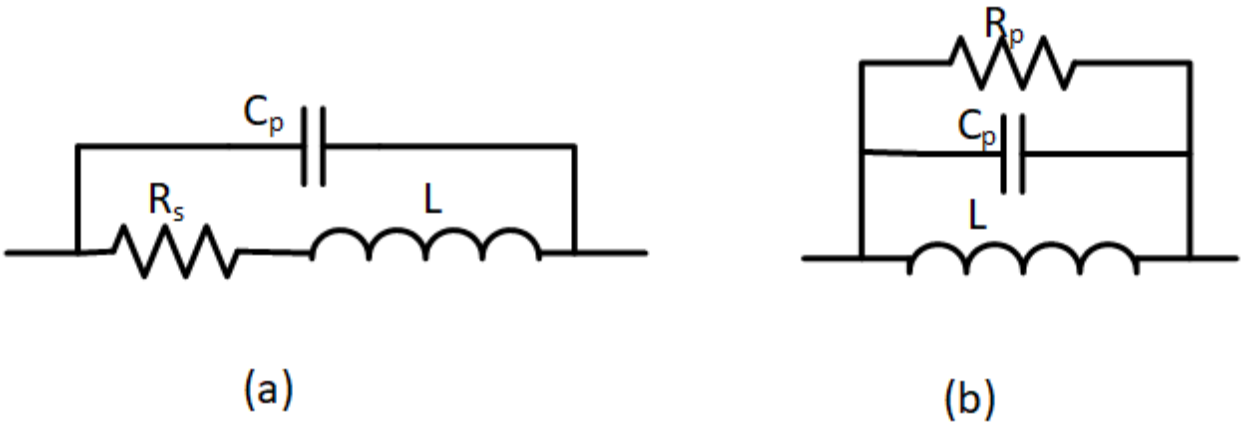


Figure 4.1: Models of an inductor.

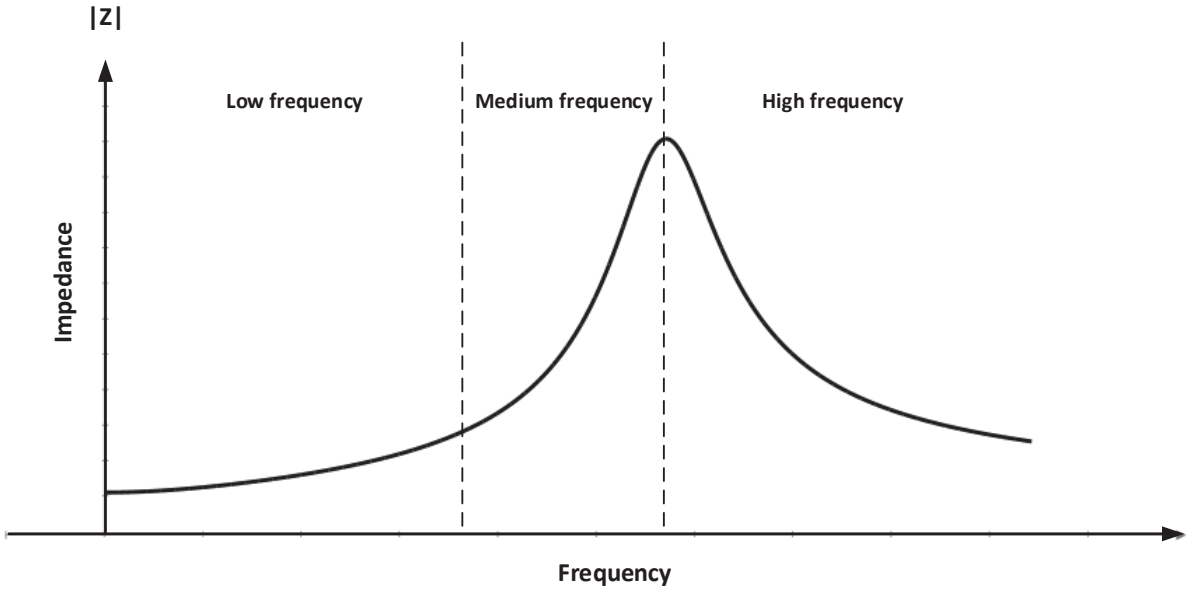


Figure 4.2: Characteristic impedance of an inductor with parasitic capacitance included in the model.

over high frequency range [13,43]. Most of the parasitic capacitance models over medium frequency range are developed for high frequency transformer applications [18]. However, there is no model of calculating the single layer inductor in medium range frequency for power electronic converters.

For single-layer inductor, there are a couple of models to calculate the parasitic capacitance for high frequency applications [12, 29, 43]. Most of these models are applied with air-core inductor in order to use them with frequencies above $1MHz$ [13, 19, 43, 45] such as EMI filter, EMC filter, and radio frequency applications.

It is essential to have accurate and simple analytical method to calculate the total parasitic capacitance for medium frequency range that can be applied to magnetic components such as inductors. Inductors can be applied as filter or energy storage for converters like a boost converter in medium frequency range.

This paper introduces a new approach to estimating the total parasitic capacitance of an inductor of a single-layer with a magnetic core in medium frequency range. This model can determine the parasitic capacitance based on the geometry of an inductor core and the approximated shape of the conductor.

In order to verify the analytical method of calculating the parasitic capacitance, two different techniques have been applied. The first technique is to test the inductor with various frequencies speed such as using network analyzer [18, 21]. The other technique is to apply the finite element analysis (FEA), which is considered to be of higher accuracy than analytical models [18, 21, 22].

The FEA simulation have two models with different accuracy that can determine the parasitic capacitance. The models of FEA simulation are two-dimensional (2-D) model which considers to be lower accuracy than three-dimensional (3-D) model of simulation [21, 22]. For more complex geometry and multiple layers, the analytical model is proved to be time efficient and more convenient for the model-based design [21].

The rest of the chapter is divided as follows. The approximation model of conductor is presented in subsection 4.2.1. In subsection 4.2.2, the analytical method of modeling the parasitic capacitance of single-layer inductor with a magnetic core is explained. The results and discussion are introduced

in section 4.3. Finally, the conclusion of the new approach of modeling the parasitic capacitance is shown in section 4.4.

4.2 Methodology of Modeling Inductors

Magnetic components contain two main parts that are magnetic core and winding conductor. For modeling the parasitic capacitance of magnetic components, the geometry of magnetic core, conductor, and the distance between them should be considered. For the trade-off between accuracy and simplicity, the conductor can be modeled in approximated shape as explained it in the subsequent text.

The magnetic core material should be chosen based on frequency and losses in the material. The magnetic core has many different shape that can be selected based on the power and magnetic flux needed. For instance, E-I & U-I shapes are used for interleaved coupled inductors, transformers, and single-phase and multi-phase inductors [4, 6, 16, 34].

4.2.1 Modeling the conductor

Modeling the parasitic capacitance of magnetic components has been one of the technically challenging topics for decades. Significant research effort has been invested in modeling the parasitic capacitance for different magnetic components geometries [16, 21, 43]. Most of the previous work on modeling the parasitic capacitance of inductors are aimed for applications with very high frequencies. Some of these models are only applicable for air-core inductors [13, 19]. There exist very few models that consider the magnetic core for calculating the parasitic capacitance of single-layer inductors. The existing models work only in very high frequencies such as EMI, and EMC filters [13, 17, 43]. Another model type of parasitic capacitance for magnetic components is aimed for transformers [18, 46]. This type of model is focused on the frequencies below first resonant frequency [16, 18]. However, most of these models are less accurate compared with 3-D electrostatic model simulations and still complex to calculate the parasitic capacitance.

In order to achieve a model that strikes a balance between accuracy and complexity in esti-

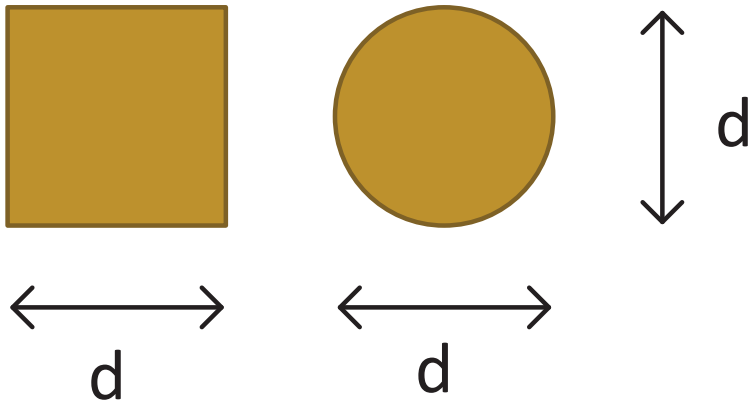


Figure 4.3: Approximation shape of rod conductor.

mating the parasitic capacitance, the approximation of conductor shape is proposed. The close approximation of rod wire conductor with a square shape can simplify the analytical calculation of parasitic capacitance. Figure 4.3 shows the approximation of rod conductor with a square shape. This approximation is applied to model and calculate the parasitic capacitance of inductors with a single-layer for power converters. Without loss of generality, the magnetic U-I core is selected in this study. Figure 4.4 shows the approximation model of single-layer inductor with magnetic U core.

The results based on this approximation method show improved accuracy as compared with other models of single-layer inductor with magnetic core such as in [43]. The percentage of error between FEA simulations such as 3D electrostatic and Q3D extractor models and the proposed analytical model is less than 8%. Moreover, the proposed model has many advantages over the model in [17, 43] such as including the distance between turn to turn, turn to core, and turn to side limb of magnetic core.

The process of calculating the parasitic capacitance for a single-layer inductor with magnetic core is presented in the following section.

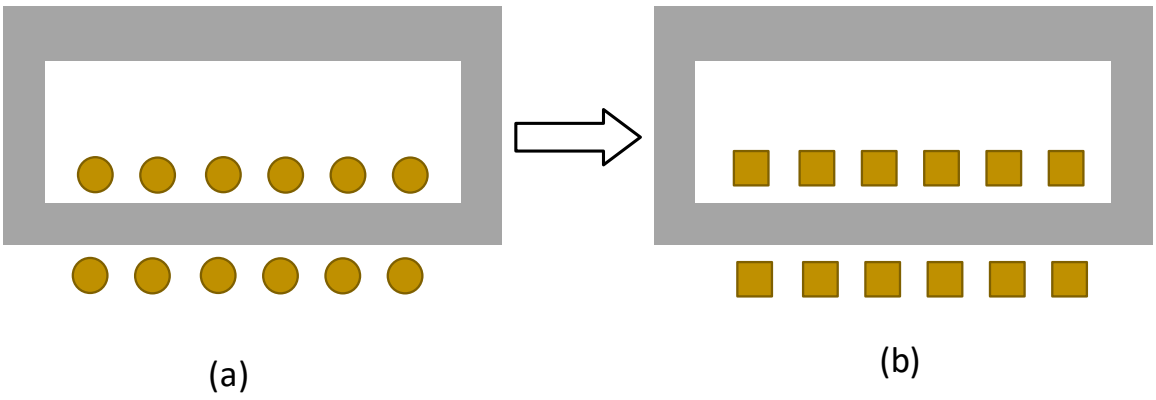


Figure 4.4: U-I core with approximation shape of rod conductor.

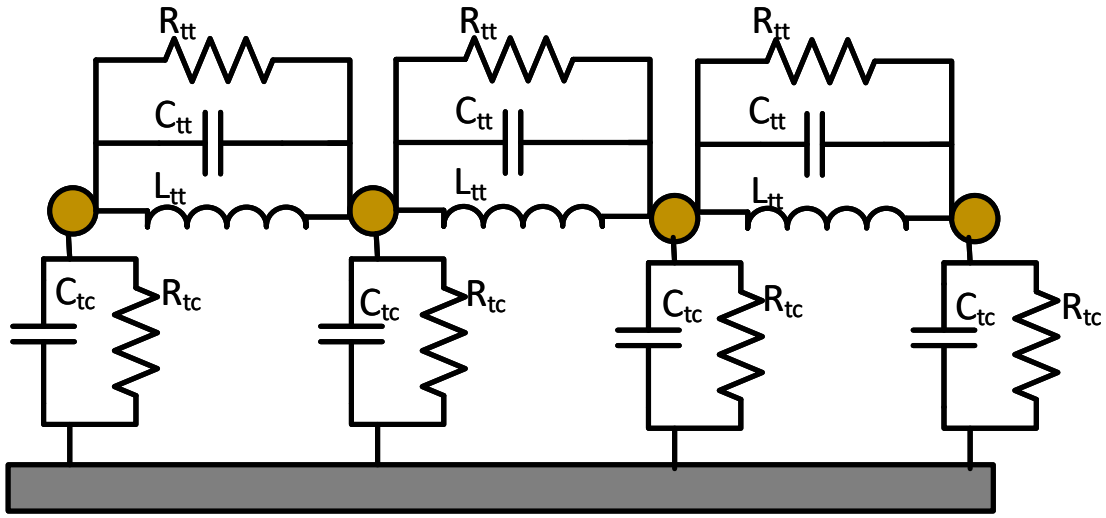


Figure 4.5: High frequency circuit of an inductor with magnetic core.

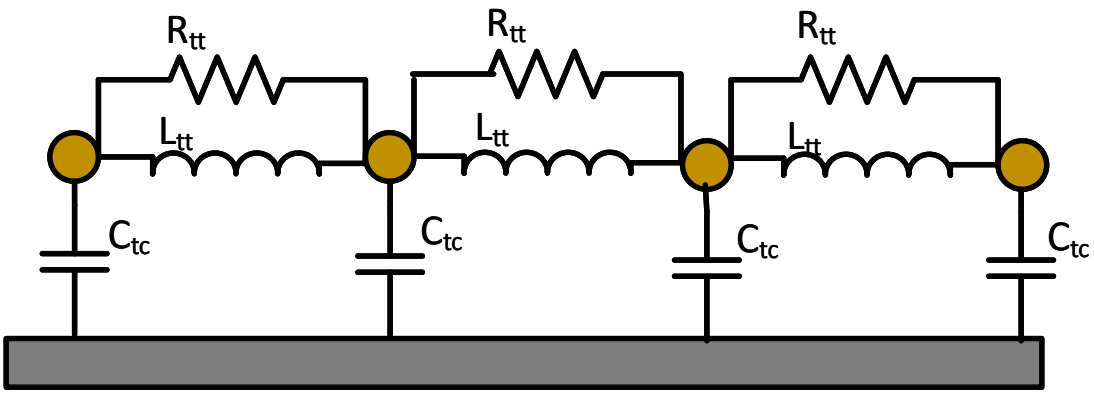


Figure 4.6: Simplified high frequency circuit of an inductor with magnetic core.

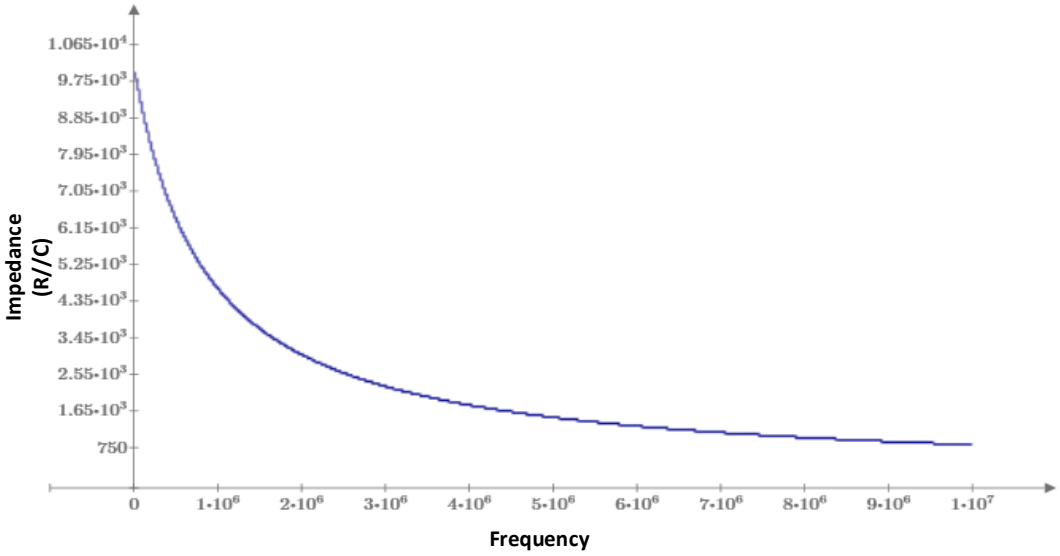


Figure 4.7: Curve of impedance versus frequency.

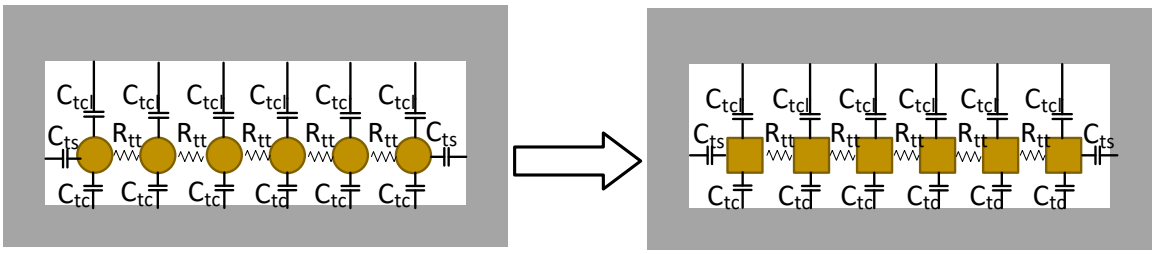


Figure 4.8: The parasitic capacitance model of U-I core.

4.2.2 Modeling inductors with single-layer

To achieve the best approximate result of parasitic capacitance, the overall parasitic capacitance including the parasitic capacitances between winding and core limbs should be considered. Figure 4.5 shows the parasitic network of an inductor for frequencies below than first resonant frequency [13, 19, 43]. The model in figure 4.5 is applicable for power converters in medium frequency range [16,18]. For high frequency applications such as EMI filter, RF circuit, and EMC applications the parasitic resistance and impedance of the branches are much higher than the reactance of shunt capacitance, which leads to neglect the inductances and parasitic resistance between turns within the same layer i.e. the parasitic resistance of turn-to-turn and turn-to-core can be treated as open circuit [13,43]. However, in frequencies below first resonant frequency, parasitic resistance of turn to turn R_{tt} should be considered. In fact, the resistance R_{tt} dominates the turn to turn parasitic capacitance C_{tt} in the medium frequency range as shown in figure4.7 where the resonant frequency is $< 1MHz$ for medium power applications. The turn to core parasitic resistance R_{tc}, which is located between wire and core, includes dielectric material. Therefore, R_{tc} is very large resistance as explained in [12, 27, 45] which acts as open circuit. Hence, The parasitic capacitance between turn and core C_{ct} should be considered. The simplified model of the inductor in medium frequency range is shown in figure 4.6.

Based on the previous simplified model, the parasitic capacitance of an inductor with U-core shape has been derived. The square shape of wire is applied as shown in figure 4.4. The variables of the approximation can be taken from the rod wire as follows

$$W = d \tag{4.1}$$

$$L_{totaln} = L_{bottom} + L_{innern} + L_{fron} + L_{back} \tag{4.2}$$

$$L_{back} = \sqrt{L_{fron}^2 + d_{tt}^2} \tag{4.3}$$

$$L_{outern} = L_{bottom} + L_{fron} + L_{back} \tag{4.4}$$

$$L_{total} = N * L_{totaln} \tag{4.5}$$

The width of square wire W can be selected from diameter d of the rod wire where W is the conductive part of wire with excluding coating and insulation parts. The length of a single turn is L_{totaln}. L_{innern} is the inner segment length of a turn while L_{outern} is the total of three outer segments of a turn. The length of a conductor L_{total} can be determined by multiplying the single turn length by number of turns N. Each turn of the inductor with U core has four different distances. The distances between turn and turn, turn and central limb, and turn and far limb are d_{tt}, d_{tl}, and d_{tcl}, respectively. Assume that d_{ts}, which is the distance of the side turn to side core, is equal to d_{tt}. which can be determined as follows.

$$d_{tt} = \frac{E - (W * N)}{1 + N} \tag{4.6}$$

where E is the length of center limb that is occupied by the winding. Each parasitic capacitance of the inductor can be determined separately. In the following analysis, parasitic capacitance of each element is presented.

$$A_{tt} = W * L_{totaln} \tag{4.7}$$

$$C_{tt} = \varepsilon \frac{A_{tt}}{d_{tt}} \tag{4.8}$$

$$\varepsilon = \varepsilon_r \varepsilon_o \tag{4.9}$$

where A_{tt} is the cross-sectional area of turn to turn capacitance while ε is the permittivity of dielectric. ε_r and ε_o are relative dielectric permittivity and dielectric permittivity of vacuum, respectively. C_{tt} is the capacitance between two turns.

$$A_{wside} = W * L_{totaln} \tag{4.10}$$

$$W_{cside} = 2\frac{d_{tt}}{2} + W \tag{4.11}$$

$$L_{cside} = 2L_{tside} + L_{bside} + \sqrt{L_{bside}^2 + d_{tt}^2} \tag{4.12}$$

when the distance increases between winding and central limb, the parasitic capacitance changes. Therefore, the average area and distance between winding and core are considered. The width of the electric field on the core is denoted by W_{cside}. L_{cside} represents the length of electric field on the core.

$$A_{cside} = W_{cside} * L_{cside} \tag{4.13}$$

$$A_{tl} = \frac{A_{wside} + A_{cside}}{2} \tag{4.14}$$

$$C_{tl} = \epsilon \frac{A_{tl}}{d_{tl}} \tag{4.15}$$

$$A_{tcs} = W * L_{innern} \tag{4.16}$$

$$C_{tcl} = \epsilon \frac{A_{tcs}}{d_{tcl}} \tag{4.17}$$

$$C_{ts} = \epsilon \frac{A_{tcs}}{d_{ts}} \tag{4.18}$$

where A_{tl} is the average area between turn to core while A_{wside} is the area of conductor. A_{cside} is the area that covers the electric field of the wire on the core and it is assumed to be uniform among all the turns. The average area is related to the distance between turns. The area of the parasitic capacitance between a turn and far limb is denoted by A_{tcs} as well as the area between the side turn and a side limb. The parasitic capacitance of turn to central limb is denoted by C_{tl} while capacitance between turn to far limb and capacitance between turn and side limb are C_{tcl} and C_{ts}, respectively. Figure 4.8 shows the represented capacitances of each turn for U-I core inductor.

To determine the total parasitic capacitance, the capacitances between turn and core limbs should be calculated in parallel. Each turn has dielectric and wire resistance which is represented as R_{tt}. Because of the RC model, which is the resistance in parallel with the capacitance, the resistance R_{tt} dominates the turn to turn capacitance C_{tt} for frequencies below the first resonant frequency. The focus of this paper is to improve the analytical mode of inductors at frequencies below first resonant frequency. The first resonant frequency usually is between several hundreds kHz up to MHz for medium power applications [16,18,43] . Also, many references are neglecting turn to turn capacitance such as [18, 46] which are applied for high-frequency transformer applications. For parasitic capacitance in high frequency transformer applications, the energy storage between turns of same layer is very small compared to energy storage between layers as explained in [16, 18, 46]. Since the parallel resistance dominates the capacitance in medium frequency range, the electric field strength is reduced between the turns of same layer. Moreover, the turn to turn are connected physically which makes the effects of turn to turn capacitance are very small and the turn to turn can be treated as short circuit. In this paper, the parasitic capacitance between turns is neglected in the overall parasitic capacitance calculation.

The total capacitance can be determined by excluding the insulation part between turns. So, the total capacitance between turns to central limb C_{tlTot}, the total capacitance between turns and far limb C_{tclTot}, and the total capacitance of side limbs C_{tsTot} are explained as follows

$$C_{tlTot} = N * C_{tl} \tag{4.19}$$

$$C_{tclTot} = N * C_{tcl} \tag{4.20}$$

$$C_{tsTot} = 2 * C_{ts} \tag{4.21}$$

$$C_{Tot} = C_{tlTot} + C_{tclTot} + C_{tsTot} \tag{4.22}$$

The total parasitic capacitance of the inductor can be determined as (9.25) where C_{Tol} is the total capacitance that determines all capacitances in parallel. The assumption of side limbs capacitances are applied when the distance between turn and limbs of two sides are equal. The assumption is satisfied and shows good results compared with FEA. The error percentage of the proposed model is $\leq$ 8% difference between 3D electrostatic simulation model and the analytical model. This model shows that there is a relationship between the parasitic capacitance with the number of turns of a single layer. By increasing the number of turns of an inductor, the total parasitic capacitance of the inductor is increased as explained in [12, 41]. This model shows higher accuracy and less complexity than other methods such as in [43]. In [43] the parasitic capacitance is approximated with multiplying the turn-to-turn capacitance by a factor. The parasitic capacitance has same value for any number of turns that is more than 10 turns. However, the parasitic capacitance has direct relationship with the number of turns in the proposed model. The total parasitic capacitance can be rewrite as follows

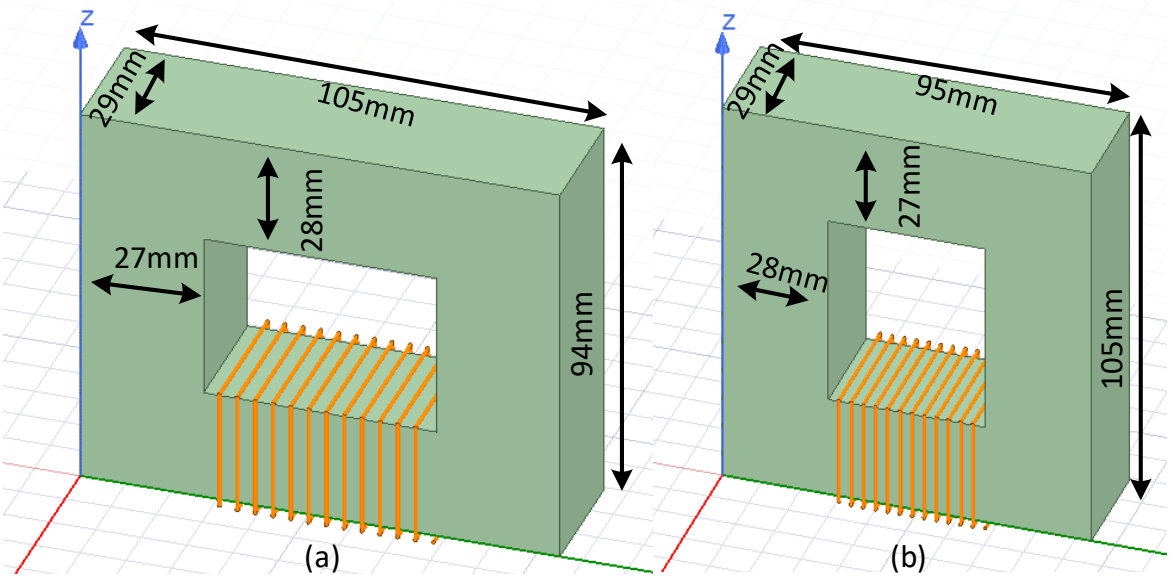


Figure 4.9: Dimension of two geometries.

$$\begin{aligned} C_{Tot} &= C_{tlTot} + C_{tclTot} + C_{tsTot} \\ &= N * (C_{tl} + C_{tcl}) + C_{tsTot} \end{aligned} \tag{4.23}$$

4.3 FEA and Experimental Results

In this section, the given results from the analytical method are compared with four different geometries of magnetic core that two of them have same inductance. Maxwell ANSYS software with 3-D electrostatic model is applied to extract the parasitic capacitance. Figure 4.9 shows that the two geometries of the inductor where the central limb of winding in figure 4.9(a) has longer length than in figure 4.9(b). The geometry of inductor in figure 4.9(b) has higher distance between a layer and the far limb than the geometry of inductor in figure 4.9(a).

The dimensions of both geometries as shown in figure 4.9 are as follows: Figure 4.9(a) the length and area of central limb are $51mm$ and $812mm$, respectively, and the distance between central limb and far limb is $38mm$. The geometry of inductor in figure 4.9 (b) are $39mm$ for the length of central limb while the area is $783mm$, and the distance between central limb and far limb is $51mm$.

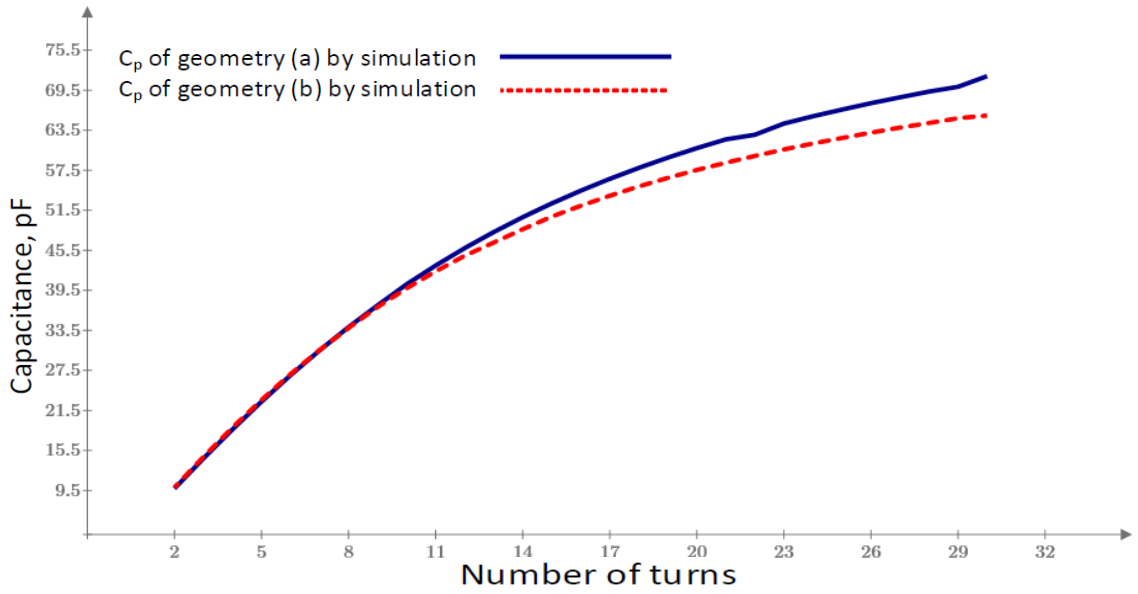


Figure 4.10: Parasitic capacitance versus number of turns by Electrostatic simulation.

The experiment is applied with different number of turns for both geometries to compare between the parasitic capacitance of two different geometries. Since both of the geometries have same inductance, the analytical proposed are compared with the simulation model. The range of number of turns are from 2 to 24 turns with a conductor diameter is $1mm$.

Figure 4.10 shows the parasitic capacitance curves of both geometries versus number of turns. The curves of both results explain that the parasitic capacitance is related to the number of turns i.e. when the number of turns increases, the parasitic capacitance increases. As a result, the parasitic capacitance of geometry in figure 4.9(a) has the large capacitance. Since the geometry in figure 4.9(a) has longer length of central limb, the conductor length of winding is higher as compared with geometry in figure 4.9(b). Therefore, the parasitic capacitance of geometry in figure 4.9(a) is higher. Beside the increasing in the parasitic capacitance, the conductor losses are increased. Hence, the shorter distance between turns has less conductor losses and less parasitic capacitance.

To verify the analytical approach, the comparison between simulation results and analytical results are shown in figure 4.11. Four curves are shown in figure 4.11 that are analytical results of both geometries and 3-D electrostatic results of both geometries versus number of turns. The curves

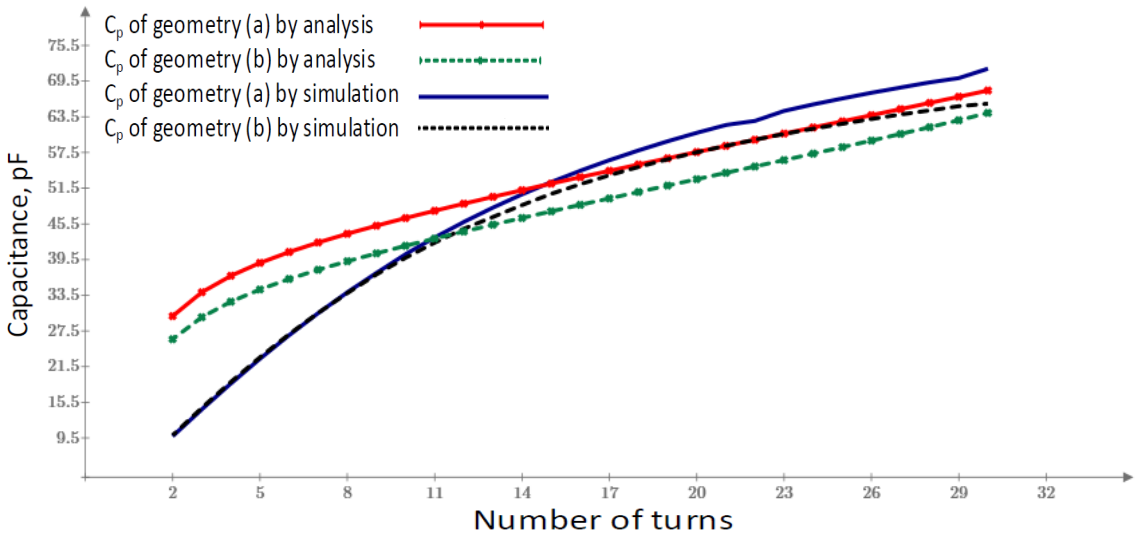


Figure 4.11: Parasitic capacitance versus number of turns by electrostatic simulation and analytical model.

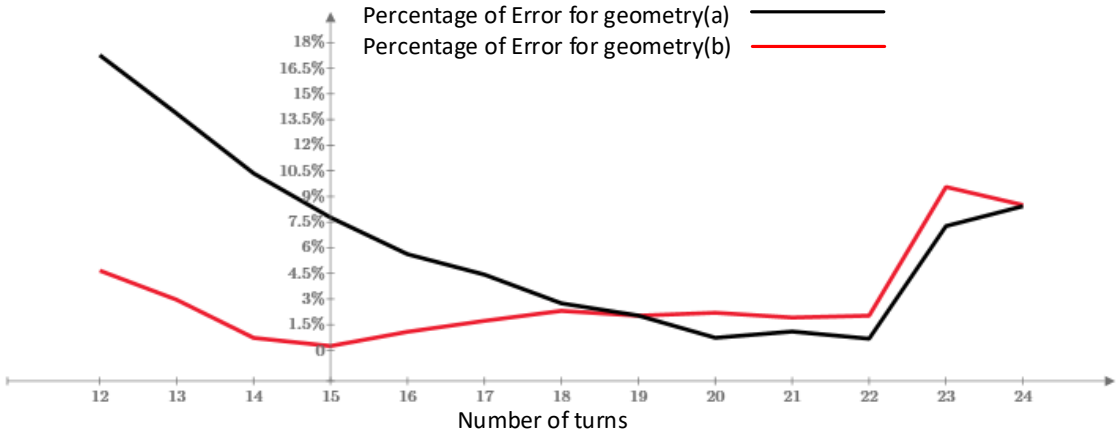


Figure 4.12: Percentage of error of two geometries.

show that the percentage of error between simulation and analytical results is less than 8% when the number of turns fill more than half of central limb area as shown in figure 4.12. The reason of difference in the percentage error that the analytical approach does not include the fringing effect while 3-D electrostatic ANSYS software includes the fringing effect as shown in figure 4.16. In order to make the simulation results close to real situation, the area of region that includes the geometries are larger than the geometries area by 30% on all the directions.

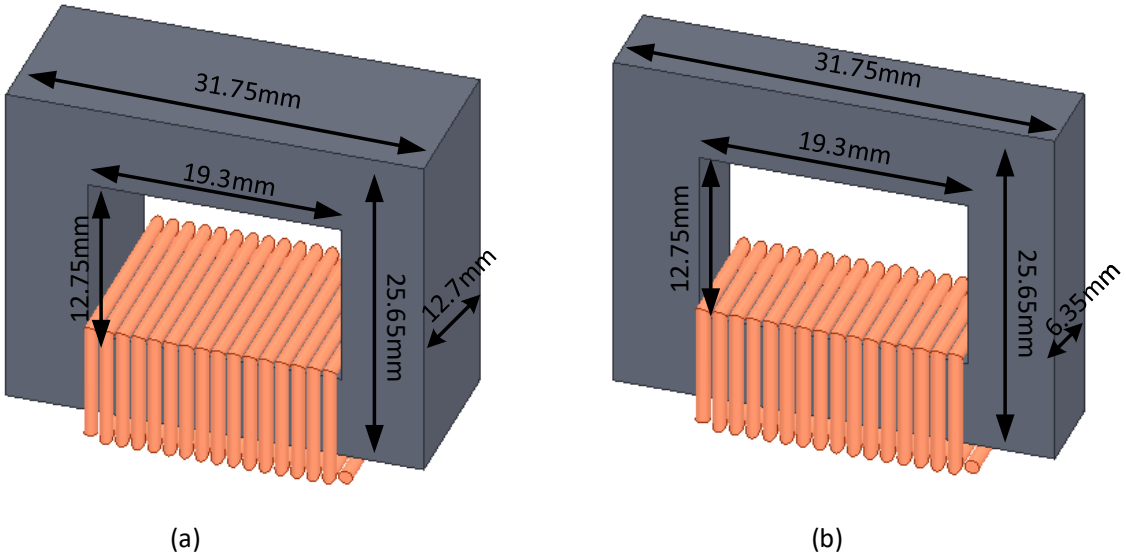


Figure 4.13: Dimension of two different inductors with same size but different volume.

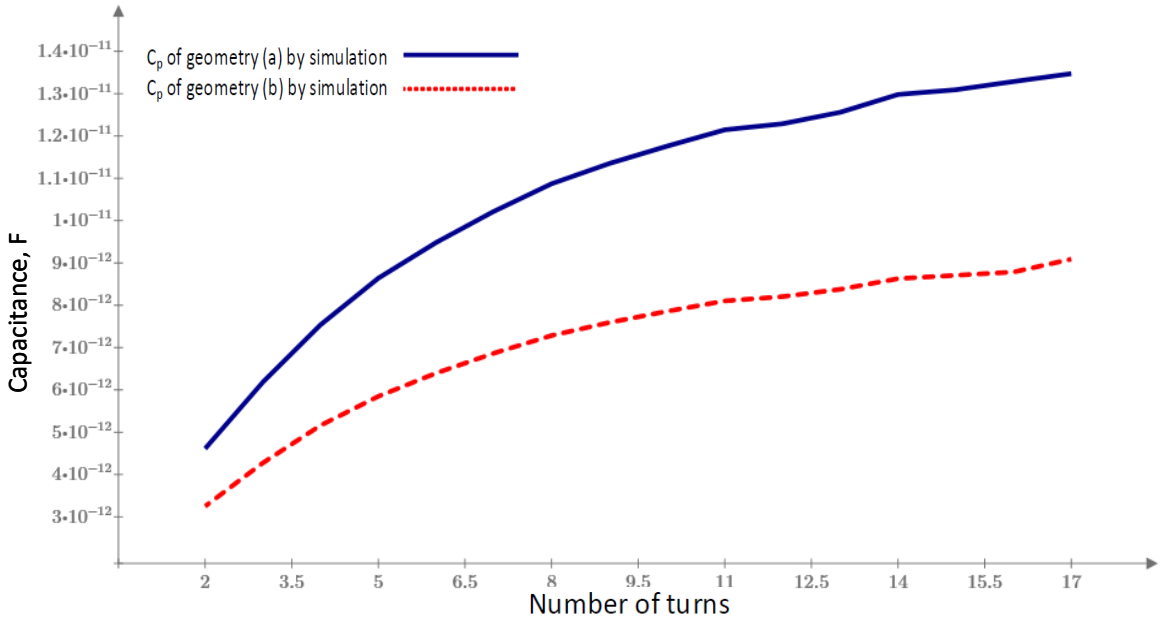


Figure 4.14: Parasitic capacitance versus number of turns by Electrostatic simulation.

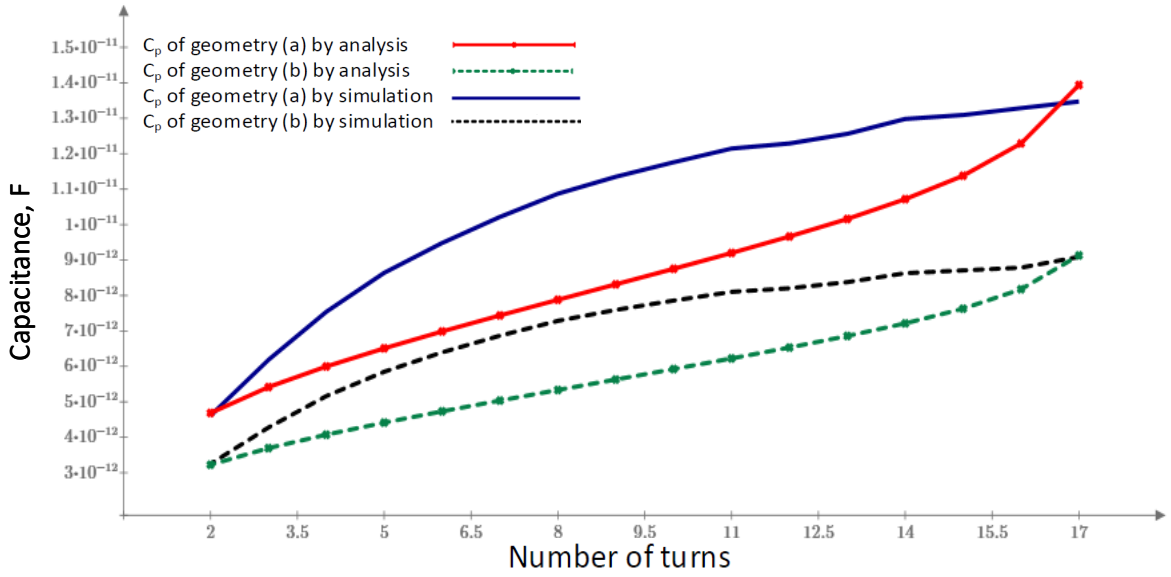


Figure 4.15: Parasitic capacitance versus number of turns by electrostatic simulation and analytical model.

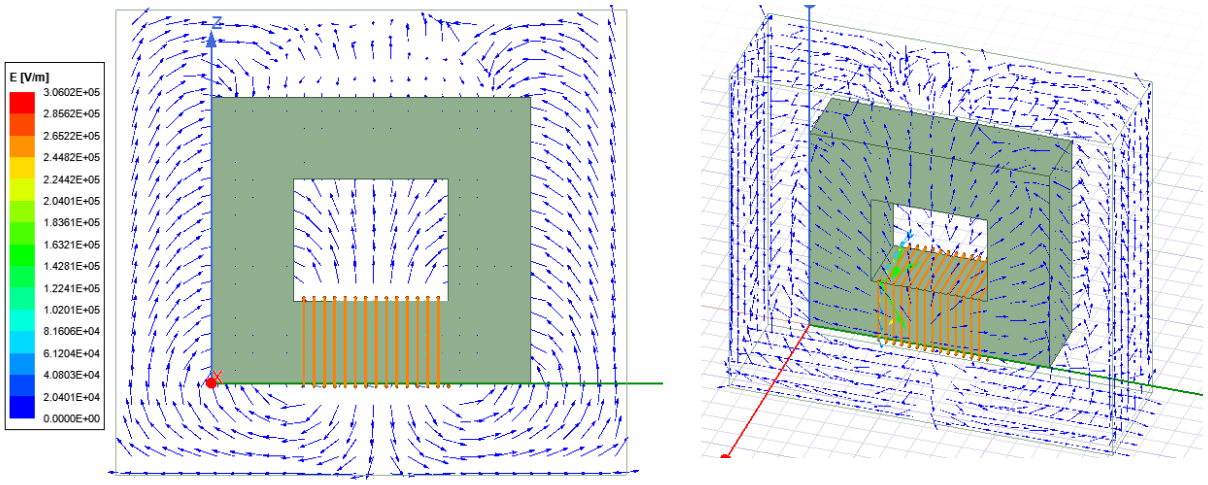


Figure 4.16: Electric field and fringing effects in ANSYS maxwell software.

On the other hand, two different volumes of the UI geometry applied in order to extract the parasitic capacitance. The distance between winding and magnetic core limbs plays an important role on the parasitic capacitance. Figure 4.13 shows two inductors with different volume. Figure 4.13 (a) has a double width size than inductor in figure 4.13 (b). The comparison between the two different inductors with same size but different volume are applied to extract the capacitance with different number of turns. Figure 4.14 shows the parasitic capacitances versus the number of turns of two different inductors which are in Figure 4.13. The results explain that the inductor with higher volume has higher parasitic capacitance than the inductor with smaller volume.

Figure 4.15 depicts the comparison between the analytical results and the simulation results for two different inductor with same size and different volume. As shown in the results that the analytical and simulation results of the inductor with higher volume have more parasitic capacitance than the inductor with lower volume. The reason of that the parasitic capacitances between winding and core limbs increase with increasing the depth of the volume.

The electric field of parasitic capacitance of the inductor is very high between turn and magnetic core compared with electric field between turns of a layer as shown in figure 4.17. Figure 4.17 depicts the electric field of a single layer inductor with magnetic core. Hence, the parasitic capacitance between turn to turn can be ignored.

The comparison between two geometries are applied. Therefore, It is important to compare between the percentage of error (P.E.) when the central limb are fully wounded and half wounded. Figure 4.18 shows the P.E. of geometry with longer length of central limb. This results present the highest P.E. that is 5.6%. The P.E. of the geometry with shorter length of central limb is shown in figure 4.19 where the highest P.E. is 7.5%.

The inductor in figure4.13 (a) with AWG 18 conductor is tested with 8 turns by using Network Analyzer as shown in figure 4.20. Figure 4.21 presents experimental, simulation, and analytical results. The P.E. between the parasitic capacitance of analytical model C_{pa} and the parasitic capacitance of the experiment C_{px} is 14.46% while P.F. between C_{pa} and the simulation result C_{ps} is 9.02%. The parasitic capacitance of the experiment result is the average value of the

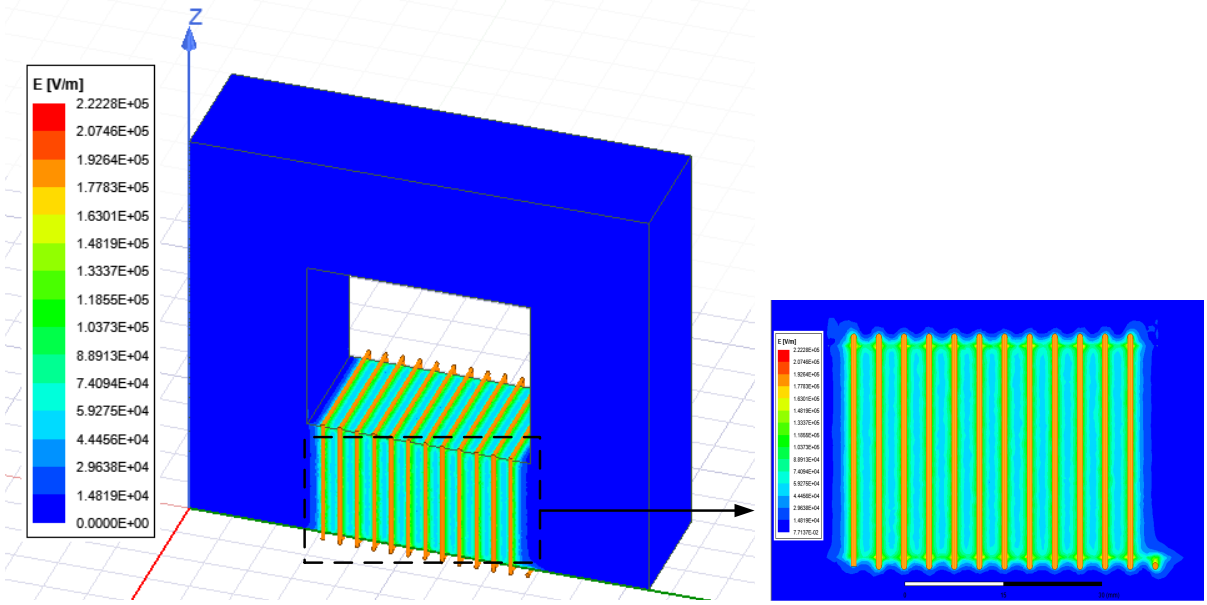


Figure 4.17: Electric field of a single layer inductor with magnetic core.

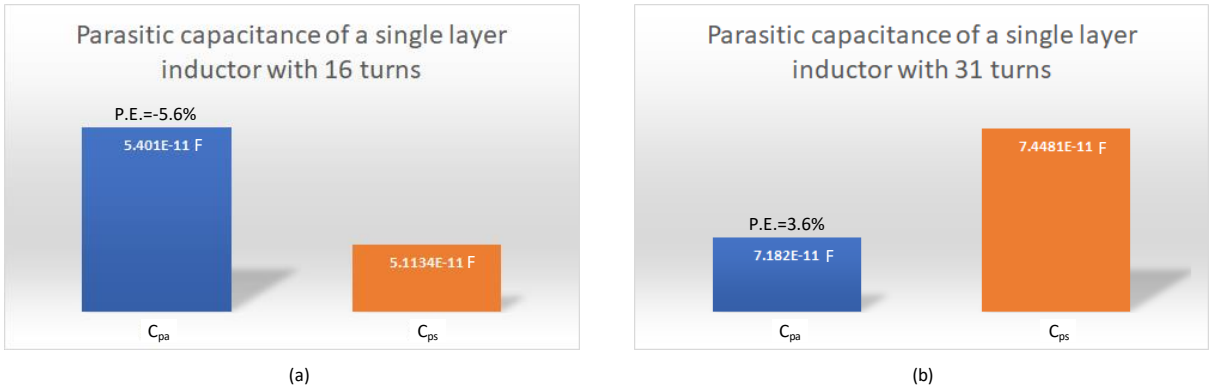


Figure 4.18: Comparison of geometry with long central limb.

parasitic capacitances at five different frequencies over the resonant frequency. The average parasitic capacitance is 20.81 pF while the parasitic capacitances at different frequencies are $20.209pF$, $19.888pF$, $22.493pF$, $22.973pF$, and $18.462pF$. However, the frequency increases, the inductance of the magnetic core material is changed. The reason of changing the inductance is that the impedance of magnetic component depends on the permeability where the permeability depends on the frequency of the magnetic core material.

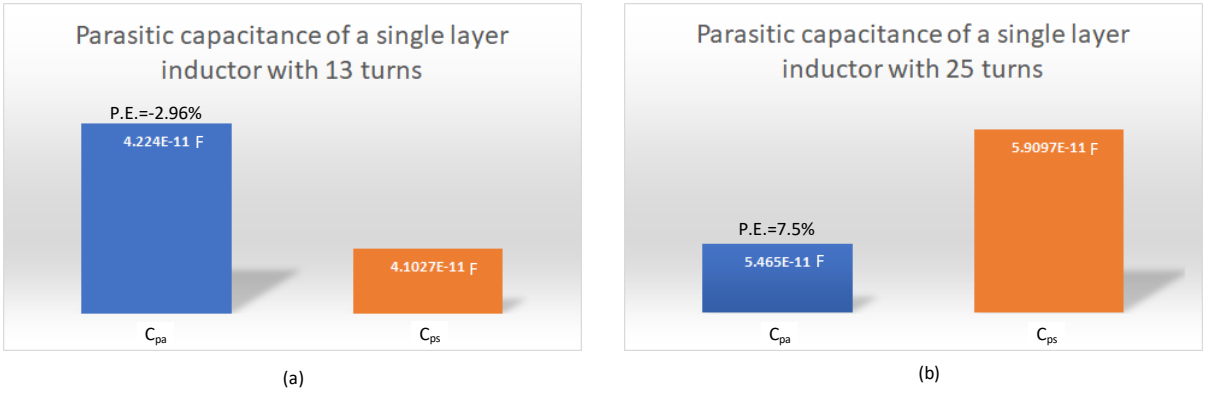


Figure 4.19: Comparison of geometry with short central limb.

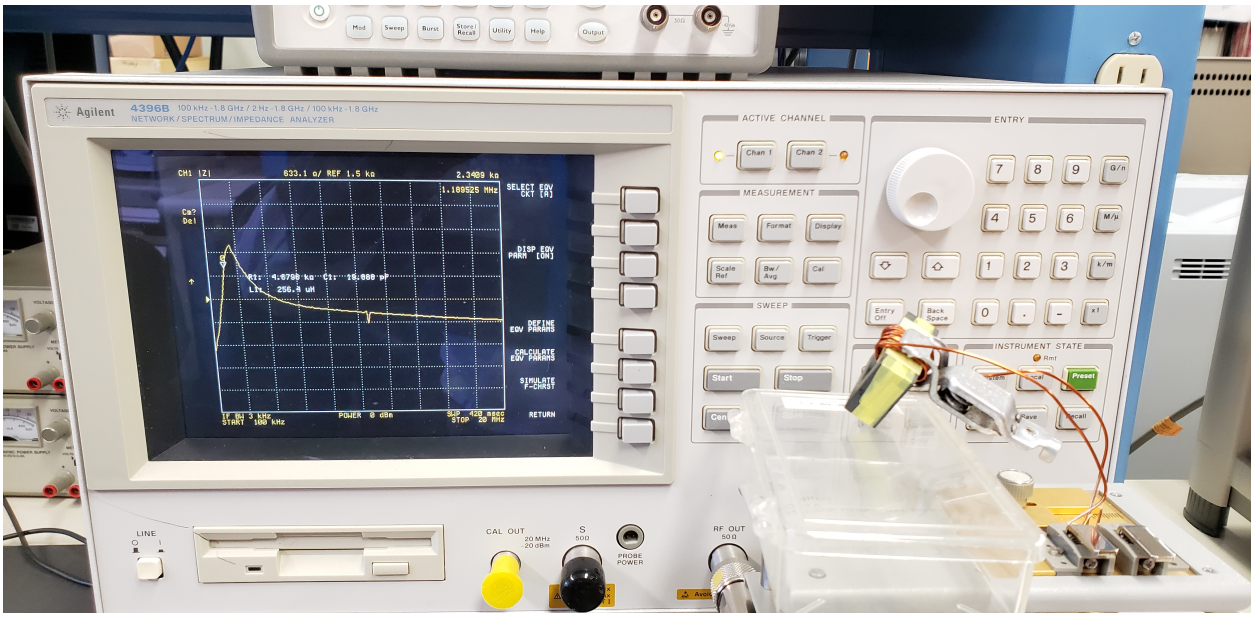


Figure 4.20: Impedance Network Analyzer device.

4.4 Conclusion

A new approach of determining the total parasitic capacitance of a single-layer inductor with magnetic core has been proposed in this paper. The analytical approach has been derived based on the physical structure of the magnetic components. The approximation of rod conductor has been presented. The total parasitic capacitance of a single-layer inductor with magnetic core in medium frequency range increases with increasing the number of turns.

The proposed model is appropriate for estimating the parasitic capacitance of medium power

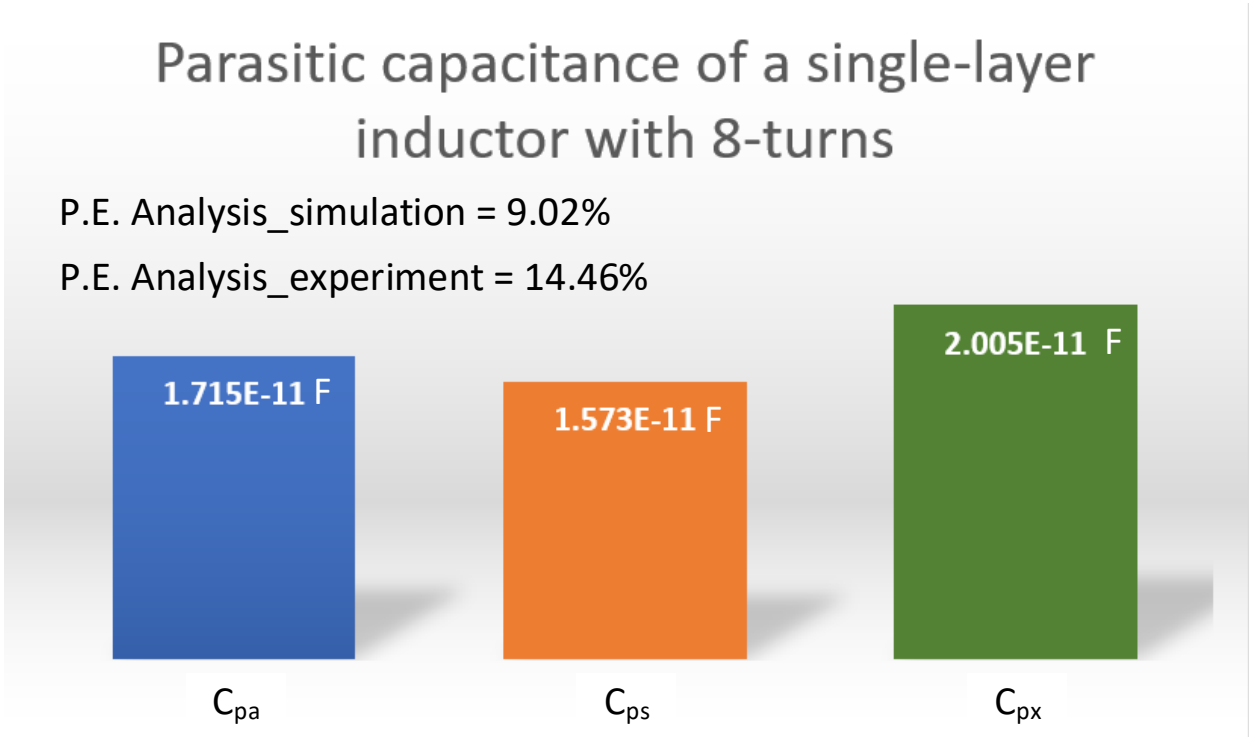


Figure 4.21: Comparison of geometry with long central limb between experiment, simulation, and analytical results.

and medium frequency range applications. The effectives of distance between turns are presented for overall parasitic capacitance and losses.

The following points summarize the original contributions of this paper.

- Achieving high accuracy with less complex model to estimate the parasitic capacitance for a single-layer inductor with magnetic core.
- Applying the new approximation of a rod conductor to estimating the parasitic capacitance.
- Determining the parasitic capacitance for applications with medium power and medium frequency range is applied.

CHAPTER 5

INVESTIGATING THE OVERALL PARAMETERS AFFECTING THE PARASITIC CAPACITANCE OF THE MAGNETIC COMPONENTS

5.1 Introduction

Magnetic components such as inductors, multi-phase inductors, and transformers are essential components of the electric and electronic systems [16, 47]. However, the magnetic components have inherent parasitics that affect their performance. The effects of the parasitics can manifest in a pronounced manner when the operating frequency is high and above a certain frequency [43].

Parasitic resistance is caused by core and conductor resistance [47]. The parasitic resistance is extensively discussed in the literature [47, 48]. The capacitances between turns, turn-to-core, and layer-to-layer constitute the overall parasitic capacitance of an inductor [16, 43]. The parasitic capacitance can reduce the power converter efficiency by changing the impedance of the inductor at high frequency. Moreover, It is the reason for electromagnetic interference to occur in the circuit. The parasitic capacitance also leads to over-voltage by occurring the resonance at the circuit besides the resonant frequency occurs because the self-capacitance [20, 21].

Modeling the parasitic capacitance of the magnetic components depends on specific parameters. These parameters can be divided into two main categories that are major parameters and minor parameters. However, most of the parasitic capacitance models focus on the major parameters. The major parameters are the conductor size, the number of turns, the distance between turns, and the number of layers [12, 16, 18, 21, 43].

Hence, the minor parameters of the parasitic capacitance should be taken into consideration to estimate the self-parasitic capacitance. The minor parameters include the permittivity of the bobbin material, the bobbin material corresponding to temperature and operating frequency, the size of the bobbin, the insulated material of the wire, the thickness of the insulated material.

With the intention to fill the knowledge gap related to the parameters that affect the parasitic

capacitance, this paper studies the overall parameters of the parasitic capacitance of magnetic components. By recognizing the major and minor parameters affecting the parasitic capacitance, the performance of the magnetic components can be designed for high operating frequency.

5.2 Major Parameters of the Parasitic Capacitance of the Magnetic Components

The parasitic capacitance of the magnetic components in high-frequency application significantly impacts the power electronics system performance [16,21]. Hence, the overall parameters of the parasitic capacitance should be taken under-consideration to estimate the parasitic capacitance of the magnetic components. The major parameters of the parasitic capacitance are presented in this section.

5.2.1 The size of the conductor

The conductor size of the winding of the inductor impacts on the parasitic capacitance value. By increasing the diameter of the conductor of the winding, the parasitic capacitance increases [41].

Fig. 5.1 shows the measured parasitic capacitances of a 20-turn inductor with different diameter size of conductors [41]. The parasitic capacitance increases when the conductor diameter increases from $0.2mm$ to $1mm$.

It has been shown that by increasing the size of the conductor, the parasitic capacitance slightly increases. The reason for that is with increasing the diameter of the conductor, the capacitance between the turn and the core increases where the area of the capacitance increased.

5.2.2 The turns number of the inductor

The number of turns N of the inductor is an essential factor to determine the inductance value as the inductance L is proportional to N^2. Therefore, it is important to consider the relationship between the parasitic capacitance and the number of turns of the inductor.

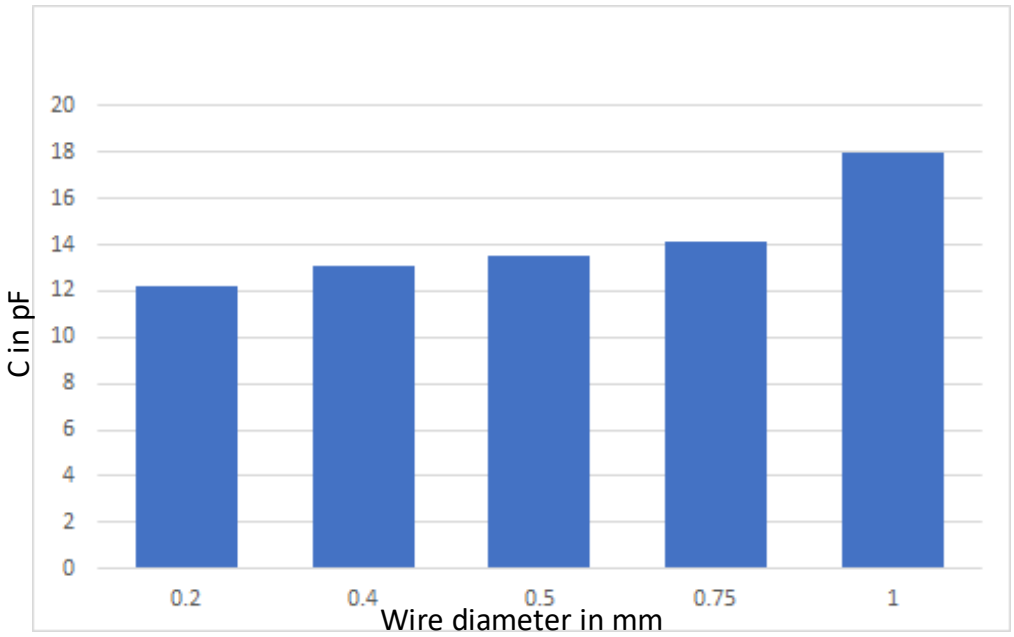


Figure 5.1: The parasitic capacitance of the 20 turn inductor with different wire diameter. The wire with $1mm$ diameter is wounded close to the core.

The parasitic capacitance of the inductor increases proportional with increasing the number of turns [12,41,43]. Fig. 5.2 shows the simulation results of an inductor with different number of turns. The U-I magnetic core with AWG 16 magnet wire is applied to extract the parasitic capacitance by electrostatic model with finite element analysis. It has been shown that by increasing the number of turns, the parasitic capacitance of the inductor increases.

5.2.3 The distance between turns

The turn-to-turn capacitance is a part of the parasitic capacitance of the inductor. Therefore, the relationship between the parasitic capacitance and the distance between turns should be taken in account. By increasing the distance between the number of turns, the parasitic capacitance of the inductor decreases as explained in [13, 44] and shown in the following equation.

$$dC_{g1}(\theta) = \frac{\epsilon_o l_t r_o}{p_1 + 2r_o(1 - cos(\theta))} \tag{5.1}$$

where C_{g1} is the equivalent elementary capacitor between the two turns with air-gap. The diameter of the conductor with and without the coating are r_o and r_c, respectively. The air gap between two

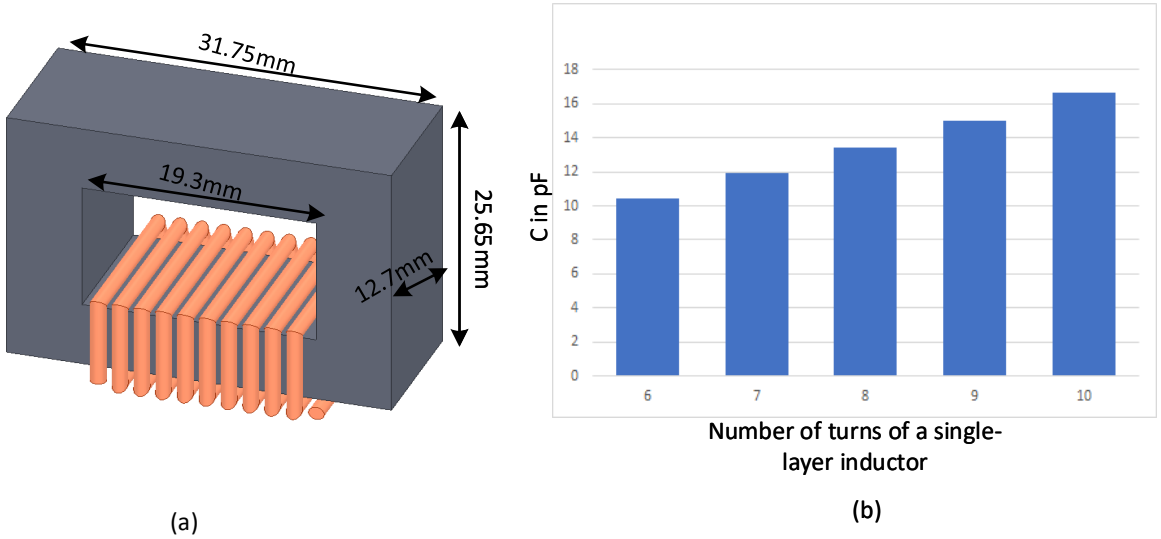


Figure 5.2: (a) The single-layer inductor with 10 turns. (b) The parasitic capacitance of the single-layer inductor in (a) with different number of turns.

turns is p_1 while l_t is the length of a single turn. The free-space permeability is represented by ϵ_o.

5.2.4 Number of layers of the winding

The coil winding of the magnetic components can be built in multiple layers. The multi-layer winding of the magnetic components can be suitable for different applications such as high-frequency transformers, and multi-layer inductor [16, 18, 21]. Therefore, it is essential to motion the impact of the multi-layer winding on the parasitic capacitance of the magnetic components.

Fig. 5.3 shows the parasitic capacitances between layers of two different multi-layer winding method structures [18]. The total equivalent capacitor of the winding C_{Wdg} is determined by the following equation.

$$C_{Wdg} = \sum_{v=1}^{NLayer-1} C_{Layer,v} \left(\frac{2}{N_{Layer}} \right)^2 \tag{5.2}$$

where the electric energy stored in one winding is represented by $W_{E,Wdg}$. The voltage of the winding and the all layers numbers of the winding are V_{Wdg} and N_{Layer}, respectively. C_{Layer} is the equivalent capacitance between two layers.

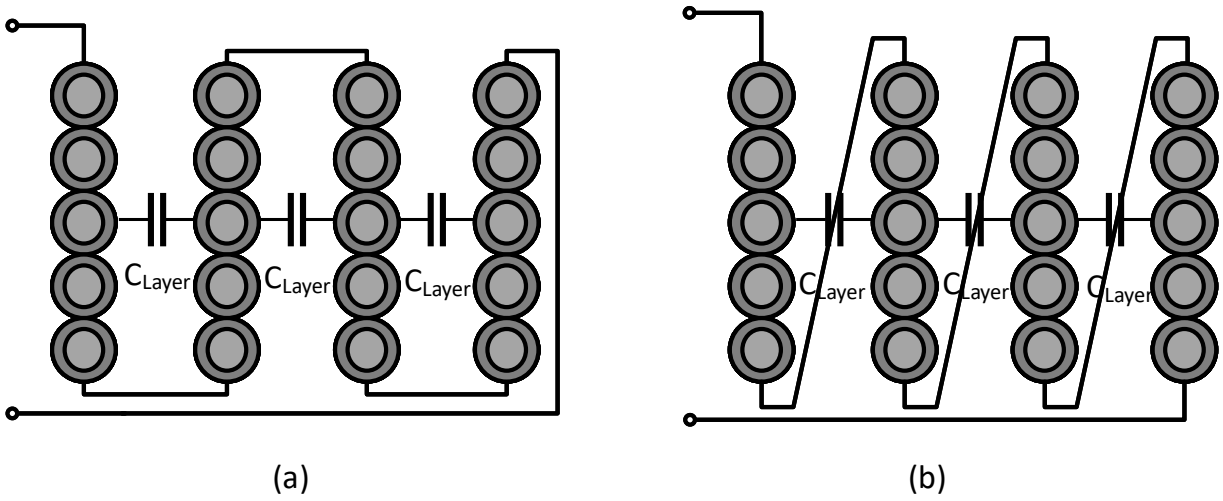


Figure 5.3: (a) Multi-layer Standard winding. (b) Multi-layer fly back winding.

With the assumption that all the capacitances between two layers $C_{Layer,v}$ are equal, the equivalent capacitance of the winding is simplified as following.

$$C_{Wdg} = 4\frac{N_{Layer} - 1}{N_{Layer}^2} C_{Layer} \tag{5.3}$$

The relationship between the number of layers and the parasitic capacitance of the winding of the magnetic components as shown in (5.3) is inverse proportional. With increased number of layers of the winding, the parasitic capacitance of the magnetic components decreases.

5.3 Minor Parameters of the Parasitic Capacitance of the Magnetic Components

The magnetic core and coil winding are the main parts of the magnetic components. The coil winding consists of a conductor and a bobbin. The coil winding parts affect the parasitic capacitance of the magnetic components. Therefore, it is essential to study the parameters of the winding parts. Moreover, the conductor is made of two main parts that are the conduction material and the insulation material. Therefore, the bobbin and the wire insulation can act as dielectric materials for the parasitic capacitance.

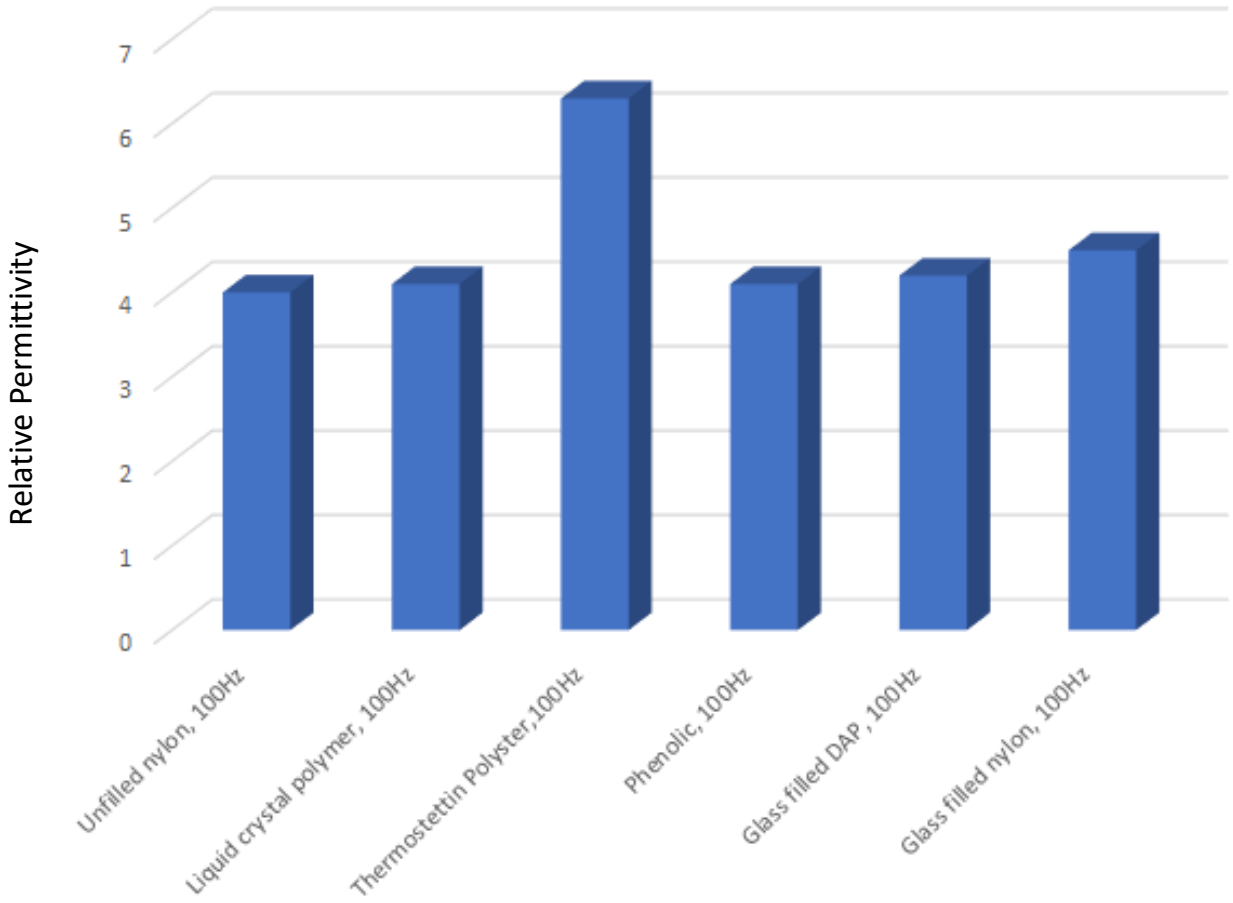


Figure 5.4: The relative permittivity of different bobbins.

5.3.1 Effects of the bobbin material

The bobbin of the magnetic components such as inductor, is located between the magnetic core and the conductor. Therefore, the bobbin acts as the dielectric material. The reason of that is the bobbin has a relative permittivity [44,49]. The relative permittivity of the bobbin material can vary with frequency among others [49,50]. For instance, the bobbin can be made from the polyethylene terephthalate (PET) material which the relative permittivity is 3.6 at $1kHz$ [51]. Fig. 5.4 depicts the relative permittivity of the several bobbin materials.

Therefore, the bobbin material affects the performance of the inductor by altering the resonant frequency which can subsequently cause the electromagnetic interference and lead to increased losses [16]. Hence, the resonant frequency and the parasitic capacitance can be designed by

selecting the suitable bobbin material.

Fig. 5.5 shows the parasitic capacitances of different bobbin materials with a single-turn inductor. The inductor with single-turn is simulated with finite element analysis to extract the parasitic capacitance as shown in Fig. 5.6. Moreover, the parasitic capacitance of the single-turn inductor can be determined by using the equations (8.1) and (8.2) as presented in [43, 44].

$$C_{tt} = \epsilon_o l_t \int_0^{\frac{\pi}{6}} \frac{1}{1 + \frac{1}{\epsilon_r} \ln \frac{2r_o}{2r_c} - \cos(\theta)} d\theta \tag{5.4}$$

$$C_s(n) = \frac{C_{tt}}{2 + \frac{C_{tt}}{C_s(n-2)}} + C_{tt} \tag{5.5}$$

where the turn-to-turn capacitance is represented by C_{tt} while the total capacitance is $C_s(n)$ with the number of turns of the inductor being n. The permittivity of the space and the relative material are ϵ_o and ϵ_r, respectively. The radii of the conductor without and with the coating are r_c and r_o, respectively. The length of each turn is represented by l_t.

The other important factors that affect the parasitic capacitance of the bobbin are the operating frequency, temperature, and thickness of the bobbin. In the following subsections, the effects of these factors are presented.

5.3.1.1 Frequency Effects on the Bobbin

The operating frequency of the inductor affects the parasitic capacitance [44, 50]. The frequency dependence of relative permittivity is one of the main reasons that the parasitic capacitance varies with the operating frequency. Fig. 8.3 presents the relative permittivity of the PET material versus the frequency [50]. The relative permittivity is determined for a range of operating frequency that is $200Hz$ up to $1MHz$ at the room temperature.

As shown in Fig. 8.3, the relative permittivity decreases with increased operating frequency. Therefore, the parasitic capacitance of the inductor can be reduced with increasing the operating frequency. Fig. 5.8 shows the estimated parasitic capacitance of the single-turn inductor with PET bobbin material.

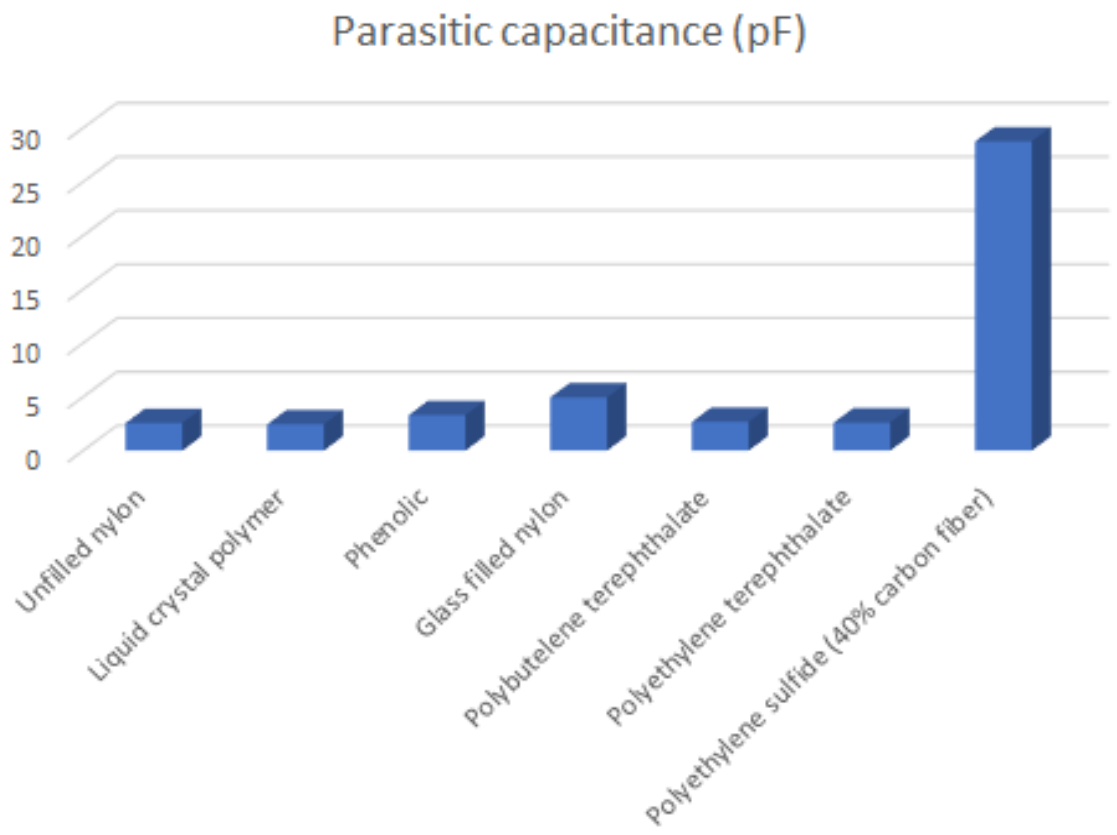


Figure 5.5: The parasitic capacitance of an inductor with different bobbins.

The parasitic capacitance of the single-turn inductor decreases with increased operating frequency. Therefore, higher operating frequency results in lower parasitic capacitance. As a result, the operating frequency is one of the important factors of varying the parasitic capacitance based on the bobbin material response. This leads to change the resonant frequency of the inductor. As shown in the following equation:

$$f_r = \frac{1}{2\pi\sqrt{C_p L}} \tag{5.6}$$

where f_r is the resonant frequency of the inductor L. The inductor with the same geometry and bobbin material can have different resonant frequency when the operating frequency changes.

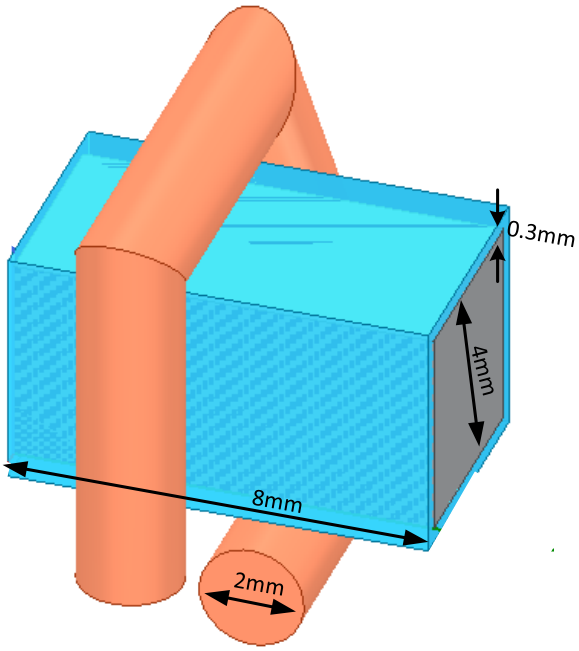


Figure 5.6: The single turn inductor with magnetic core and PET bobbin material.

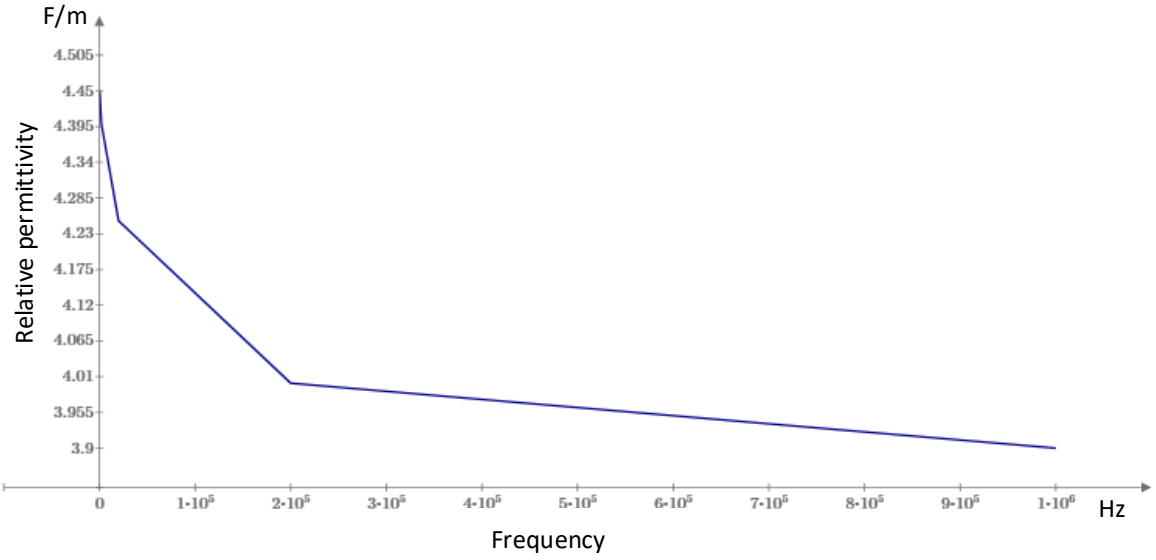


Figure 5.7: The relation between the frequency and the relative permittivity of the PET bobbin material.

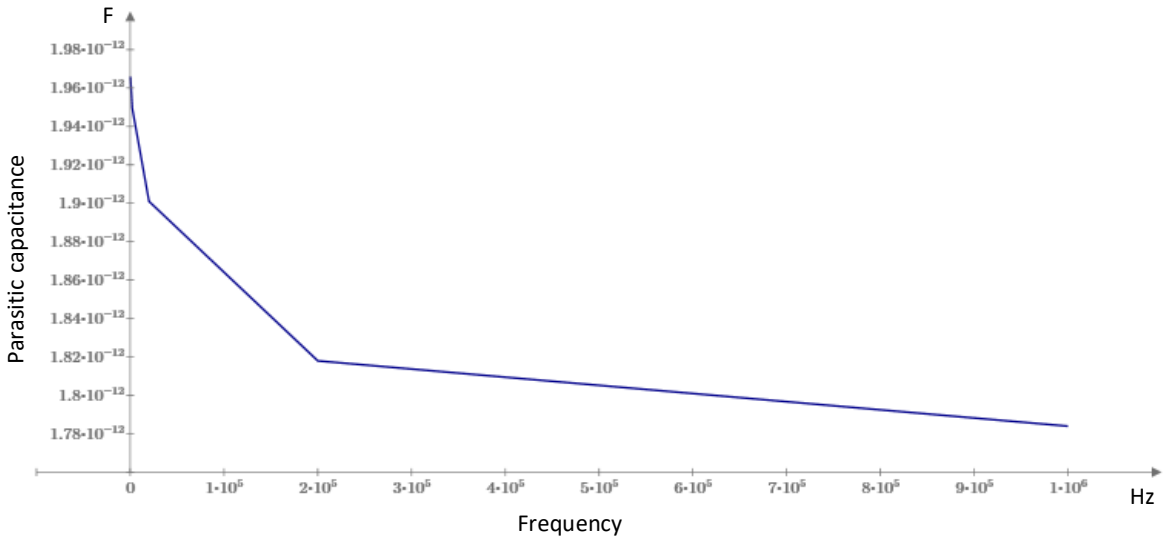


Figure 5.8: The estimated parasitic capacitance of the single turn inductor with PET bobbin versus frequency.

5.3.1.2 Temperature Effects on the Bobbin

Another factor that should be considered is the temperature of the magnetic components. When the operating temperature of the magnetic components changes, the parasitic capacitance changes too. The variation of the parasitic capacitance versus the temperature can be caused by the relative permittivity of the bobbin [50].

The parasitic capacitance of the single-turn inductor with the magnetic core can be calculated when the temperature changes. Fig. 5.9 depicts the curve of the parasitic capacitance percentage versus the temperature. The room temperature is selected as the reference temperature of the parasitic capacitance percentage. Table 5.1 shows the relative permittivity of the PET bobbin material versus the temperature at $2kHz$ [50].

As a result, the resonant frequency of the inductor can be changed when the temperature changes. Moreover, the relationship between the temperature and the parasitic capacitance of the inductor is nonlinear.

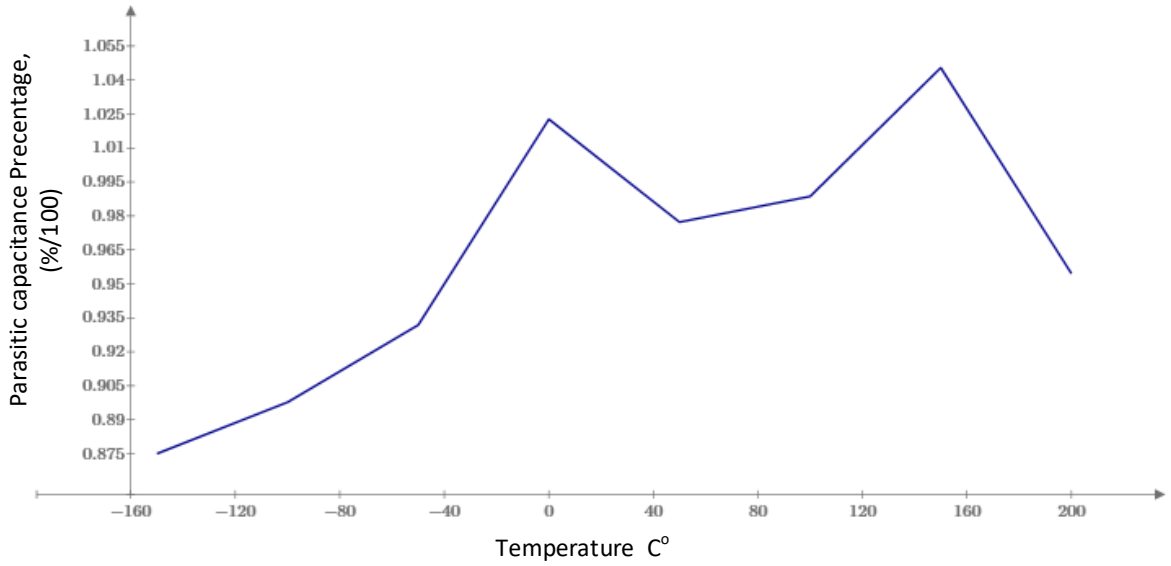


Figure 5.9: The parasitic capacitance percentage of the single turn inductor with PET bobbin versus the temperature.

Table 5.1: The PET permittivity of the bobbin versus temperature.

Temperature C^o	Permittivity ϵ	Temperature C^o	Permittivity ϵ
−150	3.85	25	4.4
−100	3.95	50	4.3
−50	4.1	100	4.35
0	4.5	150	4.6

5.3.1.3 Thickness of the Bobbin

The last factor of the bobbin is the thickness of the bobbin. The bobbin can be made by different thicknesses. Therefore, the parasitic capacitance of the inductor can be reduced by increasing the thickness of the bobbin. Fig. 5.10 shows the parasitic capacitance of the single-turn inductor with different thicknesses of the bobbin. The different thicknesses of the bobbin with PET material are simulated from $0.2mm$ to $1.2mm$ to extract the parasitic capacitance of the single-turn inductor.

As a result, the bobbin plays an important role on the value of the parasitic capacitance where it is located between the turns and the core. By selecting the bobbin material with low relative

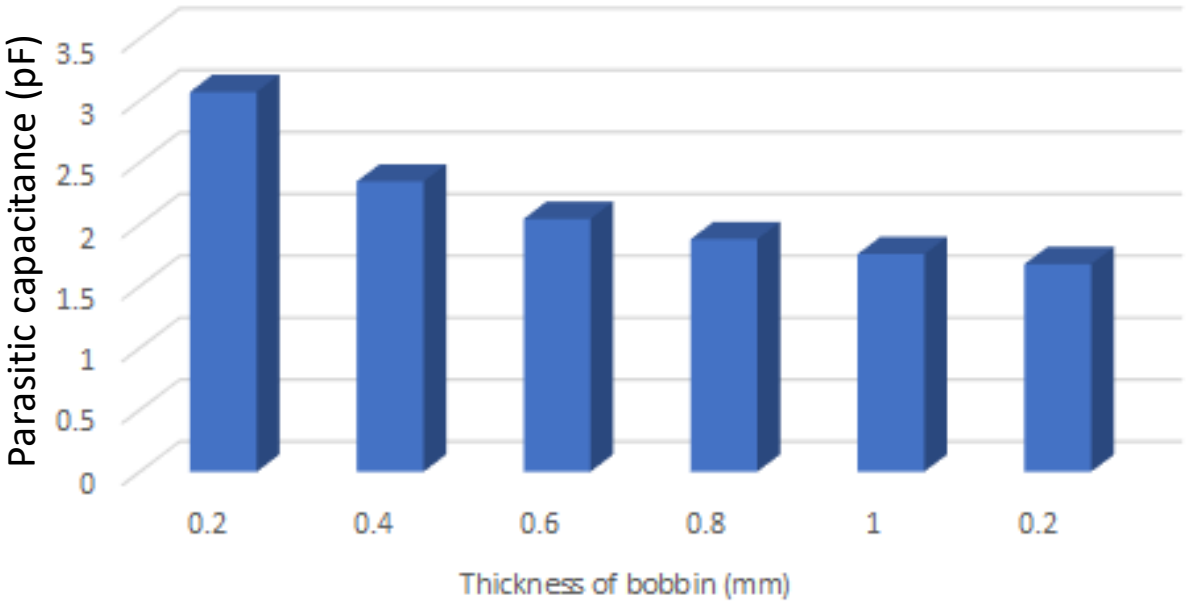


Figure 5.10: Thicknesses of the bobbin versus the parasitic capacitance.

permittivity, the parasitic capacitance of the inductor can be reduced. Moreover, the operating frequency, the temperature, and the thickness of the bobbin can be designed to achieve the desirable parasitic capacitance of the inductor.

5.3.2 Effects of the Wire

The wire of the coil winding contains two parts which are the conductor and the insulator. The wire insulation can be made by different thickness and material. Based on the thickness of the wire insulation, the wire can be divided to two types. The first type of wire is coated with a very thin insulation layer such as magnet wire is the first type [25].The wire insulation of this type of wire can be ignored for estimating the parasitic capacitance.

Another type of wire is having a thicker insulation layer than the magnet wire's [52]. The insulating material of the wire has effects on the parasitic capacitance specially of the multi-layer inductor [18, 43]. However, for the single-layer inductor, the effects of the wire insulator can be

reduced when there is a space between turns. The reason of reduced effects of the wire insulator on the parasitic capacitance is the dielectric of the air dominates the dielectric material of the wire insulator.

The focus of this paper is on the single-layer inductor with magnetic core. Therefore, the main effect of the wire insulator is for the parasitic capacitance between turns and turn-to-core. When the inductor has a bobbin, the capacitance between the turn and the core has two different dielectric materials, namely the bobbin material and the wire insulator material. The capacitance between the turn and the core can be calculated as explained in [43, 44].

The parasitic capacitance of the single-turn inductor with wire insulating thickness of 0.41 mm is extracted from electrostatic model software. The parasitic capacitance is $2.1465pF$ while the parasitic capacitance of the AWG 12 single-turn inductor with magnet wire is $2.76142pF$. The reason for reduced the parasitic capacitance with insulated wire is the increased distance between the conductor and the core. The distance with insulated wire between the conductor and the core is higher than the distance between the magnet wire and the core.

5.4 Results

A single-layer inductor with magnetic core is applied to extract the parasitic capacitance by the finite element analysis. The American wire gauge of the selected wire is 22. Therefore, two different types of wires are selected to compare between their parasitic capacitances. The magnet wire and the insulated wire such as Hook-up wire are selected [25, 52]. The parasitic capacitances are determined by using the method in [43, 44], and the electrostatic model with FEA.

The parasitic capacitances of the inductor are determined with and without the bobbin for both wires of the inductor. Fig. 5.11 shows the inductor with the magnet wire with bobbin in (a) and without bobbin in (b) while (c) shows the insulated wire of the inductor with the bobbin, and without the bobbin in (d). The bobbin thickness for both inductors is $0.3mm$ and the insulation thickness of the wire is $0.41mm$.

The selected bobbin material for the simulation experiment is PET. The material type of the

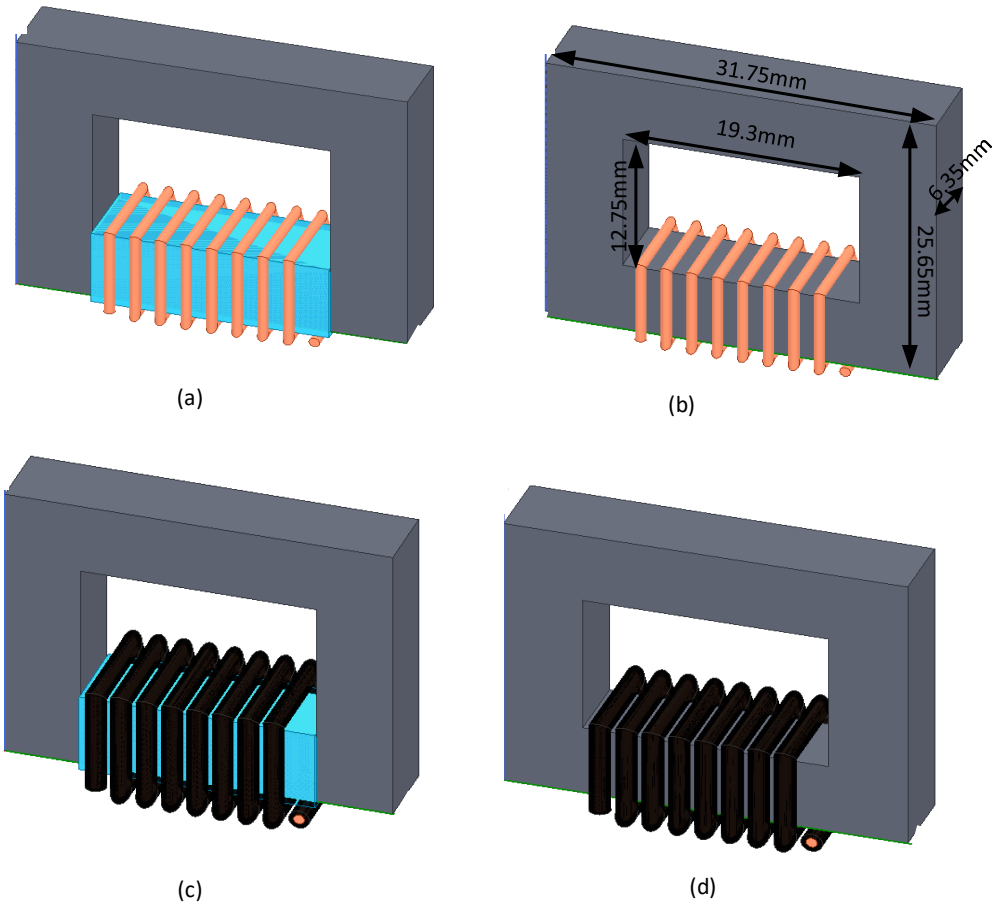


Figure 5.11: (a) the inductor with magnet wire and PET bobbin, (b) the inductor with magnet wire, (c) the inductor with insulated wire and PET bobbin, (d) the inductor with insulated wire.

wire insulator is Polyvinyl chloride. The conductor material for both wires is copper. As shown in Fig. 5.11, the inductor with magnet wire has advantage for having less space of the winding. However, the parasitic capacitance of the inductor with insulated wire is less capacitance.

Fig. 5.12 shows the parasitic capacitances of the inductor with same number of turns but different type of wires. As shown in the results, the highest parasitic capacitance is the inductor with magnet wire and without the bobbin. The main reason of increasing the parasitic capacitance is the short distance between the magnetic core and the conductor. Therefore, The insulated wire with the bobbin can reduce the parasitic capacitance of the inductor.

The results show that the inductor with insulated wire has lower parasitic capacitance. Moreover, The parasitic capacitance can be reduced with selecting the low relative permittivity of the bobbin

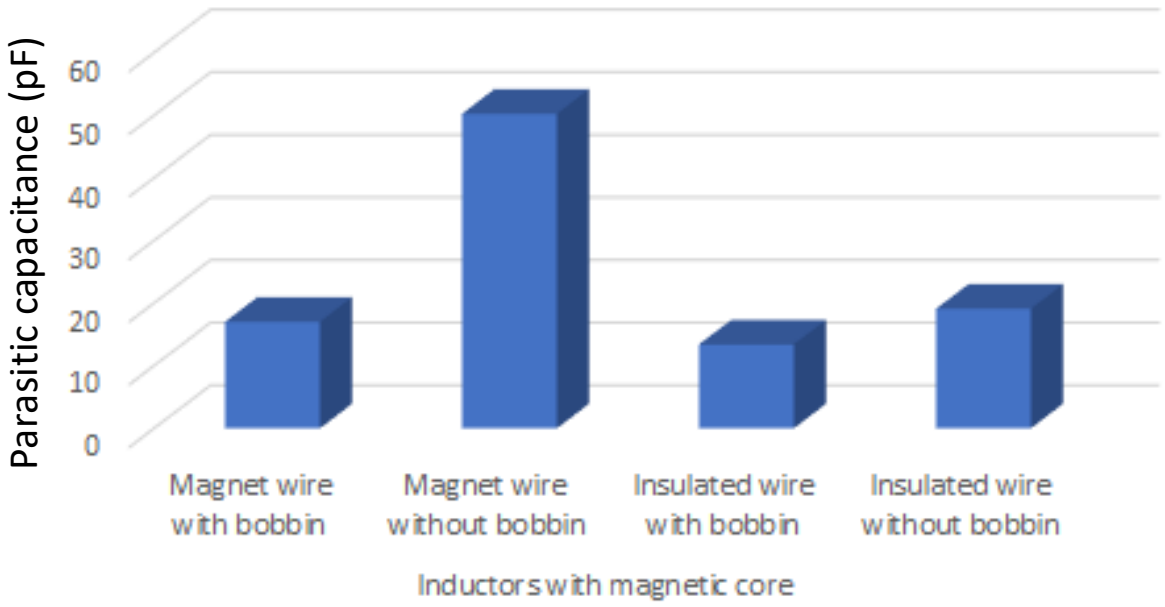


Figure 5.12: The parasitic capacitances of the four inductors with different wires and with/without bobbins.

and the insulated wire materials.

5.5 Conclusion

This paper presents the parameters that affect the parasitic capacitance of the magnetic components. These parameters should be carefully selected to design an inductor with low parasitic capacitance.

The parameters affecting the parasitic capacitance are divided into major and minor parameters. The size of the conductor, the number of turns, the distance between turns, and the number of layers are the major parameters of the parasitic capacitance.

On the other hand, the temperature, the operating frequency, and the thickness of the bobbin and insulated wire are the minor parameters which affect on the parasitic capacitance. The effects of these parameters are represented on the paper.

The parasitic capacitance of the magnetic component can be reduced by proper selecting of the

independent and dependent parameters.

CHAPTER 6

EXISTING TECHNIQUES OF REDUCTION THE PARASITIC CAPACITANCE FOR INDUCTORS

The performance of inductors can be affected at high frequency. One of the reasons that affects the performance of inductors at certain frequency is the parasitic capacitance [11–13, 16–20, 20, 22, 26–29, 43, 45]. In order to maintain the performance of inductors, the parasitic capacitance of inductors should be reduced.

Several techniques of reducing the parasitic capacitance of inductors have been proposed [27, 30, 32, 53, 54]. There are three main approaches to parasitic capacitance reduction. The first one is to reduce the parasitic capacitance using the mutual capacitance between two separate capacitors [27, 54]. The second method is to use a small capacitor with mutual inductor model to decrease the parasitic capacitance of an inductor [30, 32, 54]. The third approach is to add a small magnetic component to the inductor in order to improve its performance and reduce the parasitic capacitance [53].

The technique of adding a small magnetic component does not cancel the parasitic capacitance itself. However, it reduces the deleterious effects of the parasitic capacitance [53]. Therefore, this technique is mainly applied in the filter application.

The main approaches of reducing the parasitic capacitance of inductors are explained in this chapter. This chapter is divided into two sections as followed: Section 6.1 introduces the concept of generating a negative capacitance by using the mutual capacitance. The concept of reducing the parasitic capacitance by applying mutual inductance is shown in Section 6.2.

6.1 Using Mutual Capacitance Concept to Reducing the Parasitic Capacitance

The concept of mutual capacitance is when two capacitors are to next each other, there is a mutual capacitance between them [27, 28]. Figure **??** shows the definition of mutual capacitance

between two capacitors. The capacitances between the conductors are represented in figure **??**. The capacitors C_1, C_2, and C_M, which are shown in figure **??**(a), represent the effects of C_{12}, C_{13}, C_{14}, C_{23}, and C_{34}. The mutual capacitance is represented by C_M. The two capacitors have four conductors. C_1 is the capacitor of conductors 1 and 2, if they are grouped. Conductors 3 and 4 are grouped as capacitor C_2 while the mutual capacitance C_M is the capacitance between C_1 and C_2.

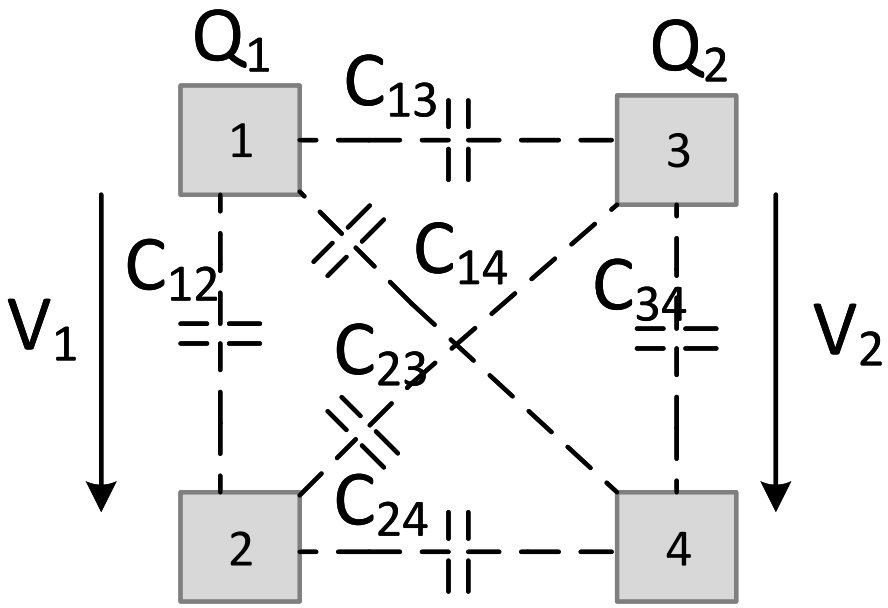


Figure 6.1: A flowchart of methods to reduce the size of magnetic components.

The mutual coupling of the capacitances can affect the total charge of capacitors as shown in equation (6.1). The voltages V_1 and V_2 are the voltages applied on C_1 and C_2, respectively.

$$\begin{aligned} Q_1 &= C_1 V_1 + C_M V_2 \\ Q_2 &= C_M V_1 + C_2 V_2 \end{aligned} \tag{6.1}$$

where the total electric charge of C_1 is denoted by Q_1. Q_2 is the total electric charge on C_2. It is noticeable that the mutual capacitance affects the electric charge of the capacitor.

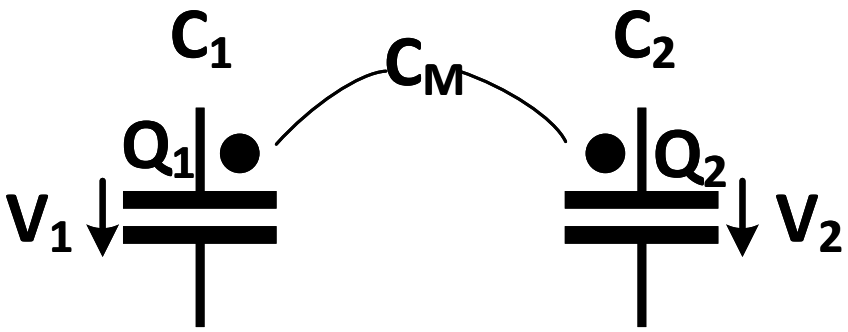


Figure 6.2: A flowchart of methods to reduce the size of magnetic components.

When the two capacitors are close to each other and the electric fields are not fully confined within the capacitors, the mutual capacitance occurs between them. The capacitors C_1 and C_2 can be determined by C_{12}, C_{24}, C_{13}, C_{14}, C_{23}, and C_{24}. The mutual capacitance can be expressed as a function of C_{13}, C_{14}, C_{23}, and C_{24}.

$$\begin{aligned} C_1 &= C_{12} + \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_2 &= C_{34} + \frac{(C_{13}+C_{14})(C_{23}+C_{24})}{C_{13}+C_{14}+C_{23}+C_{24}} \\ C_M &= \frac{C_{23}C_{14} - C_{13}C_{24}}{C_{13}+C_{14}+C_{23}+C_{24}} \end{aligned} \tag{6.2}$$

In this case, it is clear that the capacitors C_1 and C_2 are larger than their self-capacitances C_{12} and C_{34}, respectively. Moreover, the capacitors' value increases with decreasing the distance between capacitors C_1 and C_2.

The mutual capacitance concept can be applied to cancel the parasitic capacitance. By using the Wheatstone bridge theory, the mutual capacitance can be reached to zero. When the product of the capacitance on the diagonal branches is equal to the product of the capacitance on the top and bottom branches, the mutual capacitance becomes zero. Equation (6.3) shows the concept of Wheatstone bridge.

$$C_{23}C_{14} = C_{13}C_{24} \tag{6.3}$$

Using Wheatstone bridge as shown in equation (6.3) to reduce the parasitic capacitance. Figure 6.3 shows the cancellation technique of parasitic capacitance for differential mode (DM) inductor.

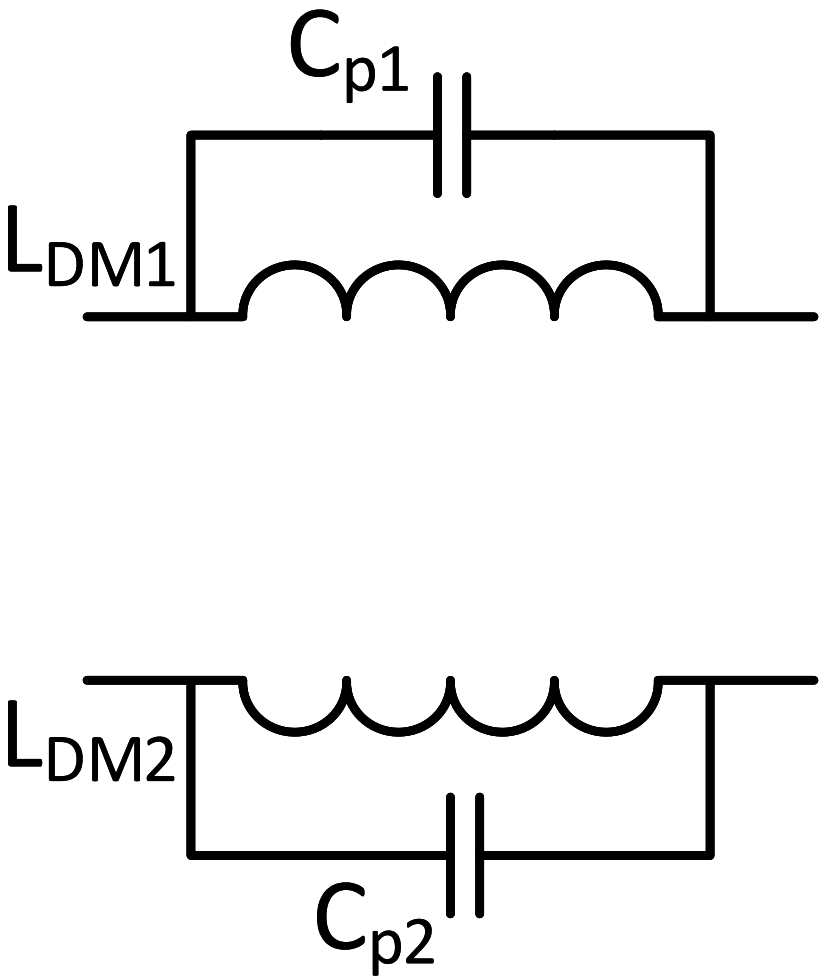


Figure 6.3: A flowchart of methods to reduce the size of magnetic components.

where the parasitic capacitances C_{p1} and C_{p2} represent the capacitances C_{13} and C_{24} of the mutual capacitance, respectively. Two small capacitors can be added to the DM inductor, which are C_{CL1} and C_{CL2}. The small capacitors C_{CL1} and C_{CL2} can represent the capacitances C_{14} and C_{23}, as shown in figure 6.4.

When the product of the capacitors C_{CL1} and C_{CL2} are equal to the product of parasitic capacitance C_{p1} and C_{p2}, the parasitic capacitances are reduced. This technique is explained with

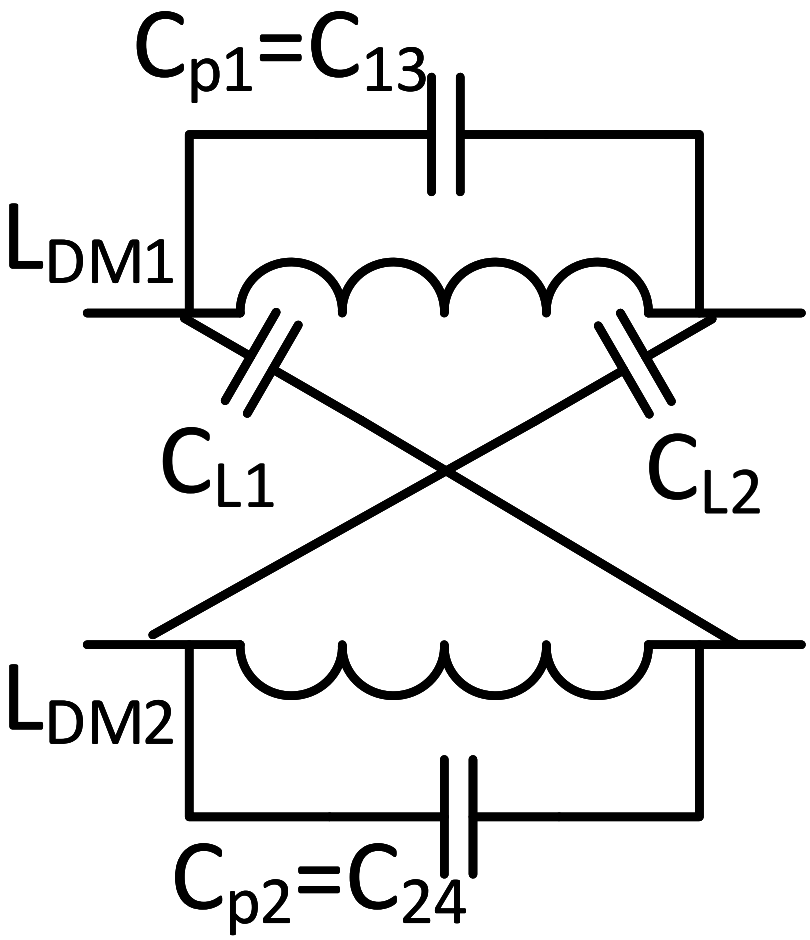


Figure 6.4: A flowchart of methods to reduce the size of magnetic components.

more details in [55].

6.2 Using the Mutual Inductance Concept for Reducing the Parasitic Capacitance

The parasitic capacitance of an inductor can be reduced by using the mutual inductance with a small capacitor [26, 28, 30–33]. The concept of reducing the parasitic capacitance of the inductor is by adding a small capacitor, as shown in figure 6.5. Figure 6.5 depicts two inductors that are connected in series with the direct coupled inductor.

where the two inductors can be represented by L and n^2L. The two inductors are directly coupled on one core. The turn ratio between the two inductors is n while the inductance ratio of

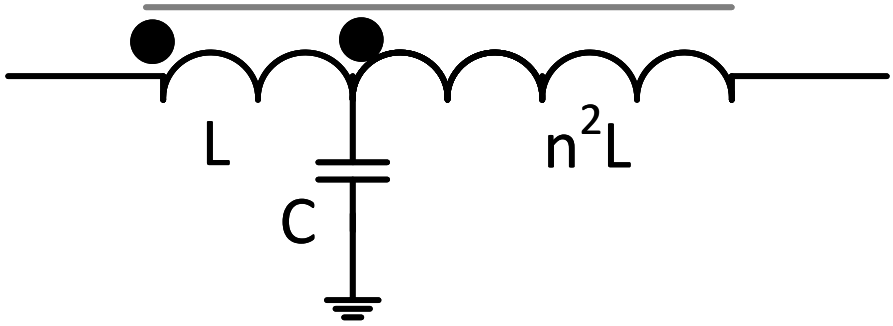


Figure 6.5: A flowchart of methods to reduce the size of magnetic components.

the two inductors is n^2. C is the small capacitor that is connected to the inductors.

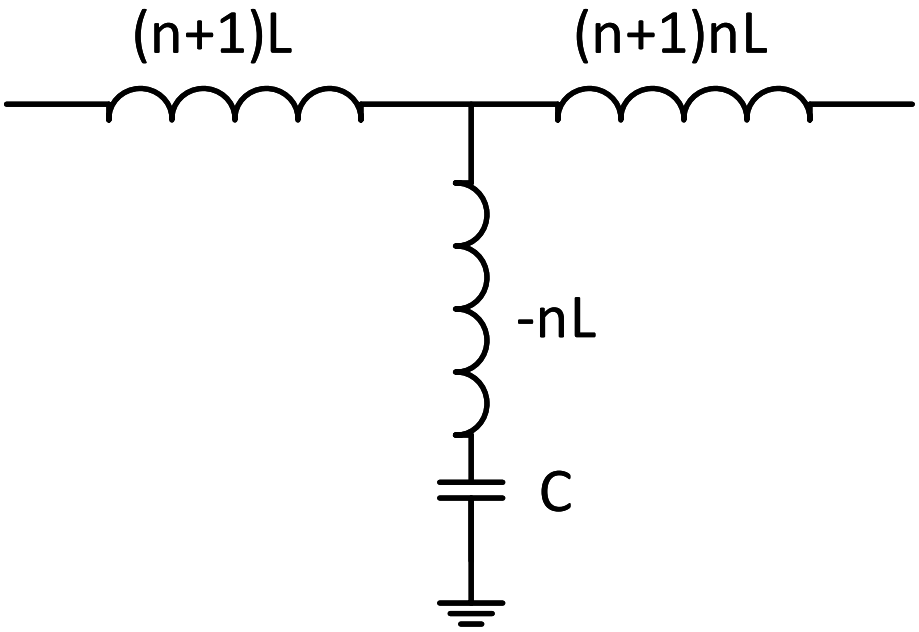


Figure 6.6: A flowchart of methods to reduce the size of magnetic components.

The equivalent circuit of a coupled inductor with adding a small capacitor is shown in figure 6.6. The equivalent circuit is represented by a T-model of coupled inductors where the magnetic coupling coefficient k is perfectly coupled.

In order to reduce the parasitic capacitance, the negative capacitance should be generated. The negative capacitance can be generated by applying the $Y - \Delta$ transformation method. Figure 6.7

shows a π model of the coupled inductor equivalent circuit. The negative capacitance is generated in the π model to cancel the parasitic capacitance.

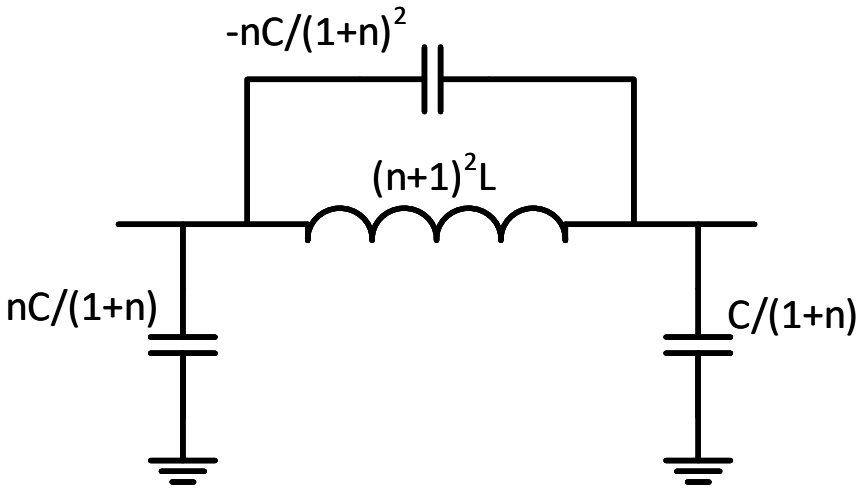


Figure 6.7: A flowchart of methods to reduce the size of magnetic components.

$$C_{neg} = \frac{nC}{(n+1)^2} \tag{6.4}$$

where the generated negative capacitance is denoted by C_{neg}. The generated capacitance and the two shunt capacitances are generated by using a small capacitor with a π model. In the direct coupled, the shunt capacitances have a positive value.

$$C_{gl} = \frac{nC}{n+1} \tag{6.5}$$

$$C_{gr} = \frac{C}{n+1} \tag{6.6}$$

where C_{gl} and C_{gr} represent the shunt capacitances of left and right capacitances of the π that are connected to the ground.

The generated capacitance depends on the connections and coupling polarities of two inductors besides the value of adding a capacitor [55]. different techniques can be applied based on mutual inductance, as explained in [55].

CHAPTER 7

PARASITIC CAPACITANCE REDUCTION TECHNIQUE BY USING MUTUAL INDUCTANCE AND MAGNETIC COUPLING

7.1 Introduction

Inductors and common-mode chokes have inherent resistance and capacitance parasitics which affect their performance. The effects of parasitics can appear when the frequencies are high. Because of rapid development of switching frequency speed, different applications in power electronics systems are affected. Electromagnetic interference (EMI) filters are applied in power electronics systems at very high frequencies for reducing EMI noise [20,21,29,45]. Inductors and transformers are important devices of magnetic components which are applied in most electronic and electrical systems. These components have advantages and disadvantages with increasing the speed of switching frequencies. The volume and size of transformers and inductors are reduced with high frequencies. However, the parasitics affect on the performance of magnetic components [16,20,21]. The magnetic components have two types of parasitics: resistance and capacitance of windings. The parasitic resistance is attributed to winding resistance and core losses. The parasitic capacitance exists due to capacitances between turn-to-turn and layer-to-layer of the winding, also due to capacitance between winding and core. The parasitic components of an inductor can be represented by lumped parameters as shown in figure 1 (a) [14, 17, 45, 53].

At high frequency, the inductor impedance is dominated by parasitic capacitance, which can affect the impedance of an inductor as shown figure 1(b). The inductor impedance increases as frequency increases up to a certain extent. This phenomenon occurs because of the properties of magnetic material and geometric dimensions of inductor [14, 32, 53].

Several techniques have been proposed to improve inductor performance at high frequencies [27, 30, 32, 53, 54]. There are three main approaches to parasitic capacitance reduction. The first one is to reduce the parasitic capacitance using the mutual capacitance between two separate

capacitors [27, 54]. The second method is to use a small capacitor with mutual inductor model to eliminate the parasitic capacitance of an inductor [30, 32, 54]. The third approach is to add a small magnetic component or radio frequency to the inductor in order to improve its performance and reduce the parasitic capacitance [53].

If the magnetic coupling coefficient changes, then the inductor value will change too. Therefore, it is necessary to develop a method that correctly sizes the small capacitor to generate an appropriate value of the negative capacitance. The calculation method of the additional capacitor should be based on the magnetic coupling coefficient to improve the efficiency of the inductor. This paper introduces a technique that calculates the additional capacitor by the value of magnetic coupling.

Adding a capacitor to an inductor has been previously done for EMI filters that are aimed at high frequencies [30, 32, 53, 54]. The proposed approach enables improved inductor performance at frequencies below its first resonant frequency. Moreover, the proposed approach can improve the inductor frequency response by shifting the first resonant frequency from low to higher frequencies. In contrast to the current EMI approaches that suffer from inferior performance at lower frequencies, the proposed technique achieves an impedance increase by up to 40 dB Ω below the first resonant frequency. The mutual inductance concept will be applied to an inductor with a new technique in order to improve its performance and reduce the parasitic capacitance. The current work is an extension of the previous work which showed [11] the sizing calculation of an additional small capacitor based on the magnetic coupling coefficient and mutual inductance which verified by simulation software. In this chapter, the experimental results are applied and compared to simulation results which show high reduction of parasitic capacitance.

The rest of the paper is organized as follows. The parasitic capacitance reduction technique for an inductor based on the relationship between mutual inductance model with magnetic coupling coefficient is presented in section 8.2. In the section 8.4, The experimental and simulation results of applying the new parasitic capacitance reduction technique by network analyzer device and MATLAB software are shown. Finally, the conclusion and discussion are presented in section 8.5.

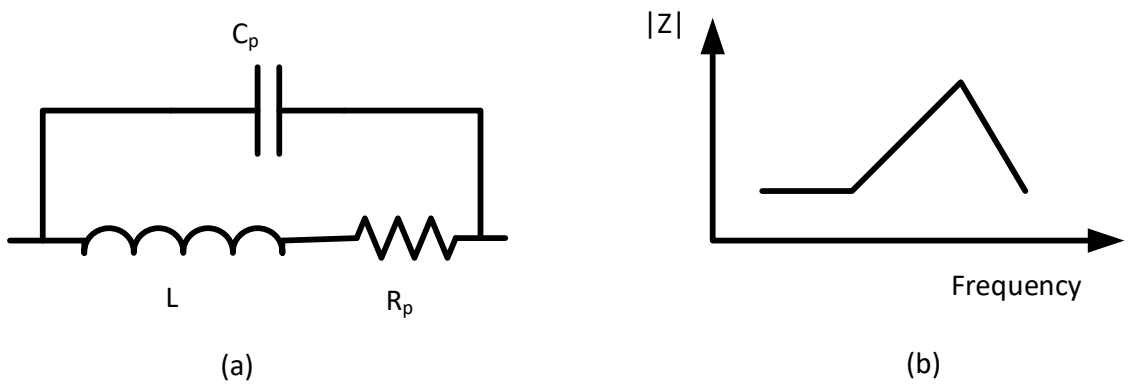


Figure 7.1: (a) Inductor model of parasitics (b) The impedance curve of an inductor versus frequency.

7.2 Reduction Technique using mutual inductance and magnetic coupling

The parasitic capacitance is modeled by the capacitor that is connected between the terminals of winding as shown in the figure 1 (a). In order to reduce the parasitic capacitance of an inductor, generating a negative capacitance is one of the effective methods [27, 32, 54]. The reduction parasitic capacitance method of two direct and indirect coupled windings of an inductor has been proposed in [**?**]. This paper introduces a technique using two coupled windings in relation to the magnetic coupling coefficient of the inductor. Fig 7.2. shows an inductor that has direct coupled windings with an additional small capacitance C. This coupled inductor has two inductances with different values L_1 and L_2. The coupling coefficient k of the two windings is treated as a parameter that may not be equal to 1. The additional capacitor with a small value, which is determined later on , is connected to the center tap of the inductor.

The number of turns can be chosen as $N = \frac{L_1}{M}$ where M is the mutual inductance of the two windings. The two windings of the inductor can be decoupled by decoupling network method. Figure 7.3 depicts the decoupled inductor with the magnetic coupling coefficient $k \neq 1$ and $N = \frac{L_1}{M}$. In order to generate a negative capacitance that can reduce the effects of parasitic capacitance, $Y - \Delta$ transformation is applied. The equivalent circuit of applying $Y - \Delta$ transformation using synthesis

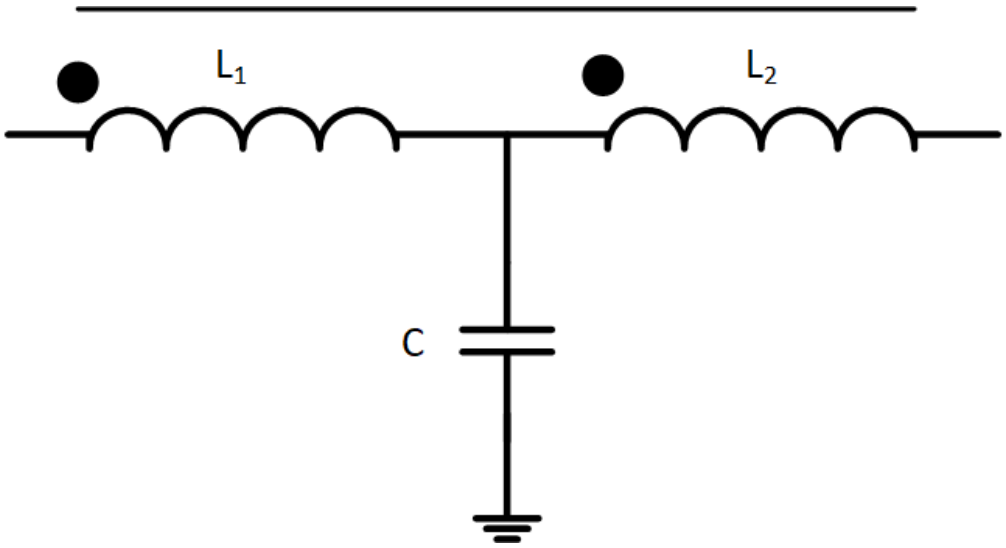


Figure 7.2: The direct coupled windings with adding small capacitor.

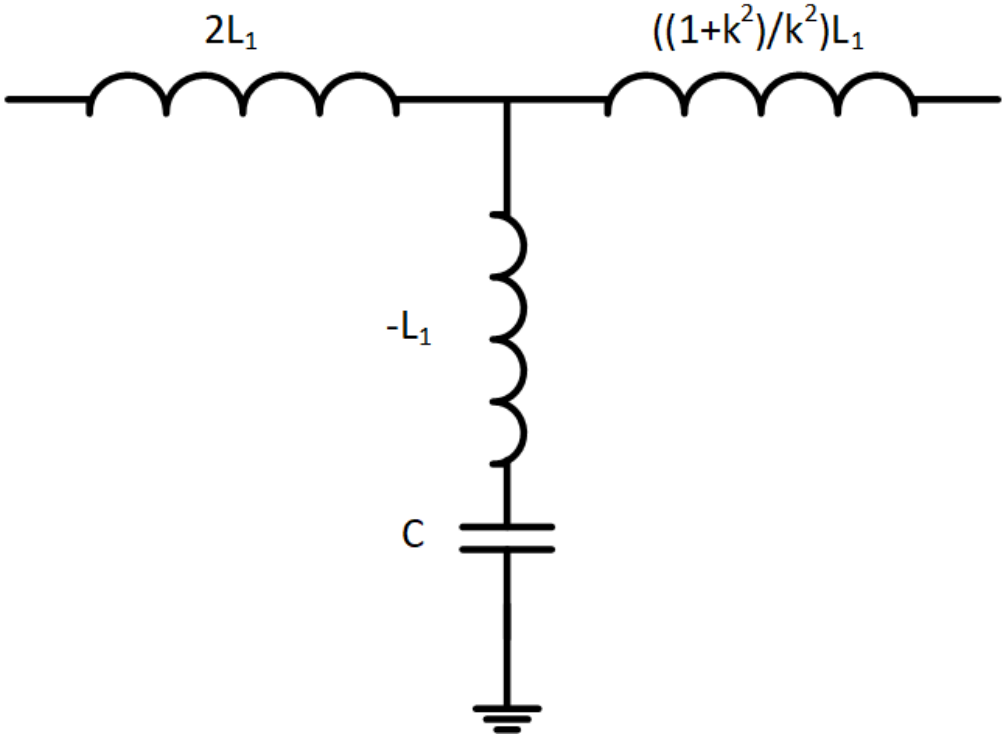


Figure 7.3: The decoupled mutual inductance with magnetic coupling coefficient.

theory is represented in figure 7.4.

As shown in figure 7.4, the effects of adding a small capacitor to the coupled inductor with $k \neq 1$ are described by three different capacitors values. First capacitor C_v is in parallel with the parasitic capacitance and series with L_s. The other two capacitors are shunt capacitors with

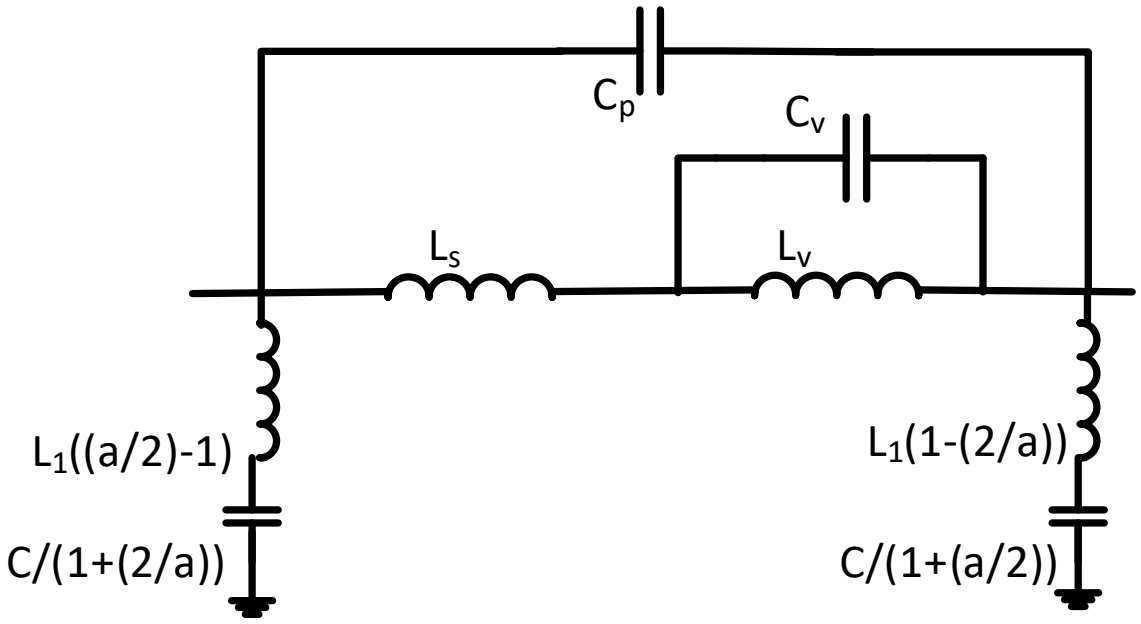


Figure 7.4: The π model of decoupled mutual inductance with k and the addition small capacitor.

different values. The parameters that are shown in the π model are the following:

$$a = \frac{1 + k^2}{k^2} \tag{7.1}$$

$$C_v = \frac{C}{-2a} \tag{7.2}$$

$$L_v = 2aL_1 \tag{7.3}$$

$$L_s = (2 - a)L_1 \tag{7.4}$$

where a is a simplified equation that is derived from the modeling of direct coupled windings when the number of turns is chosen as $N = \frac{L_1}{M}$. The highest value of a is 2 when $k = 1$. C_v has always a negative capacitance that can impact and reduce the parasitic capacitance at any value of k. L_v which is the inductance has a positive value at any the magnetic coupling coefficient.

The value of both two inductors and two capacitors on the shunt sides depend on the value of k. The two shunt inductors can be positive or negative depending on k, while the shunt capacitors

are always positive with very small capacitance. The parameters for different magnetic coupling coefficient k are determined as follows:

$$k = 1 \Rightarrow \begin{cases} L_s = 0 \\ \frac{C}{1+\frac{a}{2}} = \frac{C}{1+\frac{2}{a}} = 0 \\ L_1(\frac{a}{2} - 1) = L_1(1 - \frac{2}{a}) = 0 \end{cases}$$

$$0.9 \leq k < 1 \Rightarrow \begin{cases} -20\%L_1 \leq L_s < 0 \\ \frac{C}{1+\frac{a}{2}} = \frac{C}{1+\frac{2}{a}} = 50\%C \\ -11\%L_1 \leq L_1(\frac{a}{2} - 1) < 0 \\ L_1(1 - \frac{2}{a}) \leq 10\%L_1 \end{cases}$$

$$0.85 \leq k \leq 0.89 \Rightarrow \begin{cases} -35\%L_1 \leq L_s < 0 \\ \frac{C}{1+\frac{a}{2}} = \frac{C}{1+\frac{2}{a}} \approx 50\%C \\ 17\%L_1 = L_1(\frac{a}{2} - 1) \\ L_1(1 - \frac{2}{a}) \leq 15\%L_1 \end{cases}$$

$$0.8 \leq k \leq 0.85 \Rightarrow \begin{cases} -55\%L_1 \leq L_s < 0 \\ \frac{C}{1+\frac{a}{2}} \approx \frac{C}{1+\frac{2}{a}} \approx 50\%C \\ L_1(\frac{a}{2} - 1) \leq 28\%L_1 \\ L_1(1 - \frac{2}{a}) \leq 22\%L_1 \end{cases}$$

In the case of a coupled inductor when the magnetic coupling coefficient is in the range between $0.85 \leq k < 1$, the performance of the coupled is high and the losses are low. When the magnetic coupling coefficient $k < 0.7$, the losses of coupled inductor are increased and high.

The effects of parasitic capacitance, as shown in figure 7.4, will be on top side of the circuit which can be called Z_c. The equivalent impedance equation of the parasitic capacitance with Z_c is

as follows

$$Z_c eq = \frac{s^3 L_v L_s C_v + s(L_v + L_s)}{s^4 L_v L_s C_v C_p + s^2 (L_v + L_s) C_p + 1} \tag{7.5}$$

$Z_c eq$ is the equivalent impedance of π model including the parasitic capacitance and the generated negative capacitance. The generated capacitance can be determined through (7.5) when the parasitic capacitance value is known. C_p can be determined by using the analytical method proposed by [14], or through finding the total impedance when frequency is applied with various values by experimental results as shown in [27].

In order to increase the efficiency of the inductor by reducing C_p, the capacitance C of the additional small capacitor should be determined. C can be determined when the magnetic coupling coefficient value changes. The following equation is the equivalent impedance of the circuit including the parasitic capacitance and C to achieve more desirable cancellation for the inductor.

$$Z_{pc} = \frac{s^3 L_1^2 C(2a - g) + (sL_1 g)}{s^4 L_1^2 C C_p (2a - g) + s^2 L_1 (g C_p - C) + 1} \tag{7.6}$$

$$g = a + 2 \tag{7.7}$$

The relationship between the parasitic capacitance, magnetic coupling coefficient, and the adding small capacitor can be determined from (7.6). The following equation can determine the appropriate value of the added small capacitance based on the different values of magnetic coupling and the parasitic capacitance.

$$C = \frac{3k^2 + 1}{k^2} C_p \tag{7.8}$$

It can be observed from (8) that the additional small capacitor value varies as a function of the coupling coefficient. When the magnetic coupling have $k = 1$, the small capacitor value will be equal to four times the parasitic capacitance value. This result is same as the small capacitance value that was proposed in [32] for $k = 1$. C value is inversely proportional to the square k. However, the significance of this technique is that the value of a small capacitor is determined when the windings are not coupled perfectly. The ratio of the additional capacitor to the parasitic capacitance $\frac{C}{C_p}$ versus the magnetic coupling coefficient k is shown in figure 7.7. As shown from

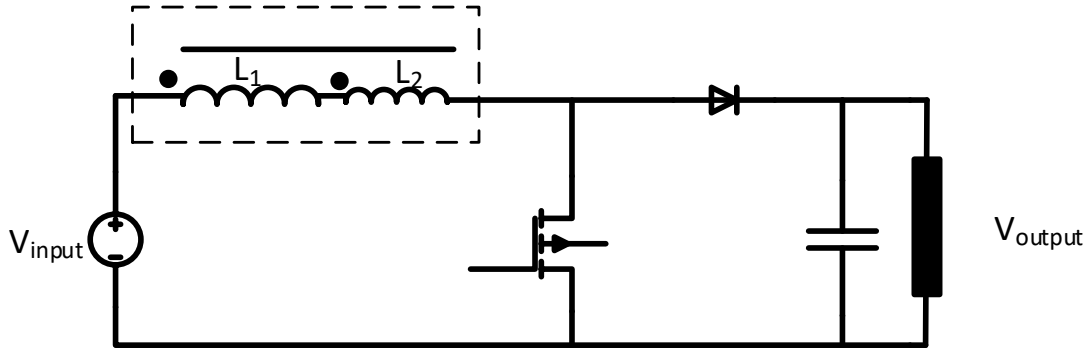


Figure 7.5: The boost converter with mutual inductance.

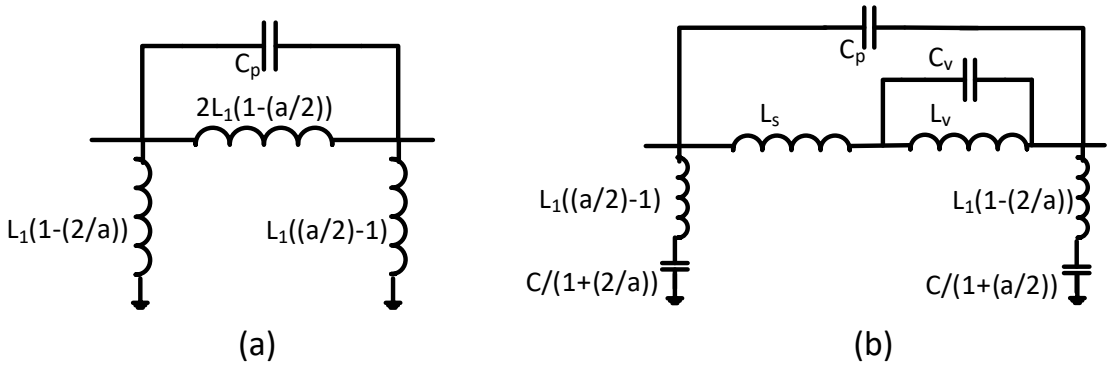


Figure 7.6: (a) The mutual inductance and magnetic coupling coefficient without additional capacitor. (b) The mutual inductance and magnetic coupling coefficient with additional capacitor.

the ratio of additional capacitor to the parasitic capacitance, the additional capacitor is various between $4C_p \leq C \leq 7C_p$ when the magnetic coupling is $0.5 \leq k$. When the magnetic coupling coefficient $k \leq 0.3$, the additional capacitor becomes more larger than 14 times of the parasitic capacitance in order to improve the efficiency of the coupled inductor. Therefore, the reduction of parasitic capacitance for an inductor can achieve the higher elimination and improve its efficiency.

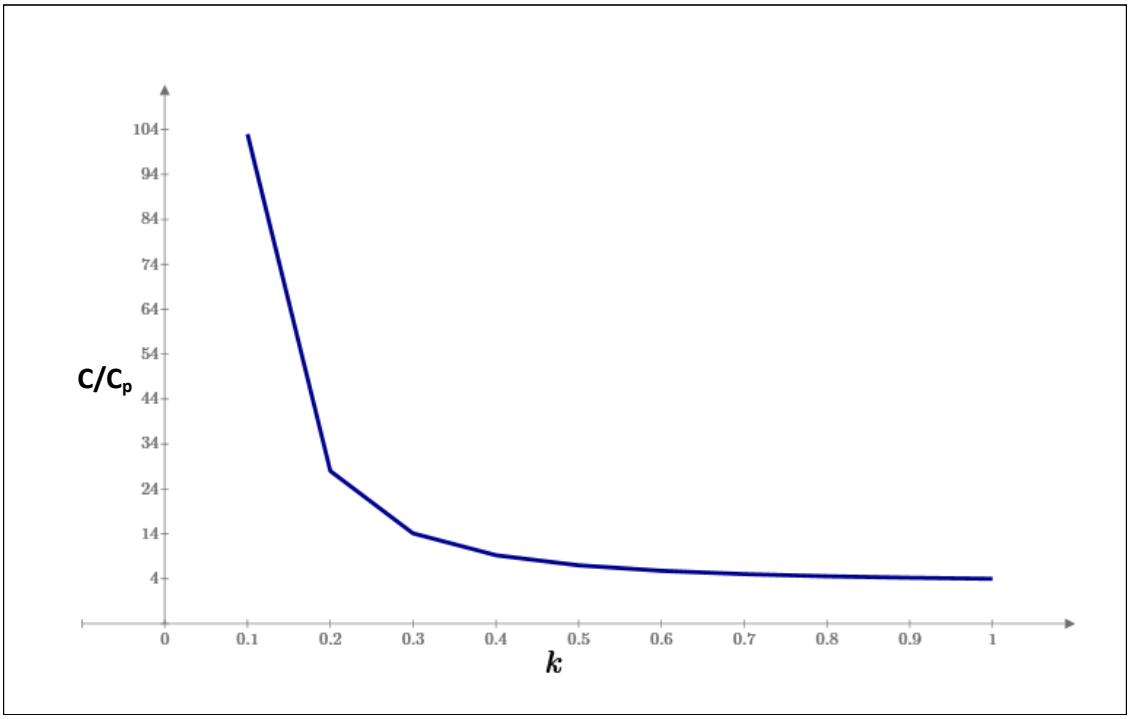


Figure 7.7: Ratio of additional capacitor to parasitic capacitance versus the magnetic coupling coefficient.

7.3 Experimental Results

The results of the parasitic capacitance reduction technique using the appropriate value of adding a capacitor for the mutual inductance and magnetic coupling coefficient of an inductor are presented in this section. The technique is first verified by MATLAB software, and subsequently validated by experimental work. The parasitic capacitance and impedance of the inductor are measured by 4396B network analyzer device. The value of the inductor is 303.07 μH that can provide a load of 1 kW for a boost converter as shown in figure7.5. The parasitic capacitance of the inductor was measured by the network analyzer which has 10.518 nF with 64 turns of the inductor. The magnetic core of the inductor is CM508060 MPP powder core. The toroidal core length is 127.3 mm with cross section area is 125.1μm^2.

Figure 7.6 (a) shows the two-winding coupled inductor that includes the parasitic capacitance of the total inductor in the π model. The magnetic coupling coefficient k is included in the model with various value of k. Figure 7.6 (b) shows the coupled inductor of two windings with including

the additional small capacitor in π model where the magnetic coupling k is not perfect.

In order to test the technique of reduction of the parasitic capacitance based on the magnetic coupling coefficient, two different models of coupled inductor with and without adding a small capacitor are applied with k. The results and performance of the coupled inductor are tested with $k = 0.97$ to network analyzer device and MATLAB software.

The additional small capacitor C is calculated depending on the magnetic coupling coefficient, which is $k = 0.97$, where $C = 43$ nF. Hence, the generated negative capacitance of the coupled inductor is $C_v = -10.09nF$.

The simulation results of reduction the parasitic capacitance technique are shown in figure 7.8. The inductance impedance is improved by using the technique of reduction C_p with appropriate value of C by around 42 dBΩ. The impedance of inductance is 14.8 dBΩ without the cancellation capacitor while the impedance value is improved to be 58.5 dBΩ when the reduction technique is applied. This means the parasitic capacitance is reduced and the inductor can store more energy and has better performance besides reducing the magnetic component size at high frequency.

Figure 7.9 shows the experimental results of the coupled inductor without using the capacitance reduction technique. The resonant frequency of the coupled inductor, at which the impedance of the parasitic capacitance is equal to the impedance of the inductance, is around $f_r = 3$ MHz. This shows the effects of the parasitic capacitance on the power electronics systems and how the losses will be increased at high frequencies. In order to improve the power of the power electronics system at high frequencies, the parasitic capacitance reduction technique is experimented to the coupled inductor. The resonant frequency is shifted from 3 MHz to 5.4 MHz as shown in figure 9. The improvement of the resonant frequency is resulted by choosing the appropriate value of the additional capacitor. The additional small capacitor in the experiment is approximated to be 50 nF. Therefore, the capacitance value of C_v can be calculated as $C_v = -11.83nF$.

The impedances of the inductor with different frequencies are shown in the Table. 1. The losses of the inductor are reduced when the parasitic capacitance reduction with appropriate additional capacitor is applied. The reduction of losses is around $80\% - 90\%$ for frequencies below the first

Table 7.1: Results of the inductor impedances.

Frequency Hz	$\|Z\|$ without C Ω	$\|Z\|$ with C Ω
200	410.51	31.399
300	620.14	69.993
400	831.83	135
500	1.0476k	191.19
600	1.271k	243.9
600	1.4969k	295.06
800	1.7387k	345.35
900	2.0279k	396
1000	2.265k	446.63
2000	6.7408k	1.0165k
3000	46.424k	1.8731k
4000	11.862k	3.7003k
5000	6.0181k	30.57k

resonant frequency of inductor without adding a small capacitor. The resonant frequency of the inductor is shifted by around 80% more than the original resonant frequency when the parasitic capacitance technique applied. This means the inductor with applying this technique can increase storing the energy for 80% more than the inductor without parasitic capacitance reduction.

The significance of this technique lies in increasing the performance and energy storage of the inductor under the first resonant frequency. Also, the size of the inductor can be reduced without compromising its performance.

By sizing the value of a small capacitor based on the magnetic coupling value of the mutual inductance, the reduction of C_p will be more effective. Thus, the inductor can work with higher efficiency at high frequencies. Also, the losses of an inductor can be reduced.

7.4 Conclusion

In this chapter, a technique for improving the inductor performance at high frequency with imperfect coupled windings by reducing the effects of parasitic capacitance has been proposed. This technique uses additional a small capacitor to be inserted into the mutual coupling of the inductor. There is a leakage inductance due the two coupled windings of the inductor.

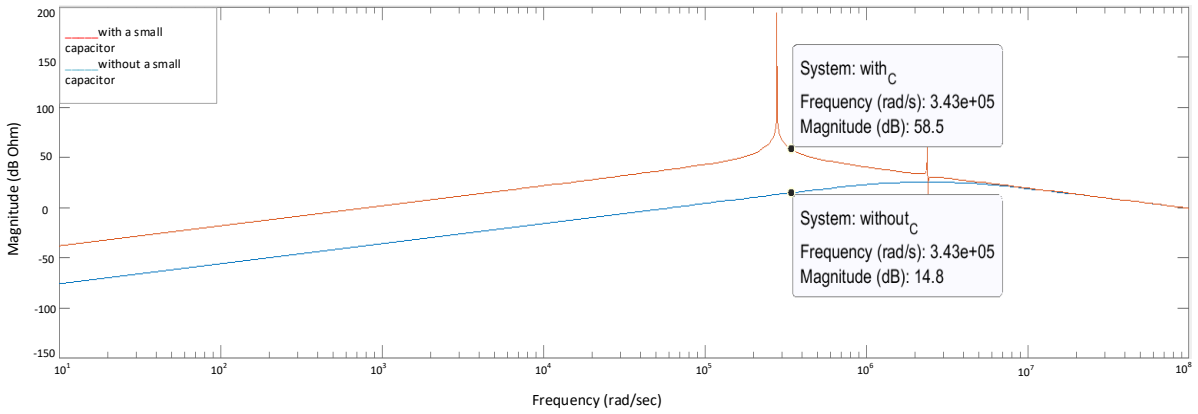


Figure 7.8: The bode diagram of comparison between with and without additional capacitor when $k = 0.97$

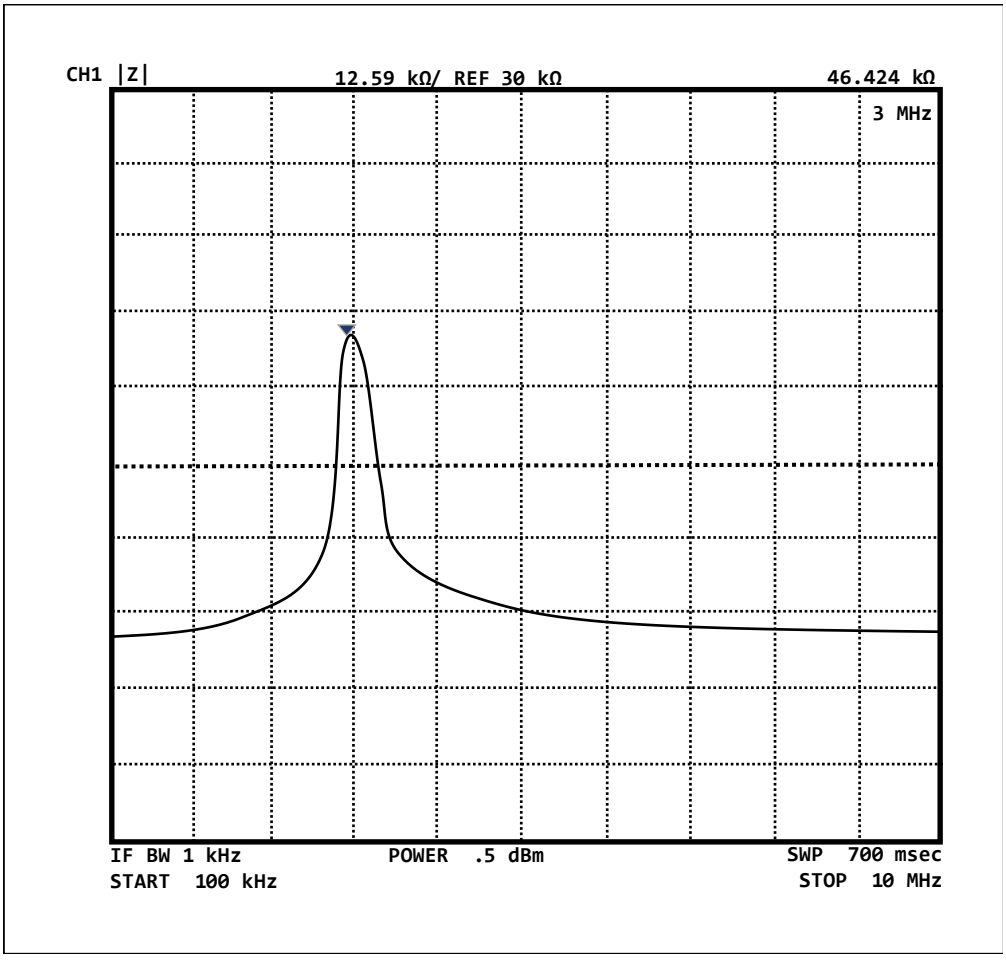


Figure 7.9: The Network Analyzer results of the coupled inductor without applying the parasitic capacitance cancellation.

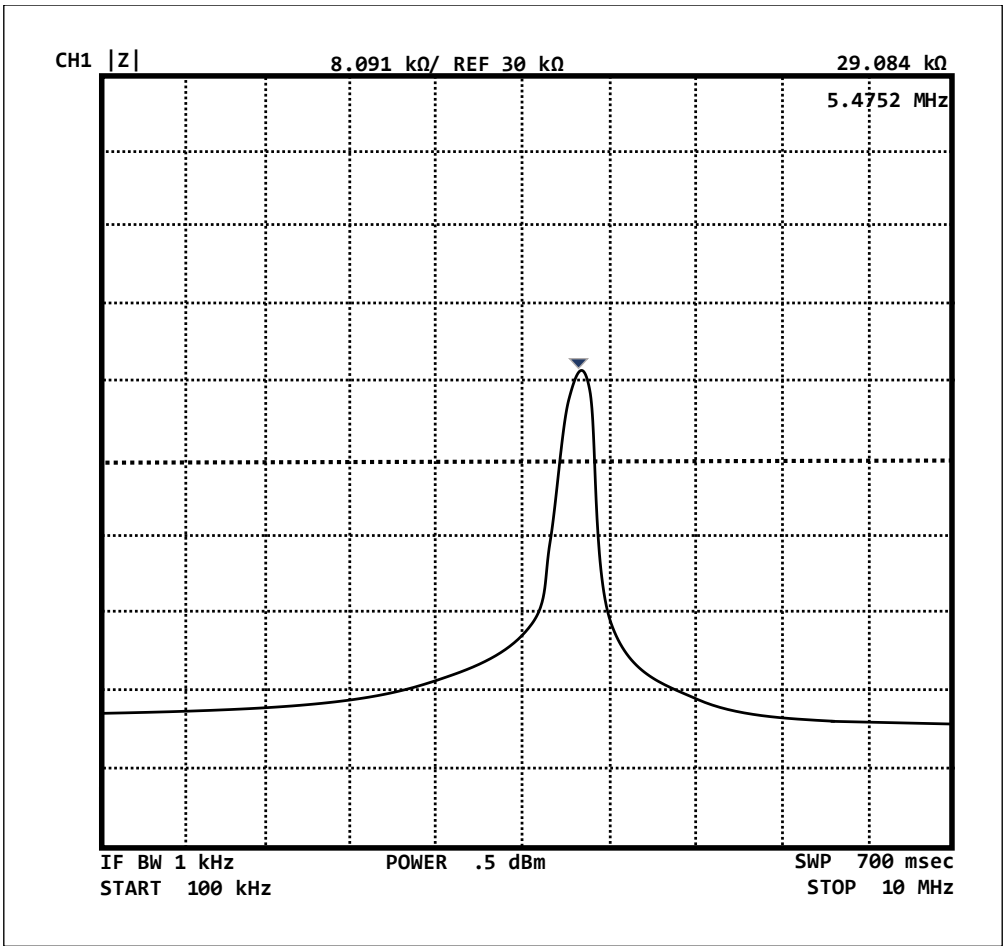


Figure 7.10: The Network Analyzer results of the coupled inductor with applying the parasitic capacitance cancellation.

Therefore, this technique represents a π model for the coupled windings with leakage inductance. The technique adds an additional small capacitor in order to have the higher parasitic capacitance reduction for the inductor. Another feature of this technique is the new method to calculate the value of the additional small capacitor based on the magnetic coupling coefficient of the inductor.

This technique shows improvement for inductor performance at frequencies below the first resonant of inductor by increasing the value of inductance impedance about 40 dBΩ depending on the magnetic coupling value. The reduction of parasitic capacitance by choosing the appropriate additional capacitor causes improvement in the inductance performance, which increases the ability of storage energy of the inductor, as shown in the results of the experiment and simulation. The inductor characteristic is changed and improved by adding the right capacitance when $k = 0.97$.

The resonant frequency of the inductor is increased to be at 5.4 MHz from the original resonant frequency which is 3 MHz. By using this technique, the inductor can be designed based on the magnetic coupling value besides the frequency and size to have a better performance.

Acknowledgment

Special thanks for Mr. Brian Wright who is Supervisor of Electrical and Computer Engineering Technical Services at Michigan State University. The experimental results could not be done without his help.

CHAPTER 8

SELECTING THE OPERATING FREQUENCY OF MAGNETIC COMPONENTS FOR DC-DC CONVERTER

To achieve a higher efficiency for the power converter at high operating frequency, the parasitic capacitance of the magnetic components should be estimated by using the proposed method which has more realistic for determining the parasitic capacitance than existing methods. The size of the power converter with magnetic components can be reduced with maintaining the efficiency at high operating frequency by designing the power converter based on the parasitic capacitance estimation.

8.1 Introduction

Magnetic components such as inductors and transformers are some of the main components in the electrical and electronic systems [16, 47]. The size and volume of the magnetic components play an important role in the weight of electric and electronic devices [4, 7, 9]. One of the main issues of automotive applications is the size of the power-train besides the electric losses.

The power-train of the automotive applications contains power converters. The volume and size of the power converter can be reduced significantly by downsizing the magnetic components [7]. The size of magnetic components such as the inductor can be reduced by two methods that are selecting the suitable magnetic core material and increasing the operating frequency [3, 4].

The magnetic core material can downsize the volume and size of the inductor by selecting higher core permeability with smaller volume such as Ferrite material. However, the magnetic core losses are high besides having lower flux density saturated for this type of material [2].

Another method to reduce the size and volume of the inductor is to increase the operating frequency. By increasing the operating frequency, the volume and number of turns of the inductor can be decreased. However, the losses of the magnetic core and conductor increase with increasing the operating frequency. Therefore, a new methodology of selecting the highest operating frequency

with the smallest size and volume while maintaining the efficiency of the inductor is needed.

In this chapter, the process of selecting the highest possible operating frequency of the inductor is presented. Moreover, the compromising between the magnetic core size, the number of turns, and the operating frequency are developed to reduce the total losses of the magnetic components. The volume of the inductor can be reduced by 70% with the same magnetic core material by using the new methodology.

8.2 Methodology

The low power density typically has negative impact on the power electronic systems. One of the effective methods to reduce the volume of the power converter is by increasing the operating frequency. However, increasing the operating frequency leads to increased power losses on the converter and especially on the magnetic components [3, 47, 48].

The power losses of the magnetic components such as inductors can be divided into two parts: the magnetic core losses and the windings losses [3]. However, the tradeoffs between the magnetic core volume, the power losses, and the operating frequency should be considered for designing the converter. The new methodology of properly selecting the high operating frequency with maintaining the efficiency of the inductor is presented in this section.

In order to design an inductor with a suitable range of operating frequency, the conventional inductor designed for a power converter is required to be modified. The conventional inductor can be designed by using the well-known inductor design methods for converter [3, 56]. By having the conventional inductor, the parameters to design a smaller inductor with maintaining the efficiency should be extracted. The required parameters from the conventional inductor are the parasitic capacitance, the power losses of both conductor and magnetic core, and the magnetic core material. Other parameters to design the new inductor are the limitation of the frequency of the selected core material that the permeability is stay constant, the switch limitation, and the selected bobbin material.

Fig. 8.1 shows the flowchart process of selecting the operating frequency range of power

converter. Each step of selecting the operating frequency are explained as the following.

8.2.1 Resonant Frequency

One of the main problems of the inductor with increasing the operating frequency is the more pronounced effect of parasitic capacitance. Many issues can be caused by the parasitic capacitance such as electromagnetic interference, and overshot voltage and current [16, 20, 21]. Moreover, the resonant frequency of the inductor occurs when the parasitic capacitance canceled out the inductance value. Therefore, it is essential to estimate the parasitic capacitance of the inductor.

The parasitic capacitance of the inductor can be estimated by several techniques [21]. The parasitic capacitance can be calculated by estimating turn-to-turn capacitance, layer-to-layer capacitance, and turn-to-core capacitance [16, 21, 43]. Besides the analytical methods of calculating the parasitic capacitance, the electrostatic model simulation with finite element analysis can estimate the parasitic capacitance of the inductor. The method of calculating the parasitic capacitance as explained in [43] are shown in (8.1) and (8.2).

$$C_{tt} = \epsilon_o l_t \int_0^{\frac{\pi}{6}} \frac{1}{1 + \frac{1}{\epsilon_r} \ln \frac{2r_o}{2r_c} - \cos(\theta)} d\theta \tag{8.1}$$

$$C_s(n) = \frac{C_{tt}}{2 + \frac{C_{tt}}{C_s(n-2)}} + C_{tt} \tag{8.2}$$

where the turn-to-turn capacitance is represented by C_{tt} while the total capacitance is $C_s(n)$. The number of turns of the inductor is n. The permeativity of the space and the relative material are ϵ_o and ϵ_r, respectively. The radius of the conductor without and with the coating are r_c and r_o, respectively. The length of the turn is represented by l_t.

Therefore, it is necessary to select the first range of the operating frequency based on the resonant frequency. Hence, the parasitic capacitance of the conventional inductor should be determined in order to find the resonant frequency. The base-range of the operating frequency of the power converter should not exceed the resonant frequency of the conventional inductor. The resonant

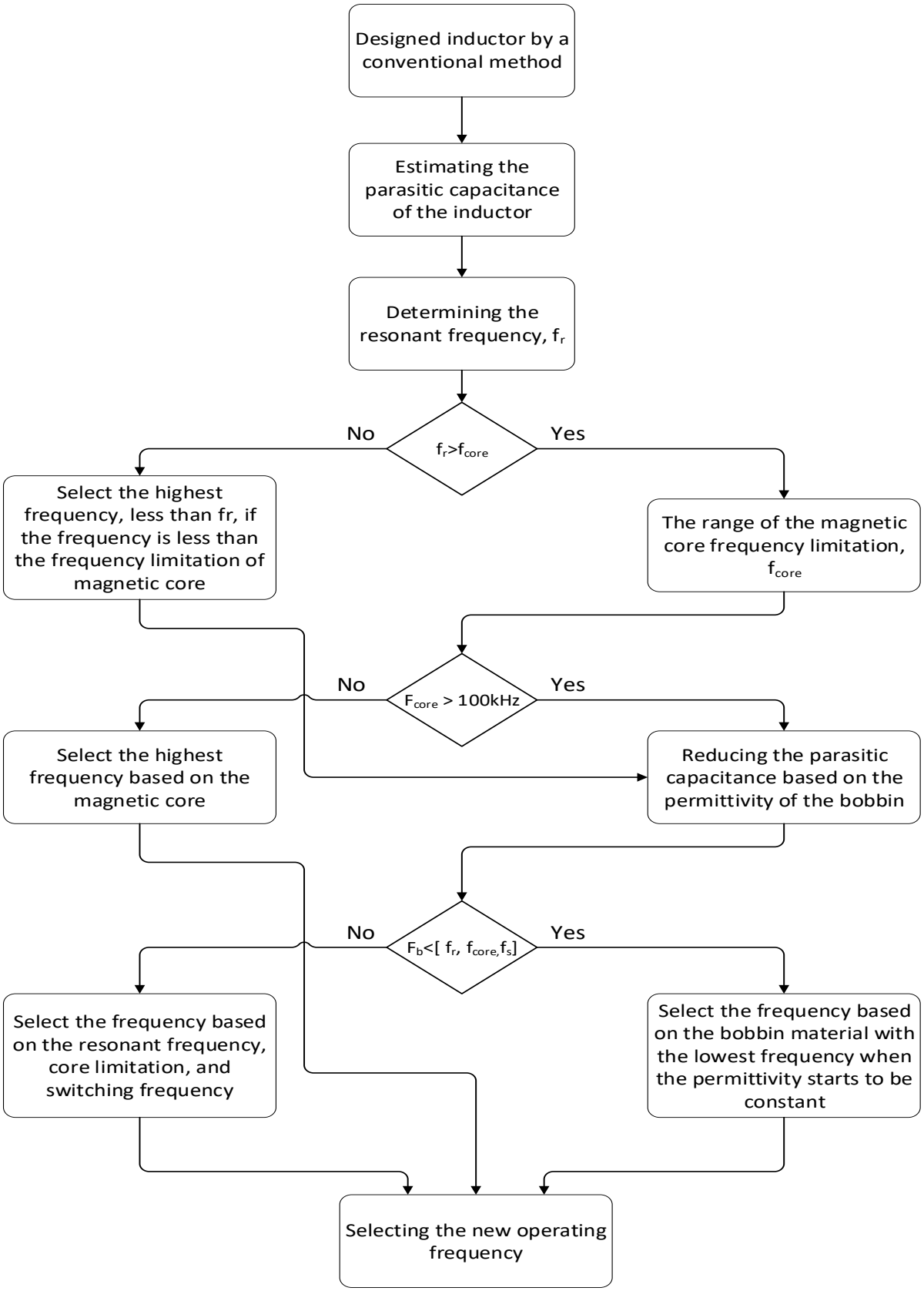


Figure 8.1: The flowchart process of selecting the operating frequency range.

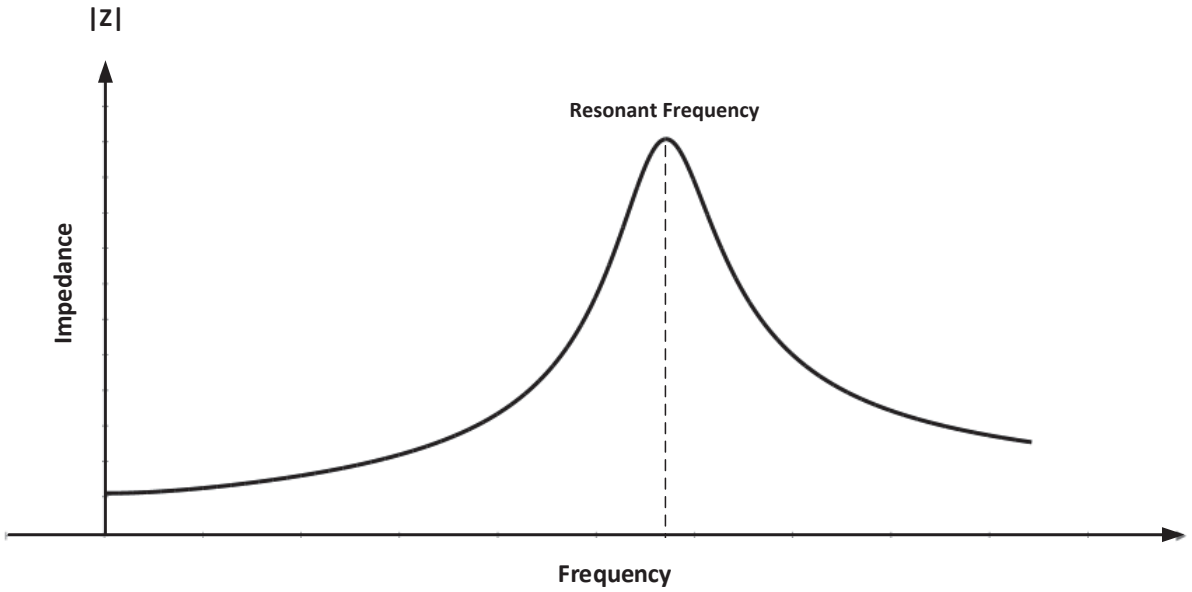


Figure 8.2: The inductor behavior with increasing the operating.

frequency of the conventional inductor is represented by f_{rc}. Fig. 8.2 shows the behavior of the inductor with increasing the operating frequency.

The first range of the operating frequency should be higher than the conventional inductor frequency and below the resonant frequency. The conventional inductor frequency is represented by f_{ci}. The first range of the operating frequency is represented by f_{1stra}.

$$f_{ci} < f_{1stra} < f_{rc} \tag{8.3}$$

Therefore, the following operating frequency ranges should be within the limitation of the first range.

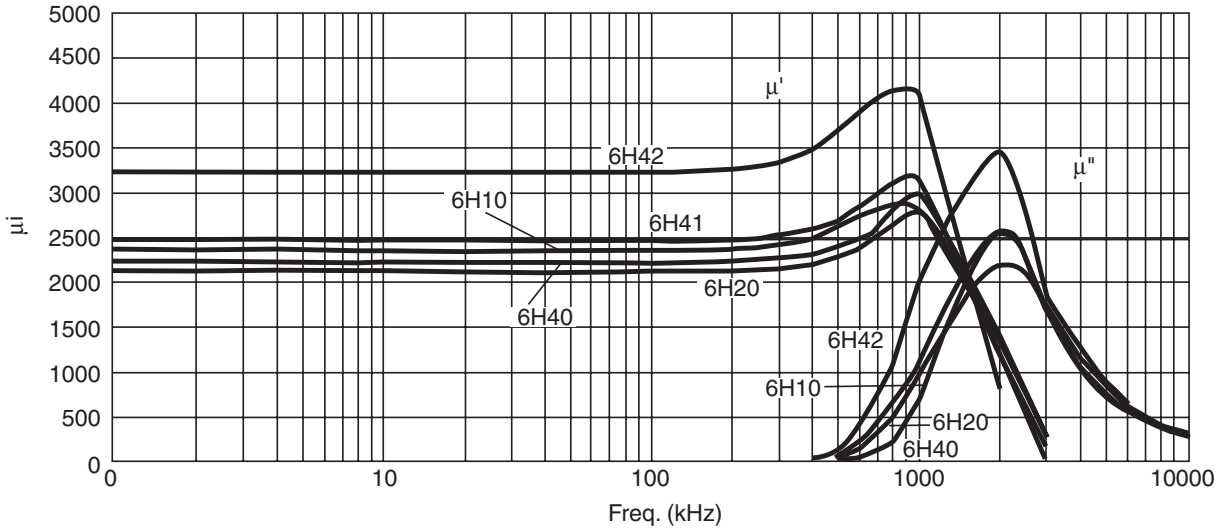


Figure 8.3: The permeability curves of different magnetic core materials versus frequency.

8.2.2 Magnetic core frequency range

The magnetic core is the main part of the inductor in the power converter. Therefore, it is important to consider the limitation of the magnetic core regarding the operating frequency. One of the important parameters of the magnetic core is the permeability.

The permeability of the magnetic core can be changed based on the frequency range. When the operating frequency increases above a certain frequency, the permeability reduces. Then, the power losses increases when the permeability reduced. This phenomenon is characterized by the complex permeability [41, 57–59]. Fig. 8.3 shows the curves of different materials permeability versus frequency where $6H10$ to $6H42$ are different materials of the magnetic core [60]. The complex permeability can be explained by the following equations where $\mu^* = \mu^{'} + j\mu^{"}$. The complex permeability is μ^* [57].

$$\mu^{'} = \frac{L_s}{L_o} \tag{8.4}$$

$$\mu^{"} = \frac{R_s}{\omega L_o} \tag{8.5}$$

where the self-inductance with magnetic core is represented by L_s. The air-core equivalent inductance, which is calculated from the space permeability, is represented by L_o while the resistance of the coil is R_s.

To maintain the performance of the inductor, the operating frequency of the inductor should be within the frequency range that the permeability stays constant. The maximum frequency of the magnetic core, which the permeability stays constant, represented by f_{cp}. Hence, the operating frequency should not exceed the maximum core frequency. Then, the second range of frequency f_{2ndra} is shown in (8.6).

$$f_{ci} < f_{2ndra} < f_{cp} \tag{8.6}$$

The second range of frequency f_{2ndra} should be within the first frequency range f_{1stra}. However, if the second frequency range is greater than the first frequency range, the only operating frequency that should be chosen is the first frequency range.

$$f_{ci} < f_{2ndra} \leq f_{1stra} \tag{8.7}$$

8.2.3 The frequency limitation of the electronic switch

The switch devices are the main part of the power electronics systems [3, 56]. The switches can be made from different materials. Each material has different characteristic and limitation for frequency, voltage, and current. Fig. 8.4 shows the switches capabilities for voltage, current, and frequency [3].

Therefore, it is necessary to consider the operating frequency range depending on the frequency limitation of the switch. The third range of the operating frequency, is f_{3rdra}, should be less than the switching frequency limitation. The switching frequency is represented by f_s.

$$f_{ci} < f_{3rdra} < f_s \tag{8.8}$$

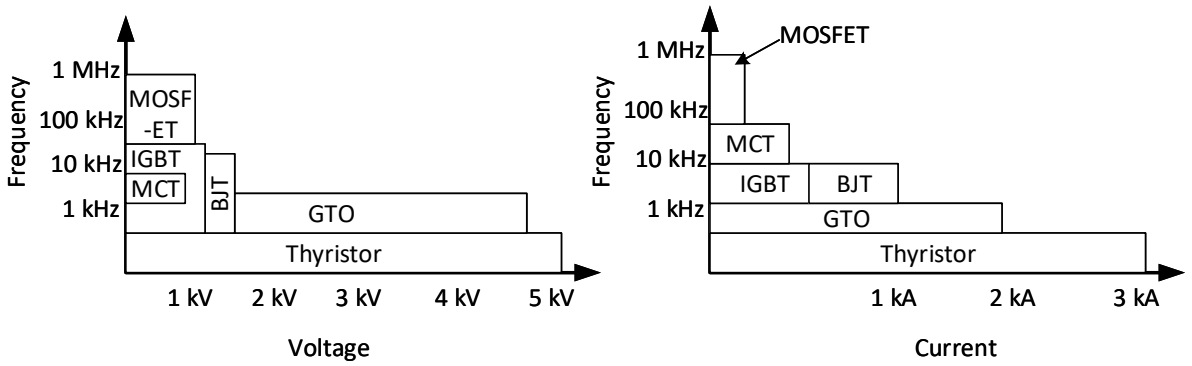


Figure 8.4: The voltage and current versus frequency for different switches.

The third range of the operating frequency should be within the first two ranges. If the third range of the operating frequency is less than the first two ranges, the operating frequency should be considered based on the third frequency range.

$$f_{ci} < f_{op} \leq f_{3rdra} \leq f_{2ndra} \leq f_{1stra} \tag{8.9}$$

If the third range of the operating frequency is greater than the first two ranges, the operating frequency should be considered based on the first two frequency ranges. Therefore, the range of the new operating frequency, which represented by f_{op}, is shown next.

$$f_{ci} < f_{op} \leq f_{2ndra} \leq f_{1stra} \leq f_{3rdra} \tag{8.10}$$

The highest operating frequency of the power converter, which reduces the size and volume of the inductor while it maintains the power efficiency of the inductor, can be properly selected. The new operating frequency should be chosen within all the frequency ranges.

8.3 Selecting the magnetic core size and number of turns

In order to have the smallest magnetic core possible with maintaining the efficiency of the inductor, the tradeoffs between the number of turns and the core size should be properly studied. The number of layers of the inductor with magnetic core have effects on the inductor efficiency by

increasing the losses [3, 61]. Therefore, a single-layer inductor with magnetic core is the optimum design to reduce the eddy current losses of the conductor.

The conductor of an inductor has two types of eddy current losses. The skin effect and the proximity effect are the AC losses of the conductor [3, 47, 48, 61]. The skin effect losses are increased with increasing the frequency while the proximity effect losses are increased by two factors. The short distance between the turns increases the proximity effect losses. Therefore, the longer distance between turns can reduce the losses of the proximity effect. Another factor of increasing the proximity effect losses is the number of layers of the coil winding. By increasing the number of layers, the AC losses of the conductor are increased [3, 61]. Hence, the single-layer inductor has the lowest AC losses that caused by the proximity effect. The total AC power losses is represented by $P_{ACLosses}$ while the proximity power losses and the skin effect power losses are $P_{Proximityeffect}$ and $P_{Skineffect}$, respectively.

$$P_{ACLosses} = P_{Proximityeffect} + P_{Skineffect} \tag{8.11}$$

Another type of conductor losses is the DC loss [3, 47]. The DC loss of the conductor is mainly depending on the conductor length L_{endc} and the resistivity of the conductor ρ.

$$R_{wdc} = \frac{\rho L_{endc}}{area} \tag{8.12}$$

$$P_{DCLosses} = R_{wdc} I_L \tag{8.13}$$

where the DC power losses of the conductor is represented by $P_{DCLosses}$. The winding DC resistance and the inductor current are R_{wdc} and I_L, respectively.

The DC losses of the conductor of the inductor for specific material can be reduced by two methods. Changing the size of the core can lead to reduce the DC loss by reducing the length of the conductor. Another method to reduce the dc losses is by increasing the operating frequency. The inductor value reduced with increasing the operating frequency which leads to reducing the

number of turns and the length of the conductor. Therefore, the tradeoffs between the number of turns and the size of the magnetic core at the new operating frequency should be properly selected.

The inductor with the smallest size possible with maintaining its efficiency can be made with the compromising between the core size, the number turns, and operating frequency. Beside selecting the highest operating frequency that is within the previous frequency ranges, the size of magnetic core and the number of turns can be properly chosen. Fig.8.5 shows the flowchart process of compromising between the number of turns and the magnetic core size after choosing the operating frequency.

To achieve the lowest conductor losses of the inductor, the inductor should be designed based on a single-layer with magnetic core. Moreover, increasing the distance between the turns leads to less losses of the conductor. On the side of the magnetic core, selecting smaller volume of the magnetic core can reduce the losses of the magnetic core [3]. The relation between core losses and the volume is shown in 8.14.

$$P_H = f_{op} A_c l_m \int_{onecycle} H dB \tag{8.14}$$

where the term $A_c l_m$ is the volume of the magnetic core. The operating frequency is f_{op} while the hysteresis power represented by P_H.

As a result, the inductor with the small size while maintaining its efficiency is achieved by following this methodology.

8.4 Experiment and Result

To verify the method of selecting the operating frequency for the magnetic components, two different type of magnetic core materials are selected to design inductors with magnetic cores. The first chosen magnetic core is $00k5527U026$ with Kool Mu Powder core. The Kool Mu Powder core has many advantages such as high flux density saturated, low core losses, and air-gap distributed [2, 62]. The limitation of the Kool Mu Powder core frequency, which its permeability stays constant, depends on the size and the permeability value. The limited frequency of the chosen

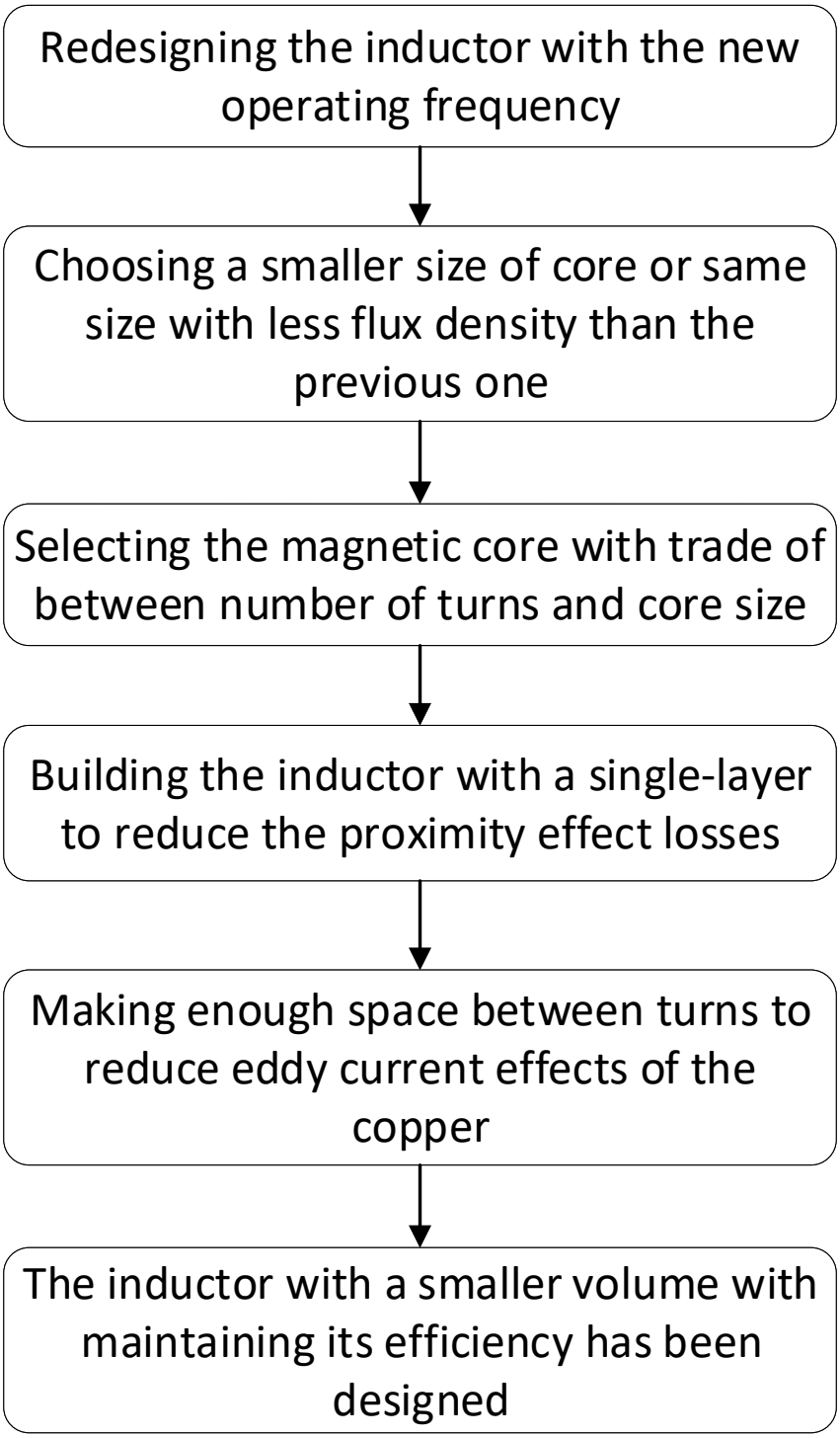


Figure 8.5: The flowchart process for selecting the appropriate number of turns and the volume of the new inductor.

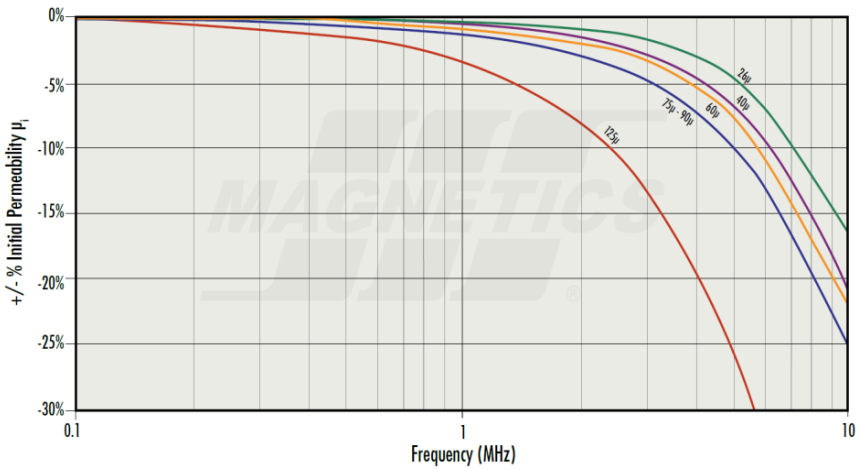


Figure 8.6: The Kool Mu powder core permeability versus the frequency [2].

core is $2MHz$ as shown on the figure 8.6 [2].

Designing the inductor by using the conventional method is a first stage. The selected operating frequency of the conventional inductor is $20kHz$. Table 8.1 shows the parameters of the inductor of the boost converter.

Table 8.1: Parameters of the Boost converter.

Parameter	Value
Input voltage, V_{in}	50 V
Output voltage, V_{out}	80 V
Output power, P_{out}	300 W
Duty ratio, D	37.5%

By using the conventional method, the inductor is designed with multi-layer winding. The powder core dimensions are shown in Fig. 8.7. Fig. 8.7 (a) is the magnetic core dimensions of the conventional inductor with 20 kHz while (b) is the dimensions of the magnetic core with the new operating frequency which is 100 kHz. The inductor has 133 turns with AWG 22 conductor for the conventional inductor. The volume of the magnetic core is 28.9 cm^3. The power losses of the core and windings are 96.757 mW and $4.927 * 10^3$ mW, respectively, at $20kHz$. Therefore, the total power losses of the inductor is 5.024 W which is calculated by using [47].

The parasitic capacitance of the conventional inductor can be estimated by the method in [18].

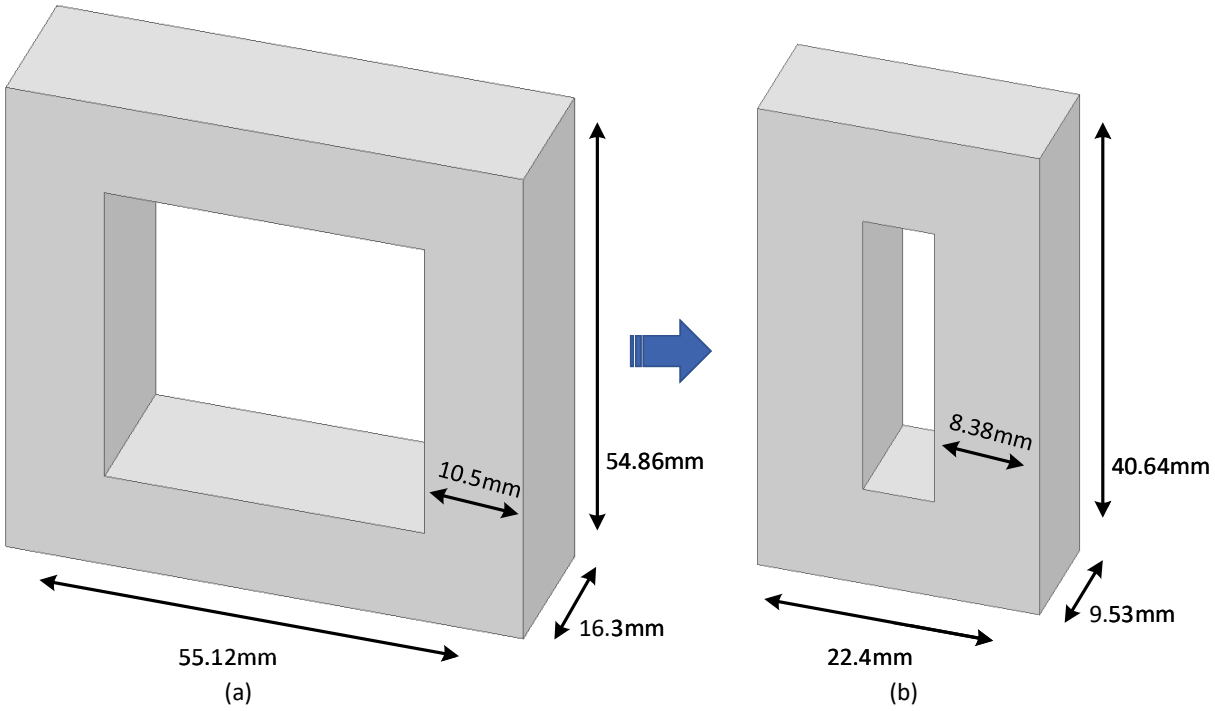


Figure 8.7: (a) The magnetic core dimensions of the conventional inductor, (b) The magnetic core dimensions of the new inductor.

The parasitic capacitance is 93 pF. Therefore, the resonant frequency of the conventional inductor can be determined by knowing the parasitic capacitance C_p and the inductance value L.

$$f_r = \frac{1}{2\pi\sqrt{LC_p}} \tag{8.15}$$

where the resonant frequency is represented by f_r. Hence, the resonant frequency of the inductor with 521 μH is 721.8 kHz. The operating frequency range should be less than both the resonant frequency and the magnetic core frequency as shown next.

$$20kHz < f_{op} < f_r = 721kHz < f_c = 2MHz \tag{8.16}$$

The MOSFET device with $RD3P100SNFRA$ is selected to be the switch of the power converter. The switching frequency of the MOSFET is selected to be 100 kHz to maintain the efficiency of the MOSFET. Therefore, the highest operating frequency for the inductor and converter is selected to be $100kHz$.

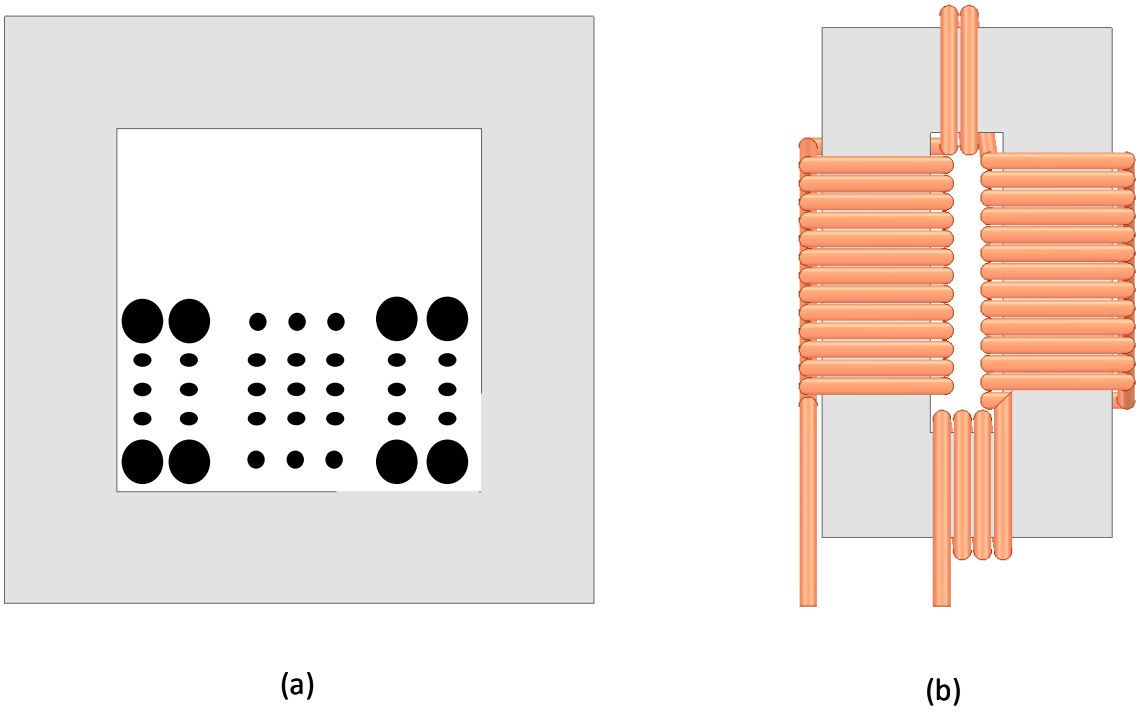


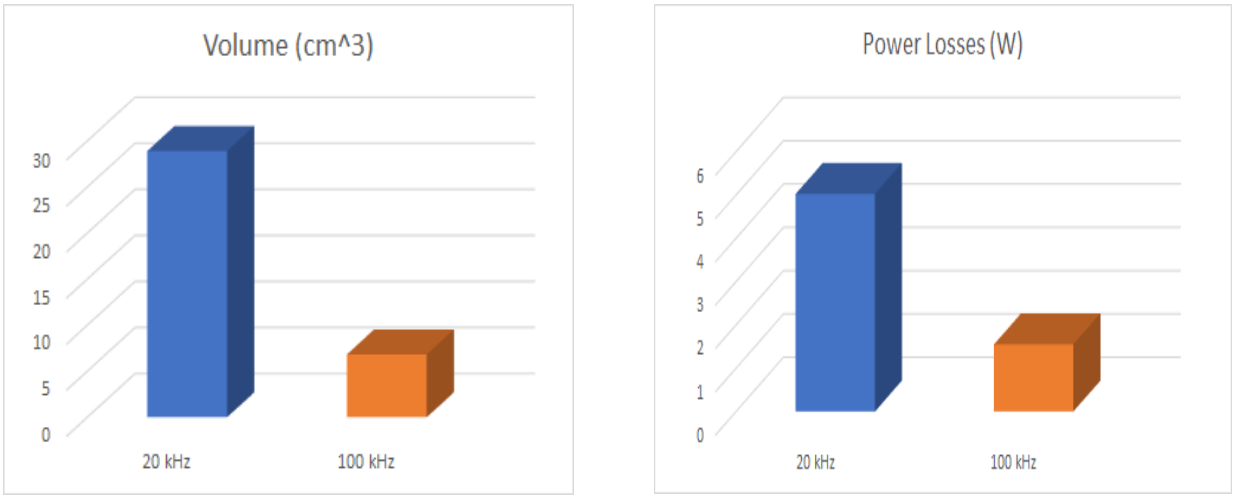
Figure 8.8: (a) The conventional inductor with milt-layer. (b) The new inductor with a single-layer.

Therefore, the new inductor value with 100 kHz is 104.2 μH. The geometry and size of the new magnetic core is shown in Fig. 8.7. The volume and number of turns are 6.82 cm^3 and 33 turns, respectively.

The power losses of the core and the winding at $100kHz$ are 708.994 mW and 842.39 mW, respectively. Hence, the total power losses of the inductor is 1.551 W. The new inductor design comparing with the conventional inductor is shown in Fig. 8.8 where (a) is the conventional inductor and (b) is the new inductor.

Fig 8.9 (a) shows the comparison between the conventional inductor volume and the new inductor volume while (b) shows the power losses of both inductors. As a result, the inductor volume is reduced by around 70% with increasing the operating frequency. Moreover, the efficiency of the inductor is increased by 69.1% while the size is reduced.

The other material that is selected to verify the method is the Ferrite core material. The ferrite core with N49 material has 200 kHz of the frequency core limitation [60]. The volume of the



(a) (b)

Figure 8.9: (a) The volume comparison between the conventional inductor and the new inductor. (b) The power losses of both the conventional inductor and the new inductor.

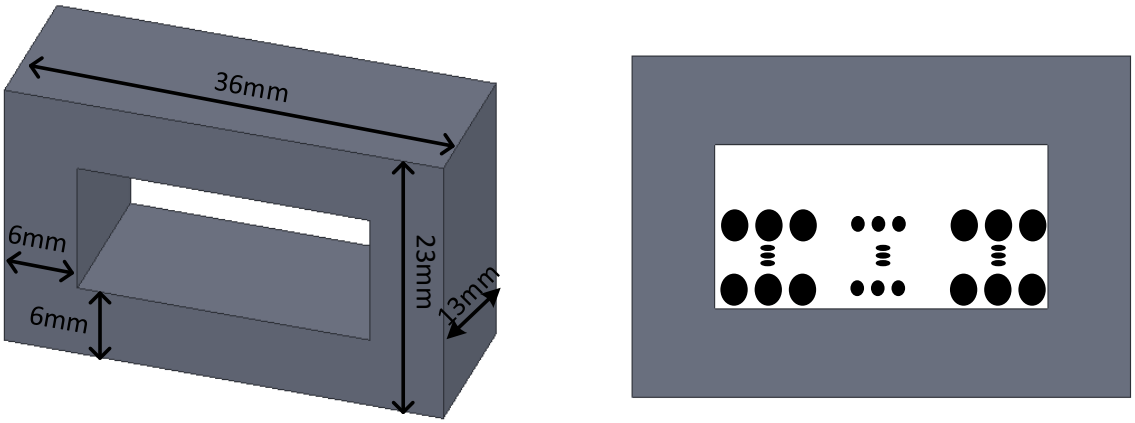


Figure 8.10: The conventional inductor with milt-layer and N49 Ferrite core.

selected core with 20 kHz operating frequency is 7.176 cm^3 with 91-turn.

Figure 8.10 shows the geometry dimensions of the N49 Ferrite core. The permeability of the inductor is 1500 with resonant frequency 580 kHz. Therefore, The selected operating frequency should not exceed both frequency of the core limitation and the resonant frequency. The selected operating frequency is 100 kHz which is same the operating frequency of the previous experiment to compare between the results.

Figure 8.11 shows the new inductor of N49 ferrite core material with dimensions. The number

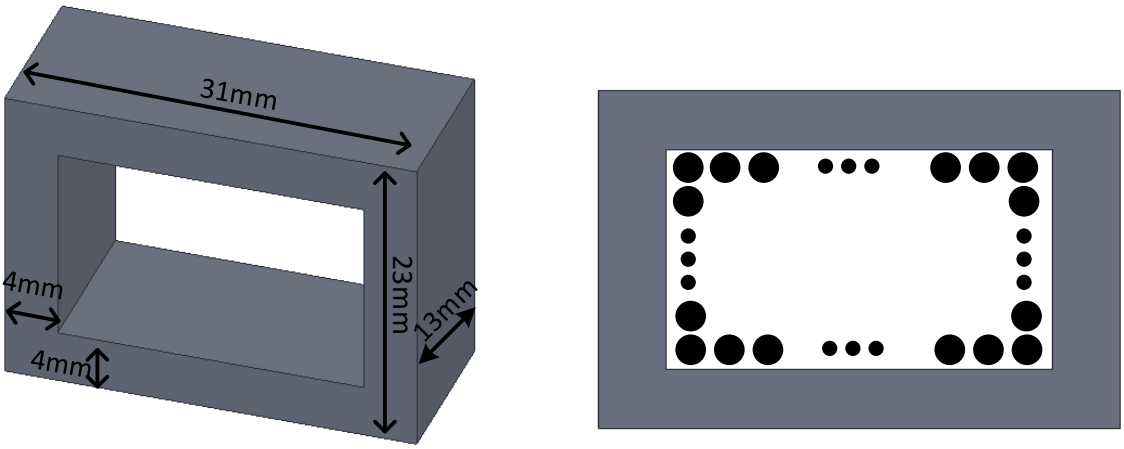
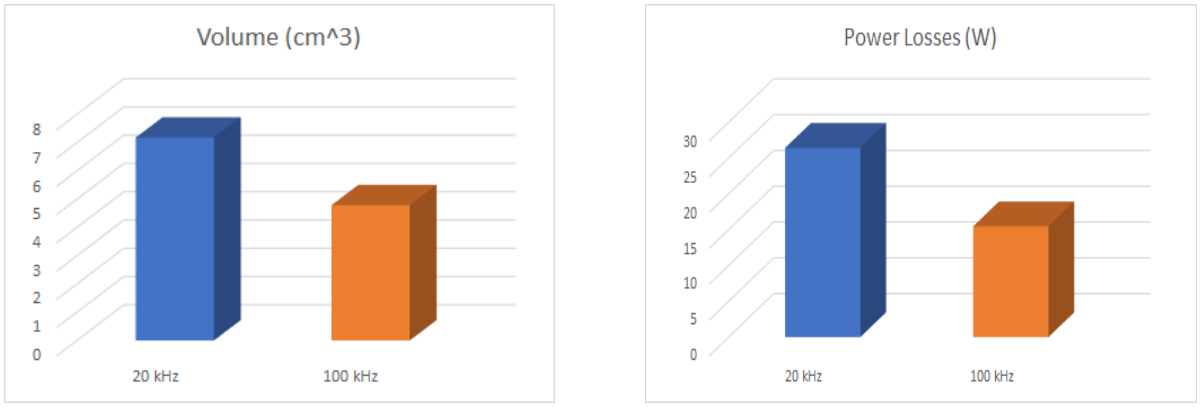


Figure 8.11: The new inductor with a single-layer and N49 Ferrite core.



(a) (b)

Figure 8.12: (a) The volume comparison between the conventional inductor and the new inductor. (b) The power losses of both the conventional inductor and the new inductor.

of turns of the winding are reduced to be 42-turn with single-layer. The volume of the new inductor is reduced by 33% which is 4.874 cm^3 of the new inductor.

Figure 8.12 shows the total losses comparisons of the two inductor with N49 ferrite core. 8.12 (a) shows the comparison between the conventional inductor volume and the new inductor volume while (b) shows the power losses of both inductors. The total losses with applying the proposed methodology with N49 ferrite core is reduced by 41.4%.

8.5 Conclusion

This paper introduces a new methodology to properly choose the highest operating frequency for the magnetic components with maintaining its efficiency. Several important parameters belong to the magnetic components are considered to select the operating frequency.

The complex permeability, the magnetic core material, and the volume of the magnetic core are the consideration parameters of the magnetic core to select the operating frequency with downsizing the magnetic components.

The losses of the conductor, which are skin effect, proximity effect, and DC resistance, are the important parameters to minimize the losses.

The parasitic capacitance and the resonant frequency are the essential parameters of the magnetic components to properly select the highest operating frequency with avoiding the electromagnetic interference and overshot voltage and current.

CHAPTER 9

INTERLEAVED COUPLED INDUCTORS

To achieve a higher efficiency for the power converter at high operating frequency, the parasitic capacitance of the multi-phase inductors should be estimated by using the proposed method which has more realistic for determining the parasitic capacitance than existing methods. The size of the power converter with multi-phase inductors can be reduced with maintaining the efficiency at high operating frequency by designing the power converter based on the parasitic capacitance estimation.

9.1 Estimating the Parasitic Capacitance of Two-Phase Inductors

Recently, many researches focused on environmental issues such as the depletion of energy resources and global warming. Therefore, programs of energy-saving and the use of high-efficient and alternative technologies have become relevant topics in many areas of our daily life [4, 7]. The transportation systems are one of the major energy consumptions such as electric vehicle (EV), and hybrid electric vehicle (HEV) [4, 7–9, 36–38]. The losses and size of the electric power-train for EV and HEV are one of the major issues for automotive applications [4, 7–9, 36–38]. In order to reduce the losses and the volume of EV, the losses of the power-train should be reduced. The technique of downsizing the power-train in EVs is done by reducing the size and volume of the DC-DC boost converter, which is located between the storage unit and the motor inverter [4, 7–9, 36–40].

The size of the DC-DC boost converter can be reduced by using the technique of coupling inductors which provides a high-power density [4, 6, 7, 37, 38, 38, 63]. Figure 9.1 shows different topologies of two-phase coupled inductors for boost converters. However, the parasitic capacitance of two-phase interleaved coupled inductors should be estimated in order to increase the reduction of the sizes of converters by increasing the switching frequency. The reduction of the size of the power converter can be represented by reducing the capacitors. By estimating the parasitic capacitance of the coupled inductor by the proposed method, the ability of increasing the operating

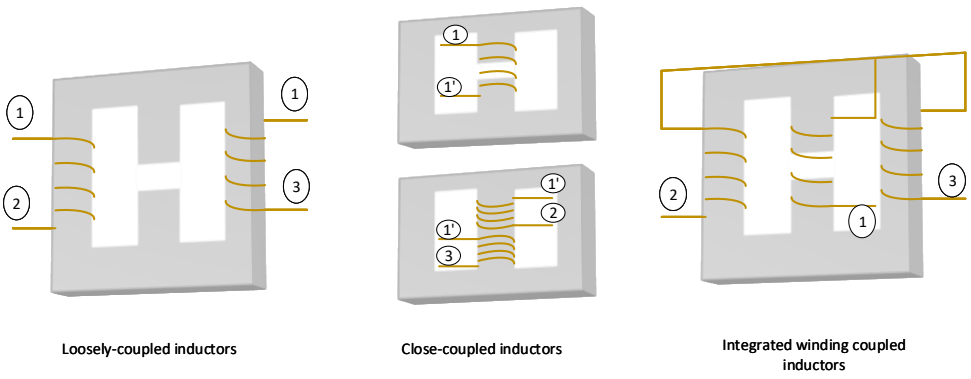


Figure 9.1: Different types of two-phase coupled inductors.

frequency can be done without reaching the resonant frequency which causes the over-voltage and current overshot besides the electromagnetic interference. Hence, two types of interleaved coupled inductors for the boost converter, which are considered to have high efficiency [4], are chosen to estimate the parasitic capacitance. The two types of interleaved coupled inductors are loosely coupled inductor (LCI) and closed coupled inductor (CCI).

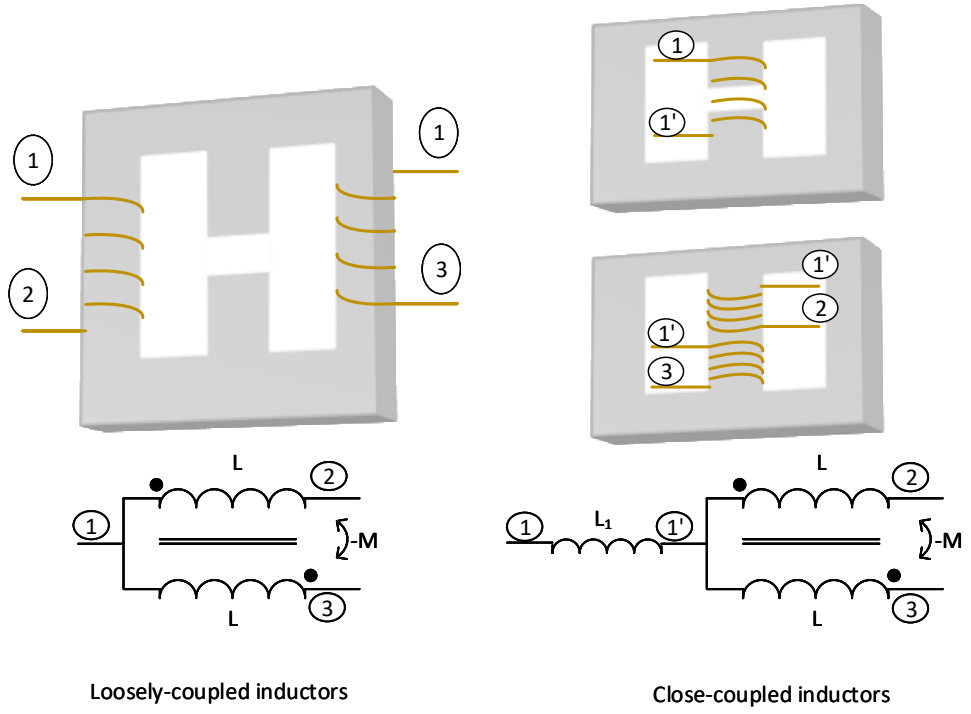


Figure 9.2: The Loosely-coupled inductor is on the left while the close-coupled inductor is on the right.

Figure 9.2 depicts the LCI and CCI of the interleaved boost converter with a multi-phase coupled inductor. The comparison between LCI and CCI, which is based on the parasitic capacitance and the capability to increase the switching frequency, will be presented in this research. The purpose of calculating the parasitic capacitance of two-phase coupled inductors is to obtain the ability of increasing the switching frequency at a safe operating point.

9.1.1 Estimating the Parasitic Capacitance of the Loosely-Coupled Inductors with a Single-Layer Windings

The multi-phase coupled inductors can be designed by using loosely-coupled inductors topology (LCI). The LCI topology with interleaved circuit combines the concept of the inductor and transformer of the CCI power converter into a single core [4, 7]. Moreover, the LCI topology with interleaved power converter can offer a low-cost and low-loss magnetic component by using the suitable magnetic core [4]. Therefore, It is essential to estimate the parasitic capacitance of the LCI inductors in order to properly select the operating frequency for reaching the highest efficiency with the smallest size possible.

Figure 9.3 shows the parasitic capacitance network of the loosely coupled inductors with a single-layer. By using the proposed modeling approach in chapter 4 with replacing the rod wire by a square shape, the following analytical calculation of parasitic capacitance can be achieved. The variables of the approximation can be taken from the rod wire as follows

$$W = d \tag{9.1}$$

$$L_{totaln} = L_{bottom} + L_{innern} + L_{fron} + L_{back} \tag{9.2}$$

$$L_{back} = \sqrt{L_{fron}^2 + d_{tt}^2} \tag{9.3}$$

$$L_{outern} = L_{bottom} + L_{fron} + L_{back} \tag{9.4}$$

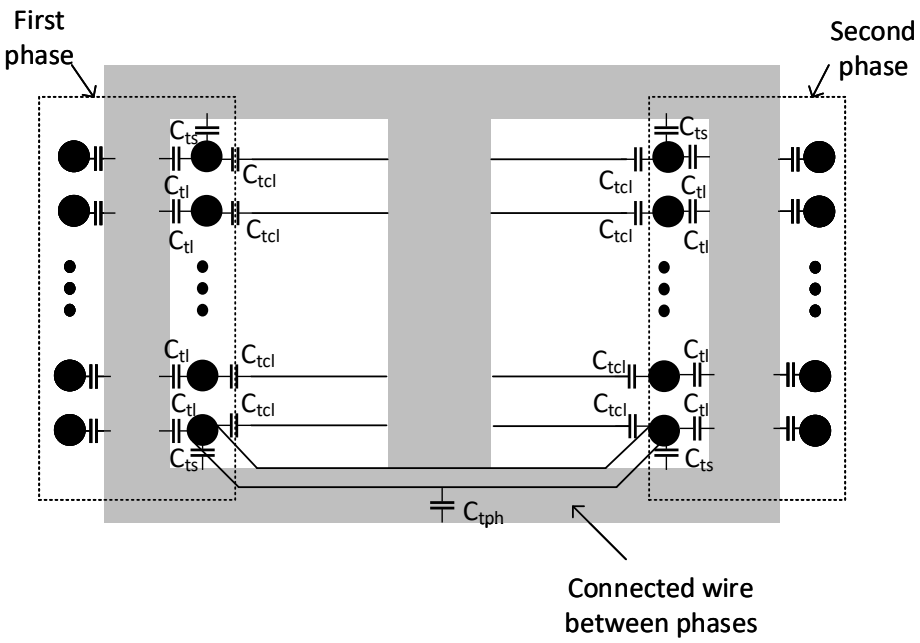


Figure 9.3: The single-layer loosely-coupled inductors with the parasitic capacitance network .

$$L_{total} = N * L_{totaln} \tag{9.5}$$

The width of square wire W can be selected from diameter d of the rod wire where W is the conductive part of wire with excluding coating and insulation parts. The length of a single turn is L_{totaln}. L_{innern} is the inner segment length of a turn while L_{outern} is the total of three outer segments of a turn. The length of a conductor L_{total} can be determined by multiplying the single turn length by number of turns N. Each turn of the inductor with LCI has four different distances. The distances between turn and turn, turn and central limb, and turn and far limb are d_{tt}, d_{tl}, and d_{tcl}, respectively. Assume that d_{ts}, which is the distance of the side turn to side core, is equal to d_{tt}. which can be determined as follows.

$$d_{tt} = \frac{E - (W * N)}{1 + N} \tag{9.6}$$

where E is the length of center limb that is occupied by the winding. Each parasitic capacitance of the LCI phases can be determined separately. In the following analysis, parasitic capacitance of

each element is presented.

$$A_{wside} = W * L_{totaln} \tag{9.7}$$

$$W_{cside} = 2\frac{d_{tt}}{2} + W \tag{9.8}$$

$$L_{cside} = 2L_{tside} + L_{bside} + \sqrt{L_{bside}^2 + d_{tt}^2} \tag{9.9}$$

when the distance increases between winding and central limb, the parasitic capacitance changes. Therefore, the average area and distance between winding and core are considered. The width of the electric field on the core is denoted by W_{cside}. L_{cside} represents the length of electric field on the core.

$$A_{cside} = W_{cside} * L_{cside} \tag{9.10}$$

$$A_{tl} = \frac{A_{wside} + A_{cside}}{2} \tag{9.11}$$

$$C_{tl} = \epsilon\frac{A_{tl}}{d_{tl}} \tag{9.12}$$

$$A_{tcs} = W * L_{innern} \tag{9.13}$$

$$C_{tcl} = \epsilon\frac{A_{tcs}}{d_{tcl}} \tag{9.14}$$

$$C_{ts} = \epsilon\frac{A_{tcs}}{d_{ts}} \tag{9.15}$$

$$\varepsilon = \varepsilon_r\varepsilon_o \tag{9.16}$$

where ε_r and ε_o are relative dielectric permittivity and dielectric permittivity of vacuum, respectively. A_{tl} is the average area between turn to core while A_{wside} is the area of conductor. A_{cside} is the area that covers the electric field of the wire on the core and it is assumed to be uniform among all the turns. The average area is related to the distance between turns. The area of the parasitic capacitance between a turn and far limb is denoted by A_{tcs} as well as the area between the side turn and a side limb. The parasitic capacitance of turn to central limb is denoted by C_{tl} while capacitance between turn to far limb and capacitance between turn and side limb are C_{tcl} and C_{ts}, respectively.

The total capacitance can be determined by excluding the insulation part between turns. So, the total capacitance between turns to central limb C_{tlTot}, the total capacitance between turns and far limb C_{tclTot}, and the total capacitance of side limbs C_{tsTot} are explained as follows

$$C_{tlTot} = N_{phase1}C_{tl} + N_{phase2}C_{tl} \tag{9.17}$$

$$C_{tclTot} = N_{phase1}C_{tcl} + N_{phase2}C_{tcl} \tag{9.18}$$

$$C_{tsTot} = 4 * C_{ts} \tag{9.19}$$

$$C_{btw} = \epsilon \frac{W * L_{cw}}{d_{cw}} \tag{9.20}$$

$$C_{Tot} = C_{tlTot} + C_{tclTot} + C_{tsTot} + C_{btw} \tag{9.21}$$

where the parasitic capacitance of the wire connected two-phases is represented by C_{btw}. The length of the connected wire between phases is L_{cw} while the distance between the connected wire and the magnetic core is d_{cw}.

9.1.2 Estimating the Parasitic Capacitance of the Closed-Coupled Inductors with a Single-Layer Windings

Another topology that can form the multi-phase coupled inductors is the closed-coupled inductors (CCI). The CCI topology with interleaved converter include an auxiliary inductor and closed-coupled inductors. The CCI topology provides higher filtering in the power converter due to the presence of the two magnetic components [4,63,64]. Furthermore, the magnetic cores materials of both magnetic components can be selected differently from each other in the CCI converter [4,64]. Moreover, due to the very high coupling coefficient and the inverse coupling of the CCI topology, the dc flux almost does not occur in the CCI. Therefore, it is essential to estimate the parasitic capacitance of the CCI topology in order to properly select the operating frequency and having the highest efficiency with smallest size possible.

Figure 9.4 depicts the parasitic capacitance network of the CCI topology with single-layer. The modeling approach of estimating the parasitic capacitance for CCI topology is extended to propose it approach in subsection 9.1.1.

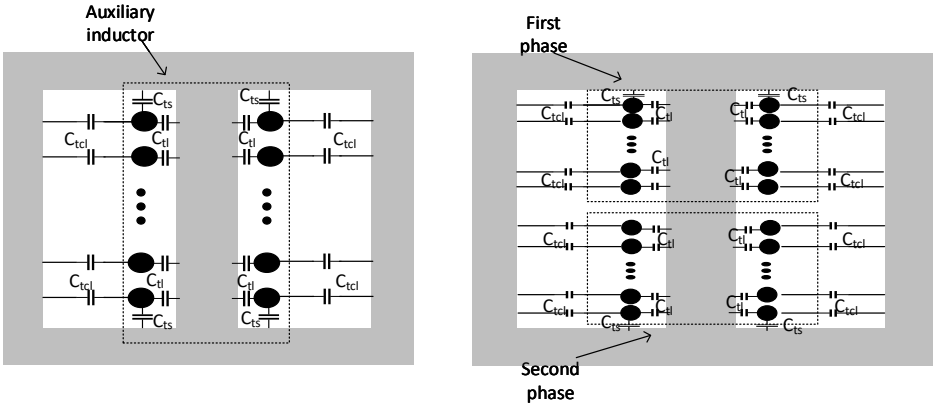


Figure 9.4: The single-layer closed-coupled inductors with the parasitic capacitance network .

As shown in figure 9.4, both phases are placed in the central leg of EE core. Therefore, the parasitic capacitance between the winding and the far legs should be considered. Hence, the total parasitic capacitance is presented as following.

$$C_{tlTot} = N_{phase1}C_{tl} + N_{phase2}C_{tl} \tag{9.22}$$

$$C_{tclTot} = N_{phase1}C_{tcl_Lift} + N_{phase2}C_{tcl_Lift} + N_{phase1}C_{tcl_Right} + N_{phase2}C_{tcl_Right} \quad (9.23)$$

$$C_{tsTot} = 4 * C_{ts} \quad (9.24)$$

$$C_{Tot} = C_{tlTot} + C_{tclTot} + C_{tsTot} \quad (9.25)$$

9.1.3 Experiments and Results

In order to verify the estimating model of the multi-phase coupled inductors, the parasitic capacitance of the LCI and CCI topologies are determined by ANSYS software with finite element analysis. Figure 9.5 shows the geometry of both the LCI and CCI inductors. Figure 9.5 (a) depicts the loosely coupled inductors with 6-number of turns for each phase while (b) is the closed-coupled inductors without the auxiliary inductor with 4-turns for each phase with smaller magnetic size and volume. The dimensions for both multi-phase coupled inductors are presented as shown in the figure 9.5.

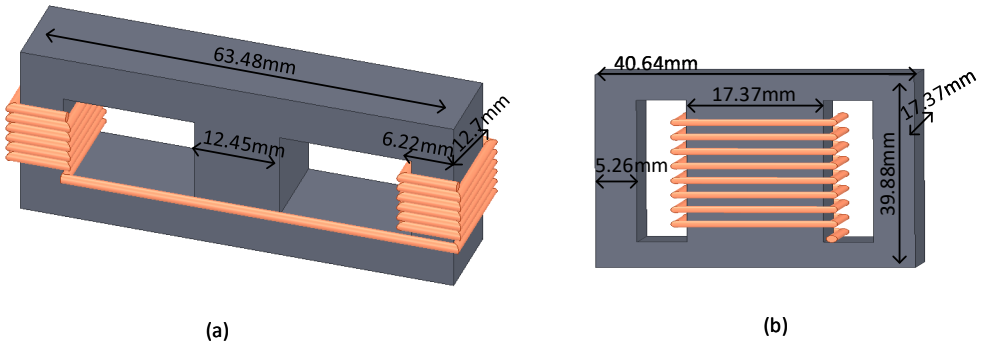


Figure 9.5: (a) The geometry of the multi-phase loosely-coupled inductors. (b) The geometry of the multi-phase closed-coupled inductors without an auxiliary inductor.

The estimating parasitic capacitance of the LCI topology from the analytical approach is 15.45 pF while the extracting capacitance by electrostatic model with FEA is 17.349 pF. The percentage error between the approaching model and the simulation is 11.405% as shown in figure 9.6.

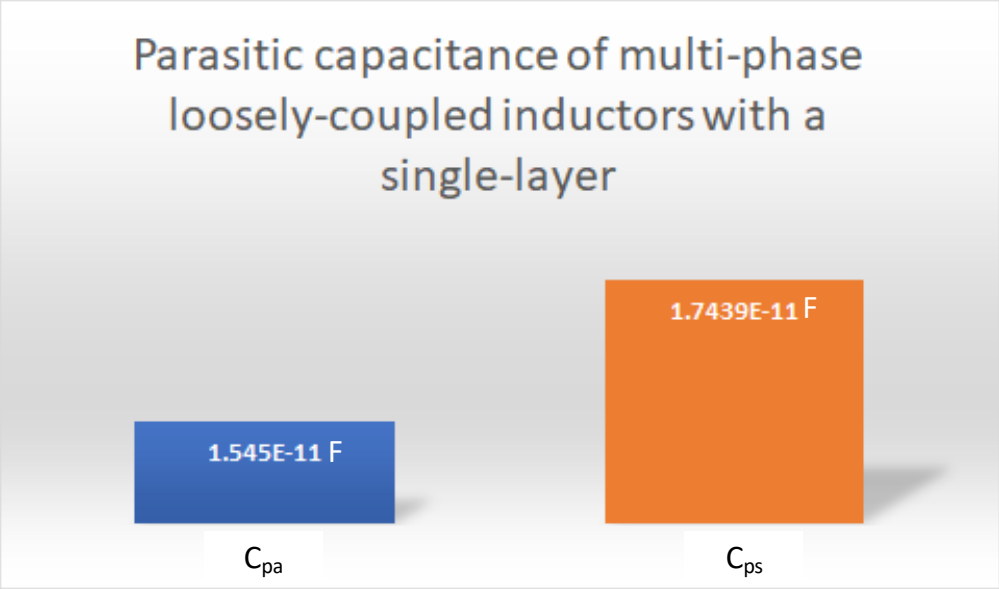


Figure 9.6: The comparison results of the multi-phase LCI between the modeling approach and the electrostatic model with FEA.

The network analyzer device is applied to experiment the LCI topology in order to extract the parasitic capacitance. Figure 9.7 shows the network analyzer with multi-phase loosely-coupled inductors. The average parasitic capacitance by the network analyzer is 23.32 pF while the parasitic capacitances at different frequencies are 22.038pF, 21.275pF, 23.197pF, 26.589pF, and 23.488pF. Therefore, the comparison results of the multi-phase LCI topology by analytical approach, simulation, and experiment are shown in figure 9.8.

On the other hand, the closed-coupled inductors is simulated to extract the parasitic capacitance. The parasitic capacitance of the CCI by electrostatic model with FEA is 24.699 pF while the parasitic capacitance by the modeling approach is 25.43 pF. That shows the percentage error between the approach model and the electrostatic model is 3% as shown in figure 9.9.

The network analyzer device is applied to experiment the CCI topology in order to extract the parasitic capacitance. Figure 9.10 shows the network analyzer with multi-phase closed-coupled inductors. The average parasitic capacitance by the network analyzer is 30.92 pF while the parasitic capacitances at different frequencies are 28.952pF, 30.843pF, 29.852pF, 33.836pF, and 31.138pF. Therefore, the comparison results of the multi-phase LCI topology by analytical

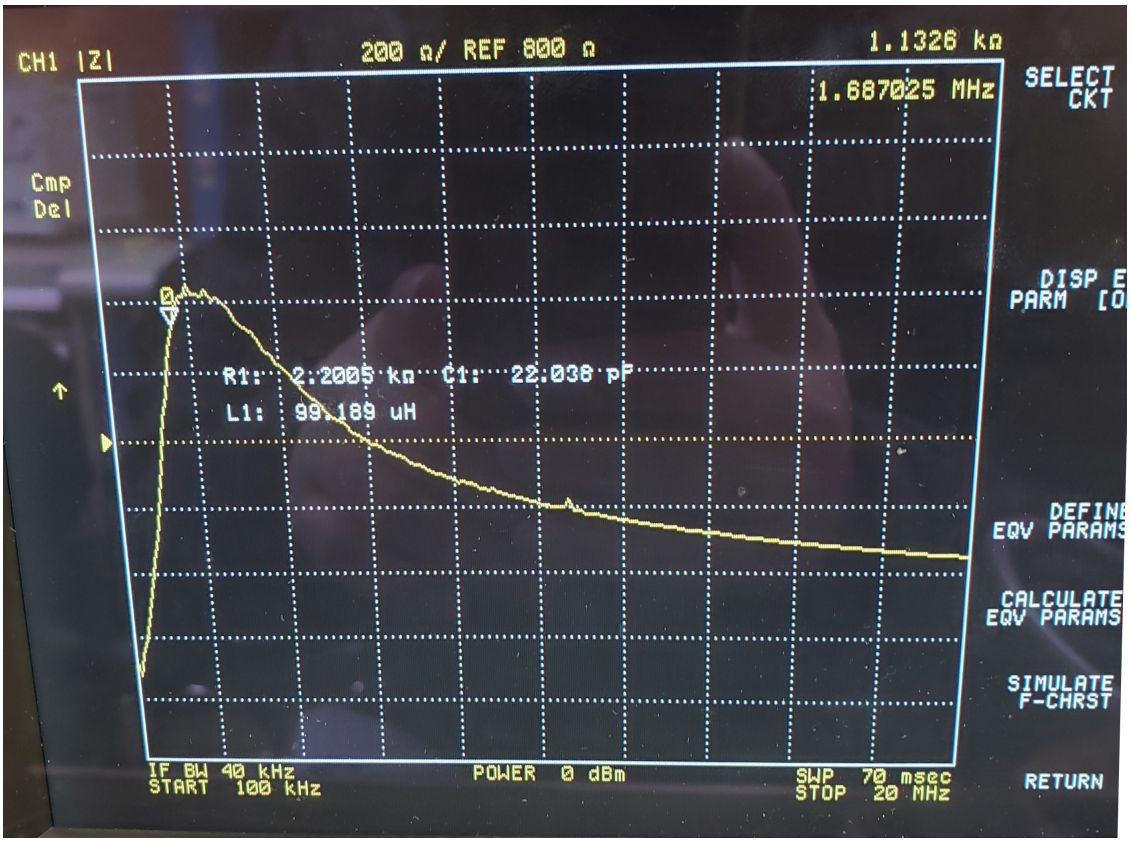


Figure 9.7: The parasitic capacitance of the multi-phase LCI with Network analyzer.

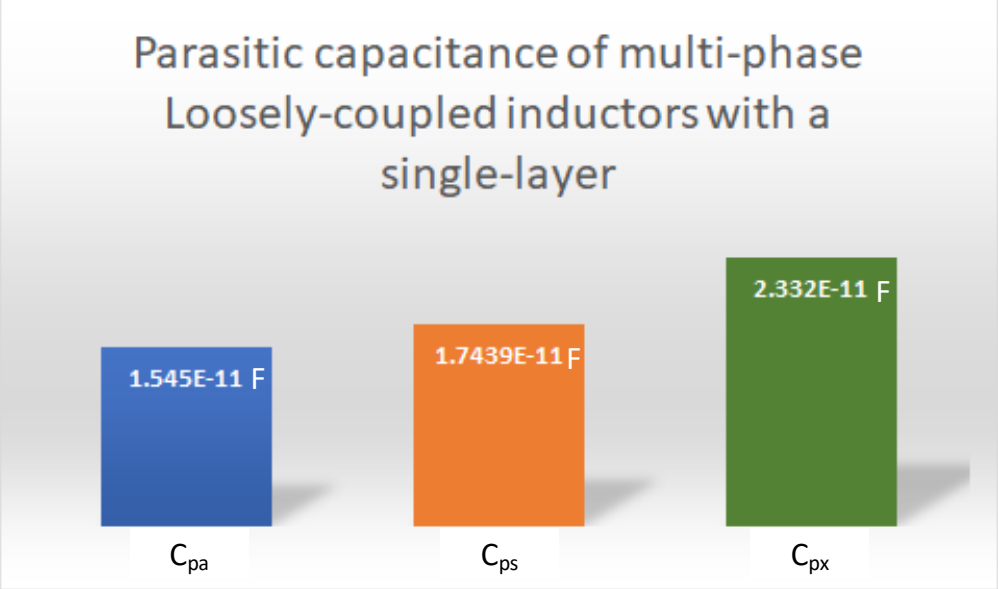


Figure 9.8: The comparison results of the multi-phase LCI between the modeling approach and the electrostatic model with FEA.

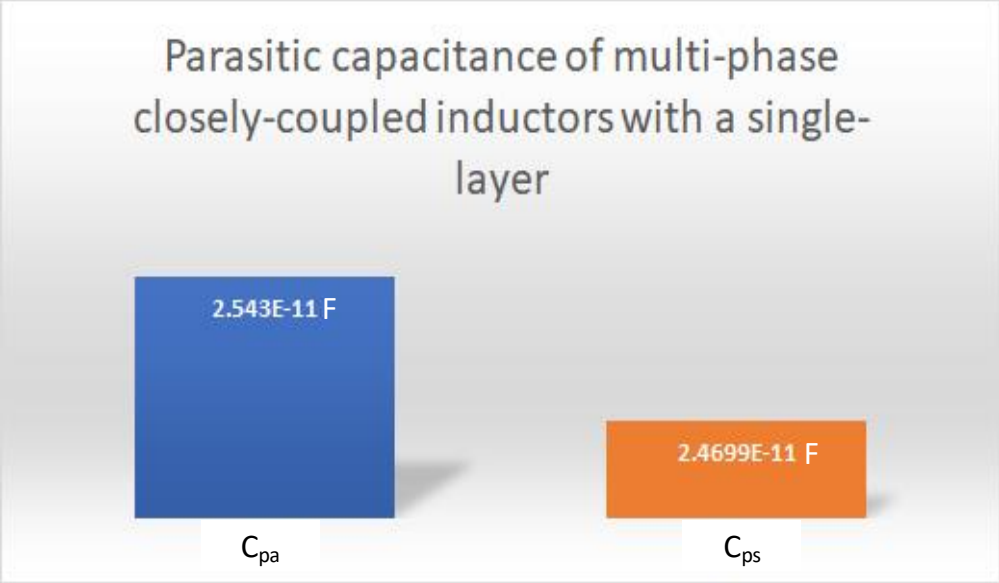


Figure 9.9: The comparison results of the multi-phase CCI between the modeling approach and the electrostatic model with FEA.

approach, simulation, and experiment are shown in figure 9.11.

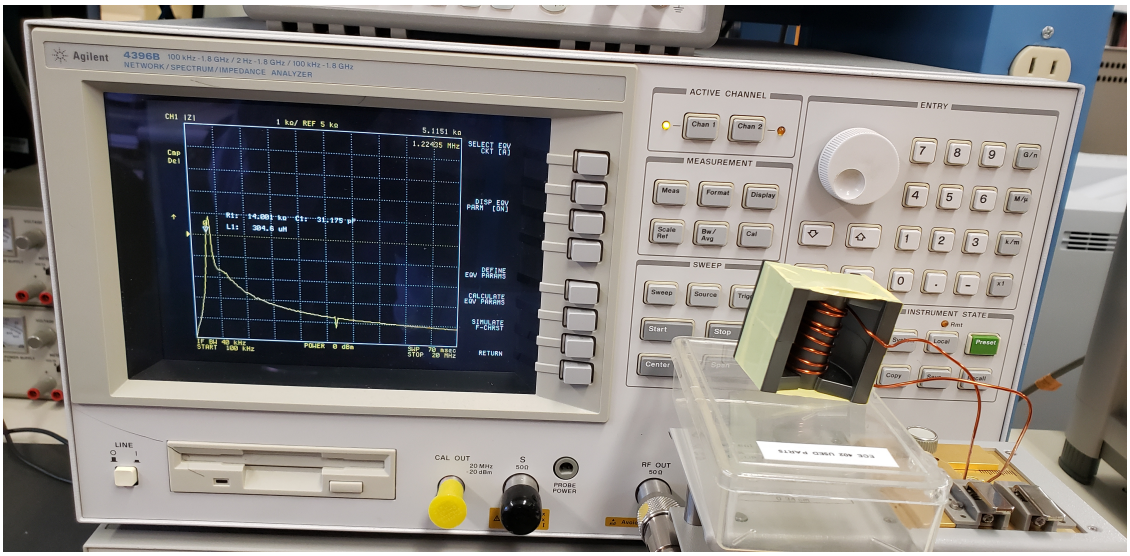


Figure 9.10: The parasitic capacitance of the multi-phase CCI with Network analyzer.

9.2 Design Interleaved Boost Converter with Two-Phase Coupled Inductors

The interleaved multi-phase coupled inductors boost converter has more advantages than the single-phase boost converter and multi-phase boost converter. The size of the magnetic components

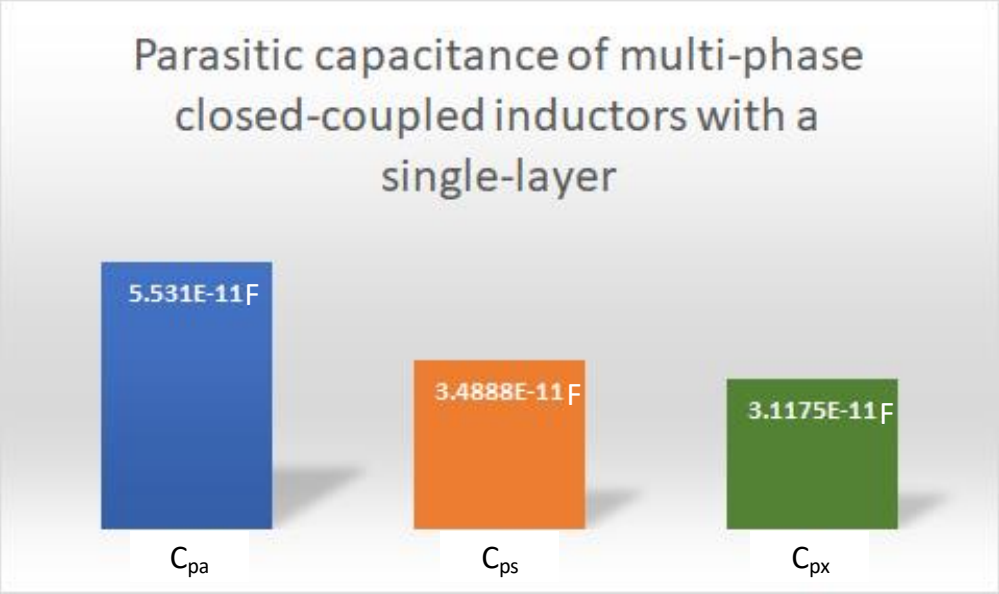


Figure 9.11: The comparison results of the multi-phase CCI between the modeling approach and the electrostatic model with FEA.

can be reduced by using the interleaved multi-phase coupled inductors boost converter. Moreover, the capacitors of the converter can be reduced. Furthermore, the better filtering and minimizing the dc flux can be occurred with multi-phase coupled-inductors [4, 7].

Therefore, the interleaved multi-phase coupled inductors boost converter is selected to apply the increasing the operating frequency with maintaining the efficiency by estimating the parasitic capacitance and using the proposed methodology in chapter 8.

The multi-phase loosely-coupled inductors topology is selected to design the interleaved coupled inductors boost converter. The reason of choosing the LCI topology rather than the CCI topology is because the more advantages than the CCI. Some of the advantages of the LCI topology are using one magnetic core with two-phases, low-cost, and low-loss in the magnetic components [4].

9.2.1 Determining the Inductance value of the Interleaved Loosely-Coupled Inductors Boost Converter

The equivalent inductances of the two-phase coupled inductors of boost converter should be determined to have the suitable coupled-inductors size. The derivation of the two-phase loosely-coupled inductors of boost, which is explained in [6, 65, 66], is presented next.

Figure 9.12 shows two inductors that can be coupled directly or inversely. Therefore, the circuit equation of the coupled inductors is shown in (9.27).

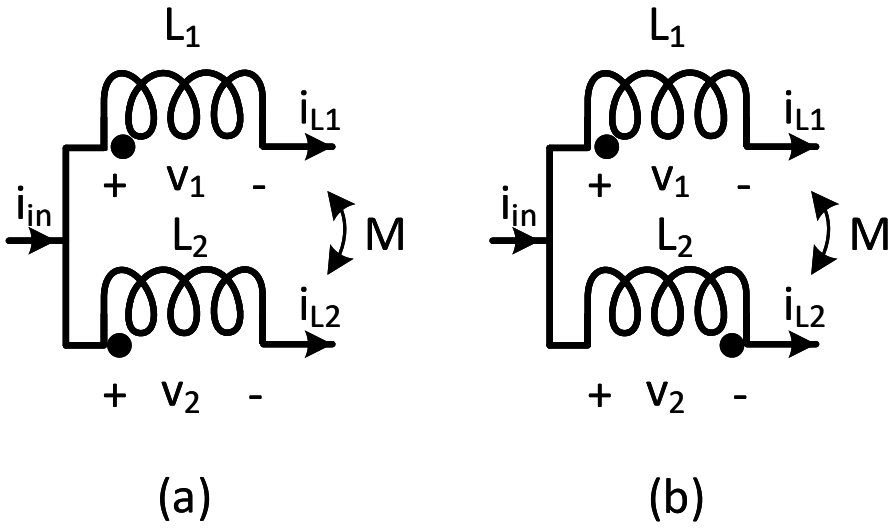


Figure 9.12: (a) The direct coupled inductors. (b) The inverse coupled inductors.

$$v_1 = L_1 \frac{di_{L1}}{dt} \pm M \frac{di_{L2}}{dt} \tag{9.26}$$

$$v_2 = L_2 \frac{di_{L2}}{dt} \pm M \frac{di_{L1}}{dt} \tag{9.27}$$

where the voltages applied on both windings are v_1 and v_2 while the inductor currents of each phase are i_{L1} and i_{L2}, respectively. The self-inductance of both windings are L_1 and L_2, while M is the mutual inductance. When the coupled inductors is inversely coupled, the sign before M is " – ".

With applying the loosely-coupled inductors to boost converter, the phase shift between switches is 180^o. Figure 9.13 shows the two-phase interleaved coupled inductors boost converter. The dc input voltage of the converter is V_{in} while the output voltage represented by V_{out}. The switches of both phases are S_1 and S_2. The two windings of the interleaved coupled inductors are are assumed to be identical, i.e., $L_1 = L_2 = L$. Therefore, the following equation for the inverse coupled can be obtained.

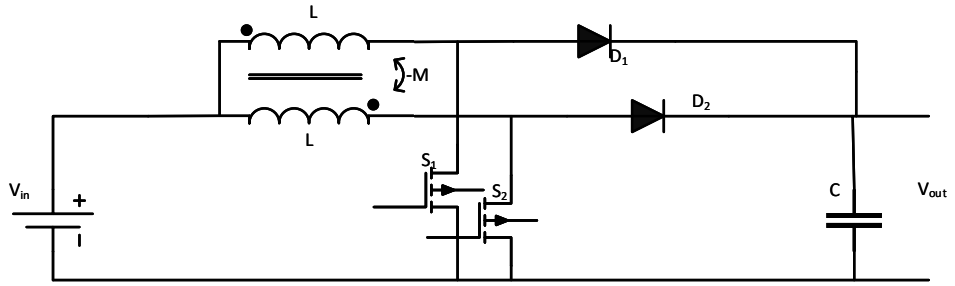


Figure 9.13: The interleaved boost converter with two-phase coupled inductors.

$$v_1 + kv_2 = (1 - k^2)L\frac{di_{L1}}{dt} \tag{9.28}$$

where the magnetic coupled coefficient is represented by k. The define of the magnetic coupling coefficient is $k = \frac{M}{\sqrt{L_1 L_2}} = \frac{M}{L}$. At steady state, the conversion ratio of the boost converter for each switching cycle is shown in (9.29).

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 - D} \tag{9.29}$$

where D is the duty cycle of S_1 and S_2.

When the switch S_1 is conducted, the voltage of the winding 1 is equal to V_{in}. Moreover, the $\frac{di_{L1}}{dt}$ can be determined by the equivalent inductance. For the voltage across the second winding when S_2 is OFF, v_2 is equal to $V_{in} - V_{out}$ while if S_2 is ON, $v_2 = V_{in}$.

Therefore, the following equation can be obtained by substituting eq(9.28), eq(9.29), and S_1 is ON and S_2 is OFF.

$$V_{in} = \frac{1 - k^2}{1 - \frac{kD}{1-D}} L\frac{di_{L1}}{dt} \tag{9.30}$$

where

$$L_{eq1} = \frac{1 - k^2}{1 - \frac{kD}{1-D}} L \tag{9.31}$$

When both switches S_1 and S_2 are conducted, the equivalent inductance will be as shown in eq(9.32).

$$L_{eq2} = (1 - k)L \tag{9.32}$$

When both switches are OFF, the voltages across both windings are $v_1 = v_2 = V_{in} - V_{out}$. The following equation can be determined by substituting eq(9.29) into eq(9.28).

$$V_{in} - V_{out} = L_{eq2}\frac{di_{L1}}{dt} \tag{9.33}$$

At the case, when S_1 is OFF while S_2 is ON, the voltage across the winding 1 is $v_1 = v_{in} - V_{out}$. The voltage across the winding 2 is $v_2 = V_{in}$. Therefore, the following equation can be obtained by substituting eq (9.29) into eq (9.28).

$$V_{in} - V_{out} = L_{eq3}\frac{di_{L1}}{dt} \tag{9.34}$$

where

$$L_{eq3} = \frac{1 - k^2}{1 - \frac{k(1-D)}{D}}L \tag{9.35}$$

Therefore, the suitable inductance size of the interleaved two-phase loosely-coupled inductors boost converter can be obtained by determining the equivalent inductance.

9.2.2 Experiment and Results

The interleaved two-phase loosely-coupled inductors boost converter is designed with estimating the parasitic capacitance then redesign it based on the proposed methodology on chapter (8). Therefore, the operating frequency of the boost converter can be increased with maintaining the efficiency by designing based on the estimating the parasitic capacitance.

Table 9.1 shows the parameters of designing the interleaved two-phase LCI boost converter. The operating frequency of the LCI boost converter is 50 kHz which is selected from [4] in order to compare it with the new operating frequency chosen based on the proposed methodology.

The chosen magnetic core of the LCI is $E65/32/54$ with 3C92 Ferrite core where the complex permeability is stay constant over the selected operating frequency as shown in figure 9.14. The

Table 9.1: Interleaved two-phase loosely-coupled inductors boost converter parameters with 50 kHz.

Symbol	Items	Value
V_{in}	Input voltage	70 V
V_{out}	Output voltage	213 V
P_{out}	Output power	500 W
$\Delta i_{Lph}/I_{Lph}$	Ratio of ripple current	0.2
f_{sw}	Switching frequency	50 kHz
D	Duty ratio	0.67
k	Magnetic coupling coefficient	0.9
L_{ph}	Self-inductance of each phase	2.991 mH
ΔV	Ratio of output ripple voltage	10%
C_o	Output Capacitor	0.99 μF

number of turns of each phase is 48-turn with two-layer. The magnetic core volume is 126.123 cm^3 with approximated wire length of two-phases is 12.52m.

The total losses of windings is 3.227 W. The magnetic core loss of the LCI is 12.612 W. Then, the total loss of the interleaved LCI is 15.839 W at 50 kHz.

By using the proposed methodology of selecting the suitable operating frequency based on knowing the parasitic capacitance and other parameters as explained in chapter (8), the parasitic capacitance is measured by using the Network Analyzer, with resonant frequency is 515.3 kHz, is 43.384 pF. Therefore, the new switching frequency is chosen to be 100 kHz.

The parameters of the interleaved two-phase LCI boost converter with 100 kHz are shown in Table 9.2. The volume of the new magnetic core with $E56/24/38$ 3C92 Ferrite core, is reduced by 60.2%. The volume is 50.223 cm^3. The number of turns of each phase is reduced from 48 to 36 turns with total length of wire is 4.896m.

The total losses of windings is 1.282 W. The magnetic core loss of the LCI is 15.067 W. Then, the total loss of the interleaved LCI is 16.349 W at 100 kHz.

Figure 9.15 shows the volume comparison between the conventional LCI inductor and the new inductor designed. Both coupled inductors are shown in figure 9.16 where the large coupled inductor is the conventional coupled inductor. The reducing percentage of each component of

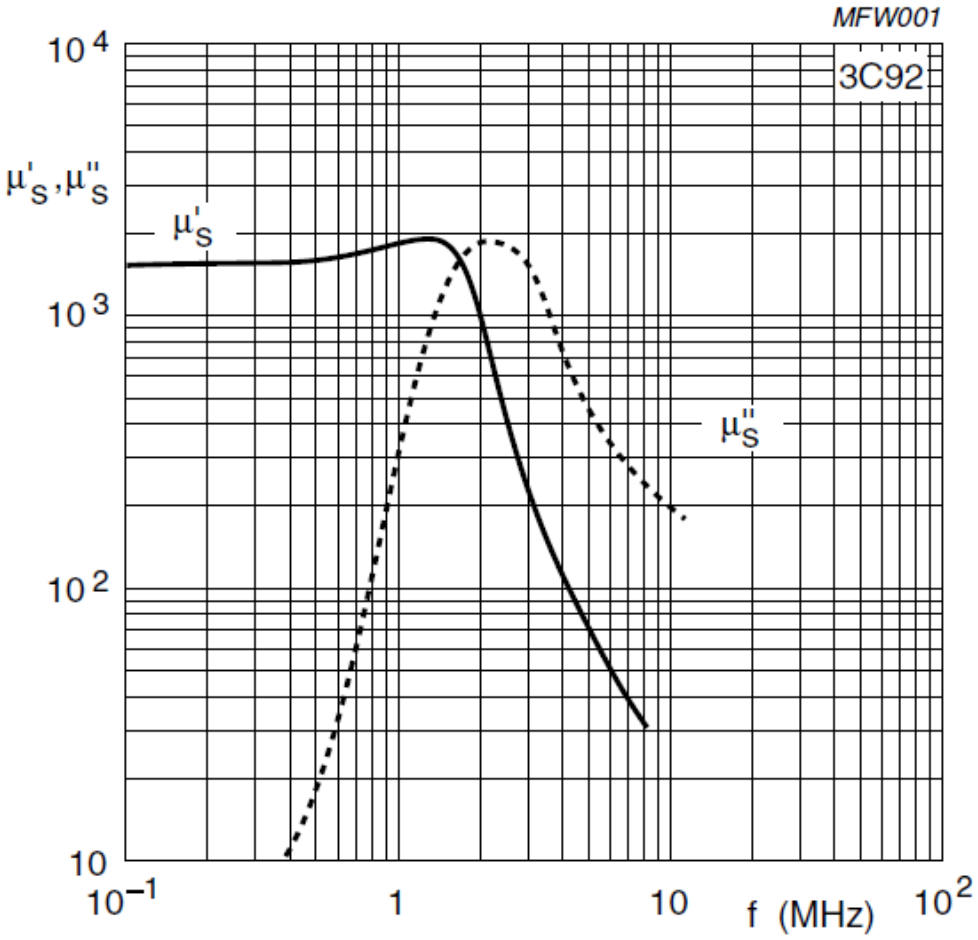


Figure 9.14: The permeability of the 3C92 magnetic core material versus the frequency.

Table 9.2: Interleaved two-phase loosely-coupled inductors boost converter parameters 100 kHz.

Symbol	Items	Value
V_{in}	Input voltage	70 V
V_{out}	Output voltage	213 V
P_{out}	Output power	500 W
$\Delta i_{Lph}/I_{Lph}$	Ratio of ripple current	0.2
f_{sw}	Switching frequency	100 kHz
D	Duty ratio	0.67
k	Magnetic coupling coefficient	0.9
L_{ph}	Self-inductance of each phase	1.495 mH
ΔV	Ratio of output ripple voltage	10%
C_o	Output Capacitor	0.66 μF

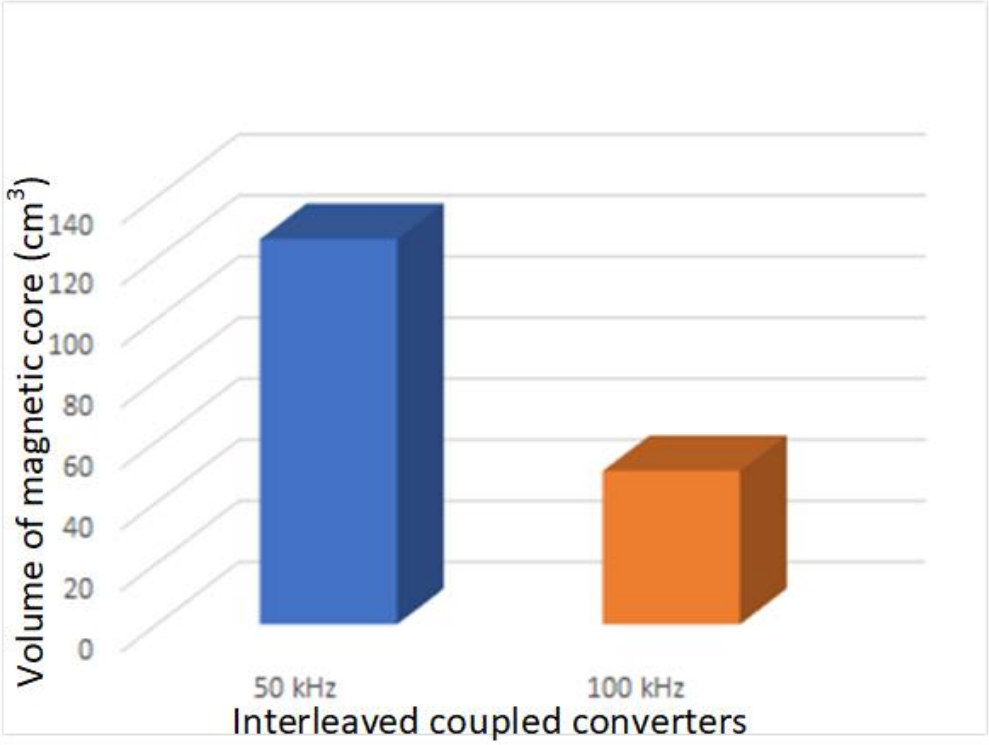


Figure 9.15: The volume comparison between the conventional LCI inductor and the new LCI inductor designed.

the converters is presented in figure 9.17. It shows that the magnetic core is reduced by 60%, the conductor of the windings is reduced by 60%, and the capacitor value is reduced by 30%.

The interleaved coupled boost converter contains two MOSFETs and two diodes as shown in figure 9.18. The MOSFET type that is used on the both experiments is IPAW60R380CE while the diode type is VS-HFA15 TB60-1-M3.

The results of both converters are measured by Oscilloscope and LabView. The measurement setup of the experiment that is connected to the LabView is shown in figure 9.19. The output current and voltage of the converter with 50 kHz that measured by the LabView measurement are shown in figure 9.20. The output current and voltage for one cycle of the interleaved coupled inductor with 50 kHz is shown in figure 9.21. Figure 9.21 shows the result are taken from the Oscilloscope where the output operating frequency of the interleaved converter is doubled the switching frequency.

The results of the new interleaved coupled inductors boost converter with 100 kHz are shown in figure 9.22. Figure 9.22 shows the output voltage and current with the LabView measurement.

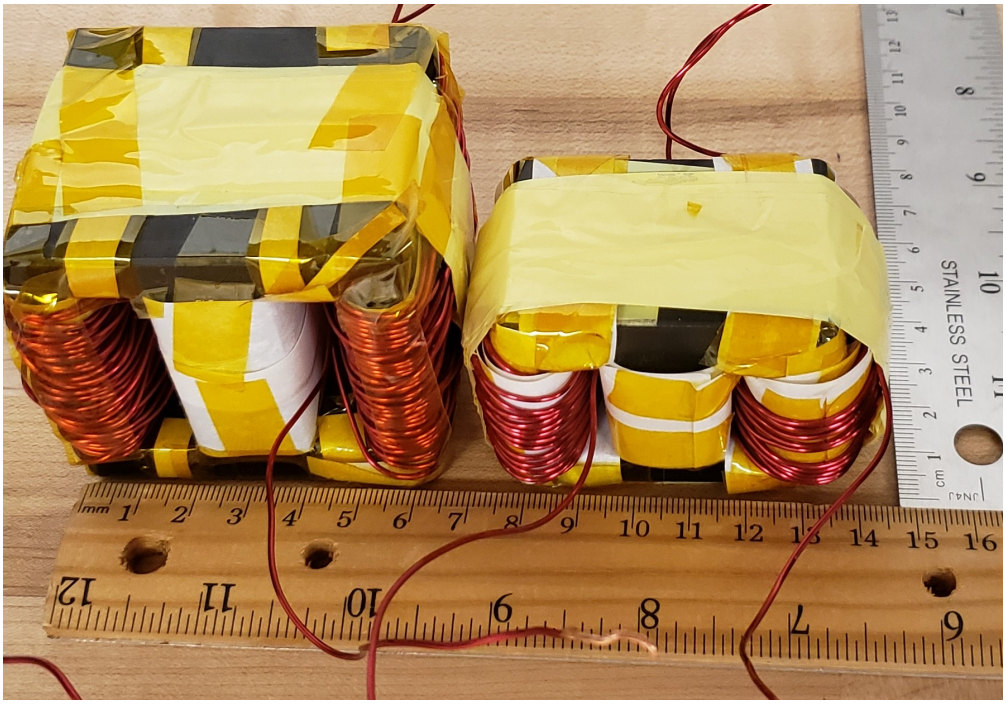


Figure 9.16: The conventional LCI inductor with 50 kHz is on the left while the new inductor designed with 100 kHz is on the right.

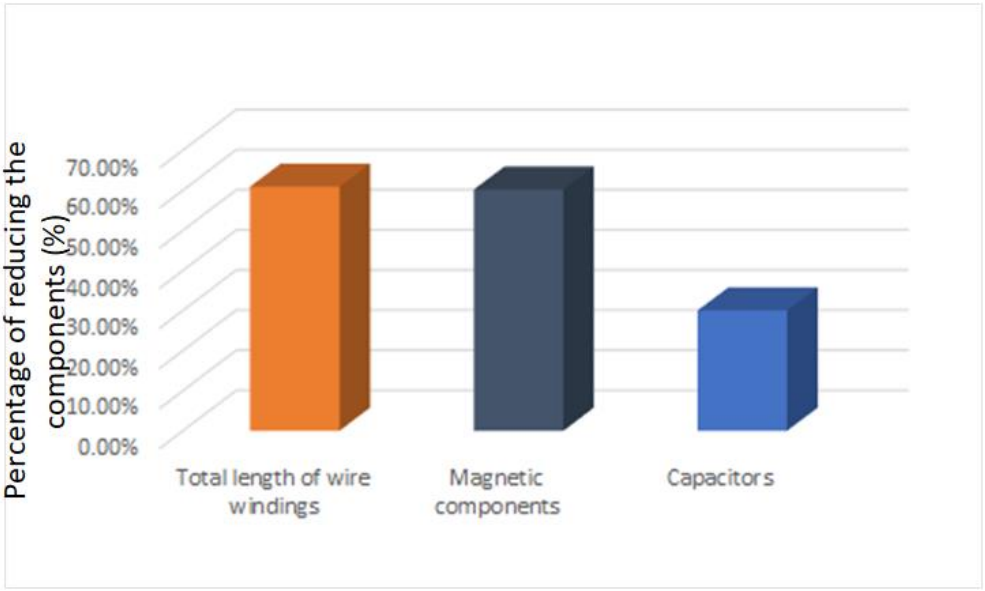


Figure 9.17: The percentage of reducing each component of the interleaved coupled boost converter compared with the conventional converter.

The output current and voltage for one cycle of the interleaved coupled inductor with 100 kHz is shown in figure 9.23. Figure 9.23 shows the result are taken from the Oscilloscope where the output

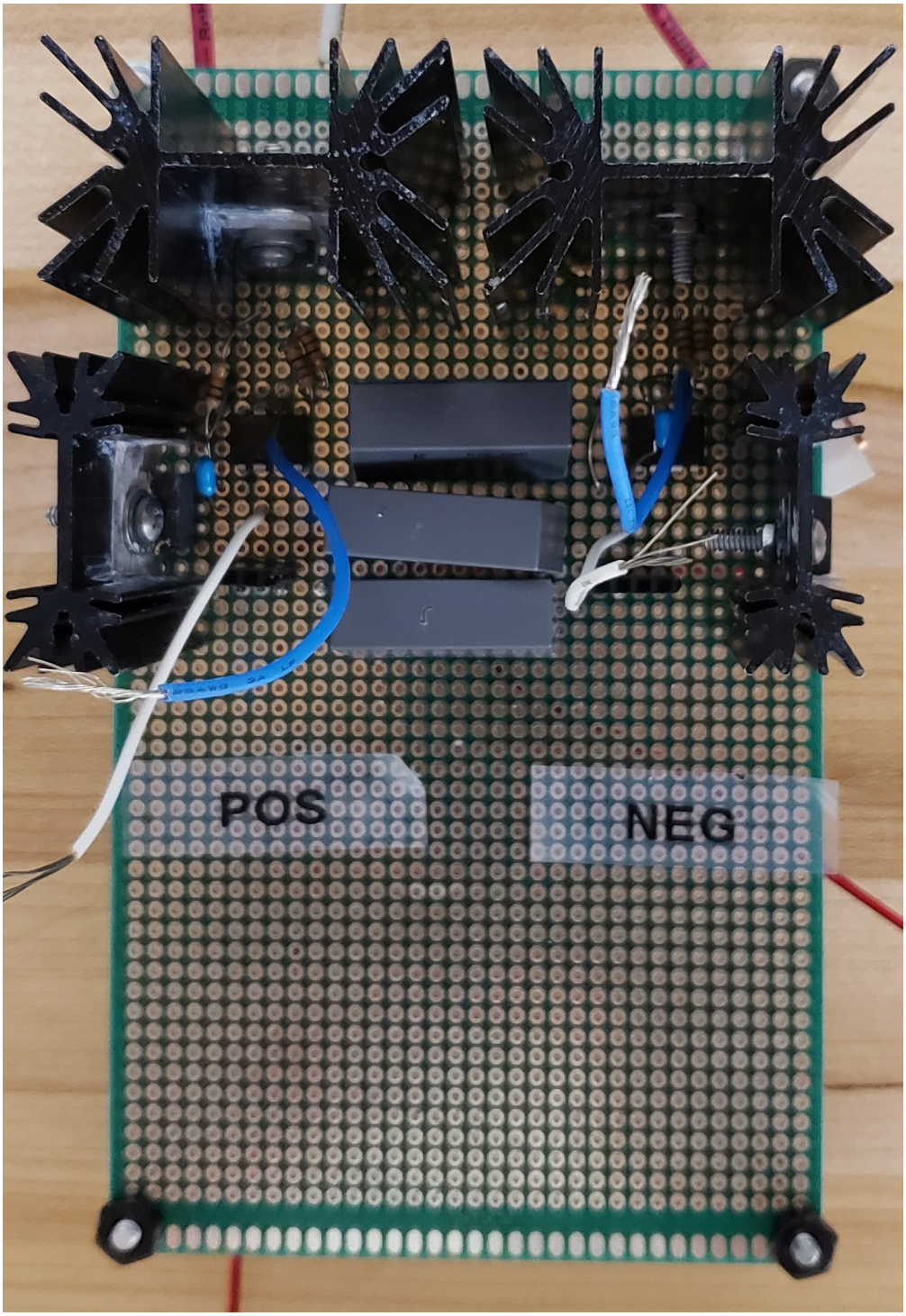


Figure 9.18: The circuit components of the interleaved boost converter.

operating frequency of the interleaved converter is doubled the switching frequency.

The total power losses of interleaved coupled converters with 50 kHz and 100 kHz are 28.116

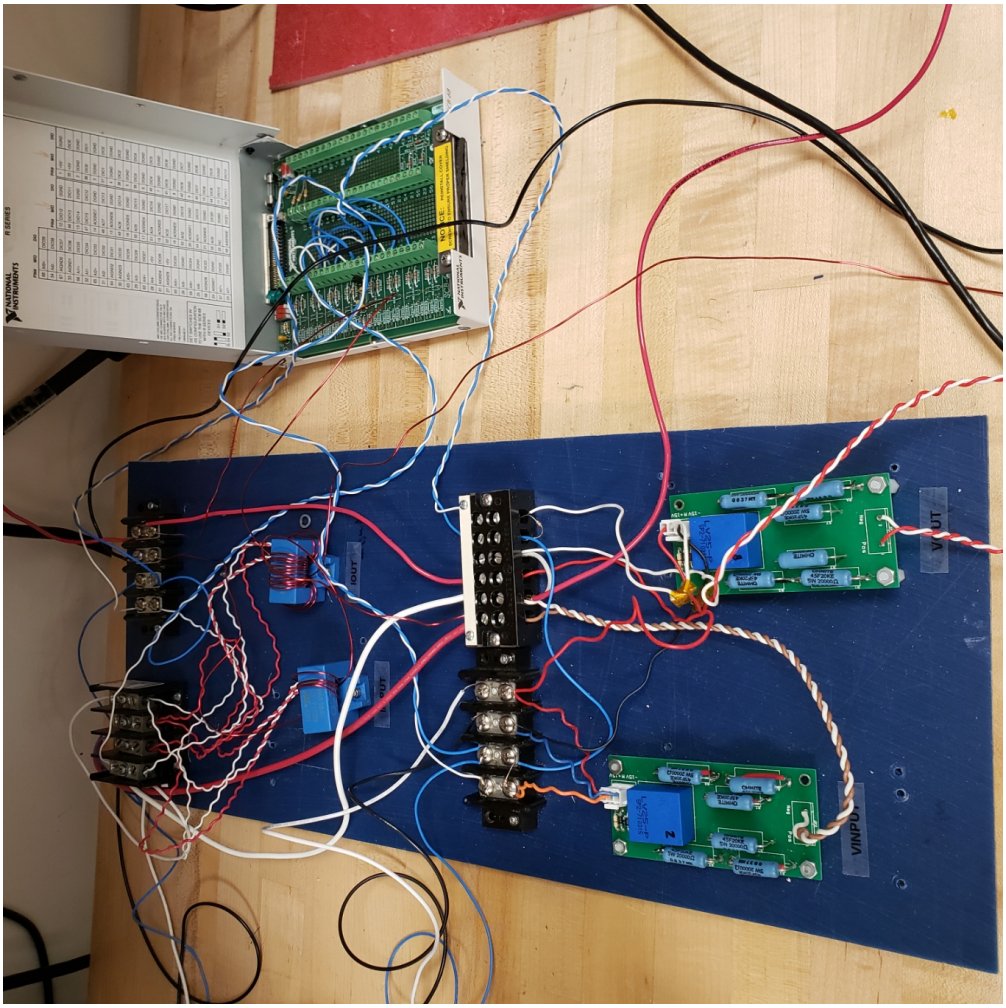


Figure 9.19: The measurement setup of the experiment.

and 32.487, respectively. The efficiency of both interleaved coupled converters are shown in figure 9.24. The efficiency of the interleaved coupled boost converter with 50 kHz is 94.376% while the efficiency of the interleaved coupled boost converter with 100 kHz is 93.503%.

Therefore, the total volume of the interleaved coupled-inductors boost converter is reduced with maintaining the efficiency of the converter. Even if with doubling the switching frequency of the converter, the efficiency of the converter is maintained and the methodology of selecting the operating frequency is verified with multi-phase coupled inductors boost converter.

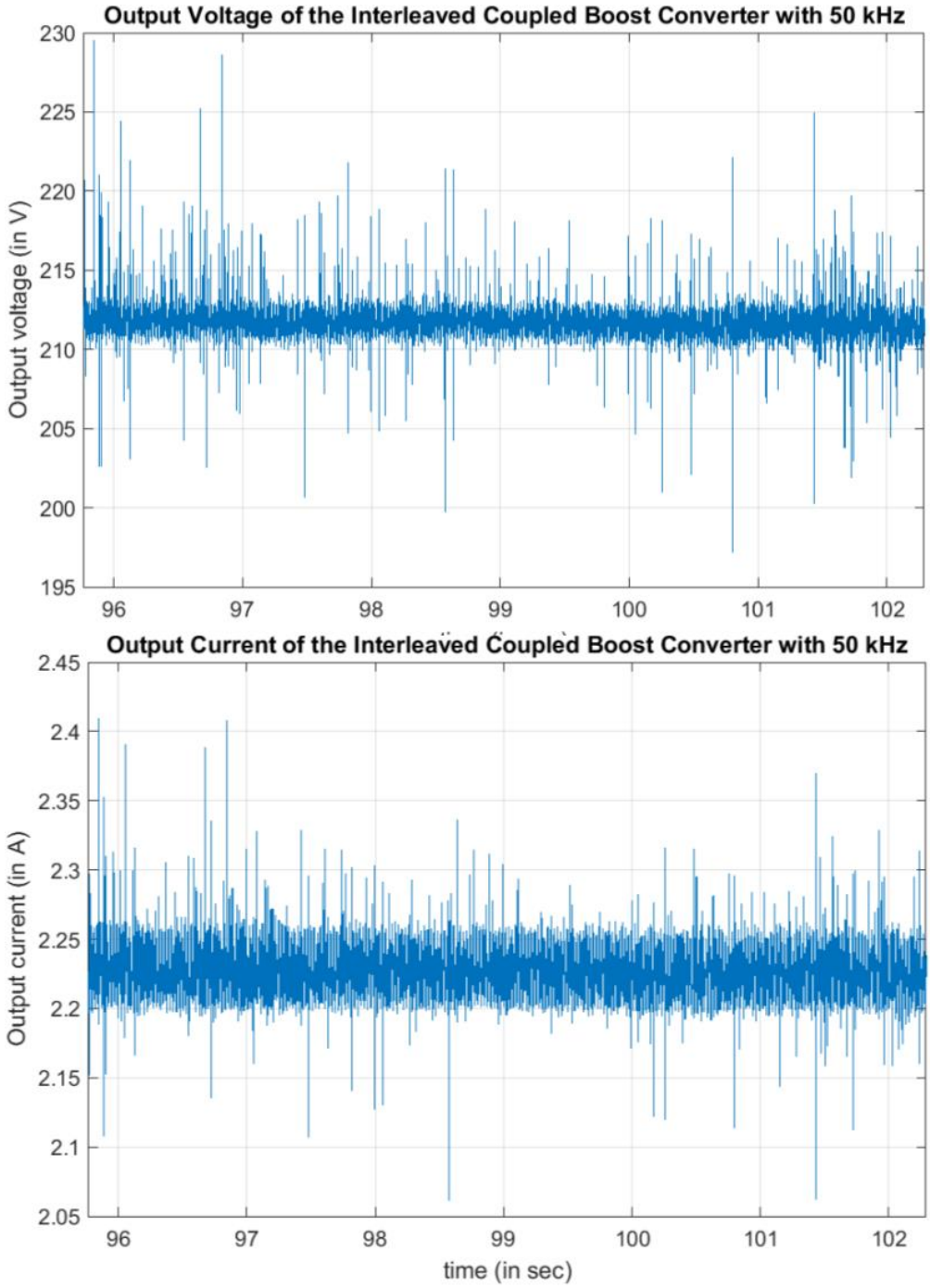


Figure 9.20: The DC output voltage and current of the interleaved coupled boost converter with 50 kHz.

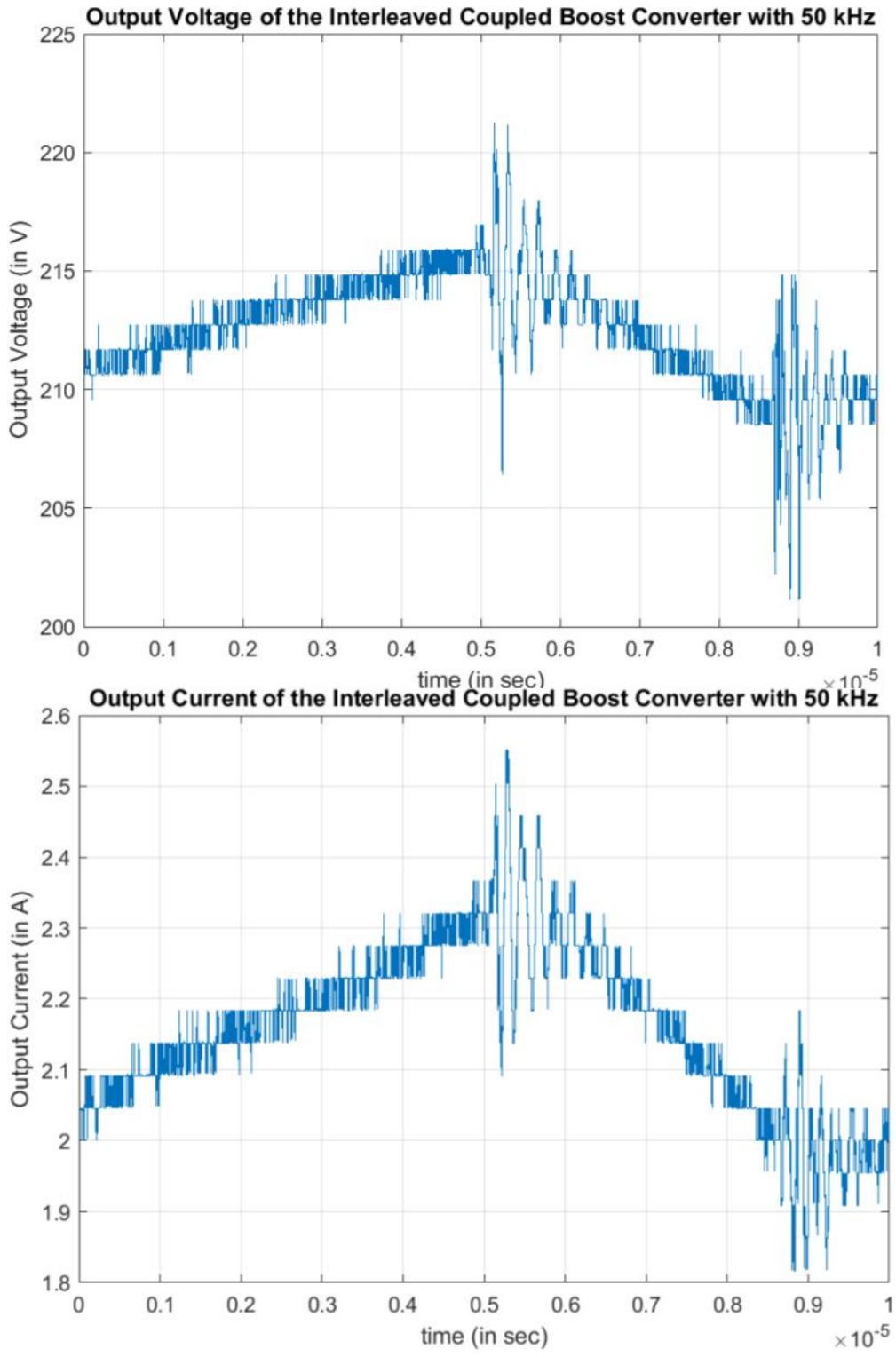


Figure 9.21: The cycle outputs of the voltage and current of the interleaved coupled boost converter with 50 kHz.

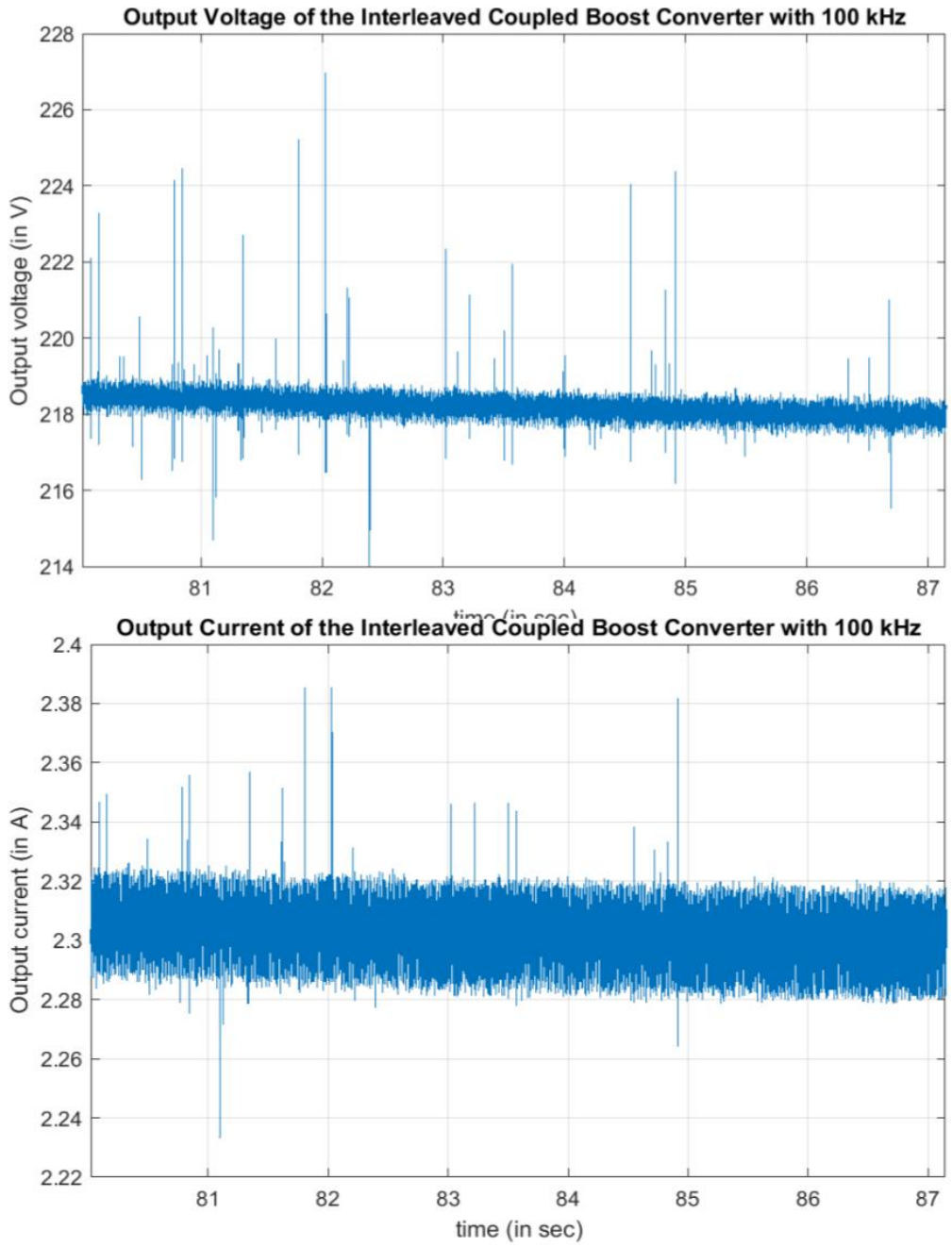


Figure 9.22: The DC output voltage and current of the interleaved coupled boost converter with 100 kHz.

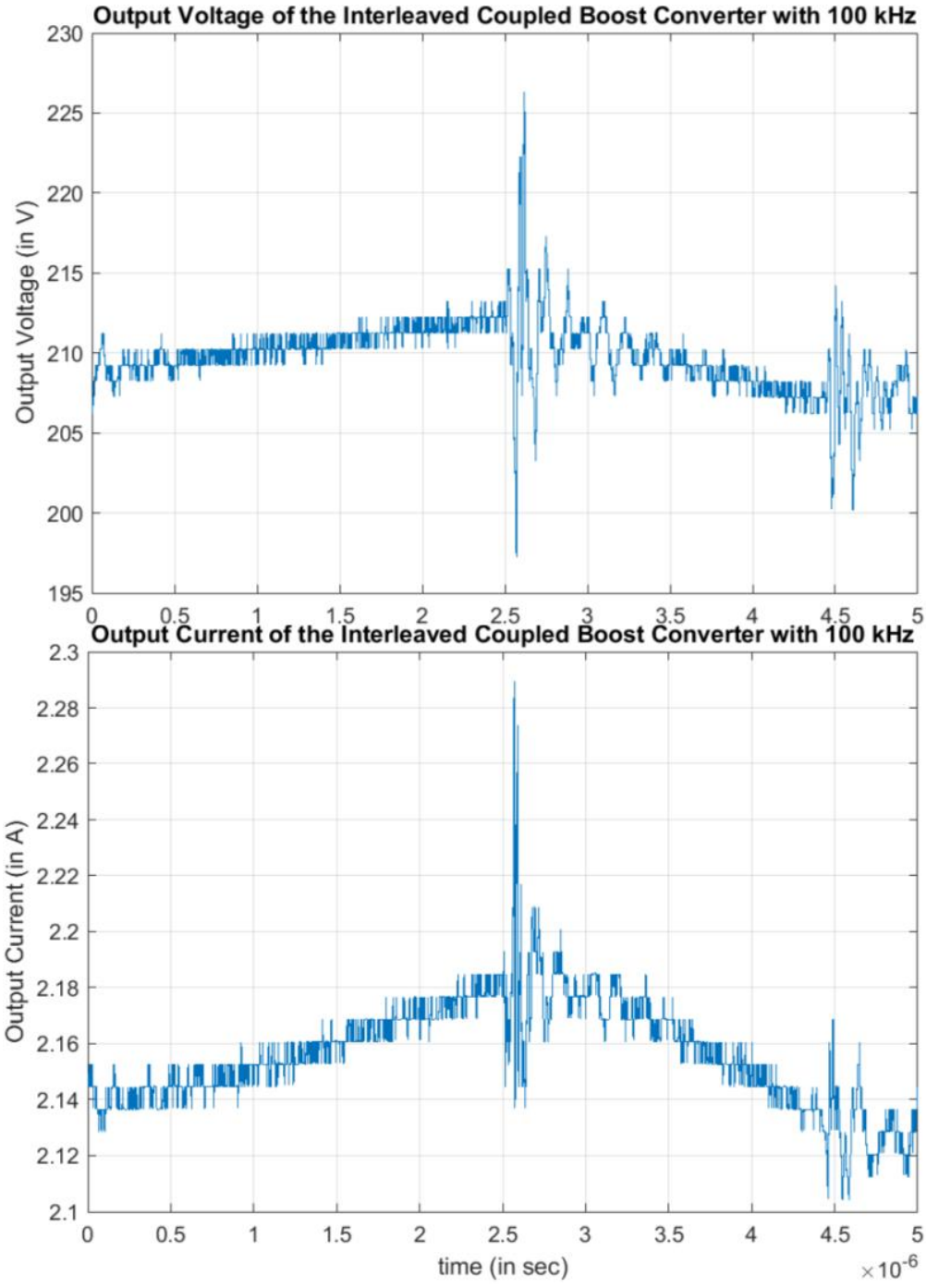


Figure 9.23: The cycle outputs of the voltage and current of the interleaved coupled boost converter with 100 kHz.

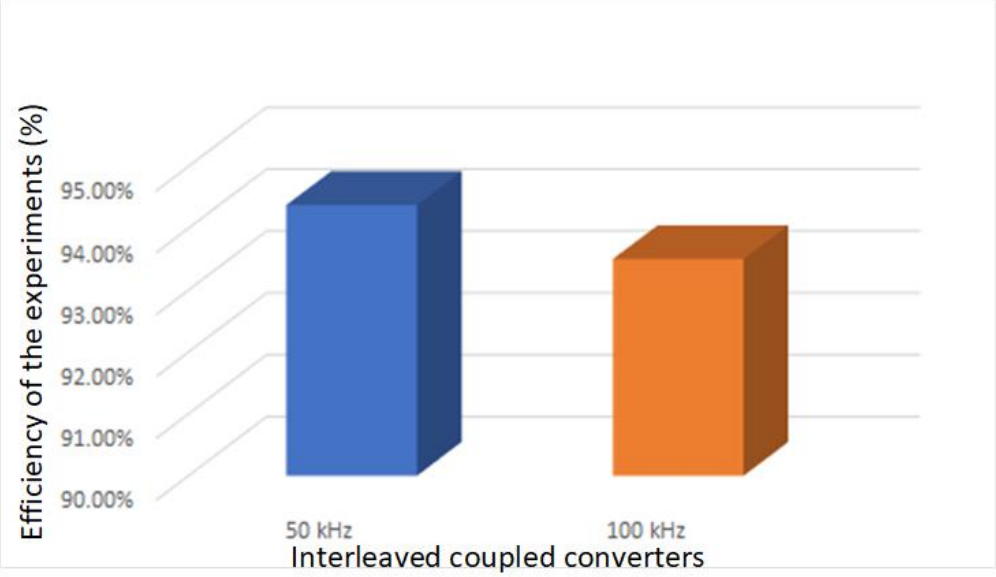


Figure 9.24: The efficiency of both The interleaved coupled converters

CHAPTER 10

CONCLUSIONS AND FUTURE WORK

10.1 Conclusions

In this dissertation, we introduced the new approach model for determining the parasitic capacitance of the magnetic components with single-layer winding for medium power applications. We first studied the analytical approaches of modeling the parasitic capacitance of the inductor with a magnetic core. Those modeling approaches of the parasitic capacitance have advantages and disadvantages as shown in chapter 3. Therefore, the new approach of modeling the parasitic capacitance of a single-layer inductors with a magnetic core is proposed in chapter 4.

Moreover, the investigating of the overall parameters affecting the parasitic capacitance of the magnetic components are presented in chapter 5. The categories of the parasitic capacitance parameters of the magnetic components are proposed where the major and minor parameters are the overall parameters of the parasitic capacitance.

Also in this work, the reduction technique of the parasitic capacitance is proposed in chapter 7. By applying this technique, the resonant frequency of the magnetic components is shifted to a higher frequency point. This technique allows the magnetic components to have a better performance at high operating frequency.

In chapter 8, The new methodology of improving the performance of the magnetic components at a high frequency operating, by the knowledge of the parasitic capacitance, is presented. The proper high operating frequency can be selected, by using the new methodology, to offer a lower size and cost of magnetic components with maintaining efficiency. The high operating frequency selected depends on three main conditions. They are the resonant frequency, the magnetic core frequency limitation, and the power electronic switch limitation. By verifying the conditions, the high frequency is properly chosen besides studying the losses of the magnetic components as shown in chapter 8.

Finally, The parasitic capacitance modeling of the interleaved two-phase coupled inductors is proposed in chapter 9. The loosely-coupled inductors and the closed-coupled inductors are the chosen topology to estimate the parasitic capacitance. The comparison of two different operating frequencies of the interleaved two-phase loosely-coupled inductors is applied with the proposed methodology to reduce the size of the magnetic components with maintaining the efficiency at high frequency operating.

10.2 Future Work

There is always a space for improvement in academia. Improving the performance of the magnetic components of power converters for high-frequency applications has many aspects to working on. Hence, following topics can be considered for the future work:

- The modeling approach for the parasitic capacitance of the interleaved multi-layer multi-phase coupled-inductors is needed to estimate the resonant frequency of the magnetic components. By increasing the number of phases more than two phases on a single-core, the parasitic capacitance should have a new method to be determined. Based on the author's knowledge, there is no analytical model to estimate the parasitic capacitance for multi-phase coupled-inductors.

- A new technique of reducing the parasitic capacitance for interleaved multi-phase coupled-inductors is needed. The interleaved coupled inductors power converter gets the intention to reduce the size of the power converter with the ability to deliver higher power to the system [4, 7]. Therefore, with increasing the operating frequency, the parasitic capacitance should be reduced to avoid over-voltage and EMI losses.

- On the other of improving and reducing the size of the power converter at high frequency, the interleaved multi-phase coupled-inductors offer more reduction of the size with improving the efficiency of the power converter. Therefore, the interleaved three-phase coupled-inductors power converter is a new area that can be modeled to improve the efficiency at high frequency

besides reducing the total size of the power converter.

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