FLEXIBLE, COMPACT, AND HIGH-POWER-COMPATIBLE PACKAGING OF MICROWAVE AND MILLIMETER-WAVE ELECTRONICS

By

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A DISSERTATION

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

Electrical Engineering – Doctor of Philosophy

2022

ABSTRACT

FLEXIBLE, COMPACT, AND HIGH-POWER-COMPATIBLE PACKAGING OF MICROWAVE AND MILLIMETER-WAVE ELECTRONICS

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This dissertation demonstrates packaging strategies for microwave and millimeter-wave (mm-wave) system integration, realized via additive manufacturing (AM), and specifically aerosol jet printing (AJP), that are mm-wave-capable, flexible, and compatible with high-power applications. These strategies build upon the concept of chip-first packaging that has been previously demonstrated via AJP. Such packaging approaches address the limitations of conventional systems-on-package (SoP)/systems-in-package (SiP) strategies and aim for heterogeneous integration and high functional density. The final SiP/SoP strategy demonstrated in this dissertation achieves improved performance comparing to previously demonstrated packages and interconnects via AM, and additionally demonstrates more material flexibility, improved interconnect reliability, incorporation of diamond platforms as heatsinks for high-power operation, and high-power performance.

The first step in the dissertation is to explore the high-power and temperature capabilities of diamond via basic high-power RF devices. Then, the compatibility of diamond and AJP is investigated by realizing RF components printed on diamond dielectric substrates. Thereafter, the state of the art in additively manufactured interconnects and components is advanced via the demonstration of compact resonant structures at mm-wave, ultra-wideband mm-wave interconnects on non-planar structures, as well as components at near-THz frequencies, all manufactured fully via AJP. Then, AJP-enabled SiP/SoP packaging strategies for mm-wave system integration are laid out and then used for the realization of RF front-end modules. Finally, these strategies are adapted to incorporate diamond platforms, with the final packages demonstrating high RF power performance.

"Prepare the child for the road, not the road for the child."
Folk wisdom of unknown origin

This dissertation is dedicated to my parents, Dimitris and Elena,
who did their best to prepare me, Katerina, and Nasos for the road.

ACKNOWLEDGEMENTS

I would like to express my gratitude to my advisors, Dr. John D. Albrecht and Dr. John Papapolymerou, for their continuous guidance, mentoring, support, and encouragement, all of which made this dissertation possible. I would also like to thank Dr. Premjeet Chahal for his valuable advice and enlightening conversations that assisted me at critical points during my research. Additionally, I want to thank Dr. Patrick Kwon for serving as a member in my dissertation guidance committee and for his useful comments.

It has been my privilege and pleasure to work and take classes with many talented graduate students at MSU. First, I would like to express my deepest appreciation for Dr. Michael Thomas Craton and Dr. Yuxiao He for their mentoring and advice during my time as a graduate student with regards to both research and transitioning from my graduate studies to employment. I would also like to express my gratitude to my former lab members who graduated before me, Dr. Asad Ali Nawaz, Dr. Jubaid Abdul Qayyum, Dr. Si-Wook Yoo, Dr. Shih-Chang Hung, and Ibrahim Kagan Aksoyak for their advice, insight, and friendship, all of which were extremely valuable to me while striding my path towards completing this dissertation. Also, I am grateful to have worked and co-authored publications with Christian J. Herrera-Rodriguez, Adamantia Chletsou, Nick Sturim, and Wesley Spain while working to complete this dissertation. I would also like to thank Dr. Saikat Mondal and Dr. Saranraj Karuppuswami for their useful insight and help.

I would also like to thank the instructors of all my graduate coursework not already mentioned, including Dr. A. Cagri Ulusoy, Dr. Sangmin Yoo, Dr. Jeffrey Nanzer, Dr. Tim Hogan, Dr. Timothy Grotjohn, Dr. Qi Hua Fan, and Dr. Ana Vazquez.

I want to express my gratitude to the MSU employees who assisted me with completing my work and provided me with all the necessary resources, including Brian Wright, Roxanne Peacock, Michelle Stewart, and Meagan Kroll.

Additionally, I would like to thank everyone outside MSU who contributed to my work and with whom I co-authored publications, including Aaron Hardy at the Fraunhofer USA Center

Midwest, Junyu Lai and Dr. Jung-Hun Seo at the University at Buffalo, and Dr. Xing Lan at Space Systems, Northrop Grumman Corporation.

I have been very lucky to be close friends with Dr. Stavros Vakalis, Dr. Serge Mghabghab, Sofia Stathoulia, Sarah Keyes, Dr. Emily Joan Elliott, Dr. Heather Brothers, Ben Greyerbiehl, Mike Lark, and Angelos Lagoudakis. Their fellowship and our moments together gave me a second home in the US, far from home. I have been lucky enough to know Dr. Elias Strangas and Dr. Jane Turner, and I want to thank them for their kindness and for fostering a tiny community that came together for Easter and on other occasions. Also, I would like to thank my dear friends back home, George Chalkiopoulos, Charis Kentrotis, Alex Alexiou, and Yiannis Lytras, for persistently keeping in touch with me.

Finally, I owe my gratitude to my family. To my parents, Dimitris and Elena, who devoted their life to my up-bringing and well being, who made it possible for me to achieve my goals and enter the graduate school, and who have been continuously supporting me ever since. To my siblings, Katerina and Nasos, for being there for me on video calls during the long, grey Michigan winters and when we reunited in Greece in the summer. To my "yiayia" (grandma), Paraskevi, for picking up the phone on Sundays. And finally, to my life partner, Kathryn, who has been a constant source of love, strength, and courage during all our years together, and for supporting me in pursuing my dreams.

The work demonstrated in this dissertation was funded by the Defense Advanced Research Projects Agency (DARPA), a MSU Foundation professorship, and the Department of Energy's Kansas City National Security Campus, operated by Honeywell Federal Manufacturing & Technologies, LLC, under contract number DE-NA0002839.

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KEY TO ABBREVIATIONS

ACPR Adjacent-Channel Power Ratio

Ag Silver

Al Aluminum

AM Additive Manufacturing

AJP Aerosol Jet Printing

Au Gold

B Boron

BCB Benzocyclobutene

BSF Bandstop Filter

CH_4 Methane

CF_6 Hexafluoroethane

COTS Commercial-off-the-Shelf

CPW Coplanar Waveguide

CTE Coefficient of Thermal Expansion

Cu Copper

CVD Chemical Vapor Deposition

CW Continuous-Wave

DI Deionized

DUT Device-Under-Test

EBG Electromagnetic Bandgap

FDM Fused Deposition Modeling

FGC Finite Ground Coplanar

GaAs Gallium Arsenide

GaN Gallium Nitride

GCPW Ground Coplanar Waveguide

GND Ground

GSG Ground-Signal-Ground

H_2 Hydrogen Gas

HCl Hydrochloric Acid

HEMT High Electron Mobility Transistor

HPHT High-Pressure High-Temperature

ICP Induced Coupling Plasma

IM3 Third-Order Intermodulation

InAg Indium Silver

InP Indium Phosphide

IJP Inkjet Printing

LCP Liquid Crystal Polymer

LMM Laser Micromachining

LNA Low Noise Amplifier

LO Local Oscillator

L-P Load-Pull

LPF Lowpass Filter

LRM Line-Reflect-Match

LRRM Line-Reflect-Reflect-Match

LTCC Low-Temperature Co-Fired Ceramic

MD Microdispensing

MMAJP Multi-Material Aerosol Jet Printing

MMIC Monolithic Millimeter Wave Integrated Circuit

Mm-Wave Millimeter-Wave

Mo Molybdenum

MoCu Molybdenum Copper

MPACVD Microwave Plasma-Assisted Chemical Vapor Deposition

MS Microstrip

N_2 Nitrogen

Ni Nickel

NiCr Nickel Chromium

NMP N-Methyl Pyrrolidinone

PA Pneumatic Atomizer

PAPR Peak-to-Average Power Ratio

PECVD Plasma-Enhanced Chemical Vapor Deposition

PI Polyimide

QAM Quadrature Amplitude Modulation

RIE Reactive-Ion Etching

RF Radio Frequency

RTA Rapid Thermal Annealing

SCD Single Crystalline Diamond

Si Silicon

SiGe Silicon Germanium

SiO_2 Sillicon Dioxide

SiP System-in-Package

SLA Stereolithography

SLS Selective Laser Sintering

SMC Surface-Mount Component

SoA System-on-Antenna

SOLT Short-Open-Load-Thru

SoC System-on-Chip

SoP System-on-Package

S-P Source-Pull

Ti Titanium

TL Transmission Line

T/R Transmit/Receive

TRL Through-Reflect-Line

UA Ultrasonic Atomizer

UWB Ultra-Wideband

VCO Voltage-Controlled Oscillator

WPD Wilkinson Power Divider

CHAPTER 1

INTRODUCTION

In recent years, the demand for high-frequency electronics has been increasing steadily without any indication it will come to an end. These electronics at microwave and millimeter-wave (mm-wave) frequencies have applications with significant impact on human societies and their growth potential. Wireless communications for 5G and beyond, wearable electronics, high-data-rate digital electronics, high-precision remote sensing, and imaging for either automotive or medical applications are high-impact areas that need such electronics. Specifically, mm-wave frequencies have attracted interest for imaging applications as they can yield, compared to infrared and optical imaging, higher resolution and smaller modules [10], as well as for mobile communications due to the large bandwidth available at these frequencies [11]. Furthermore, there is a recent trend for digital and analog design to significantly coincide as data rates have been increasing. Even though, traditionally, digital and RF packaging have utilized different approaches, high-speed digital circuits entail a rising number of signal integrity concerns [12], rendering very high-frequency RF design more and more relevant to digital.

System integration for electronics at mm-wave that satisfies the requirements for the aforementioned applications, without introducing performance bottlenecks, entails cost-effective packaging methodologies that will achieve low-loss and broadband interconnects while enabling high functional density and heterogeneous integration (defined in this dissertation as the in-package simultaneous integration of different semiconductor technologies, such as Si, III-V semiconductors, ceramics, etc.). The requirement for effective thermal management comes inherently with increased functional density as integrate circuits (ICs) come closer to each other. Moreover, the use of mm-wave frequencies for wireless communications means high-power amplifier dies will need to be alongside other ICs in compact modules, thus packaging strategies must allow for effective heat dissipation to alleviate thermal stress of ICs.

1.1 Current Electronics Packaging Concepts

1.1.1 State-of-the-Art in Conventional Packaging

Packaging is a crucial part of system integration for semiconductor technologies, and packaging techniques have been evolving alongside circuits to satisfy rapidly changing needs, be it performance, shelf life, or robustness. Despite the continuous efforts for improvement, packaging oftentimes introduces performance bottlenecks that limit the applications of contemporary electronics. There have been plenty of developments in the packaging domain towards strategies that will accommodate the need for high-speed, broadband circuits while, at the same time, increasing functional density, i.e. including more functional system bits or blocks in a smaller area.

The advent of the System-on-Chip (SoC) strategy was a significant step towards this direction. The idea entails an entire system, comprised of smaller, pre-designed and verified functional blocks, realized on a single semiconductor platform [13]. This concept has been used in digital applications, as demonstrated in [14] and [15], but also for microwave, mm-wave, and near-THz electronics. Mm-wave SoCs with integrated antennas for radar sensors at 122 and 245 GHz were discussed in [16]. SoCs for near-THz modules for deep-space communications were discussed in [17]. In [18], a SoC receiver for mm-wave passive imaging at 77 GHz was demonstrated. Nevertheless, since the SoC concept realizes the entire system on a single semiconductor platform, this strategy is limited to one semiconductor at a time, usually defined by the most demanding smaller block. In a complex system comprised of multiple low- and high-frequency, and low- and high-power components, a packaging strategy compatible with heterogeneous integration would allow to design the high-frequency components on InP or GaAs, the high-power components on GaN, and the low-frequency components on cheaper semiconductors such as Si. SoC does not support that, and its material inflexibility introduces design limitations and can significantly increase manufacturing costs.

The concept of the system-in-package (SiP) arrived as an effort to address challenges faced by SoCs and to increase functional density. This concept also targets to further integrate analog and

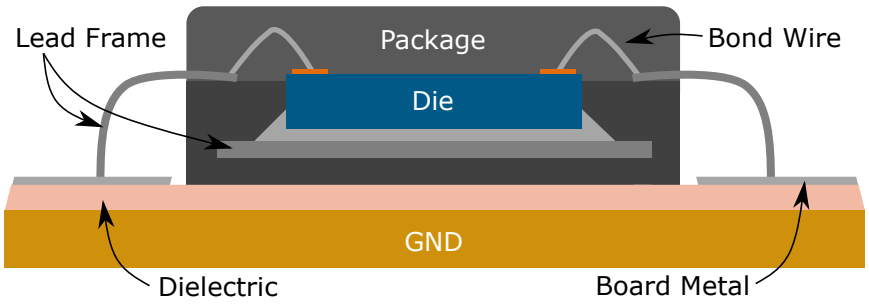


Figure 1.1: Typical SoC packaging concept.

digital circuits [19]. The predominant definition in the literature is a broad one, with the basic idea being to employ dielectric carriers and replace the lead frame (i.e. the in-package metal structures connecting the die to the outside world). These are usually either semiconductor carriers or highly dense ceramic/organic/laminate carriers [20]. People following the first approach have mostly used Si, as in [21–24], but in certain cases other materials such as polyimide (PI) [25, 26], or combination of benzocyclobutene (BCB) and Si [27, 28]. In the second approach, a very popular carrier choice are the Low-Temperature Co-fired Ceramic (LTCC) substrates, as demonstrated in [29–31]. A wide variety of organics has been also used, such as in [32, 33]. A very popular laminate used in SiP applications is Liquid Crystal Polymer (LCP) [34–37] due to its low cost and low-loss characteristics. Other laminates have been used, as well, depending on the application [38, 39]. Both SiP approaches have been evolving towards 3D implementations, in an effort to further increase functional density and improve performance with shorter interconnects, and towards including passive components in-package, as demonstrated in [29].

A more recent term is the System-on-Package (SoP), introduced in [40], which assumes a narrow definition for SiP as "the vertical stacking of similar or dissimilar ICs", or as "a multi-dimensional approach" [41]. This allows room for SoP to emphasize on the integration of various non-IC components in-package, alongside the ICs, such as resistors, capacitors, or antennas. Quite often, however, SiP and SoP are used interchangeably (as in this dissertation). Definitions aside, the evolution of these strategies aims to increase functional density, enable heterogeneous integration, and transcend performance bottlenecks at mm-wave and beyond.

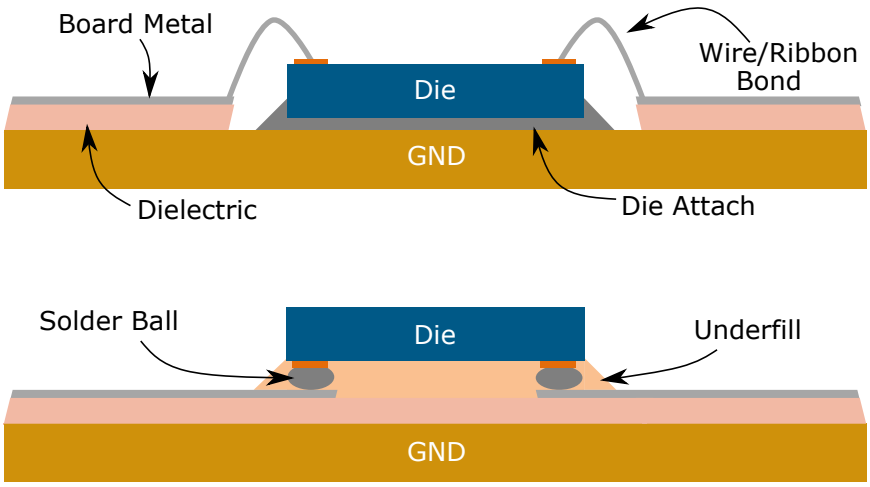


Figure 1.2: Typical conventional strategies for in-package interconnects: wire/ribbon-bonding (top), and flip-chip (bottom).

1.1.2 Performance Bottlenecks

The first performance bottleneck of conventional SiP/SoP approaches discussed here are the interconnects. These strategies predominantly employ chip-and-wire interconnect techniques that utilize wire/ribbon bonds to interconnect the die with the carrier, as shown in 1.2 (top). Mm-wave interconnects like this are attainable, but come with significant design challenges. Precise die placement is required [29] and, more importantly, these interconnects introduce large impedance discontinuities in the RF path that usually have to be compensated with narrowband matching networks [42], which is a significant limitation considering modern circuit performance requirements. Flip-chip interconnects are often employed to bypass wire/ribbon bonding issues, as shown in Fig. 1.2 (bottom), and can attain wideband performance at mm-wave, as demonstrated in [42–44], but also face challenges. Flip-chip technology has high manufacturing costs and introduces strict mechanical design constraints, such as for surface planarity of the die. Moreover, as discussed in [44], there are risks of detuning of microwave circuits, reflections at the interconnects due to dielectric loading, and parasitic coupling.

Material limitations of conventional SiP/SoP strategies, as well, introduce package performance bottlenecks. These strategies require a number of successive lithography and wet/dry etch-

ing steps in a cleanroom environment. These methods are thus confined to a narrow material arsenal, without the capability to use composites or material gradients. Different functional blocks might require different materials, be it for high-frequency or high-power operation, and many of these materials are not compatible with certain processes required for other materials in the same package. High costs also come with the implementation of these processes since numerous pieces of equipment are required in the cleanroom, while large quantities of material are wasted.

Finally, conventional SiP/SoP design lacks flexibility, which is progressively sought in order to achieve higher functional density but also to yield packages compatible with an increasingly wide range of applications. Application-specific packages are unattainable because design changes to adapt the package to a specific application are hard and costly. This results in large complexity in systems, as MMICs that are originally designed to accommodate a variety of applications require additional components to tailor the package to a specific application.

1.2 Additive Manufacturing for SiP/SoP

Additive manufacturing (AM) technologies can provide viable solutions for system integration and packaging at mm-wave frequencies. These technologies can resolve many of the deficiencies of conventional approaches, while simultaneously having an enormous potential for heterogeneous integration and higher functional density. Advantages over conventional packaging strategies come with the inherent flexibility of AM, its wide arsenal of available materials, and its ability to manufacture complicated structures in 3D without use of lithography or other conventional processes. A wide range of dielectric, conductive, magnetic, and other photosensitive or non-photosensitive materials can be selectively deposited in three dimensions, following highly customizable and application-specific designs. This design flexibility is not possible with the strategies discussed in Section 1.1. Furthermore, far less equipment is required with AM and less material is wasted.

Various AM technologies have been employed thus far, predominantly for to manufacture passive RF components, and more lately for SiP/SoP system integration. Stereolithography (SLA) was first used in [45] for various microwave components. Afterwards, various AM technologies have

been used, including fused deposition modeling (FDM) [46], microdispensing (MD) [47], selective laser sintering (SLS), as well as the so-called "direct write" AM technologies, i.e. inkjet printing (IJP) [46, 48] and aerosol jet printing (AJP) [49]. Demonstrated state-of-the-art passives via AM include, for frequencies all the way to THz, waveguides and transmission lines (TLs) [50–53], filters, couplers, and other components [53–57], as well as antennas [46, 50, 58–60].

To the best of my knowledge, the prospect of using of AM to realize a complete SiP/SoP interconnect strategy was first shown clearly in [61] and [62], the first demonstrating printed dielectrics on the side of the chip and the second demonstrating printed dielectrics and metal paths interconnecting the chip, via IJP. A more complete picture of a SiP/SoP strategy via IJP for microwave and mm-wave applications was given by Tehrani *et al.* in [63], in which dielectric ramps on the side of a blank die that was attached on a glass slide and metal interconnects were printed over them with the use of IJP. The first demonstrations of complete SiP/SoP strategies for system integration with the use of AM were demonstrated by Craton *et al.* in [64] and by Tehrani *et al.* [65], published in the same year. In [64], a Si attenuator bare die from 0 to 25 GHz was attached directly on a metal carrier, without use of other dielectric substrates, and then fully packaged via AJP, with printed dielectric ramps and RF interconnects. In [65], a GaAs attenuator die and a GaAs LNA die, attached on a pre-manufactured laminate, were fully packaged via IJP, with printed dielectric ramps, RF interconnects, as well as DC lines for the LNA die, with surface mount components attached for LNA biasing. Craton *et al.* in [66] evolved the methodology followed in [64] to improve performance and extend the strategy up to 67 GHz, opening the path for fully additively manufactured SiP/SoP interconnect strategies at even higher, mm-wave frequencies. Additionally, the term "chip-first" for SiP/SoP was first introduced in [66], as the die is placed first on a metal carrier, with absence of other dielectric substrates, and the entire package, including both dielectric and conductive paths, is designed and fabricated with respect to the die, as shown in Fig. 1.3.

Other AM-enabled hybrid approaches for SiP/SoP interconnects at mm-wave and near-THz have been demonstrated. Ramirez *et al.* [67] used a hybrid approach, employing multiple AM processes alongside laser micromachining (LMM). Ihle *et al.* [68] employed MD and AJP to demon-

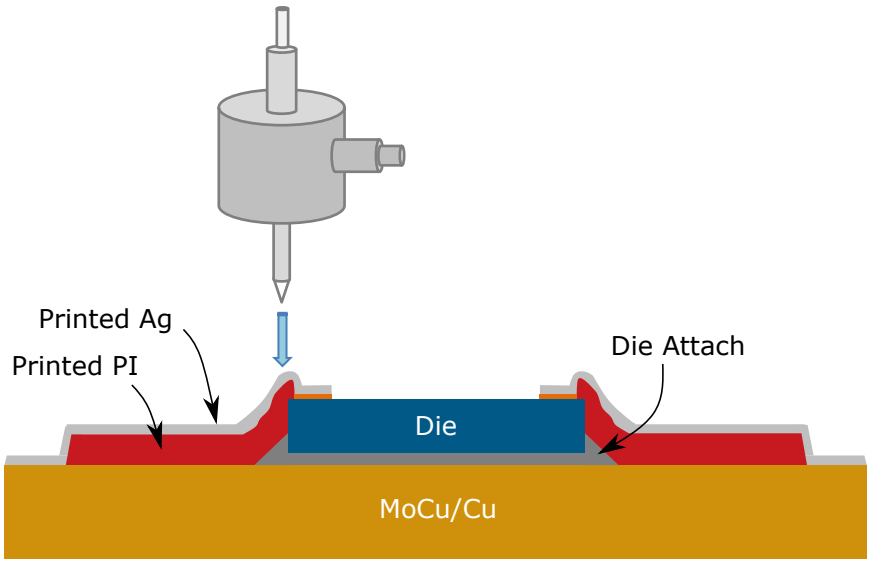


Figure 1.3: AJP-enabled chip-first SiP/SoP interconnect strategy.

strate SiP/SoP interconnects on LTCC. In [69], Oakley *et al.* used lithography to form pockets on a LCP substrate, placed dies in the pockets, filled the gap around the die with epoxy, and printed RF interconnects via AJP. Spain *et al.* [70] went one step further and filled the gap via AJP. Crump *et al.* [71] followed a different approach, also AJP-enabled, printing a dielectric wall around the cavities in LCP and then printed a lower-viscosity dielectric material in the gap to achieve thick dielectric regions for RF interconnects. Albeit these approaches have achieved good mm-wave performance and constitute solid alternatives to conventional SiP/SoP strategies, they demonstrate far less flexibility than the fully AJP-enabled chip-first strategy in [66]. The hybrid methods utilizing pre-manufactured laminates or dielectric carriers are bound to their material limitations, without any great potential for heterogeneous integration. Integrating various dies with different functions in the same package, such as low-frequency, high-frequency, and high-power dies, would require employing a different carrier for each and interconnecting all carriers. This adds complexity and many potential fabrication failure points. Approaches that employ AJP/IJP for metal interconnects alone and utilize additional methods also have limited flexibility and often lack the high resolutions required for very high-frequency interconnects on die.

The chip-first SiP/SoP strategy, fully via AJP, that was demonstrated in [66] was expanded

in [72] to package a microwave power amplifier die alongside capacitors integrated in-package and fabricated via MMAJP as discussed in [73]. This strategy was further used in [74] to package a W-band amplifier die alongside MMAJP capacitors, and in [75] for a fully aerosol jet-printed W-band SoP realizing a transceiver by integrating amplifier dies, a switch die, MMAJP capacitors, and a fully aerosol jet-printed patch antenna.

1.3 Objective of this Dissertation

The objective of this dissertation is to expand on the state of the art in AM methodologies discussed in Section 1.2 towards a complete SiP/SoP strategy for system integration at mm-wave frequencies that will utilize the advantages of previously demonstrated AM strategies and additionally address some of their limitations. AJP is the employed AM technology in this dissertation, and the final SiP/SoP strategy I target follows the fundamentals of the chip-first strategy demonstrated in [66].

Albeit the SiP/SoP prototypes shown in [66, 72, 75] establish the potential for fully printed packages for variety of applications, certain topics were not addressed. First, there has been no demonstration of a particularly high-power package or any integration of heatsink or high-temperature/power semiconductor platform in the package. As discussed earlier in this chapter, there is a lot of interest in high-power applications for SiP/SoP, while effective thermal management becomes an increasingly important parameter of package reliability as functional density increases. A basic idea for the integration of a heatsink in a AM-enabled SiP/SoP strategy was demonstrated in [76], in which a system-on-antenna (SoA) module was shown, but the strategy used was limited to pre-packaged MMICs and showed limited design and material flexibility. This dissertation addresses this deficiency and explores the integration of high-power/temperature semiconductor platforms in AJP-enabled SiP/SoP strategies, as well as the high-power performance of packages manufactured entirely with the use of AJP.

A second area with room for novelty is the diversification of dielectric inks printed in-package in AJP-enabled SiP/SoP strategies. While the printing of dynamically mixed dielectric and nanocomposite inks was demonstrated in [73, 77] in gradients as well as abrupt material changes,

with dielectric constant and loss tangent tuning, a sole dielectric ink was printed for areas supporting the die interconnects and the TLs. In a package that integrates heterogeneous dies, coefficient of thermal expansion (CTE) matching between the die and the surrounding printed dielectrics is essential for package reliability. CTE tuning through mixing of dielectrics with nanocomposites is possible, as discussed in [77, 78]; nevertheless, it has not been demonstrated in-package and around the die. Moreover, as will be discussed in this dissertation, certain dielectric inks, such as PI, introduce package reliability issues when printed adjacent to dies. This dissertation explores more materials and their combination to support RF die interconnects. Printing different dielectric materials for the same package also targets to transcend the limitations of hybrid methods that rely on laminate and dielectric carriers, as discussed earlier. Different dielectric materials can be printed in the same package and in close proximity to the die with abrupt material changes, as will be demonstrated in this dissertation. This allows to accommodate the requirements of each individual die and semiconductor technology, and integrate all separate functional blocks in a single package. A demonstration of different dielectric materials printed around the die was shown in [71], but the package was not fully printed as it utilized a pre-manufactured substrate.

Furthermore, very limited work has been shown on packaging on non-planar and complex surfaces and structures. Conformal antennas have attracted research interest in recent years, but there has been no demonstration of interconnects on non-planar structures or surfaces of significant size, nor any steps towards SiP/SoP strategies on such. There are many applications that would gain from printed packages on non-planar surfaces, such as wearable electronics, electronics on automotive and aircraft parts, and others. Printing on non-planar structures can also enable complex 3D structures integrated in-package and further increase functional density. Additionally, no work has been shown for fully additively manufactured interconnects at near-THz frequencies above the W-band. In this dissertation, I demonstrate a first step towards interconnects on non-planar surfaces, as well as the first fully aerosol jet-printed components above the W-band.

The goal of this dissertation is to demonstrate an alternative SiP/SoP strategy via AJP that will address the deficiencies of previous strategies, as discussed above. The steps towards this

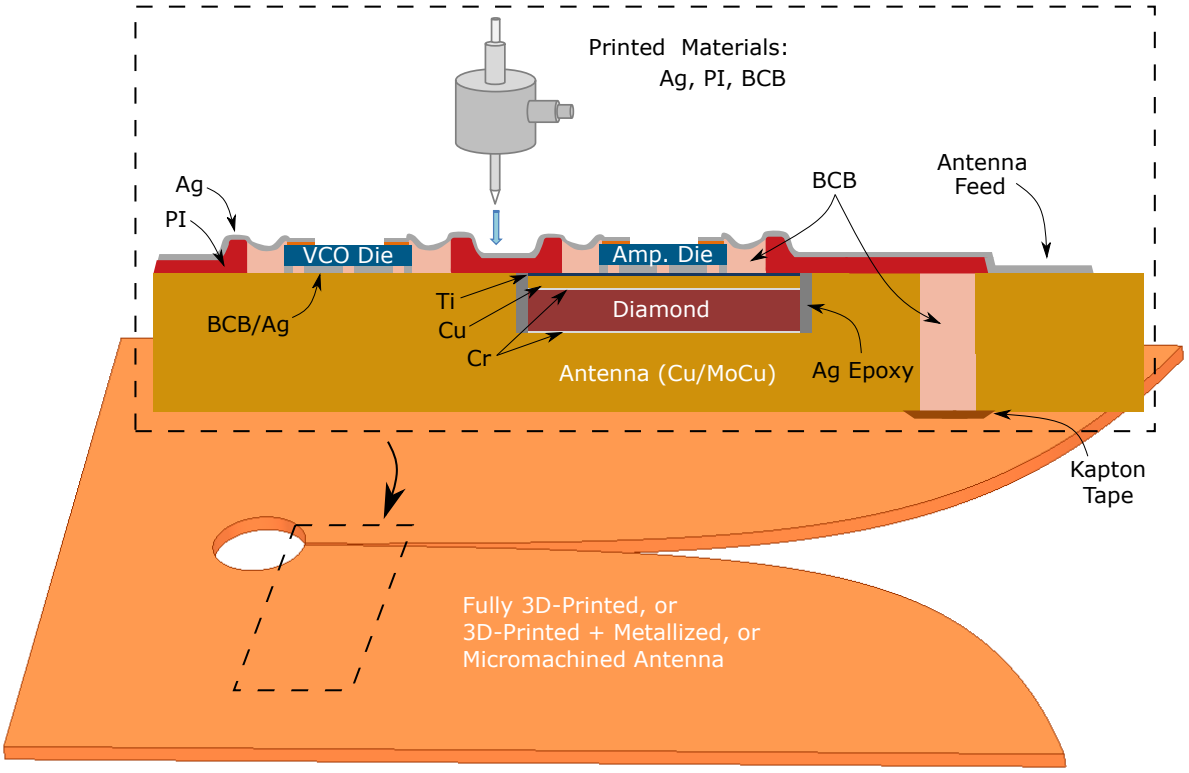


Figure 1.4: Possible AJP-enabled packaging concept for an RF front end transceiver module on-antenna, with two basic dies shown.

strategy are structured and divided into chapters in due order. A final system that can potentially be manufactured following my strategy is demonstrated in Fig. 1.4, in which a RF front end transceiver module can be realized almost exclusively via AM. A diamond platform can be used as a heatsink for the high-power dies, while the rest of the dies can be attached directly on the antenna. All dielectrics and conductive paths, as well as the die attach patterns, can be fully aerosol jet-printed. The antenna can also be fully additively manufactured, as metal structures can be fully 3D-printed as discussed in [79–83]. Only metals on the diamond wafer serving adhesion and RF ground purposes would be sputtered. The chapters of this dissertation are structured as follows.

In chapter 2, I investigate whether diamond is a good semiconductor platform for high-power/temperature applications at high frequencies by demonstrating basic high-power RF structures on diamond. I realize X-band Schottky Barrier Diodes (SBDs) and SBD-based multiplier structures. These components are a first step towards MMIC frequency sources that could out-

perform the current, power-limited ones at mm-wave. Moreover, the performance of these structures indicates that diamond platforms can be included in SiP/SoP strategies for compatibility with high power and temperature.

Chapter 3 expands on the compatibility of AJP and diamond semiconductor platforms. The purpose is to prove that basic RF structures can be additively manufactured on diamond, so that diamond can be included in the SiP/SoP strategy demonstrated later in the dissertation. A mm-wave lowpass filter (LPF) and Ka-band Wilkinson power divider (WPD) are presented.

Chapter 4 expands the current state of the art to give compact, fully additively manufactured components up to near-THz frequencies, as well as interconnects on non-planar structures. Resonators are realized up to W-band, utilizing basic electromagnetic-bandgap (EBG) building blocks to form compact filtering structures that can be integrated into SiPs/SoPs. Morever, TLs and radial stubs at near-THz are demostrated. Finally, ultra-wideband (UWB) transmission lines (TLs) up to W-band are manufactured on non-planar structures significantly larger than the ones reported in the literature at these frequencies.

Chapter 5 proposes a flexible SiP/SoP strategy fully via AJP with use of different dielectrics to support RF interconnects around the die. This strategy bypasses challenges of previous strategies at the die-dielectric interface and allows for the choice of dielectric materials depending on the application. This material flexibility is especially important for high-power and high-temperature applications. Then, this strategy is employed to realize a SoA transmitter module.

Chapter 6 demonstrates the integration of a diamond platform in the SiP/SoP strategy as a heatsink. The basic implementation is shown, with fabrication of the package via AJP on diamond. In addition, high-power RF measurements are demonstrated alongside small-signal measurements.

Finally, chapter 7 gives a conclusion of the dissertation and a summary of possible future work.

CHAPTER 2

HIGH-POWER MICROWAVE COMPONENTS ON DIAMOND

As discussed in Chapter 1, there is a deficiency of SiP/SoP strategies showing the integration of semiconductors with high-power/temperature capabilities. This dissertation addresses that by proposing the integration of diamond platforms in-package. The first step is to demonstrate the high-power and high-temperature capabilities of diamond with basic RF devices. In this chapter, I demonstrate diode [1] and multiplier [2] structures on diamond as a way to show these capabilities that SiP/SoP strategies can exploit, but also to show the general potential of high-frequency devices on diamond for high-power/temperature applications.

Over the years, diamond has become very popular as a candidate for semiconductor applications at microwave and mm-wave frequencies, in the domain of wireless communications, imaging, and sensing. The combination of great electronic, thermal, and mechanical properties it possesses can offer solutions for device integration into highly dense packages when mainstream semiconductor choices are not compatible with the physical stresses that these packages must face. Chemical vapor deposition (CVD) diamond properties are compared to the ones of other, common semiconductors in Table 2.1 [84–86], with diamond comparing favorably as a choice to realize functional blocks operating both at high frequencies and under high-voltage and thermal stress simultaneously. This fact is known in the research community, and plenty of commonly used devices have been realized on diamond, such as power diodes and field-effect transistors (FETs) operating at high voltage, current, and temperature [87–89], while there have also been initial attempts towards realizing diamond-collector heterojunction bipolar transistors (HBTs) [90, 91].

Table 2.1: Comparison of properties and figures of merit (FoM) of CVD diamond with common semiconductors at room temperature

Property/FoM	**Si**	**4H-SiC**	**GaAs**	**GaN**	**GaP**	**InP**	**CVD Diamond**	**Device Benefit***
Dielectric constant	11.7	9.7	12.9	8.9	11.1	12.5	5.7	-
Bandgap (eV)	1.1	3.2	1.44	3.04	2.26	1.34	5.47	High-Temperature Operation
Breakdown Field (MV/cm)	0.3	3	0.4	5	1	5	10	High-Voltage Operation
Electron Saturation Velocity ($\times 10^7$ cm/sec)	0.86	3	0.72	2.5	0.88	0.68	2	High-Frequency Operation
Electron Mobility (cm^2/V/sec)	1450	900	8800	1350	250	4100	4500	-
Hole Mobility (cm^2/V/s)	500	120	400	13	150	150	3800	-
Thermal Conductivity (W/cm/K)	1.5	5	0.56	1.3	1.1	0.68	24	High-Power Operation
Johnson's FoM (JFoM)†	1	1217	1.3	2347	11.6	174	6009	Large Power-Frequency Product

* Larger value of each property/FoM increases the corresponding device benefit.

† Calculated as JFoM $= \left(\frac{E_{\mathrm{M}}\upsilon_{\mathrm{s}}}{2\pi}\right)^2$ and normalized to $\mathrm{JFoM_{Si}}$, where E_{M} is the breakdown field and υ_{s} is the electron saturation velocity [92].

2.1 Schottky Barrier Diodes

The first part of this chapter focuses on Schottky Barrier Diodes (SBDs) on diamond. This type of diodes is omnipresent in electronics for a variety of applications, and the utilization of diamond properties can help provide solutions unattainable with other common semiconductors. In power-conversion systems, the high breakdown field and low conduction resistance of a diamond device can increase the system efficiency and reduce power consumption. The low junction capacitance reported for diamond SBDs [87], on the other hand, yields high cutoff frequencies for fast-switching applications or mm-wave electronics.

Frequency multipliers, rectifiers, and detectors are components widely used in SBD applications, and for these to deliver adequate output power (P_{out}) impedance matching by means of matching networks is required. Diode matching has been predominantly done using S-parameters. However, specifically in the case of SBDs, the diode impedance is a function of the RF power delivered to the diode, ($P_{SBD,in}$), as well as of the carrier frequency, f_0, i.e. [93]:

$$Z_{SBD} = Z_{SBD}\left(P_{SBD,in}, f_0\right). \tag{2.1}$$

Small-signal matching hence introduces inaccuracy when designing SBDs that need to handle high RF power levels. To transcend this problem, active load/source-pull (L/S-P) can be employed to perform large-signal, high-power matching at both input and output sides of the diode. In general, an active L/S-P system can present any impedance on the Smith Chart to the device-under-test (DUT) to optimize the power delivered by the DUT to the load (P_L), i.e. the output power, P_{out}, or other parameters such as linearity or efficiency. An extensive overview of L/S-P techniques for power and linearity optimization is given in Appendix A.

In this Section, I demonstrate the development of high-power RF SBDs on high-pressure high-temperature (HPHT) single-crystalline diamond (SCD) and their characterization for large RF signals, for the first time to the best of my knowledge, via the active L-S/P technique. These devices

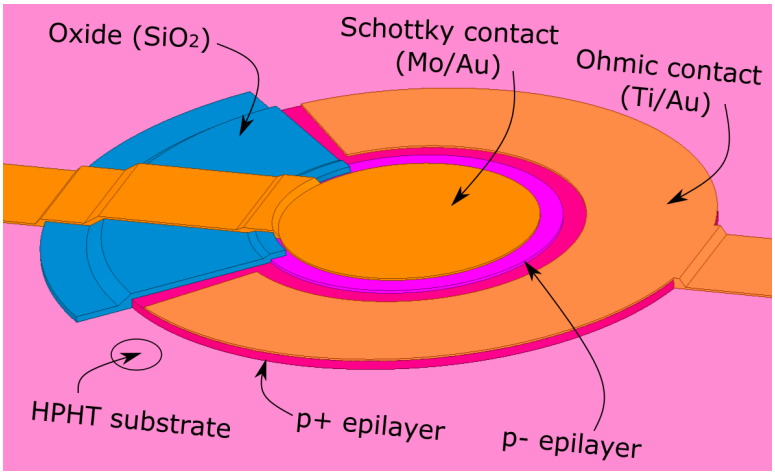


Figure 2.1: Detailed view of a single SBD in ANSYS HFSS©.

were manufactured with conventional methods in a cleanroom environment. The input and output of the SBD were matched to maximize P_{out}. An input power of P_{in} = 34 dBm yielded P_{out} = 33 dBm at f_0 = 10 GHz. These achieved RF power levels are higher than what other RF diodes in the literature have demonstrated, which, alongside the capability to perform harmonic active L/S-P at f_0, $2f_0$, and $3f_0$, demonstrates the potential of active L-S/P characterization of RF diodes as a great asset in designing frequency multipliers, rectifiers, and detectors as functional blocks in high-power RF systems.

2.1.1 Design

The basic diode structure was first designed in Synopsys© Sentaurus Device. Thereupon, further design and optimization was done in ANSYS HFSS© to minimize the device parasitics, such as parasitic capacitances formed between the metal layers and the doped diamond layers, as well as to design the RF feeds that are connected to the diode. A detailed view of the designed SBD is shown in Fig. 2.1. The Schottky contact is formed between a circular metal stack and the lightly boron-doped (B-doped) p^- epilayer (diode anode, or input), while a ring-shaped metal stack and the heavily B-doped p^+ epilayer form the ohmic contact (diode cathode, or output). A SiO_2 layer was designed to isolate the Schottky metal from shorting to the p^+ epilayer. The total parasitic

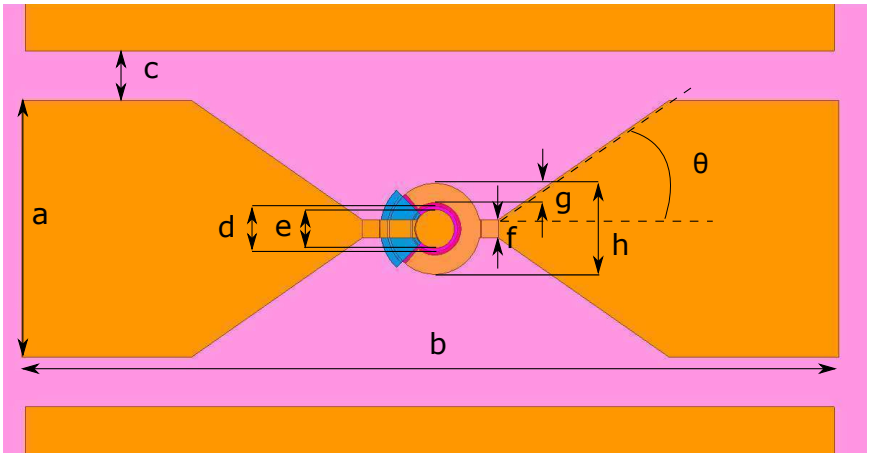


Figure 2.2: The designed SBD structure in ANSYS HFSS© (with units in μm): (a) CPW TL width = 282, (b) structure length = 895, (c) CPW TL gap = 55, (d) p^- mesa diameter = 50, (e) Schottky contact diameter = 42.5, (f) finger width = 20, (g) ohmic ring width = 21, (h) p^+ mesa diameter = 100, (θ) width transition angle = 46°. From [1] ©2020 IEEE.

capacitance is directly related to the diode cutoff frequency, which is given by:

$$f_c = \frac{1}{(2\pi R_s C_t)}, \tag{2.2}$$

where R_s is the diode series resistance and $C_t = C_j + C_{par}$ is the total diode capacitance, with C_j being the junction capacitance and C_{par} the total parasitic capacitance [94]. C_{par}, thus, needed to be minimized. The SBD was designed to have a cylindrical shape in order to decrease the sharp discontinuities and aid in minimizing C_{par}.

The RF feeds connected to the diode were comprise of coplanar waveguide (CPW) transmission lines (TLs), with a designed width transition to connect to the small diode contacts. The CPW TLs were designed and fabricated on-wafer, on the same diamond substrate as the SBDs. The TLs were designed to have a 50-Ω characteristic impedance at 10 GHz. The entire designed structure is shown in Fig. 2.2.

2.1.2 Fabrication

A commercial HPHT SCD type-Ib wafer with lateral dimensions of 5×5 mm^2 and a 3° off-cut angle in the (100) surface orientation was used as the semiconductor platform. This wafer was processed by Aaron Hardy at the Coatings and Diamond Technologies Division, Fraunhofer USA

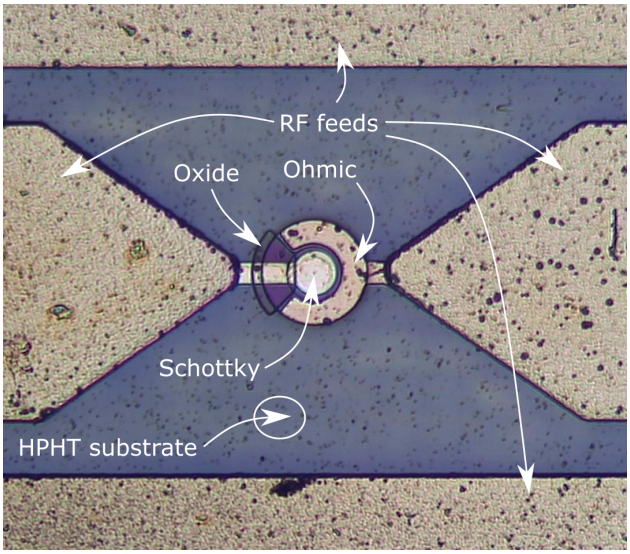


Figure 2.3: Top view of a fabricated SBD.

Center Midwest (Fraunhofer USA CMW). Mechanical polishing using diamond powder and olive oil was performed to reduce surface roughness, followed by a 3 μm reactive-ion etching (RIE) process to remove any sub-surface damage and an acid cleaning process.

Doped diamond growth was done by Aaron Hardy and Cristian J. Herrera-Rodriquez at the Coatings and Diamond Technologies Division, Fraunhofer USA CMW. B-doped diamond epilayer growth on the SCD wafer was done in two separate microwave plasma-assisted chemical vapor deposition (MPACVD) reactors, one for heavily and one for lightly B-doped diamond deposition, with ultra-high purity levels of hydrogen (H_2) and methane (CH_4) process gases. The heavily B-doped epilayer was grown on the diamond substrate first, with the lightly B-doped epilayer grown in a second reactor. The mesa structures of the grown epilayers were defined via a fluorine plasma etching process and an aluminum (Al) hard mask. All remaining fabrication steps were done by Cristian J. Herrera-Rodriquez at the Michigan State University (MSU) Engineering Research Complex (ERC). A SiO_2 layer was grown via plasma-enhanced chemical vapor deposition (PECVD) and patterned lithographically to isolate the Schottky metal from shorting to the p^+ mesa structure. A sputtered titanium (Ti)/gold (Au) (10-nm/200-nm thick) ohmic contact layer was patterned via liftoff to cover the p^+ mesa structure. A thermal annealing process was thereupon done under vacuum at 600°C for 1 h to achieve a carbide formation at the metal-diamond

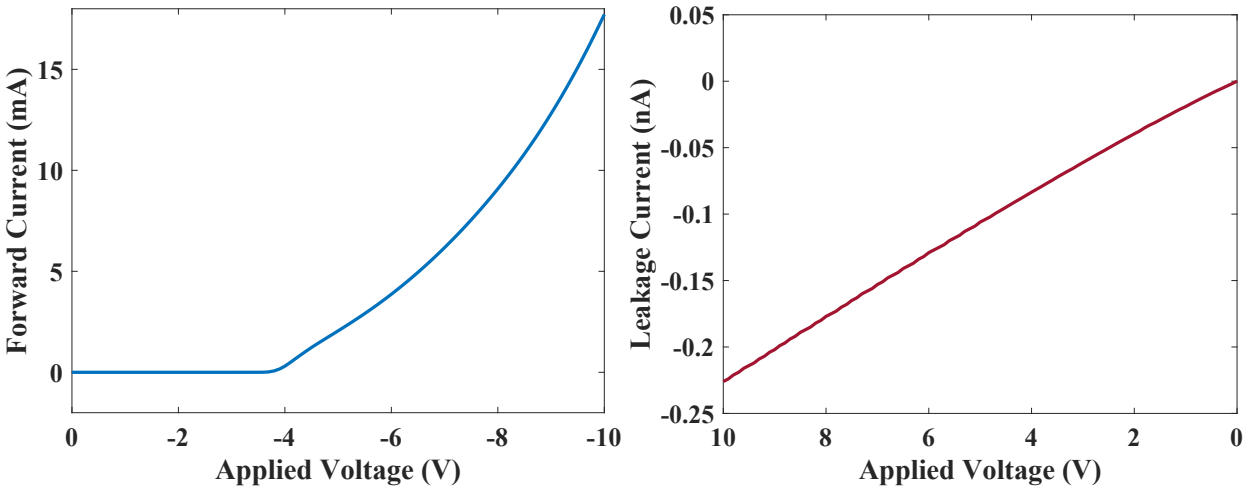


Figure 2.4: SBD DC I-V curves: (a) forward mode, illustrating the forward current, and (b) reverse mode, illustrating the leakage current. From [1] ©2020 IEEE.

contact interface. An oxygen plasma treatment was performed on the wafer to oxygen-terminate the diamond surface prior to the deposition of a Mo/Au (20-nm/200-nm thickness) layer for the Schottky contact, also defined via liftoff, on top of the p^- mesa structure. The final step was the Au plating of the RF structures to a thickness of 3.5 µm. A fabricated diode is shown in Fig. 2.3.

2.1.3 Results

DC measurements were performed first to acquire the diode I-V characteristics and the turn-on voltage. I did a DC voltage sweep using an Agilent B1500A Semiconductor Device Analyzer, and the I-V curves are shown in Fig. 2.4. The turn-on voltage is around -4V and the maximum achieved forward current is around 18 mA at -10 V applied. In reverse mode, a low leakage current is shown in the range of 0 to 10 V applied. Low leakage current and large reverse breakdown voltages are critical for many diode applications, such as high-power multipliers.

I performed all S-parameter measurements using a pair of 67A-GSG-250-C picoprobes and all L/S-P measurements using a pair of 40A-GSG-250-P picoprobes (both by GGB Industries). A short-open-load-thru (SOLT) calibration was performed using a dedicated CS-9 calibration sub-

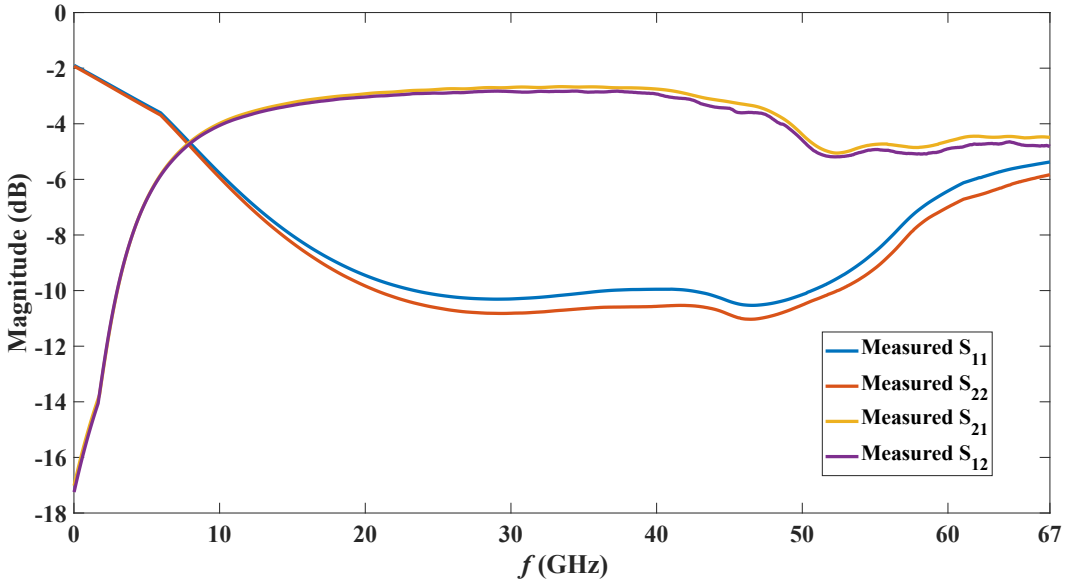


Figure 2.5: SBD S-parameters measured from 10 MHz to 67 GHz, with -5 V applied. From [1] ©2020 IEEE.

strate (GGB Industries) to bring the reference planes to the tips of the probes. Diode S-parameters were measured first, shown in Fig. 2.5, using a MPI TS150-THZ Probe System and the Keysight N5227 PNA from 10 MHz to 67 GHz. Even though SBD impedance matching was not performed before measuring the S-parameters, transmission loss is limited to $<$ 4dB in the range from 10 to 50 GHz, hence f_c is above 50 GHz. S_{11} and S_{22} are maintained below -10 dB in the range from 20 to 50 GHz. The high loss from 10 MHz to around 10 GHz is due to a small capacitance formed between the Schottky contact and the p^+ epilayer. The p^- epilayer is non-conductive at room temperature for low power levels as B forms deep acceptor levels in the bandgap that require very high energies to be activated for low doping concentrations [95]. Therefore, the p^- epilayer acts as a dielectric, forming a capacitance between the Schottky contact and the p^+ epilayer.

To maximize the power delivered to the load through the SBD at a specific frequency and for a specific P_{in}, impedance matching of the SBD input and output needs to be performed under those conditions. Impedance matching will satisfy the maximum power transfer theorem, presenting the SBD input/output with the conjugate of the SBD input/output impedance, i.e. Z^*_{in} and Z^*_{out}, respectively. Post-matching mismatch losses are minimal and power loss is exclusive to the SBD ohmic resistance. I performed SBD large-signal measurements and impedance matching using

a Maury MT2000 Active L/S-P System. The source and load sides correspond to the DUT (i.e. SBD) input and output, respectively. The MT2000 has an open-loop architecture for the purpose of tuning the reflection coefficients, Γ_x, where $x = \{\mathrm{S}, \mathrm{L}\}$, by injecting arbitrary RF signals into the DUT to find the optimal Γ_S and Γ_L (hence Z_S and Z_L) to maximize $\mathrm{P_L}$ [96]. The conditions $Z_\mathrm{S} = Z_\mathrm{in}^*$ and $Z_\mathrm{L} = Z_\mathrm{out}^*$ will apply since the maximum power transfer theorem will be satisfied. I did active L-S/P using continuous-wave (CW) signals for $f_0 = 10$ GHz, $\mathrm{P_{in}} = 34$ dBm, and -5 V applied. I first performed L-P on the SBD to get a first estimation of the optimal Z_L ($Z_\mathrm{L,opt}$) for maximum $\mathrm{P_L}$ ($\mathrm{P_{L,max}}$), and then set Z_L to $Z_\mathrm{L,opt}$ and performed S-P to locate the $Z_\mathrm{S,opt}$ for $\mathrm{P_{L,max}}$. Thereafter, I matched Z_S to $Z_\mathrm{S,opt}$ and performed L-P again. This procedure was repeated until L-P gave me the largest $\mathrm{P_{L,max}}$ possible and conjugate impedance matching was achieved, hence $Z_\mathrm{S,opt} = Z_\mathrm{in}^*$ and $Z_\mathrm{L,opt} = Z_\mathrm{out}^*$. As shown in Fig. 2.7, a $\mathrm{P_{L,max}} = 33.3$ dBm was achieved for $\Gamma_\mathrm{S} = 0.85 + \mathrm{j}0.2$ and $\Gamma_\mathrm{L} = 0.8 + \mathrm{j}0.2$, yielding $Z_\mathrm{in} = 190 - \mathrm{j}320\ \Omega$ and $Z_\mathrm{out} = 200 - \mathrm{j}250\ \Omega$. The discrepancy between Z_in and Z_out could be due to imperfections in the L-P system calibration that cause power measurement errors. The diode structure, including the junction and the metal contacts, can handle 34 dBm at the input and 33.3 dBm at the output. Comparing to other RF SBDs, as shown in Table 2.2, these RF power values are very high.

It is important to note that these results do not indicate the intrinsic upper limits of the RF diamond SBD power handling capabilities. While record or near record, these results were safely within the operating regime of the diodes and were performed multiple times without device degradation. These power-related results, along with the high f_c = 50 GHz of the fabricated device and the availability of active L/S-P at the second and third harmonic, are a motivation to use large-signal harmonic impedance matching to realize high-power, SBD-based multipliers for high-frequency applications.

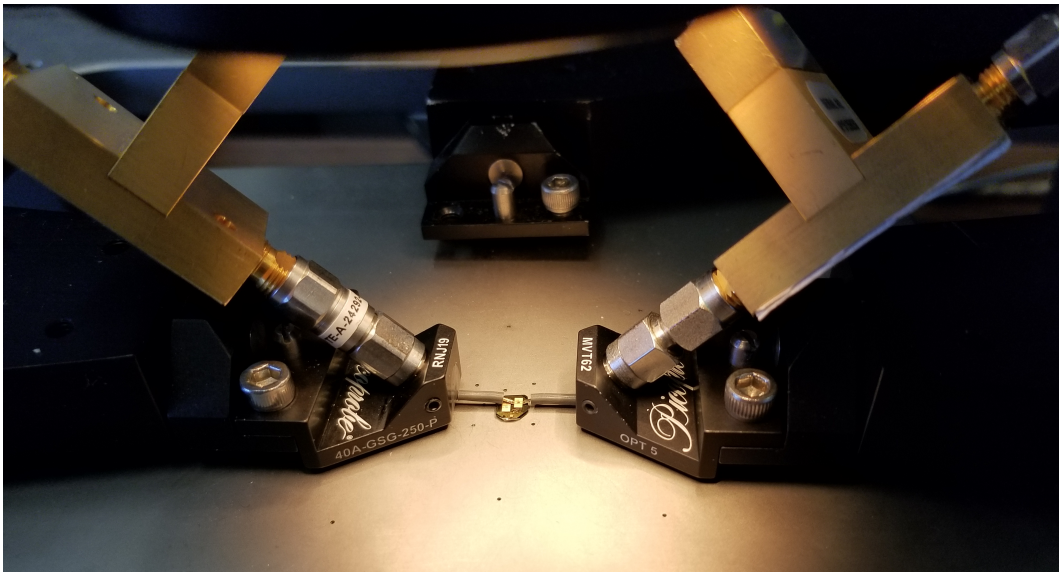


Figure 2.6: Setup for L-P measurements.

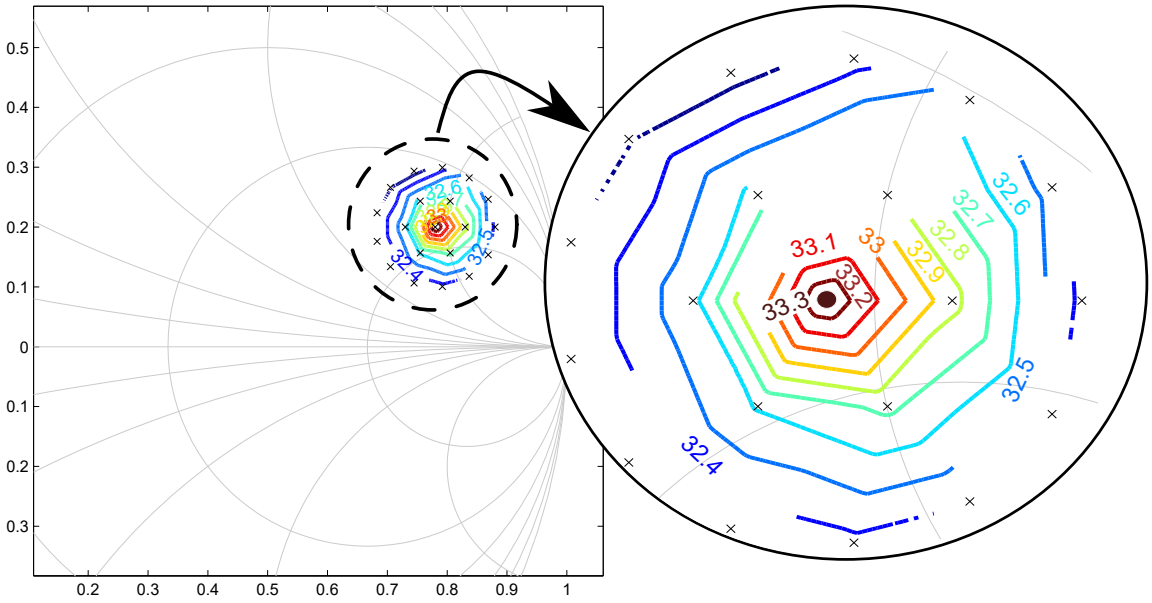


Figure 2.7: P_L contours for $P_{in} = 34$ dBm and an applied voltage of -5 V. Every contour line encloses Γ_L (or Z_L) points that correspond to a specific attained P_L value, or larger. The optimal Γ_L (or Z_L) to maximize P_L is indicated by the dot. $P_{L,max} = 33.3$ dBm is attained for $\Gamma_L = 0.8 + j0.2$, which correspond to an impedance of $Z_L = 200 + j250\ \Omega$. From [1] ©2020 IEEE.

Table 2.2: Comparison with state-of-the-art RF SBD components

Ref.	**Diode Technology**	f_0 **(GHz)**	$\mathbf{P_{in,f_0}}$ **(dBm)**	$\mathbf{P_{out}}$ **(dBm)**
This work	**SCD SBD**	**10**	**34**	**33.3**[‡]
Oishi *et al.* [97][*]	β-Ga_2O_3 SBD	1.4	23.7	N/A
Hamed *et al.* [98][†]	Graphene Diode	10	14	-14[§]
Liu *et al.* [99][†]	GaAs SBD	90	27	20.4[§]
Siles *et al.* [100][†]	GaAs SBD	92.5	27	21[§]

[*] Rectifier application, [†] multiplier application, [‡] P_{out,f_0}, [§] $P_{out,2f_0}$. From [1] ©2020 IEEE.

2.2 Multipliers

The second part of this chapter focuses on high-frequency multipliers on diamond. The multiplier structures presented here utilize the SBDs demonstrated in the first part of the chapter, with the difference that in this case the SBDs are manufactured on chemical vapor deposition (CVD) B-doped diamond rather than HPHT. In recent years, there has been an increased demand for efficient, compact, and high-power-compatible local oscillator (LO) sources for mm-wave and THz applications in the areas of terrestrial and space communications, remote sensing, and spectroscopy. Thus far, people have mostly used Gunn, varactor, and Schottky barrier diodes, with semiconductors such as GaAs and InP, to realize such devices. Albeit such efforts, there is a lack of efficient LOs at frequencies between microwave and far-infrared radiation that can generate signals at adequate power levels for the operational requirements of next-generation instruments [101, 102].

As discussed in Section 2.1, SBDs on diamond have demonstrated great potential to realize functional blocks for high-power frequency sources at mm-wave frequencies. Here, I present the first attempt towards this goal by demonstrating monolithic SBD-based multiplier structures on diamond, and specifically two different doubler configurations, which multiply X-band signals. These structures are compact, occupying an area smaller than 10 mm^2 each. Preliminary small-signal RF measurements are shown from 50 MHz up to 67 GHz. The work demonstrated here shows that, with further high-power RF device improvements and additional characterization of the fabricated structures, MMIC frequency multipliers utilizing diamond SBD as the core device can achieve power levels, at various harmonics, higher than current frequency sources at mm-wave. This would also be the first significant material change in SBD multiplier approaches in decades as the majority of the work to date is on optimizing and integrating GaAs or InP devices.

2.2.1 Design

I designed the multiplier structures utilizing SBDs, bandstop filters (BSFs), and finite-ground coplanar (FCG) TLs, all integrated monolithically on the same diamond wafer. The SBDs were designed following the model presented in Section 2.1 and in [1]. As previously discussed, it is important to minimize the parasitic capacitances between the metal contacts, diode interconnects, and doped diamond epilayers. A reduction of parasitic capacitance values increases the diode cut-off frequency, which needs to be above the desired harmonics generated by the multiplier. The diode metal contacts are interconnected to the TLs through contact-to-TL transitions. FGC TLs were chosen over CPW due to their compact nature, since their GND planes are narrower. They also overcome the parasitic parallel-plate waveguide mode issues of CPW TLs [103]. They were also chosen over microstrip (MS) lines, as FGC lines do not have characteristics that significantly depend on the substrate thickness, like MS lines. The FGC TLs are designed with a 50-Ω characteristic impedance.

Two separate isolation networks are necessary in each configuration for doubler operation, on the input/output sides, respectively. These networks trap unwanted frequencies on each side and are realized as EBG resonator-based BSFs, as demonstrated in [5]. These EBG resonator structures are discussed in more details in Chapter 4, wherein they are fabricated fully via AJP and are measured up to W-band. Since the goal here is to operate the doublers multiplying 10-GHz signals, I designed the BSFs to trap the signal at 20 and 10 GHz at the input and output, respectively. I designed two doubler configurations, the first one (configuration A) utilizing a single series diode and the second one (configuration B) two diodes in parallel. I designed all structures to have symmetry around the center conductor in order to suppress the coupled slotline mode supported by the FGC TLs [104]. As before, I used ANSYS HFSS© minimize the diode parasitics and design the TLs, and additionally the BSFs. All designs are shown in Fig. 2.8.

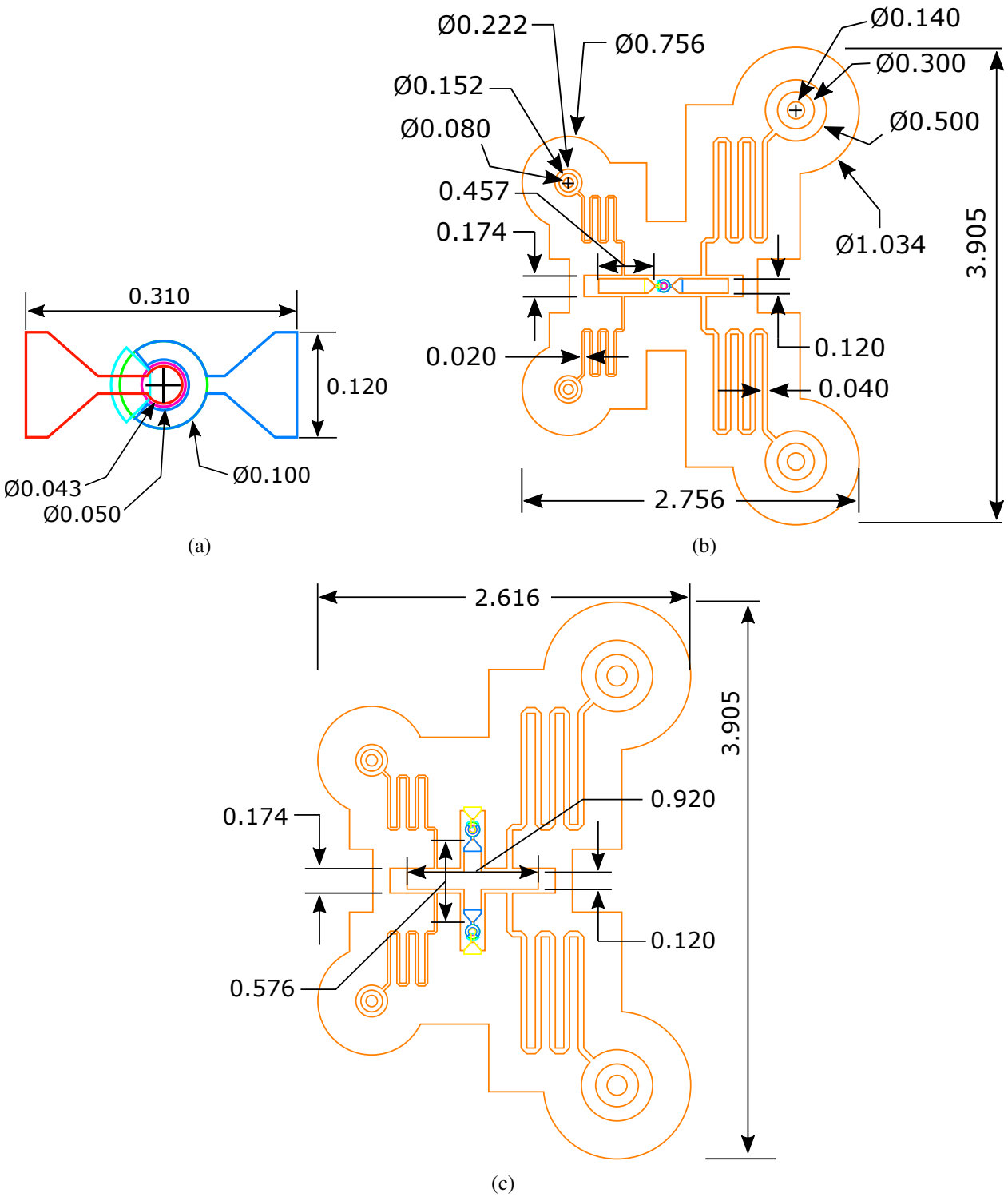


Figure 2.8: Layout of designed structures, with dimensions in mm: (a) SBD used in doubler structures, (b) doubler per configuration A (series), and (c) per configuration B (parallel). From [2] ©2021 IEEE.

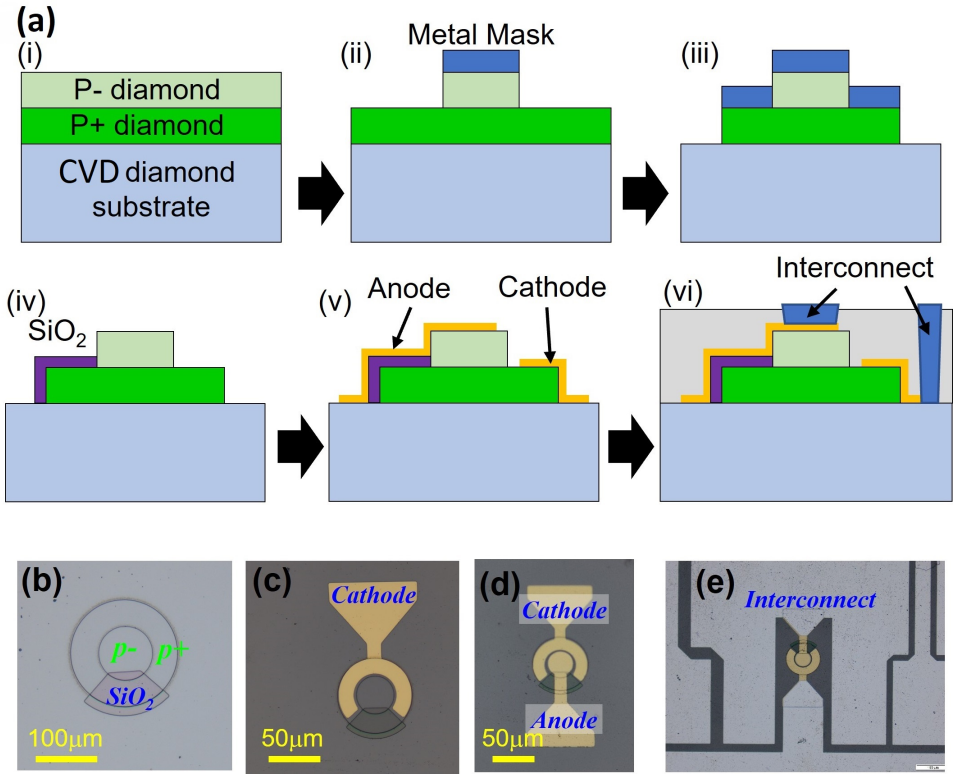
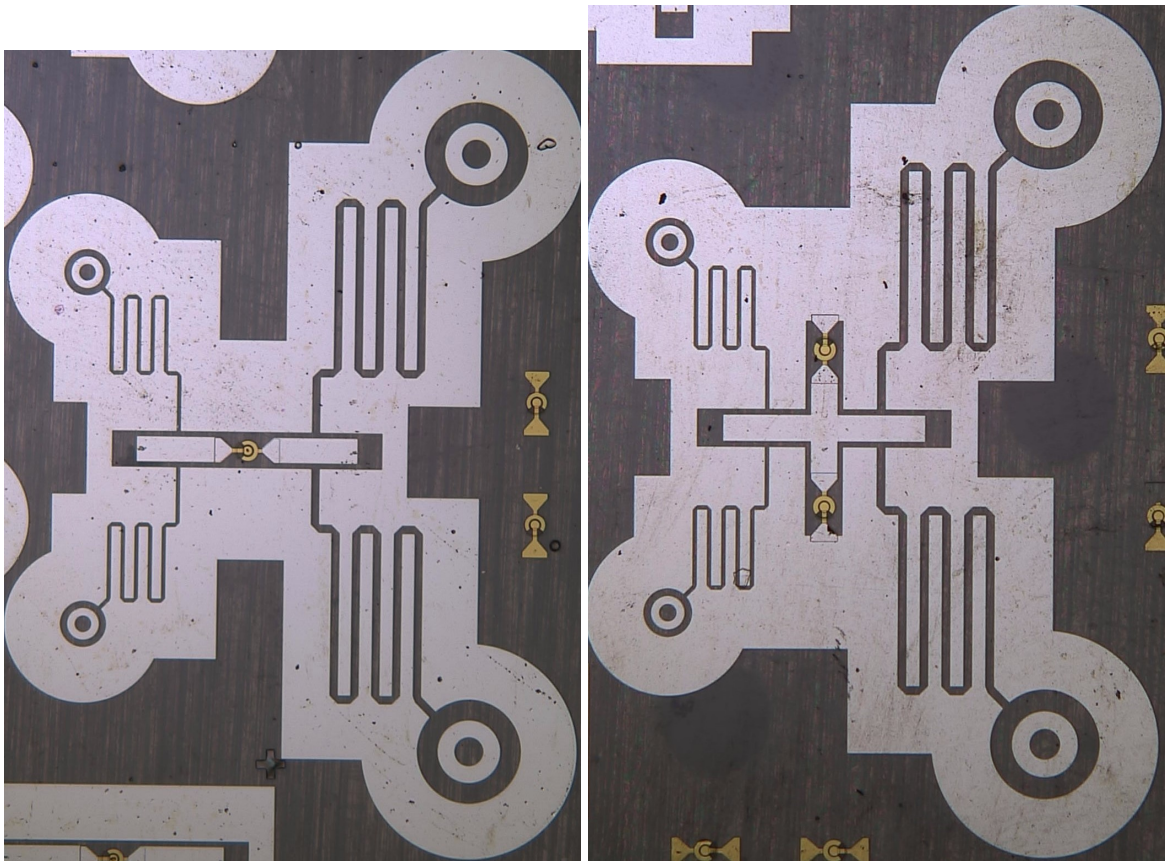


Figure 2.9: (a) Schematic illustration of the device fabrication process flow: (i) p^-/p^+ diamond epitaxy growth on undoped CVD diamond substrate, (ii) mesa etching using a Ni/Ti metal mask to define p^- layer, and (iii) p^+ layer, (iv) SiO_2 insulation layer deposition via PECVD, (v) metallization via e-beam evaporation to deposit Ti/Au cathode (Ohmic contact) and Mo/Au anode (Schottky contact), and (vi) metallization with 1.5-μm-thick Ag for the interconnection. (b)-(e) Microscopic images taken during the fabrication step. From [2] ©2021 IEEE.

2.2.2 Fabrication

The fabrication of the diamond SBD-based doubler structures follows similar steps as the ones for the diamond SBDs in Section 2.1, but with some considerable differences. The fabrication steps are shown in Fig. 2.9. A commercial CVD SCD wafer with lateral dimensions of 5×5 mm^2 and a 3° off-cut angle in the (100) surface orientation was used. As before, mechanical polishing was performed to reduce surface roughness, followed by a 3-μm RIE to remove any sub-surface damage and an acid cleaning process. These initial processes were done by Aaron Hardy at the Coatings and Diamond Technologies Division, Fraunhofer USA CMW.

All following steps were done by Cristian J. Herrera-Rodriquez at the MSU ERC, and by Junyu



(a) (b)

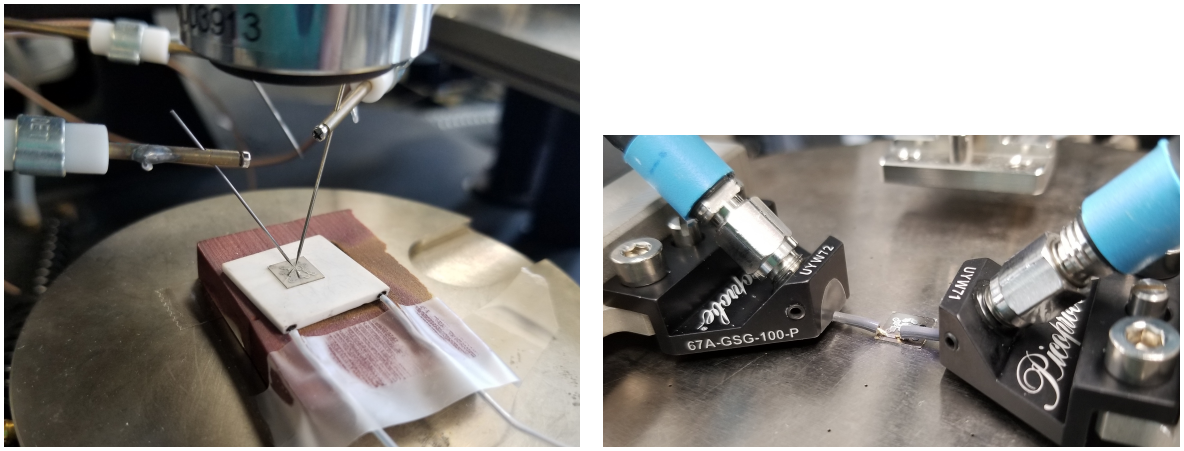
Figure 2.10: Overview of the two fabricated diamond SBD doubler structures: (a) configuration A (series), and (b) configuration B (parallel). From [2] ©2021 IEEE.

Lai and Jung-Hun Seo at the University at Buffalo, the State University of New York. B-doped diamond epilayer growth (lightly and heavily doped), was performed on two separate MPACVD reactors with ultra-high purity levels of H_2 and CH_4 process gases. As before, the p^+ epilayer was grown on the diamond wafer first in the first reactor, followed by the lightly p^- epilayer in the second reactor. The epilayer mesa structures were defined with a disk shape nickel (Ni)/Ti etching mask and an induced coupling plasma (ICP) etcher using hexafluoroethane (CF_6)/O_2 gases, as shown in Fig. 2.9(ii)-(iii). The p^- epilayer has a thickness of 430 nm and a B concentration of 5×10^{16} cm^{-3}, while the p^+ epilayer has a thickness of 930 nm and a B concentration of 10^{20} cm^{-3}. A 300-nm-thick SiO_2 was again deposited via PECVD to electrically isolate the anode and

cathode. A molybdenum (Mo)/Au metal stack (Mo: 20 nm/ Au 200 nm) and a Ti/Au metal stack (Ti: 20 nm/ Au: 200 nm) were deposited via electron-beam evaporation (E-beam) on the p^- and p^+ layers to form a Schottky contact (anode) and ohmic contact (cathode), respectively, as shown in Fig. 2.9(v). The device then underwent a thermal annealing process at 600 °C for 1 min using a rapid thermal annealing (RTA) system in a N_2 environment to further lower the contact resistance of the ohmic contact. Finally, 1.5 μm of Ag were deposited to form the interconnections and RF paths, configuring the diamond multiplier. Figures 2.9(b)-(e) show microscopic images taken during the fabrication process. The fabricated structures are shown in Fig. 2.10. The design is compact, with each configuration occupying an area smaller than 10 mm^2, whereas each diode (including interconnects) an area smaller than 0.037 mm^2.

2.2.3 Results

The first step in the measurements process was to measure the DC I-V characteristics of the fabricated SBDs that are utilized in the doubler structures. DC measurements were performed by Junyu Lai and Jung-Hun Seo at the University at Buffalo, the State University of New York using a Keithley 4200 SCS semiconductor parameter analyzer in a darkbox, and verified by me and Cristian Herrera-Rodriguez at MSU using an Agilent B1500A Semiconductor Device Analyzer, with my DC measurement setup shown in Fig. 2.11a. Fig. 2.12 shows I-V curves measured from six different SBDs on the same wafer. The ideality factor is found to be n = 1.13, following the method outlined in [105]. The good uniformity of the I-V curves and the small ideality factor indicate that the p^- and p^+ diamond layers were grown uniformly and without significant defect sites. One thing to note is that the on-state SBD resistance values, as observed at DC, show that the p^- layer thickness and doping conditions can be significantly improved without compromising the reverse breakdown at any reasonable RF power level. The forward current could be significantly increased when operating at elevated temperatures where a greater fraction of the B dopants would be ionized. The turn-on voltage for the fabricated SBDs is among the lowest reported for diamond, which was a significant design limitation. For the more common high-power diode applications



(a) (b)

Figure 2.11: Measurement setup for: (a) DC I-V, and (b) S-parameters.

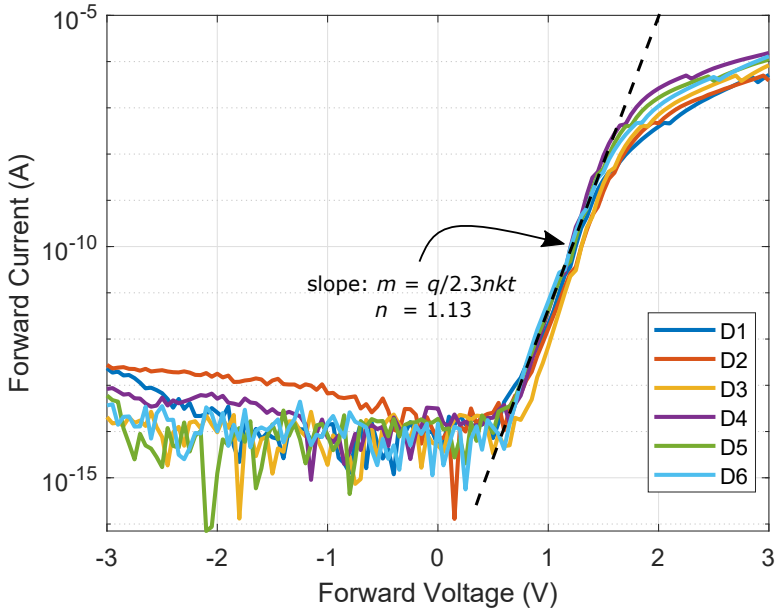


Figure 2.12: DC I-V curves measured from six different SBDs on a single CVD wafers with the ideality factor of $n = 1.13$. From [2] ©2021 IEEE.

with much thicker epilayers to support breakdown voltages at kV, the on-state voltage threshold is often above 3 V.

I performed small-signal RF measurements from 50 MHz up to 67 GHz using two 67A-GSG-100-P picoprobes (GGB), an MPI TS150-THZ Probe System, and a Keysight N5227 PNA. A line-reflect-reflect-match (LRRM) calibration was performed using a CS-5 (GGB) dedicated calibration

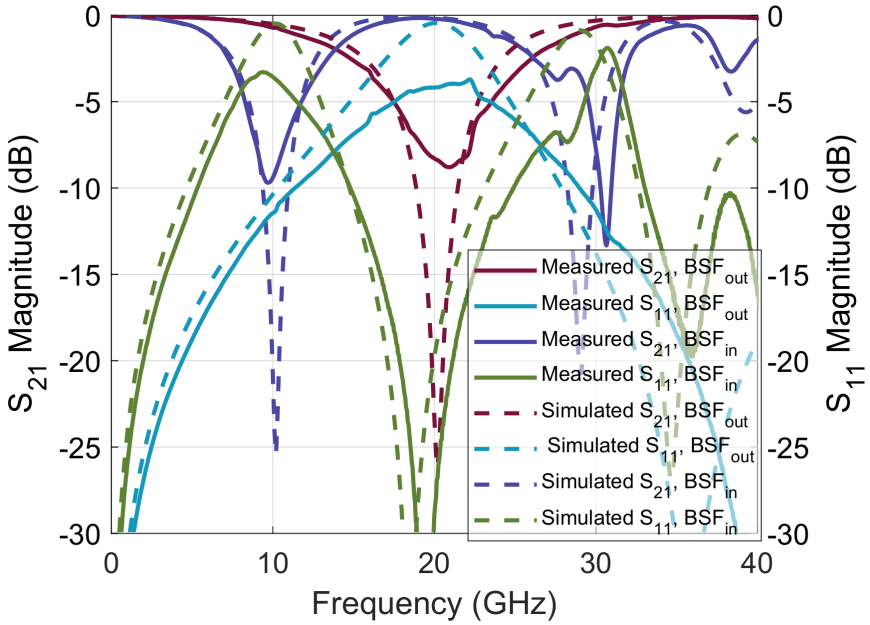
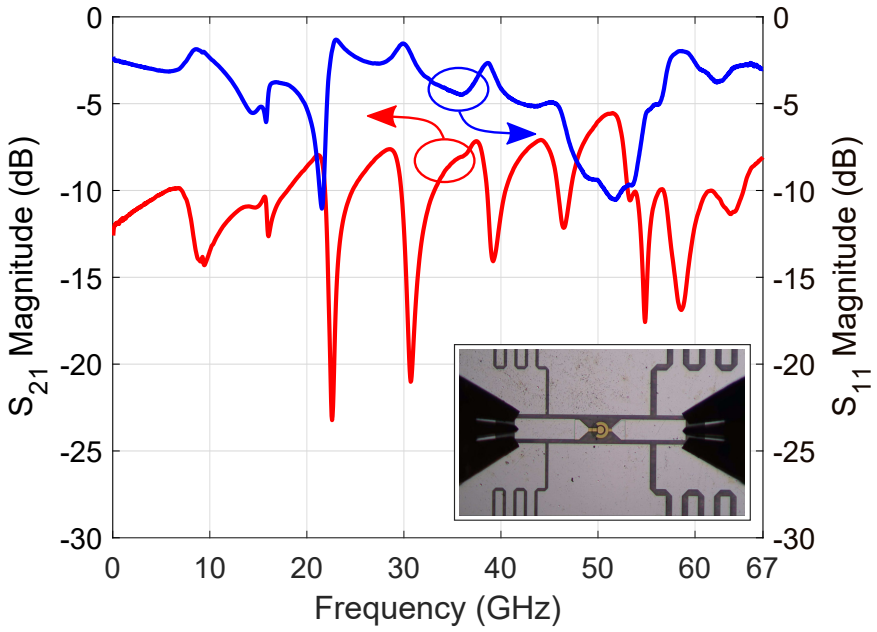
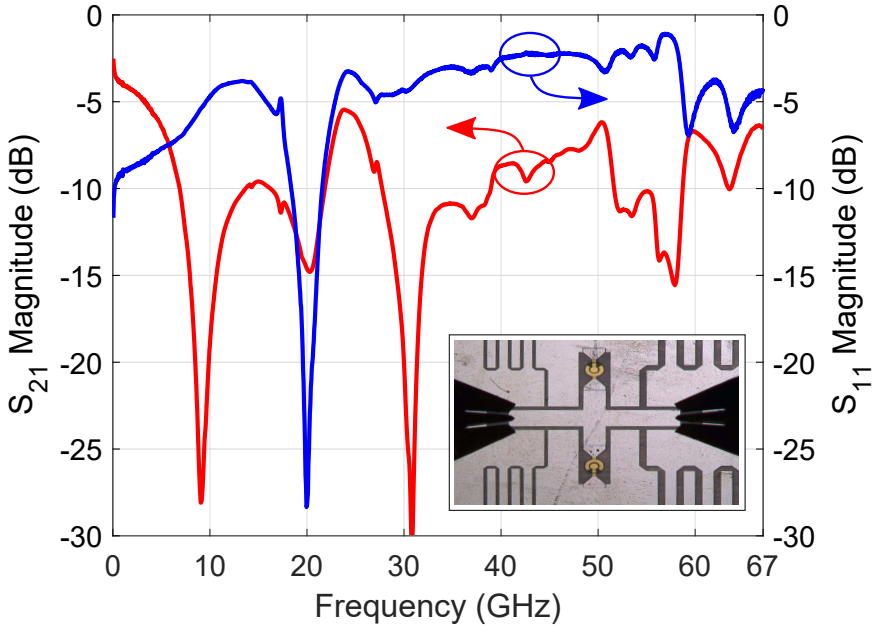


Figure 2.13: Measured vs. simulated S-parameters for the fabricated input and output BSFs. From [2] ©2021 IEEE.

substrate to bring the reference planes to the tips of the probes. I first measured S-parameters for separate input and output BSFs, fabricated on the same wafer as the doubler structures. The BSFs provide resonances at the designed frequencies of 20 and 10 GHz, respectively, allowing them to block the corresponding frequencies, as shown in Fig. 2.13. I then measured S-parameters for the two doubler configurations under a forward bias of 5 V, which performed as expected. In Fig. 2.14a, S_{21} is minimum at -14 dB near 10 GHz and peaks to -7 dB near 20 GHz, providing output isolation from the fundamental and allowing the signal to pass at the second harmonic. In Fig. 2.14b, similar behavior is observed, with S_{21} values of -28 dB near 10 GHz and a peak to -7 dB around 23 GHz. Transmission at 20 GHz is limited due to mismatch, but it can be improved for high power via active L/S-P, as demonstrated in Section 2.1, to design matched circuits on-wafer. The entire structure can be characterized via L/S-P and the optimal matching conditions can be found to maximize P_{out} at $2f_0$. Input and output matching networks can then be added, or the input and output isolation networks and transmission lines can be modified accordingly.



(a)



(b)

Figure 2.14: Measured S-parameters for the fabricated (a) doubler per configuration A, and (b) doubler per configuration B. From [2] ©2021 IEEE.

2.3 Conclusion

This chapter demonstrates basic high-power RF structures monolithically realized on diamond. The power levels demonstrated for the SBDs are higher than other RF diodes in the literature. The initial RF multiplier structures are a first step towards MMIC frequency sources on diamond that can potentially outperform the current, power-limited ones at mm-wave frequencies and beyond. In addition, this chapter demonstrates the general high-power/temperature capabilities of diamond and establishes that diamond platforms would be a useful addition in SiP/SoP strategies seeking to provide effective thermal management in a variety of applications.

CHAPTER 3

ADDITIVELY MANUFACTURED MM-WAVE COMPONENTS ON DIAMOND

In chapter 2, I discussed the high-power/temperature capabilities of diamond and basic RF devices, demonstrating high-power measurements and the potential to integrate diamond into RF systems, either as the semiconductor platform for high-power devices or as a heatsink to alleviate dies from thermal stress. This chapter focuses on demonstrating fundamental compatibility of diamond with AJP manufacturing processes. It is important to demonstrate a basic compatibility first, before attempting to integrate diamond into a complete AJP-enabled SiP/SoP strategy.

I show this basic compatibility by realizing basic RF passives on diamond via AJP, using diamond as the dielectric substrate. This chapter demonstrates a LPF [3] and a WPD [4] printed on diamond and measured at mm-wave. Both are comprised of grounded CPW (GCPW) launches that transition to MS TL parts through via-less transitions on top and a ground plane on the bottom side of a diamond wafer. All conductive paths for the LPF were fully printed with Ag ink. For the WPD, the resistor is a nickel chromium (NiCr) resistor manufactured via a thin-film process, while all conductive paths were printed with silver (Ag) ink. The LPF was measured from 10 MHz to 67 GHz, and the WPD from 22 to 40 GHz. The results demonstrate the potential for integration of diamond platform into packaging concepts via AJP.

3.1 Design

3.1.1 LPF

To design the LPF, I implemented the stepped-impedance prototype and followed the methodology in [106]. I chose to include seven MS TL elements to yield a 0.5-dB equal ripple response, a cutoff

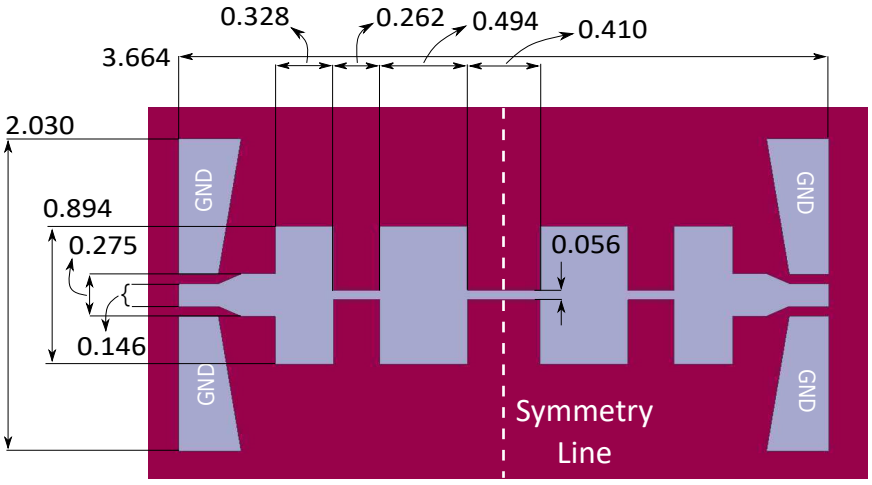


Figure 3.1: Top view of the designed LPF in ANSYS HFSS©(in units of mm, with bottom GND plane everywhere). From [3] ©2020 IEEE.

frequency at 40 GHz, an insertion loss of 30 dB at 50 GHz, and a characteristic impedance of 50 Ω at the input and output. The design is shown in Fig. 3.1. The stepped-impedance prototype utilizes MS TL elements with two different characteristic impedances, 20 and 120 Ω, and the design is symmetric with respect to the middle 120-Ω element. The first and last 20-Ω elements are terminated to 50-Ω MS TLs leading to 50-Ω GCPW launches though via-less GCPW-to-MS transitions as in [107]. The dielectric substrate was assumed to be 0.2-mm thick HPHT diamond with ϵ_r = 5.7, and a ground plane was designed on the entire bottom side of the substrate. The LPF was optimized in ANSYS HFSS©.

3.1.2 WPD

A WPD ideally splits the input signal equally into two output signals, with the resistor isolating the two output ports. The designed WPD is shown in Fig. 3.2. All three ports utilize 50-Ω GCPW launches for probing, as in the case of the LPF, which lead to 50-Ω MS TLs through via-less transitions. The 50-Ω MS on the input side splits into two λ/4-transformer MS TLs with an characteristic impedance of $Z_0 = 50\sqrt{2} = 70.7\ \Omega$ that are isolated by a NiCr 100-Ω resistor. The resistor was designed to make the WPD as compact as possible, and thus I chose a curved shape as shown in Fig. 3.2. I also needed to design a resistor width that will be feasible to be fabricated

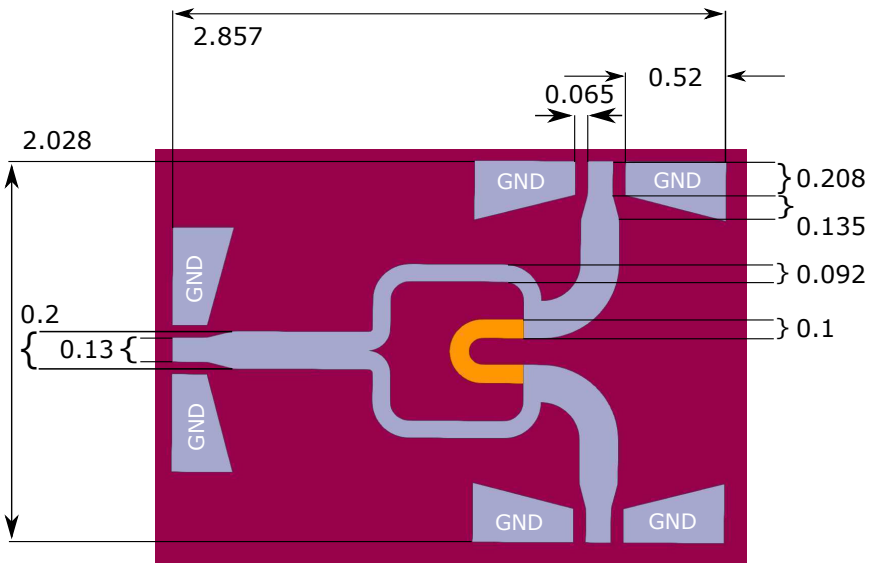


Figure 3.2: The designed WPD in ANSYS HFSS©(in units of mm, with bottom GND plane everywhere). From [4] ©2020 IEEE.

following the thin-film process that will be described in Section 3.2, so I chose the width to be w_{res} = 100 µm. With the resistor width chosen, the resistor length l_{res} was chosen to achieve

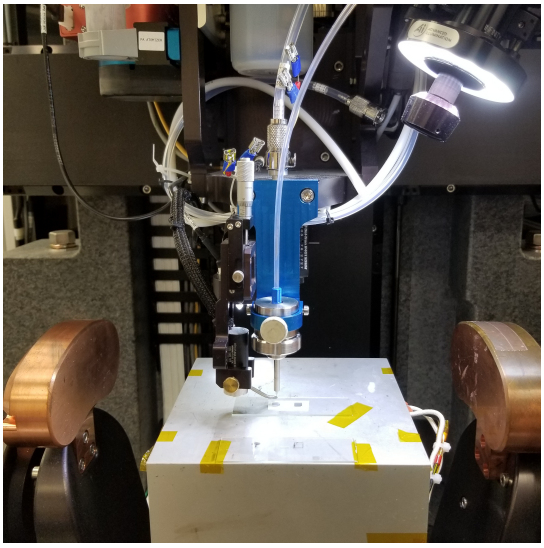
$$\text{R}_{\text{res}} = \rho \cdot l_{\text{res}}/(t_{\text{res}} \cdot w_{\text{res}}) = 100\ \Omega, \tag{3.1}$$

where $t_{\text{res}} = 120$ nm is the designed thickness of the resistor and $\rho \simeq 1.5 \times 10^{-6}\ \Omega$·m is the NiCr resistivity. In this case, the dielectric substrate was assumed to be 0.15-mm thick HPHT diamond with ϵ_{r} = 5.7, and a ground plane was designed on the entire bottom side of the substrate. The TLs were optimized in ANSYS HFSS©.

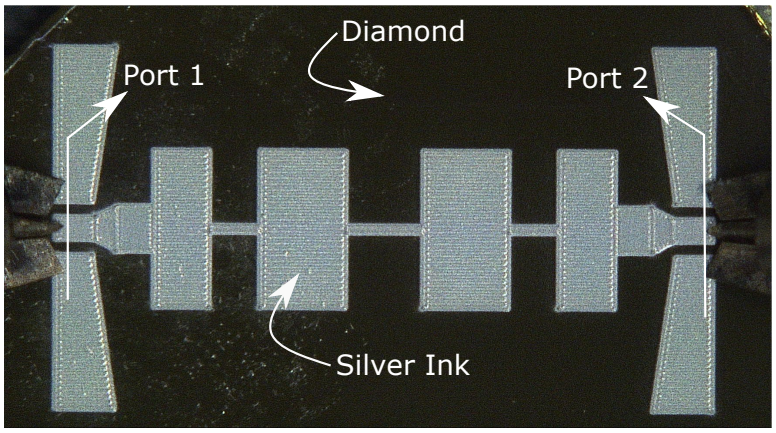
3.2 Fabrication

3.2.1 LPF

The diamond substrate was a commercially purchased HPHT SCD wafer, with (100) crystal oriented top and bottom surfaces, and was processed by Aaron Hardy at the Coatings and Diamond Technologies Division, Fraunhofer USA CMW. The wafer was cut to a thickness of 0.2 mm with an infrared laser and then mechanically polished to a thickness of 0.15 mm on a cast iron polishing wheel with diamond powder and olive oil.



(a)



(b)

Figure 3.3: (a) Overview of the Optomec Aerosol Jet 5X printer setup at Michigan State University during printing, and (b) a fabricated LPF on diamond, with the two measurement ports indicated. From [3] ©2020 IEEE.

All TLs and the bottom ground plane were manufactured via AJP using an Optomec Aerosol Jet 5X Printer. Six layers of Ag ink were printed to achieve a thickness of 6 µm on top and bottom. The bottom ground plane was printed and sintered first, followed by printing and sintering of the LPF on the top side. The Ag ink consisted of 25 wt.% Clariant Prelect TPS 50 + deionized (DI) water and was cured at 180 °C for 5 h, with details of the thermal processing discussed in Appendix B. The fully fabricated LPF is shown in Fig. 3.3b.

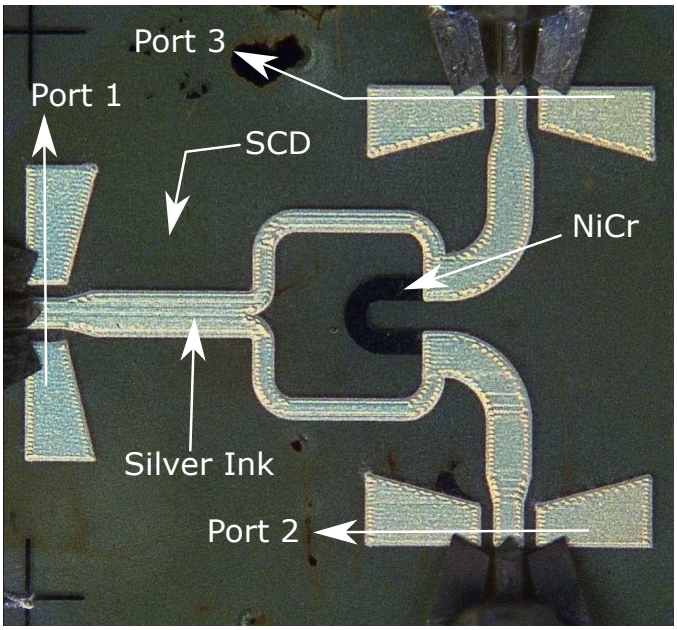


Figure 3.4: A fabricated WPD on diamond, with the three measurement ports indicated. From [4] ©2020 IEEE.

3.2.2 WPD

The WPD was fabricated on the same type of HPHT SCD wafer as the LPF after following the same polishing process, with a final thickness of 0.15 mm. The NiCr resistor was fabricated by Cristian Herrera-Rodriguez with a combination of thin-film deposition and lithography. First, the designed resistor was patterned on the diamond surface via lithography using the AZ nLOF 2020 negative photoresist and the AZ 726 MIF developer. Then, NiCr was deposited on the surface via DC magnetron sputtering under a process pressure of 5 mTorr and at a power level of 90 W. The fabricated resistor was realized with a final step of liftoff using the AZ 400T photoresist stripper. The realized resistor thickness was measured to be 186 nm using the Dektak 6M Profilometer. Fabrication of the remaining parts of the WPD come after the resistor. All TLs and the bottom ground plane, as in the case of the LPF, were manufactured via AJP using an Optomec Aerosol Jet 5X Printer by printing Ag ink. The ground plane was printed first on the entire bottom side of the diamond wafer and then cured. The TLs were printed on the top side, making proper contact with the fabricated NiCr resistor, and then cure. All Ag was cured at 180 °C for 5 h. Five layers of Ag were printed for a thickness of 5 μm. The fully fabricated WPD is shown in Fig. 3.4.

3.3 Results

All measurements for the LPF and the WPD were taken using a MPI TS150-THZ probe station and a Keysight N5227 PNA. For the LPF, I used two 67A-GSG-250-C picoprobes (GGB Industries), while for the WPD I used three 40A-GSG-250-P-OPT5 picoprobes (GGB Industries). In all cases and before measuring the fabricated components, SOLT calibration was performed to bring the reference planes to the tips of the probes.

3.3.1 LPF

The simulated and measured results for transmission (S_{21}) and reflection (S_{11} and S_{22}) ratios are shown in Fig. 3.5 and 3.6, respectively, in the frequency range from 10 MHz to 67 GHz. The measured results at selected frequencies are summarized in Table 3.1. The measured results are very close to the simulated ones. The LPF cutoff frequency is close to the designed one at 40 GHz and the measured loss at 50 GHz is 25.8 dB, with the measured transmission rolloff closely following the simulated one. The LPF is low-loss in the pass-band. The high loss at low frequencies is due to the absence of vias in the GCPW-to-MS transition, as top and bottom grounds are not connected and there is no DC return path. Also, increased noise can be observed in the measurements at low frequencies for both transmission and reflection coefficients, since little to no power is coupled from the ground pads to the bottom ground plane. Similar behavior has been observed in [53]. Nevertheless, measured and simulated performance has good agreement and the LFP exhibits the desired behavior from 10 to 67 GHz.

3.3.2 WPD

The WPD was designed to achieve an equal power split, which would ideally yield a transmission loss on each branchby 3 dB. The measured performance for the WPD is shown in Fig. 3.7. The worst-case loss is 2.66 dB at 40 GHz. The discrepancy between S_{21} and S_{31} might be due to the variation between the designed t_{res} and the achieved NiCr thickness, which might also cause

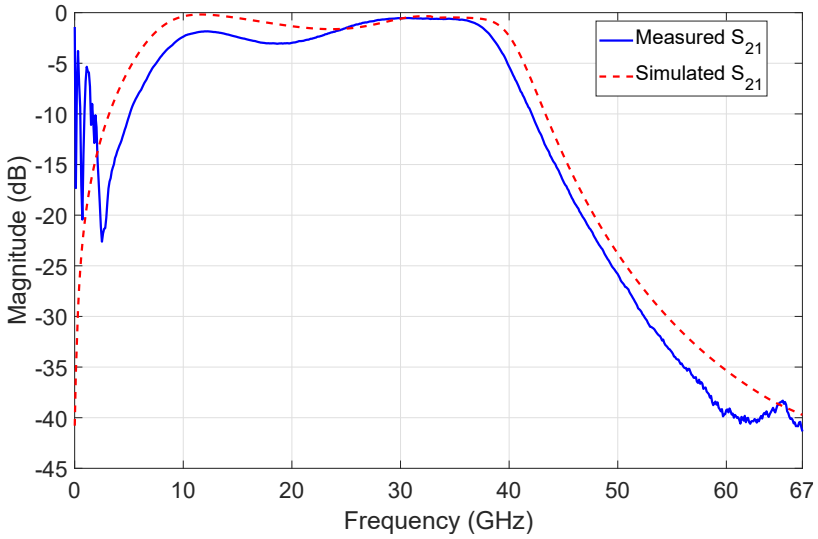


Figure 3.5: Measured and simulated transmission ratio (S_{21}) for the fabricated LPF. ©2020 IEEE.

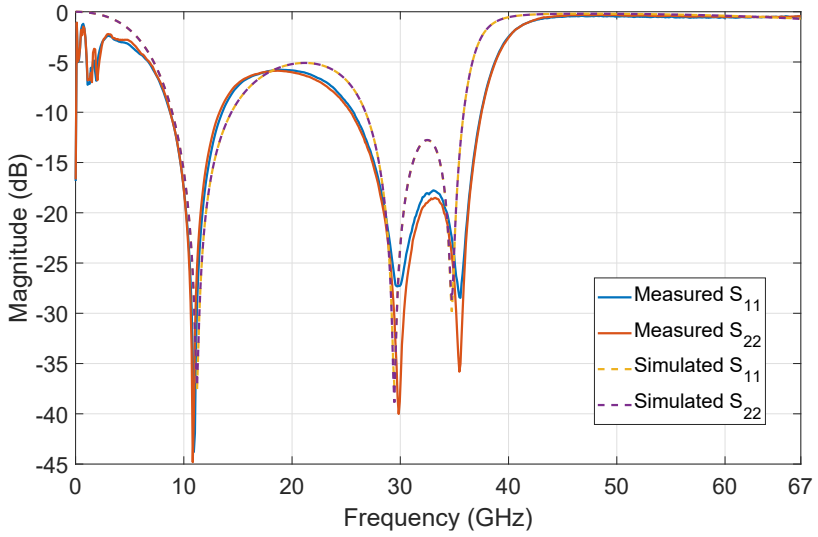


Figure 3.6: Measured and simulated reflection ratios (S_{11} and S_{22}) for the fabricated LPF. From [3] ©2020 IEEE.

Table 3.1: Measured LPF metrics at 10, 20, 30, 40, and 50 GHz

Measured Metric	**10 GHz**	**20 GHz**	**30 GHz**	**40 GHz**	**50 GHz**
S_{21} (dB)	-2.4	-3	-0.5	-5.5	-25.8
S_{11} (dB)	-17.7	-5.8	-30	-2.5	-0.3
S_{22} (dB)	-18	-6	-37.3	-2.6	-0.5

From [3] ©2020 IEEE.

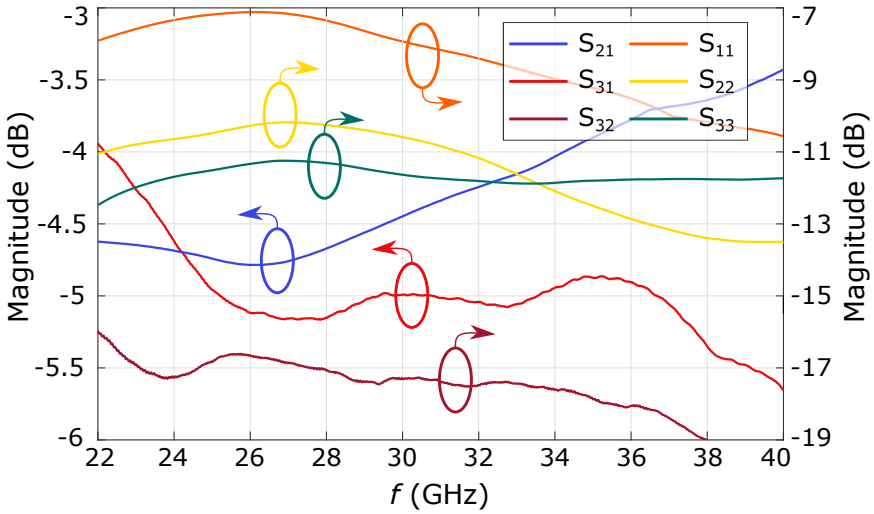


Figure 3.7: Measured S-parameters for the fabricated WPD.

Table 3.2: Measured metrics at 22, 30, and 40 GHz

Measured Metric	**22 GHz**	**30 GHz**	**40 GHz**
S_{21} (dB)	-3.9	-5	-5.7
S_{31} (dB)	-4.6	-4.5	-3.4
S_{11} (dB)	-7.9	-7.9	-10.6
S_{22} (dB)	-11	-10.6	-13.5
S_{33} (dB)	-12.5	-10.6	-11.7
S_{32} (dB)	-16	-17.3	-19.7

the increased reflection at the input port. The two output ports are well isolated, as the WPD demonstrates isolation of more than 16 dB at all frequencies.

3.4 Conclusion

This chapter demonstrates basic RF components fabricated on diamond via AJP at mm-wave frequencies. A LPF was fully printed, while a WPD was fabricated with a combination of thin-film process and AJP. These components perform well at mm-wave and demonstrate fundamental compatibility between AJP and diamond semiconductor platforms. This is important for later chapters of this dissertation, wherein diamond will be integrated into AJP-enabled SiP/SoP strategies.

CHAPTER 4

FULLY ADDITIVELY MANUFACTURED MM-WAVE AND NEAR THZ COMPONENTS

As discussed in Chapter 1, there is a lack of published work in the areas of AM-enabled packaging and interconnects on non-planar surfaces and structures, and at frequencies above the W-band. In recent years, there has been research done on conformal antennas but no demonstration of interconnects on complex structures of significant size or any incorporation of such interconnects in SiP/SoP strategies. In the frequency domain above 110 GHz, interconnects have been realized either via conventional methodologies exclusively or via combination of some AM and conventional methods, but not fully via AM. For SiP/SoP strategies via AJP to be employed for near-THz and THz applications, an initial demonstration of fully printed interconnects at these frequencies is necessary.

Therefore, in this chapter I address the deficiencies mentioned above by showing fully aerosol jet-printed components and interconnects at mm-wave and near-THz frequencies. I first demonstrate compact EBG resonators at mm-wave frequencies up to W-band [5]. These fully aerosol jet-printed resonators are compact and demonstrate the capability to increase functional density by integrating such components as filtering or matching functional blocks in fully aerosol jet-printed electronics and packages. Then, I show fully aerosol jet-printed TLs on non-planar structures of height up to 5 mm, that operate up to 110 GHz [6]. Finally, I demonstrate fully aerosol jet-printed TLs and stubs that operate from 140 to 220 GHz. The work shown in this chapter demonstrates the potential for AJP-enabled SiP/SoP interconnect strategies on non-planar surfaces and at near-THz frequencies, as well as the capability to integrate highly compact filtering and matching structures in such strategies.

4.1 EBG Resonators

The first part of this chapter discusses compact, fully aerosol jet-printed components at mm-

 Section 4.1 is based on "X. Konstantinou, M. T. Craton, J. D. Albrecht and J. Papapolymerou, "Aerosol Jet 3D-Printed Compact EBG Resonators," 2021 IEEE 71st Electronic Components and Technology Con-

wave frequencies, and specifically focuses on aerosol jet-printed EBG resonator structures that can be used as bandstop structures integrated into packages. In recent decades, microwave and mm-wave periodic structures have been of great interest thanks to their filtering capability. These structures are oftentimes called "electromagnetic crystals" or "electromagnetic bandgaps" and have a similar behavior with photonic bandgaps. In effect, they can very readily deter microwave signal propagation at specific frequency bands, featuring high rejection levels [108, 109]. Hence, they have been used extensively in components for surface wave, harmonics, and higher-order mode suppression in microwave circuits [110].

To date, EBG structures have been predominantly fabricated via conventional methodologies, either patterned on metal layers or embedded in semiconductor substrates. These structures have been utilized to realize directive and wearable antennas [111,112], as well as filters [110,113,114]. Despite the wide range of applications for EBG filtering components, there has been a deficiency of use of AM technologies to manufacture them. Since one of the goals of SiP/SoP via AM, and specifically via AJP, is to increase functional density in circuits, it would be beneficial to show that fully printed EBG structures are possible and can be integrated into mm-wave SiP/SoP strategies.

In this section, I demonstrate fully aerosol jet-printed EBG structures at microwave and mm-wave frequencies. I design, fabricate, and measure EBG resonant blocks incorporated into FGC TLs, at three different bands: Ka-, V-, and W-band. PI ink is printed as the dielectric substrate, while Ag ink is printed to realize all conductive patterns. The printed structures are compact, with the printed Ag for the W-band resonator having an area of ~ 0.4 mm^2. This work demonstrates the potential for fully aerosol jet-printed resonant and filtering components integrated into printed packages for applications at mm-wave and beyond.

4.1.1 Design

The designed EBG structures include EBG resonant blocks incorporated into FGC TLs, with the latter enabling probing with ground-signal-ground (GSG) probes. The designed resonant blocks

ference (ECTC), 2021, pp. 2308-2313, doi: 10.1109/ECTC32696.2021.00361", with permission.

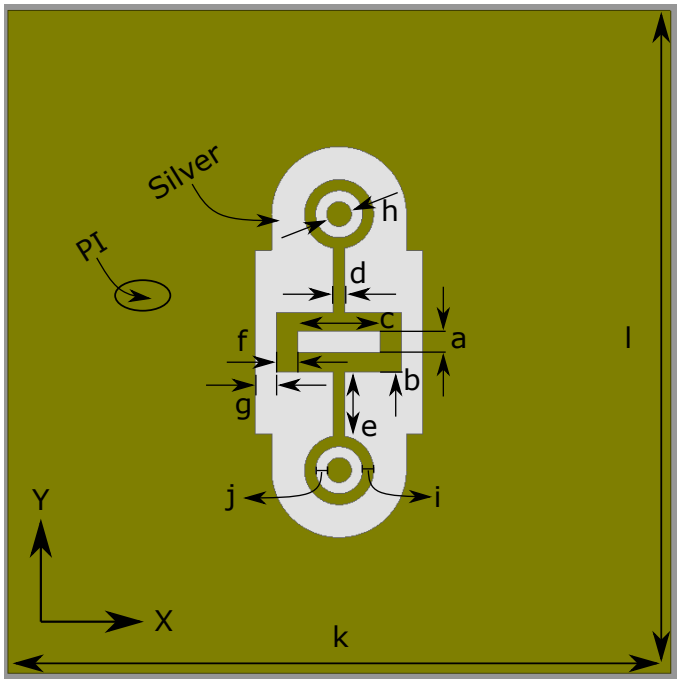


Figure 4.1: Detailed top view of the generic designed resonator in ANSYS HFSS©, featuring the design parameters tabulated in Table 4.1 per resonator type. From [5] ©2021 IEEE.

are "loaded" EBG structures, as defined in [115], each one consisting of two parallel structures of a transverse slot that extends perpendicularly from the FGC line-to-ground gap leading to an aperture, and a ring within the aperture. The latter forms a second aperture and a ring slot, as shown in Fig. 4.1. In this "loaded" resonator configuration, the lumped capacitance and inductance, and hence the resonant frequency, are mainly determined by the slot features, the width of the ring, and the sizes of the two apertures. As discussed in Chapter 2, FGC lines have certain advantages over CPW lines, such as a more compact size and the deterrence of parasitic parallel-plate waveguide modes, and thus I chose them for this application.

I designed three resonators, types A, B, and C, with corresponding resonant frequencies in the Ka-, V-, and W-band, respectively. All design and optimization was done in ANSYS HFSS©. The generic structure design is shown in Fig. 4.1, and design parameters for each resonator type are shown in Table 4.1.

Table 4.1: Design Parameters for the Manufactured Resonator Types A, B, and C

Ref.	Size per resonator type (mm)			Description
	A	B	C	
a	0.077	0.077	0.065	Line width
b	0.07	0.07	0.04	Vertical line-to-ground gap
c	0.3	0.3	0.2	Line length
d	0.04	0.04	0.04	Transverse slot width
e	0.712	0.232	0.072	Transverse slot length
f	0.077	0.077	0.065	Horizontal ground width
g	0.077	0.077	0.065	Horizontal Line-to-ground gap
h	0.09	0.09	0.08	Ring hole diameter
i	0.05	0.04	0.04	Ring slot width
j	0.04	0.04	0.03	Silver ring width
k	3	2	1.5	Total package length
l	3	2	1.5	Total package width

From [5] ©2021 IEEE.

4.1.2 Fabrication

The components were fabricated fully via AJP using an Optomec Aerosol Jet 5X printer [116]. I used PI ink to fabricate the dielectric substrate for the resonators on a 0.5-mm thick 85% Mo 15% Cu alloy carrier, and Ag nanoparticle ink to fabricate the conductive patterns on the PI. During the fabrication, the ambient temperature in the printing chamber ranged from 25 to 27 °C and the relative humidity from 34 to 36 %. The PI ink consisted of PI-2611 (HD Microsystems) diluted to 40 vol.% PI-2611 + N-Methyl-2-Pyrrolidone (NMP) (Sigma Aldrich). Cured PI-2611 has an $\epsilon_r = 2.9$ and a $\tan\delta = 0.002$. The Ag ink consisted of 25 wt.% Clariant Prelect TPS 50 + DI water. Immediately prior to printing PI, I applied the VM651 adhesion promoter (HD Microsystems) to improve adhesion. I first printed 8 layers of PI ink to attain a 10-µm thickness. These layers were then soft baked at 200 °C in N_2 for a 2 min, with a 2 °C maximum temperature gradient and a

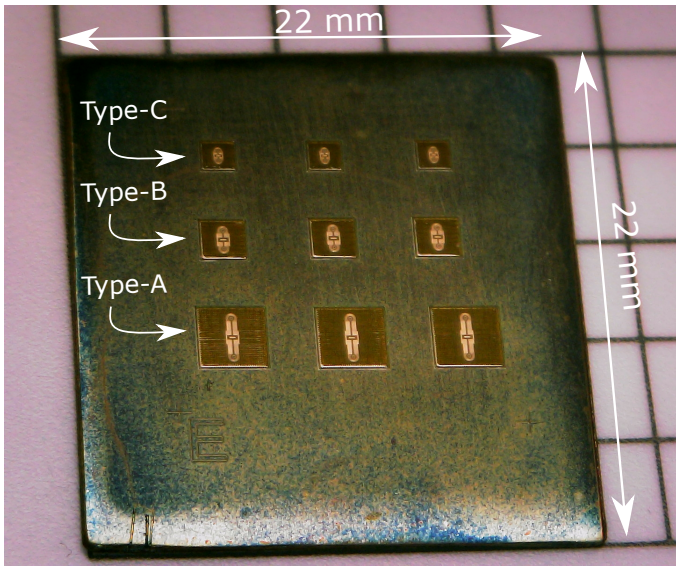


Figure 4.2: Overview of a MoCu carrier with manufactured resonators. From [5] ©2021 IEEE.

rise time of $\sim$ 90 min. I then printed an additional 18 layers of PI to achieve a total target PI thickness of 30 µm post-curing. A final hard bake was done at 295 °C in N_2 for a 30 min, with a 2 °C maximum temperature gradient and a rise time of $\sim$ 138 min. In-between processing steps, all samples were kept under vacuum to deter moisture absorption and mitigate air bubbles trapped in the uncured PI. The final step was to print Ag on the cured PI, followed by a sintering thermal processing in air at 180 °C for 5 h. Detailed steps of the fabrication process for these resonators, including printing parameters, are included in Appendix C. The fabricated resonators on MoCu are shown in Fig. 4.2.

4.1.3 Results

The first set of measurements was in regards with the thickness of the printed materials for the resonators. I took thickness profiles of a type-B resonator using a NanoMap-500LS surface profilometer. The thickness profiles were taken across the paths shown in Fig. 4.3 and are shown in Fig. 4.4. The measured and target thicknesses are shown in Table 4.2. Additionally, a thickness scan of the resonator in 3D is shown in Fig. 4.5. The surface roughness of the PI in paths B-B' and C-C' has a roughness arithmetic mean deviation (Ra) of $\sim$ 10.4 µm.

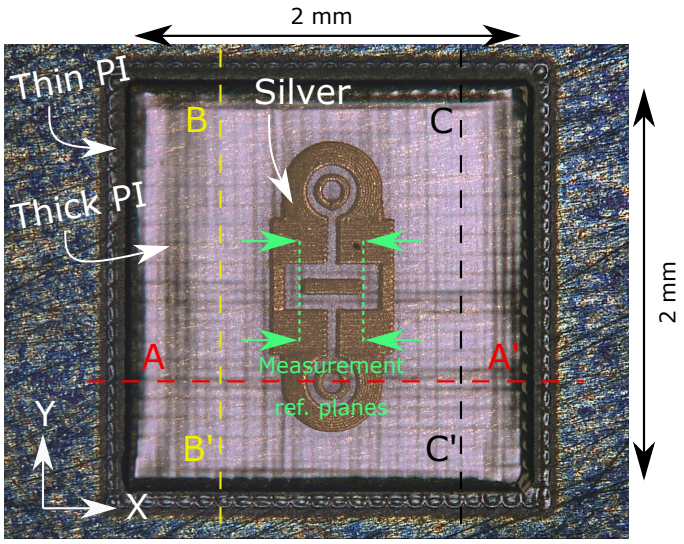
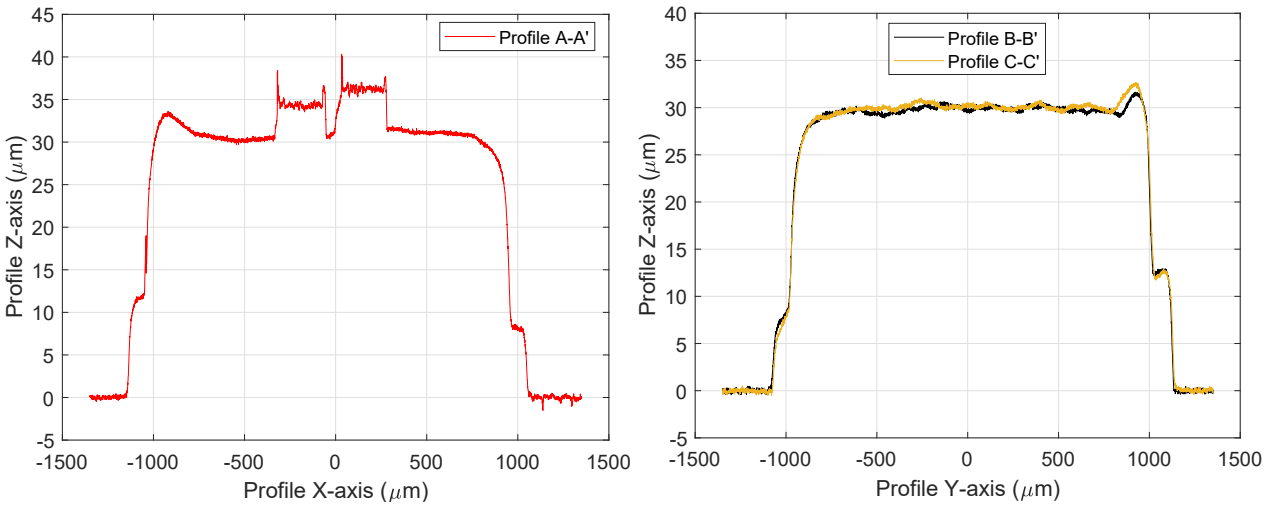


Figure 4.3: Close-up top view of a manufactured type-B resonator, with detailed view of the thickness measurement profile paths. From [5] ©2021 IEEE.



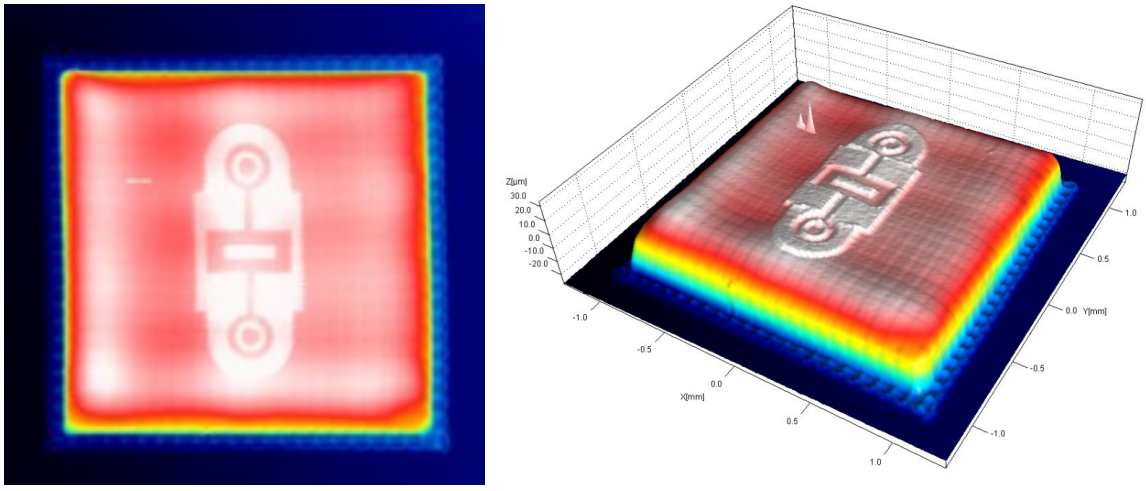
(a) (b)

Figure 4.4: Measured thickness profile of a manufactured type-B resonator along paths featured in Fig. 4.3: (a) path A-A', and (b) paths B-B' and C-C'. From [5] ©2021 IEEE.

Table 4.2: Measured Thickness of Printed Materials

Material	**Target Thickness (μm)**	**Measured Thickness (μm)**
Thin PI	10	8
Thick PI	20	22
Total PI	30	30
Silver	5	4.8

From [5] ©2021 IEEE.



(a) (b)

Figure 4.5: 3D thickness profile of a type-B resonator in (a) top view and (b) in perspective view. From [5] ©2021 IEEE.

I then measured the RF performance of the resonators. I did all the measurements from 50 MHz to 67 GHz using a MPI TS150-THZ Probe System, a Keysight N5227 PNA, and a pair of GGB 67A-GSG-100P picoprobes, and all the measurements from 75 to 110 GHz using VDI WR10-VNAX extension modules and pair of GGB 120-GSG-100-BT picoprobes. In all cases, I did a LRRM calibration using a GGB CS-5 calibration substrate to bring the measurement reference planes to the tips of the probes, as shown in Fig. 4.3. The simulated and measured RF performance of the resonators is shown in Fig. 4.6, with key simulated and measured metrics summarized in

Table 4.3. For all three resonator types, the simulated and measured frequencies correlate well, which is also the case for the insertion and return loss in the pass band. I calculated the unloaded quality factor, Q_{U}, of the resonators as [117]:

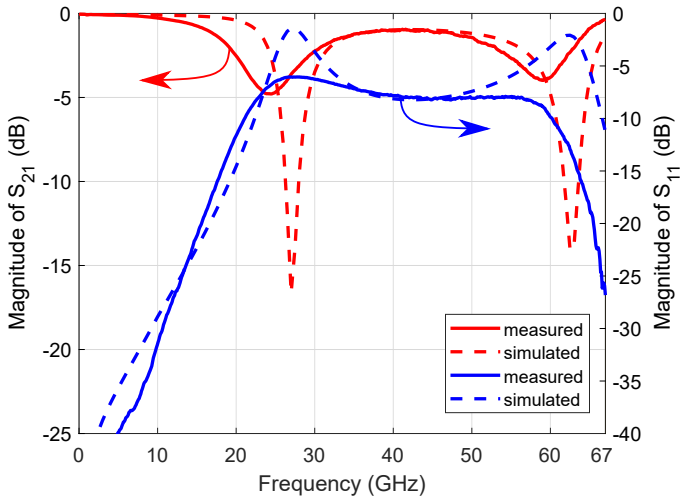
$$Q_{\mathrm{U}} = \frac{Q_{\mathrm{L}}}{1 - 10^{S_{21,\mathrm{res}}/20}}, \tag{4.1}$$

where $S_{21,\mathrm{res}}$ is the S_{21} (in dB) at the resonant frequency, f_{res}, and Q_{L} is the loaded quality factor:

$$Q_{\mathrm{L}} = \frac{f_{\mathrm{res}}}{\Delta f_{3\mathrm{dB}}}, \tag{4.2}$$

where $\Delta f_{3\mathrm{dB}}$ is the 3-dB bandwidth of the resonator. The simulated and measured Q_{U} are close, as shown in Table 4.3.

As can be seen in Fig. 4.6, the depth of the insertion loss resonance is higher in the simulated performance than measured, and the return loss at the resonance is measured lower than simulated. This means that, despite the fact that simulated and measured resonant frequencies and quality factors have adjacent values, the simulated resonators present higher suppression at f_{res}. In general, for resonators used in BSFs, such as in this section and in [117], a deep resonance is desired at f_{res}, which requires a large input impedance, Z_{in}, to be presented by the resonator at that frequency. Since the measured resonance is not as good as simulated, the achieved Z_{in} is not high enough. This is likely due to small differences between designed and realized feature sizes. Moreover, Ag overspray deposited on the resonator slots and apertures can contribute to lower Z_{in}. This can be improved by making modifications of manufacturing steps, such as optimizing the distance of the printing nozzle from the surface of printing, as well as reducing the aerosol flow rates and printing more Ag passes instead. Furthermore, resonators with higher Q_{U} can be designed to compensate for any differences between designed and realized Z_{in}. Nonetheless, the achieved performance of the resonators demonstrates that resonant and filtering blocks can be fully printed and be integrated in SiP/SoP strategies to increase functional density.



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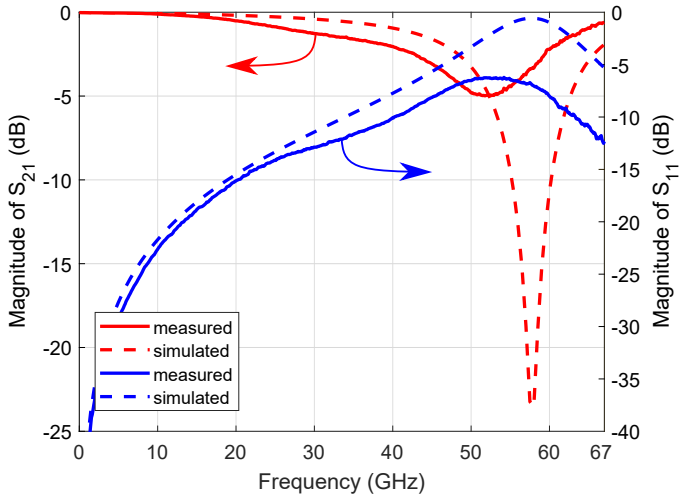

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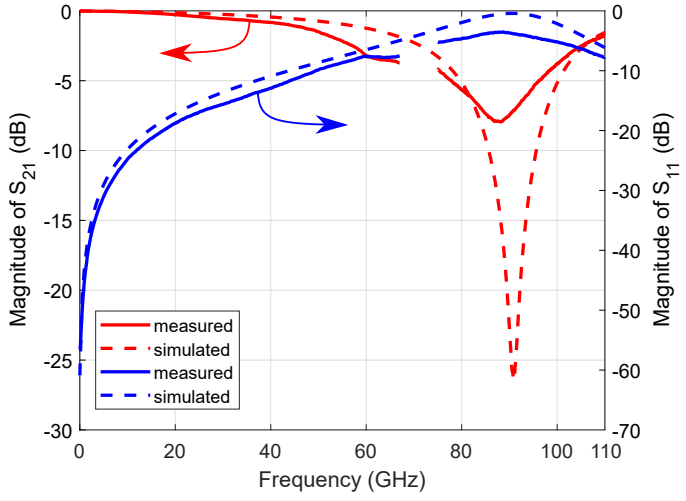


(c)

Figure 4.6: Measured vs. simulated S-parameters of the fabricated resonators (a) type-A, (b) type-B, and (c) type-C. From [5] ©2021 IEEE.

Table 4.3: Simulated vs. Measured Metrics for the Resonator Types A, B, and C

Metric	**Value per resonator type**		
	A	**B**	**C**
Simulated/measured f_{res}	27/24.3 GHz	58/52 GHz	91/87.7 GHz
Simulated/measured insertion loss at f_{res}	16.6/4.8 dB	23.5/5 dB	26.5/8 dB
Simulated/measured return loss at f_{res}	1.4/6.9 dB	0.6/6.3 dB	0.4/3.6 dB
Simulated/measured Q_{u}	5.5/7.63	3.1/8.6	3.2/3.5

From [5] ©2021 IEEE.

4.2 UWB TLs on Non-Planar Structures

The second part of this chapter focuses on the capabilities that AJP technology affords for the fabrication of components and packages on non-planar surfaces and structures. As discussed in Chapter 1, albeit there has been increased interest in conformal antennas in recent years, there has been very limited work in fabricating interconnects and packages on conformal or any non-planar surface.

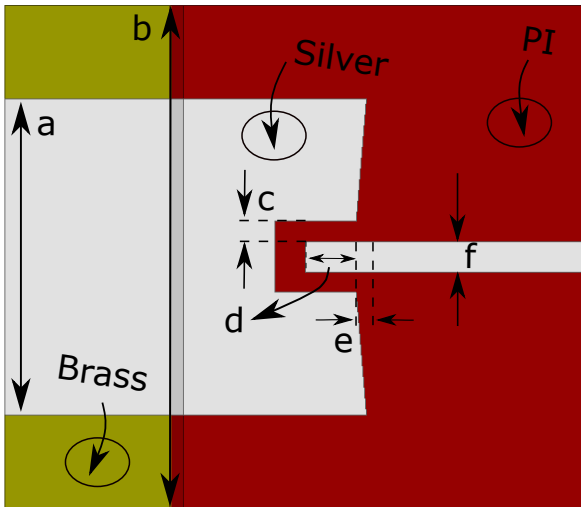
Being able to realize such electronics would benefit multiple contemporary applications. There has been a lot of interest in integrating antennas, sensors, and other electronics on automotive and aircraft parts, which are typically conformal or ramped structures. In the area of wearable electronics, the capability to integrate multi-functional blocks into networked devices on non-planar structures reliably would expand the current state of the art [118–120] and bring significant advances in healthcare and the human–machine interface. In all these application fields, it would be highly desired to develop SiP/SoP strategies that would allow the integration of active dies and

passives into a single package manufactured on a non-planar surface. Increased functional density to reduce the total size of the electronics and design flexibility to tailor each package to a specific non-planar structure and application are essential in these packaging concepts.

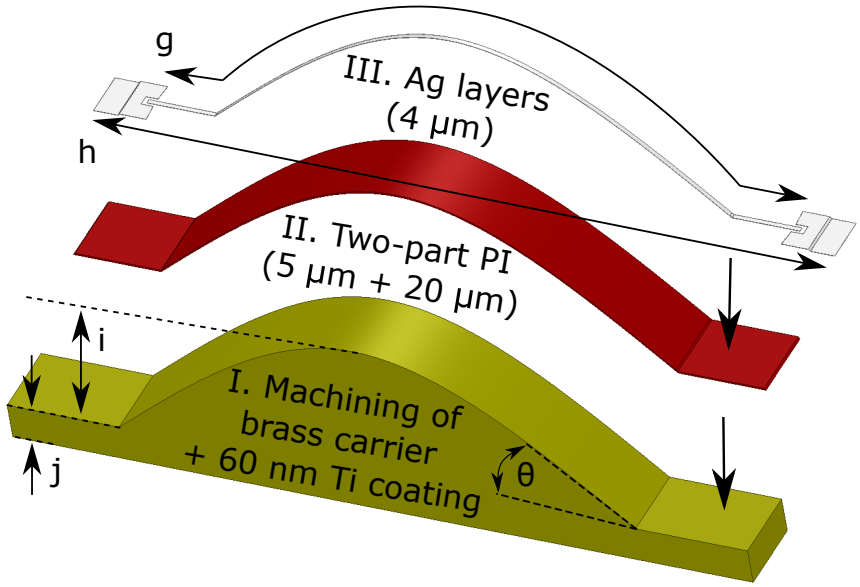
AM manufacturing technologies can be very beneficial in this case, and AJP most of all. While maintaining all the advantages of AM with regards to design flexibility and material availability, AJP is uniquely capable to realize electronics on non-planar structures because it allows for printing from a standoff distance of at least 10 mm away from the substrate without any loss in printing resolution, attaining feature sizes down to at least 10 μm. This attribute can be highly beneficial when printing over non-planar structures of significant size, and is not afforded by other AM methods such as IJP. To date, most of the research on AM technologies has focused on manufacturing on either planar and rectilinear surfaces or on non-planar structures smaller than 1 mm. This chapter expands on the state of the art by demonstrating ultra-wideband (UWB) mm-wave components on larger non-planar structures. For the first time, I demonstrate the realization of UWB mm-wave TLs, fabricated fully via AJP (both dielectric substrates and conductive patterns printed), on conformal and ramped metal structures with non-planar features of different heights ranging up to 5 mm. PI ink was printed to form the dielectric substrate, while Ag nanoparticle ink was printed to form all conductive layers. The RF performance was measured from 50 MHz to 67 GHz and from 75 to 110 GHz. The fabricated parts demonstrate very good results which are relatively insensible to the shape and size of non-planar features, showing that AJP is a potentially very powerful tool in manufacturing electronics on non-planar, complex surfaces and structures for a variety of applications.

4.2.1 Design

The design procedure is as follows. First, I designed two metal carrier types, conformal (curved) and ramped, using brass as the material, in ANSYS HFSS©, with non-planar feature heights of 2 mm and 5 mm. I then designed the PI dielectric substrates and the Ag TLs on the brass carriers. The TLs consist of GCPW launches that transition to MS TLs by means of via-less GCPW-to-



(a)



(b)

Figure 4.7: (a) Top view of the designed TLs, featuring the GCPW TL, the via-less GCPW-to-MS transition, and the MS TL, in ANSYS HFSS©, and (b) exploded view of the TL on a conformal brass carrier, with overview of the basic fabrication steps (I-III). From [6] ©2021 IEEE.

MS transitions. The GCPW launches enable testing using standard GSG probes, and they feature grounding straps to the brass for improved performance near DC. All TLs are designed to have a 50-Ω match. After the basic TL structures were designed, I intergrated longer TLs on the brass carriers and optimized them in ANSYS HFSS©. Key design parameters are shown in Fig. 4.7 and summarized in Table 4.4.

Table 4.4: Design Parameters for Manufactured TLs

Ref.	Size per nonplanar feature type and height				Description
	2-mm curve	**2-mm ramp**	**5-mm curve**	**5-mm ramp**	
a (mm)	0.620	0.620	0.734	0.734	GND width
b (mm)	0.984	0.984	1.2	1.2	PI width
c (mm)	0.040	0.040	0.037	0.037	GCPW-to-GND gap
d (mm)	0.100	0.100	0.100	0.100	GCPW TL length
e (mm)	0.020	0.020	0.020	0.020	GCPW-to-MS transition length
f (mm)	0.060	0.060	0.060	0.060	GCPW and MS TL width
g (mm)	9.97	12.31	13.85	15.61	Total (GCPW + MS) TL length
h (mm)	9.96	12.46	9.93	11.93	Total package lateral length
i (mm)	2	2	5	5	Nonplanar feature height
j (mm)	1.5	1.5	1.5	1.5	Carrier base thickness
θ (deg.)	40	30	65	60	Curve/ramp tangential angle

From [6] ©2021 IEEE.

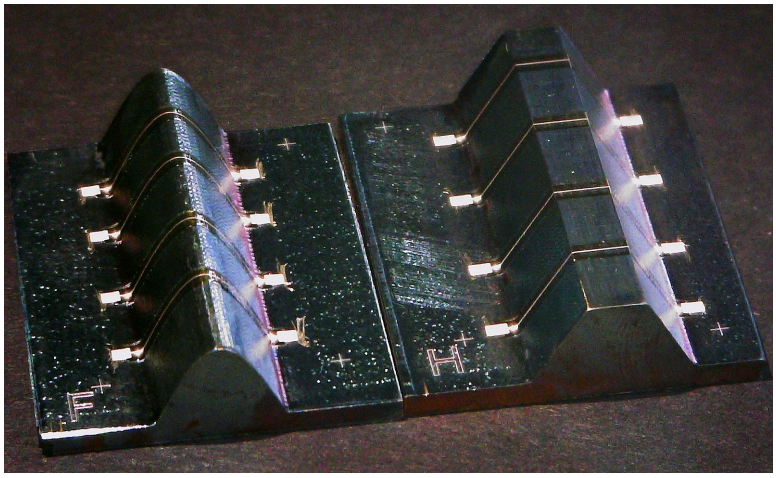
4.2.2 Fabrication

The basic steps of the fabrication procedure are shown in Fig. 4.7b. The first step was to form the desired brass carrier shapes. Bulk rectangular brass parts were cut down to a desired thickness, and then conformal and ramped features were CNC-machined on the brass utilizing the 3D profiles I created in ANSYS HFSS©. The brass part cutting and CNC machining was done by Brian Wright at MSU. I then mechanically polished the parts. A 60-nm titanium (Ti) coating was then sputtered on the brass surface (by Brian Wright) to act as an adhesion layer for the PI and deter brass oxidation during the subsequent fabrication steps.

The PI ink printed to form the dielectric layers was composed of PI-611 (HD Microsystems) diluted to 40 vol.% PI-2611 + NMP (Sigma Aldrich). The Ag ink consisted of 25 wt.% Clariant Prelect TPS 50 + DI water. All inks were printed using an Optomec Aerosol Jet 5x printer [116] from a standoff distance of 8 mm from the top surface of the carrier base, which was the lowest printing point. Immediately before printing PI, I applied the VM651 adhesion promoter (HD Microsystems) to improve the adhesion of the PI to the Ti/brass surface. First, I printed 4 layers of PI ink to get a 5-μm thickness. These layers were then soft baked at 200 °C in N_2 for a 2 min. I then printed an additional 18 layers of PI to get a total target PI thickness of 25 μm post-curing. A final hard bake was done at 295 °C in N_2 for a 45 min to fully imidize the printed PI. The final step was to print the Ag TLs on the cured PI, which were then sintered in air at 180 °C for a 5 h. Details of the manufacturing process are included in Appendix C. The final parts are shown in Fig. 4.8.

4.2.3 Results

I first took measurements of the surface profile of the fabricated TLs using a NanoMap-500LS surface profilometer. The printed thin PI with a target thickness of 5 μm was measured to be 4.5-μm-thick, while the thick PI with a target thickness of 20 μm was measured to be 18.5-μm-thick, giving a total PI thickness of 23 μm. The printed Ag with a target thickness of 4 μm was measured to be 4.2-μm-thick. I also took roughness profiles of the Ti/brass surface in two different areas on conformal and ramped carriers, away and near the curve/ramp edge, as shown



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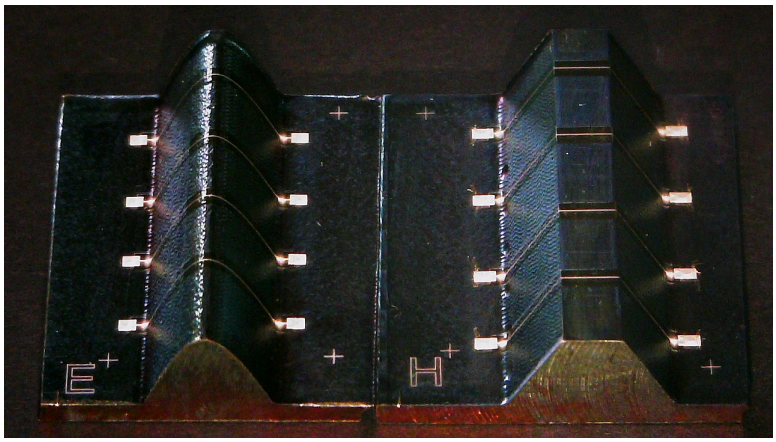


(b)

Figure 4.8: Perspectives of fabricated TLs on conformal (left) and ramped (right) brass carriers with 5-mm high nonplanar features. From [6] ©2021 IEEE.

in Fig. 4.9 (profiles #1 and #2, respectively). I took multiple measurements of the same profiles in different areas of both conformal and ramped carriers and then averaged the results. The Ti/brass surface away from the curve/ramp edge was found to have an average roughness arithmetic mean deviation (Ra) of 0.20 μm with a peak-to-peak surface variation of 1.6 μm, while the surface near the curve/ramp edge had a roughness Ra of 0.95 μm with a peak-to-peak surface variation of 5.5 μm, demonstrating a higher surface roughness near and on carrier edges, as expected. This increased surface roughness in certain areas of the brass parts can contribute to increased losses comparing to the simulation, especially in the W-band.

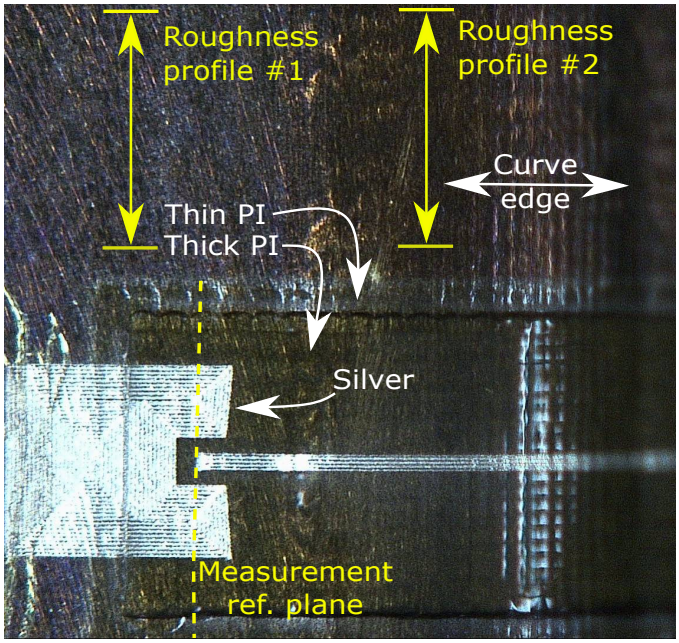
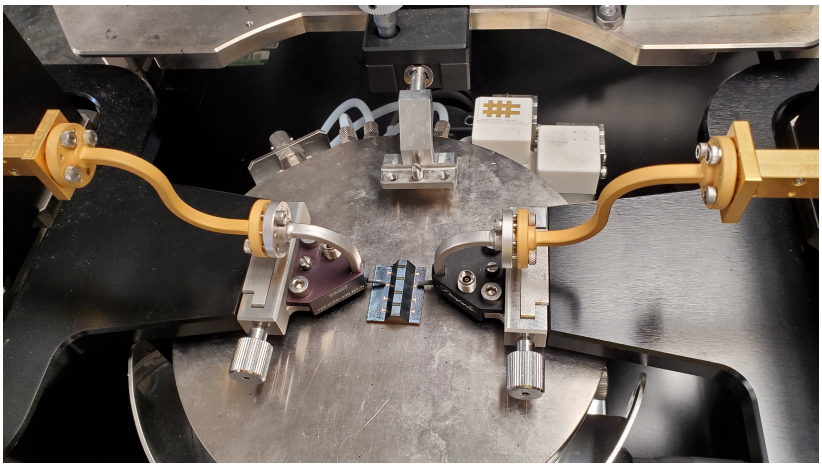
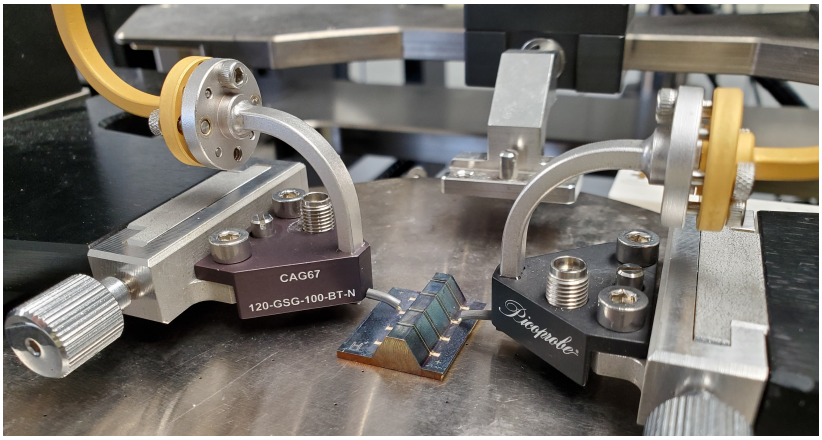


Figure 4.9: Detailed view of the roughness profile measurement areas near the curve edge on a conformal carrier. From [6] ©2021 IEEE.

I then measured the RF performance of the TLs from 50 MHz to 67 GHz using a MPI TS150-THZ Probe System, a Keysight N5227 PNA, and a pair of GGB 67A-GSG-100P picoprobes, and from 75 to 110 GHz utilizing VDI WR10-VNAX extension modules and using a pair of GGB 120-GSG-100-BT picoprobes. The measurement setup for W-band is shown in Fig. 4.10. In all cases, I performed LRRM calibration using a GGB CS-5 calibration substrate to bring the measurement reference planes to tips of the probes, as shown in Fig. 4.9. The simulated and measured small-signal RF performance for the TLs on 2- and 5-mm high conformal carriers is shown in Fig. 4.11, and for ramped carriers in Fig. 4.12. For each carrier type, the insertion and return loss for the two different heights are very close. The insertion loss is kept below 1 dB/mm up to 110 GHz and S_{11} below -10 dB at most frequencies. All TLs were printed from the same standoff distance of 8 mm, thus the fabrication process is demonstrated to be extendable from planar surfaces to non-planar features up to at least 5 mm without any loss in printing resolution, as the parts RF performance is only minimally affected by the change in non-planar feature size. Printing on larger features can be achieved by printing from a larger standoff distance while simultaneously adjusting the printer flow rates detailed in Appendix C to focus the aerosol stream to the lowest printing point.



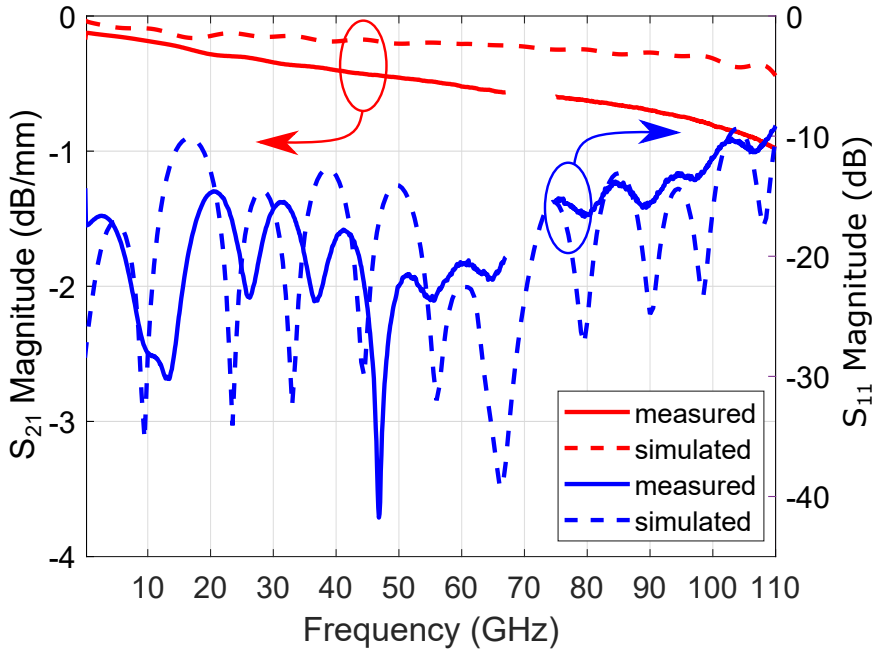
(a)



(b)

Figure 4.10: Measurement setup for W-band: (a) top view, and (b) side view.

The achieved line loss (in dB/mm) is compared to that of other additively manufactured components in Table 4.5. The parts realized in this work perform similarly or better than other state-of-the-art additively manufactured components on either planar surfaces or non-planar features of much smaller size. Additionally, the parts shown here achieve the widest operational frequency range of all from near-DC up to 110 GHz, only shown in [121]. These parts are, to the best of my knowledge, the only example of UWB mm-wave components manufactured fully additively on non-planar structures with features larger than 1 mm, and demonstrate for the first time a printing technology extendable to accommodate non-planar features of size up to at least 5 mm.



(a)

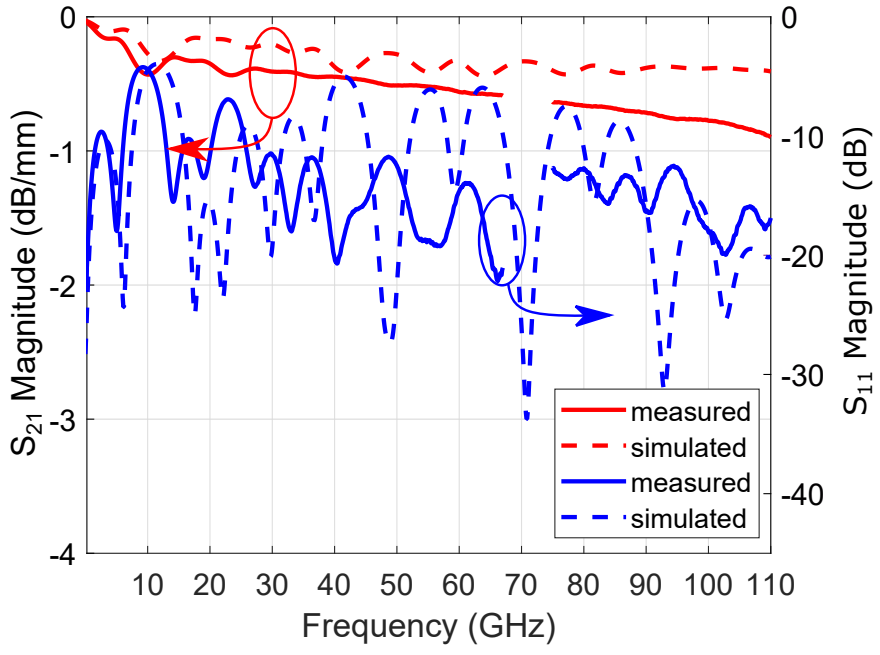


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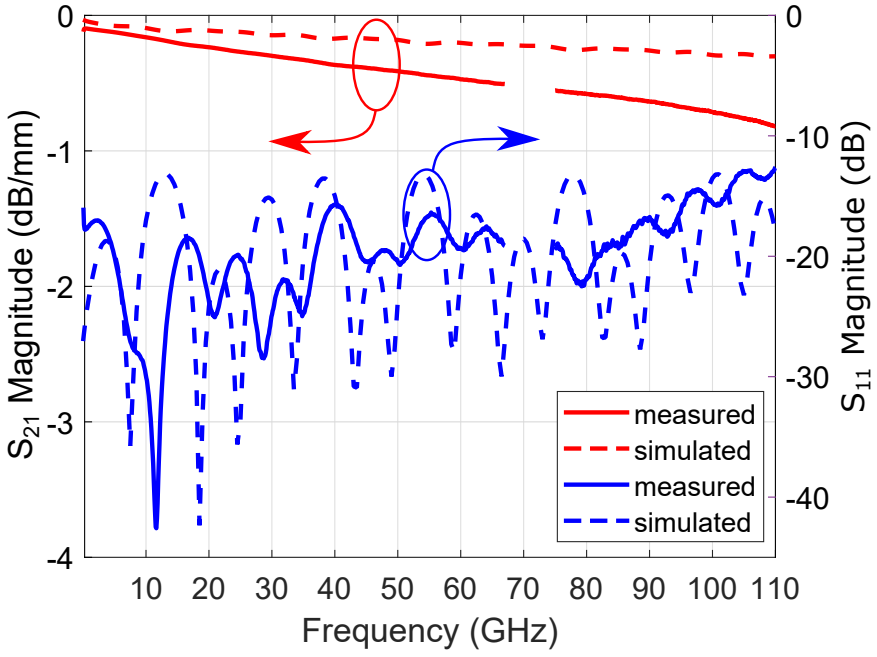
Figure 4.11: Measured vs. simulated S-parameters of the fabricated TLs on the conformal carriers: (a) 2-mm and (b) 5-mm features. From [6] ©2021 IEEE.



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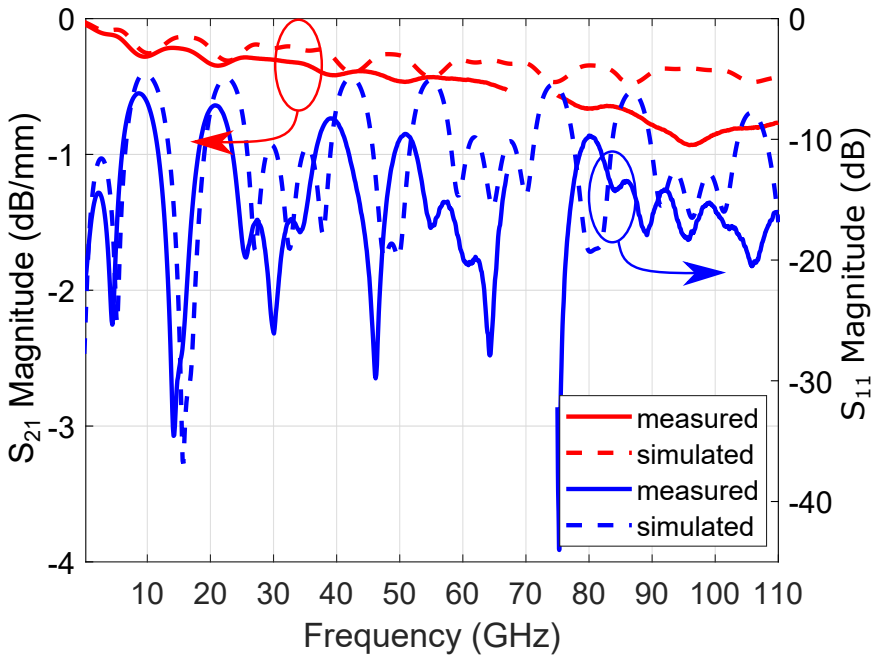


(b)

Figure 4.12: Measured vs. simulated S-parameters of the fabricated TLs on the ramped carriers: (a) 2-mm and (b) 5-mm features. From [6] ©2021 IEEE.

Table 4.5: Comparison with state-of-the-art AM components

Ref.	Fabrication Process	Application	Non-Planar Structure	Line Loss (dB/mm)
This work	**AJP**	**UWB interconnects on non-planar structures**	**Yes**[†]	**0.26 (20 GHz),**[*] **0.49 (60 GHz),**[*] **0.67 (90 GHz)**[*]
			Yes[#]	**0.34 (20 GHz),**[*] **0.51 (60 GHz),**[*] **0.75 (90 GHz)**[*]
Delage *et al.* [122]	AJP on ceramic	TLs on ceramic substrates	Yes[‡]	0.17 (20 GHz),[**] 0.4 (60 GHz)[**]
Hester *et al.* [123]	AJP, SLA	Filter on multi-curve substrate	Yes[§]	N/A (stopband 6-14 GHz)
Qayyum *et al.* [121]	AJP on Verowhite/LCP	UWB interconnects	Yes[¶]	0.49 (110 GHz)
Ihle *et al.* [68]	AJP on LTCC	Interconnects on GaAs[††]	No	0.64 (90 GHz),[**] 0.8 (140 GHz)
Tehrani *et al.* [65]	IJP	Interconnects on GaAs[‡‡]	No	0.45 (24.5 GHz)
		Interconnects on GaAs[§§]	No	0.57 (24.5 GHz)

[*] Avg. loss of conformal and ramped cases; [**] approximated for comparison;
[†] 2-mm and [#] 5-mm high conformal and ramped features;
[‡] 500-µm high 3D-printed ceramic ridge; [§] 2.6-mm high 3D-printed "roller-coaster" features;
[¶] 200-µm high 3D-printed Verowhite trapezoid; [††] GaAs CPW die; [‡‡] GaAs 0-dB attenuator die;
[§§] GaAs LNA die.
From [6] ©2021 IEEE.

4.3 Components at 140-220 GHz

The final section of this chapter focuses on fully aerosol jet-printed components at near-THz frequencies. As discussed at the beginning of the chapter, additive manufacturing for electronics above the W-band has had only limited growth. There is enormous interest for electronic components and packages at near-THz and THz, mainly because there are large bandwidths available at those frequencies, but also due to the demand for higher sensing precision. Nevertheless, design becomes increasingly difficult as frequencies increase beyond the W-band, as wavelength become very small and the performance issues introduced by chip-and-wire and flip-chip interconnects worsen. Therefore, the design flexibility afforded by SiP/SoP strategies fully via AM, and specifically via AJP, can assist in such design efforts.

To the best of my knowledge, there have been no reports of fully aerosol jet-printed components above the W-band. To date, at these frequencies, AJP has only been employed alongside conventional methods and exclusively to deposit metal layers on pre-manufactured dielectric or LTCC substrates. Cai *et al.* [124] showed the first D-band TLs by printing Ag on LCP. Ihle *et al.* printed Ag TLs on LTCC up to 320 GHz in [125] and D-band Ag interconnects on a GaAs die on LTCC while dielectric ramps where formed via MD in [68]. I conclude this chapter by showing the first fully aerosol jet-printed passives above 110 GHz. I use AJP to print both dielectrics and metals in order to realize MS TLs and radial stubs at 140-220 GHz that utilize GCPW launches and vialess GCPW-to-MS transitions. The results demonstrated here show the potential of AJP as a tool for developing SiP/SoP strategies for highly integrated electronics at near-THz and beyond.

4.3.1 Design

The designed components are divided into two sets, namely Zones 1 and 2, with two different dielectric substrate thicknesses. PI was used as the material to design the dielectric substrates and Ag to design all conductive layers, while MoCu is used for the bottom ground plane. The components are TLs and radial stubs and were designed along with respective thru-reflect-load

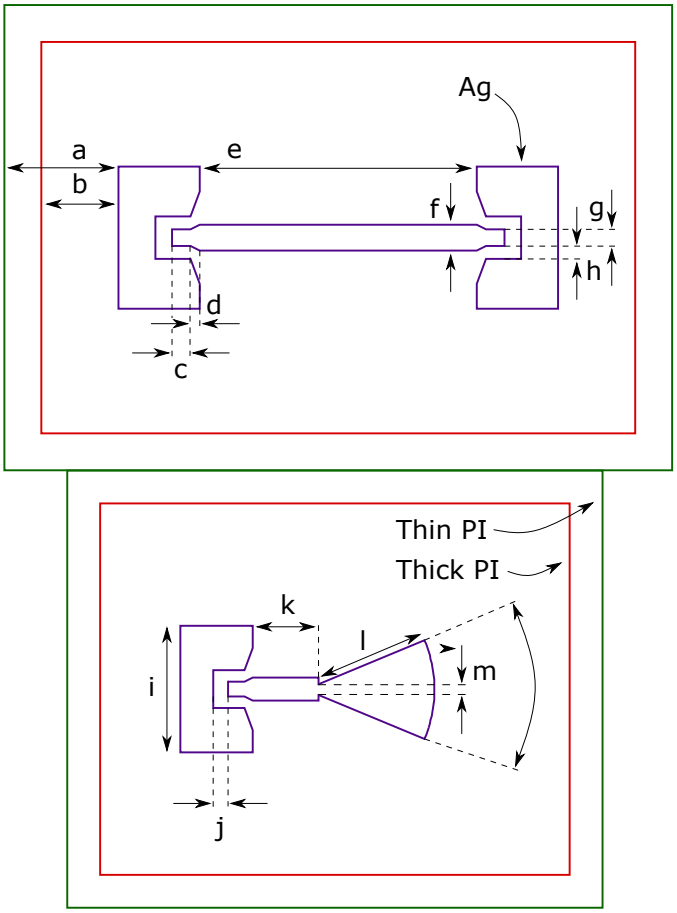


Figure 4.13: Top view of the designed components, with annotated dimensions: TL (top), and radial stub (bottom), with bottom ground everywhere.

(TRL) calibration standards for each zone. I designed both TLs and stubs by starting with the GCPW launches and then incorporating the MS TLs and the via-less GCPW-to-MS transitions. For the radial stubs, the stub opening is at the end of a MS TL. All TLs were designed to have a 50-Ω match. The components were simulated in ANSYS HFSS©, and important design parameters are defined in Fig. 4.13 and summarized in Table 4.6. All designs and simulations were verified with assistance from Xing Lan at Space Systems, Northrop Grumman Corporation. The TRL calibration standards specifically were designed by Xing Lan.

Table 4.6: Design Parameters for Components at 140-220 GHz

Ref.	Size per feature		Description
	Zone 1	Zone 2	
a (mm)	0.309	0.309	GND-thin PI edge distance
b (mm)	0.163	0.163	GND-thick PI edge distance
c (mm)	0.050	0.050	GCPW TL length
d (mm)	0.025	0.025	GCPW-to-MS transition length
e (mm)	0.750	0.750	MS TL length
f (mm)	0.040	0.070	MS TL width
g (mm)	0.040	0.045	GCPW TL length
h (mm)	0.035	0.035	GCPW TL gap
i (mm)	0.385	0.385	GND width
j (mm)	0.045	0.045	Backside GCPW TL gap
k (mm)	0.200	0.200	Radial stub MS TL length
l (mm)	0.345	0.353	Radial stub length
m (mm)	0.033	0.033	Radial stub input width
θ (deg.)	45	45	Angle subtended by stub

4.3.2 Fabrication

The first step of the fabrication process was to prepare a MoCu (85% Mo 15% Cu) carrier plate via mechanical polishing to act as the bottom ground plane. Before printing PI and to improve the adhesion of printed PI with the MoCu surface, I applied the VM651 adhesion promoter (HD Microsystems). I then printed some initial PI layers (thin PI) to get a target thickness of 5 μm. These first layers served as an adhesion layer, which was crucial to avoid delamination of the PI from the MoCu surface. I did a soft bake for these PI layers at 200 °C in N_2 for 2 min. Then, I printed additional 20 μm of PI (thick PI) for a total thickness of 25 μm for the components in Zone 1, and another 10 μm of PI for the components in Zone 2 for a total thickness of 35 μm. I then did a hard bake at 295 °C in N_2 for 1 h to fully imidize all the printed PI layers. I finally printed 3 μm of Ag, followed by a sintering thermal process at 180 °C in atmosphere for 5 h.

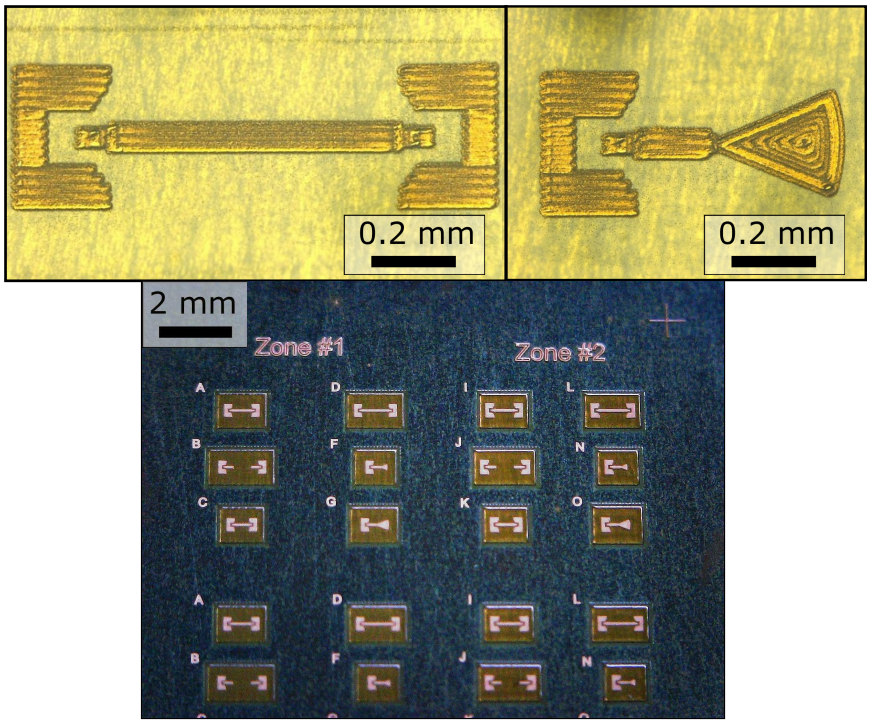


Figure 4.14: Pictures of fabricated components on a MoCu carrier: a TL (top left) and a radial stub (top right) in Zone 2, and overview of fabricated components and calibration structures (bottom).

For all thermal processing profiles I maintained a temperature gradient of less than 2 °C/min, and in-between printing and thermal processing all samples were kept under vacuum to mitigate air bubbles trapped in uncured PI and deter moisture absorption by printed PI and oxidation of printed Ag. Details of the manufacturing steps are included in Appendix C.

As all aerosol jet-printed components demonstrated in this chapter, the components shown here were fully fabricated using an Optomec Aerosol Jet 5X Printer [116]. The PI ink was composed of PI-2611 (HD Microsystems) diluted to 40 vol.% PI-2611 + NMP (Sigma Aldrich). The Ag ink was composed of 25 wt.% Clariant Prelect TPS 50 + DI water and was mixed under ultrasonication for 30 min prior to printing. The MoCu carriers were placed on a heated stage while printing so that the printed materials dry soon after deposition. The stage temperature was kept low enough so that the inks do not begin to cure or sinter. The fully manufactured components are shown in Fig. 4.14.

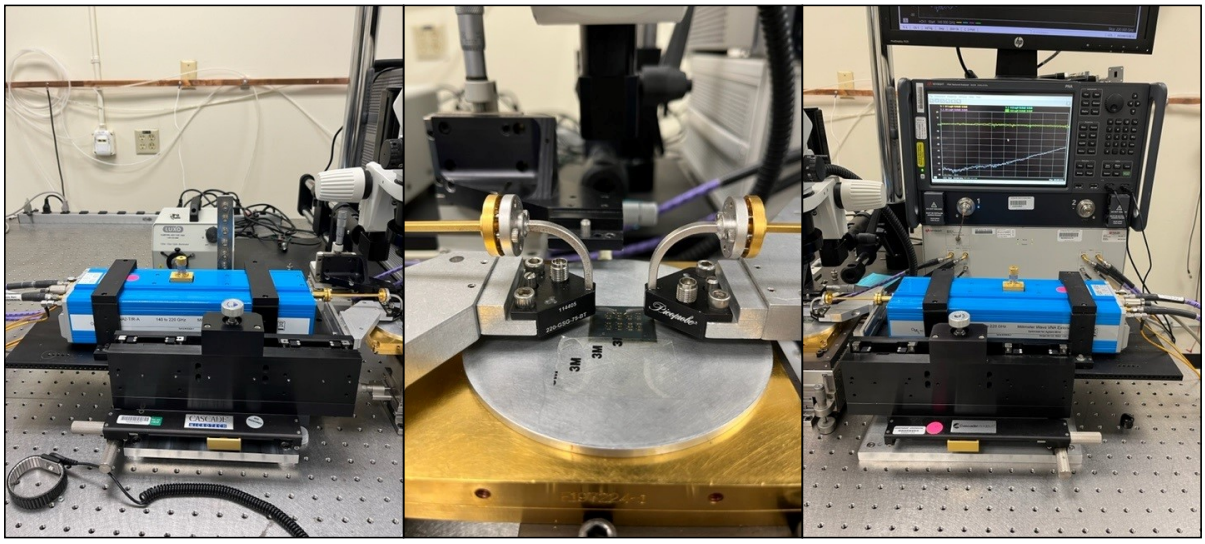
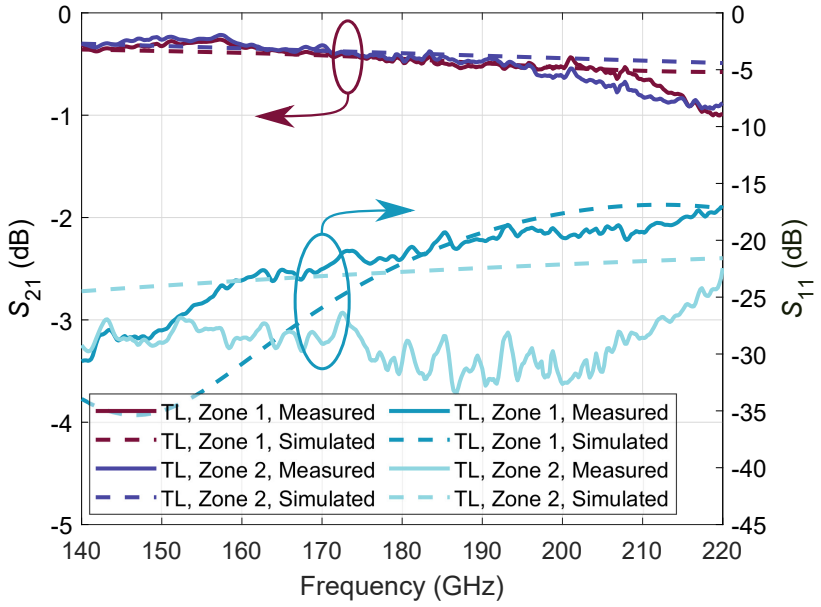


Figure 4.15: Overview of the measurement setup at Space Systems, Northrop Grumman Corporation: PNA and 140-220 GHz extenders (left and right), and a carrier with fabricated components under test using GSG probes (middle). Used with permission.

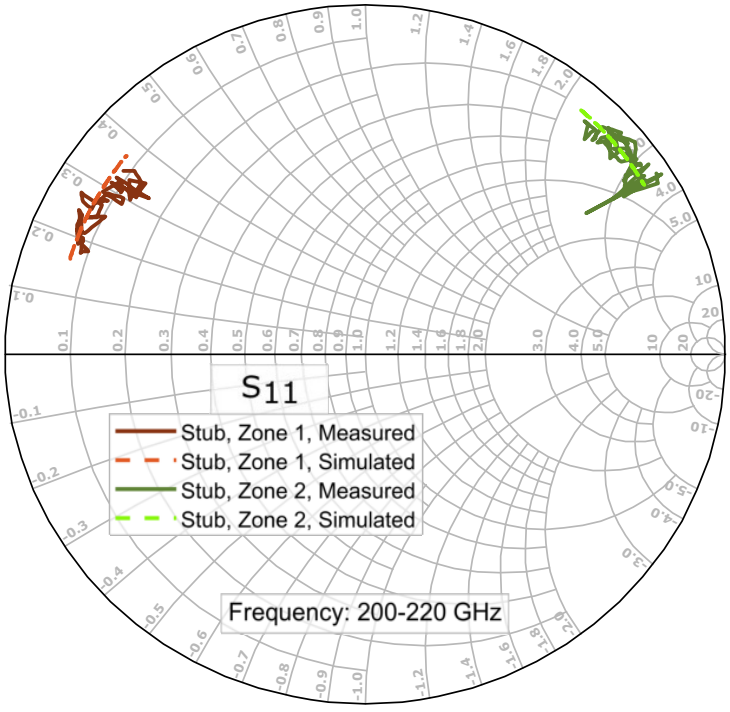
4.3.3 Results

I first took profile measurements for the fabricated components with a NanoMap-500LS surface profilometer. The total PI in Zone 1 with a target thickness of 25 µm was measured at 23 µm, while in Zone 2 a target thickness of 35 µm was measured at 32 µm. The Ag thickness with a target of 3 µm was measured at be 2.7 µm. Before printing Ag, I measured the actual PI thicknesses and adapted the designs in ANSYS HFSS© accordingly.

All RF measurements were performed by Khanh Nguyen and Alfonso Escorcia at Space Systems, Northrop Grumman Corporation using a Keysight PNA N5227B, OML V05VNA2 mm-wave frequency extenders, and 220-GSG-75-BT waveguide picoprobes with a 75-µm pitch by GGB Industries Inc. The measurement setup is shown in Fig. 4.15. A set of TRL calibration standards were fabricated alongsidethe TL and stub structures on MoCu carriers, which covered a 8:1 bandwidth ratio that fully accommodated the frequency range of interest. Post-calibration, the reference planes were at the ends of the reflect standards, thus $(c + d + k)$ away from the GCPW TL edge as defined in Fig. 4.13. Sonnet® was used to derive the calibration coefficients. The TLs were measured from 140 to 220 GHz and performed well, with the measured results correlating well



(a)



(b)

Figure 4.16: Measured and simulated S-parameters of the fabricated components after TRL calibration: (a) TLs and (b) radial stubs.

Table 4.7: Comparison with State-of-the-Art mm-Wave and Near-THz Components

Ref.	Process	Application	Line Loss (dB/mm)
This work	**AJP**	**TLs at 140-220 GHz**	**0.86 (140 GHz)**[*†] **0.98 (170 GHz)**[*†] **1.64 (200 GHz)**[*†]
Khan *et al.* [126]	Conventional on LCP	D-band TLs	0.18 (110 GHz)[*], 0.33 (170 GHz)[*]
Gramlich *et al.* [127]	AJP on PI	D-band TLs	0.12 (110 GHz)[*], 0.36 (170 GHz)[*]
Cai *et al.* [124]	AJP on LCP	D-band TLs	0.35 (110 GHz)[*], 0.51 (170 GHz)[*]
Ihle *et al.* [125]	AJP on LTCC	TLs up to 320 GHz	0.8 (280 GHz)
Ihle *et al.* [68]	AJP on LTCC	Interconnects on GaAs	0.64 (90 GHz)[#], 0.8 (140 GHz)
Qayyum *et al.* [121]	AJP on Verowhite/LCP	UWB TLs	0.49 (110 GHz)
Piekarz *et al.* [53]	AJP	W-band TLs	0.47 (90 GHz)[*#], >1.6 (110 GHz)[*]

[*] Loss of GCPW TLs + GCPW-to-MS transition has been removed; [†] average of TLs in Zones 1 and 2; [#] approximated for comparison; [§] avg. loss of conformal and ramped cases.

with simulated, as shown in Fig. 4.16a. The average line loss of Zones 1 and 2 varies from 0.86 to 2.6 dB/mm. The radial stubs, measured from 200 to 220 GHz, also performed well and close to the simulations, as shown in Fig. 4.16b.

The components demonstrated here are, to the best of my knowledge, the only example of fully aerosol jet-printed components above 110 GHz. The only other component realized entirely via AJP at an adjacent frequency band was demonstrated in by Piekarz *et al.* in [53], with a demonstrated loss above 1.6 dB/mm at 110 GHz. The TLs I demonstrated maintain an average loss of less than that up to at least 200 GHz. As shown in Table 4.7, TLs demonstrated in [124, 126, 127] yield lower loss, but these examples employed hybrid approaches with printed Ag on pre-manufactured

substrates and are not able to accommodate SiP/SoP strategies for system integration via AJP. Furthermore, the loss shown here can be reduced by curing dielectrics at higher temperatures, as well as by using Ag inks with conductivity closer to the one for bulk Ag.

4.4 Conclusion

This chapter addresses some of the deficiencies in the current state of the art in additively manufactured components and interconnects at mm-wave frequencies and beyond. Specifically, I focused on the need for compact filtering functional blocks that can be integrated into fully printed packages, the lack of fully printed components and packages on non-planar surfaces, as well as the lack of fully printed components operating above the W-band. These deficiencies were addressed by demonstrating certain components manufactured fully via AJP. I first demonstrated compact EBG resonator structures in various mm-wave bands that can be used in BFSs in SiP/SoP strategies. I then demonstrated the first attempt for fully printed interconnects on complex and ramped structures with sizes above 1 mm, operating up to W-band. Finally, I showed the first fully aerosol jet-printed components above the W-band, at 140-220 GHz.

CHAPTER 5

AJP-ENABLED CHIP-FIRST PACKAGING

In chapter 4, I addressed some of the deficiencies in additive manufacturing for RF interconnects and packages, and specifically in the areas of interconnects on non-planar surfaces and at near-THz, by demonstrating fully aerosol jet-printed passives, which showed the potential for SiP/SoP concepts in such scenarios via AJP. In this chapter, I focus directly on the development of AJP-enabled SiP/SoP strategies and their applications. As discussed in Chapter 1, AJP-enabled strategies came to address bottlenecks in conventional methodologies as well as in other AM technologies for interconnects and packaging.

Albeit the strategies via AJP demonstrated in the literature brought about significant advancements in performance, design flexibility, and functional density, they did not address certain challenges and areas, such as accommodating the use of a variety of dielectric materials or packaging of high-power dies. In this chapter, I demonstrate SiP/SoP strategies that address such deficiencies. I first show the development of basic strategies for packaging at mm-wave, realized fully with the use of AJP, that can be a reliable alternative to other AJP-enabled strategies demonstrated in the literature [7]. I then utilize one of those strategies to realize a SoA transmitter module, printing the entire package on an antenna operating in the Ku-band, showing that this strategy can be used for system integration. The work in this chapter will be extended in Chapter 6, in which the SiP/-SoP strategy used for the SoA will be improved, will incorporate a diamond platform, and will additionally demonstrate high-power RF performance.

5.1 Chip-First Packaging Strategy

The first part of this chapter focuses on the development of SiP/SoP strategies via AJP for system integration at mm-wave frequencies. As discussed in Chapter 1, conventional SiP/SoP strategies

predominantly utilize chip-and-wire interconnect techniques, either with wire or ribbon bonds [29], or, more recently, flip-chip interconnects [44]. All these approaches come with disadvantages that can introduce performance bottlenecks, especially at mm-wave frequencies, such as impedance discontinuities at the RF path over the bond wires/ribbons, or the risk of detuning and parasitic coupling in the case of flip-chip. Furthermore, none of these methodologies allows for the design and material flexibility afforded by approaches via AM.

AM technologies have been proven as a viable alternative to conventional SiP/SoP strategies, with the potential to replace them entirely. Amongst AM techniques, AJP has been proven uniquely capable of providing SiP/SoP solutions compatible with heterogeneous integration and with performance at mm-wave and beyond. Unlike other AM methods such as IJP, AJP allows for material deposition from a standoff distance up to 10 mm away from the substrate without resolution loss. This enables printing on multi-level structures and non-planar structures, as well as the manufacturing of complex packages with multiple layers of different dielectric and conductive materials in a very small area. These capabilities can be used to print packages on non-planar surfaces and packages with multi-die stacks, which would be challenging with other AM methods.

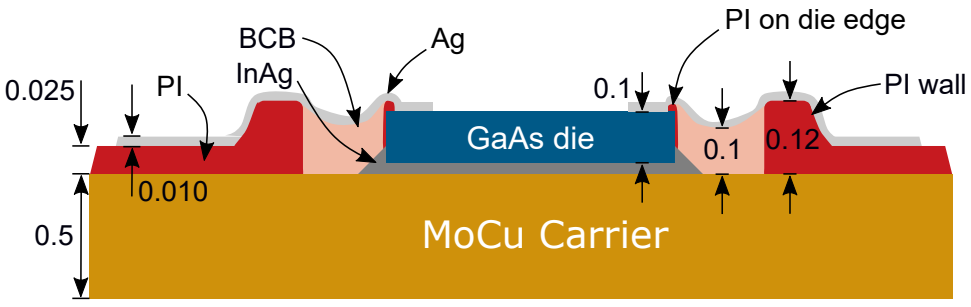
There has been demonstration of plenty of SiP/SoP strategies via IJP and with combination of conventional techniques with AM, including with AJP. IJP has been used in [63, 65]. A combination of FDM, MD, and LMM was used in [67]. Combinations of AJP with conventional methods were used in [68–71]. However, all these approaches employ either multiple methods or pre-manufactured substrates with printing to realize the package. The SiP/SoP chip-first strategy demonstrated in [64,66,72,74,75], in contrast, employed only AJP to manufacture the entire package around the die, as well as capacitors and antennas in-package. There are certain challenges, though, that this strategy left unaddressed. The challenge addressed in this section has to do with adhesion issues at the die-dielectric interface. PI ink alone was used to fabricate the dielectric substrate for the packages. PI is prone to delamination from the the die at elevated temperatures during thermal curing, as discussed in [128], which is a significant reliability issue. A dielectric delamination requires re-work by means of additional PI deposition to fix the die-dielectric inter-

face prior to printing metal interconnects. Even if re-printing fully covers the sides of the die, the interconnects in those areas can be prone to failure under high-stress conditions or if temperature rose again. Hence, it is important to have other AJP-enabled strategies available, as an alternative, that will allow to explore different materials for printing in-package dielectrics that will reliably support RF interconnects for high-stress applications. These strategies need to be flexible enough so that the dielectric material choices can be tailored to a specific application. Another challenge, which is to demonstrate that the packages are compatible with high power, will be addressed in Chapter 6.

In this section, I demonstrate two chip-first packaging strategies via AJP that yield RF performance comparable to, or better than, previously shown AM interconnects and packages, but additionally are material-flexible, overcoming adhesion challenges at the die-dielectric interface. I show the printing of dielectric materials of different viscosities and ensure that these packages provide high functional density but also optimal support for RF interconnects. As previously demonstrated chip-first SiP/SoP strategies, the ones shown here are highly adaptable and can be used for multiple die system integration.

5.1.1 Design

I demonstrate two different package design approaches that follow the fundamental concept of the chip-first strategy first shown in [66], but have significant differences. My goal is to yield application-specific SiP/SoP strategies that build on the basic concept of the chip-first approach, employing its flexibility and adaptability, but simultaneously enable the use of different dielectric materials in close proximity of the die in order to avoid adhesion issues on the die-dielectric interface. I designed the packages to be manufactured fully via AJP around a COTS die which is placed first on a metal carrier using solder ribbon. The first approach (approach 1) includes elements from the strategy demonstrated in [71], in which dies were placed in pre-manufactured substrate cavities, PI walls were printed around the cavities, and BCB was printed as a filler material and to support RF interconnects. In my approach, in contrast, the die is placed first on a metal carrier



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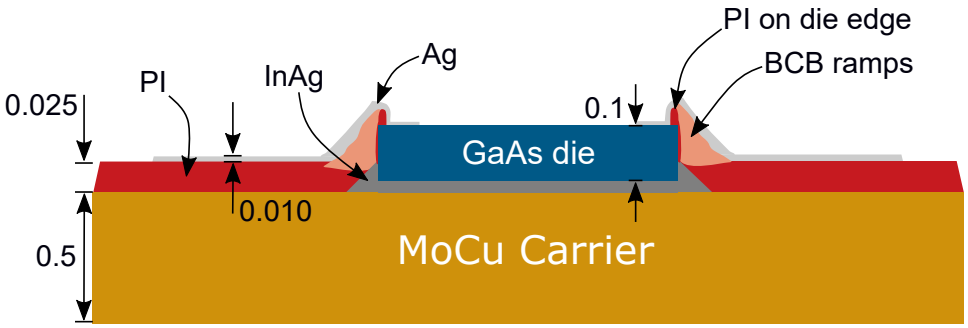


(b)

Figure 5.1: Cross-sectional illustration of the two chip-first packaging strategies, with target thicknesses in mm: (a) approach 1, and (b) approach 2. From [7] ©2022 IEEE.

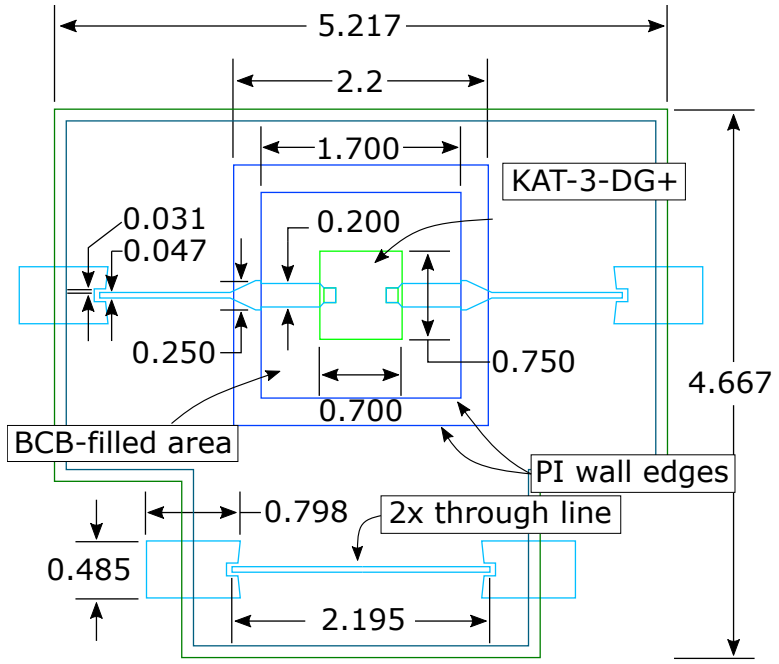
and all dielectrics and metals are manufactured around it fully via AJP. As shown in Fig. 5.1a, the PI wall extends to PI layers that act as the dielectric for the TLs, and BCB is used to fill the area between the die and the PI wall. The interconnects are designed to be printed on the die pads, over the edge of the die, and over the BCB and the PI wall, and then extend to TLs. On the other hand, approach 2, as shown in Fig. 5.1b, is an adaptation of the strategy demonstrated in [66], in which I replace the PI ramps/fillets with BCB ramps. The interconnects are to be printed on the die pads, over the edge of the die, and over the BCB ramps, and then extend to TLs. In both of these strategies, a PI path is designed to be printed on the edge of the die to smoothen the transition from the die to the BCB and deter unwanted diode effects between the printed metal and GaAs in the die [69].

All conductive paths were designed to be printed using Ag ink and consist of GCPW TLs that lead to MS TLs by means of via-less GCPW-to-MS transitions.The metal carrier is MoCu and acts as a ground reference for the die and printed circuits. The GCPW launches allow for probing with

standard GSG probes and have additional grounding straps to the MoCu carrier for improved near-DC performance. I designed the TLs to have a 50-Ω match and the via-less GCPW-to-MS transitions as demonstrated in [107]. I chose 0-dB and 3-dB attenuator bare dies (KAT-0-DG+ [129] and KAT-3-DG+ [130], by Mini-Circuits) to be packaged, both of which have an operational frequency range of 0-43.5 GHz and dimensions of $x_{\mathrm{d}} = 0.70$ mm $\times$ $w_{\mathrm{d}} = 0.75$ mm $\times$ $h_{\mathrm{d}} = 0.1$ mm. Approach 1 was used for the 3-dB attenuator and approach 2 for the 0-dB attenuator. I designed the packages to be fabricated on 0.5-mm-thick 85% Mo 15% Cu alloy plate in order to match the CTE of the GaAs dies.

Details of each design follow. In approach 1, the gap between the die and the PI wall has a rectangular footprint with dimensions of $x_{\mathrm{g}} = (x_{\mathrm{d}} + 0.5$ mm$) \times w_{\mathrm{g}} = (w_{\mathrm{d}} + 0.5$ mm$)$, so there is a gap of 0.5 mm between the die and the PI wall. This gap is to be filled with printed BCB traces of widths between 40 and 70 µm without space limitations. Reducing this gap below 0.15 mm requires smaller BCB trace widths, which might be hard to achieve with AJP, while increasing it leads to longer interconnects and higher losses. The BCB to-be-printed was designed to have a thickness of $h_{\mathrm{BCB}} = h_{\mathrm{d}} = 0.1$ mm to account for the die being slightly raised by the solder ribbon and to avoid covering the die surface with BCB while printing. I designed the PI wall with a footprint of $x_{\mathrm{w}} = (x_{\mathrm{g}} + 0.25$ mm$) \times w_{\mathrm{w}} = (w_{\mathrm{g}} + 0.25$ mm$)$, hence a total width of 0.25 mm on all sides. The area near the inner edge of the PI wall was designed to be printed thicker with more print passes, while I gradually reduced the number of passes moving towards the outer edge of the wall to achieve a smooth ramp from the wall peak to the PI acting as a dielectric substrate for the TLs. The wall peak was designed to have a thickness of $h_{\mathrm{wall}} = 1.2 \times h_{\mathrm{BCB}} = 0.12$ mm, ensuring the printed BC will not overflow it. In approach 2, the BCB ramp area was designed with a footprint of $x_{\mathrm{r}} = (x_{\mathrm{d}} + 0.15$ mm$) \times w_{\mathrm{r}} = (w_{\mathrm{d}} + 0.15$ mm$)$. The small width of 0.15 mm is enough to form smooth ramps while the interconnects are kept short to minimize losses. Both approaches can be used to package dies of different thicknesses h_{d} and areas $x_{\mathrm{d}} \times w_{\mathrm{d}}$, provided that the design fundamentals detailed here are followed.

An important design feature of the designed packages are the shaped conformal ramp intercon-



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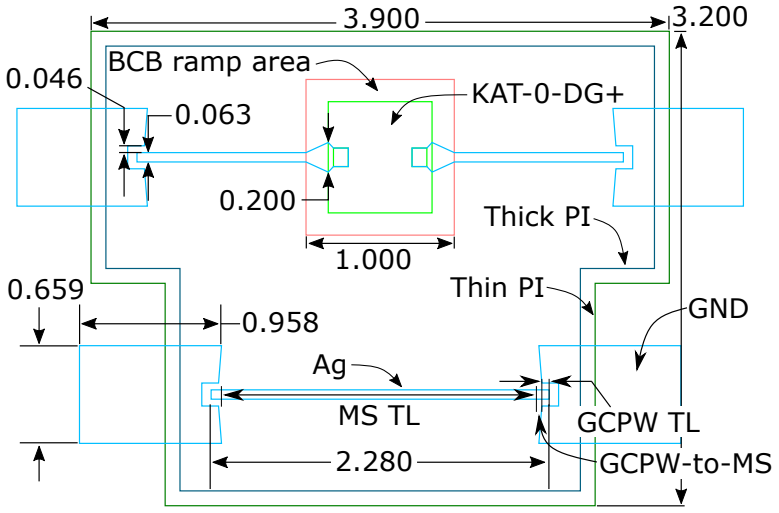
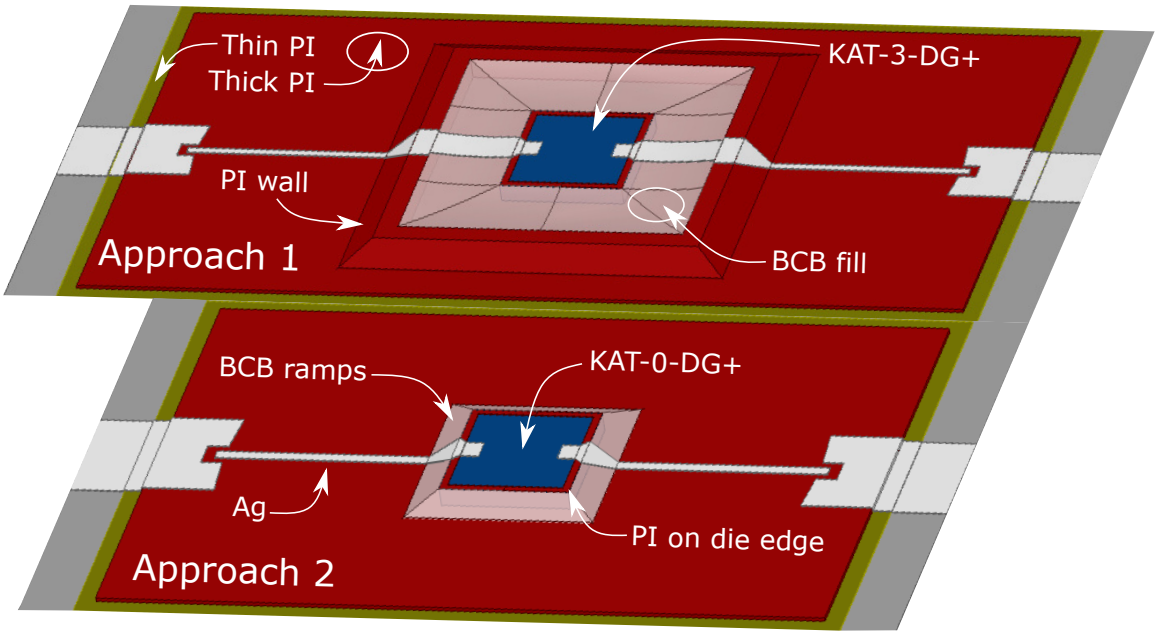


(b)

Figure 5.2: Top-down view of the design layout for both approaches, with dimensions in mm: (a) approach 1, and (b) approach 2. From [7] ©2022 IEEE.



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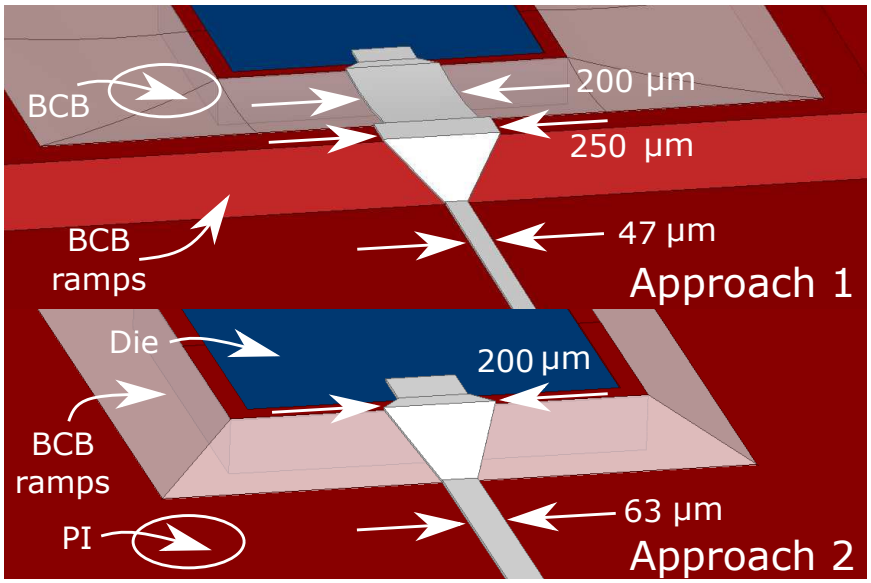


(b)

Figure 5.3: Illustrations in ANSYS HFSS©: (a) overview the package for the two approaches, and (b) close-up view of the designed shaped interconnects. From [7] ©2022 IEEE.

nects, which were first demonstrated in [74, 75]. These interconnects are shaped on the PI wall, BCB fill area and ramps, and on the die edge PI, respectively, to prevent impedance discontinuities, making the interconnects frequency-agile. For approach 1, the MS TL widens to the width of a 50-Ω MS TL on the 120-µm PI, then narrows to the right width for 100-µm BCB, and finally narrows down to the width of the COTS die pad. Respectively, for approach 2, the MS TL widens to the width of a 50-Ω MS TL on 100-µm BCB, then narrows down to the width of the COTS die pad. The packages were simulated and optimized in ANSYS HFSS©. The GCPW launches were designed to extend by 0.5 mm from the edge of the thin PI to form the grounding straps with the MoCu carrier. Design details for the two packages are shown in Fig. 5.2, an overview of the designed packages is shown in Fig. 5.3a, and details of the interconnects are shown in Fig. 5.3b. Prior to printing Ag, I optimized the TLs and interconnect dimensions after measuring the actual achieved dielectric thicknesses. A 2× through line was designed for each package to allow me to remove line loss from package measurements.

In both packaging strategies, I adjusted the package design with respect to the actual position of the placed die. This was done by rotating the design to account for a rotation or misalignment of the die after die attach. These strategies, being chip-first, are inherently flexible and tolerant to large deviations and misalignment during die attach, even in the case of packages with multiple dies as shown in [75], in which case the TLs interconnecting different dies can be designed appropriately, such as being curved or having a serpentine shape.

5.1.2 Fabrication

The first step in the fabrication process was to prepare the MoCu (85% Mo 15% Cu) carrier plate by mechanically polishing it. I chose MoCu for its CTE of 6.2 ppm/°C, which is close to the GaAs die CTE of 5.7 ppm/°C. I then did die attach using 50-µm-thick 97% In 3% Ag (97In3Ag) solder ribbon (Indium Corp.), which I first cleaned in a solution of 10 vol.% HCl + DI water. After placing the die, I reflowed the solder ribbon in a nitrogen environment to prevent oxidation of the MoCu.

The remaining of the fabrication process was to print the dielectric and conductive inks to realize the packages. As mentioned earlier, PI and BCB were utilized to print the dielectric substrates, while Ag nanoparticle ink was used to print all conductive patterns. To improve adhesion of the printed dielectrics, I applied the VM651 adhesion promoter (HD Microsystems) and the AP3000 adhesion promoter (Dow Chemicals) prior to printing PI and BCB, respectively. Like for the fully aerosol jet-printed components shown in Chapter 4, the PI ink was composed of PI-2611 (HD Microsystems [131]) diluted to 40 vol.% PI-2611 + NMP (Sigma Aldrich). Cured PI-2611 has a published $\epsilon_{\mathrm{r}} = 2.9$ and $\tan\delta = 0.002$ at 1 KHz, with a thermal curing at 350 °C for 30 min recommended to achieve its final properties. I chose PI-2611 amongst other PI inks due to its low published CTE of 3 ppm/°C to match the CTE of the GaAs dies and the MoCu carrier. The BCB ink was the Cyclotene 3022-35 resin (Dow Chemicals [132]), composed of B-staged BCB monomers diluted in mesitylene by the manufacturer. Cured Cyclotene 3022-35 has a published $\epsilon_{\mathrm{r}} = 2.65$ at 1-20 GHz and a $\tan\delta = 0.0008$. This ink has a low viscosity of 14 cSt at room temperature, thus is a good candidate to fill the area between dies and the wall formed by the higher-viscosity printed PI. Finally, as for all previous printed packages shown in this dissertation, the Ag ink consisted of 25 wt.% Clariant Prelect TPS 50 + DI water. This ink was mixed under ultrasonication for 30 min right before printing.

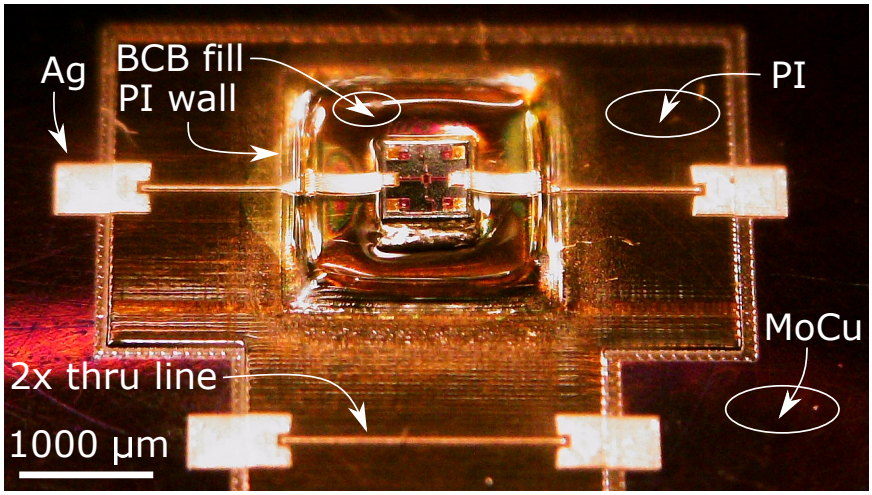
I printed all the packages with an Optomec 5X Aerosol Jet Printer [116] from a standoff distance of $\sim$3 mm from the top surface of the carrier base. While printing, I kept the MoCu carrier grounded to deter any accidental static charge building up during the aerosol deposition, which could damage the dies. During printing, the ambient temperature ranged from 24 °C to 26 °C and the relative humidity in the print chamber was between 35% and 40%. I made sure the stage was heated while printing, so that the printed dielectrics and Ag dry soon after being deposited. However, I kept the stage temperature low enough to deter curing or sintering of the materials while printing.

An overview of the printing steps follows. For approach 1, I first applied the adhesion promoter on the entire MoCu carier using a transfer pipette, allowed it to stand for 20 sec, and then blew

it dry with air. I then printed some initial PI layers (thin PI) to get a target thickness of 5 μm. Thereafter, I printed the initial layers of the PI wall to get a top height of 10 μm. Then, I printed PI on the die edge. All these first PI layers were printed at a speed (i.e., the nozzle travel speed when depositing ink) of 4 mm/sec. I did a partial curing for all the initial PI layers at 200 °C for a 2 min with a rise time of approximately 90 min and a 2 °C/min maximum temperature gradient in an inert oven under N_2. These initial PI layers acted as an adhesion layer with the MoCu surface. After the initial PI layers were cured, I printed the rest of the PI (thick PI) layers to get a total target PI thickness of 25 μm, as well as the remaining of the PI wall layers for a target peak height of of 120 μm. These layers were printed at 2 mm/sec. I then did a full curing of all printed PI at 295 °C for a 1 h with a rise time of approximately 2 h 18 min, again with a 2 °C/min maximum temperature gradient under N_2. The next step was to print BCB, after applying the adhesion promoter, at 2 mm/sec, to fill the area between the PI wall and the die. A full curing of the printed BCB layers followed, at 250 °C for a 1 h with a rise time of approximately 2 h and a 2 °C/min maximum temperature gradient under N_2.

For approach 2, I modified the printing steps to include the BCB ramps and remove the PI wall and BCB fill from the printing process. Same as in approach 1, initial PI layers were printed first, as well as PI on the die edge, followed by partial curing. I then printed the remaining PI, followed by a full curing of all PI layers. I finally printed BCB on all sides of the die, at a speed of 2 mm/sec, to form the BCB ramps.

The final step for both approaches was to print the Ag ink for the interconnects and TLs. I printed Ag at 1 mm/sec for a target thickness of 10 μm. I then sintered the printed Ag ink in air at 180 °C for 5 h with a rise time of approximately 80 min and a 2 °C/min maximum temperature gradient. The total printing time for a single package following approach 1 was around 78 min, and following approach 2 was around 60 min. As for all printed components demonstrated earlier in the dissertation, all samples were kept under vacuum in-between printing and thermal processing to deter moisture absorption and to mitigate air bubbles trapped in uncured dielectrics. The fabricated packages are shown in Fig. 5.4.



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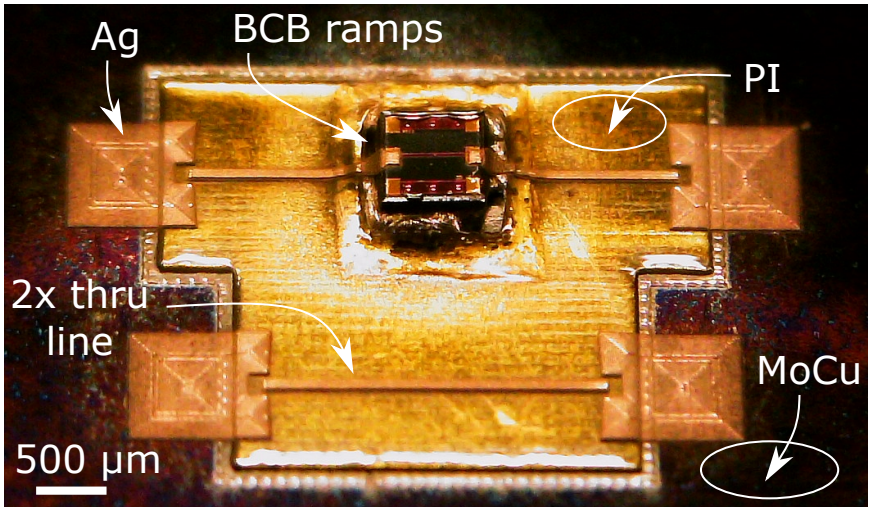


(b)

Figure 5.4: Perspective of the fabricated chip-first packages and 2× through lines: (a) approach 1, and (b) approach 2. From [7] ©2022 IEEE.

Detailed pictures of the realized interconnects for both packages are shown in Fig. 5.5 and 5.6, taken with an Olympus BX41M microscope. For approach 1, the BCB filling the area between the PI wall and the die forms a ramp after being cured, both on the BCB-die and BCB-PI wall interfaces, ensuring a smooth transition for the Ag interconnect. This happens in approach 2, as well, on the BCB-die interface, with BCB covering the side of the die completely, not allowing a short between the interconnects and the ground. This BCB characteristic behavior allowed me to print all inks at 90° relative to the MoCu surface, unlike in [66, 72, 74, 75] wherein the PI ramps

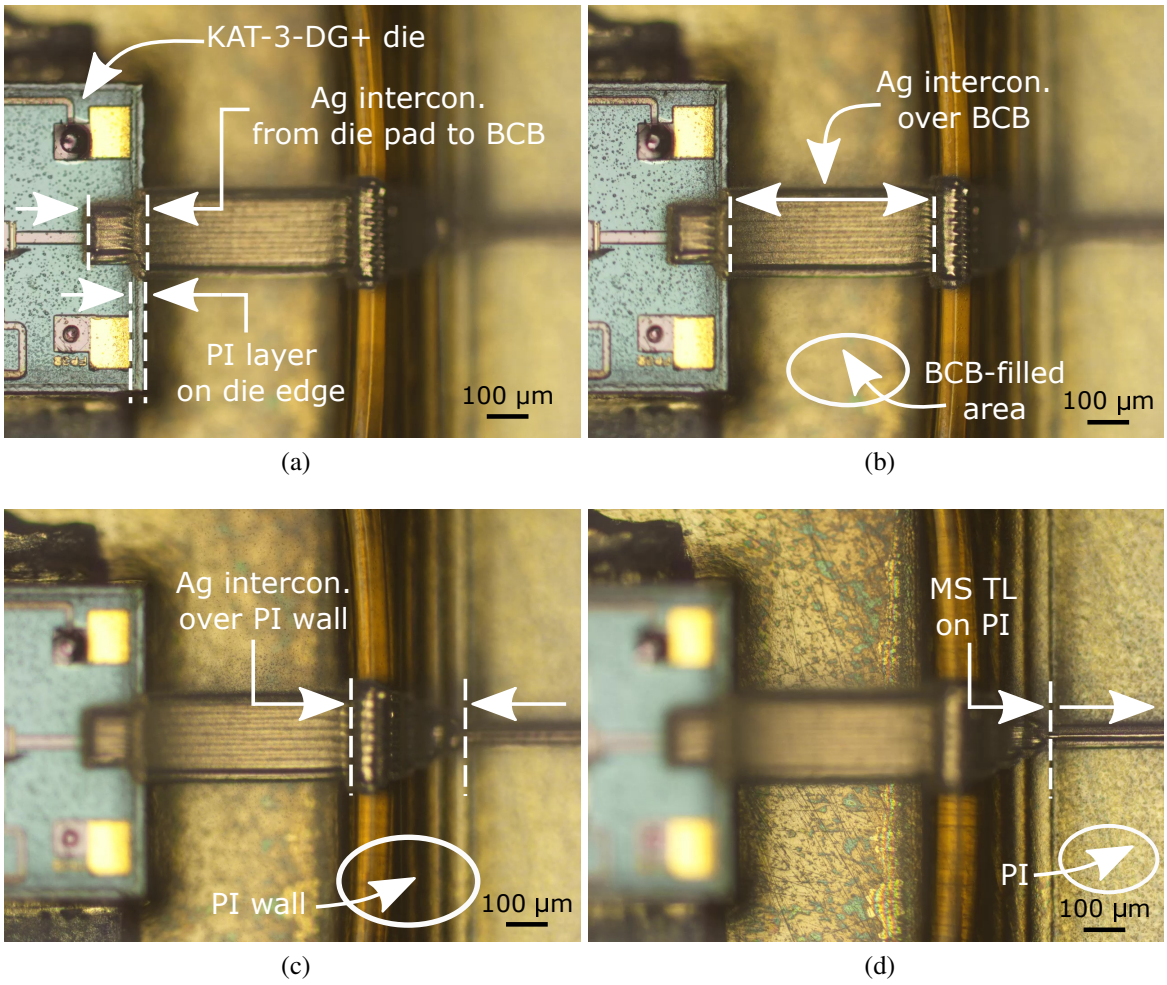


Figure 5.5: Microscopic 10× magnified photographs of the interconnect section of a fabricated package following approach 1, with focus on (a) the die, (b) the BCB-filled area, (c) the PI wall, and (d) the MS TL on PI. From [7] ©2022 IEEE.

had to be printed at a 25° to 30° angle relative to the carrier surface, from all four sides for each individual die of the package. Therefore, apart from deterring delamination of the dielectrics from the die, the two SiP/SoP strategies demonstrated here allow for printing ramps for all the dies in the package with a single printing pass, which significantly simplifies the manufacturing process comparing to the strategies shown in [66, 72, 74, 75].

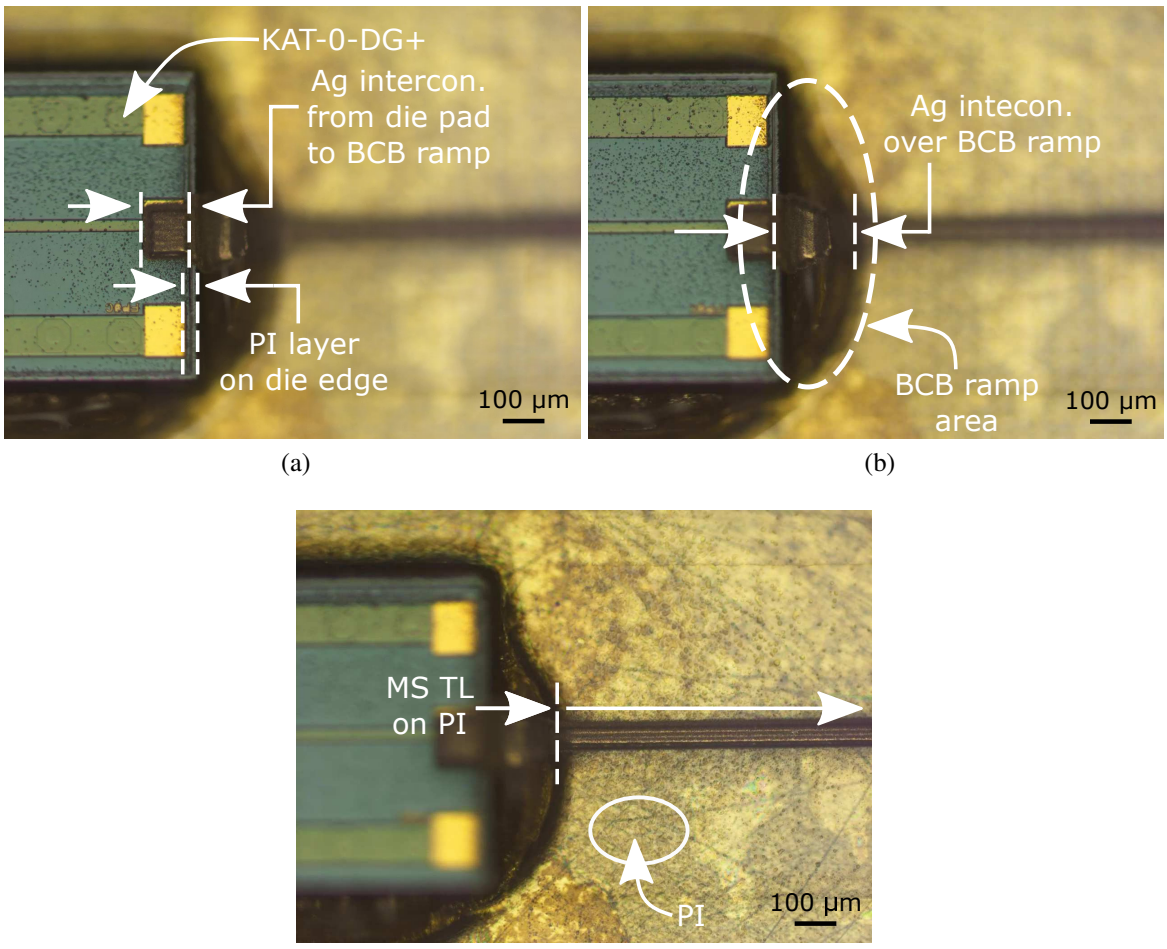
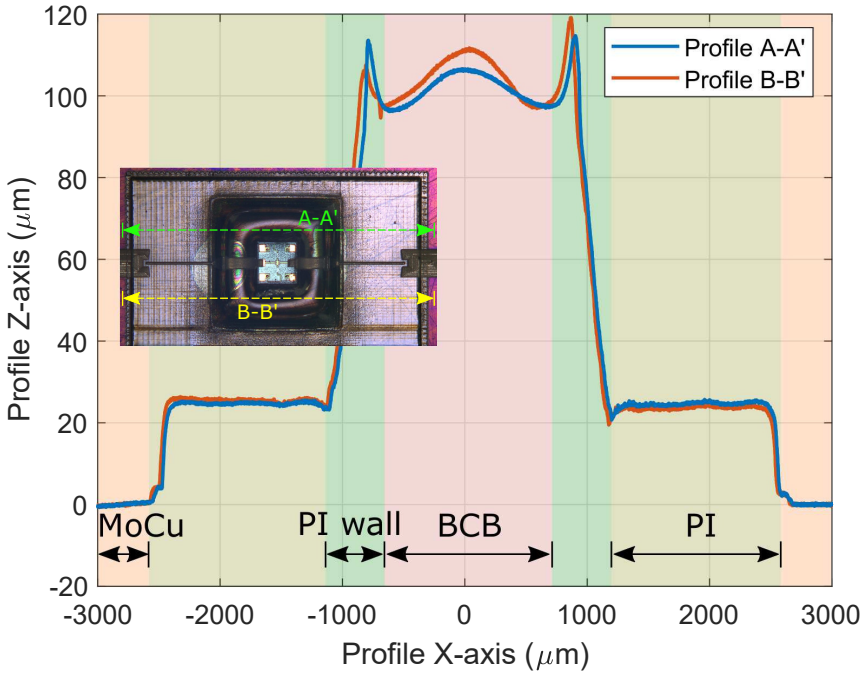


Figure 5.6: Microscopic 10× magnified photographs of the interconnect section of a fabricated package following approach 2, with focus on (a) the die, (b) the BCB ramps, and (c) the MS TL on PI. From [7] ©2022 IEEE.

Different custom versions of the demonstrated approaches are possible since they allow for design flexibility. First, regarding the carriers on which the packages were fabricated, there is no limitation on the carrier material, be it metal or dielectric, provided that sufficient adhesion is ensured (for instance, by applying adhesion promoter). Additionally, as discussed in Chapter 4 and shown in [6], printing packages on non-planar surfaces is possible with AJP, and the designs demonstrated here can be adjusted as such. There is also a lot of flexibility in terms of materials. BCB can be replaced with other, low-viscosity inks depending on the application, while a low-loss, higher-viscosity ink can replace PI, provided that there is no significant CTE mismatch between dielectric inks, the substrate, and the die. Furthermore, AJP has high alignment accuracy and is capable of aligning the printer to fine die features, such as pad corners. This enhances the design flexibility and allows for highly customized packages incorporating multiple dies, something that would be impossible to achieve with conventional manufacturing methods. Finally, as in [66, 72, 74, 75], the packages demonstrated here were fabricated using only one major piece of equipment, i.e. the aerosol jet printer. As discussed in Chapter 1, conventional methodologies a lot more equipment, a cleanroom environment, and a lot more chemical processes that generate a lot more material waste.

5.1.3 Results

I first took measurements of the surface profiles of the manufactured packages using a NanoMap-500LS surface profilometer. The profiles for approach 1 are shown in Fig. 5.7. Profiles A-A' and B-B' in Fig. 5.7a show the transitions from the MoCu to the PI, then to the peak of the PI wall, and then to the BCB fill. The BCB peak at $\sim X = 0$ is due to the solder ribbon underneath the printed BCB and does not indicate the actual thickness of the BCB; the actual BCB thickness can be seen left and right of the peak. The measured thicknesses for both approaches are summarized in Table 5.1. Differences between the intended and achieved thicknesses are due to variations in ink atomization during printing. Nevertheless, the measured thicknesses are consistent with the targeted ones. These variations can be mitigated using methods such as described in [133, 134].



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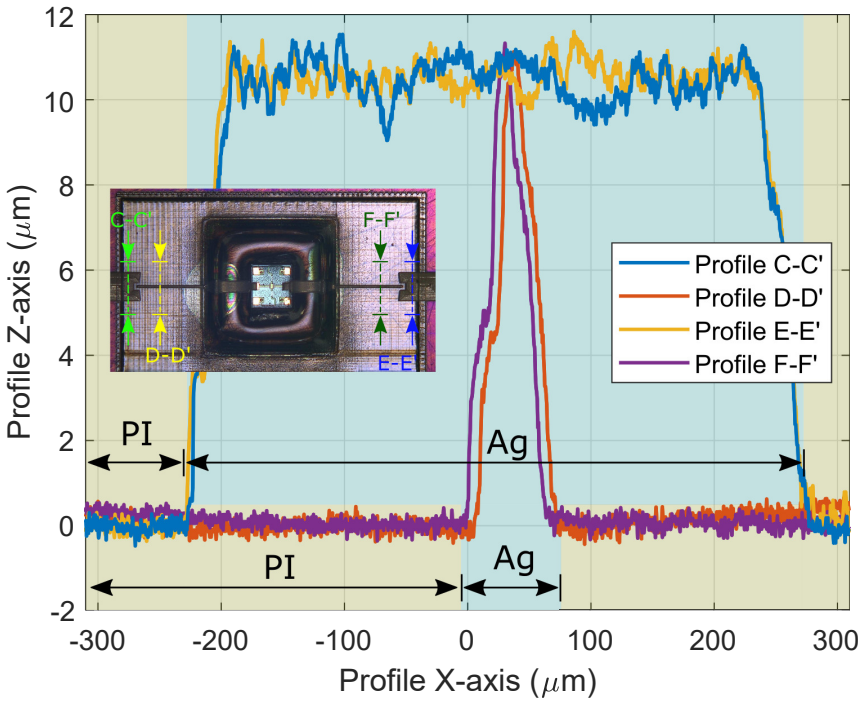


(b)

Figure 5.7: Measured thickness profiles for a package fabricated following approach 1, with detailed view of profile measurement paths and areas for: (a) PI and BCB surfaces, and (b) Ag surface. From [7] ©2022 IEEE.

Table 5.1: Measured Printed Material Thicknesses

Ref.	Target Thickness (μm)	Measured Thickness (μm)	
		Approach 1	Approach 2
PI	25	24	27
PI wall†	120	113	N/A
BCB fill#	100	98	N/A
Ag	10	11	8

† Measured at peak; # measured at valley. From [7] ©2022 IEEE.

The actual dielectric thicknesses were taken into consideration while optimizing the TLs and interconnects in ANSYS HFSS©, before printing Ag. The final Ag thickness was taken into account in the final simulations that are compared to measurements later.

I analyzed the dimensional integrity of the fabricated packages by taking microscopic pictures with an Olympus BX41M microscope. Pictures of key parts of the printed Ag patterns with overlaid measured features are shown in Fig. 5.8. The realized line widths are greater than the designed ones by only 2-3 μm, and the realized gaps are narrower by 2-3 μm. These small differences are likely a result of the toolpath generation algorithm or due to small variations in the individual printed lines width. Overall, the printed lines are consistent and feature a small number of sharp edges as expected from AJP.

I then measured the RF performance of the packages from 50 MHz to 50 GHz, which covers the operational frequency range of the attenuators from 0-43.5 GHz, using an MPI TS150-THZ Probe System, a Keysight N5227 PNA, and a pair of GGB 67A-GSG-250-P picoprobes. I performed an LRRM calibration using a GGB CS-5 calibration substrate to bring the reference planes to the probe tips. I measured two packages for each approach to ascertain if there is repeatability in RF performance. For each package, I examine the transmission and reflection coefficients and compare to those of the unpackaged die, as well as the package after removing the TL loss. I also characterize single interconnect loss and total line and interconnect loss per package, and compare

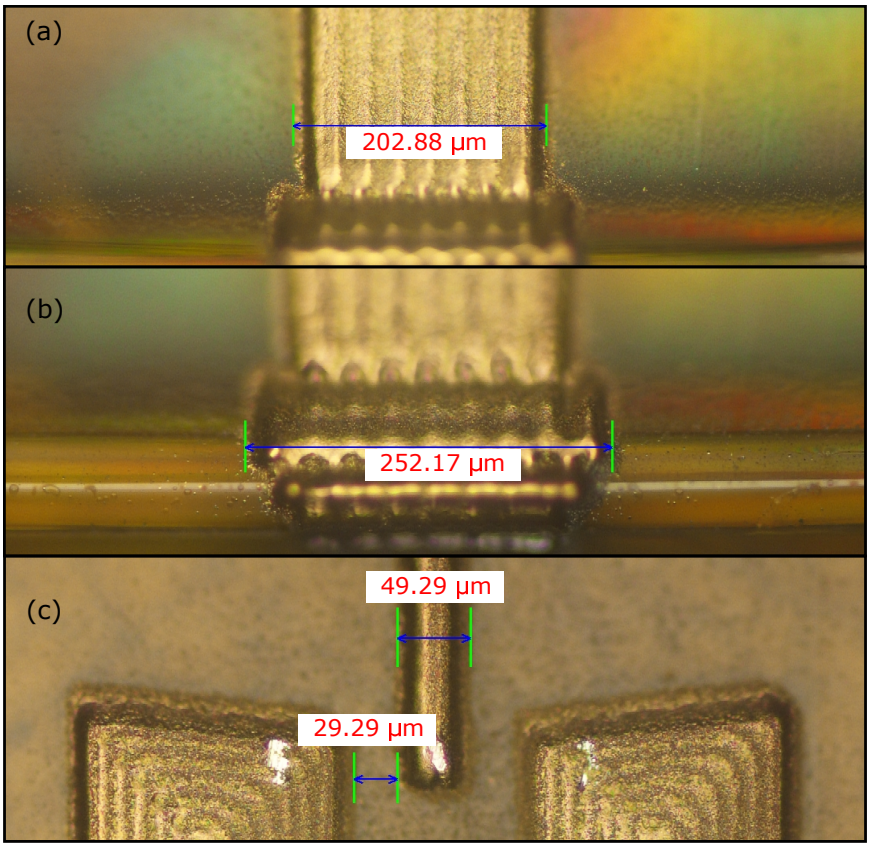


Figure 5.8: Microscopic 50× magnified photographs of the TL and interconnects of a fabricated package following approach 1, with overlaid measured dimensions: (a) interconnect over the BCB fill, (b) interconnect over the PI wall, and (c) GCPW and MS TL. From [7] ©2022 IEEE.

to other state-of-the-art interconnects and packages in the literature.

I first show the simulated and measured RF performance for the two packages following approach 1 in Fig. 5.10. I measured the unpackaged die under and the 2× through line under the same conditions as the packages. I used the 2× through line measurements to calculate the interconnects + die loss alone, which is (in dB):

$$S_{21}^{id} = S_{21}^{m} - S_{21}^{l}, \tag{5.1}$$

where S_{21}^{m} and S_{21}^{l} are the loss (in dB) of the measured package and the 2× through line, respectively. All these losses are compared in Fig. 5.10a. The interconnects + die losses for both packages correlate well with the loss of the die alone, showing that the realized interconnects have low loss. In addition, the 2× through line has a loss ≤ 0.8 dB up to 50 GHz. The reflection ratios

Figure 5.9: RF measurements setup for the fabricated packages.

are shown in Fig. 5.10b, with both packages demonstrating an $S_{11} < -10$ dB up to 50 GHz. As shown in Fig. 5.11, the interconnect losses are higher for the packages following approach 2, hence these packages have higher losses than the 0-dB attenuator die. They demonstrate $S_{11} < -10$ dB up to 30 GHz, but show higher reflections as frequency approaches 50 GHz.

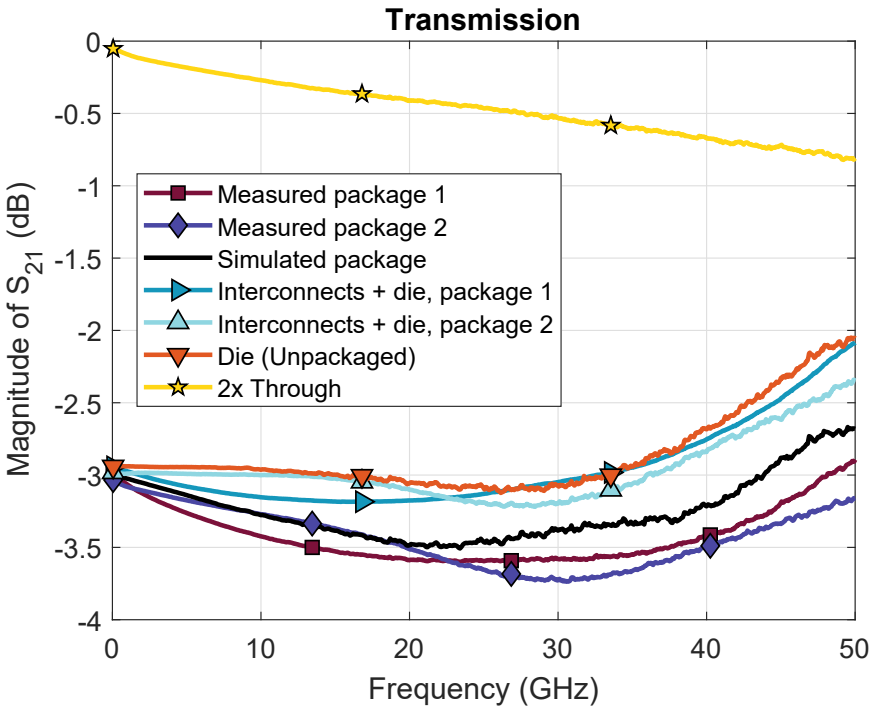
I also characterize the single interconnect loss for both approaches. The loss of a single interconnect is given (in dB) by:

$$S_{21}^{i} = (S_{21}^{m} - S_{21}^{l} - S_{21}^{d})/2, \tag{5.2}$$

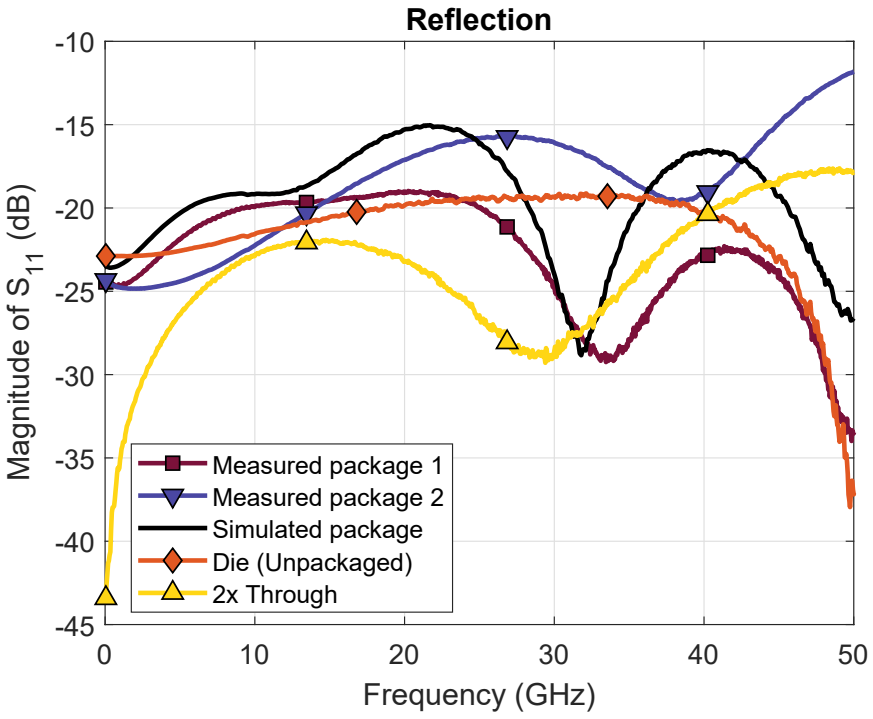
where S_{21}^{d} represent the die loss (in dB), and is shown for all packages in Fig. 5.12a. The interconnects of both packages using approach 1 demonstrate a very low loss of < 0.2 dB up to 50 GHz and their individual performances correlate well, with a variation in loss of less than 0.13 dB over the range of measurement and less than 0.04 dB over the operating range of the attenuator. These loss variations are smaller than the ones reported up to 50 GHz for the two packages demonstrated in [66]. For approach 2, package 1 shows a loss < 0.4 dB up to 50 GHz, while package 2 shows a loss of ≤ 0.93 dB. The loss variation is less than 0.58 dB over the range of measurement and less than 0.54 dB over the operating range of the attenuator. In the frequency range from 19.6 to 21.5 GHz and from 27.9 to 33.8 GHz for package 2 following approach 1 and for package 1 following approach 1, respectively, one can notice nonpassivity errors in S_{21}^{i}, with magnitudes ≤ 0.02 dB.

These errors can be attributed to variations in the magnitude of the reflection between the calibration trace and the measured packaged dies, and to the fluctuation in the performance of the probe launches at the measured frequency range.

The performance variation between the two packages following approach 2 can be ascribed to the landing position of the GSG probes on the GCPW launches and deviations in the profile of the BCB ramps. Specifically, using solder ribbon or epoxy for die attach cannot ensure the die rests flat on the carrier, since the ribbon or the deposited epoxy have thicknesses comparable to the die. In general, if the die does not sit planar on the ribbon/epoxy surface, small gaps can be formed underneath the die, and the low-viscosity BCB will tend to flow to those gaps, causing deviations in the ramp profile. Furthermore, non-uniformities on the ribbon/epoxy surface extending around the die can cause the BCB to flow away from the die edge, also causing deviations in the ramp profile. These deviations generally cause impedance discontinuities at the RF path on the interconnects printed over the BCB. The higher measured losses observed for approach 2 comparing to the simulations, as well as the higher losses of packages following approach 2 compared to approach 1, can be ascribed to such impedance discontinuities, as well. Unlike approach 2, approach 1 is inherently resistant to this problem, since the area where I printed BCB is significantly larger than in approach 2 and a non-planar die or non-uniformities in the ribbon/epoxy surface do not significantly affect the uniformity of the BCB thickness profile. The robustness of approach 2 against such problems can be improved, however, by using a solder ribbon much thinner than the die, or with aerosol jet-printed die attach pads with controlled thickness and dimensions, which will facilitate a planar die placement and achieving uniform dielectric thicknesses around the die.

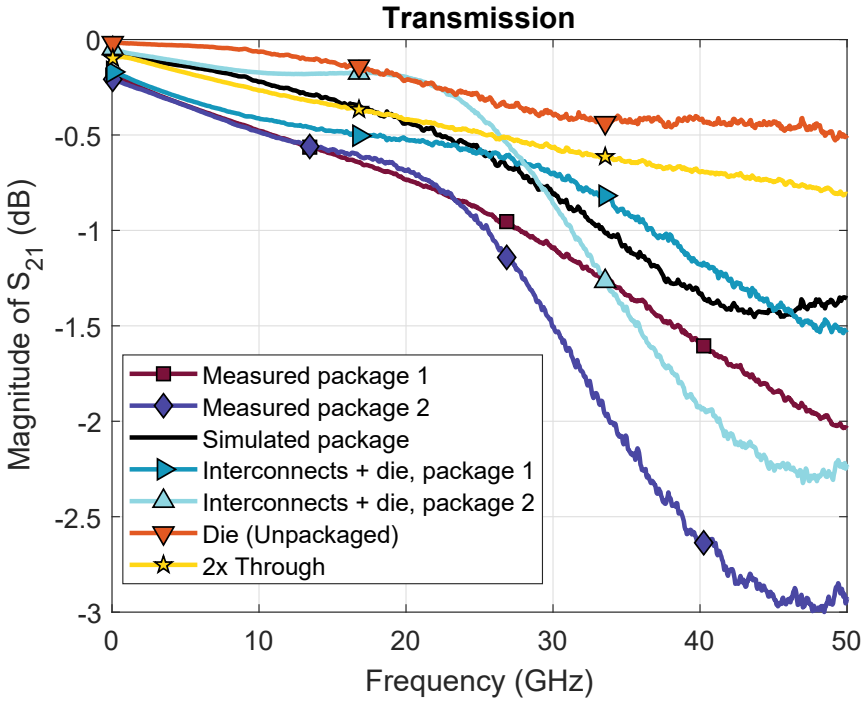


(a)

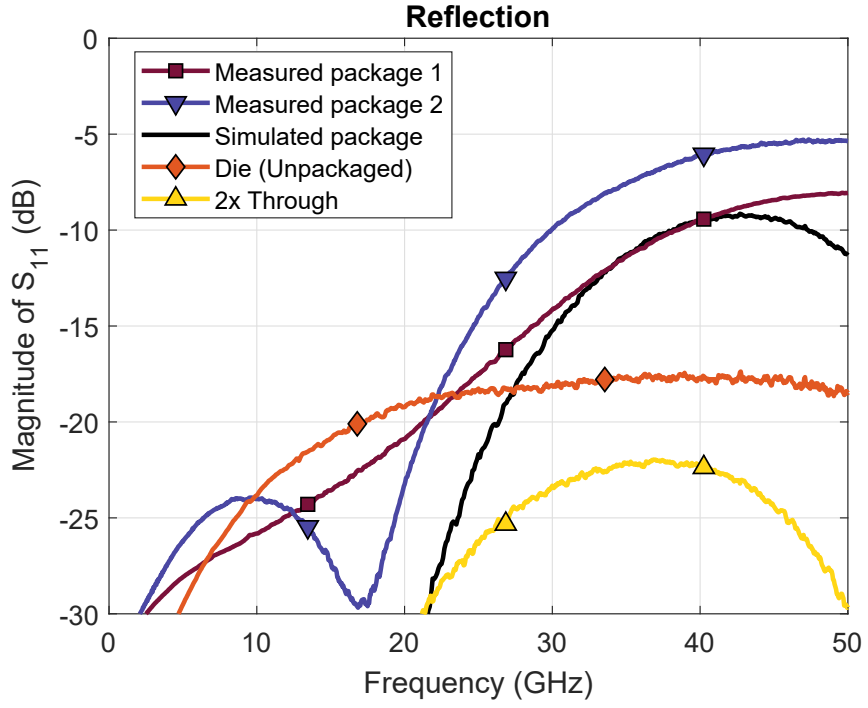


(b)

Figure 5.10: Measured and simulated (a) transmission, and (b) reflection S-parameters of the two identical fabricated packages following approach 1, the unpackaged attenuator die, and the fabricated 2× through line. Approach 1 uses a 3-dB attenuator die. From [7] ©2022 IEEE.

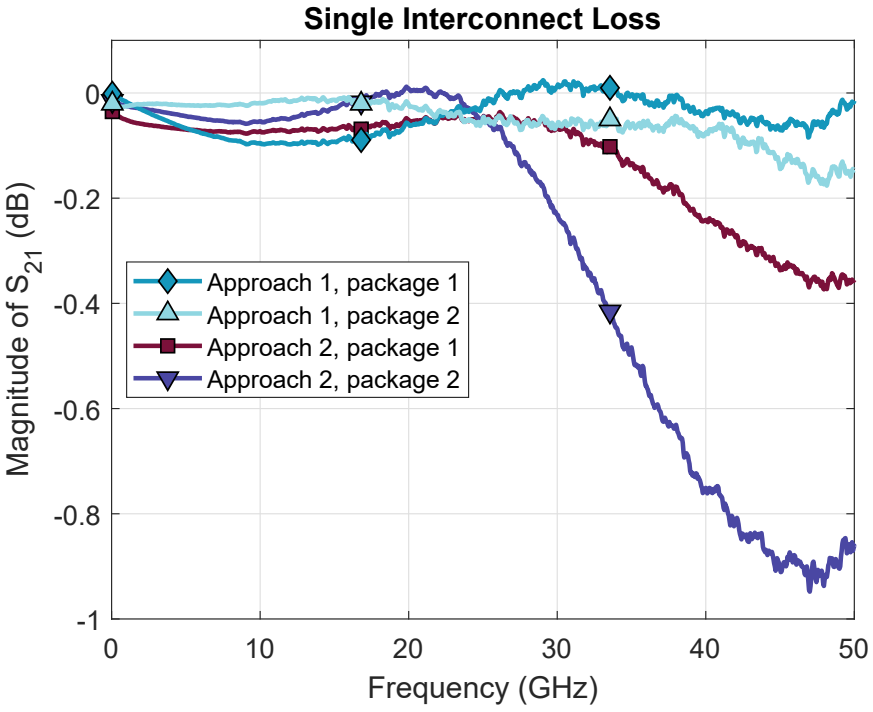


(a)

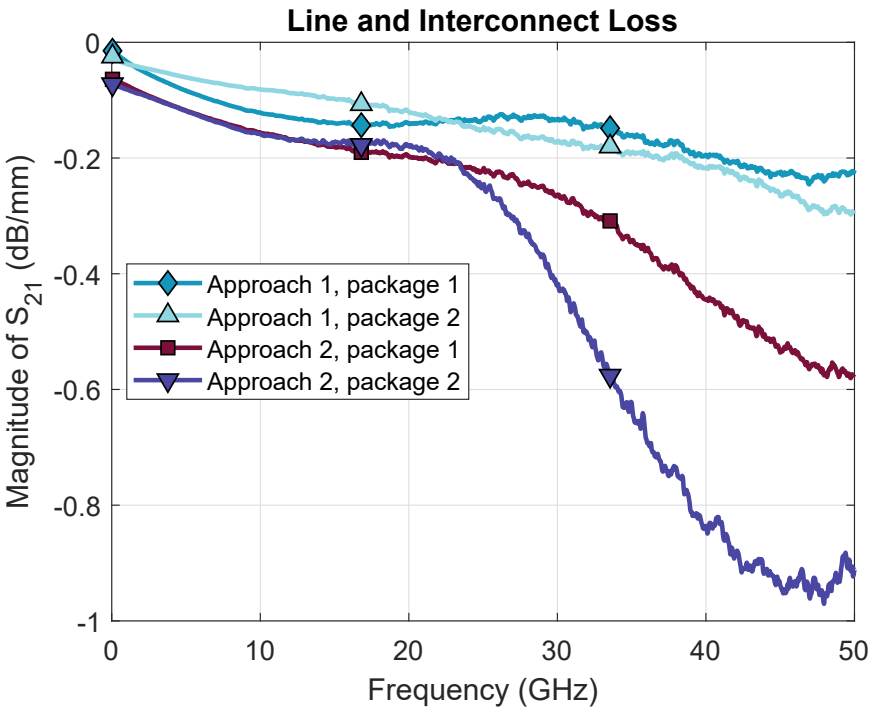


(b)

Figure 5.11: Measured and simulated (a) transmission, and (b) reflection S-parameters of the two identical fabricated packages following approach 2, the unpackaged attenuator die, and the fabricated 2× through line. Approach 2 uses a 0-dB attenuator die. From [7] ©2022 IEEE.



(a)



(b)

Figure 5.12: (a) Single interconnect loss, and (b) normalized line and interconnect loss. From [7] ©2022 IEEE.

To compare with other additively manufactured packages and interconnects, I calculated the total line + interconnect loss per mm for each package, which is given by:

$$S_{21}^{il} = (S_{21}^{m} - S_{21}^{d})/L, \tag{5.3}$$

where L is the total interconnect + line length in each case, and is shown for all packages in Fig. 5.12b. Same as for the single interconnects, the line + interconnect loss for the two individual packages following approach 1 is very close, whereas the loss difference for the two packages following approach 2 is larger. In spite of these differences, all packages are fully functional at mm-wave, high-performance, and fully aerosol jet-printed. The packages following either approach demonstrate performance comparable to, or better than, other packages and interconnects in the literature, as shown in Table 5.2. Approach 1 has an average line + interconnect loss of ≤ 0.26 dB/mm up to 50 GHz. This performance is similar to [66, 72], but approach 1 allows for more flexibility in dielectric material choice to deter delamination near the die. In [122], 0.1 dB/mm was shown at 20 GHz, but the interconnects were not fully printed and there was no packaged die. Comparing to SiP/SoP methods via IJP, the strategies in this work show line + interconnect loss of 0.14 dB/mm and 0.23 dB/mm at 24.5 GHz for approaches 1 and 2, respectively, in contrast to 0.45 dB/mm and 0.57 dB/mm achieved in [65]. Finally, [67–69] employed hybrid strategies combining conventional and AM techniques, and show performance comparable to this work, or worse, but their processes require longer prototyping time, more equipment, more chemical processes, and more material waste. Importantly, the loss calculations in Equations (5.1)−(5.3) include, in addition to transmission loss, the effect of mismatch loss. These calculations yield the true total loss and do not exclude the effect of mismatch at any frequencies, thereby reflecting the real RF performance of interconnects and packages.

Table 5.2: Comparison of State-of-the-Art AM Packages and Interconnects

Ref.	Fabrication Process	Packaging Application	Package Loss (dB) *	Intercon. + Line Loss (dB/mm)
This work	**AJP**	**Intercon. on GaAs†**	**3.55 (20 GHz),** ** **3.03 (50 GHz)** **	**0.13 (20 GHz),** ** **0.26 (50 GHz)** **
		Intercon. on GaAs#	**0.71 (20 GHz),** ** **2.5 (50 GHz)** **	**0.19 (20 GHz),** ** **0.74 (50 GHz)** **
Craton *et al.* [75]	AJP	AM SoP (3×GaAs)	2.8 (78 GHz)	0.6 (78 GHz)
Craton *et al.* [74]	AJP	AM SoP (GaAs)	1.1 (85 GHz)	0.37 (85 GHz)
Craton *et al.* [72]	AJP	Intercon. on GaAs	1 (15 GHz)	0.33 (15 GHz)
Craton *et al.* [66]	AJP	Intercon. on GaAs	0.42 (20 GHz)	0.15 (20 GHz)
Delage *et al.* [122]	AJP on ceramic	Intercon. on 3D half-sphere	0.17 (20 GHz),‡ 0.34 (60 GHz)‡	0.1 (20 GHz),‡ 0.6 (60 GHz)‡
Konstantinou *et al.* [6]	AJP	UWB TLs	4.19 (20 GHz),** 6.28 (60 GHz)**	0.34 (20 GHz),** 0.51 (60 GHz)**
Qayyum *et al.* [121]	AJP on Verowhite/LCP	UWB TLs	1.26 (50 GHz), 3.43 (110 GHz)	0.18 (50 GHz),‡ 0.49 (110 GHz)
Tehrani *et al.* [65]	IJP	Intercon. on GaAs	1.08 (24.5 GHz)	0.45 (24.5 GHz)
		Intercon. on GaAs	2.9 (24.5 GHz)	0.57 (24.5 GHz)‖
Ihle *et al.* [68]	AJP on LTCC, MD§	Intercon. on GaAs	0.6 (20 GHz),‡ 1 (50 GHz)‡	0.24 (20 GHz),‡ 0.4 (50 GHz)‡
Ramirez *et al.* [67]	FDM,¶ MD, LMM	Intercon. on GaAs	2.4 (20 GHz)	0.2 (20 GHz)
Oakley *et al.* [69]	AJP on LCP, conventional	Intercon. on GaAs	N/A	0.13 (20 GHz),‡ 0.42 (40 GHz)‡

* Includes unpackaged COTS die losses; † approach 1 (3-dB attenuator die);
# approach 2 (0-dB attenuator die); ** avg. loss of two packages; ‡ approximated for comparison;
‖ measured at low-loss point; § micro-dispensing; ¶ fused deposition modeling.

5.2 System-on-Antenna Module

The second part of the chapter focuses on system integration using the SiP/SoP fundamentals discussed in Section 5.1. I utilize approach 1, which performed the best, to show system integration for a microwave transmit module. Microwave and mm-wave electronics for wireless applications such as automotive and biomedical imaging, wireless communications, and military and space systems have seen an increasing demand over the recent years. Inherently, flexible and cost-effective techniques for heterogeneous system integration with high functional density for such electronics is highly desired. The design and material flexibility and high functional density afforded by AJP can be employed in realizing microwave and mm-wave transmit/receive (T/R) RF front-end modules.

To the best of my knowledge, the only example of a module fully via AM was shown in [75], where a W-band SoP was fully printed alongside an in-package patch antenna. This approach, though, is limited to very high frequencies, as patch antennas at lower frequencies are large and printing them requires long prototyping time. In contrast, SoA concepts offer a lot of design flexibility while simultaneously allowing the designer to use antennas of desired size and type. To date, such SoA have been manufactured predominantly with conventional or hybrid AM-conventional methods. Gjokaj *et al.* [135] demonstrated SoAs for which circuits were fabricated via lithography and were embedded in 3D-printed Vivaldi antennas, while in [136] used AJP as part of the circuit manufacturing process, as did Oakley in [137]. He *et al.* [76] showed a SoA by placing pre-packaged MMICs on a 3D-printed antenna and using IJP to print dielectric filling and RF interconnects. To the best of my knowledge, there have been no demonstration of SoAs with AM packaging of bare dies on-antenna.

In this section, I demonstrate the packaging entirely via AJP of a COTS amplifier die to realize a transmitter SoA module in the Ku-band. The package design is flexible and is adapted to accommodate the positioning of the amplifier die on a conventionally manufactured Vivaldi antenna. I utilized a modified version of approach 1 that was demonstrated in Section 5.1 to realize all dielectrics, interconnects, TLs, and DC paths fully via AJP. In this work, I show the packaging,

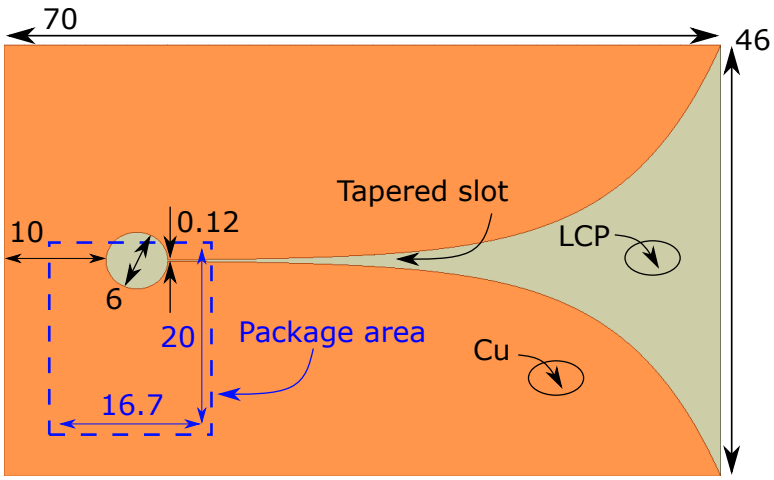


Figure 5.13: Annotated design of the Vivaldi antenna in ANSYS HFSS© (with dimensions in mm).

fully via AJP, of a commercial-off-the-shelf amplifier die to realize a transmitter SoA at Ku-band. The design is flexible, with the entire package designed with respect to the die, and is adapted to fit on a conventionally manufactured Vivaldi antenna. The die is packaged using a chip-first approach, with all dielectrics and conductive paths aerosol jet-printed. The transmit module shows radiated power levels of 0.4-0.66 W, higher than other SoAs in the literature at similar frequencies. The work demonstrated in this section shows the potential to realize high-functional-density RF front-end modules fully via AJP.

5.2.1 Design

The first step was to design the Vivaldi antenna. I aimed to achieve loss and high gain at the desired frequencies. The package and circuity were designed thereafter, adapted to the antenna. The antenna designed was a notch Vivaldi antenna on a Cu/LCP/Cu board. Important design parameters were the cavity radius, the width of the slot opening, and the position of the feed relative to the start of the slot opening, which all determined the antenna impedance and are shown in Fig. 5.13.

The designed package combines an amplifier die and a pre-packaged voltage-controlled oscillator (VCO) MMIC, and I designed it with respect to the amplifier die. The package design follows the chip-first strategy, specifically approach 1, as demonstrated in Section 5.1. The package design

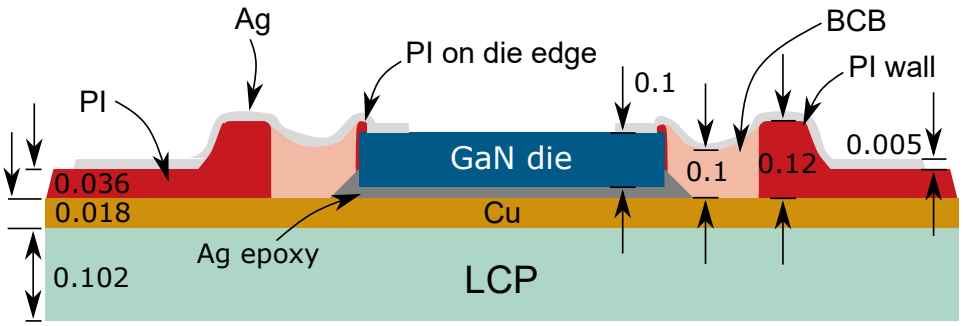


Figure 5.14: Cross-sectional view of the packaging strategy for the amplifier die, with target material thicknesses (with dimensions in mm).

was modified to integrate the surface-mount VCO, as well as surface-mount components (SMCs) for the required biasing networks. The amplifier used was a TGA2958 (Qorvo) GaN driver amplifier die and the VCO was a HMC632LP5 (Analog Devices) pre-packaged MMIC. The package incorporates a multi-level dielectric substrate structure, in which a PI wall was designed to be printed around the die and the area between the die and the wall was designed to be filled with BCB. The RF and DC amplifier die interconnects were designed to be printed over the PI wall and the BCB all the way to the die pads. A layer of PI was designed on the die edge to deter unwanted diode effects. Ag conductive patterns were designed for die interconnects, DC lines, RF TLs, and pads for the VCO and the SMCs. The pattered Cu of the antenna was designed to act as the ground for the circuit. Design details for the interconnects, TLs, and the antenna feed are shown in Fig. 5.15. The entire structure was optimized in ANSYS HFSS©.

Importantly, the packaging strategy demonstrated here is not limited to one die only, but can incorporate a VCO die if one is available at desired frequencies. Besides, the concept of multi-die, chip-first packaging has been demonstrated in [75]. This SiP/SoP strategy is mm-wave-capable, as demonstrated in Section 5.1 [7] and can be used for mm-wave SoAs. Moreover, choosing a VCO die and smaller SMCs and DC connectors can significantly reduce the package area and the package can thus be printed on smaller, mm-wave antennas.

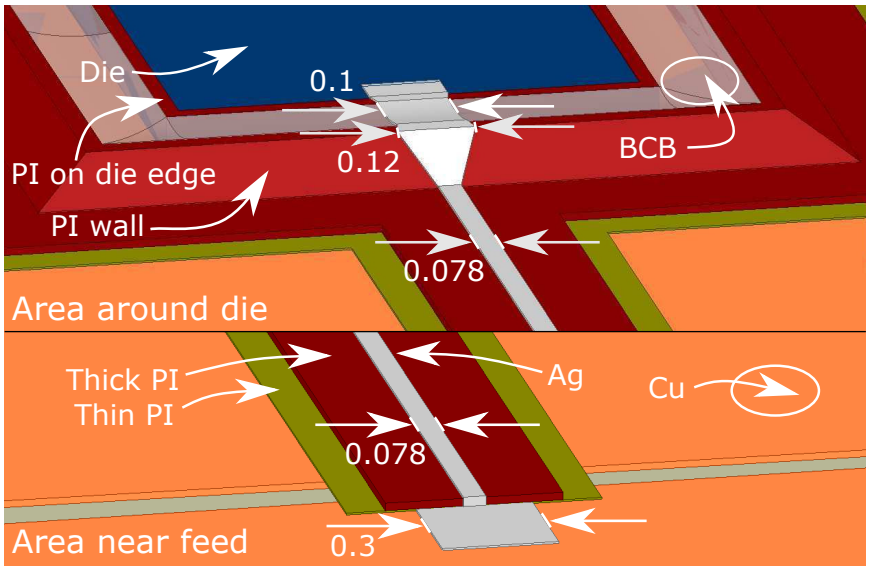


Figure 5.15: Details of the amplifier die RF interconnects, MS TL, and antenna feed in ANSYS HFSS© (with dimensions in mm).

5.2.2 Fabrication

The fabrication of the antenna was done first and with help from Brian Wright at MSU. The Cu on a 4-mil-thick Felios R-F705T LCP board was etched via lithography to form the antenna shape and the pads for the DC connector. I then did die attach for the amplifier die on the antenna Cu using Epo-Tek H20E Ag epoxy, which was cured in N_2 to prevent oxidation of the Cu. The rest of the fabrication was for the package and was done entirely via AJP, following the procedures detailed in Section 5.1. Before printing PI and BCB, I applied the appropriate adhesion promoter in each case. I first printed the initial PI layers for a target thickness of 5 µm, the first layers of the PI wall for a top height of 10 µm, and PI on the die edge, followed by a partial curing at 200 °C in N_2. I then printed additional 31 µm of PI in areas supporting the MS TLs and the VCO pads, as well as the rest of the PI wall for a target top height of 120 µm, followed by a full curing of all PI layers at 295 °C in N_2. Next, I printed BCB to fill the area between the die and the PI wall, and then fully cured it at 250 °C in N_2. I finally printed Ag ink on the PI and BCB to form the TLs and the die interconnects, the DC lines, the pads for the VCO and SMCs, and the antenna feed, followed by a sintering in atmosphere at 180 °C. Details of the printing process are given in Appendix C.

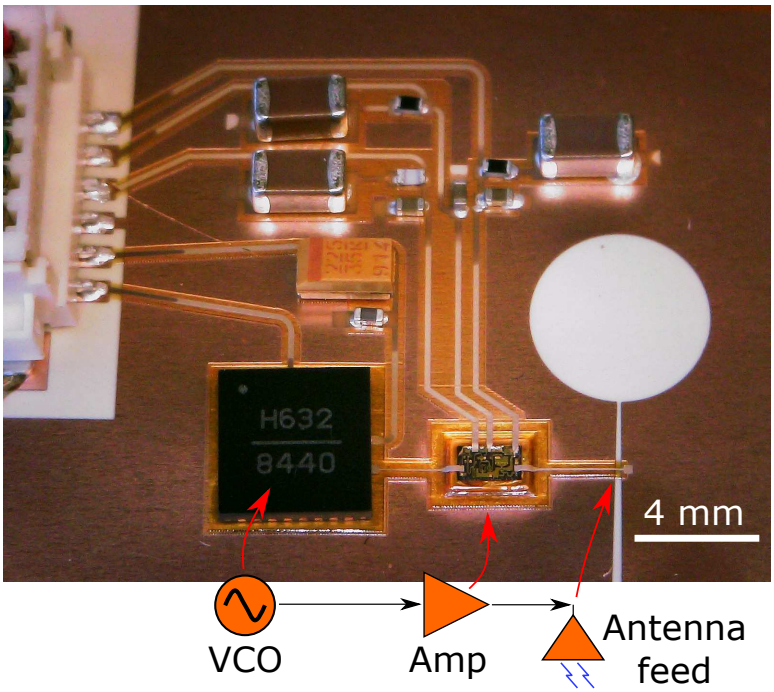


Figure 5.16: Close-up photo of the manufactured SoA package.

The final step was the placement of the VCO, SMCs, and DC connector using Epo-Tek H20E Ag epoxy, followed by reflow and sintering of the Ag epoxy. The manufactured package is shown in Fig. 5.16 and the packaged amplifier die is shown in Fig. 5.17.

As in the rest of this dissertation, all printing was done with an Optomec Aerosol Jet 5X Printer. The PI ink was composed of PI-2611 (HD Microsystems) diluted to 40 vol.% PI-2611 + NMP (Sigma Aldrich). The BCB ink was the Cyclotene 3022-35 resin (Dow Chemicals). The Ag ink was diluted in 25 wt.% Clariant Prelect TPS 50 + DI water. The total printing time for the package was 6 h and 31 min.

5.2.3 Results

I measured the received power spectrum of the SoA with a N9917A FieldFox Handheld Microwave Analyzer connected to a Vector Telecom PTY Ltd horn antenna via a 4-ft-long coaxial cable and an attenuator to protect the analyzer. The measurement setup is shown in Fig. 5.18a. The horn antenna had a gain of $G_{\mathrm{r}} = 20$ dBi at the measurement frequencies, the total cable loss was $L_{\mathrm{r}} = 3.5$ dB,

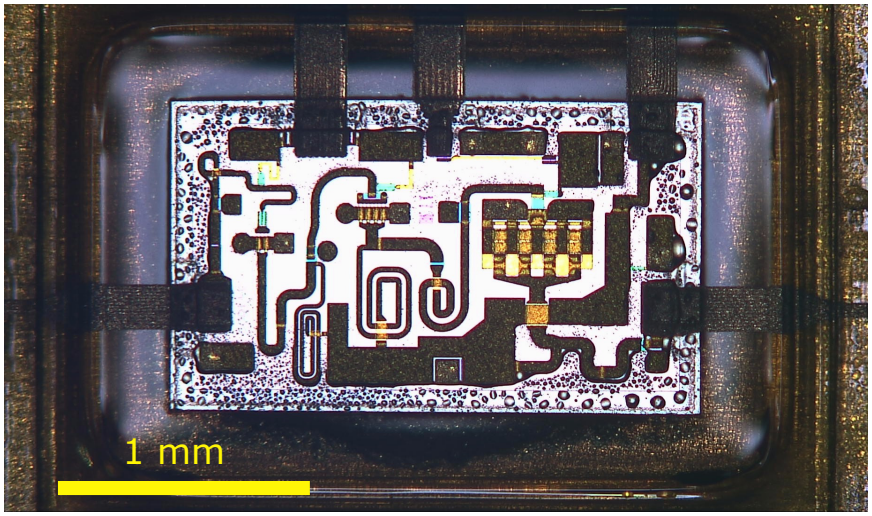
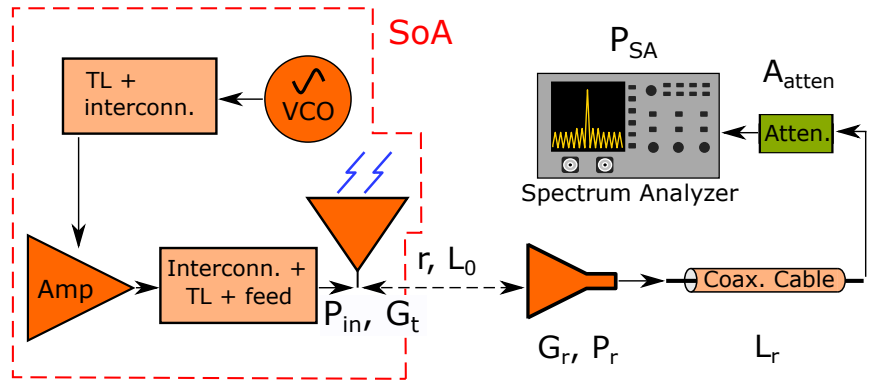


Figure 5.17: Close-up photo of the packaged amplifier die and interconnects.

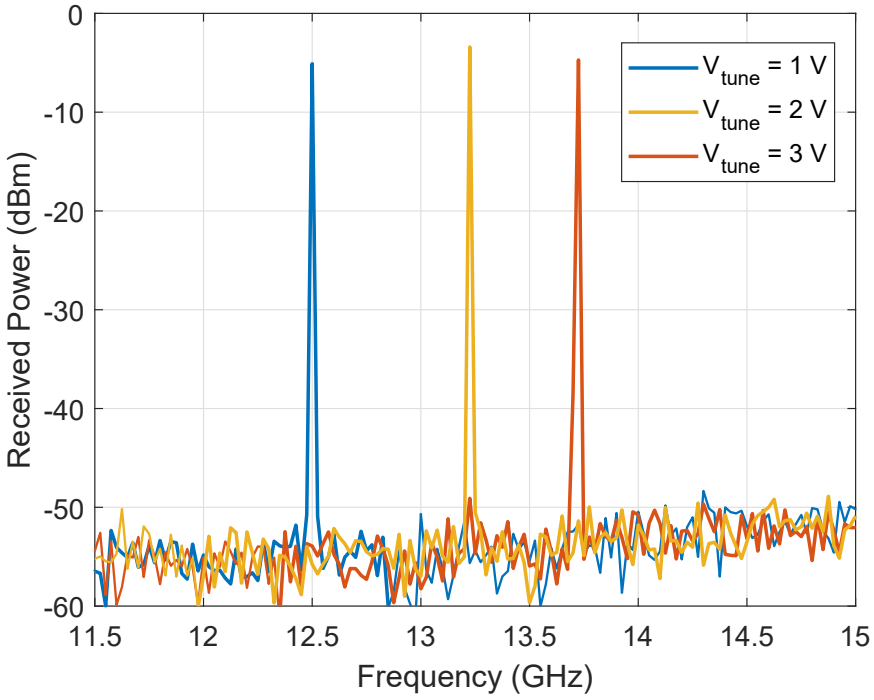
and the attenuator gave an attenuation of $A_{\text{atten}} = 5$ dB. I placed the SoA at a distance of $r = 240$ mm from the receiving horn antenna, and the free-space loss was $L_0 = 20\log(4\pi r/\lambda)$. I measured the received power applying three different VCO tuning voltages, with the VCO generating an RF signal at different frequency each time. The measured attenuated received power, P_{SA}, is shown in Fig. 5.18b. To compare with other state-of-the-art SoAs, I calculated the effective isotropic radiated power (EIRP) in the maximum gain direction, which is given (in dBm) by:

$$\text{EIRP} = P_{\text{in}} + G_{\text{t}} = P_{\text{SA}} + L_0 + L_{\text{r}} - G_{\text{r}} + A_{\text{atten}}. \tag{5.4}$$

The results are compared with other SoAs in Table 5.3. There is a 2-2.5 dB difference between the simulated and measured EIRP, which includes both antenna gain and system loss variation. Comparing to other SoAs in the literature, the SoA demonstrated here achieves much higher EIRP at similar frequencies. Moreover, it is the only SoA that integrates a bare die. The results shown here can be improved with specific design modifications. Using a VCO die instead of a pre-packaged MMCI and smaller SMCs can reduce the package area, which allows for reducing the distance between the amplifier and the antenna feed. This RF path contributes the most to insertion loss. It would also give more flexibility with the location of antenna feed relative to the start of the tapered slot, which can be changed to increase antenna gain and minimize the feed coupling loss.



(a)



(b)

Figure 5.18: (a) Diagram of the measurement setup for the SoA, with the parameters used for power calculations, and (b) measured P_{SA} vs. frequency, for different VCO tuning voltages.

Table 5.3: Comparison of State-of-the-Art SoAs

Ref.	**Circuity/Package Fabrication**	**Antenna Fabrication**	**EIRP (dBm)**
This work	**AJP**[†]	**Conventional**	**25.9 (12.5 GHz), 28.2 (13.2 GHz), 26.7 (13.7 GHz)**
Gjokaj *et al.* [136]	Conventional + AJP[§]	3D Printing + Metalization[‡]	20.8 (14.8 GHz)[*]
Oakley *et al.* [137]	Conventional + AJP[¶]	3D Printing + Metalization[‡]	18.7 (12 GHz)[*]
He *et al.* [76]	IJP	3D Printing + Metalization[‖]	17.2 (14.7 GHz)[*], 17.5 (15.3 GHz)[*]

[†] AJP for all dielectrics and conductive paths,
[§] conductive paths, and [¶] die pasivation layer and conductive paths;
[‡] seed layer via electroless plating, followed by electroplating; [‖] seed layer sputtering, followed by electroplating; [*] calculated for comparison;

5.3 Conclusion

This chapter addresses some of the deficiencies in previously demonstrated SiP/SoP strategies by showing flexible, mm-wave-capable packaging strategies via AJP. These strategies showed RF performance comparable to, or better than, other strategies in the literature, and additionally address problems they faced, such as adhesion problems in the die-dielectric interface. The best-performing strategy was utilized for system integration by realizing a SoA transmitter module, with the package aerosol jet-printed on the antenna. What remains to be shown in this dissertation is the adaptation of this SiP/SoP strategy to operate at high RF power and incorporate diamond platforms for high-power/temperature operation.

CHAPTER 6

A HIGH-POWER-CAPABLE CHIP-FIRST PACKAGE ON DIAMOND

Chapter 2 demonstrated basic high-power RF structures on diamond to show its high-power capabilities and its potential as a semiconductor platform for integration into SiP/SoP strategies as tool for effective thermal management. Chapter 3 showed the basic compatibility of diamond and AJP by means of basic RF components printed on diamond. Chapter 5 demonstrated a complete SiP/SoP strategy via AJP, as well as its use for system integration by means of a SoA. This chapter completes this dissertation by combining elements of all chapters to show a mm-wave package on diamond that can support high RF power.

I demonstrate a chip-first package on diamond fabricated fully via AJP. The packaging strategy followed here was first demonstrated in Chapter 5 [7] and delivers a package consisting of a multi-level dielectric substrate structure, with a PI wall printed around the die, followed by printing of BCB to cover the area between die and PI. The RF interconnects are supported by BCB and the PI wall and extend to MS TLs supported by PI. The launches are GCPW TLs that transition to MS TLs through via-less transitions as in Chapter 5. This package shows improved RF performance comparing to the packages shown in Chapter 5 and additionally extends the highest frequency from 50 to 67 GHz. It also demonstrates better RF performance than other additively manufactured packages and interconnects in the literature. Finally, I show high-power measurements performed on the package via active L-P, following the same method as for the high-power SBDs on diamond in Chapter 2. The maximum achieved output RF power is 1.95 W at 6 GHz. The work presented in this chapter is the last part of this dissertation, and shows the potential of application-specific and flexible packaging methodologies, fully realized via AJP, for system integration at mm-wave that can accommodate high-power applications.

6.1 Design

The package design follows the fundamentals of the chip-first PI wall approach demonstrated in Chapter 5 [7], with minor differences. I chose the KAT-0-DG+ 0-dB attenuator (Mini-Circuits) [129] as the package die. As in Chapter 5, the entire package was designed with respect to the die, which was placed first. The designed package consists of a multi-level dielectric structure, with a PI wall around the die and BCB filling the area between the PI wall and the die. The RF interconnects are supported by the BCB and the PI wall, and they extend to MS TLs on PI. Finally, the MS TLs transition to GCPW launches through via-less transitions as in [107].

This design, unlike the design in Chapter 5, includes a designed BCB/Ag die attach pad. The designed pad consists of discrete BCB lines surrounded by Ag. BCB is meant to act as the adhesion layer between the die bottom and the ground plane, holding the die in place, while the Ag ensures an electrical connection between the two. Another design difference with the package in Chapter 5 is that, instead of PI, BCB is used on the die edge as a layer that deters unwanted diode effects. Printing BCB over the die edge further reduces the risk of dielectric delamination from the die, as discussed in Chapter 5, since there is no die-PI interface in this design. Finally, this design utilizes frequency-agile shaped interconnects, as in Chapter 5, but improved to be shaped continuously over all of the varying dielectric thicknesses and from one dielectric to another, without abrupt changes in width. This contributes to an improved RF performance, as will be discussed later. All interconnects and TLs were designed and optimized in ANSYS HFSS©. A cross-sectional view of the packaging strategy is shown in Fig. 6.1, and details of the designed package are shown in Fig. 6.2.

6.2 Fabrication

The first step of the fabrication process is the development of the ground plane on the diamond surface. The wafer used was a TM200 CVD diamond wafer (Element Six). Before the deposition of the ground metal, I needed to take steps for its adhesion on the diamond surface. First, a 20-nm layer of Cr was sputtered on the surface. Then, 2 μm of Cu were sputtered to act as the ground

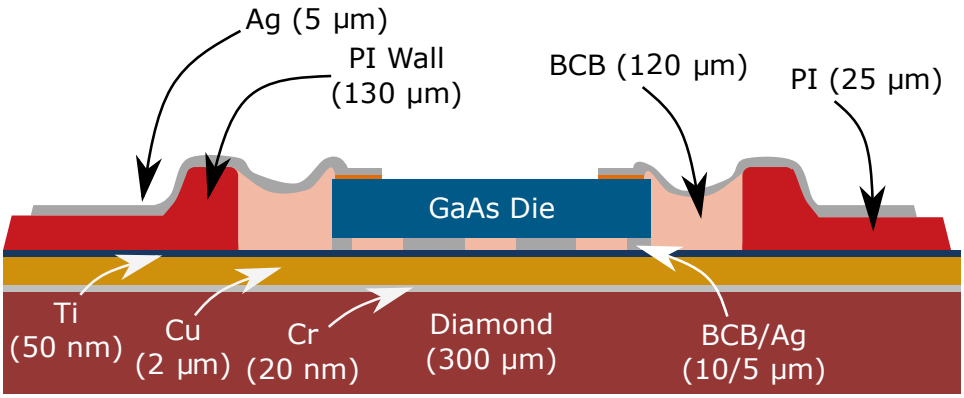


Figure 6.1: Cross-sectional view of the chip-first packaging strategy on diamond, with annotated target thicknesses.

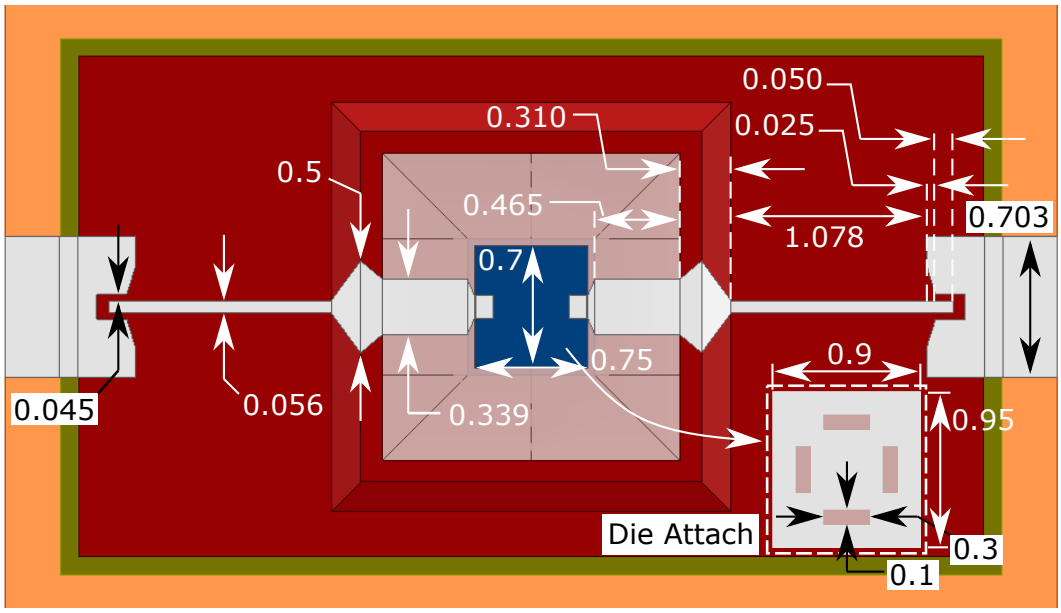


Figure 6.2: Overview of the designed package, with annotated dimensions in mm.

plane, followed by 50 nm of Ti to avert oxidation of the Cu. All sputtering was done with help from Brian Wright at MSU.

All following steps included material deposition via AJP only. All printed was done using an Optomec 5X Aerosol Jet Printer [116]. The first part of the package to be printed was the BCB/Ag die attach. 10 μm of BCB were printed first, followed by 5 μm of Ag. Then, the die was placed on the die attach pad and underwent two phases of thermal curing. The first phase, at 250 °C for 2 h in N_2, is for die attach reflow, during which the BCB flows so that the die bottom metal comes in contact with the printed Ag. The second phase, at 180 °C for 5 h in atmosphere, is to sinter the printed Ag. The sputtered Ti on the Cu ground deters the Cu from oxidizing during the latter phase.

The remaining fabrication follows the steps demonstrated in Chapter 5 for the chip-first strategy following the PI wall approach [7]. Before printing PI, I applied the VM651 adhesion promoter (HD Microsystems). I then printed initial PI layers for a total thickness of 5 μm, and the first PI wall layers for a top height of 10 μm. I then did a soft bake of these layers at 200 °C for 2 min in N_2. Consecutively, I printed another 20 μm of PI for a total thickness of 25 μm, and the remaining PI wall for a top height of 130 μm. All PI was then cured at 295 °C for 1 h in N_2, for full imidization of the PI. The next material to be printed was the BCB. Before that, I applied the AP2000 adhesion promoter (Dow Chemicals). Then, I printed 120 μm of BCB to fill the area between the die and the PI wall. This was followed by a hard cure for the BCB at 250 °C for 2 h in N_2. The final step in the manufacturing process was printing Ag ink for TLs and die interconnects. Ag ink was printed with a target thickness of 6 μm and then sintered in atmosphere at 180 °C for 5 h. As in previous chapters, the PI ink I used was composed of PI-2611 polyamic acid (HD Microsystems [131]) diluted to 40 vol.% PI-2611 + N-Methyl-2-Pyrrolidone (NMP) (Sigma Aldrich), the BCB ink was the Cyclotene 3022-35 resin (Dow Chemicals), and the Ag ink consisted of 25 wt.% Clariant Prelect TPS 50 + DI water. A fully fabricated package on diamond is shown in Fig 6.3. Details of the interconnects are shown in Fig. 6.4, with pictures taken with an Olympus BX41M microscope. As in Chapter 5, the interconnects demonstrate good quality, without any discontinuities in the

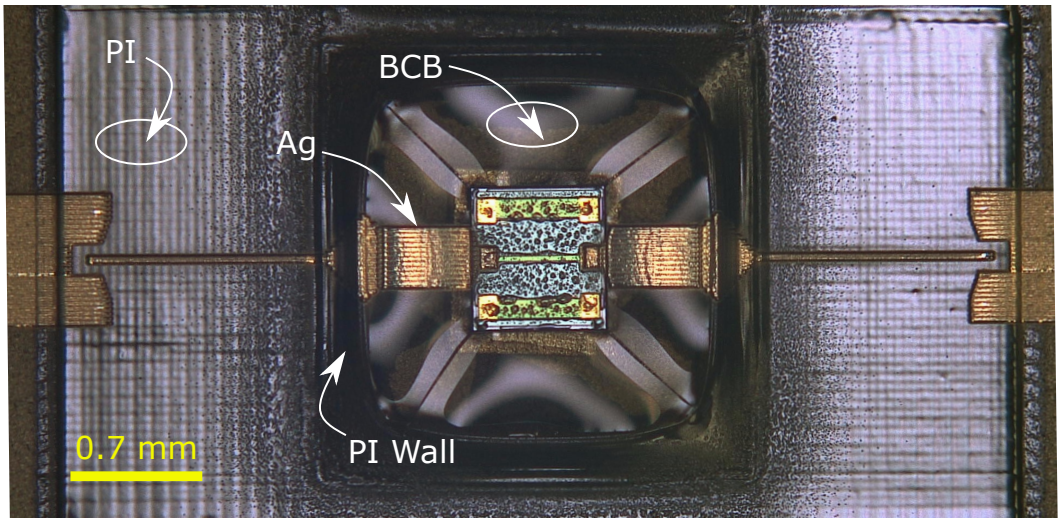


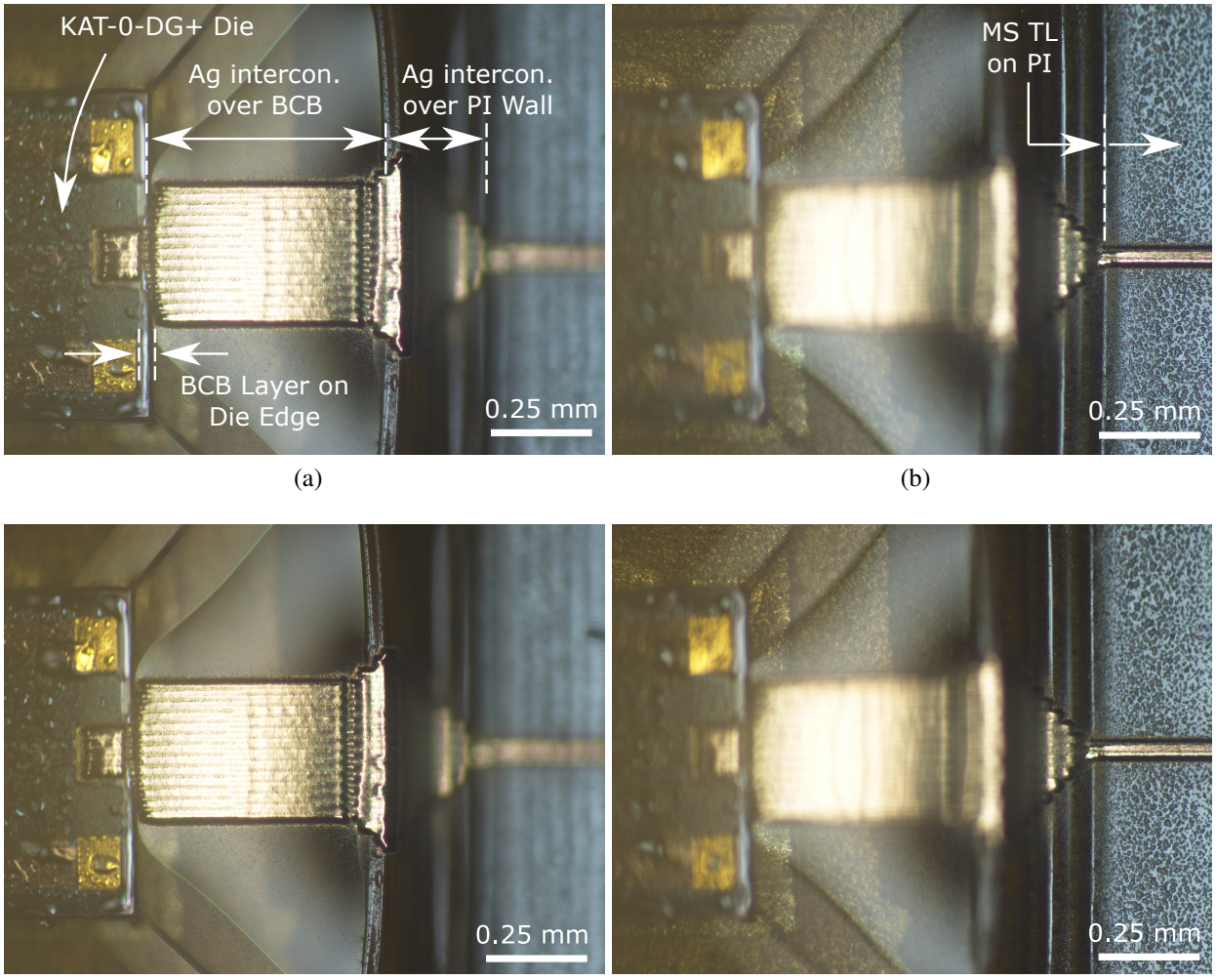
Figure 6.3: Close-up view of the fabricated package.

die-BCB or BCB-PI interface. I also show the interconnects after the high-power measurements discussed later in this chapter, demonstrating that these interconnects were not affected visually by the RF power close to 2 W. Details of the printing steps followed for the fabrication of this packages are given in Appendix C, while details of the curing profiles are given in Appendix B.

6.3 Results

I first measured the surface profiles of the cured dielectrics and sintered Ag using a NanoMap-500LS surface profilometer. I found the PI thickness to be $\sim$ 25 µm and the top PI height to be 128 µm. The BCB fill adhered well on the die and the PI wall, with a maximum thickness of 120 µm. The Ag had a thickness of 7 µm. Prior to printing Ag, the measured dielectric thicknesses were taken into account to optimize the TLs and interconnects. After printing Ag, all measured thicknesses were taken into account for the final simulation.

I took small-signal RF measurements from 50 MHz to 67 GHz using an MPI TS150-THZ probe system, a Keysight N5227 PNA, and a pair of GGB 67A-GSG-250-P picoprobes. A LRRM calibration was performed using a GGB CS-9 calibration substrate to bring the measurement reference planes to the tips of the probes. I measured the fabricated package on diamond and an unpackaged die. In addition to the performance of the entire package, the performance of the TLs



(a) (b)

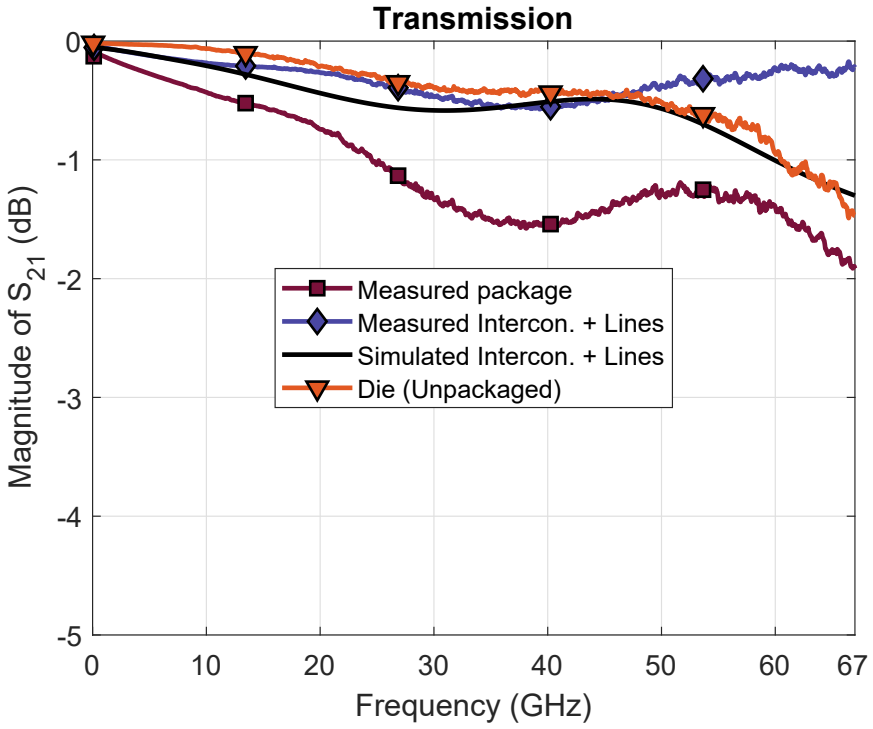
(c) (d)

Figure 6.4: Microscopic 10× magnified photographs of the interconnect section of a fabricated package, with focus on the die area (left) and the MS TL on PI (right): (a), (b) before and (c), (d) after high-power measurements.

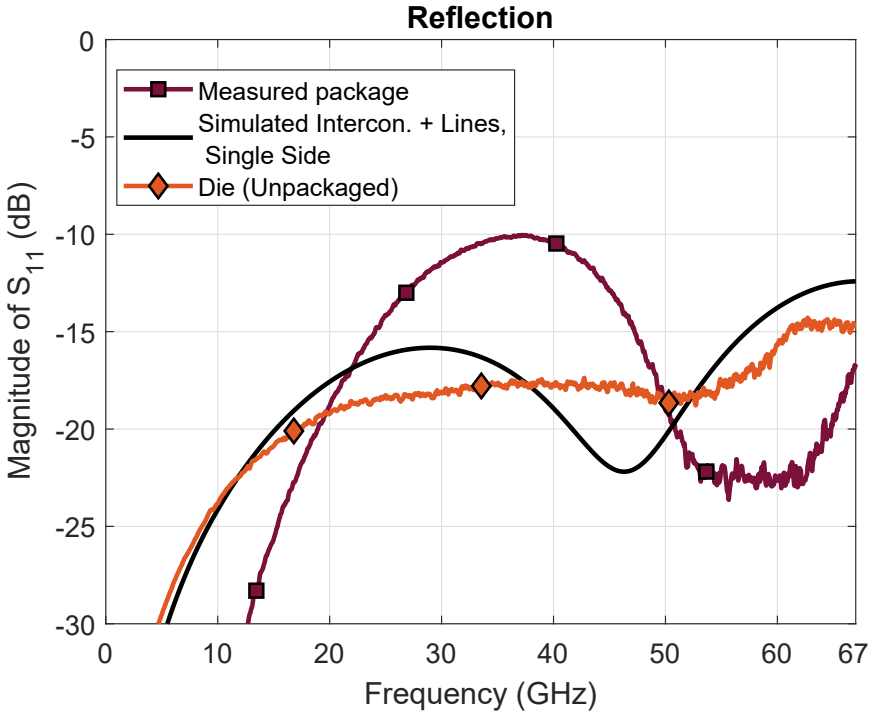
and interconnects alone is calculated as in Chapter 5 via Eq. 5.3 by removing the effect of the attenuator die. Measured and simulated transmission and reflection coefficients are shown in Fig. 6.5a and 6.5b, respectively. Normalized measured and simulated performance of the interconnects and TLs alone is shown in 6.6. Overall, the package demonstrates low loss at the entire range from 50 MHz to 67 GHz, with a worst-case loss for interconnects and TLs of 0.56 dB at around 40 GHz, while S_{11} for the package is maintained below -10 dB. The normalized loss for interconnects and TLs is at worst 0.28 dB/mm at 40 GHz, achieving 0.11 dB/mm at 67 GHz.

The interconnects demonstrated here perform better than the ones demonstrated in Chapter 5 [7]. Loss at the same frequencies is lower, and additionally this chapter extends the highest frequency from 50 to 67 GHz. As discussed earlier in this chapter, the improved performance is partially due to the modified shaped interconnects design, which are shaped continuously without abrupt changes in width. Moreover, the PI wall and BCB in this package were designed thicker, thus the MS TLs in these areas were designed wider, contributing to lower attenuation due to conductor loss. The interconnects of the package in this chapter also perform better than other interconnects presented in the literature. The interconnects and TLs in [66] show similar loss up to 50 GHz, but higher loss above that. Comparing to [66], an additional advantage of my approach, as discussed in Chapter 5, is that it addresses adhesion problems on the die-dielectric interface by replacing PI with BCB for the area surrounding the die and employing PI for the PI wall and for supporting the TLs. Performance comparison with other packages and interconnects in the literature is shown in Table 6.1.

After small-signal measurements, I took high-power RF measurements via active L-P. I used a pair of GGB 40A-GSG-250-P picoprobes and a Maury MT2000 Active L/S-P System, as in Chapter 2. I performed a line-reflect-match (LRM) calibration via the MT2000 software using a GGB CS-5 calibration substrate, bringing the measurement reference planes to the probe tips. As discussed in Chapter 2, the MT2000 tunes the reflection coefficients on the source and load (input and output) sides, Γ_x, where $x = \{\mathrm{S}, \mathrm{L}\}$, by injecting arbitrary RF signals into the measured device to find the optimal Γ_S and Γ_L to maximize the power delivered to the load, $\mathrm{P_L}$ (i.e., output power,



(a)



(b)

Figure 6.5: Measured and simulated (a) transmission, and (b) reflection S-parameters of the fabricated package on diamond and an unpackaged 0-dB attenuator die.

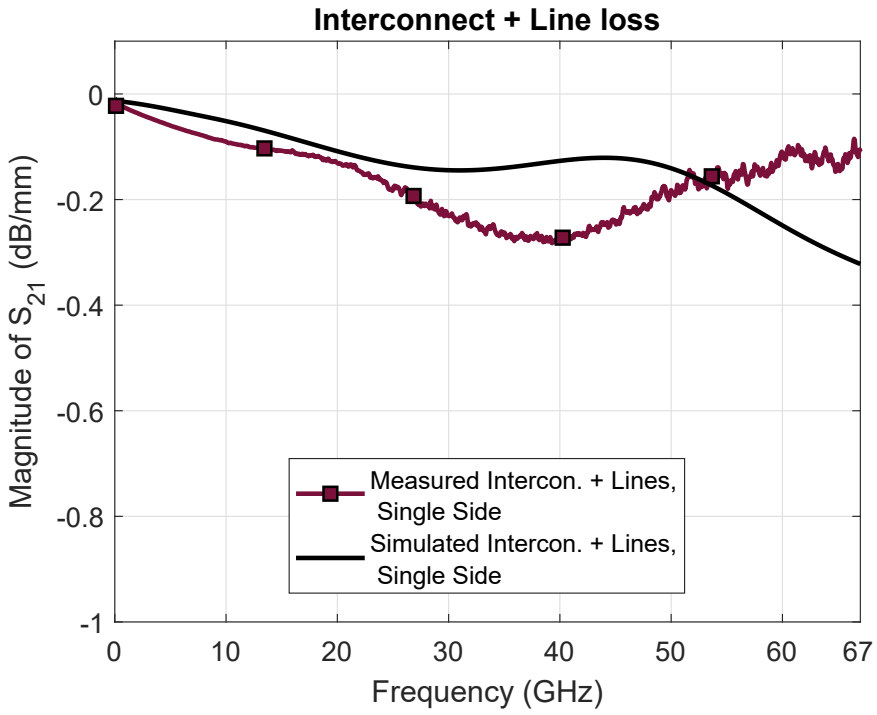


Figure 6.6: Measured and simulated interconnect and line loss.

P_{out}). Following the measurement approach described in Chapter 2, I performed L-P using CW signals with an input power of P_{in} = 33 dBm at 6, 10, and 18 GHz. The results are shown in Fig. 6.7. A P_{out} of 32.9 is achieved at 6 GHz, yielding 0.1 dB loss under optimal matching conditions. At 10 and 18 GHz, a P_{out} of 32.5 and 32.7 dBm, respectively, is achieved. The achieved P_{out} in this work is orders of magnitude higher than previously published packages or interconnects fabricated fully via AM. To the best of my knowledge, the highest P_{out}, other than the ones presented here, for a fully additively manufactured package was shown by Craton *et al.* in [72] at 0.16 W at 9 GHz. The lowest P_{out} shown here is 1.78 W at 10 GHz, and the highest is 1.95 W at 6 GHz. There are examples of conventionally manufactured packages that have achieved higher P_{out}. Pavlidis *et al.* in [138] showed a GaN high-power amplifier packaged on an organic substrate using conventional methods and achieved a P_{out} = 5.4 W. Nevertheless, this package does not offer all the advantages that SiP/SoP strategies via AM, and particularly entirely via AJP, afford. The same applies for [70], which achieved similar P_{out} levels as the package I showed, but employs AJP alongside conventional methods and pre-manufactured substrates, as in [69, 71]. Moreover, the approach

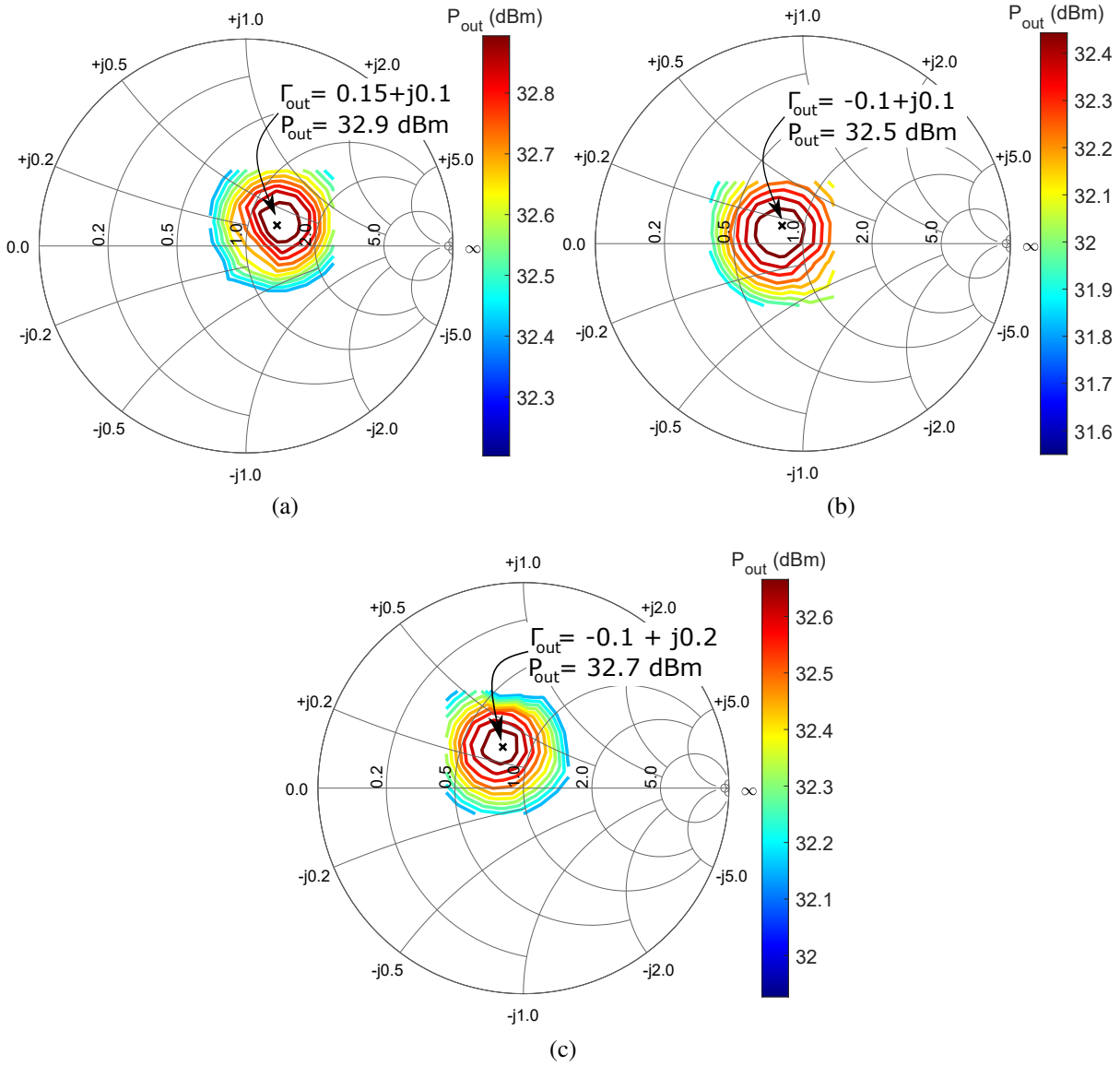


Figure 6.7: Load-pull measurements for the package on diamond, all with P_{in} = 33 dBm, at (a) 6 GHz, (b) 10 GHz, and (c) 18 GHz.

shown here was limited by the intrinsic upper power levels of the attenuator die, at 2 W, whereas the die in [138] has a saturated power rating of 5.4 W. Using dies with power ratings > 2 W in the AJP-enabled approach shown here can potentially yield higher P_{out} levels. Furthermore, high-power performance can be demonstrated up to 67 GHz for this package, provided that external amplifiers at the required frequencies are available for the L/S-P system setup (see Appendix A). A comparison of my package with other packages, in terms of P_{out}, is shown in Table 6.1, along with the small-signal RF performance that was discussed earlier.

As mentioned in Section 6.2, the printed interconnects were able to withstand the RF power levels achieved and did not show any signs of degradation or damage. It is important to note that several measurements were taken while applying a 33-dBm CW signal at the input due to the sequence of steps to achieve the maximum P_{out}. I first did L-P to optimize Γ_L, then S-P for the optimal Γ_S, and then L-P again for optimal Γ_L. This process was done at the three measurement frequencies separately, and the interconnects were unaffected by all these measurements, as shown in Fig. 6.4. Finally, as mentioned above, I did not reach the upper power limits of the interconnects, as I limited the applied RF power to 2 W which is the rated power for the KAT-0-DG+ die. Thus, a die with higher power rating could be used in future work to test the upper breakdown limits of the interconnects.

The purpose of the package shown in this chapter was to demonstrate that the SiP/SoP strategy employed can realize fully additively manufactured packages for system integration that are capable of handling high RF power, and to show that diamond platforms, having great thermal capabilities, can be successfully integrated into the strategy without fabrication challenges and used as heatsinks. However, I did not focus on the die attach and its impact on the heat dissipation, and I did not perform thermal simulations. The fully aerosol jet-printed die attach used here provided adequate adhesion for the die on the diamond wafer and an electrical connection to the ground. Since good mm-wave performance and high RF power was demonstrated here, along with the successful integration of diamond into the strategy, future work can focus on the die attach, including design and material choice, for optimal thermal and electrical conductivity.

Table 6.1: Comparison of State-of-the-Art Packages and Interconnects

Ref.	Fabrication Process	Packaging Application	Intercon. + Line Loss (dB/mm)	P_{out} (dBm)
This Work	**AJP**	**Intercon. on GaAs**	**0.13 (20 GHz), 0.19 (50 GHz), 0.11 (60 GHz)**	**32.9 (6 GHz), 32.5 (10 GHz), 32.7 (18 GHz)**
Konstantinou *et al.* [7]	AJP	Intercon. on GaAs*	0.13 (20 GHz)#, 0.26 (50 GHz)#	N/A
		Intercon. on GaAs†	0.19 (20 GHz)#, 0.74 (50 GHz)#	N/A
Craton *et al.* [66]	AJP	Intercon. on GaAs	0.16 (20 GHz)‖‡, 0.32 (50 GHz)‖‡, 0.38 (60 GHz)‖‡	N/A
Craton *et al.* [72]	AJP	Intercon. on GaAs	0.33 (15 GHz)	21.9 (9 GHz)
Craton *et al.* [75]	AJP	AM SoP (3×GaAs)	0.6 (78 GHz)	N/A
Craton *et al.* [74]	AJP	AM SoP (GaAs)	0.37 (85 GHz)	N/A
Tehrani *et al.* [65]	IJP	Intercon. on GaAs†	0.45 (24.5 GHz)	N/A
		Intercon. on GaAs§	0.57 (24.5 GHz)¶	4.2 (24.5 GHz)
Ihle *et al.* [68]	AJP on LTCC, MD	Intercon. on GaAs	0.24 (20 GHz)‡, 0.4 (50 GHz)‡	N/A
Ramirez *et al.* [67]	FDM, MD, LMM	Intercon. on GaAs	0.2 (20 GHz)	N/A
Oakley *et al.* [69]	AJP on LCP, conventional	Intercon. on GaAs and GaN	0.13 (20 GHz)‡, 0.42 (40 GHz)‡	N/A
Spain *et al.* [70]	AJP on LCP, conventional	Intercon. on GaAs	N/A	33 (14 GHz)
Pavlidis *et al.* [138]	Conventional on organic	Power amp. package	N/A	37.3 (10.2 GHz)

* 3-dB attenuator die; † 0-dB attenuator die; # avg. loss of two packages; ‖ best-case loss; ‡ approximated for comparison; § LNA die; ¶ measured at low-loss point.

6.4 Conclusion

This chapter demonstrated the first integration of diamond platforms into AM-enabled SiP/SoP strategies. A chip-first package was manufactured fully via AJP on a diamond wafer, incorporating an attenuator bare die. The SiP/SoP strategy used here utilizes the multi-dielectric packaging approach shown in Chapter 5, with printed PI and BCB dielectric inks along with Ag nanoparticle conductive ink. This package demonstrates three accomplishments. First, it shows RF performance better than the packages shown in Chapter 5, but also extends the frequency of use from 50 to 67 GHz. It also achieves better performance than other additively manufactured packages and interconnects in the same frequency range. Second, this package is the first entirely additively manufactured package to demonstrate high-power performance, with a maximum P_{out} = 1.95 W. Finally, this package is the first to demonstrate a basic, successful integration of diamond in an AM-enabled SiP/SoP strategy. These accomplishments show the potential to deliver flexible, application-specific SiP/SoP strategies aiming for higher functional density that can be used in high-power applications.

CHAPTER 7

CONCLUSION AND FUTURE WORK

This dissertation expands on the current state of the art in SiP/SoP packaging towards strategies realized fully via AJP for microwave and mm-wave system integration. The newly shown strategies build on previously demonstrated strategies via AJP and other AM methods and additionally address many of their limitations. The final strategy presented here demonstrates improved RF performance at mm-wave, comparing to previously shown strategies, and is additionally compatible with high power. Also, this strategy successfully integrates diamond platforms to act as heatsinks during high-power operation.

I first discussed the state of the art in packaging for system integration in Chapter 1, where I presented the major conventional SiP/SoP methodologies, as well as the ones via AM that have been demonstrated as alternatives. I also discussed some of the deficiencies in recent work on packaging strategies via AM, such as the absence of interconnects on non-planar surfaces and of high-power packages. Diamond was investigated as a semiconductor platform for high-power and temperature applications in Chapter 2 via the demonstration of basic high-power RF structures on diamond, such as SBDs. Then, in Chapter 3, I investigated the basic compatibility of diamond and AJP by demonstrating mm-wave RF components printed on diamond dielectric substrates. In Chapter 4, I demonstrated fully aerosol jet-printed components on non-planar surfaces for mm-wave, and at near-THz frequencies, as well as highly compact resonant mm-wave structures. Chapter 5 laid out SiP/SoP strategies via AJP for mm-wave frequencies, as well as its use for system integration in the case of a microwave SoA transmitter module. Finally, in Chapter 6, I improved these strategies to yield better mm-wave performance, as well as adapted it to incorporate diamond platforms as heatsinks and to be capable of high-power operation. This dissertation demonstrates that complete SiP/SoP strategies for system integration in a variety of applications, at mm-wave and beyond, are achievable fully via AJP, including on complex, non-planar structures and for high-power applications.

The work demonstrated in this dissertation can be continued using the fundamentals laid out for the fully aerosol jet-printed components and packages. First, following similar design and fabrication methods shown for the fully aerosol jet-printed TLs and stubs at near-THz in Section 4.3, other components can be realized, such as filters, couplers, and antennas. With regards to the complete SiP/SoP strategy demonstrated in Section 5.1 and further used in Section 5.2 and Chapter 6, it can be used in different concepts. First, its performance in the W-band and at near-THz frequencies can be investigated. Furthermore, since basic TLs were demonstrated on non-planar surfaces in Section 4.2, packaging of dies on such surfaces using the AJP-enabled SiP/SoP strategy from Section 5.1 can be pursued. Finally, application-specific modules realized entirely, or almost entirely, with AM, such as the RF front end transceiver module on-antenna discussed in Chapter 1 and shown in Fig. 1.4, could be a potential extension of the work shown in this dissertation.

APPENDICES

APPENDIX A

ACTIVE LOAD-PULL FOR POWER AND LINEARITY

This appendix focuses on the use of active L-P for power and linearity optimization. I demonstrate active L/S-P measurements performed on a pre-packaged GaN HEMT. The measurements were taken using single-tone (1-tone), two-tone (2-tone), and modulated (128-QAM) signals at 2 GHz. A test fixture with a 6 W COTS GaN HEMT was used as the device-under-test (DUT). Linearity was optimized by minimizing IM3 and ACPR. Furthermore, a comparison of the optimized power delivered to the load (P_L) between 1-tone and 128-QAM is shown. The results shown here demonstrate that the impedance matching conditions for power or linearity optimization can be reliably predicted via active L-P using modulated signals. Moreover, there are considerable differences between 1-tone and the modulated signals in the P_L contours and optimal P_L impedance matching conditions. These ascertainments could impact power amplifier design depending on the power and linearity specification trade-offs.

A.1 HEMT Test Fixture Design and Fabrication

Given the additional complications of on-wafer probe testing at 5G [139], I focus on a packaged transistor to isolate the effects of modulated waveforms from other testing complexities. The design parameters of the test fixture illustrated in Fig. A.2 are summarized in Table A.1. An R-C network was used at the gate of the GaN HEMT (T_1) to provide stability. All component values were chosen to optimize the trade-off between unconditional stability and power gain. In order to maintain a safe T_1 temperature and avoid self-heating effects that would lead to an input reflection coefficient shift and dynamic input mismatch, an aluminum heat sink was used. T_1 was soldered onto a copper sheet that was thereupon attached to the heat sink.

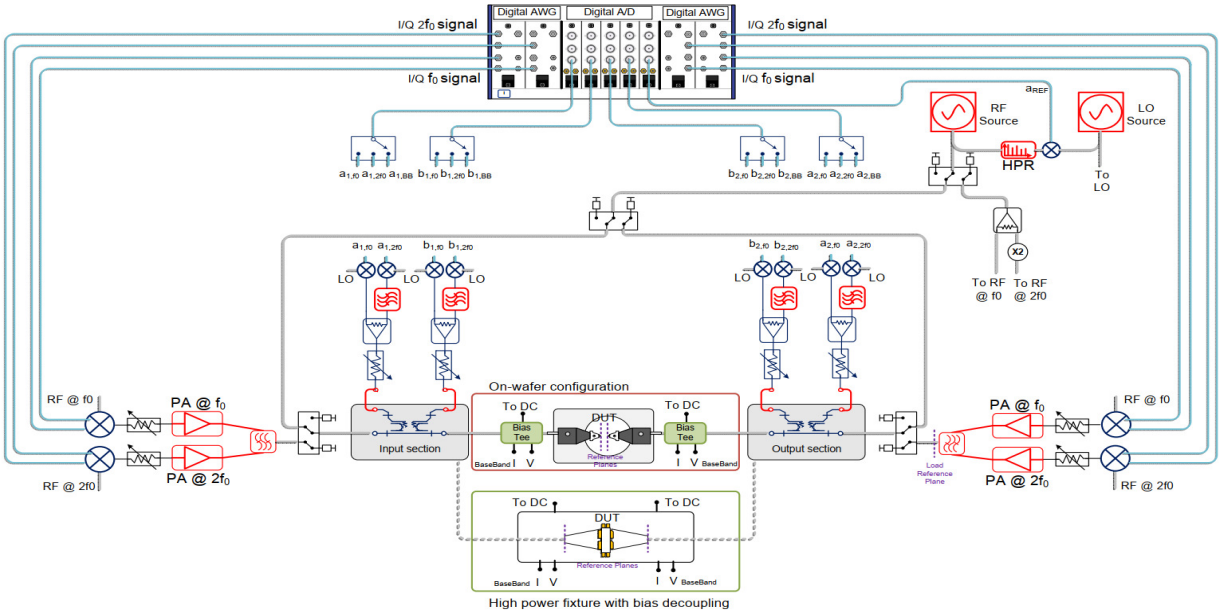


Figure A.1: Simplified block diagram of the MT2000 Mixed-Signal Active L-P System [8]. In this configuration example, external amplifiers are used both on the source and load side (DUT input and output, respectively) to tune Γ at f_0 and $2f_0$. In this work, measurements are taken only at f_0, hence only one amplifier is used per side. From [9] ©2020 IEEE.

A.2 Measurement Setup and Approach

As in Chapters 2 and 6, active L/S-P for this appendix was done using the MT2000 Mixed-Signal Active L-P System. The MT2000, shown in Fig. A.1, uses an open-loop architecture to tune Γ_x, where $x = \{\mathrm{S}, \mathrm{L}\}$, on the source and load side (at the DUT input and output, respectively), by directly injecting arbitrary signals into the DUT. Γ_x represents the ratio of power waves, b_x/a_x, with a_x being the incident and b_x being the DUT-generated power wave, respectively. The a_x- and b_x-waves, and thereby Γ_x, are controlled via software iterations. When the DUT is excited with a modulated signal a_S, it generates signals b_S and b_L. By measuring all a_x- and b_x-waves, the system estimates the waves that need to be injected to the DUT at each iteration to achieve the desired Γ_S and Γ_L. The injected a_x-waves are generated by wideband baseband arbitrary waveform generators (AWG) and up-converted using in-phase/quadrature (I/Q) modulators. The acquired DUT-generated signals are down-converted to an IF frequency and then sampled with wideband A/D converters [96]. The measurements were taken using 1-tone, 2-tone, and 128-QAM

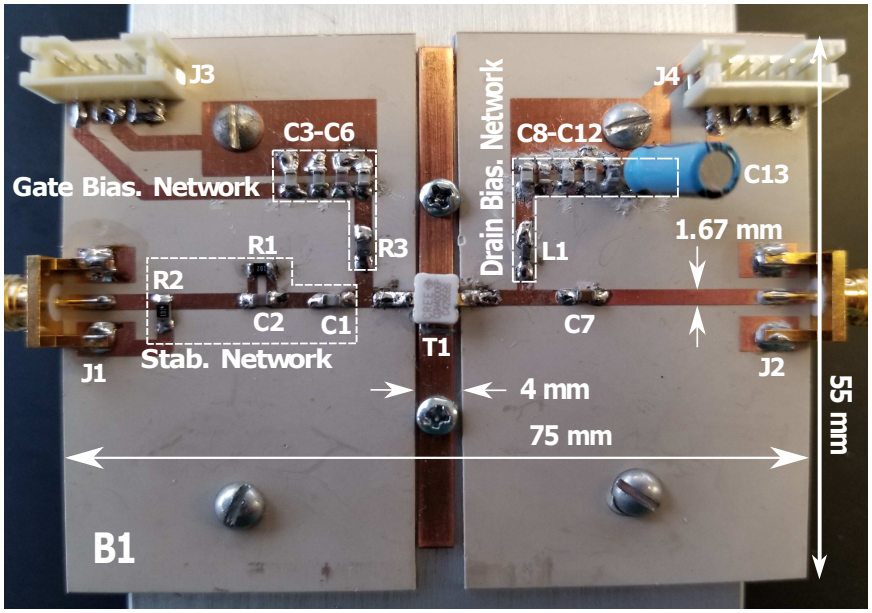


Figure A.2: The in-house fabricated HEMT test fixture. From [9] ©2020 IEEE.

Table A.1: Summary of the test fixture design parameters

Ref.	**Corresponding Values/Parameters/Description**
T_1	CREE CGH40006P
B_1	RT/duroid 6035HTC, 0.032”, 35 µm copper cladding
C_1, C_2, C_7	1.3 pF, 6 pF, 330 pF
C_3-C_6	330 pF, 450 pF, 1 µF, 10 µF
C_8-C_{12}	100 pF, 330 pF, 450 pF, 1 µF, 10 µF
C_{13}	33 µF
R_1, R_2, R_3	200 Ω, 300 Ω, 50 Ω
L_1	2.2 µH
J_1, J_2	CONN SMA EDGE MNT
J_3, J_4	CONN HEADER SMD

From [9] ©2020 IEEE.

continuous-wave (CW) signals at $f_0 = 2$ GHz. Different levels of available source power (P_{avs}) were applied to investigate the differences in P_L, IM3, and ACPR contours with respect to a changing drive. Every contour line encloses load impedance (Z_L) points that correspond to a specific attained parameter (P_L, IM3, or ACPR) value, or better (larger in absolute value). The optimal Z_L for the corresponding parameter is located around the center of each contour family and is indicated by P_i on the Smith Chart. For IM3 and ACPR, the measurements were taken in two adjacent frequency channels below and above the signal bandwidth. IM3 and ACPR were measured using a 2-tone and a 128-QAM input signal, respectively. The 2-tone signal was chosen to have a tone spacing of 50 MHz, while the 128-QAM signal was chosen with a PAPR of 7 dB, a symbol rate of 65 Msym/sec, a roll-off factor of 0.22, square root raised-cosine pulses, and a bandwidth of 80 MHz.

An SOLT calibration was performed to bring the reference planes to the inputs of J_1 and J_2. In order to accurately measure IM3 and ACPR, the MT2000 source signal pre-distortion feature was used to reduce the distortion of the actual source signal with respect to the ideal source signal by extracting the distortion caused by the two external amplifiers. T_1 was biased with $V_{GS} = -2.74$ V and $V_{DS} = 28$ V, maintaining $I_{DS} = 100$ mA and $I_{GS} = 0$. To locate the 1 dB compression point (P_{1dB}), a 1-tone P_{avs} sweep was performed, showing that P_{1dB} occurs for $P_{avs} = 32$ dBm. The 128-QAM signal has a PAPR of 7 dB, which needs to be taken into account during the L-P measurements. While the 128-QAM signal gets amplified as P_{avs} approaches P_{1dB}, T_1 is driven to saturation, causing the gain and P_L of the DUT to be confined due to nonlinearity. Hence, to ensure a fair comparison between 1-tone and 128-QAM signal amplifications, a careful choice of P_{avs} needed to be made to exhibit high-power operation while avoiding nonlinearity. In my comparison, I allow P_{avs} = 28 dBm. Finally, for all L-P measurements, the source impedance, Z_S, was set to 50 Ω, thus there was mismatch and a considerable reflection at the input and the power at the T_1 input is lower than P_{avs}.

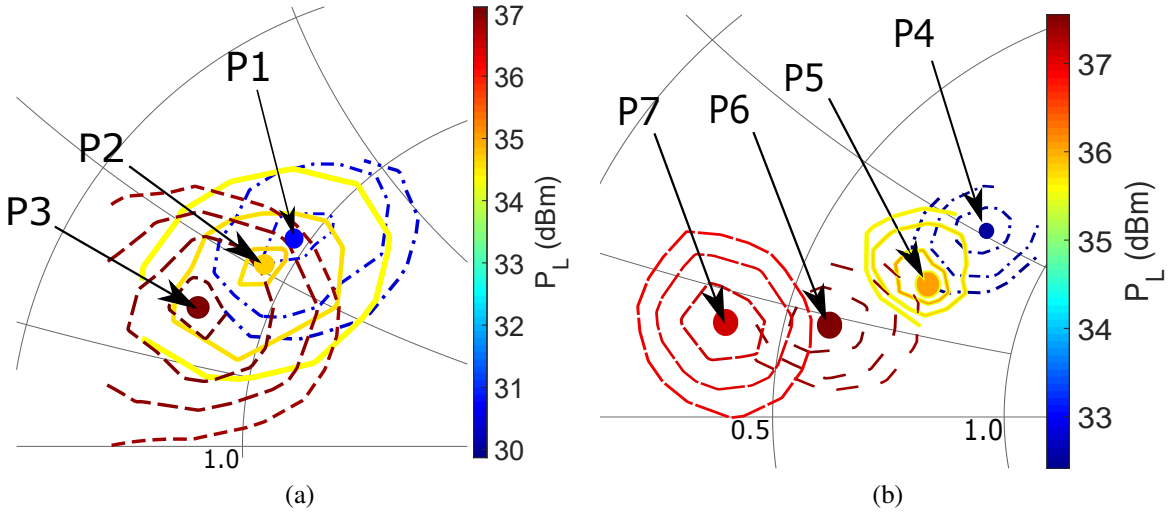


Figure A.3: P_L contours, with increasing P_{avs}, for the: (a) 1-tone signal, (b) 128-QAM signal. Every contour family, indicated by a different line type, corresponds to a different P_{avs} level. From [9] ©2020 IEEE.

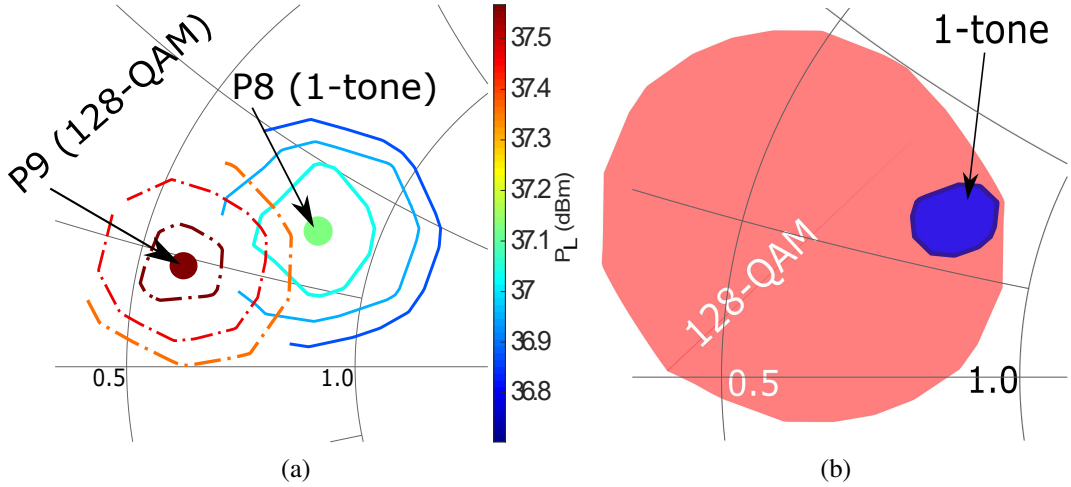
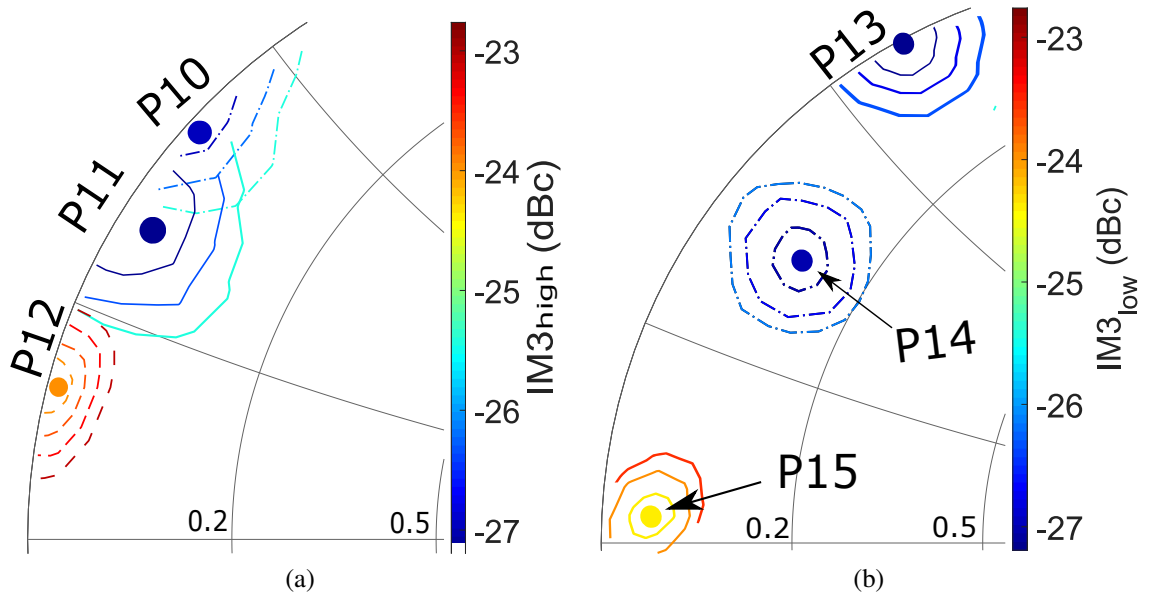
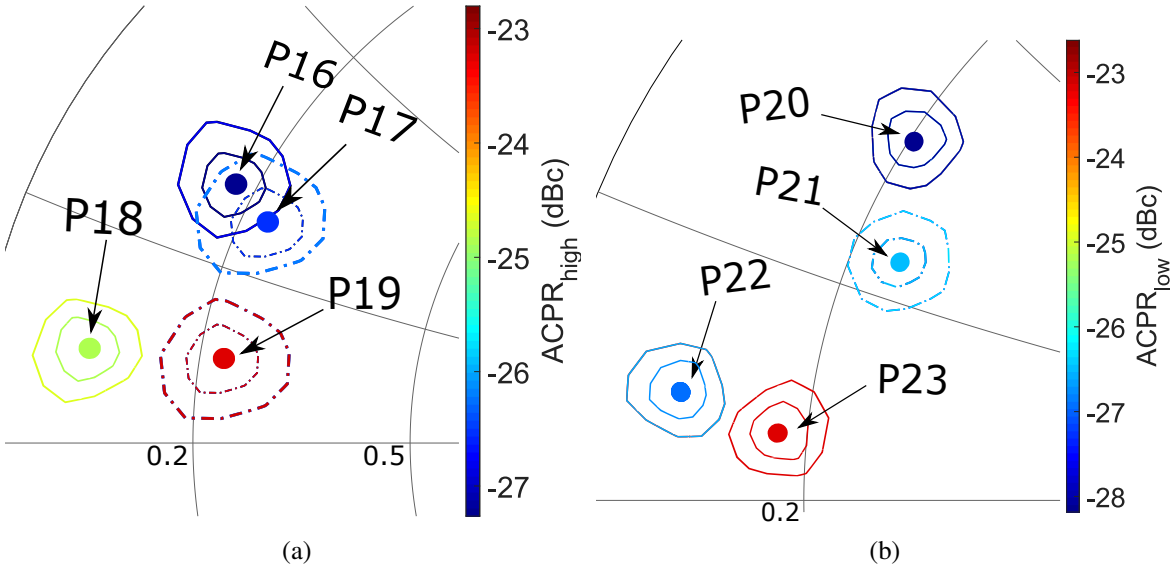


Figure A.4: P_L comparison of 1-tone and 128-QAM for a constant $P_{avs} = 28$ dBm: (a) P_L contours, with every contour family, indicated by a different line type, corresponding to a different signal waveform, (b) isolated contours for $P_L \simeq 37$ dBm. From [9] ©2020 IEEE.



(a) (b)

Figure A.5: IM3 contours, with increasing P_{avs}, for: (a) $IM3_{high}$, (b) $IM3_{low}$. From [9] ©2020 IEEE.



(a) (b)

Figure A.6: ACPR contours, with increasing P_{avs}, for: (a) $ACPR_{high}$, (b) $ACPR_{low}$. From [9] ©2020 IEEE.

A.3 Active L-P Measurements

The measurements for all optimal load impedances are summarized in Table A.2. The P_L contours for 1-tone and 128-QAM are shown in Fig. A.3, with a peak P_L of 37.2 and 37.7 dBm attained, respectively, for P_{avs} = 28 dBm. The effects of nonlinearity on high-PAPR signals near the saturation region can be seen on the 128-QAM contours, since increasing P_{avs} from 28 to 32 dBm results in a decreased P_L.

Furthermore, a comparison of 1-tone and 128-QAM P_L performance for P_{avs} = 28 dBm is shown in Fig. A.4a. Maximum P_L for the two signals is acquired for different Z_L, with 128-QAM providing a higher P_L. This means that if the DUT output is matched to P_8 based on the 1-tone contours, a 128-QAM operation would give P_L = 37.2 dBm $\simeq$ 5.3 W, whereas the maximum attainable is 37.7 dBm $\simeq$ 5.9 W. The difference is 0.6 W, which can be a significant power value in wireless communications. Another way to underline this difference is to isolate the contours for a certain P_L level, as shown in Fig. A.4b. The 1-tone contour for $P_L \simeq 37$ dBm overlaps with the corresponding 128-QAM contour only over a very small region of the latter.

For linearity, 2-tone IM3 and 128-QAM ACPR measurements were performed in two adjacent frequency channels below and above the signal bandwidth. The measurements, shown in Fig. A.5 and Fig. A.6, show IM3 and ACPR values for each P_{avs} level being similar. All optimal Z_L points are adjacent on the Smith Chart and move towards the real axis as P_{avs} level increases, with linearity worsening, as expected, since the drive moves closer to saturation.

Table A.2: The L-P measurement results for all $P_{i\in[1,23]}$

Figure	P_i	Signal Type	Z_L (Ω)	P_{avs} / P_L (dBm)	IM3 / ACPR (dBc)	Figure	P_i	Signal Type	Z_L (Ω)	P_{avs} / P_L (dBm)	IM3 / ACPR (dBc)
A.3a	P_1	1-tone	48.6 + j31.4	20 / 30.7	– / –	A.5b	P_{13}	2-tone	0.3 + j29.8	20 / –	-27.6 / –
	P_2	1-tone	47.4 + j26.7	24 / 34.4	– / –		P_{14}	2-tone	5.8 + j16.4	24 / –	-27.3 / –
	P_3	1-tone	40.9 + j16.7	28 / 37.2	– / –		P_{15}	2-tone	1.3 + j0.4	28 / –	-24.8 / –
A.3b	P_4	128-QAM	40.2 + j25.8	20 / 32.6	– / –	A.6a	P_{16}	128-QAM	8.8 + j14.7	20 / –	– / -27.5
	P_5	128-QAM	37.7 + j15.6	24 / 35.7	– / –		P_{17}	128-QAM	11.6 + j13.5	24 / –	– / -26.7
	P_6	128-QAM	29.1 + j9.1	28 / 37.7	– / –		P_{18}	128-QAM	4.6 + j4.2	28 / –	– / -25
	P_7	128-QAM	20.6 + j7.6	32 / 37.2	– / –		P_{19}	128-QAM	11.3 + j5	32 / –	– / -23.3
A.4a	P_8	1-tone	40.9 +j16.7	28 / 37.2	– / –	A.6b	P_{20}	128-QAM	10.2 + j17.8	20 / –	– / -28.4
	P_9	128-QAM	29.1 + j9.1	28 / 37.7	– / –		P_{21}	128-QAM	12.2 + j12	24 / –	– / -26.6
A.5a	P_{10}	2-tone	0.4 + j18.7	20 / –	-27 / –		P_{22}	128-QAM	4.6 + j4.2	28 / –	– / -27
	P_{11}	2-tone	1.6 + j14.3	24 / –	-25.7 / –		P_{23}	128-QAM	8.7 + j3	32 / –	– / -23.3
	P_{12}	2-tone	0.5 + j18.7	28 / –	-23 / –						

From [9] ©2020 IEEE.

APPENDIX B

AEROSOL JET PRINTING MATERIALS

B.1 Material Mixing, Handling, and Storage

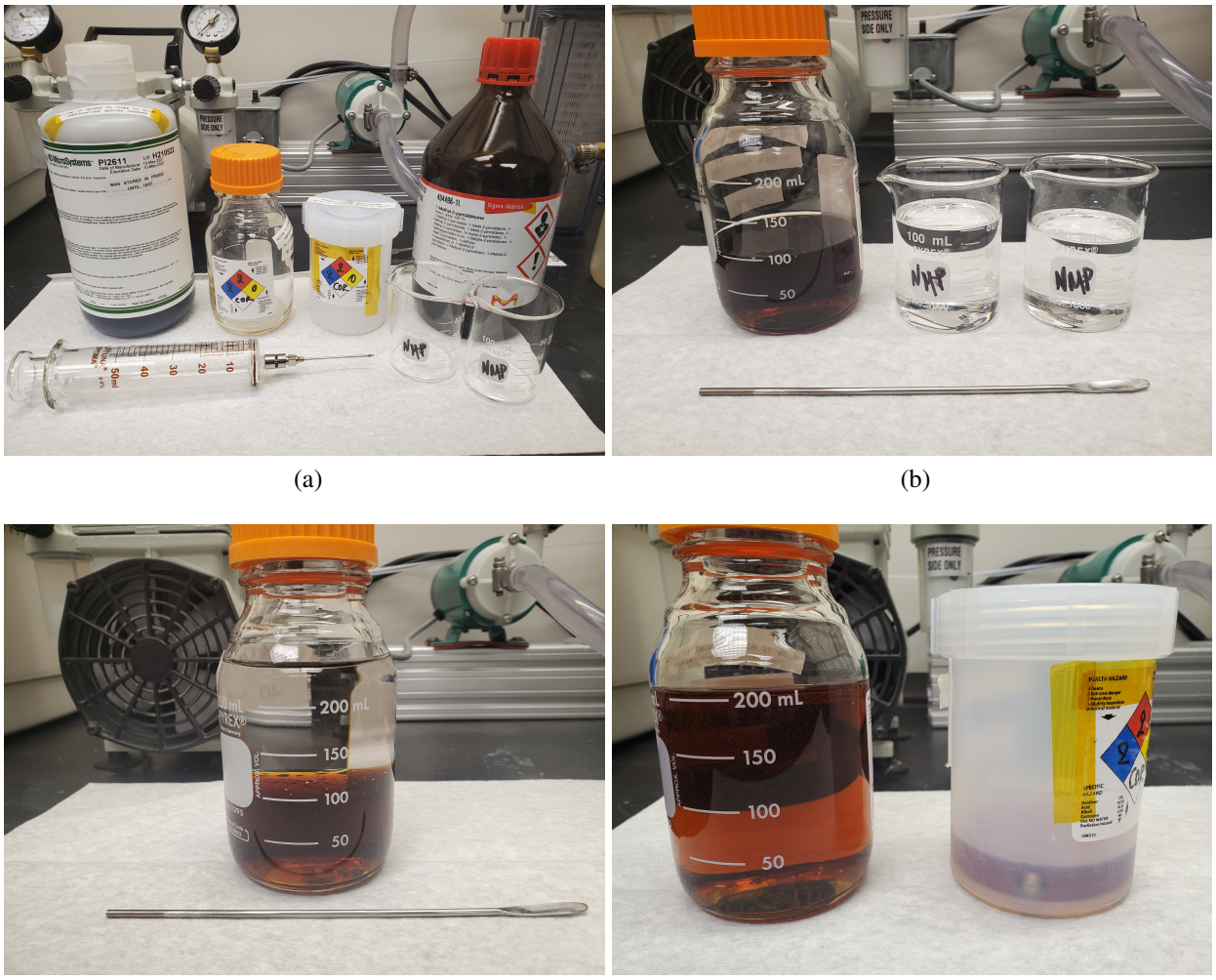
This section provides a summary of mixing procedures, as well as suggestions for handling and storing the materials used for the fabrication of aerosol jet-printed components in this dissertation. All the materials were printed using the Optomec Aerosol Jet 5X printer. Details on the printer and the printing procedures are given in Appendix C. PI and BCB inks are used for the fabrication of dielectrics that support TLs and interconnects, while Ag ink is used for the conductive paths of the TLs and interconnects. Following are details for each ink.

B.1.1 Polyamic Acid/Polyimide

The PI ink used was composed of PI-2611 polyamic acid (by HD Microsystems [131]) diluted to 40 vol.% PI-2611 + N-Methyl-2-Pyrrolidone (NMP) (by Sigma Aldrich), following the recipe used by Craton in [128]. Cured PI-2611 has a published $\epsilon_{\mathrm{r}} = 2.9$ and $\tan\delta = 0.002$ at 1 KHz, with a thermal curing at 350 °C for 30 min adequate to achieve the fully cured film properties. The steps for mixing PI ink are shown in Fig. B.1. PI is sensitive to moisture, which makes it prone to delamination from the edges of the die at elevated temperature during thermal curing. Therefore, steps to minimize PI ink exposure to moisture are necessary. Handling measures for the PI ink are the following:

i. Store unmixed and mixed PI in tightly sealed containers, in a freezer (to maintain expected shelf life and minimize moisture absorption).

ii. Minimize time outside of freezer (to maintain expected shelf life and minimize moisture absorption).



(a) (b)

(c) (d)

Figure B.1: Steps for mixing PI-2611 ink, mixing 100 mL PI-2611 with 150 mL NMP: (a) Setup before mixing, (b) PI-2611 added to glass container and NMP added to glass beakers, (c) glass container with unmixed PI-2611 and NMP, (d) mixed PI-2611 with NMP in glass container and in PA jar.

iii. Allow containers to come to room temperature before opening (to minimize moisture absorption).

iv. Minimize exposure of unmixed and mixed PI with air (to minimize moisture absorption).

v. Apply 0.1 vol % VM651 + DI water adhesion promoter before first layers of PI-2611 are printed on metal or dielectric (to enhance adhesion of PI).

B.1.2 Benzocyclobutene

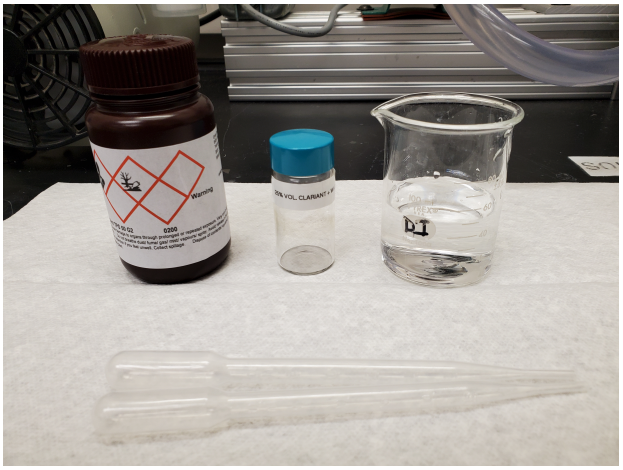
The BCB ink used is the Cyclotene 3022-35 resin (by Dow Chemicals [132]), which is composed of B-staged benzocyclobutene (BCB) monomers diluted in mesitylene by the manufacturer. Cured Cyclotene 3022-35 has a published $\epsilon_r = 2.65$ from 1 to 20 GHz and a $\tan\delta = 0.0008$. This ink has a low viscosity of 14 cSt at room temperature. This ink comes pre-mixed and is robust and not sensitive to moisture. It can be stored in tightly sealed containers, in room temperature. It is suggested to apply the AP2000 adhesion promoter before the first layers of BCB are printed on metal or dielectric, to enhance adhesion.

B.1.3 Silver

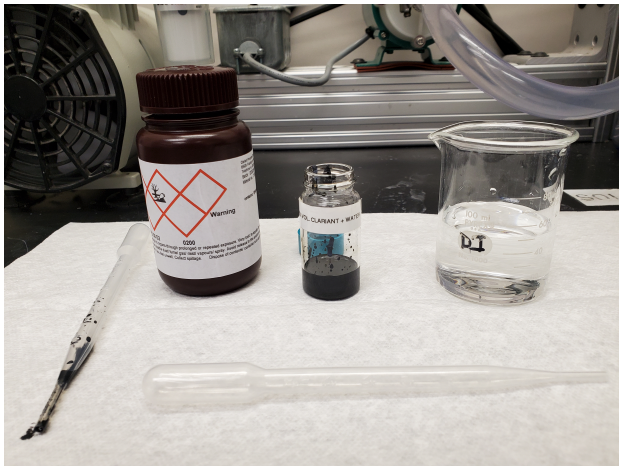
The Ag ink used is an Ag nanoparticle ink which consists of 25 wt.% Clariant Prelect TPS 50 + DI water, following the recipe used by Craton in [128]. The Ag nanoparticles and the mixed Ag ink need to be stored in tightly sealed containers, in a fridge. The steps for mixing Ag ink are shown in Fig. B.2. The ink can be further mixed under ultrasonication for 30 min prior to printing.

B.2 Thermal Curing and Sintering

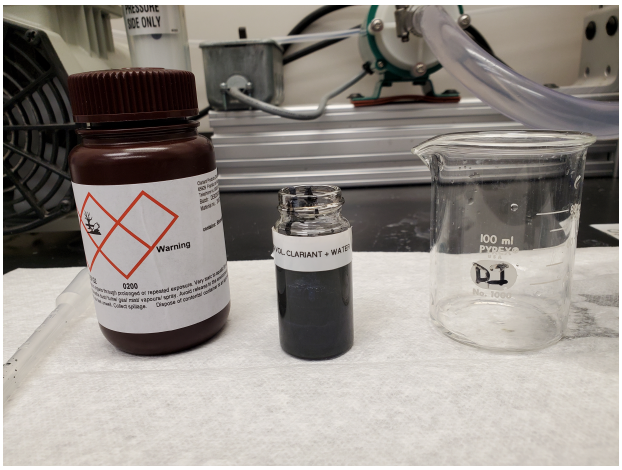
After inks are deposited via AJP, thermal processing is necessary for them to acquire final properties. The Ag ink needs to be sintered to become conductive, while the PI and BCB inks need to be thermally cured to attain their final dielectric properties. A summary of the thermal curing and sintering profiles used in this dissertation is given in Table B.1. All thermal processing was done using a Yamato inert oven.



(a)



(b)



(c)

Figure B.2: Steps for mixing Ag ink, mixing 5 mL Ag with 15 mL DI water: (a) Setup before mixing, (b) Ag nanoparticles added to glass container and DI water added to glass beaker, (c) mixed Ag with DI water in glass container.

Table B.1: Basic Thermal Curing and Sintering Profiles for AJP Materials

Program	**Step #**	**Time**	**Target Temperature (°C)**	**Environment**	**Application**
1	1	1 h 30 min†	200	N_2	Soft cure for PI
	2	2 min	200		
	3	0#	40		
2	1	2 h 18 min†	295	N_2	Hard cure for PI
	2	1 h	295		
	3	0#	40		
3	1	2 h†	250	N_2	Hard cure for BCB
	2	1 h	250		
	3	0#	40		
4	1	1 h 20 min†	180	Atmosphere	Sintering Ag
	2	5 h	180		
	3	0#	40		

† Time in step 1 is time to reach target temperature; # time in final step is set to zero to allow for slow cooldown to target temperature.

APPENDIX C

AEROSOL JET PRINTING PROCEDURES

This appendix focuses on the printing procedures used for the fabrication of additively manufactured components and packages in this dissertation. An overview of the printer used is given first, where I discuss the basic parts of the printer. An overview of cleaning procedures for the printer parts are presented, as well. Then, several examples of printing procedures are presented, for various parts exhibited in earlier chapters of the dissertation.

C.1 Printer Setup and Cleaning Procedures

All the aerosol jet-printed parts demonstrated in this dissertation were printed using an Optomec Aerosol Jet 5X Printer. This printer is equipped with two ink atomizers: a pneumatic atomizer (PA), generally used to atomize high-viscosity inks, and an ultrasonic atomizer (UA), for low-viscosity inks. In this dissertation, all dielectric inks (PI and BCB) are printed using the PA, while Ag ink is printed using the UA. The printer has the capability to resolve features below 10 μm and to print from a standoff distance up to 10 mm without significant resolution loss.

The material in each atomizer is aerosolized via nitrogen gas, directed towards the print head through tubes, and then focused through a printing nozzle via sheath nitrogen gas. The atomizers and print head parts need to be assembled by the user, and detailed assembly steps have been presented by Craton in [128]. The UA utilizes ultrasonic energy alone to produce the aerosol stream, thus the entire set flow rate is directed towards the print head. In the case of the PA, the aerosol flow is rather divided into two flows: a flow towards an exhaust, filters, and finally a vacuum pump, and a flow towards the print head. The printer user can control the aerosol flow rates, atomizer pressure, ink temperature, printing stage temperature, as well as the movement of the stage and print head. Controlling the print head and stage movement gives an overall 5-axis movement capability (x, y, z, θ, and ϕ). A basic diagram with the major parts of the printer is shown in Fig. C.1.

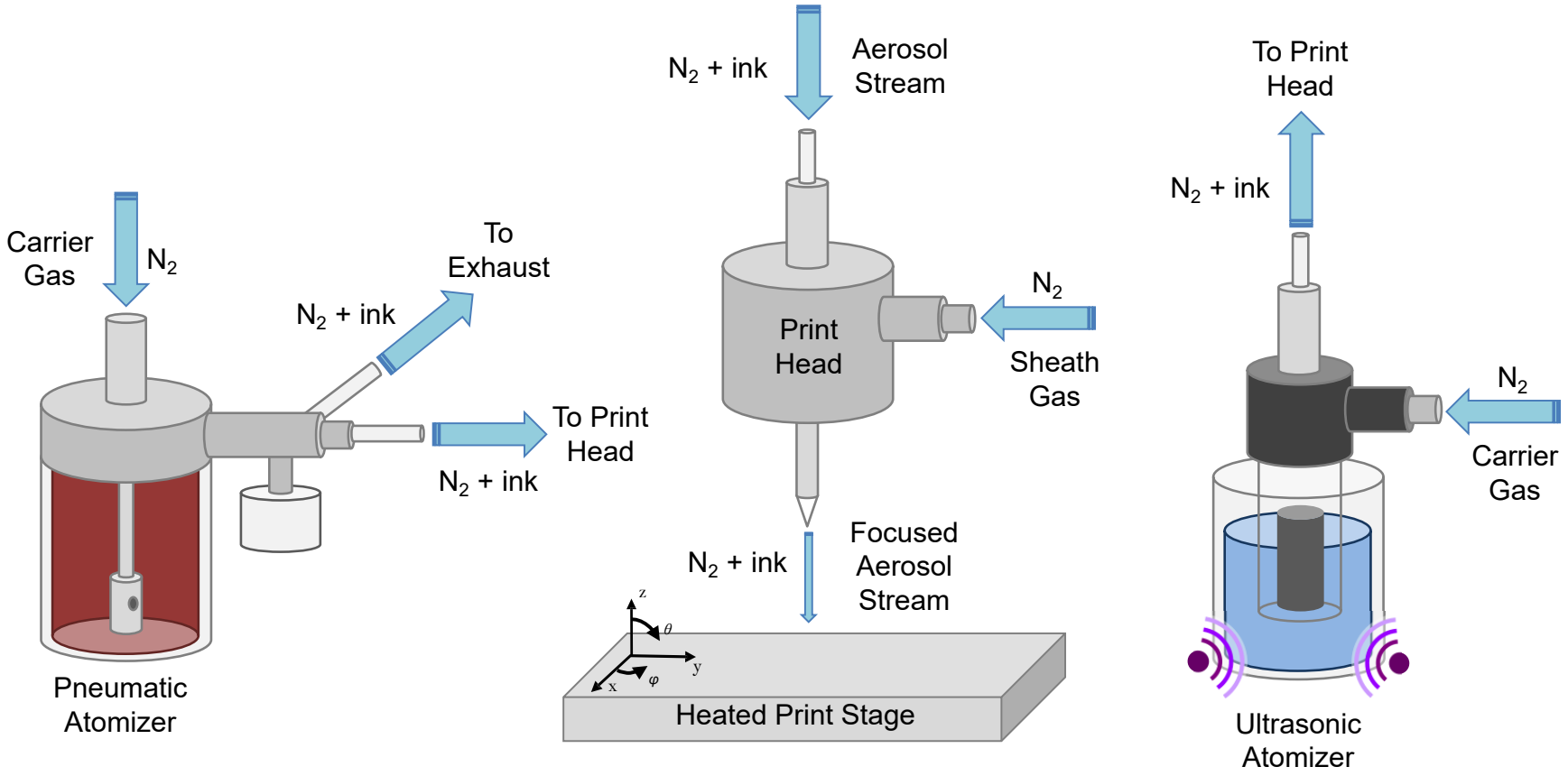


Figure C.1: The major parts of the Optomec Aerosol Jet 5X Printer.

Table C.1: Printer Cleaning Procedures for Used Materials

Material-to-be-cleaned	Step #	Cleaning Solution	Cleaning Process
PI	1	NMP	Ultrasonic bath for 30 min
	2	IPA	Ultrasonic bath for 30 min or rinse
BCB	1	Mesitylene	Ultrasonic bath for 30 min
	2	Acetone	Ultrasonic bath for 30 min or rinse
	3	10% Branson IS + DI water	Ultrasonic bath for 30 min
	4	IPA	Ultrasonic bath for 30 min or rinse
Ag	1	DI water	Rinse
	2	10% Branson IS + DI water	Ultrasonic bath for 30 min
	3	DI water	Rinse
	4	IPA	Ultrasonic bath for 30 min or rinse

Maintaining all printer parts clean is necessary to obtain good printing results. Therefore, cleaning of the printing equipment must be done after every printing session, specifically since ink particles that remain on the parts will partially cure if not removed after printing and will be harder to remove after a while. The chemicals used for cleaning depend on which ink is printed. In general, the first cleaning step is to clean the parts using the same solvent used with the ink printed (e.g. NMP for PI ink, mesitylene for BCB ink). Detailed cleaning steps have been presented by Craton in [128], thus here I only give an overview of the cleaning steps I followed for each ink I used in this dissertation in Table C.1.

C.2 Printing Procedures

This sections includes details of the procedures I followed to fabricate the aerosol jet-printed parts demonstrated in this dissertation. For each part, the basic steps for the printing drawing are given, followed by tables that give details of the printing procedures. For each additively manufactured part, each table details the following:

i. Fabrication part: The individual part of the prototype being manufactured. PI and BCB are printed for dielectric parts, to support either TLs or die interconnects, while Ag is printed for conductive parts of the TLs and interconnects.

ii. Process/rapid speed: Process speed is the speed while the shutter is open and material is being deposited. Rapid speed is the speed while the shutter is closed and the print head moves between printing positions. Both speeds are maintained lower while printing Ag, as the minimum resolution required for conductive paths is smaller that for dielectrics.

iii. Nozzle diameter: The diameter of the nozzle/tip used with the print head. In general, smaller nozzle diameter allows for smaller printed trace widths.

iv. Run No.: Print run number.

v. S_MFC: The sheath gas flow rate (in SCCM), with the corresponding measured local pressure (in PSI).

vi. PA_MFC: The gas flow rate in the PA (in SCCM), with the corresponding measured local pressure (in PSI).

vii. EX_MFC: The gas flow rate in the PA exhaust (in SCCM), with the corresponding measured local pressure (in PSI).

viii. UA_MFC: The gas flow rate in the UA (in SCCM), with the corresponding measured local pressure (in PSI). The current for the ultrasonic power was kept at $\sim$ 500 mA in all cases.

ix. Run duration: The total time for each printing run.

C.2.1 EBG Resonators

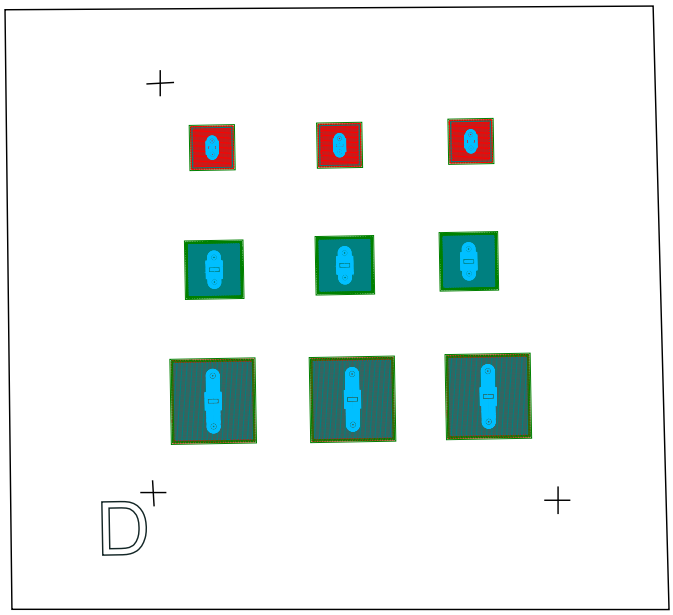


Figure C.2: Complete AutoCAD© drawing of a MoCu carrier with 3 sets of resonators.

The fully aerosol jet-printed resonators were fabricated on MoCu carriers. On each carrier, three sets of three different resonator structures (type-A, B, and C, as defined in Section 4.1) were designed and fabricated. An example of a complete drawing of a MoCu carrier with EBG resonators is shown in Fig. C.2. A general drawing procedure on AutoCAD© for the resonator parts is the following:

i. Drawing of MoCu carrier outline using printer alignment camera.

ii. Drawings of thin PI, thick PI, and Ag layers, as well as alignment marks and part name.

iii. Generation of printing paths.

iv. Addition of alignment mark locations as fiducial points in printing file.

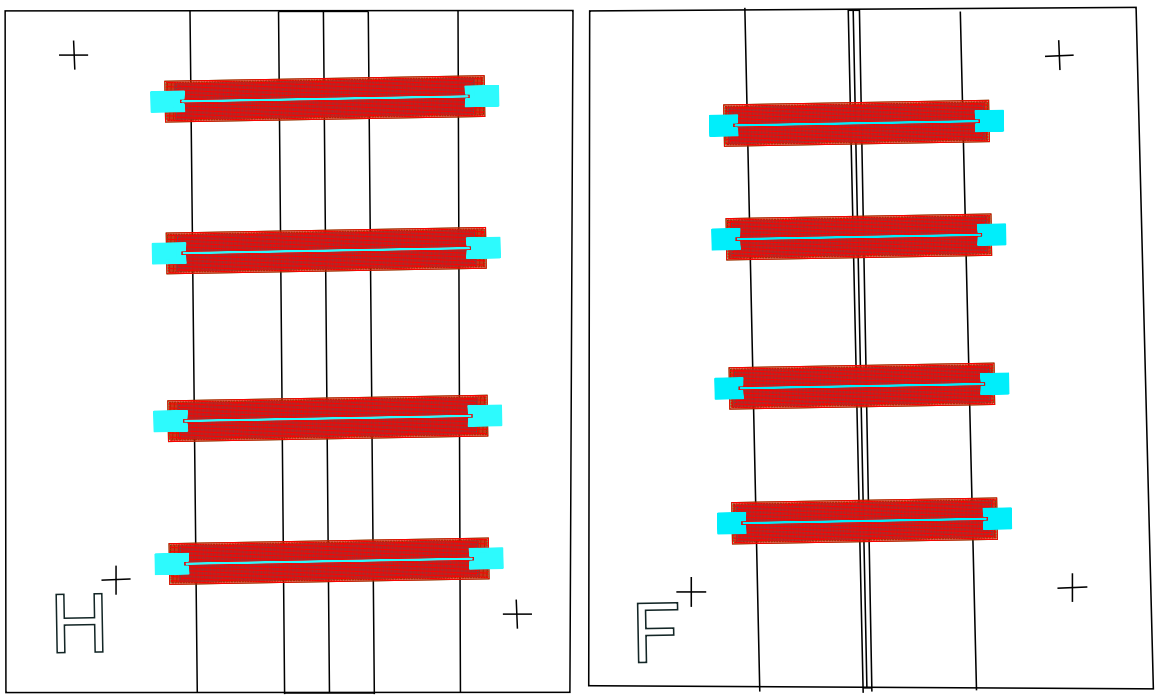
v. Structures can be re-simulated and re-drawn based on printed dielectric thicknesses prior to printing Ag.

The printing procedures for the part shown in Fig. C.2 are presented in Table C.2.

Table C.2: Example of Printing Procedures for EBG Resonators

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thin PI	4/8	300	1	120/0.25	1010/5.16	975/0.17	N/A	9 min 26 sec
			2	120/0.25	1010/5.24	975/0.16		9 min 28 sec
			3	120/0.25	1010/5.30	975/0.15		9 min 27 sec
			4	120/0.26	1010/5.31	975/0.17		9 min 27 sec
			5	120/0.26	1010/5.34	975/0.18		9 min 27 sec
Soft bake PI								
Thick PI	2/8	300	1	100/0.21	1000/5.05	965/0.14	N/A	15 min 56 sec
			2	100/0.22	1000/5.16	965/0.12		15 min 58 sec
			3	100/0.22	1000/5.21	965/0.12		15 min 58 sec
Hard bake PI								
Ag	1/4	100	1	30/1.84	N/A	N/A	21/2.89	12 min 22 sec
			2	30/1.83			21/2.89	11 min 56 sec
			3	30/1.85			21/2.89	11 min 56 sec
Sinter Ag								

C.2.2 UWB TLs on Non-Planar Structures



(a) (b)

Figure C.3: Complete AutoCAD© drawing of (a) a 5-mm-high ramped part, and (b) a 5-mm-high conformal/curved part.

The fully aerosol jet-printed UWB TLs were fabricated on machined brass carriers. On each carrier, four TLs were designed and fabricated. I fabricated TLs on 2-mm- and 5-mm-high ramped parts and on 2-mm- and 5-mm-high curved parts. Examples of complete drawings are shown in Fig. C.3. A general drawing procedure on AutoCAD© for the UWB TLs follows the same steps as described in Section C.2.1, with the difference of drawing the brass carrier outline, ramp/curve edges, and center axis instead of the carrier outline, using the printer alignment camera. The printing procedures for the parts shown in Fig. C.3a and C.3b are presented in Tables C.3 and C.4, respectively.

Table C.3: Example of Printing Procedures for UWB TLs on Nonplanar Structures (Ramped Part Case)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thin PI	4/8	300	1	120/0.26	1000/5.09	972/0.25	N/A	11 min 4 sec
			2	120/0.26	1000/5.15	972/0.24		11 min 2 sec
			3	120/0.26	1000/5.17	972/0.24		11 min 2 sec
			4	120/0.26	1000/5.17	972/0.24		11 min 2 sec
			5	120/0.26	1000/5.21	972/0.24		11 min 2 sec
Soft bake PI								
Thick PI	2/8	300	1	120/0.24	1000/5.06	972/0.26	N/A	17 min 16 sec
			2	120/0.24	1000/5.14	972/0.26		17 min 16 sec
			3	120/0.25	1000/5.20	972/0.26		17 min 16 sec
			4	120/0.25	1000/5.23	972/0.25		17 min 16 sec
			Printing tube change					
			5	120/0.24	1000/5.02	972/0.26	N/A	17 min 16 sec
			6	120/0.25	1000/5.14	972/0.26		17 min 16 sec
			7	120/0.25	1000/5.18	972/0.26		17 min 16 sec
			8	120/0.25	1000/5.21	972/0.25		17 min 16 sec
			9	120/0.25	1000/5.23	972/0.24		17 min 16 sec
Hard bake PI								
Ag	1/4	150	1	65/0.94	N/A	N/A	21/2.01	11 min 41 sec
			2	65/0.94			21/2.00	11 min 37 sec
			3	65/0.93			21/1.99	11 min 37 sec
Sinter Ag								

Table C.4: Example of Printing Procedures for UWB TLs on Nonplanar Structures (Conformal/Curved Part Case)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thin PI	4/8	300	1	120/0.26	1000/5.12	972/0.23	N/A	8 min 58 sec
			2	120/0.26	1000/5.16	972/0.22		8 min 59 sec
			3	120/0.26	1000/5.18	972/0.22		8 min 59 sec
			4	120/0.26	1000/5.20	972/0.22		8 min 59 sec
			5	120/0.26	1000/5.22	972/0.21		8 min 59 sec
Soft bake PI								
Thick PI	2/8	300	1	120/0.25	1000/5.32	972/0.23	N/A	14 min 14 sec
			2	120/0.25	1000/5.34	972/0.23		14 min 14 sec
			3	120/0.24	1000/5.34	972/0.25		14 min 14 sec
			4	120/0.24	1000/5.36	972/0.25		14 min 14 sec
			Printing tube change					
			5	120/0.24	1000/5.02	972/0.25	N/A	14 min 14 sec
			6	120/0.24	1000/5.14	972/0.26		14 min 14 sec
			7	120/0.24	1000/5.18	972/0.26		14 min 14 sec
			8	120/0.25	1000/5.21	972/0.25		14 min 14 sec
			9	120/0.25	1000/5.23	972/0.24		14 min 14 sec
Hard bake PI								
Ag	1/4	150	1	65/0.94	N/A	N/A	21/1.99	9 min 36 sec
			2	65/0.94			21/2.00	9 min 31 sec
			3	65/0.93			21/1.98	9 min 31 sec
Sinter Ag								

C.2.3 Components at 140-220 GHz

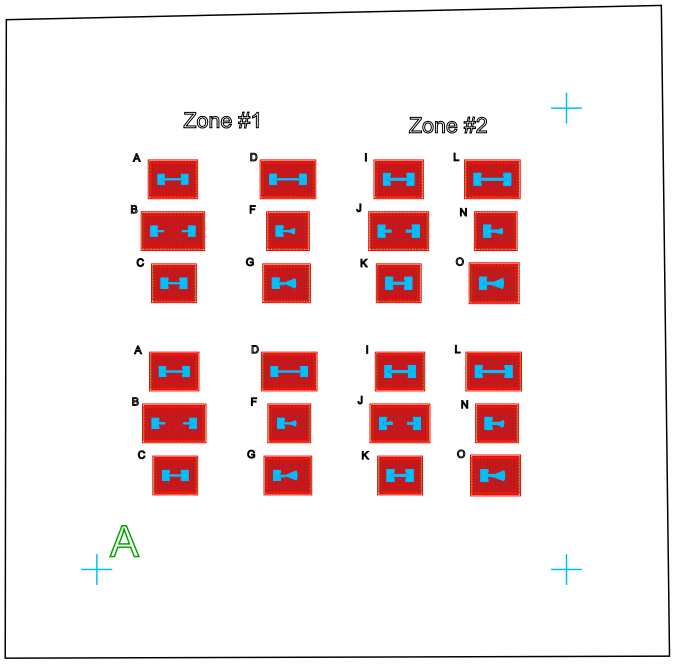


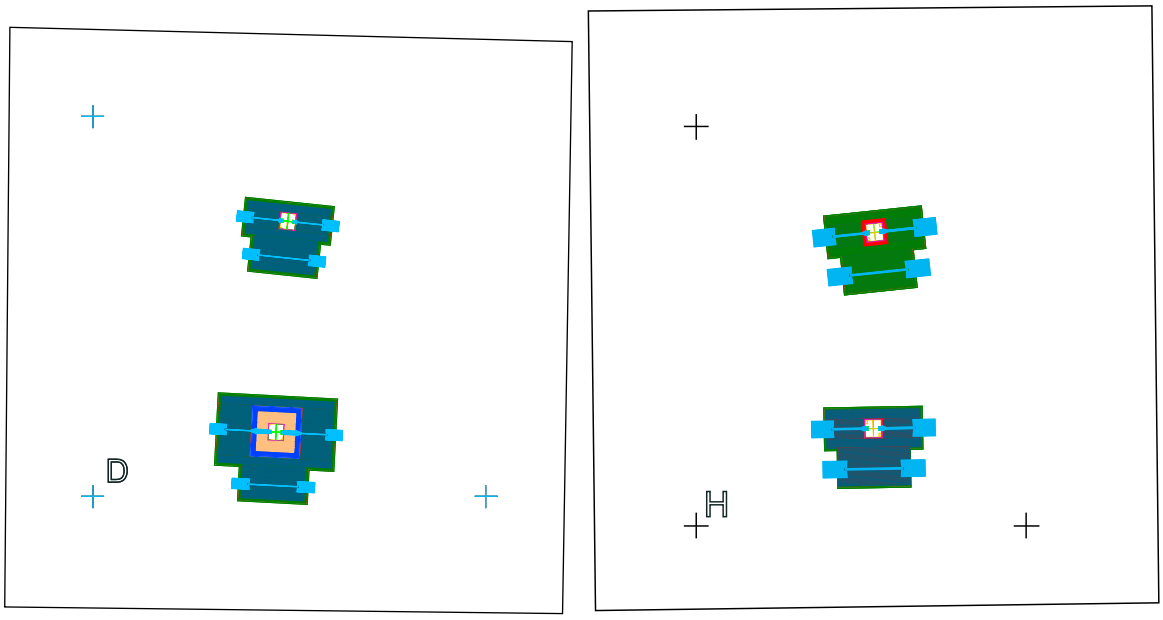
Figure C.4: Complete AutoCAD© drawing of a MoCu carrier with TLs and radial stubs at 140-220 GHz.

The fully aerosol jet-printed components at near-THz frequencies were fabricated on MoCu carriers. Each carrier has two sets of TLs, radial stubs, and calibration structures, namely Zones 1 and 2. What distinguishes the two Zones is the thickness of the PI, which is larger for Zone 2. An example of a complete drawing is shown in Fig. C.4. A general drawing procedure on AutoCAD© for the chip-first packages follows the same steps as described in Section C.2.1. The printing procedures for a single carrier are presented in Table C.5.

Table C.5: Example of Printing Procedures for Components at 140-220 GHz

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thin PI	4/8	300	1	100/0.18	1000/4.82	972/0.11	N/A	10 min 18 sec
			2	100/0.18	1000/4.90	972/0.10		9 min 21 sec
			3	100/0.18	1000/4.95	972/0.09		9 min 21 sec
			4	100/0.18	1000/4.96	972/0.08		9 min 21 sec
			5	100/0.18	1000/4.99	972/0.10		9 min 21 sec
Soft bake PI								
Thick PI (Zones 1 & 2)	2/8	300	1	100/0.19	1010/5.29	980/0.09	N/A	13 min 48 sec
			2	100/0.18	1000/5.24	975/0.10		13 min 25 sec
			3	100/0.18	1000/5.25	975/0.09		13 min 23 sec
			4	100/0.18	1000/5.27	978/0.08		13 min 23 sec
			5	100/0.18	1000/5.28	978/0.08		13 min 23 sec
			6	100/0.17	1000/5.30	978/0.07		13 min 23 sec
Thick PI (Zone 2)	2/8	300	1	100/0.18	1000/5.29	978/0.06	N/A	6 min 25 sec
			2	100/0.19	1000/5.15	970/0.11		6 min 25 sec
			3	100/0.19	1000/5.19	970/0.11		6 min 23 sec
			4	120/0.19	1000/5.21	970/0.11		6 min 23 sec
			5	100/0.19	1000/5.22	970/0.11		6 min 23 sec
			6	100/0.18	1000/5.23	970/0.10		6 min 23 sec
Hard bake PI								
Ag	1/4	150	1	65/0.85	N/A	N/A	21/1.94	8 min 8 sec
			2	65/0.85			21/1.92	8 min 6 sec
			3	65/0.85			21/1.92	8 min 6 sec
Sinter Ag								

C.2.4 Chip-First Packages



(a) (b)

Figure C.5: Complete AutoCAD© drawing of (a) a carrier with a part following approach 1 (bottom) and a part with PI ramps (top, for experimentation), and (b) a carrier with two parts following approach 2.

The fully aerosol jet-printed chip-first packages were fabricated on MoCu carriers. On each carrier, two attenuator dies were packaged following either approach 1 or approach 2. Examples of complete drawings are shown in Fig. C.3. A general drawing procedure on AutoCAD© for the chip-first packages follows the same steps as described in Section C.2.1, with additional drawing for the die apart from the MoCu carrier, as well as PI wall and BCB fill for approach 1, and BCB ramps for approach 2. The design is tailored to the exact position of the two dies on each carrier. The printing procedures for the packages following approach 1 are presented in Tables C.6-C.8 and for approach 2 in Tables C.9, C.10.

Table C.6: Example of Printing Procedures for Chip-First Package Following Approach 1 (Part 1)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
PI ramps	2/8	300	1	100/0.19	1000/4.95	970/0.18	N/A	N/A
			2	100/0.19	1000/4.97	970/0.17		
			3	100/0.19	1000/4.99	970/0.17		
			4	100/0.19	1000/5.01	970/0.17		
PI on die edge	2/8	300	1	100/0.19	1000/5.02	970/0.17	N/A	N/A
			2	100/0.19	1000/5.02	970/0.18		
Thin PI & PI wall	4/8	300	1	100/0.19	1000/5.05	970/0.18	N/A	5 min 50 sec
			2	100/0.19	1000/5.05	970/0.18		5 min 49 sec
			3	100/0.19	1000/5.07	970/0.18		5 min 49 sec
			4	100/0.19	1000/5.09	970/0.18		5 min 49 sec
Soft bake PI								

Table C.7: Example of Printing Procedures for Chip-First Package Following Approach 1 (Part 2)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
PI on die edge	2/8	300	1	100/0.18	1000/4.87	970/0.17	N/A	N/A
			2	100/0.18	1000/4.89	970/0.17		
Thick PI	2/8	300	1	100/0.18	1000/4.92	970/0.16	N/A	8 min 45 sec
			2	100/0.19	1000/4.97	970/0.16		8 min 46 sec
			3	100/0.19	1000/5.02	970/0.16		8 min 46 sec
			Printing tube change					
			4	100/0.19	1000/4.92	970/0.16	N/A	8 min 49 sec
			5	100/0.19	1000/4.97	970/0.15		8 min 46 sec
			6	100/0.19	1000/5.01	970/0.15		8 min 46 sec
			7	100/0.19	1000/5.04	970/0.14		8 min 46 sec
			8	100/0.19	1000/5.04	970/0.14		8 min 46 sec
			Printing tube change					
PI Wall	2/8	300	1	100/0.19	1000/4.99	970/0.19	N/A	1 min 39 sec
			2	100	1000	970		1 min 40 sec
			3	100	1000	970		1 min 40 sec
			4	100	1000	970		1 min 40 sec
			5	100	1000	970		1 min 40 sec
			6	100	1000	970		1 min 40 sec
			7	100	1000	970		1 min 40 sec
			8	100	1000	970		1 min 40 sec
Hard bake PI								

Table C.8: Example of Printing Procedures for Chip-First Package Following Approach 1 (Part 3)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
BCB Fill	2/8	200	1	65/0.34	680/2.82	650/0.40	N/A	42 sec
			2	65	680	650		42 sec
			3	65	680	650		42 sec
			4	65	680	650		42 sec
			5	65/0.34	680/2.85	640/0.43		42 sec
			6	65	680	650		42 sec
			7	65	680	650		42 sec
			8	65/0.34	680/2.86	650/0.44		42 sec
Hard bake BCB								
Ag	1/4	150	1	65/1.00	N/A	N/A	23/2.12	5 min 11 sec
			2	65/0.99			23/2.10	5 min 14 sec
			3	65/0.99			23/2.09	5 min 13 sec
			4	65/1.01			23/2.11	5 min 13 sec
			5	65/1.01			23/2.11	5 min 13 sec
Sinter Ag								

Table C.9: Example of Printing Procedures for Chip-First Package Following Approach 2 (Part 1)

Fabrication Part	Process/ Rapid Speed (mm/sec)	Nozzle Diameter (μm)	Run No.	S_MFC (SCCM/ PSI)	PA_MFC (SCCM/ PSI)	EX_MFC (SCCM/ PSI)	UA_MFC (SCCM/ PSI)	Run Duration
PI on die edge	2/8	300	1	100/0.19	1000/4.86	975/0.20	N/A	5 sec
			2	100/0.19	1000/4.86	975/0.20		5 sec
			3	100/0.19	1000/4.86	975/0.20		5 sec
Thin PI	4/8	300	1	100/0.19	1000/4.87	970/0.21	N/A	3 min 59 sec
			2	100/0.19	1000/4.89	970/0.20		3 min 57 sec
			3	100/0.19	1000/4.90	970/0.18		3 min 57 sec
			4	100/0.19	1000/4.93	970/0.18		3 min 57 sec
Soft bake PI								
Thick PI	2/8	300	1	100/0.18	1000/4.90	972/0.20	N/A	6 min 39 sec
			2	100/0.19	1000/4.92	972/0.21		6 min 40 sec
			3	100/0.19	1000/4.95	972/0.18		6 min 40 sec
			4	100/0.19	1000/4.97	972/0.18		6 min 40 sec
			5	100/0.19	1000/4.99	972/0.17		6 min 40 sec
			6	100/0.19	1000/5.01	972/0.19		6 min 40 sec
			Printing tube change					
			7	100/0.19	1000/4.90	972/0.19	N/A	6 min 42 sec
			8	100/0.19	1000/4.96	972/0.18		6 min 40 sec
			9	100/0.18	1000/4.99	972/0.17		6 min 40 sec
Hard bake PI								

Table C.10: Example of Printing Procedures for Chip-First Package Following Approach 2 (Part 2)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
BCB Ramps	2/8	200	1	65/0.34	680/2.82	650/0.32	N/A	41 sec
			2	65/0.34	680/2.82	650/0.32		41 sec
Hard bake BCB								
Ag	1/4	150	1	65/0.98	N/A	N/A	21/2.05	7 min 3 sec
			2	65/0.97			21/2.04	7 min 6 sec
			3	65/0.98			21/2.04	7 min 6 sec
			4	65/0.98			21/2.04	7 min 6 sec
Sinter Ag								

C.2.5 System-on-Antenna

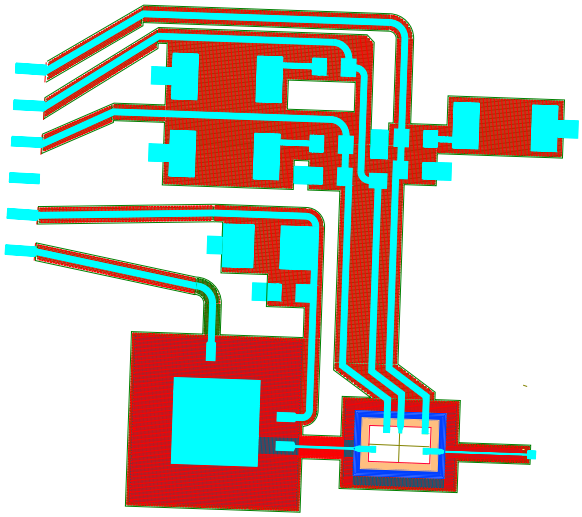


Figure C.6: Complete AutoCAD© drawing of a SoA.

The SoA package was fabricated on a conventionally manufactured Vivaldi antenna. The package includes an amplifier die, printed dielectrics for the die package, TLs, antenna feed, and biasing networks, as well as SMC VCO, resistors, and capacitors. An example of a complete drawing is shown in Fig. C.6. A general drawing procedure on AutoCAD© for the chip-first packages follows the same steps as described in Section C.2.4, with the differences being the inclusion of antenna features (such as tapered slot points an DC pads) in the drawing and the placement of SMCs after curing of the printed Ag. The printing procedures for a single carrier are presented in Tables C.11-C.14.

Table C.11: Example of Printing Procedures for the Ka-Band SoA (Part 1)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
PI on die edge	2/8	300	1	100	1000	970	N/A	9 sec
			2	100	1000	970		9 sec
Thin PI & PI wall	4/8	300	1	100/0.19	1000/4.88	970/0.12	N/A	26 min 56 sec
			2	100/0.20	1000/5.02	970/0.12		26 min 44 sec
			3	100/0.20	1000/5.05	970/0.11		26 min 44 sec
			4	100/0.19	1000/5.07	970/0.13		26 min 44 sec
Soft bake PI								

Table C.12: Example of Printing Procedures for the Ka-Band SoA (Part 2)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thin PI & PI Wall	4/8	300	1	100/0.20	1005/5.54	970/0.12	N/A	33 min 46 sec
Thick PI	2/8	300	1	100/0.21	1005/5.54	970/0.12	N/A	12 min 14 sec
			2	100/0.20	1000/5.50	970/0.11		12 min 13 sec
			3	100/0.20	1000/5.51	970/0.11		12 min 13 sec
			4	100/0.20	1000/5.53	970/0.11		12 min 13 sec
			5	100/0.20	1000/5.53	970/0.11		12 min 13 sec
			6	100/0.20	1000/5.53	975/0.10		12 min 13 sec
			7	100/0.19	1000/5.54	975/0.09		12 min 13 sec
PI Wall	2/8	300	1	100/0.19	1000/5.53	975/0.09	N/A	1 min 51 sec
			2	100/0.19	1000/5.53	975/0.09		1 min 51 sec
			3	100/0.19	1000/5.53	975/0.09		1 min 51 sec
			4	120/0.19	1000/5.53	975/0.09		1 min 51 sec
			5	100/0.19	1000/5.53	975/0.09		1 min 51 sec
			6	100/0.19	1000/5.35	975/0.09		1 min 51 sec
			7	100/0.19	1000/5.53	975/0.09		1 min 51 sec
			8	100/0.19	1000/5.55	975/0.09		1 min 51 sec
Hard bake PI								

Table C.13: Example of Printing Procedures for the Ka-Band SoA (Part 3)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
BCB Fill	2/8	200	1	65/0.37	685/2.82	650/0.40	N/A	42 sec
			2	65	680	685		42 sec
			3	65	680	685		42 sec
			4	65	680	685		42 sec
			5	65	685/2.85	640/0.43		42 sec
			6	65	685	650		42 sec
			7	65/0.36	680	650		42 sec
			8	65	680/2.86	650/0.44		42 sec
			9	65	680	650		42 sec
			10	65	685	650		42 sec
			11	65	685/2.85	640/0.43		42 sec
			12	65/0.37	685	650		42 sec
			13	65	685	650		42 sec
			14	65/0.34	685/2.86	650/0.44		42 sec
Hard bake BCB								

Table C.14: Example of Printing Procedures for the Ka-Band SoA (Part 4)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Ag (TLs & Interconnects)	1/4	150	1	65/0.87	N/A	N/A	22/2.00	2 min 40 sec
			2	65/0.87			22/1.99	2 min 40 sec
			3	65/0.87			22/1.99	2 min 40 sec
			4	65/0.86			22/1.98	2 min 40 sec
			5	65/0.86			22/1.98	2 min 40 sec
Ag (VCO GND)	1/4	150	1	65/0.87	N/A	N/A	22/1.98	11 min 25 sec
			2	65/0.87			22/1.97	11 min 27 sec
Ag (VCO DC Lines)	1/4	150	1	65/0.87	N/A	N/A	22/2.00	13 min 48 sec
			2	65/0.90			23/2.03	13 min 50 sec
Ag (HPA DC Lines)	1/4	150	1	65/0.88	N/A	N/A	23/2.02	38 min 1 sec
			2	65/0.86			23/2.00	38 min 1 sec
Sinter Ag								

C.2.6 Chip-First Package on Diamond

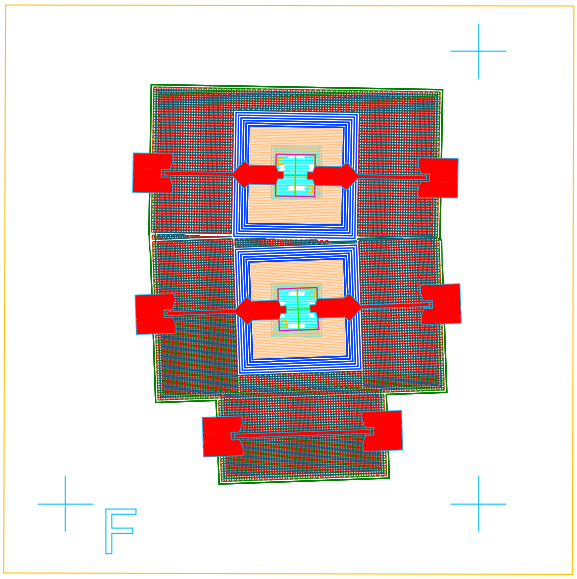


Figure C.7: Complete AutoCAD© drawing of a diamond wafer with a chip-first package, integrating two packaged attenuator dies and a TL.

The chip-first packages were fabricated on diamond wafers. The diamond wafer surface was sputtered with 20 nm Cr, 2 μm Cu, and 50 nm Ti. On each wafer, two attenuator dies were packaged following approach 1 (with the PI and the BCB fill). An example of a complete drawing is shown in Fig. C.7. A general drawing procedure on AutoCAD© for the chip-first packages on diamond follows the same steps as described in Section C.2.4 for approach 1, with the difference of drawing the outline of the diamond wafer instead of a MoCu carrier and the addition of the BCB/Ag die attach pad drawing. The design is tailored to the exact position of the two dies on each wafer. The printing procedures for the packages are presented in Tables C.15-C.17.

Table C.15: Example of Printing Procedures for Chip-First Package on Diamond (Part 1)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
BCB (die attach)	4/8	200	1	65/0.31	670/2.69	650/0.38	N/A	N/A
Ag (die attach)	4/8	200	1	65/0.37	N/A	N/A	25/1.55	N/A
			2	65/0.38			26/1.54	N/A
			3	65/0.38			26/1.53	N/A
			4	65/0.38			26/1.52	N/A
			5	65/0.39			26/1.52	N/A
			6	65/0.39			26/1.51	N/A
			7	65/0.38			26/1.50	N/A
Die attach reflow (cure BCB + sinter Ag)								
Thin PI & PI wall	4/8	300	1	100/0.18	1000/5.03	970/0.17	N/A	5 min 58 sec
			2	100/0.19	1000/5.04	970/0.17		5 min 59 sec
			3	100/0.18	1000/5.05	970/0.17		5 min 59 sec
			4	100/0.19	1000/5.06	970/0.16		5 min 59 sec
Soft bake PI								

Table C.16: Example of Printing Procedures for Chip-First Package on Diamond (Part 2)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
Thick PI	2/8	300	1	100/0.19	1000/4.98	972/0.20	N/A	7 min 34 sec
			2	100/0.19	1000/5.00	972/0.20		7 min 34 sec
			3	100/0.20	1000/5.03	970/0.20		7 min 34 sec
			4	100/0.20	1000/5.04	970/0.20		7 min 34 sec
			5	100/0.20	1000/5.06	970/0.20		7 min 34 sec
			6	100/0.20	1000/5.07	970/0.20		7 min 34 sec
			7	100/0.20	1000/5.08	970/0.20		7 min 34 sec
			8	100/0.20	1000/5.08	970/0.20		7 min 34 sec
			9	100/0.20	1000/5.09	970/0.20		7 min 34 sec
PI Wall	2/8	300	1	100/0.19	1000/5.09	975/0.19	N/A	2 min 59 sec
			2	100/0.19	1000/5.10	975/0.19		2 min 59 sec
			3	100/0.19	1000/5.10	975/0.19		2 min 59 sec
			4	100/0.19	1000/5.10	975/0.19		2 min 59 sec
			5	100/0.19	1000/5.10	975/0.15		2 min 59 sec
			6	100/0.19	1000/5.10	975/0.16		2 min 59 sec
			7	100/0.19	1000/5.11	975/0.16		2 min 59sec
			8	100/0.19	1000/5.11	975/0.16		2 min 59 sec
			9	100/0.19	1000/5.11	975/0.16		2 min 59 sec
			10	100/0.19	1000/5.11	975/0.16		2 min 59 sec
Hard bake PI								

Table C.17: Example of Printing Procedures for Chip-First Package on Diamond (Part 3)

Fabrication Part	**Process/ Rapid Speed (mm/sec)**	**Nozzle Diameter (μm)**	**Run No.**	**S_MFC (SCCM/ PSI)**	**PA_MFC (SCCM/ PSI)**	**EX_MFC (SCCM/ PSI)**	**UA_MFC (SCCM/ PSI)**	**Run Duration**
BCB on die edge	2/8	200	1	65	680	650	N/A	N/A
BCB Fill	2/8	200	1	65/0.30	670/2.66	650/0.34	N/A	1 min 24 sec
			2	65/0.30	675/2.71	650/0.36		1 min 24 sec
			3	65/0.32	675/2.74	650/0.37		1 min 24 sec
			4	65/0.33	675/2.75	650/0.38		1 min 24 sec
			5	65/0.33	675/2.76	640/0.37		1 min 24 sec
			6	65/0.32	675/2.73	650/0.36		1 min 24 sec
			7	65/0.30	675/2.72	650/0.34		1 min 24 sec
			8	65/0.30	675/2.72	650/0.36		1 min 24 sec
			9	65/0.30	675/2.72	650/0.36		1 min 24 sec
			10	65/0.30	675/2.72	650/0.36		1 min 24 sec
			11	65/0.30	675/2.73	650/0.36		1 min 24 sec
			12	65/0.30	675/2.75	650/0.36		1 min 24 sec
Hard bake BCB								
Ag	1/4	150	1	65/1.07	N/A	N/A	23/2.24	5 min 57 sec
			2	65/1.07			23/2.23	5 min 58 sec
			3	65/1.07			23/2.21	5 min 58 sec
			4	65/1.07			23/2.21	5 min 58 sec
			5	65/1.08			23/2.22	5 min 58 sec
Sinter Ag								

APPENDIX D

LIST OF PUBLICATIONS

- **X. Konstantinou**, J. D. Albrecht, P. Chahal and J. Papapolymerou, *"Flexible Chip-First Millimeter-Wave Packaging Using Multiple Dielectrics,"* in IEEE Transactions on Components, Packaging and Manufacturing Technology, vol. 12, no. 4, pp. 682-691, April 2022, doi:10.1109/TCPMT.2022.3160626.

- **X. Konstantinou** et al., *"Towards High-Power Multipliers Using Diamond Schottky Barrier Diodes,"* 2021 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), 2021, pp. 111-115, doi:10.1109/COMCAS52219.2021.9629034.

- **X. Konstantinou**, M. T. Craton, J. D. Albrecht and J. Papapolymerou, *"Ultra-Wideband Transmission Lines on Complex Structures via Extendable Aerosol Jet 3D-Printing,"* 2021 IEEE International Conference on Microwaves, Antennas, Communications and Electronic Systems (COMCAS), 2021, pp. 103-106, doi:10.1109/COMCAS52219.2021.9629015.

- **Xenofon Konstantinou**, Michael Thomas Craton, John D. Albrecht, and John Papapolymerou, *"Aerosol Jet 3D-Printed Compact EBG Resonators"*, 2021 IEEE 71st Electronic Components and Technology Conference (ECTC), 2021, pp. 2308-2313, doi:10.1109/ECTC32696.2021.00361.

- M. T. Craton, **X. Konstantinou**, J. D. Albrecht, P. Chahal and J. Papapolymerou, *"Additive Manufacturing of a W-Band System-on-Package"*, in IEEE Transactions on Microwave Theory and Techniques, doi:10.1109/TMTT.2021.3076066.

- Sang June Cho, Dong Liu, Aaron Hardy, Jisoo Kim, Jiarui Gong, Cristian J. Herrera-Rodriguez, Edward Swinnich, **Xenofon Konstantinou**, et al. *"Fabrication of AlGaAs/-*

GaAs/diamond heterojunctions for diamond-collector HBTs", AIP Advances 10, 125226 (2020); https://doi.org/10.1063/5.0027864.

- **Xenofon Konstantinou**, Michael Thomas Craton, Cristian J. Herrera-Ridriguez, Aaron Hardy, John D. Albrecht, Timothy Grotjohn, and John Papapolymerou, *"A Monolithic RF Lowpass Filter on Diamond via Additive Manufacturing,"* 2020 IEEE USNC-CNC-URSI North American Radio Science Meeting (Joint with AP-S Symposium), 2020, pp. 123-124, doi:10.23919/USNC/URSI49741.2020.9321615.

- **Xenofon Konstantinou**, Cristian J. Herrera-Ridriguez, Aaron Hardy, John D. Albrecht, Timothy Grotjohn, and John Papapolymerou, *"High-Power RF Characterization of Diamond Schottky Barrier Diodes at X-band,"* 2020 IEEE/MTT-S International Microwave Symposium (IMS), 2020, pp. 297-300, doi:10.1109/IMS30576.2020.9223773.

- Michael Thomas Craton, **Xenofon Konstantinou**, John D. Albrecht, Premjeet Chahal, and John Papapolymerou, *"A Chip-First Microwave Package Using Multimaterial Aerosol Jet Printing,"* in IEEE Transactions on Microwave Theory and Techniques, vol. 68, no. 8, pp. 3418-3427, Aug. 2020, doi:10.1109/TMTT.2020.2992074.

- **Xenofon Konstantinou**, John D. Albrecht, and John Papapolymerou, *"Using Active Load-Pull with Modulated Signals to Optimize Power and Linearity,"* 2020 94th ARFTG Microwave Measurement Symposium (ARFTG), 2020, pp. 1-4, doi:10.1109/ARFTG47584.2020.9071645.

- **X. Konstantinou**, C. J. Herrera-Rodriguez, M. T. Craton, A. Hardy, C. Crump, J. D. Albrecht, Q. H. Fan, T. Grotjohn, and J. Papapolymerou, *"A Monolithic Wilkinson Power Divider on Diamond via a Combination of Additive Manufacturing and Thin-Film Process,"* 2020 IEEE Radio and Wireless Symposium (RWS), 2020, pp. 201-204, doi:10.1109/RWS45077.2020.9050128.

- D. Liu, S. J. Cho, A. Hardy, J. Kim, C. J. Herrera-Rodriguez, E. Swinnich, M. A. Baboli, J. Gong, **X. Konstantinou**, J. Papapolymerou et al., *"Toward Diamond-Collector Heterojunction Bipolar Transistors via grafted GaAs-Diamond n-p junction,"* 2019 IEEE BiCMOS and Compound semiconductor Integrated Circuits and Technology Symposium (BCICTS), 2019, pp. 1-4, doi:10.1109/BCICTS45179.2019.8972766.

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