TRANSFERABLE MILLIMETER-WAVE STRUCTURES AND PACKAGES USING AEROSOL-JET PRINTING

By

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ABSTRACT

IC packaging is a critical factor in emerging next generation RF and mmWave systems design. As demand for higher data bandwidth and greater device connectivity increases, methods for developing low cost and high quality RF systems in the mmWave range and beyond must be developed and improved upon. Many traditional manufacturing techniques have been iterated on to address this issue, but most run into a hard limit in terms of RF performance and the ability to miniaturize heterogeneously integrated architectures into cost effective packages.

Additive manufacturing (AM) offers emerging processes that may be used to address these issues, providing solutions that are low operating cost and flexible to a wide range of design geometries. Some high performance designs that are difficult or unavailable with traditional manufacturing techniques may be realized using AM, extending the use of more robust IC packaging to high frequency applications.

This dissertation presents engineering advancements in the field of RF and mmWave systems manufacturing through the use of AM techniques. Chip-in-Pocket (CiP) IC packaging is investigated, including the impact of printed die fill materials and interconnects on RF system performance at Ku-band. Printed die attach techniques and their effect on the reliability of printed interconnects and die leveling are explored. Finally, a processes for transferring printed RF components and packages from the printing substrate to other surfaces will be demonstrated for Ku to Ka-band components as a means to improve manufacturing reliability of systems leveraging AM components and demonstrate the efficacy of combining AM components with traditional manufacturing. Aerosol-Jet Printing (AJP) is leveraged as the main AM method for high precision RF structures including IC interconnects and vias, all the way up to full IC packages that may be applied to PCB pad layouts.

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To my parents, who taught me that knowledge and understanding are our greatest strengths.

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CHAPTER 1

AEROSOL-JET PRINTING FOR MILLIMETER-WAVE STRUCTURES

1.1 Introduction

Radio Frequency (RF) microelectronics are an ever present component of our modern communication infrastructure. It is what enables the massive flow of data carrying voice, images, videos, documents, and more between millions of devices at every moment of every day. As networked devices become smaller and more numerous, the implementation of communication hardware must become more efficient and robust. This will require significant overhauls to the way that key components are manufactured, packaged, and operated. Larger data throughput demands higher bandwidth, in turn requiring higher operating frequencies and pushing the capabilities of modern electronics manufacturing beyond their limits. New semiconductor technologies and methods of integrating them into existing and next generation communication environments will need to be developed, putting higher than ever requirements on packaging technology. Increased device count and density means more infrastructure and higher power consumption across the board, making efficient operation an important factor in the next generation of communication systems.

While device technology races ahead, one of the main sources of signal reduction on the board is the IC packaging. This interface between the IC and the outside world can contribute to lowering the power output or signal integrity in a variety of ways. Package interconnects represent both an impedance matching and a mode shape matching challenge, generally being considered the largest source of signal degradation in a mmWave IC package[1, 2]. Various grounding strategies both at the die ground interface and the RF signal pads on lead frames affect thermal path and signal integrity respectively. Encapsulation methods necessary to protect the IC from its external environment have a subtle influence on RF performance through dielectric loading. All of these factors vary from method to method, and each new innovation extends the range of operating frequencies and power handling capabilities a little bit further.

Many strategies have been developed to bring the other RF system components closer to the die

to reduce signal losses, such as antenna-in-package (AiP) [3, 4], antenna-on-chip (AoC) [5], and system-on-package (SoP) [6, 7, 8]. Many examples of the application of additive manufacturing (AM) to these packaging techniques have been cropping up in recent years, opening the door for the use of these technologies to create packages that operate well above the Ka-band. With further development, AM technologies offer a pathway to manufacturing package and system geometries that are not easily realizable using traditional manufacturing techniques.

This dissertation presents advancements in the use of high precision AM for the development and fabrication of RF and mmWave IC packaging. New processes are developed and characterized which leverage the specific advantages of AM over traditional manufacturing techniques for complex RF system assemblies, and methods of integrating these processes into existing RF system environments are explored. Impacts of the AM processes on signal characteristics are measured to show the efficacy of the approach for future manufacturing.

1.2 Aerosol-Jet Printing

Aerosol-Jet Printing (AJP) is an emerging additive manufacturing technology with the potential to contribute previously unavailable capabilities to the RF microelectronics manufacturing pipeline. In recent years it has been used for IC interconnect deposition [9], thermoplastic functionalization [10], sensor electrodes [11], wideband power dividers [12], high frequency passive devices [13], and all manner of IC packaging strategies [14, 15, 16, 17]. It is a direct-write technology, meaning that material is deposited from a nozzle directly onto a surface to build a part. This most commonly refers to the ability to "write" a PCB style circuit layout to a dielectric or other supporting surface with a metal ink, typically silver nanoparticle based. It is not limited to this application however, and can be used to fabricate a wide range of 2.5D or 3D structures due to a comparatively large nozzle stand-off distance of 2-6mm. Indeed, several times throughout this work structures such as elevated MMIC die pockets or air-gap layer supports will be demonstrated. These are features that would be challenging to print with other typically mentioned direct-write systems such as ink-jet printers. AJP also allows for a wide range of ink viscosity due to the different atomization methods, and is generally less sensitive to ink formulation. In several cases, commonly used materials in

semiconductor processing such as passivation layer materials or photo-resists are simply diluted in whatever solvent they typically contain and are immediately usable in the machine. Of course specially tailored inks do perform better, often with less overspray and improved repeatability, but the flexibility and adaptability is a major benefit for those looking to push the state of the art at a rapid pace.

The system used in this work was an Optomec AJ-5X aerosol-jet printer, a schematic of which is shown in Fig. 1.1. This system is equipped with both a pneumatic and ultrasonic atomizer for use with high viscosity inks (0-1000cP) and low volume, low viscosity inks (0-100cP) respectively. Once aerosolized, the aerosol stream is directed the print head where it is focused through the print nozzle using a nitrogen sheath gas.

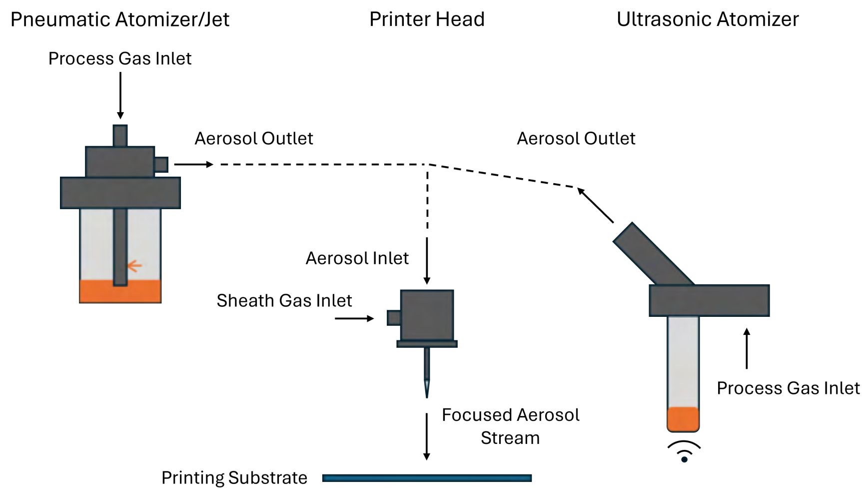


Figure 1.1 A diagram of the Optomec AJ-5X aerosol-jet printer.

Additional features of this machine include a jar heater for lower ink viscosity thermally in the pneumatic atomizer, a platen heater for adjusting the viscosity of deposited materials once on the printing substrate, and a UV lamp mounted to the print head which may be used to cure UV sensitive materials as they are deposited during printing. These variables, combined with the ability to adjust the process and sheath gas mass flow rates, leave a wide range of process conditions to optimize for whatever ink is required for fabrication.

AJP does come with several drawbacks, for example the difficulty associated with developing process parameters for a given ink on a new system [18]. Process parameters can drift from session

to session, and can even vary significantly during a single print session due to buildup of material in the machine components. For this reason, it also has relatively high maintenance requirements, necessitating a full cleaning of aerosol-handling components after nearly every print session and a full clean out of the exhaust lines for pneumatic atomizers on a regular basis. The generation of overspray, caused by particles escaping the sheath gas stream after leaving the deposition head [19], is also a concern. This can make it difficult to properly delineate where the edge of a printed line or substrate is, and can even cause electrical shorting in the worst case. Finally, closed loop control schemes for this process are still very much an active area of research for AJP. Currently existing control loops involve reading the mass flow and pressure of the sheath and process gases, but these do not always correlate well with the amount of material that is output from the nozzle. Some groups are working on methods to measure the aerosol stream for better control [20], but these techniques have yet to make their way into commercial systems.

AJP is most often compared to ink-jet printing for both its similar mode of operation and overlap in fabricable geometries. Many MS structures and even interconnects [21, 22, 23] have been fabricated using ink-jet printing, and it is a competitive process. One disadvantage of ink-jet printing is a relatively low stand-off distance and a lower range of compatible ink viscosity [24]. This limits both the range of materials that may be used as inks for these systems, as well as preventing them from easily depositing materials on surfaces with 3D geometries like ramps and curves. Another process worth comparison is SLA printing, an AM method where a UV layer image is created with an LCD or DLP focusing optic. Several interesting structures are possible using SLA printing, including microfluidic sensors [25] and mmWave package structures [26], but these processes are generally limited to UV settable dielectrics with no way to reasonably place surface conductors without relying on other methods.

For this work, AJP is the most attractive choice due to the ability to deposit materials around relatively tall objects such as dies or SLCs, and its superior resolution to most other currently available AM methods. The ability to print a wide range of materials using a single process limits the problems that arise at the boundaries when trying to combine one or more techniques.

Additionally, the range of feature sizes available with different nozzle sizes make it possible to fabricate most aspects of complex systems such as die packages.

CHAPTER 2

USING AJP IN RF SYSTEMS

Among the many AM technologies, aerosol Jet Printing (AJP) is attractive for RF circuit fabrication due to its ability to deposit materials (inks) with high resolution on both planar and non-planar structures. AJP has the advantage of high print resolution (10μm), the ability to deposit inks with wide range of viscosity, and a large stand-off distance of the nozzle from the substrate (2-6mm) which allows for the deposition of a wide range of materials on complex geometries. This chapter contains and expands on the work found in [27].

2.1 Chip-in-Pocket RF Tone Generator

RF and mmWave systems can leverage many semiconductor technologies, and an approach that allows heterogeneous integration of these components within a small footprint is desired to meet the challenge of the next generation of systems. Additive manufacturing has been applied to several chip integration techniques for RF applications in recent years, including: (i) chip in pocket [28], (ii) embedded devices [29]; (iii) chip on board with interconnect ramp [30] and (iv) chip first [31]. These techniques allow the assembly of many devices within a small foot print with low interconnect losses. Among all these, the chip in pocket technique is attractive as it takes advantage of conventional lithographic fabrication for large area fabrication and AM for the fine features at the chip-board transition, such as low loss interconnects with minimal parasitic inductance and the supporting die fill material.

For RF and mmWave circuits, materials of interest tend to be low loss dielectrics and high conductivity metals. Low loss printed silver (Ag) ink and benzocyclobutene (BCB) have been demonstrated recently [32]. BCB has the desired properties needed for the fabrication of RF and mmWave circuits, including: (i) self-planarization, (ii) low dielectric constant and loss (2.5 and 0.002), (iii) good wetting to GaAs and InP, (iv) good adhesion to most organic and inorganic substrates, and (v) low thermal expansion (CTE = 42 ppm/°C) [33]. The BCB ink used in this process is Cyclotene 3022-35 purchased premixed with a mesitylene solvent from Dow Chemical, Inc. It is 35 wt.% BCB by weight, with the remaining 65 wt.% being composed of solvent

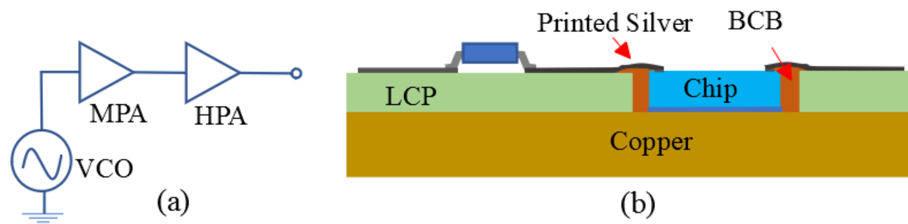


Figure 2.1 (a) Transmit module design; (b) Package design.

(mesitylene). The silver nanoparticle ink used is composed of 25 wt.% (Clariant Prelect TPS 50) in deionized water. Building upon the work in [32], here a functional Ku-band transmitter module with high power output is demonstrated utilizing a hybrid process which combines standard lithographic circuit fabrication with AJP.

2.1.1 Fabrication

2.1.1.1 Process

A Ku-band transmit module with two stage amplification was fabricated, the schematic of which is shown in Fig. 2.1a. The circuit utilizes both COTS packaged components and AJP integrated bare dies. Analog Devices' HMC451 GaAs pHEMT MMIC Medium Power Amplifier (MPA) is used for the first stage, and the Qorvo TGA2958 13-18 GHz 2W GaN driver amplifier is used for the second stage high power amplification (HPA). The voltage controlled oscillator used is the HMC632LP5 MMIC VCO from Analog Devices.

The circuits were fabricated on a 3 mil Liquid Crystal Polymer (LCP) laminated to a copper carrier plate. The unpackaged amplifier dies are mounted inside the pocket formed in LCP and packaged components are solder mounted to the copper pads on the surface. An illustration of the surface mount and pocket mount components is shown in Fig. 2.1b. Fig. 2.2 shows the process flow for the fabrication of this circuit. Pockets and vias in the LCP and acrylic bond ply were formed using a CO2 laser cutting system before lamination to the carrier plate. The LCP is then fixed to the copper backing plate using the 1 mil acrylic bond ply by sending the aligned assembly through a heated lamination roller. The amplifiers are then placed in the pocket, attached using conductive epoxy between the copper backing and the ground plane of the amplifier chip.

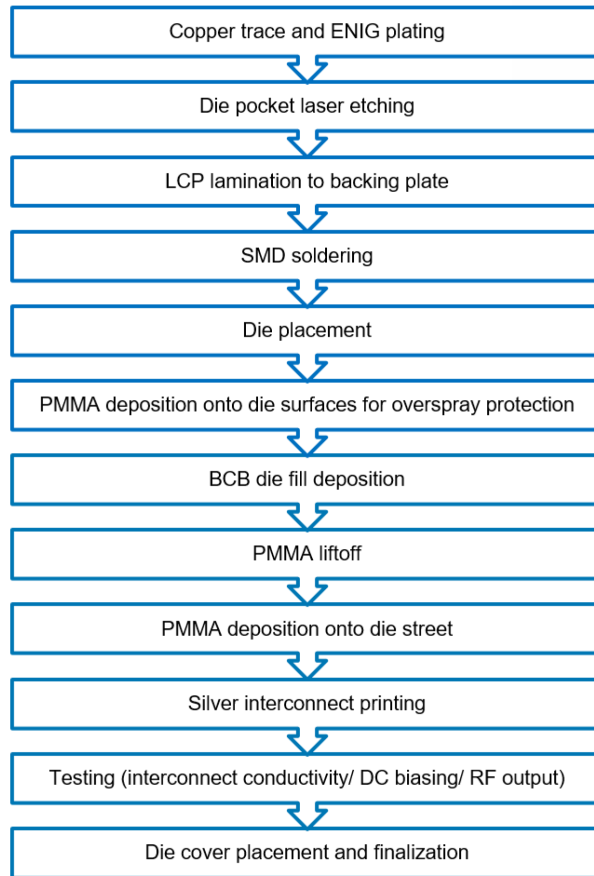


Figure 2.2 Flowchart describing the RF Transmit module fabrication.

Using AJP, a temporary layer of Poly(methyl methacrylate) (PMMA) is selectively deposited on the surface of the unpackaged amplifiers. BCB is then deposited into the spacing around the die as a die pocket fill material to provide structural support for both the die and the silver interconnects. The PMMA film protects the amplifier from die fill material overspray, providing a layer where BCB droplets are caught and can be rinsed away with the PMMA film when acetone is applied. The BCB is cured in a nitrogen oven at 180 °C for 20 hours, following the steps suggested in the data sheet [33]. This extended cure at a lower temperature is to prevent delamination of the LCP film from the copper backing plate due to the low melting temperature (200°C) of the bond ply. Once the BCB is cured, the PMMA die cover is removed with an acetone rinse. A thin strip of PMMA is printed along the outer perimeter of the die to cover the unpassivated die street region. This prevents the interconnects from contacting the street and creating an unwanted conductive short or diode effect. The interconnects are then printed using a silver nanoparticle ink, and are sintered in an oven

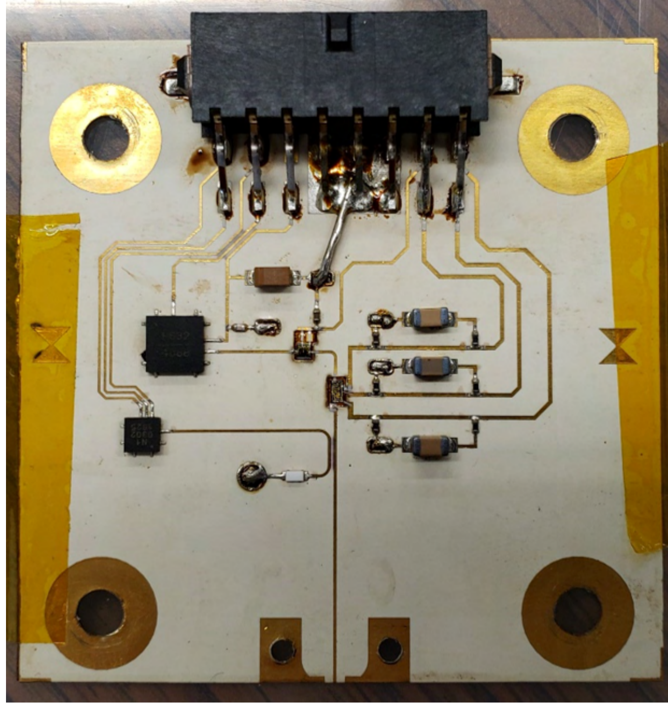


Figure 2.3 The completed Ku-band transmit module.

at 180 °C for 6 hours. Fig. 2.3 shows the finished board. Post processing microscope images of the MPA (PA1) and HPA (PA2) dies are shown in Fig. 2.4.

PMMA is also useful for smoothing out physical discontinuities at the die pocket edge or on the PCB to facilitate interconnect deposition. The PCB traces for a board using a 1oz. copper pour are on the order of 35μm thick, which can cause disconnections for printed interconnects that are on the order of 3-5μm thick. Fig. 2.5 shows an example of this use case.

2.1.1.2 Benefits and Challenges

One advantage of using unpackaged components at this frequency is the minimization of material between the heat generating die, in this case the amplifiers, and the heat sink. Epoxy Technology's EPO-TEK H20E-FC electrically conductive epoxy is used to attach the unpackaged components to a copper backing plate. This provides a shorter thermal path to the heat sink, which improves our ability to run active devices at higher power for longer duration.

As mentioned, BCB as a material has many benefits in mixed technology circuitry. The self-planarization of the material for instance, which is shown in Fig. 2.6. However, AJP deposition of BCB does produce a large amount of overspray. Overspray can occur during relatively heavy

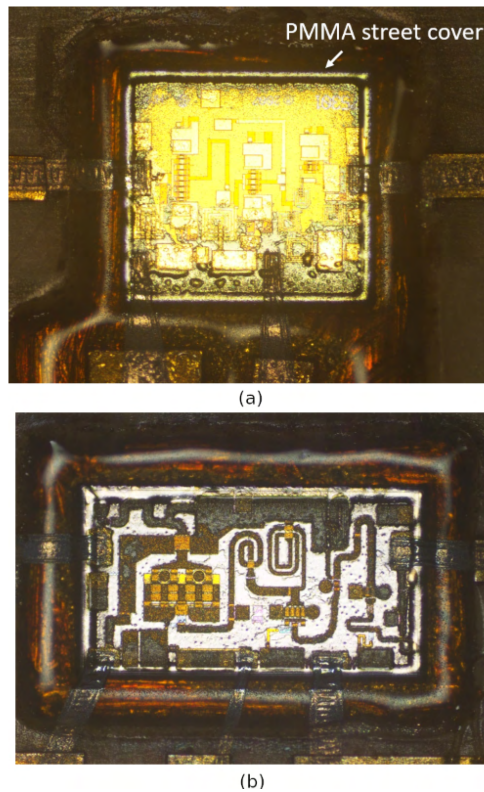


Figure 2.4 (a) Microscope image of the filled and connected HPA and (b) Microscope image of the filled and connected MPA.

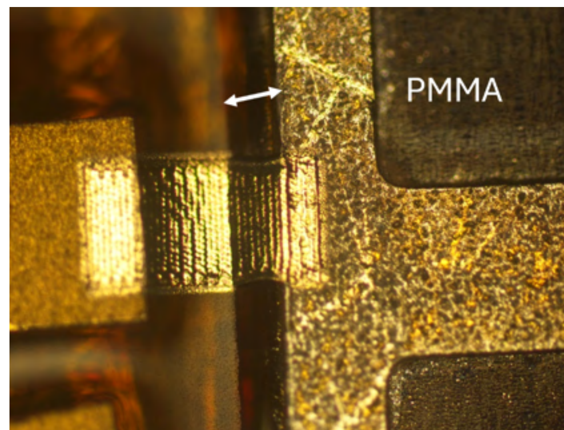


Figure 2.5 The PMMA ramps used at the die edge are also useful for smoothing out large steps in height at the PCB, including discontinuities at the die pocket edge and the PCB traces.

depositions, leading to a large number of droplets accumulating on the die surface and, more importantly, on the pads. This can make it difficult to form a good connection between the pad and the silver interconnect. An example of this with a comparison to a clean die surface is shown on a 5 dB attenuator test die in Fig. 2.7.(a). Our proposed solution to this problem is the AJP PMMA

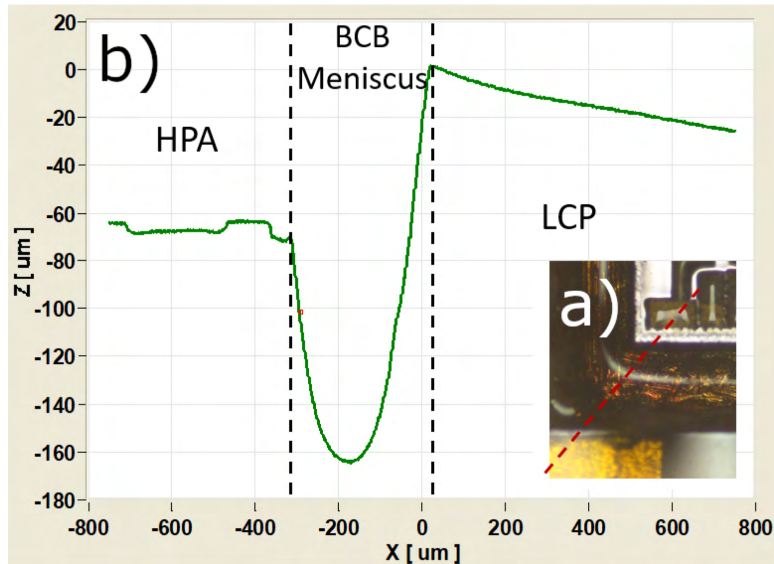


Figure 2.6 (a) Optical image of profilometer scanline across the BCB fill along HPA drain interconnect. (b) Graph of profilometer scanline.

cover film layer that is deposited onto the die before BCB fill to collect the overspray droplets as shown in Fig. 2.7.(b). This cover layer is then removed via an acetone rinse once the BCB has been cured and the fill level has been verified with a profilometer measurement. The thickness of this cover layer and the material of the die substrate and surface conductors can affect the ability to fully remove this layer. Further study of thickness and cover material variation is warranted to reduce the amount of residue left over on the die to an acceptable minimum.

Some errors that can occur in the BCB fill region are bunching and receding. Bunching (Fig. 2.8) can occur during a high temperature cure due to bubbling of the mesitylene solvent left over in the material after deposition. The simplest way to overcome this is to cure the BCB at a lower temperature for a longer period of time (150-180C for 24hrs). This does run the risk of damaging temperature sensitive components or bindings in the PCB however, and can lead to the second issue for board stack ups with a fragile lamination ply layer. The second issue, receding, may be caused by mesitylene bubbling, but is also caused by incomplete lamination around the die pocket edge. This creates a space for the BCB material to flow out of the die pocket, causing voids or even the complete relocation of the material to the space between the PCB and the metal carrier plate. An example of receding caused by bubbling is shown in Fig. 2.9.

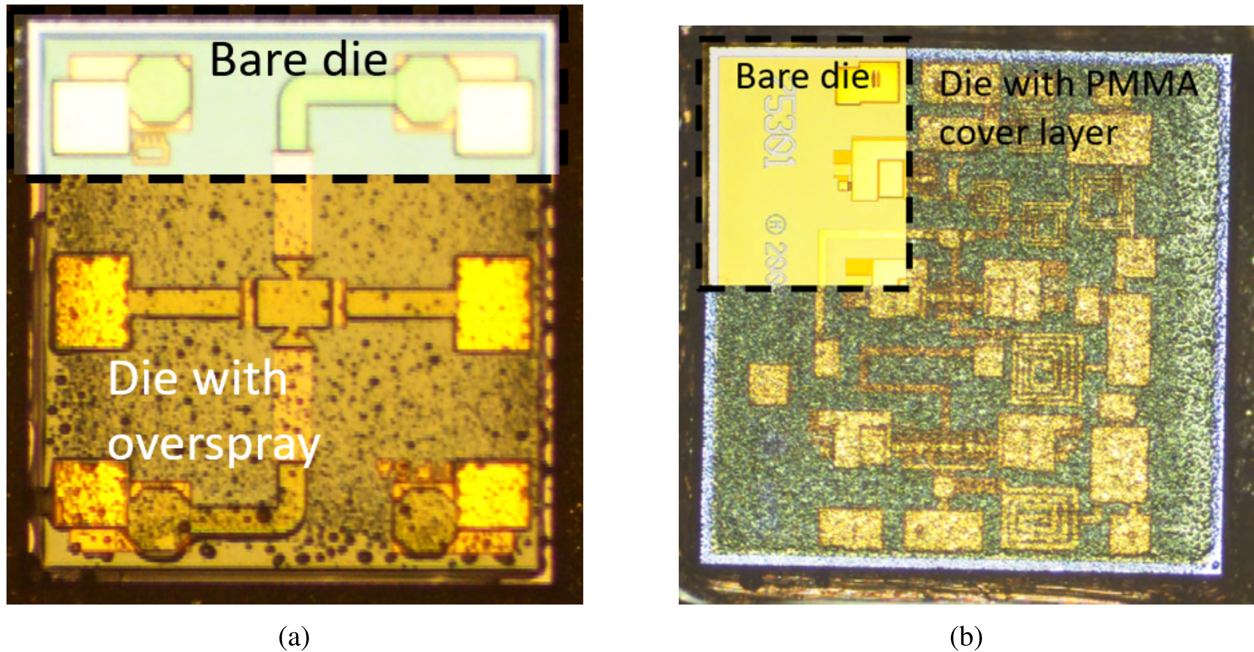


Figure 2.7 (a) BCB overspray comparison on a 5 dB attenuator test die. (b) MPA with PMMA overspray cover applied.

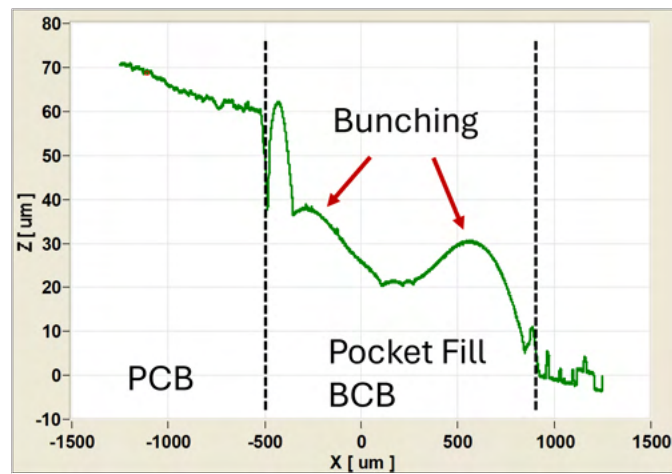


Figure 2.8 Profilometer scan of BCB bunching in die fill region.

These pocket fill material fabrication errors can be especially problematic at the die edge. Since the printed interconnects depend on physical support across the gap between the die and the PCB, unexpected fill material behavior may lead to structural discontinuities at corners of height steps. An example of this effecting the interconnect integrity is shown in Fig. 2.10, where a low fill around the MPA die created a sharp corner at the die edge causing the interconnect to break. This can be difficult to detect until interconnect deposition due to the transparent nature of the fill material, and

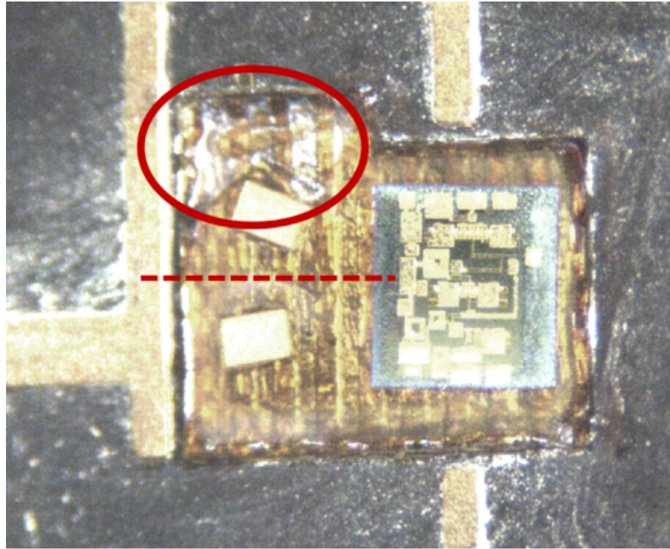


Figure 2.9 The BCB die fill material in a large MPA pocket has receded due to material shrinkage and bubbling during the curing cycle.

is a major contributor to low process yield. This may be mitigated during the street passivation step by adding extra PMMA around the die to form a short ramp down to the fill material surface, but only if this issue is caught before interconnect deposition and the fill material does not undergo significant physical shifting during the silver sintering cycle (this is usually the case but is not guaranteed).

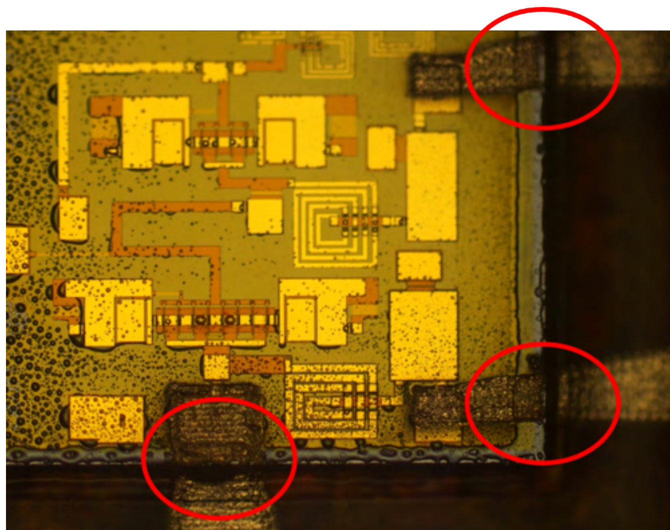


Figure 2.10 Interconnect failure due to physical discontinuity at the MPA die edge.

Another potential problem arising from the nature of a surface contacting interconnect is the

conductivity of the die street and edge (unpassivated region of the chip). Here, PMMA guard layer of several micrometers thick around the outside edge of the die is used to cover the unpassivated regions. This layer is explicitly pointed out in Fig. 2.4 (a). Issues can occur during silver sintering, or any post processing cycle that brings the temperature above the PMMA melting point of about 180C, where pinholes will form in this street passivation layer. This can cause the interconnect to contact the die street which leads to a parasitic diode effect as described in [32]. An example of such pinhole formation is shown in Fig. 2.11, where PMMA passivation has not distributed evenly during heating causing both pinhole formation and a physical discontinuity at the die edge.

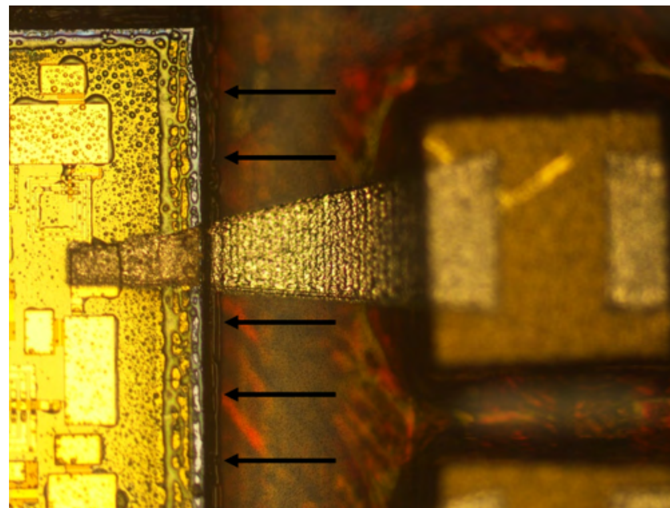


Figure 2.11 Pinhole formation in the PMMA die street passivation layer caused during silver sintering above the PMMA melting point.

2.1.2 Measurement

Here we present the power output of the transmit module. The focus is on the second stage high power amplifier where the most biasing control and output power variation may be realized. HPA drain current draw and the output center frequency for both devices are compared in Fig. 2.13. The current draw varies from 400-450 mA and is consistent with the datasheet's given maximum draw of 576 mA, indicating that there are no unexpected sources of power dissipation such as electrical shorting or resistive losses in the silver interconnects. The center frequency also matches the manufacturer data for the surface mount VCO chip.

The circuit is operated at recommended power supply biasing values for all chips excluding

biasing conditions for the HPA. The HPA is run at a gate voltage of -3V and a drain voltage of 20V. The RF output of the system is connected to a Keysight Fieldfox spectrum analyzer and measured at 1V intervals on the tuning voltage of the VCO from 2V to 13V.

Additionally, an SMD variant of the RASR board (Fig. 2.12) was fabricated for direct comparison with the AJP version of the board. Output power measurements were taken using the same equipment and are plotted alongside the measurements from the AJP board in Fig. 2.14. The output power for the AJP board is between 31.5 and 33 dBm, and shows similar performance to the SMD variant and good agreement with the manufacturer test data (wire-bonded). One thing to note is that manufacturer testing of the HPA is run at a higher gate voltage of -2.7V and a lower power input of 12 dBm. The surface mount variant of the circuit tends to output 1 to 2 dBm higher than the AJP version.

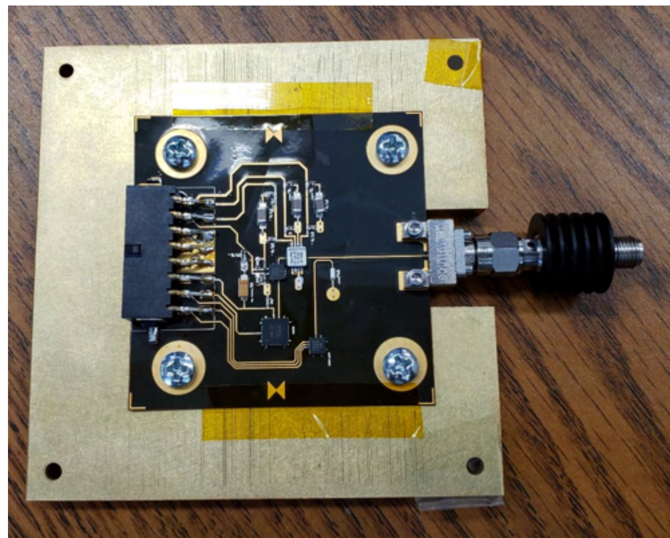


Figure 2.12 Surface mount device variant of the RASR beacon mounted to a copper heat sink.

2.2 Chip-in-Pocket RF Transmitter with IQ Mixer

An attempt to fabricate an RF transmitter board with an IQ mixing component was also carried out using the AJP chip-in-pocket method. The board was similar to the RF tone generator described above, with the addition of several extra amplifiers and an IQ mixer to facilitate IF signal injection. The first version of this was a chain of 2 boards, one containing the IQ mixer die and the other containing an amplifier chain, designed to test the compatibility of the AJP process and materials

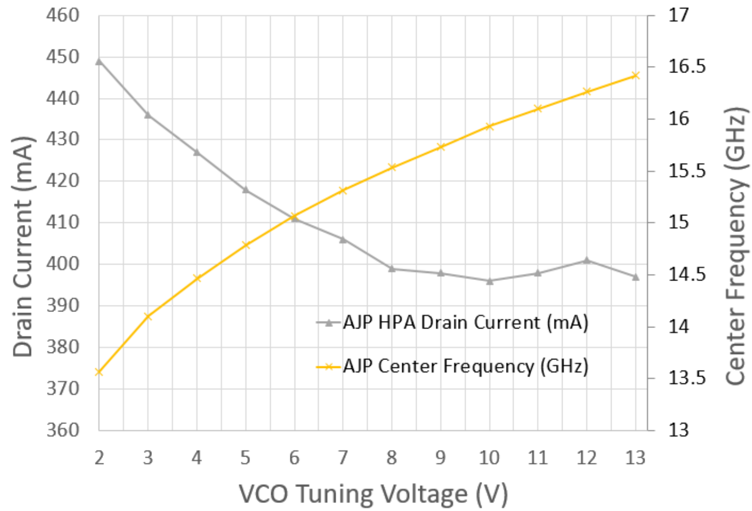


Figure 2.13 Current and center frequency measurement data for a range of tuning voltage inputs.

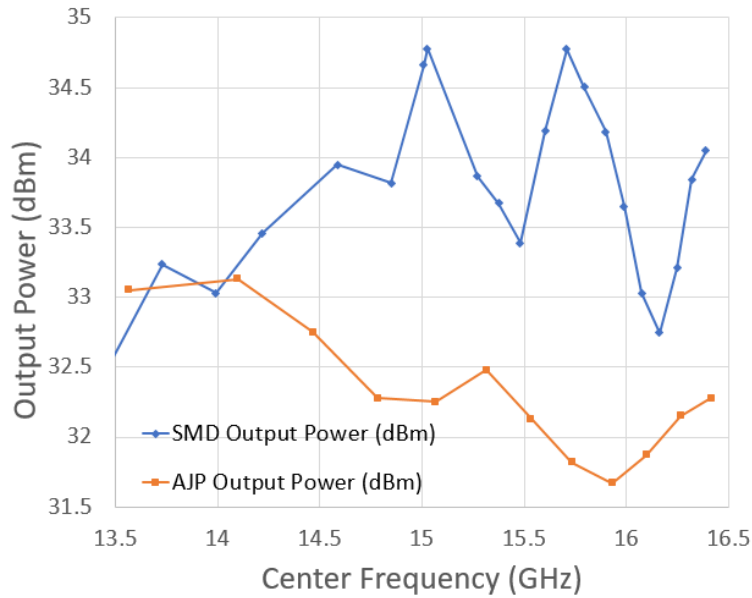


Figure 2.14 Power outputs for both AJP and SMD circuit variants.

with these components.

Fig. 2.15 shows the boards and the port connections. The IQ mixer is driven by an RF tone generator at the LO port and an arbitrary waveform generator that is fed through a 90° hybrid coupler to provide the IF signals.

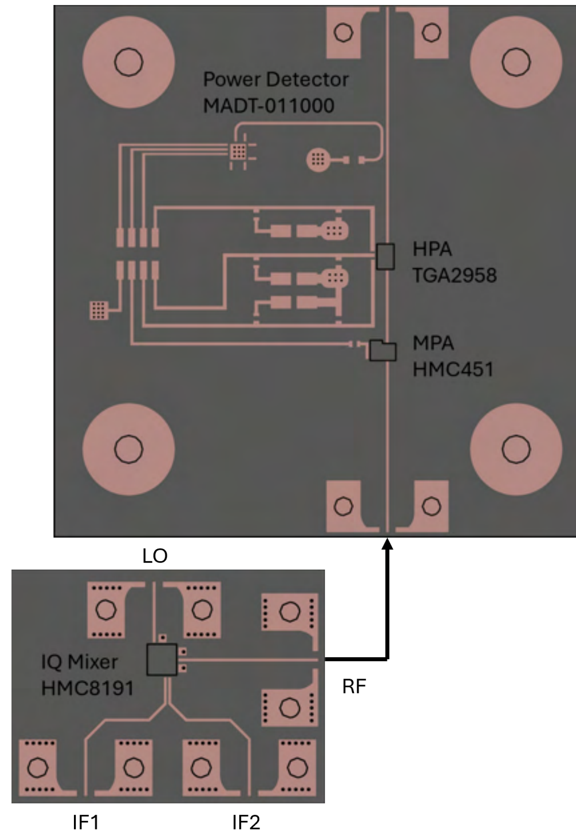
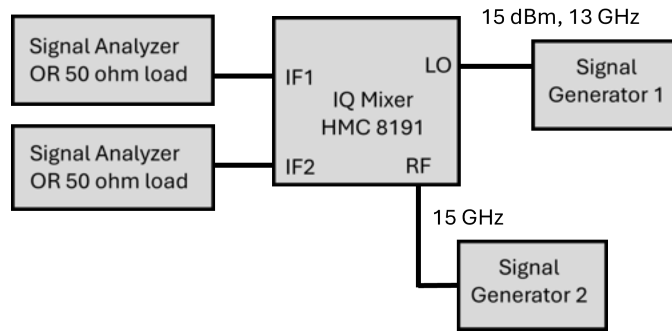


Figure 2.15 The chained IQ mixer and amplifier boards. The IQ mixer was driven by an external signal generator at the LO port and an arbitrary function generator split using a 90° hybrid coupler at the IF ports.

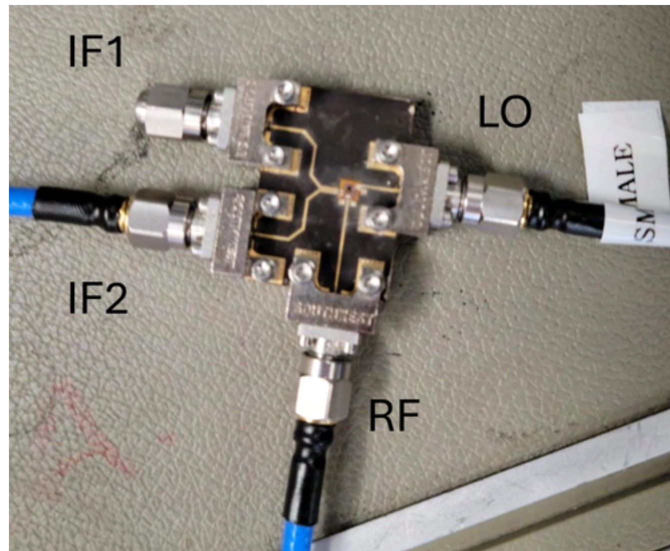
2.2.1 IQ Mixer Breakout Board

First, the IQ mixer board was tested independently to determine its compatibility with the AJP CIP fabrication process. The test bench schematic and connected IQ mixer board are given in Fig. 2.16. For this initial testing, the 90° hybrid coupler was omitted to simplify the test setup, and each IF port was tested independently with a 50 ohm terminator fixed to the inactive port.

AJP packaging the IQ mixer die presented several manufacturing challenges. The first of these was related to the BCB die fill material. As shown in [32], the performance of AJP interconnects directly benefits from a level die fill region with minimal meniscus. The acquisition of a VK3000 laser profilometer from Keyence around this time made it possible to easily take area surface scans around the die and address this issue more directly than before, including scans of the material before curing. Fig. 2.17 shows the results of such a scan around the IQ mixer die before and after



(a)

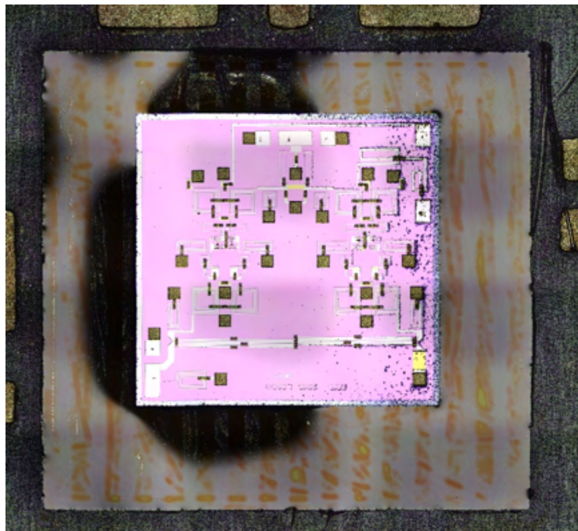


(b)

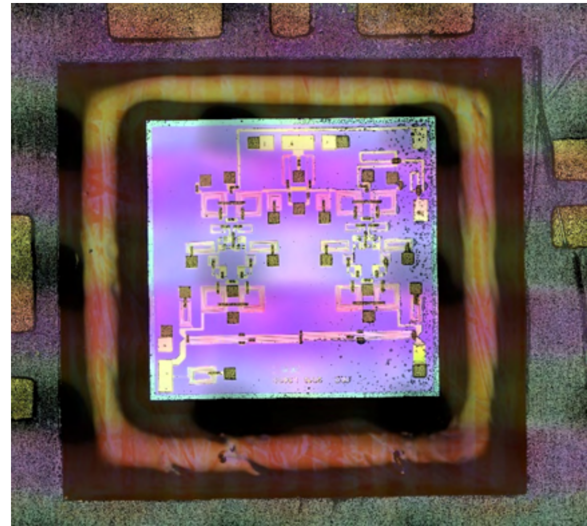
Figure 2.16 (a) The test bench schematic for the IQ mixer and (b) connectorized IQ mixer die board.

the BCB curing step, revealing an average 80um reduction in fill height at the midpoint. This is due to the deposited material containing a large percentage of mesitylene solvent that evaporates out during the high temperature curing cycle. The BCB starts as a mixture of 62% mesitylene by volume, which would correlate to a reduction roughly on par with the observed effect.

In light of this, the next attempted procedure was to simply refill the die fill region in an attempt to recover as much lost volume as possible. This was only partially successful for several reasons. The first was that the refill material was subject to the same volume loss as the first die fill pass, being that it was the exact same material. The second was an issue with the self-planarization of a small volume of the material on top of an already cured BCB layer. The AJP deposited BCB did not properly wet to the cured BCB, and significant material bunching occurred. This irregular surface



(a)



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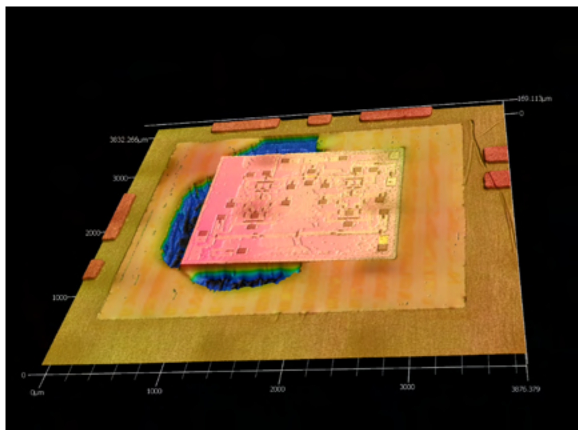
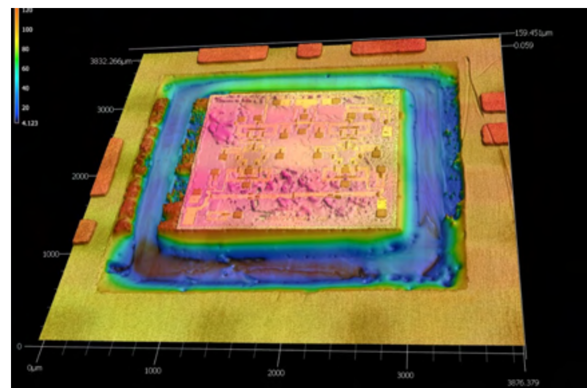


(c)

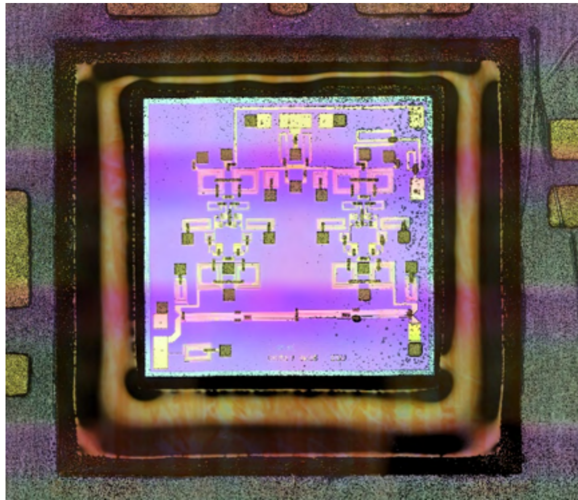


(d)

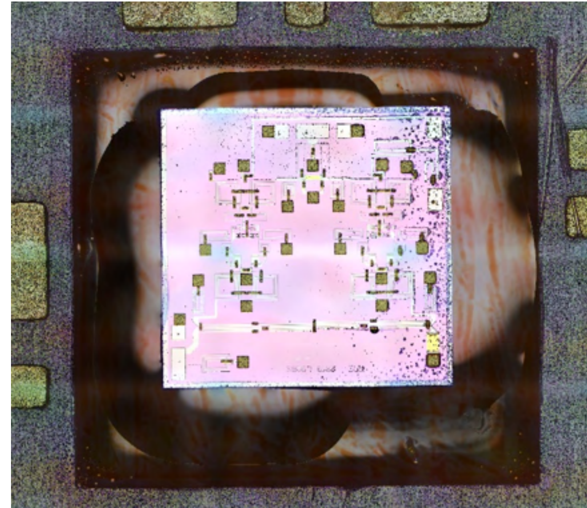
Figure 2.17 The fill level of the BCB in the IQ mixer die pocket was measured before ((a) and (c)) and after ((b) and (d)) curing the material using a Keyence VK3000 laser profilometer. A significant reduction in fill level was observed due to solvent evaporating out of the material at high temperatures.

still had edges at the die pocket PCB boundary in areas that needed to be smoothed over for proper interconnect deposition, as seen in Fig. 2.18. Finally, depositing multiple layers requires multiple thermal cycles to cure each additional layer. As the recommended range of curing temperatures for BCB is generally above 180°C, this repeated exposure to high temperatures can be damaging to both the sensitive RF dies and the EPO-TEK layer adhering the PCB to the copper carrier plate, risking delamination at the board edge or around the die pocket.

Another fabrication challenge was related to the routing of the IF2 line on the die taking the



(a)



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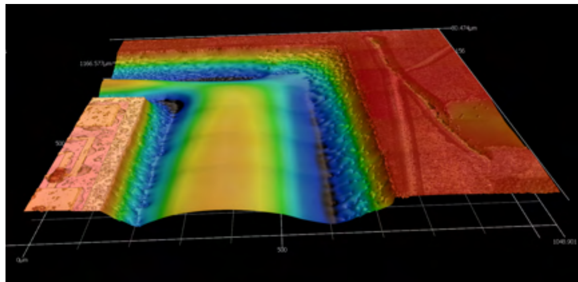

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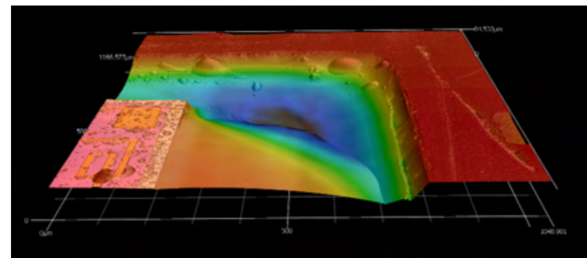


(d)

Figure 2.18 A second die fill step was performed after observing the large reduction in fill level. The material did not properly self-planarize when deposited on previously cured BCB as can be seen in (a) and (c), and significant bunching occurred during the second curing cycle as can be seen in (b) and (d).

line around the outside of the RF output pad. Since AJP interconnects contact the surface they are deposited on, this line needed to be isolated from the RF output interconnect with an insulating material at minimum. PMMA was already in use for street passivation at the time, so it was chosen as the material to isolate this line. Unfortunately this caused significant interconnect faulting and fracturing as shown in Fig. 2.19 and 2.20. This was a major contributor to low board yield, and would not be addressed until much later with the introduction of low temperature and UV curable materials (Ch. 5).

A finished AJP CIP packaged IQ mixer is shown in Fig. 2.21. This board was then connectorized and used to take the measurements of the chained boards in Fig. 2.22. While the interconnects passed DC conductivity inspections, the RF performance was still under performing compared to

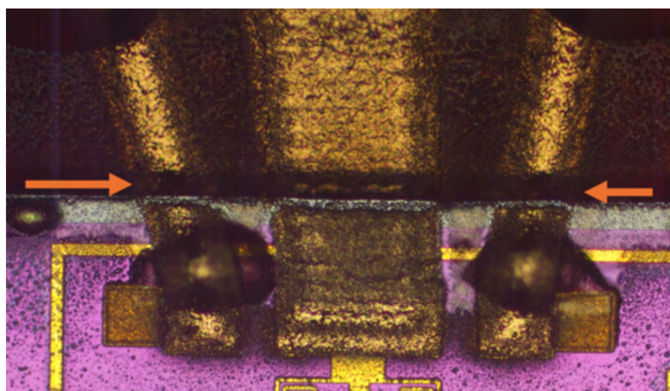


Figure 2.19 Interconnect physical discontinuity on the RF output of the IQ mixer die.

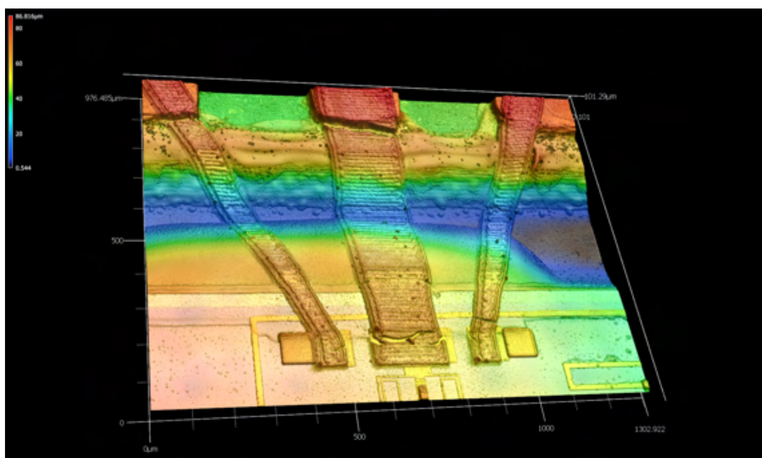


Figure 2.20 A detailed profilometer scan of the RF output including the PMMA insulated jumper shows interconnect silver cracking that occurred during sintering. This is due to the remelting point of the PMMA ink being approximately the same as the sintering temperature required, causing cracks due to shifting material under the interconnects.

the expected output by an amount not explainable by AJP inaccuracies. It was hypothesized that the board and connectors were introducing too much transmission line length, and therefor loss, which was degrading the performance of the die.

2.2.2 The Combined RF Transmitter Module

A combined board with the IQ mixer, an onboard VCO, and the amplifier chain was designed and fabricated to bring the IQ mixer closer to the rest of the components. The fully populated board, including 5 separate AJP CIP packaged Rf dies, is shown in Fig. 2.23. The inputs to this board were DC biasing lines for the VCO, both MPAs, and the HPA die and the RF ports for the IF signals. The IF signals were driven using the same AWG as was used with the IQ mixer breakout board test

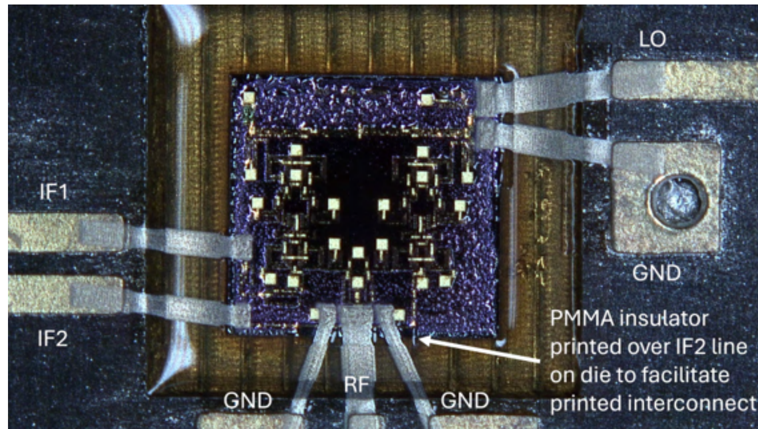


Figure 2.21 The finished AJP connected IQ mixer. Due to the routing of the die, a PMMA insulated jumper line was used to prevent the RF output from contacting the IF2 transmission line on the chip.

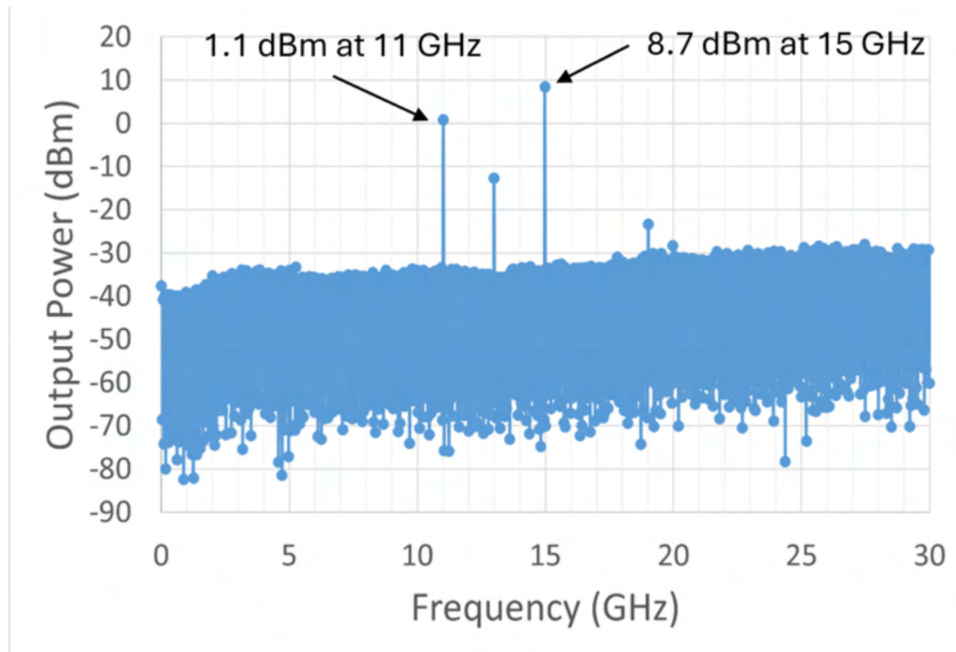
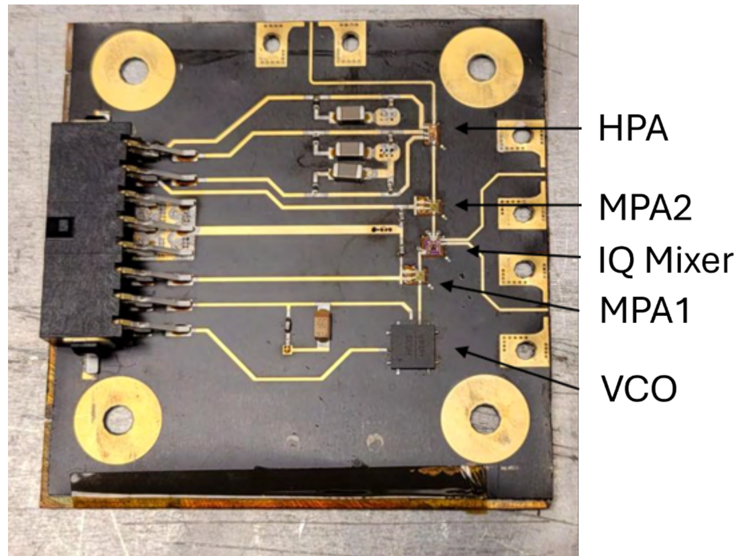


Figure 2.22 Measurements of the chained board setup taken with a spectrum analyzer. The center frequency of the output is at 15 GHz, with additional components at 11 and 13 GHz. The center frequency output power was measured to be 8.7 dBm but was expected to be closer to 32 dBm.

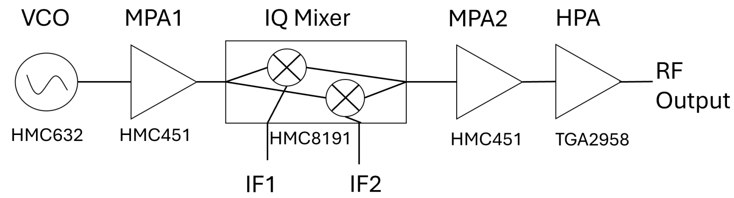
setup.

The biasing conditions were given in Table 2.1. Power output measurements were taken with a spectrum analyzer, and the results are shown in Fig. 2.24. The VCO was tuned to an output frequency of 15GHz, generating a measured power of 3.5dBm at the board RF output.

This result was approximately 30dB lower than expected, even after a thorough investigation of potential measurement error. It was determined that the yield was too low to construct a board



(a)



(b)

Figure 2.23 (a) The combined transmitter board with the IQ mixer and on board VCO and (b) a schematic of the RF signal chain.

Table 2.1 Biasing Conditions for the Combined RF Transmitter Module

Die	Vg (V)	Vd (V)	Id (mA)	IF Input Power
TGA2958	-2.7	20	85-115	-
HMC451(x2)	-	5	239	-
HMC8191	-	-	-	4.5dBm @ 2GHz

with this many components reliably due to the high temperatures required during material post processing of the AJP inks. This would go on to be a common issue in Ch. 4, and was a significant motivator to shift to UV curable and low temperature reactive inks in Ch. 5.

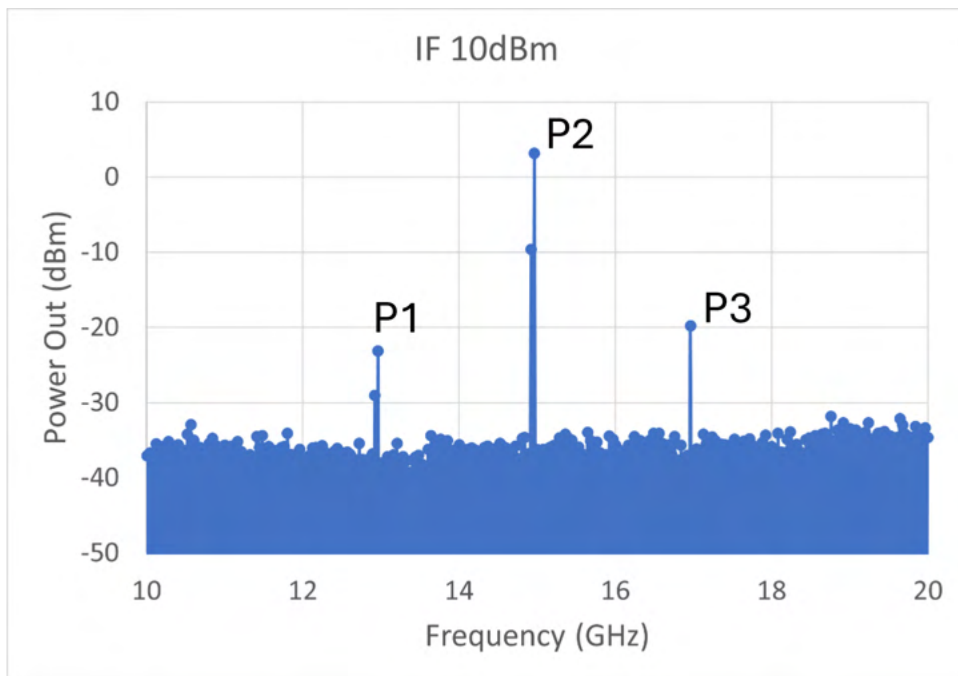


Figure 2.24 The measured power output of the combined transmitter board (P2=3.55dBm @ 15GHz). The output power at P2 was nearly 30dB lower than expected, and probing revealed issues with the MPA biasing line connections and the IF ports of the IQ mixer.

CHAPTER 3

AJP DIE ATTACH METHOD

RF systems utilizing a chip-in-pocket approach were demonstrated in chapter 2 to be a way of integrating bare die components of several different process technologies into a single RF module with good thermal management and RF properties. One of the issues with the manufacturing of these parts that greatly affects the reliability and yield is the die attach interface with the carrier metal plate. Interest in using additive manufacturing techniques to print the materials at this interface has been demonstrated in recent years [34], [35], and it has been shown that a level die surface is preferred for the reliability and longevity of mounted die systems [36]. Between CTE mismatch causing grounding failure and mechanical tilt of the die surface due to attach procedure, many of the fabricated modules from chapter 2 were lost to defects. The proposed die attach method here allows for the mitigation of both of these issues; the first by replacing the attach material with more mechanically compliant materials (BCB and silver nanoparticle ink) to reduce the impact of CTE mismatch, and the second by providing a repeatably flat surface to mount the die to, which helps reduce incidences of die fill material overflow by improving the die level after attach layer cure. This chapter contains and expands on work found in [37].

3.1 Attach Pattern Design

The attach pattern design has two main considerations; electrical/thermal conductivity and adhesion. These will largely depend on the attach materials used and the coverage of each on the bottom die surface. While the materials are fixed by the process, the exact patterning of the attach layer may be tailored to the use case. A die producing more waste heat, like an amplifier, may require a greater ratio of conductive to adhesive material to function, or special attention to ensure that the area under the transistors is all conductive material. Dies with larger areas may require a more even distribution of adhesive material to prevent chip detachment during a die pocket fill step or for applications involving a lot of thermal cycling.

Several attach patterns were attempted to determine the impact of attach layer design, both of which can be seen in Fig. 3.1. The first and most simple was a bar pattern in which alternating bars

of BCB and nanoparticle silver were deposited at a thickness of <5μ. The ratio of the widths of these bars may be tailored during printing to provide either more conductivity or more adhesion as desired. The second of these patterns was a grid pattern, where silver vias approximately 50μm in diameter were left in a BCB attach pattern. This was an attempt to spread out the conductivity more evenly across the die surface. This pattern was limited by both overspray from the BCB deposition limiting the contact between the silver and the carrier plate, and by the spread of the BCB as its viscosity reduces during the thermal curing cycle.

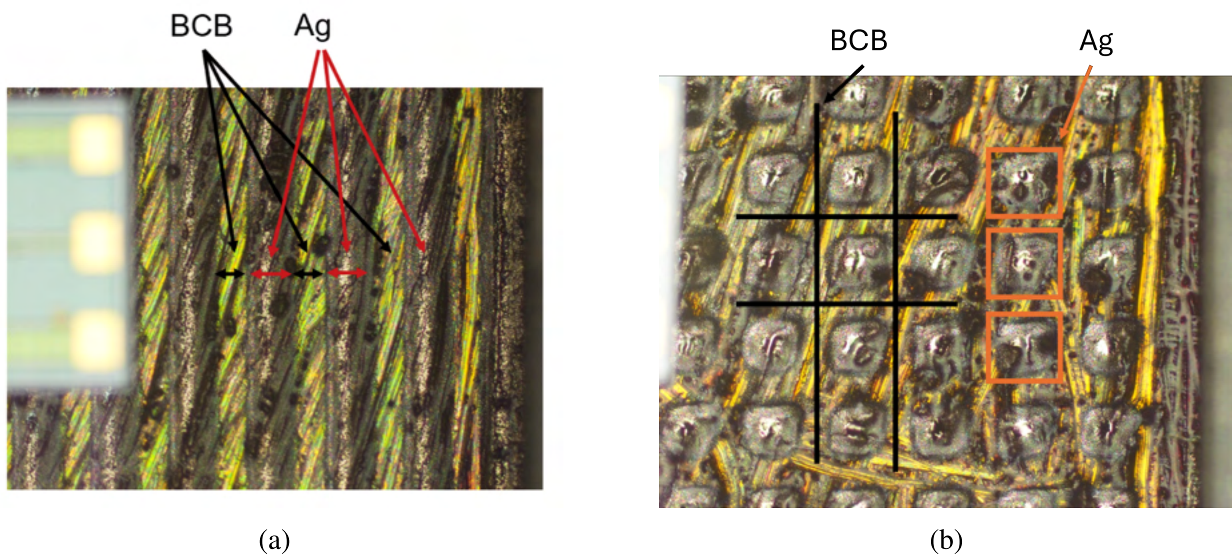


Figure 3.1 (a) A bar and (b) a grid pattern for the printed die attach method.

3.2 Process

A process flowchart for AJP die attach is given in Fig. 3.2. The steps are completed after the PCB is mounted to the carrier metal, but can also be done in other manufacturing schemes, such as chip-first [38], as a first step.

Beginning with a carrier surface prepared by either sanding or polishing, the first step in the process is to print a single layer of BCB in the chosen pattern on the carrier. After this print is completed, the conductive material (in this case silver) is printed into the gaps left in the pattern by the first step. Once the metal layer is placed, the die may be mounted to the surface. The assembly is then placed into an oven to cure at 250°C for 2 hours. This step also sinters the silver ink to bring

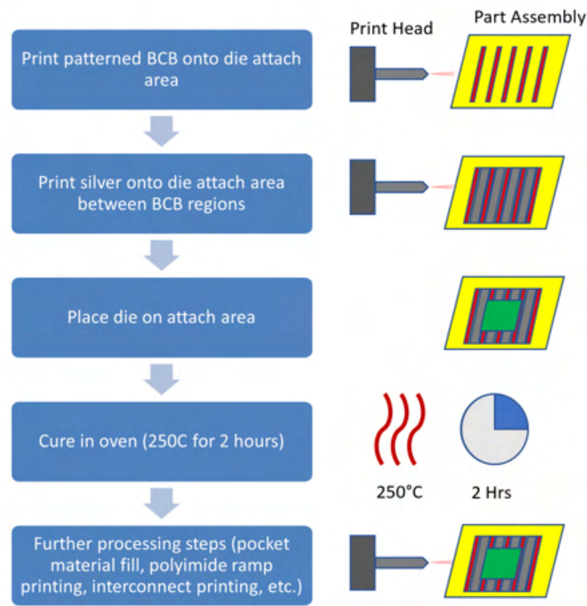


Figure 3.2 The process flow chart for PMM die attach method is shown in the figure above.

it up to the proper conductivity. Once this is complete, the assembly is ready for further processing. An example of a completed part at this stage is shown in Fig. 3.3.

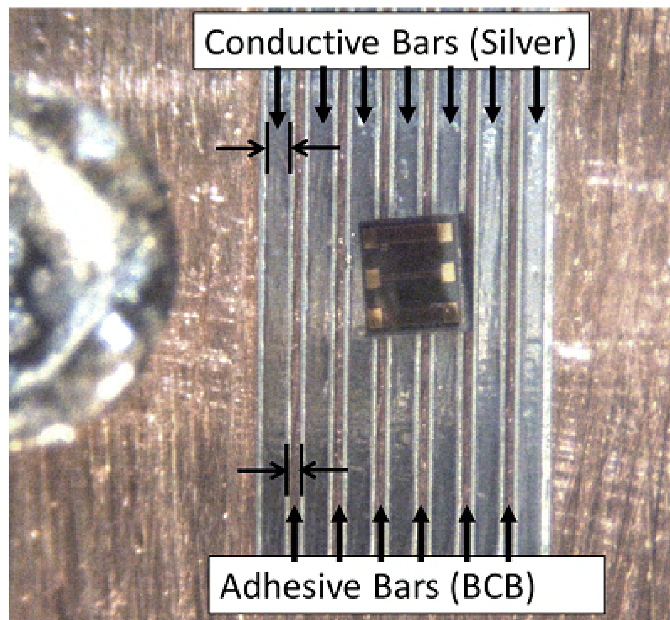


Figure 3.3 A 0 dB attenuator die that has gone through the PMM die attach process at the final step before curing. Silver and BCB bar regions are used to provide electrical and thermal conductivity and die adhesion to the carrier plate.

3.3 Fabricated Test Structures

Fabrication was focused on a bar pattern as it was the most straight forward and reliable to print. An additional pattern consisting of a grid of BCB square tiles surrounded by silver conductor was attempted, but difficulties during printing lead to lower reliability. Patterns of higher intricacy may provide benefits for specific applications, but greater care must be taken during printing to minimize the effects of overspray and ink spreading (in the case of BCB or other low viscosity inks).

3.3.1 0dB Attenuator

The method described here was first tested with 0 dB attenuator dies attached with a range of attach material bar ratios. After being attached to a copper carrier plate, an RF probe pad was deposited on the low end of a BCB ramp and a microstrip line interconnect was printed up the ramp and onto the RF pad of the attenuator die. This allowed S-parameter measurements to be taken which include the effects of the attach layer on the die as the main distinction between the measured structures. These measurements, along with the measurement setup, are given in Fig. 3.4.

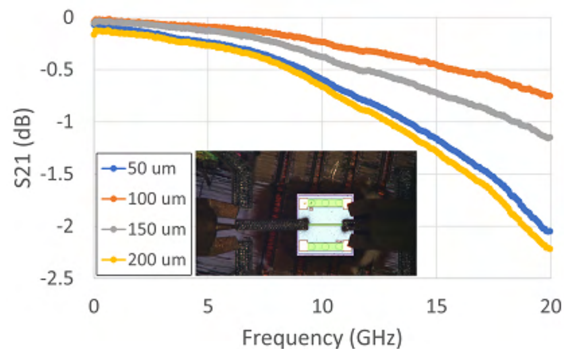


Figure 3.4 S-parameter measurements for a 0dB attenuator with off chip printed pad using the proposed die attach method are shown above. Inset image is the measurement setup. BCB width is held constant while silver width is varied from 50 to 200 μm.

Losses are shown to be less than 2 dB for the whole assembly at frequencies of 20 GHz or less. Complicating factors include the varying impedance of the probe pad line leading up to the die due to the changing ramp thickness, and the exact placement of the die itself, which could vary in conductor coverage from what is expected due to die rotation during hand placement. A minimum of 50 μm width for the adhesive lines was found to be optimal to avoid issues caused by overspray.

While no maximum adhesive line width was determined, a minimum ratio of 1:1 conductor to adhesive coverage is recommended with an even distribution of the two materials on the bottom die surface to maintain good RF grounding and thermal conductivity across the die.

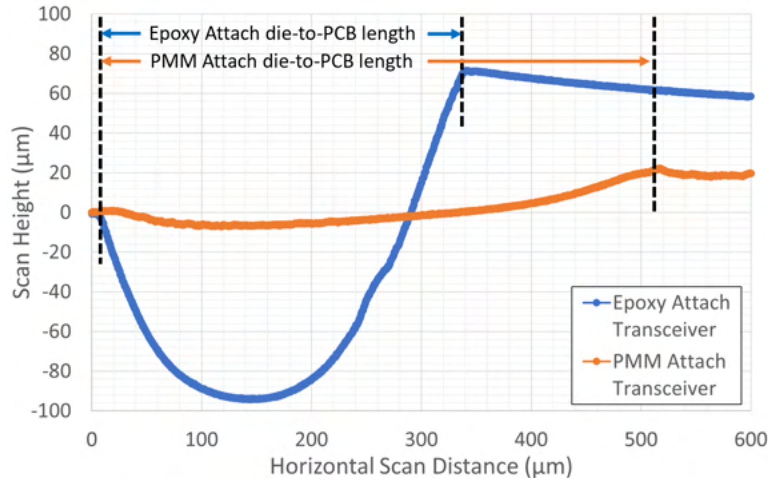


Figure 3.5 A comparison between typical die pocket fill profiles for epoxy attach methods and the PMM attach method. The under filled transceiver die using the conductive epoxy attach method is shown in blue, and the level filled transceiver die using the PMM attach method is shown in orange.

3.3.2 RF Transceiver Module

An RF transceiver was fabricated using the PMM die attach method to mount both a medium power amplifier (MPA) and a high power amplifier (HPA) with two of its in-pocket biasing capacitors (Fig. 3.6). A similar device that was previously manufactured using a standard conductive epoxy attach serves as a direct comparison for the effectiveness of the new attach method. The power output for this circuit was measured with a spectrum analyzer as a function of the VCO output frequency, and is plotted in Fig. 3.7. Both transceivers reach an output power greater than 30 dBm between 13 and 17 GHz. A comparison of profilometer scans between the two methods (Fig. 3.5) reveals the difference in die pocket fill material leveling, with the PMM die attach providing a more leveled chip surface allowing the pocket to be filled more evenly. This is the primary benefit for the chip-in-pocket manufacturing method, and has reduced failures due to die fill ink overflow onto the die pads and CTE related grounding detach issues. Additionally, it has been shown in previous works that die pocket fill level can have a substantial impact on printed interconnect loss. A leveled

die fill material surface provides the ideal conditions for low interconnect loss [32].

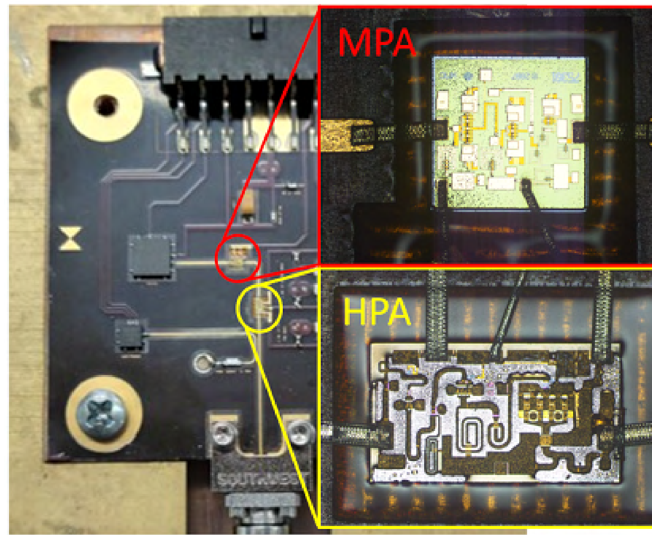


Figure 3.6 An RF transceiver module fabricated using the PMM die attach method to mount the MPA and HPA bare die components with microscope images of the bare die chips is shown above.

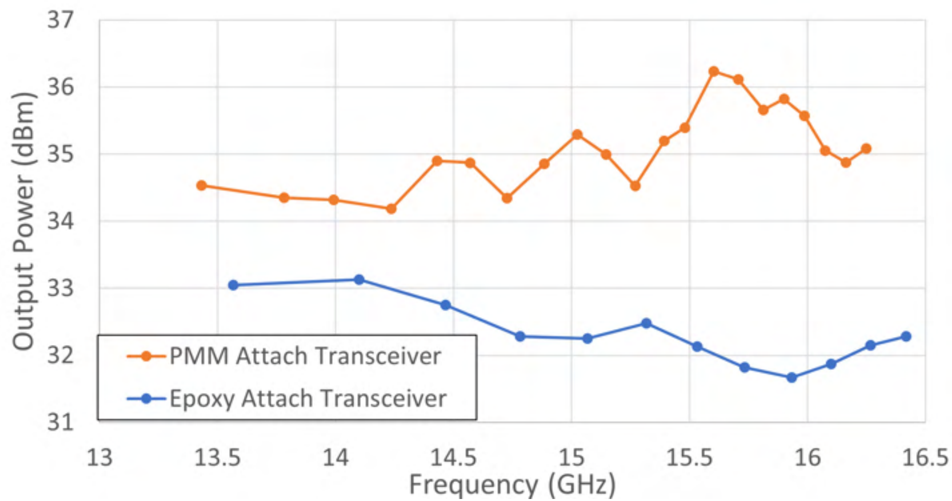
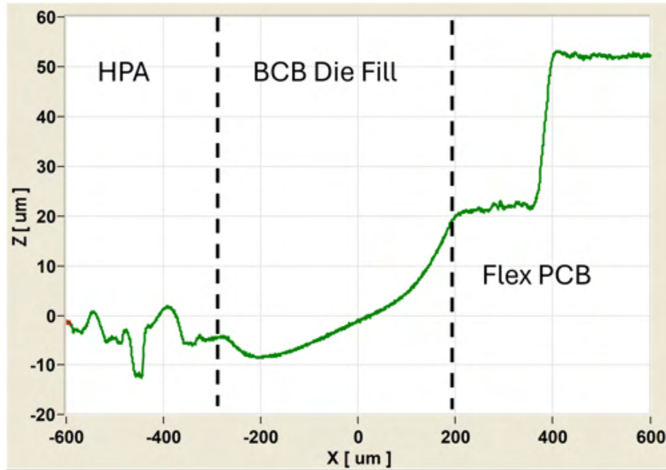
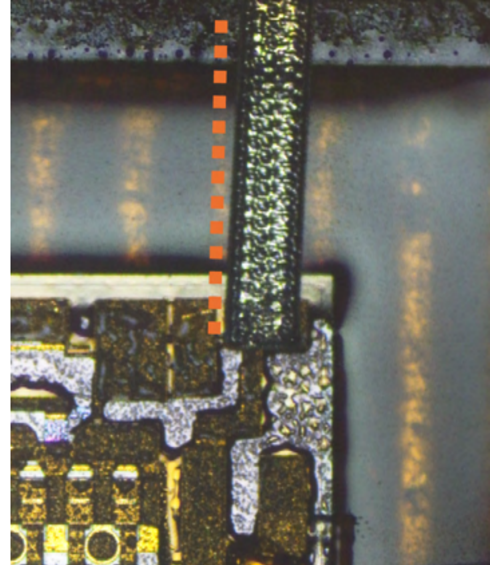


Figure 3.7 S-parameter measurements comparing the power output of RF transceiver modules. Comparison includes a transceiver built with the proposed die attach method and a transceiver built with a standard conductive epoxy die attach method.

Fig. 3.8 gives a more detailed look of a scan taken along the HPA drain interconnect line, with further examples of well leveled interconnects from the gates and RF output shown in Fig. 3.9.

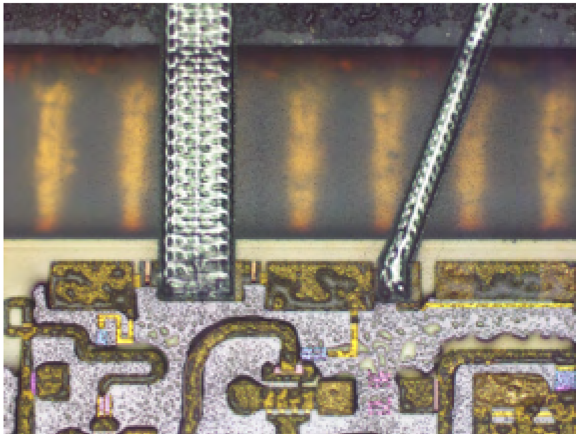


(a)

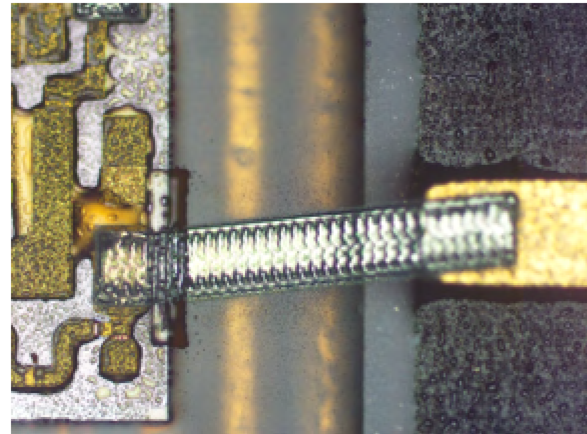


(b)

Figure 3.8 (a) is a profilometer scan of the die fill material along the drain interconnect, and (b) shows the scan line. The impact of the die attach on the flatness of the die makes it significantly easier to fill the die pocket flush with the die and PCB, supporting better interconnects.



(a)



(b)

Figure 3.9 Further examples of flat interconnects that were able to be deposited on an HPA attached with AJP die attach.

Finally, Fig. 3.10 shows a close up of the SLCs in the MPA die pocket. These were also mounted using the AJP die attach method, proving its use for more than just die components. Leveling the die fill material for this die pocket is difficult due to the height mismatch between the MPA die and the SLCs, making it crucial for all components to be well leveled to prevent BCB spillover while still providing an adequate ramp for the biasing interconnects to connect with the upper plate of the

SLCs.

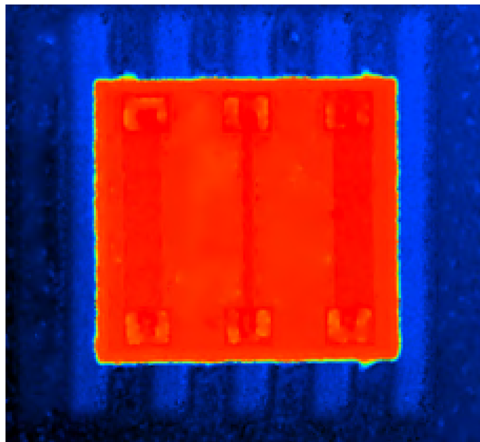
Figure 3.10 An example of the printed die attach method being used to mount SLCs in the same die pocket as the MPA die.

3.3.3 Printed Dam-and-Fill Pocket on Glass

A compatibility test for the Tresky T-5300 die bonder at MSU with the printed die attach method was carried out on glass. The glass printing substrate was first cleaned with isopropanol and the BCB and silver bar pattern was deposited using a bar width of 100μm at a 1:1 material ratio. A 0dB attenuator die was then mounted using the die bonder, and the assembly was thermally cured at 200°C for 5 hours to set the BCB. A scan of the die was taken after curing, and the die surface was found to be level to within 0.012° of the glass reference plane. The post cure attached die as well as the profilometer surface scan is shown in Fig. 3.11. This figure also gives a bit more insight on the interaction between the die attach materials and the die, showing how the BCB wicks up to the die, as well as the way it flows onto the silver when no die is present.

A dam-and-fill print was also performed to test the physical stability of the die when subjected to the force of the AJP sheath gas stream. A polyimide dam wall on the order of 100μm tall was built up around the die and soft cured at 200°C for 5 minutes on a hot plate to solidify the material. The gap between the die and the dam wall was then filled with BCB and cured at 200°C for 5 hours. Fig. 3.12 shows that with the die leveled by the attack layer and the die bonder assisted mounting

(a)



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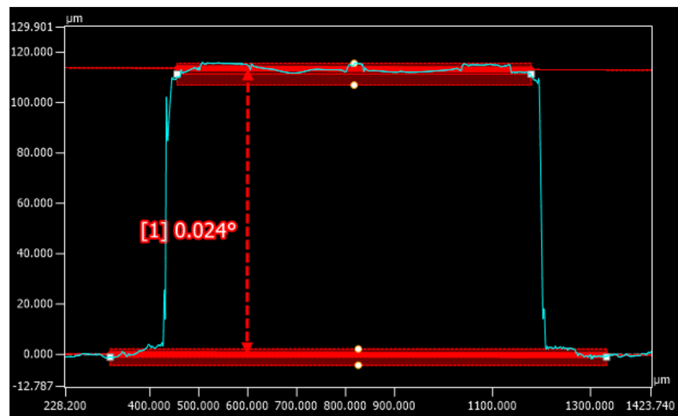
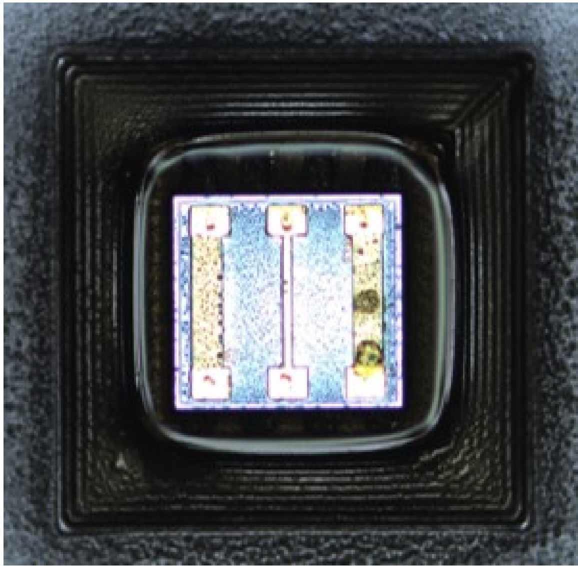


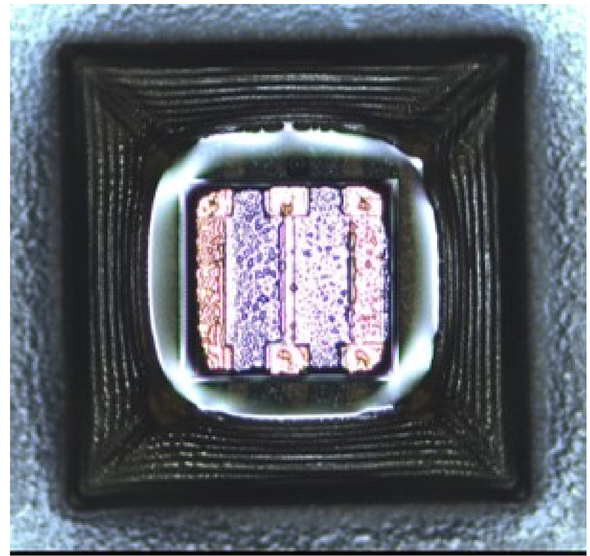
(c)

Figure 3.11 (a) Images and (b) profilometer area scan taken of a 0dB attenuator die attached to glass using the AJP die attach method. The die was mounted using a Tresky T-5300 die bonder and is flat to within <0.1° of the glass reference plane as shown by the scan data in (c).

procedure, the major contributor to pocket fill level is the ability to match the wall height to the die.



(a)



(b)

Figure 3.12 Dam-and-fill process completed on 0dB attenuator dies mounted using the T-5300 die bonder and the AJP die attach method. With the die leveled by the attach layer and die bonder machine process, the major contributor to pocket fill level is the ability to match the wall height to the die. (a) shows an example of a well matched die fill volume and (b) shows the overflow onto the die that can occur when attempting to fill up to a wall that is taller than the die thickness.

CHAPTER 4

DEVELOPING AN AJP COMPATIBLE TRANSFER PROCESS

If the goal is to develop AJP techniques for the fabrication of compact, multi-layered, truly 3D packaging and system design, then several shortcomings of the technology will have to be addressed. One of these shortcomings is a lack of tailored dielectric inks for AJP. Many of the inks used at the time of writing are adapted from typical materials used in semiconductor manufacturing processes, such as polyimide or PMMA. This leads to a lot of difficulties during the post processing phase, particularly when thick layers or multiple layers are desired. Thermal curing cycles have some maximum recommended layer thickness to avoid solvent capture and warping or delamination, which can add many thermal cycles to the post processing procedure. This is a significant issue when fabricating single layer structures, and becomes even more prohibitive when considering 3D structures with potentially many layers. Each layer has a thermal budget, a limit to how many thermal cycles it can survive before damage occurs that degrades RF performance or outright destroys the part, and this budget can be easily exceeded for system-on-package or stacked chip designs. Additionally, it may be desirable to use materials in the lower layers that cannot survive the processing temperatures of a material in the upper layers. For either of these scenarios, it would be beneficial to be able to process the layers separately and combine them at the end to form the final structure.

A process in which AJP fabricated layers can be separated from the printing substrate and assembled together after going through the respective post processing steps individually is what will be explored in the next several chapters. This chapter contains work that was published in [39].

4.1 Initial Development

The first iteration of the transfer process involved taking a polyimide dielectric layer on a glass printing substrate, submerging the part in a beaker of DI water, and bringing the water to a boil, which would release the polyimide layer from the glass. The polyimide layer would then float to the top of the water and could be skimmed out with a mesh basket. The layer was strong enough to be handled without breaking as long as the thickness was greater than $5\mu m$, an example of which is

shown in Fig. 4.1.

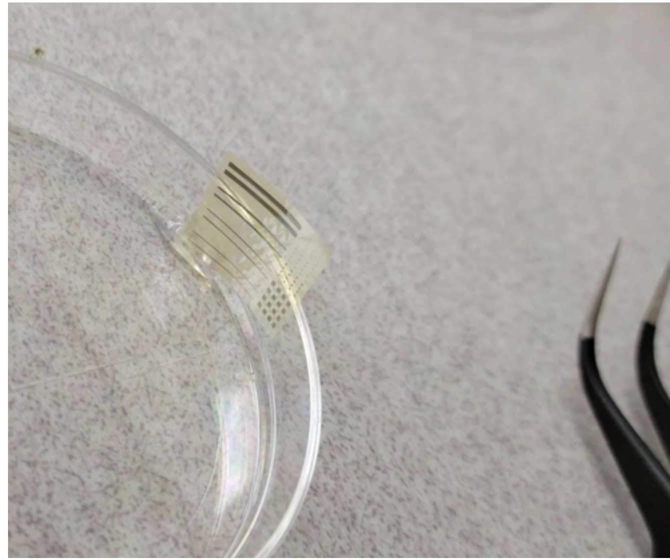


Figure 4.1 An early polyimide liftoff test coupon after release from the glass substrate. Several silver features are included to test the resilience of top metal features against the process.

While this process was highly repeatable for the liftoff portion of the procedure, the use of boiling water as the release agent brought up concerns about its compatibility with active die components, more complex 3D structures, and other inks. Additionally, the transfer procedure carried a high risk of wrinkle defects or tear damage to the part due to the lack of a semi-rigid backing material to support the part after release. Precision placement onto the target surface is also difficult to achieve, again due to the lack of backing material for handling by a micro-manipulator system. This version of the process was set aside in favor of exploring other options.

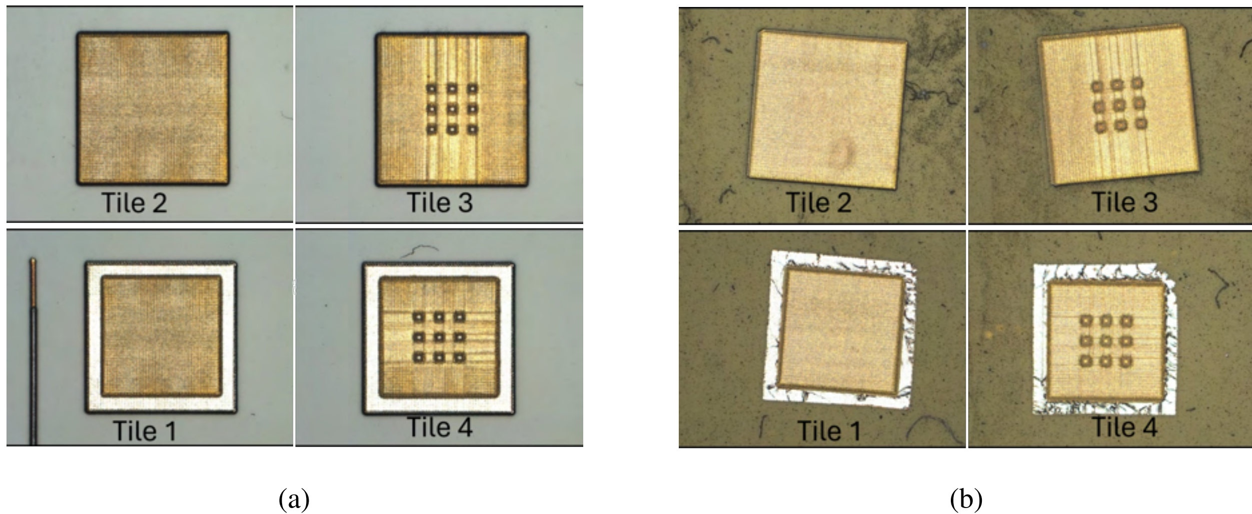
A stamping method, borrowed from semiconductor and MEMS fabrication processes and involving the use of a strip of PDMS material to pick up and then place the printed part, was selected to facilitate the transfer process. PDMS provides a flexible yet solid substrate for handling any printed parts with, and has the added benefit of the viscoelastic effect, allowing for variable adhesion on pickup and release depending on the velocity of stamp removal. It can also be cast around 3D structures in liquid state and cured at low temperatures to form a compliant stamp rubber for transferring structures with large height differences or otherwise odd physical dimensions. These stamps can be handled with custom attachments for systems such as die bonders that grab the much

more durable PDMS substrate and allow for precise placement of the printed part. With the method of handling decided, the next critical step to re-evaluate is the liftoff procedure.

4.2 The Transfer Process for Polyimide Substrates

4.2.1 Adhesion Tailoring with Polyimide Dielectrics

One of the investigated methods of the liftoff procedure was to attempt to fabricate the printed parts without the use of adhesion promoter on the printing substrate to maintain minimal adhesion at the interface, and this came with a few challenges. This adhesion must be strong enough to survive the post processing thermal cycles required by the AJP materials, but weak enough to be overcome by the PDMS stamp. Depending on the material and deposition rate during dielectric printing, these adhesion regions may not overlap. Typically, adhesion of a printed dielectric to the printing surface is maximized by using an adhesion promoter. However, this method results in the printed part being inseparable from the printing surface, even by scraping tools such as a razor blade.



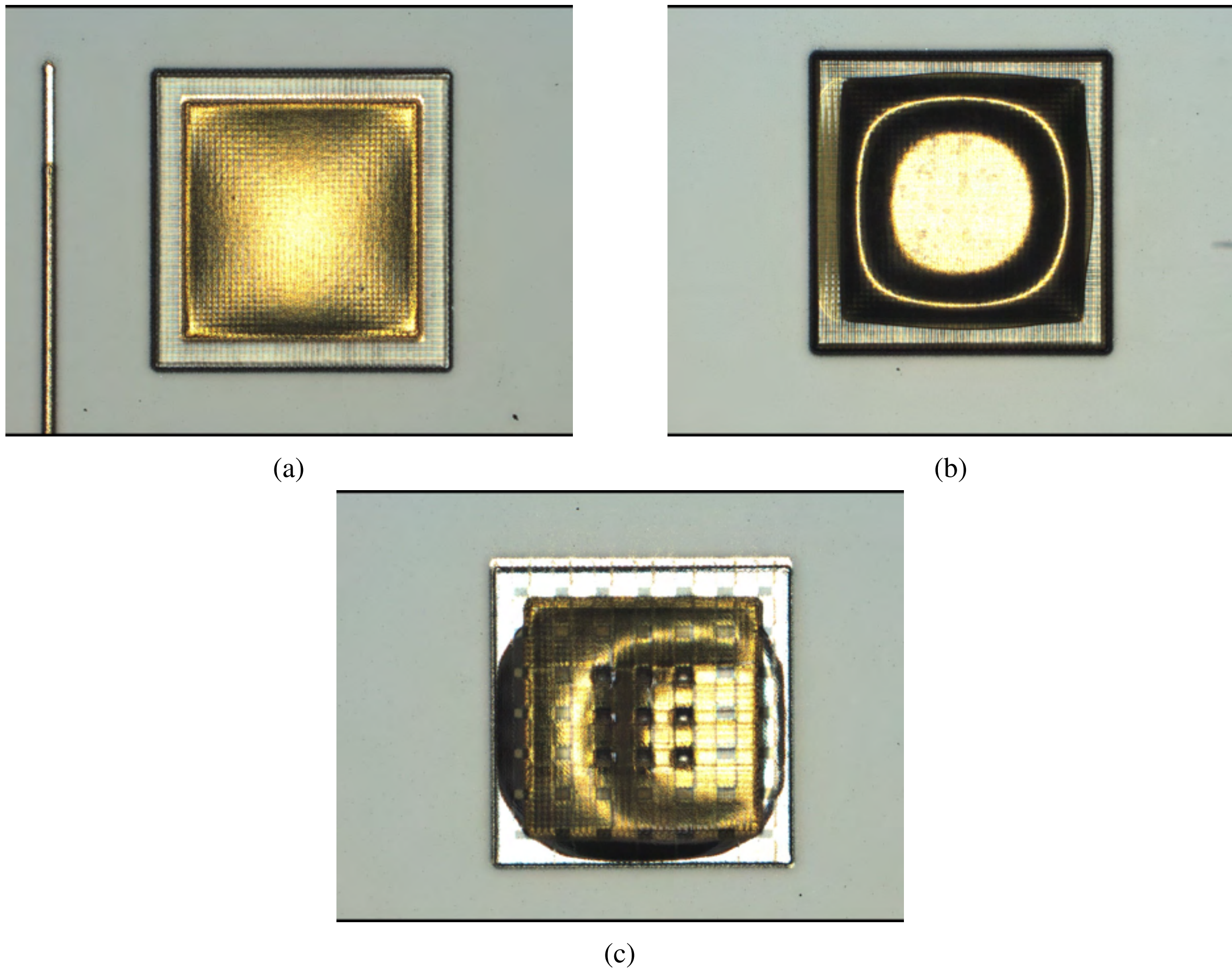
(a) (b)

Figure 4.2 A mechanical test tile set used to determine interlayer adhesion stability when subjected to the transfer procedure. (a) is the tiles on glass pre-transfer, and (b) is the tiles after transfer on double sided Kapton tape.

The first trial of this method was to print several test stacks with the goal of determining whether or not the layer-to-layer adhesion in the stacks would hold up to the liftoff procedure. These stacks, arranged in tile sets (Fig. 4.2), were square patches with a $5\mu m$ thick polyimide foundation layer, followed by a layer of silver to simulate a ground plane, and a top layer of polyimide to simulate a

dielectric. Several patterns were tried for both the ground plane, including solid fill and perforations of various sizes to compensate for the poor polyimide to silver adhesion. Likewise, the upper polyimide layers included several variations such as vias and size reduction.

Through this trial, it was found that a significant issue with not using adhesion promoter is an increased risk of delamination between the first layer and the printing substrate. Uncured polyimide, which contains a variable amount of NMP solvent, tends to bubble during curing as that solvent evaporates and is trapped between the curing PI layer and the printing substrate.



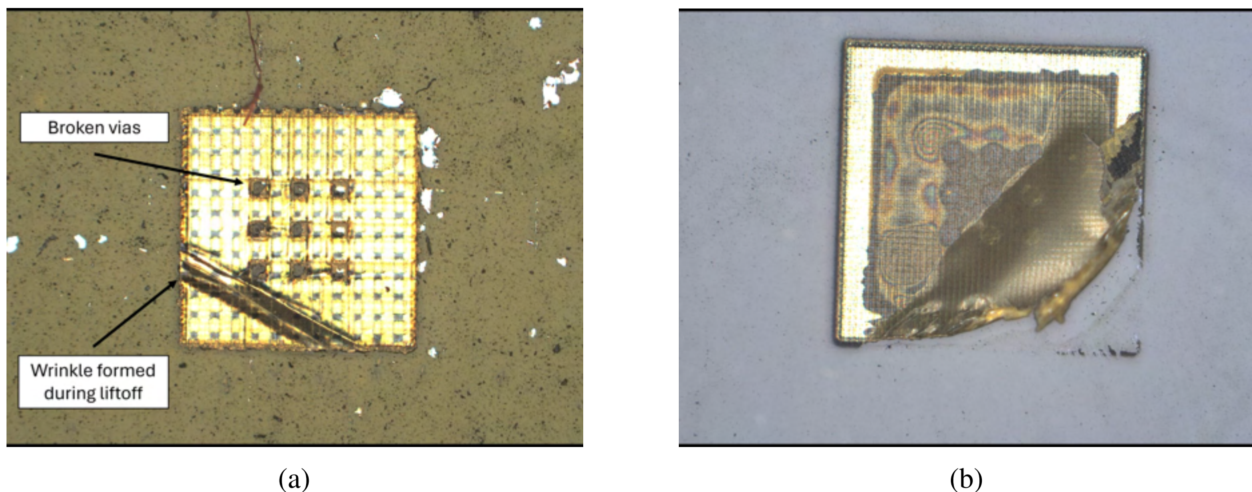
(a) (b) (c)

Figure 4.3 Solvent bubble delamination defects that can occur during curing. (a) Early release of the base PI layer from the printing substrate. (b) Delamination of internal PI to silver interface. (c) Metal plane perforations allowing for contact between dielectric layers above and below the metal layer help prevent internal delamination, but they do not address the early release problem.

Skipping the adhesion promoter leads to an increased need for soft curing or dehydration bake

steps at more frequent intervals. This reduces the chance of early delamination due to drastic material shrinkage or warping during the final hard cure step, examples of which are shown in Fig. 4.3. A low temperature bake every 5-10μm can improve the yield of these parts, but leads to an increase in the amount of time required for fabrication. Yield with this procedure is still quite low, and defects are not very predictable.

Issues that can arise during the transfer process are surface wrinkling and interlayer delamination, both of which are shown in Fig. 4.4. A surface wrinkle can occur when a structure is only partially adhered to the stamp or maintains a partial adhesion to the surface below. When a transfer is attempted in this case, the surface may be bent before landing on the target surface leading to wrinkle formation that is not generally reversible. Interlayer delamination is the unintended separation between inner layers of a structure, and can occur when the adhesion over a large area between the layers is poor, such as in the case of an embedded silver ground plane on a PI substrate. This can also cause the destruction of unsupported via metal at the base of the via. These problems are often related, as unexpected behavior during liftoff can cause incomplete adhesion to the stamp, which in turn often leads to physical defects during deposition of the structure onto the target surface.



(a) (b)

Figure 4.4 Several defects that can occur during the transfer step. (a) An inset tile with vias that has experienced an inter-layer delamination and wrinkling. (b) The remainder layer of a tile that experienced an inter-layer delamination.

An issue that arises from the transfer step of this process with polyimide dielectrics is the detachment of the silver top metal from the dielectric substrate (Fig. 4.5.a). It has been well reported on that the adhesion strength of printed silver to polyimides is notably weak [40, 41]. Based on incomplete removal of the top metal by the PDMS stamp during early transfers, it seems reasonable to estimate that the adhesion strength between the stamp and the silver is nearly equal to the adhesion strength between the silver and the polyimide dielectric layer. A potential solution to this is to switch to a metal ink that demonstrates better adhesion to printed polyimide material. A more universal solution would be to integrate a top dielectric layer into the design that covers everything but the areas of the part that must be exposed, such as probe pads. Using such a layer on the top, bottom, or both sides of the part would increase the required print time and processing steps. It does, however, come with the added benefit of making the part more durable and resistant to light abrasion, dust particles, and chemical fumes in its operating environment due to the strength and chemical resistance of polyimide films.

Using this top cover solution requires all parts to be designed to accommodate the dielectric loading introduced by this layer. Depending on the required thickness, this may or may not introduce a significant change in performance. The effect on radiating elements, however, may be significant enough to restrict the use of certain designs with this process.

In some cases, fabricating without the use of adhesion promoter may be impossible or lead to unacceptably low yield. For such a situation, an alternative process is proposed in Fig. 4.6. This alteration to the process leverages the silver nanoparticle ink's tendency to adhere preferentially to the polyimide layer above it in the stack rather than the polyimide layer below to create a more reliable separation interface. In this alternative process, the printing surface is first treated with adhesion promoter to ensure that the first polyimide layer will be strongly adhered and is not transferred. This layer may be spin coated to reduce fabrication time and surface roughness, and is hard cured prior to silver printing. This interface becomes the most likely plane for delamination when the PDMS strip is applied and removed for single layer circuits.

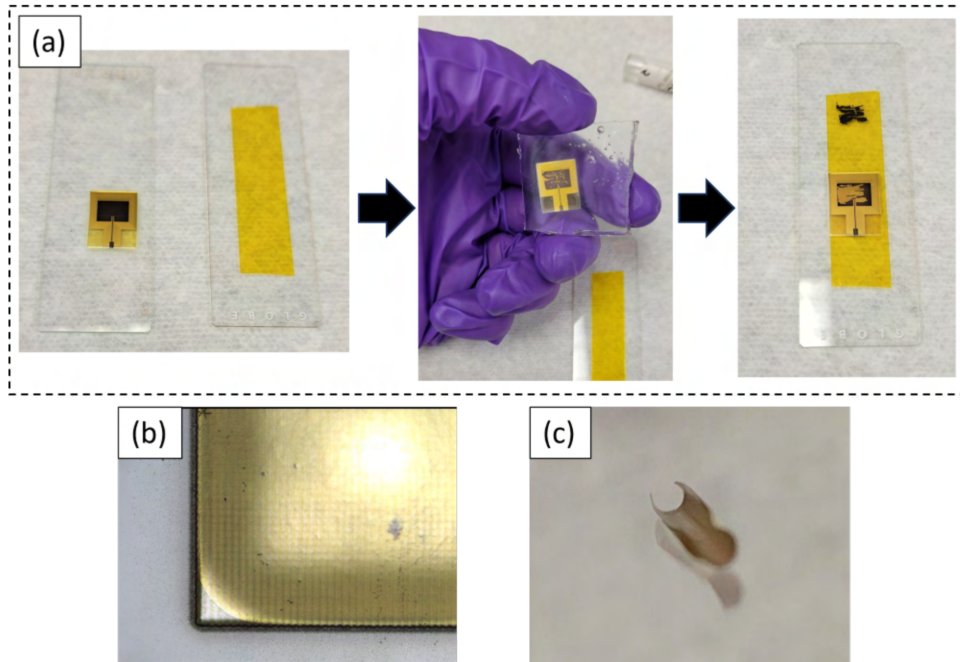


Figure 4.5 Several potential failure modes of the transfer process. (a) Top metal is removed by the stamp due to low silver to PI adhesion. (b) Interior delamination of the PI substrate. (c) Curl delamination caused by low silver to glass adhesion.

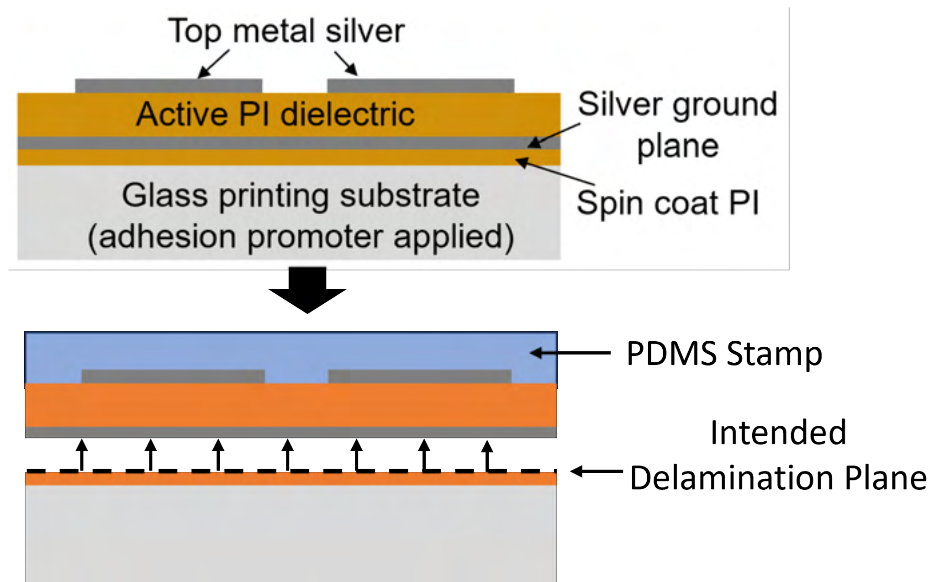


Figure 4.6 Proposed alternative transfer method. The structure is built on a spin coated PI layer that is deposited after applying adhesion promoter to the glass printing surface. Liftoff occurs between the spin coat PI and silver ground plane layers, instead of between the spin coated PI and the glass.

4.2.2 Process Description

The process for fabricating the circuits to be transferred is similar to previously demonstrated AJP circuits with additional preparation steps to ensure separability. Starting with a glass substrate,

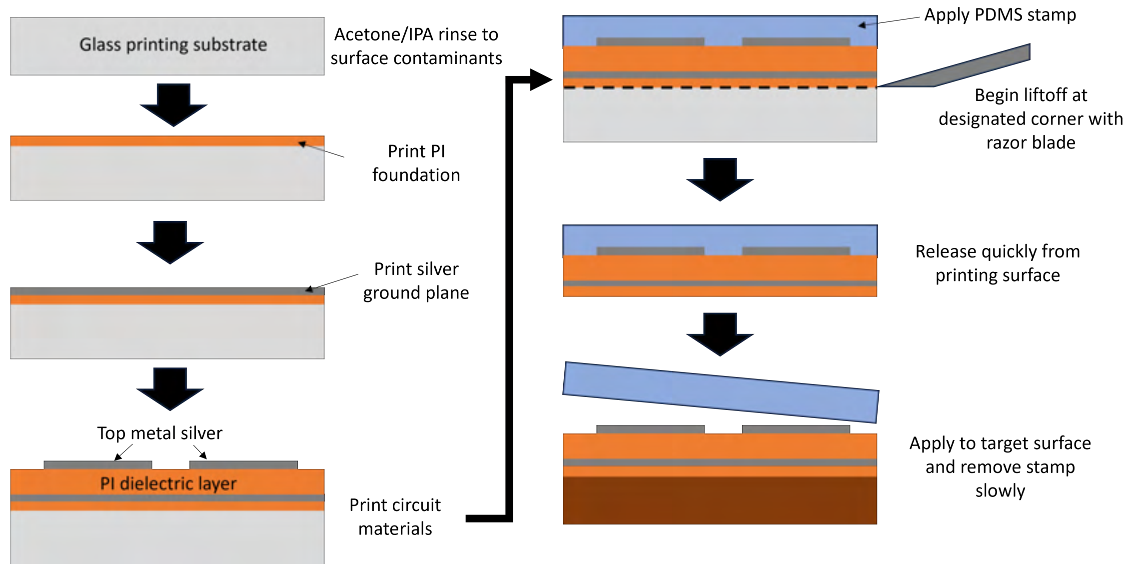


Figure 4.7 A flowchart detailing the steps of the transfer process. Adhesion between the printed part and the print surface is broken with a razor blade, and a PDMS strip is used to pick up and transfer the part to a target surface.

the first step is to clean the printing surface thoroughly with acetone and isopropanol. This is critical, as the use of adhesion promoter prevents the removal of the part for transfer, and any contaminants on this surface will increase the chance of early delamination. Next a thin layer ($< 5\mu m$) of HD Microsystems PI2611 Polyimide is applied through either AJP or spin coating, followed by a dehydration bake at 150°C for 5 minutes. This layer serves as structural support for otherwise unsupported metal features or embedded dies. After this layer is prepared, printing begins with a layer of Clariant Prelect TPS 50 G2 silver nanoparticle ink to form the ground plane. The rest of the circuit is then printed on top, in this case including printed PI2611 dielectric layers and more silver ink to form the top metal circuit structures. Post-processing is carried out between each printed material switch to cure the latest material before moving on to the next material. After the top metal is sintered, a 1-2μm thick layer of polyimide is deposited to protect the top metal. Finally, a PDMS strip is applied using a rolling motion to remove the printed structure from the printing substrate, forming the stamp. This stamp may then be applied to any adhesive surface of sufficient strength to overcome the PDMS adhesion, thus transferring the printed circuit. A flowchart of the full process is given in Fig. 4.7.

The adhesion strength between the first layer and the printing substrate is an important factor.

Excessively weak adhesion will lead to premature release during post processing of printed dielectrics, while excessively strong adhesion will defeat the PDMS stamp's ability to lift the structure off of the printing substrate. Vias may be formed in the dielectric substrate layer during printing by leaving a gap in the printed polyimide to be filled in during top metal printing.

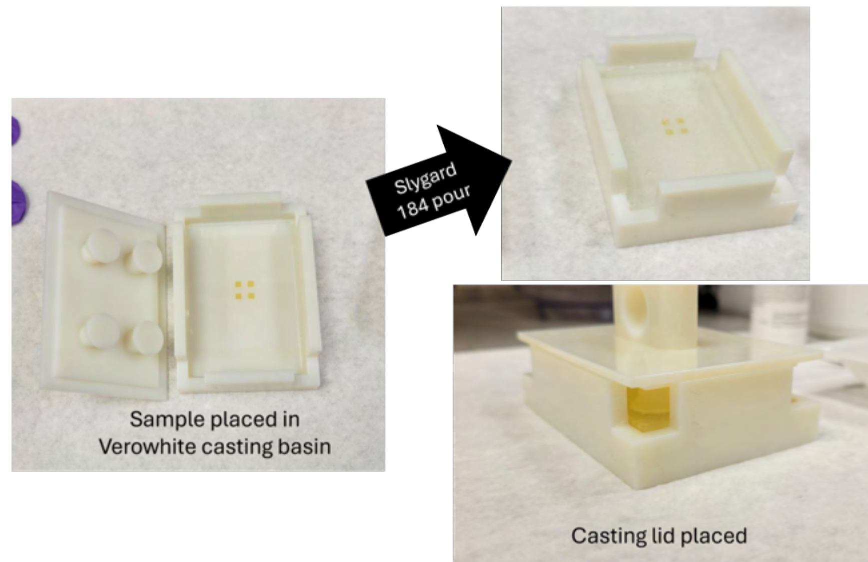
The transfer was to be carried out using the stamping tool depicted in Fig. 4.8. The tool was designed so that the PDMS stamp may be cast around the printed part to maximize contact surface area between the stamp and the part, therefore maximizing the stamp adhesion during lift off. This proved unreliable for both the release and stamp curing as material tended to flow under the printing substrate and remain uncured around the edges of the tool. The method for transferring the parts was revised to use separately cured PDMS stamps that were applied by hand, or later using a tool that the pre-cured stamps could be mounted to.

An early example of a transferred structure is shown in Fig. 4.9. These test coupons were used to determine whether or not multiple layers of polyimide would stay together during transfer if they were separated by a layer of silver. This has important applications in RF grounding and signal isolation within a circuit or package. It was found that the layers adhere together quite well under the assumption that the adhesion of the bottom layer to the printing surface is not significantly stronger than the stamp adhesion. If the lowest layer is too well adhered, then the intermediate layers tend to separate at a polyimide to silver boundary, with the silver adhering preferentially to the polyimide layer above. This turns out to be useful for an alternative transfer method that will be described in a later section.

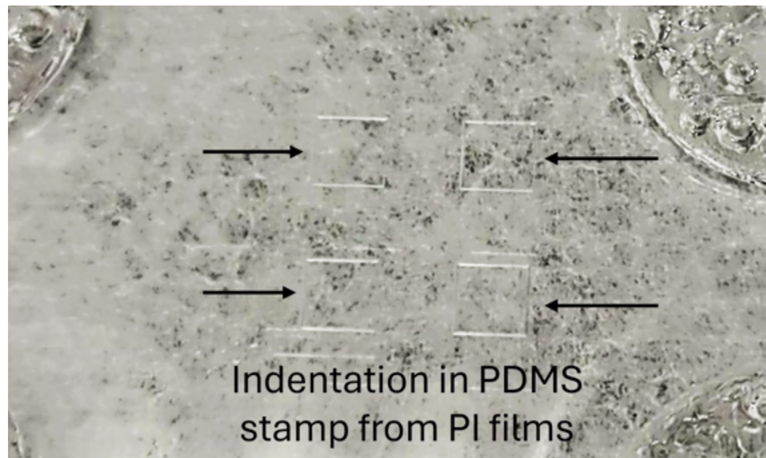
4.2.3 Design and Fabrication

Several mmWave structures were designed and fabricated on a test coupon to characterize the effect of the transfer process on RF performance. Dimensional measurements were taken with an optical profilometer during printing for verification and to guide manual AJP parameter correction mid-process. Fig. 4.10 provides an overview of the test coupon, as well as a comparison map taken from profilometer scans done before and after transfer.

The first structure chosen for the characterization of the transfer process is the series Beatty



(a)



(b)

Figure 4.8 (a) An early prototype transfer jig and (b) the resulting PDMS stamp cast. Indentations can be seen where the material was cast around the printed layers.

standard [42, 43]. This structure is a segment of low impedance line inserted into a standard MS line path. The sharp impedance discontinuities at either end of the wide segment create a resonant cavity-like effect, giving a series of peaks in both the S21 and S11 measurements. If the geometry of the structure is precisely known, these peaks may be used to extract the dielectric constant of the substrate material using EM simulators such as Ansys HFSS. It may also be used to characterize the loss tangent if the resistivity of the top metal is well-known across the measured frequency range. The number of resonant peaks measurable within a given frequency range is determined by the

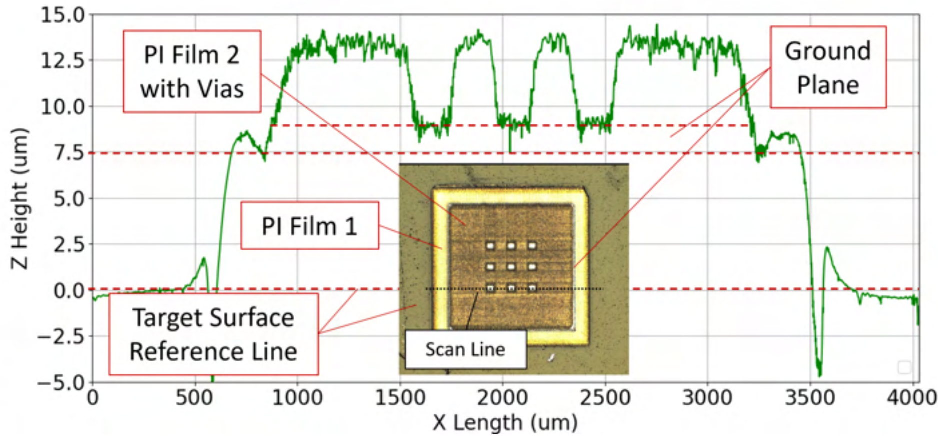


Figure 4.9 Profilometry data is shown for a test coupon after transfer used to determine whether or not multiple polyimide layers with via perforations separated by silver are compatible with the stamp transfer process.

length of the low impedance region in the center of the standard, with the length being equal to 1/4 of the wavelength of the lowest resonant frequency. The Beatty standards were made as long as possible to balance printing time with the need to fit multiple resonant peaks within the limited measurement range (0-50GHz) of the PNA. A low impedance region length of 3.2mm was selected for resonance frequencies at 15.6, 32.2, 48.8GHz, with a width of 3 times the MS line trace width to provide a strong impedance discontinuity at either end. A closer look at the procedure used to extract the dielectric constant of a printed material using this method is provided in Appendix .A.

The other structures chosen were MS lines, which are among the most universally applicable RF structures and provide a baseline for the effectiveness of the transfer process. Comparing the RF performance of the lines before and after transfer using S-parameter measurements gives us some information about the effects of transfer on the printed part. For instance, a strong degradation of S21 from the pre-transfer to the post-transfer measurements could indicate that the stamp has a destructive effect on the exposed surface metal, or that the forces applied during transfer have somehow damaged the substrate. The performance of these lines depends on the impedance match to the measurement system, which is set by the ratio of the line width and the substrate thickness. These lines were designed to be 70μm wide for a polyimide substrate thickness of 30μm. Due to low solid loading in the polyimide ink and inconsistencies with vertical shrinkage during hard curing, the resulting substrate thickness was approximately 20μm after hard curing. This had a

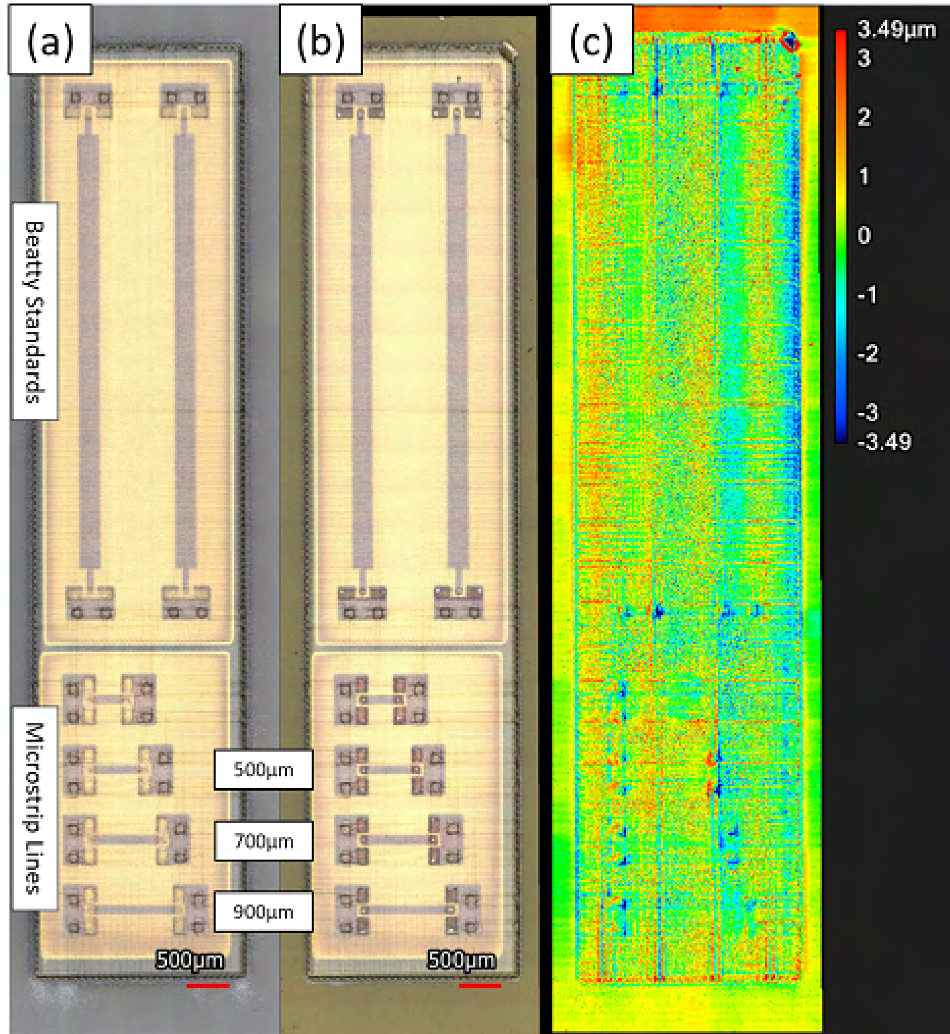


Figure 4.10 The progression of the full MS test coupon. The images are (a) pre-transfer, (b) post-transfer, and (c) a comparison of the height data from (a) and (b). No significant physical deformities were present on the test coupon post transfer.

negative impact on MS line performance that was unrelated to the transfer process. Further study towards predicting and controlling the post-cure dielectric thickness in the future is required.

4.2.4 Measurements

The main attributes of the transferred test coupon to be characterized with measurements are the structural cohesion and the RF performance before and after transfer. A Keyence VK3000 optical profilometer was used to take profile measurements of the test coupon before and after transfer to determine whether or not any damage occurred as a result of the stamping process. Examples of such damage would be the formation of wrinkles, layer to layer delamination, or substrate tearing.

Fig. 4.11 shows a comparison of the scan results.

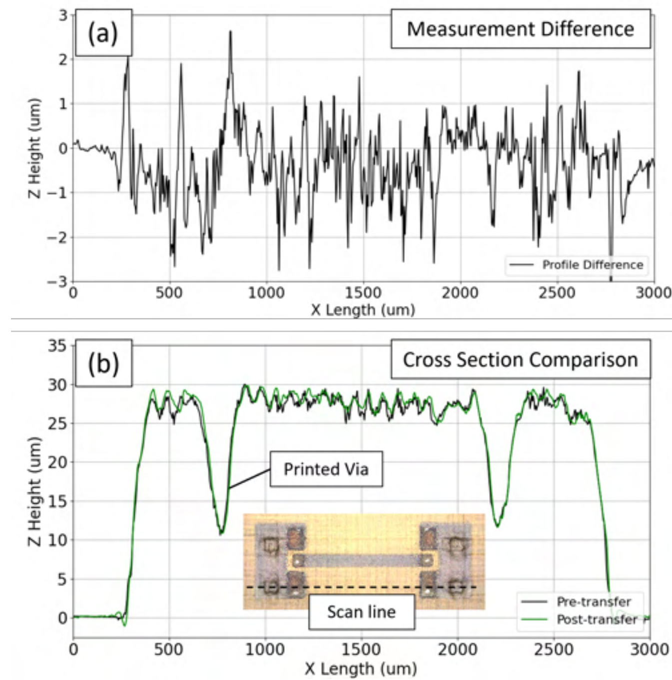


Figure 4.11 A thickness profile comparison between pre-transfer and post-transfer measurements is plotted. Shown are (a) the difference between the profile measurements, and (b) a plot of the profile measurements overlapping each other.

As can be seen in Fig 4.11.a, the height deviation between pre-transfer and post-transfer measurements is less than $3\mu m$ across the $900\mu m$ MS line. This is representative of the average across the test coupon, with most of the deviation stemming from alignment error between the pre-transfer and post-transfer measurements. Fig. 4.11.b shows the overlapped profiles, the agreement of which indicates that no significant damage has been introduced at any point during transfer.

S-parameter measurements were taken on all test structures to analyze the effects of the transfer process using a Keysight N5227A PNA. Since materials deposited via AJP do not have the same properties as bulk materials, this also allows verification of the electrical properties of the printed structures. Measurements were performed just before and immediately after transferring the devices from the glass printing surface to a strip of double sided Kapton tape mounted to a separate glass slide.

4.2.4.1 Beatty Standard

The measurements of the Beatty standard structure are shown in Fig. 4.12. The measured peaks allow the characterization of resonance shift due to potential deformities caused by the circuit transfer (e.g. internal layer delamination, substrate wrinkle formation, micro-fracturing of the polyimide). Comparing the results to an HFSS simulation of the same structure, the dielectric constant of this material was found to range from 3.65 to 3.2 between 15.6 GHz and 48.8 GHz, respectively.

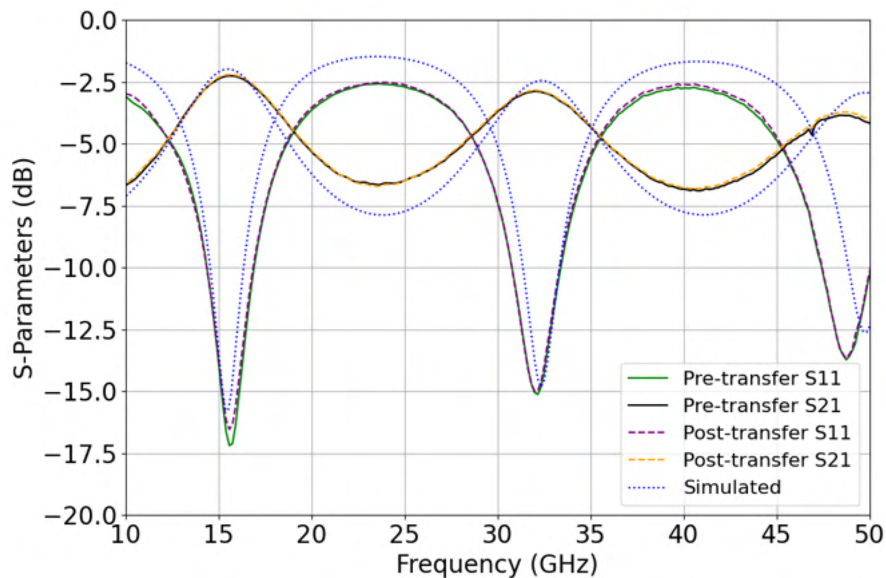


Figure 4.12 S-parameter measurements of a Beatty Standard resonant structure, before and after transfer. No significant shift in resonant frequency due to the transfer process was detected.

The resonant frequency before and after transfer can give us some information about the effect of the process on the dielectric. For example, a shift in resonant frequency could indicate that the competing forces from the stamp lifting off and the adhesion to the printing surface may be causing small voids or internal layer delaminations, changing the effective substrate thickness.

4.2.4.2 Microstrip Transmission Lines

The measurements of the MS lines, both pre-transfer and post-transfer, are shown in Fig. 4.13, and a plot for the difference in pre-transfer and post-transfer S21 measurements is given in Fig 4.14. The difference in these measurements is below 0.05 dB from 5-40 GHz and is below 0.1 dB

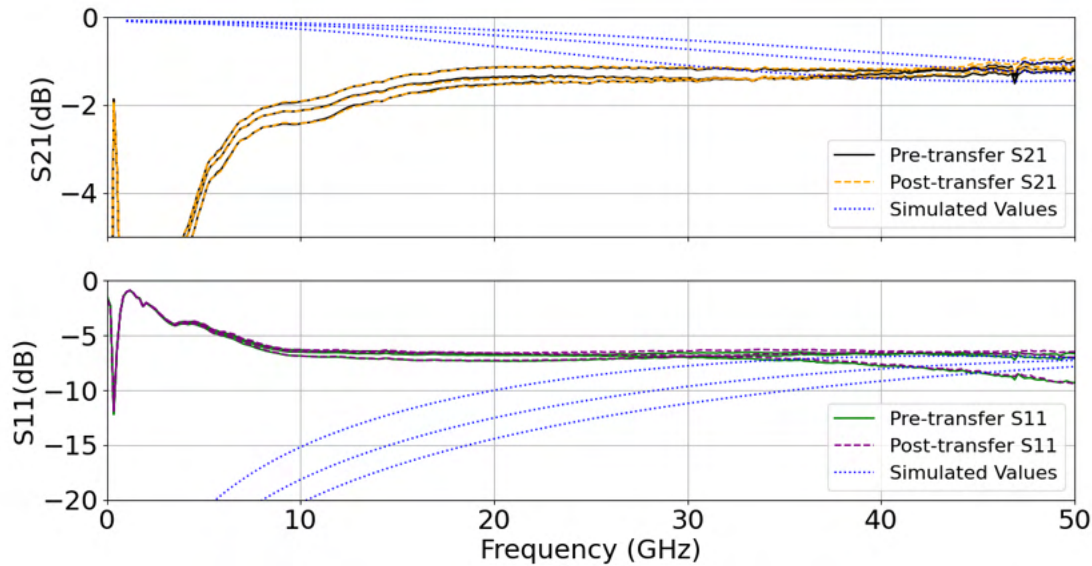
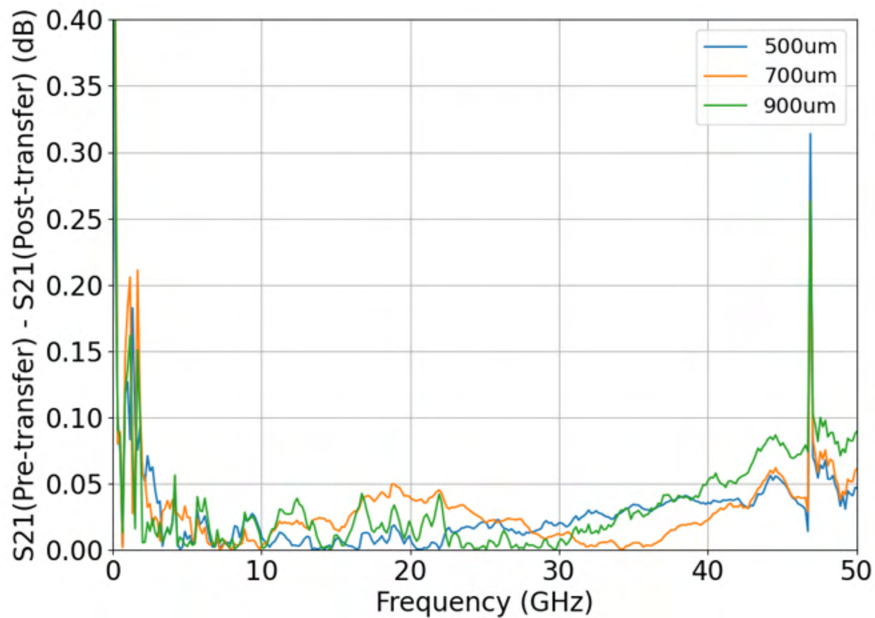


Figure 4.13 S-parameter measurements for a few MS lines with lengths of 500, 700, and 900μm. Measurements indicate generally stable performance before and after transfer. The divergence from simulated values at low frequencies is discussed further with Fig. 4.15.

from 40-50 GHz, both of which are within the range of measurement error due to probe landing inconsistencies. This indicates that the RF performance is not greatly affected by the transfer process for the MS lines.

Another important factor in RF performance, particularly at lower frequencies that may be used by base-band signals, is the via quality. Ground pads for RF probes and CPW lines require continuous, high quality via connections or large areas for capacitive coupling to function effectively for low frequency signals (<10-20 GHz). In the case of an AJP fabricated circuit, the via well may contain some amount of overspray [44] from the dielectric substrate deposition that reduces the effective via depth. As the overspray layer becomes thicker, the low frequency drop-off of the structure is more pronounced. This is the effect seen in the S-parameter measurements of the MS lines causing poor performance below 20 GHz. Fig. 4.15 shows the simulated effect of changing the via depth compared to the S-parameter measurements of the 900μm MS line. The thickness of the overspray layer at the bottom of the via is given by h_{iso}, which is varied from 0μm (no overspray) to 2μm, demonstrating the low frequency roll off caused by the overspray effect.

Several transmission lines were fabricated with special attention to via metal fill to improve



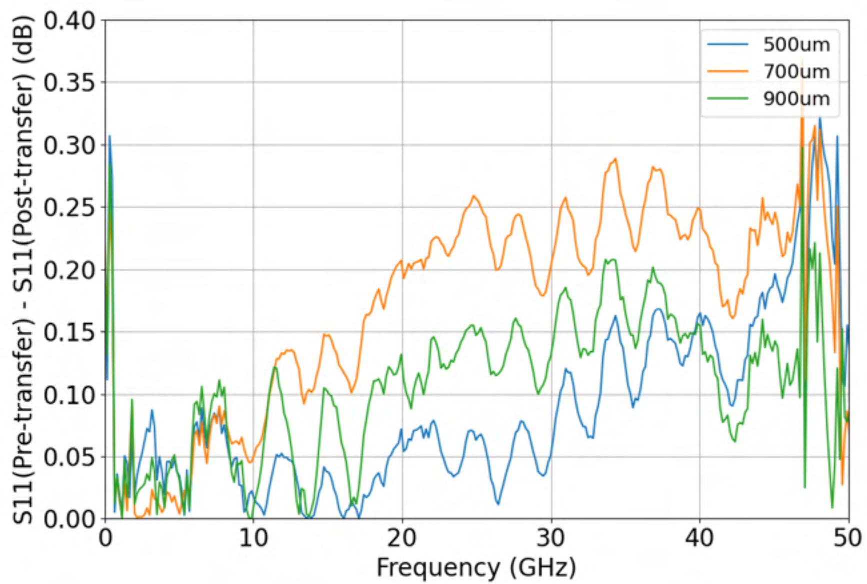


Figure 4.14 Difference between the pre-transfer and post-transfer S21 and S11 measurements for the MS lines. The low values across the measurement range indicate negligible shift in RF performance due to transfer.

performance. Post transfer measurements of these lines were taken that show less than 1dB of loss per mm from 0-67GHz. Both the post transfer lines and the measurements are shown in Fig. 4.16, and profilometer scans showing the cross section of the substrate and vias along with the trace metal

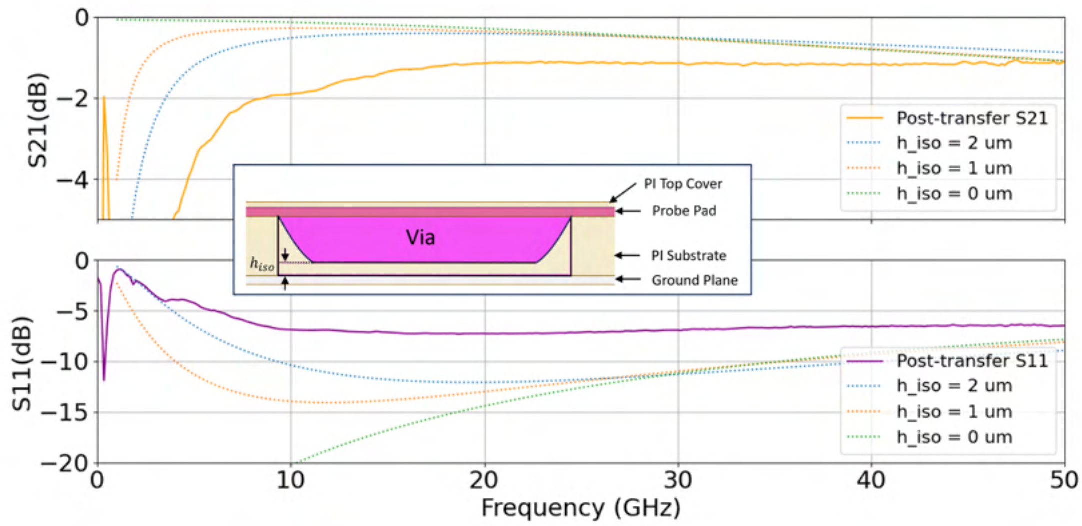
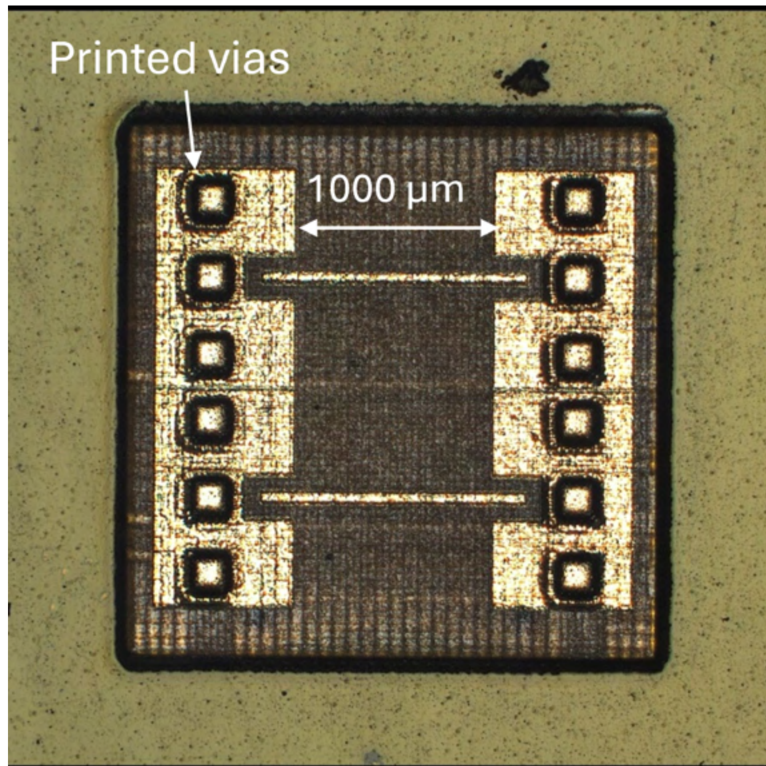
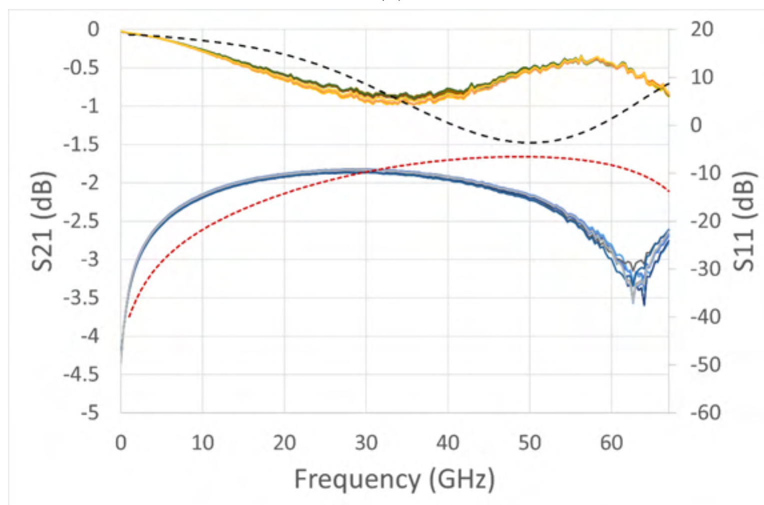


Figure 4.15 Effect of overspray on via quality compared with measurement data for the 500μm MS line. Effective via depth is modeled for a 20μm thick dielectric substrate. Low frequency roll off is observed as the thickness of the isolation layer (h_{iso}) caused by overspray between the ground plane and the via metal increases, where $h_{iso} = 0\mu m$ is a via without isolation.

thickness are given in Fig. 4.17.

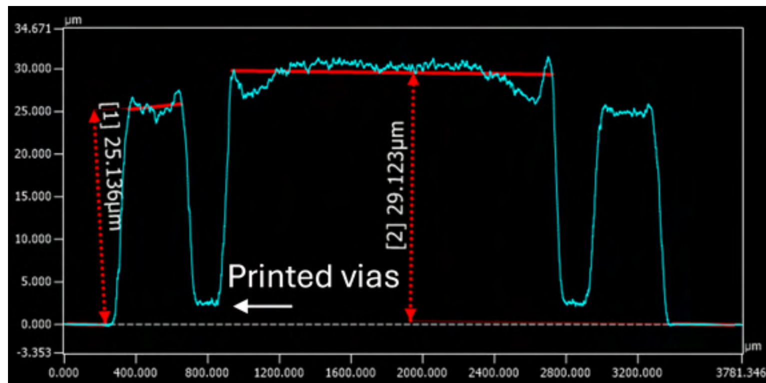


(a)



(b)

Figure 4.16 (a) An early transferred transmission line. (b) Measurements were taken post transfer and compared with simulated values, showing less than 1dB of loss for all measured lines from 0-67GHz.



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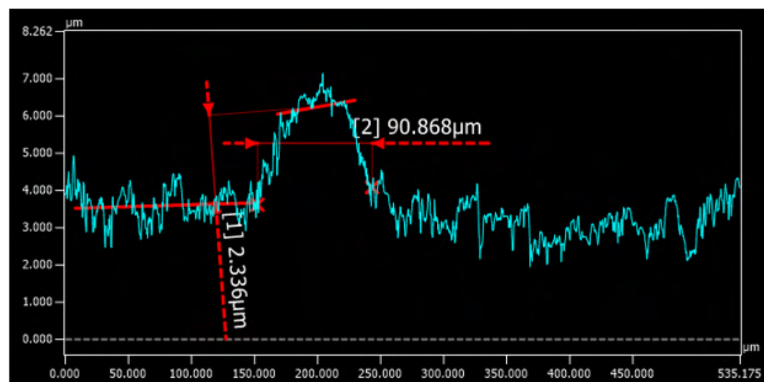


(b)

Figure 4.17 Profilometer cross section measurements of (a) the PI substrate with vias included (25-29μm) and (b) the width and thickness of the microstrip lines in Fig. 4.16 (90μm and 2.3μm).

CHAPTER 5

INTEGRATING RF AND MMIC DIES INTO TRANSFERRED LAYERS

With a process for transferring AJP structures established, we can turn to the next step in developing this process for general use in RF systems. Integrating RF and MMIC dies into the transferred structures is a key capability to draw out the utility of the process, allowing us to take full advantage of both the improved system manufacturing yield from individually verified components and the improved component yield from the selective post processing of pre-assembled printed layers.

5.1 The Transfer Process for NEA-121 Dielectrics

Since using PI as a dielectric substrate material lead to many manufacturing defects due to the post processing conditions and surface adhesion characteristics, it was decided that a new material should be selected to fill this role. This material should be AJP compatible, not require high post processing temperatures, and have reasonable adhesion characteristics on glass or metal printing substrates. Norland Adhesive's NEA-121 UV curable resin was chosen for its previously demonstrated AJP compatibility [45] and the ability to thermally and UV cure the material. The thermal cure begins at 120°C, which is significantly lower than the 300°C required for PI, and the UV cure can be done at room temperature as the material is deposited using AJP. Development steps and process parameters are provided in Appendix B.

A mechanical test structure was fabricated for alignment and release testing on an FR-4 board. The structure was a port-to-port thru test package with a passivated MS line run over a central plateau simulating the die foundation layer (Fig. 5.1). The major steps of the printing procedure are shown in Fig. 5.2. Starting with a glass printing substrate, first the pads are deposited using EI-615 reactive silver ink. The die foundation layer, including slot vias, is placed next, followed by a round of silver deposition to metalize the via walls and foundation top surface. A via fill step using NEA-121 is done to planarize the foundation layer and the surface is metalized again. Finally, the dielectric substrate layer is deposited followed by the surface metal trace and the passivation layer. A table of typical layer thicknesses is given in Table 5.1.

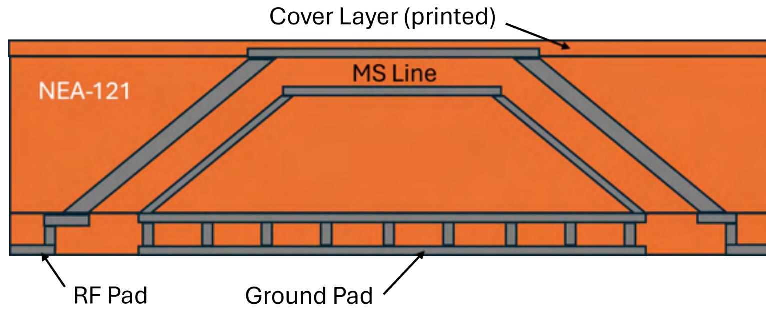


Figure 5.1 Cross section of the proposed port-to-port thru test structure. An MS line is used to set a performance benchmark for printed packages, including the effects of interconnects, vias, and RF pads.

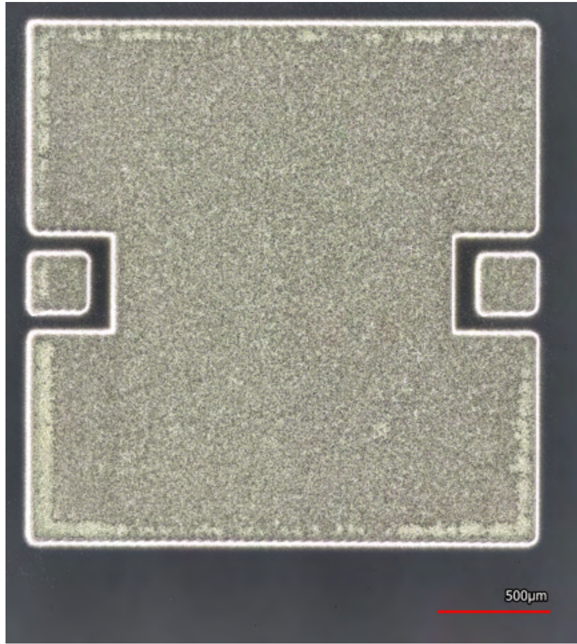
Table 5.1 Layer thicknesses of the Mechanical Test Structure

Layer Name	Printed Material	Measured Thickness (μm)
Pad Metal	EI-615	2.8
Die Foundation	NEA-121	62
Foundation Ground Plane	EI-615	3+/- 0.5
Dielectric Substrate	NEA-121	30
MS Trace	EI-615	9.0
Passivation	NEA-121	10

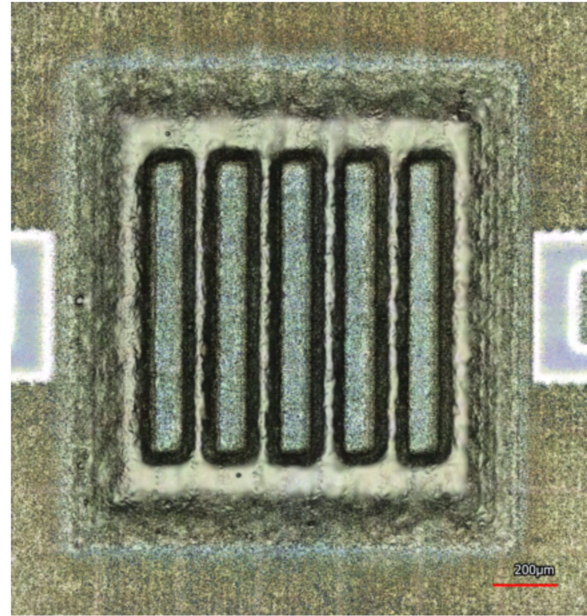
The transfer was carried out using a custom printed PDMS stamp holder that was fitted to the spindle of a Tresky T-5300 die bonder tool. EPO-TEK H20E conductive epoxy was applied to the PCB mounting pads prior to transfer to act a conductive adhesive material. The structure was first transferred onto the stamping tool by releasing from the glass printing substrate with a razor and collecting it onto the PDMS stamp. The stamp was then mounted to the die bonder spindle and aligned to the PCB. The stamp was landed and maintained 30g of force while the platen temperature was raised to 150°C for 45 seconds to cure the EPO-TEK bond layer.

5.1.1 Package Foundation Layer Considerations and Design

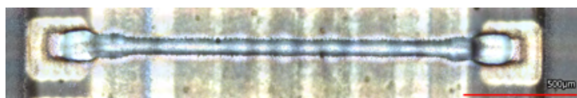
The die foundation layer serves as both a structural support for the packaged die as well as an interface that must channel heat away from the die. It also must connect the die ground plane to the package ground pad for proper RF grounding. The layer should be as thin as possible for the thermal considerations, and contain vias to improve conductivity across the dielectric. Early iterations of the design include a 50-60μm thick dielectric foundation that is perforated with channel vias as



(a)



(b)



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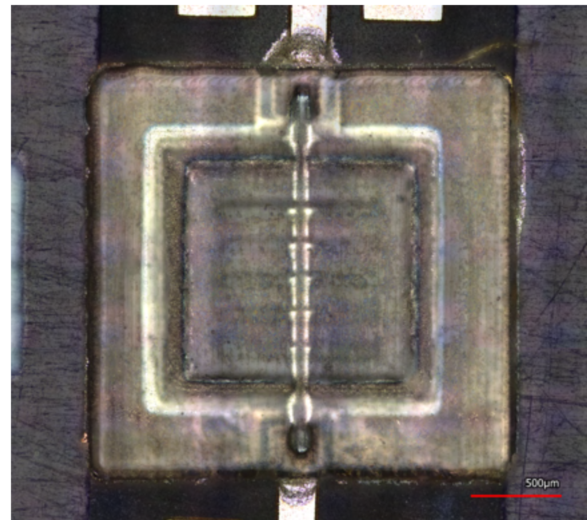
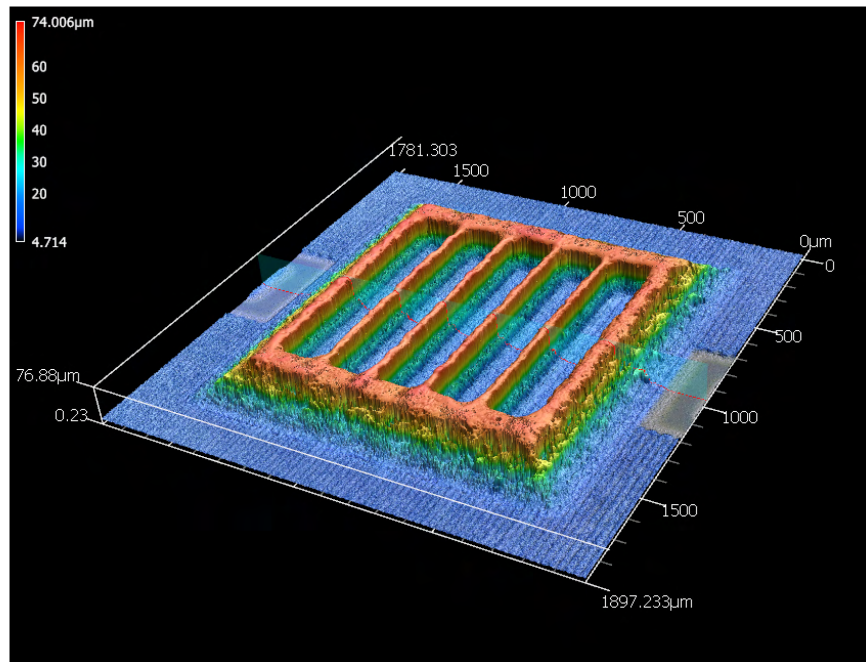


(d)

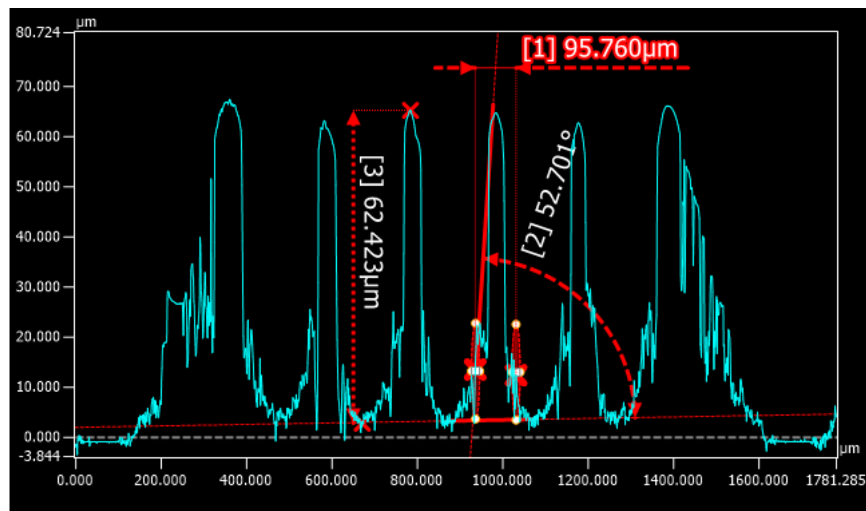
Figure 5.2 The major steps of the printing sequence for the mechanical test transfer structure. (a) is the pad layer, (b) is the foundation dielectric, (c) shows the MS line on the printed substrate, and (d) shows the package after transfer to the FR-4 board.

in Fig. 5.3. These channels are then metalized by spraying silver (EI-615) across the entire area, including the higher regions. The via channels are filled with NEA-121 using a platen temperature of 80°C and low power UV exposure to increase the time the material spends at a lower viscosity, which leads to better planarization of the material.

On experimenting with via fill techniques, it was determined that this layer should be reduced



(a)



(b)

Figure 5.3 Profilometer scans of the chip ground foundation layer. Trench vias are formed in the foundation to provide thermal and electrical conductivity to the carrier ground.

in thickness to a maximum of 10μm in order to lower the height deviation at the peaks of the via channels. This also reduces the length of the thermal path to the heat sink, and makes the via fill step and subsequent die attach step more reliable.

5.2 Port-to-Port Package Thru Line

Using the information gained in the mechanical test package fabrication, a port-to-port thru line package was designed to provide a benchmark for future die packages. The updates to this component include a switch to a CPWG line with channel vias to connect the coplanar ground planes to the substrate ground for improved mmWave performance. Additionally, liftoff testing on different NEA-121 test samples determined that adhesion to the glass printing substrate was mostly determined by the contact area between the NEA-121 and the glass. This meant that if the dielectric substrate layer extended beyond the silver pads, the adhesion between the part and the glass would be too great to release the part using the PDMS stamp adhesion alone, and partially destructive methods like razor blade release would be required to lift up the part. This often leads to damage to either the dielectric substrate or the large ground pad on the bottom of the package. Since the silver ink has a lower adhesion to glass, it was hypothesized that preventing a large contact area between the NEA-121 and the glass could be achieved by over sizing the pad metal regions. The result of all of this is the port-to-port thru package in Fig. 5.4.

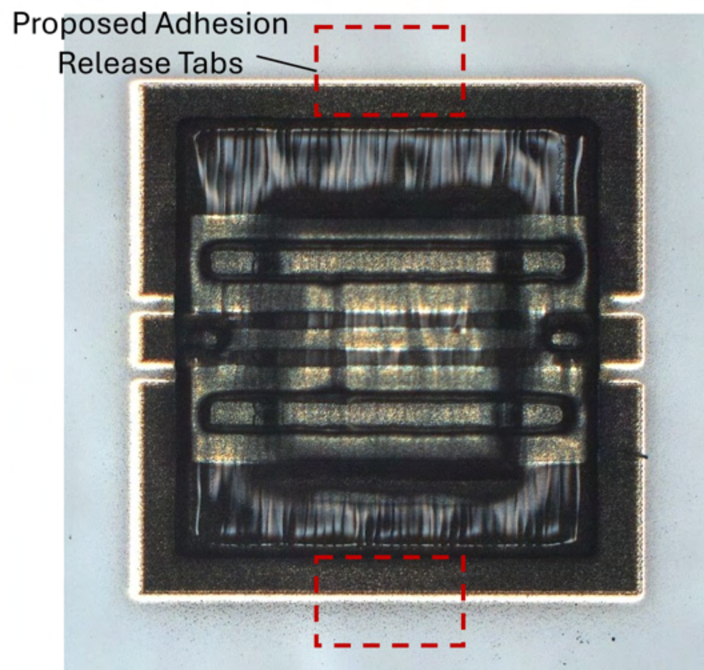
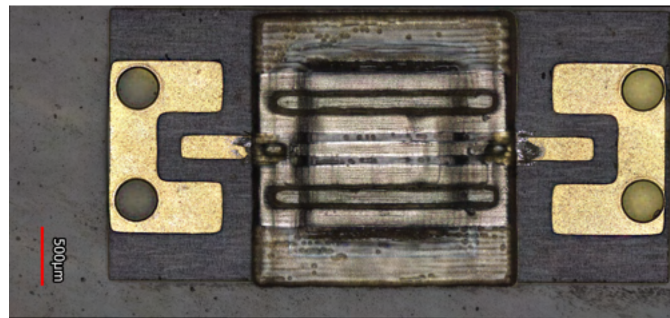


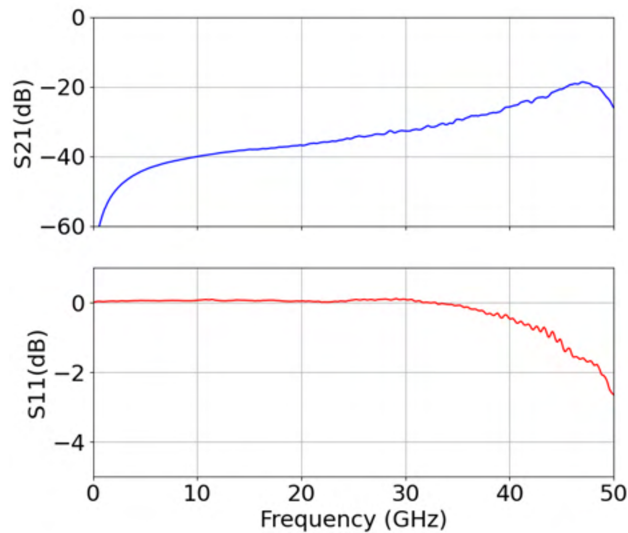
Figure 5.4 A port-to-port thru structure with a central CPWG line. The CPW ground planes are connected using channel vias through the substrate layer to the foundation ground layer. The dotted lines show the area for the proposed adhesion tabs.

While this did give the intended result of lower adhesion, several of the parts partially released without prompting after the final round of curing. Using small area tabs of NEA-121 to increase the adhesion and prevent early release of the structure would allow for some tailoring of the required release force, providing a noncritical area of material that may be cut without damaging the part if necessary.

After transfer to a PI flex PCB, S-parameter measurements were taken. Fig 5.5 shows the results of this process.



(a)

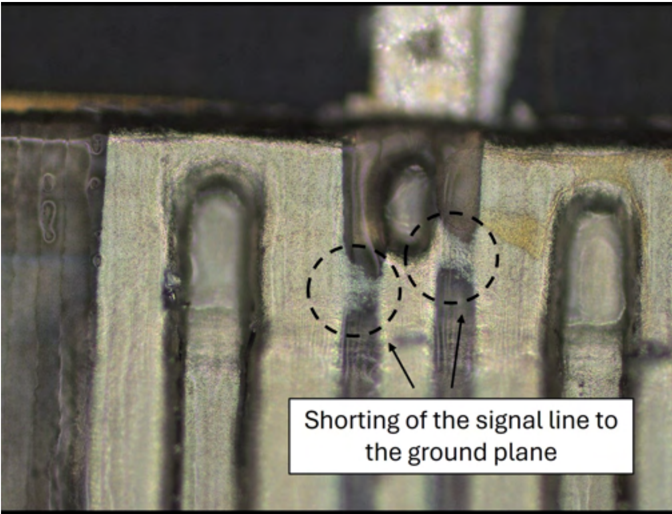


(b)

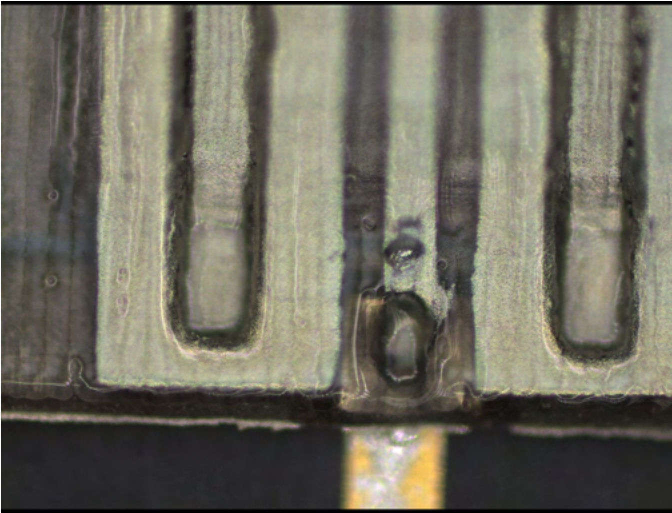
Figure 5.5 (a) A port-to-port thru test package after transfer onto a polyimide substrate flex PCB. (b) S-parameter measurements of the transferred test package.

While the mechanical aspects of the transfer were successful and no detectable shorting from the EPO-TEK attach material was observed, the RF performance is significantly degraded by in-package

defects. Of the test packages that were printed, all were defective due to unexpected ink spreading of the EI-615 on the ground planes of the CPWG. Fig. 5.6 shows a close up of the electrical shorting caused by the ink flowing into the signal pad vias, connecting the ground and signal metals. This failure mode places a limit on the proximity of unconnected metals to printed vias, and can only be addressed in the long term by re-evaluating the post-processing procedures or printing conditions.



(a)



(b)

Figure 5.6 (a) A shorted signal line caused by silver ink flowing into the via well during curing. (b) The intended line geometry for reference.

5.3 Package Design for mmWave ICs

Package design for mmWave frequencies typically involves minimizing interconnect parasitics, whether that be offsetting inductive effects for wire/ribbon bonds or optimizing via performance. Additive manufacturing techniques increase the available options for dealing with parasitic losses by allowing designs with more complex physical structures. This could include MS lines that run straight from the package pads to the die pads along a path that includes 90 degree bends or diagonal sloping, or resonant coupling structures where the required bandwidth is well defined and reasonably narrow.

This process will separate the package design into 3 layers for independent evaluation before recombining the designs at the end to form the full package. As shown in Fig. 5.7, these layers are; (i) the pad layer, where the package will attach to the PCB or other carrier substrate; (ii) the interconnect layer, which surrounds the die and includes all structures for mounting the die and bringing the signals from the pad layer to the die pads; and (iii) the cover layer, which encloses the die to protect it from the environment and can be used to form an air box if necessary. Using Ansys' Electronics Desktop HFSS, the relevant parameters of each component were optimized prior to full package modeling.

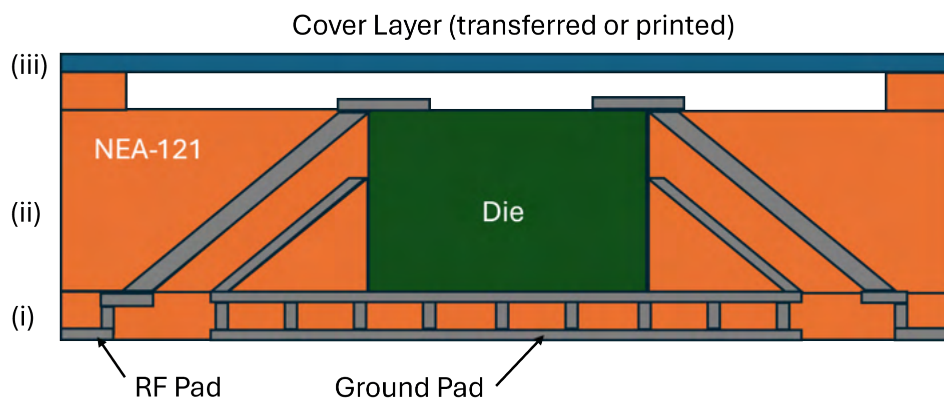


Figure 5.7 Cross-sectional view of the 0dB attenuator package model showing the different layers. (i) is the RF pad layer, (ii) is the interconnect layer, and (iii) is the cover layer.

One potential drawback of using AM techniques for die packaging is the potentially reduced thermal handling capabilities of printed materials. Thermal management is a critical part of any die

packaging strategy, as dies with components such as power amplifiers will generate large amounts of waste heat during operation. This places a power limit on the dies that may be packaged using this method, making the process more attractive for things like LNAs or IQ mixer dies that are optimized for receiving and producing low noise signals. As such, this formative work will focus on passive structures in order to develop key aspects of the process.

5.3.1 Pad Layer

The pad layer serves 3 important and interrelated functions. First, it must transfer the signals from the lower surface where the pads are located to the upper surface with minimal loss. Since this layer will be thin, a simple square via connection between the signal trace will be sufficient. The minimum size of this via affects the minimum pad size, and is set by the overspray width of the dielectric material as described in [39]. Second, it must provide structural support for the die and everything in the interconnect layer. The most important aspect of this function is that the pad layer be as close to planarized as possible. Any defects in this layer will propagate up the package as the interconnect and cover layers are printed or assembled, which could lead to an impact on performance or yield. Finally, the pad layer must provide adequate electrical and thermal grounding for the packaged die. This means that the printed vias under the die must be of a sufficient number and have thick enough metal walls to transfer the waste heat produced to the ground pad of the PCB.

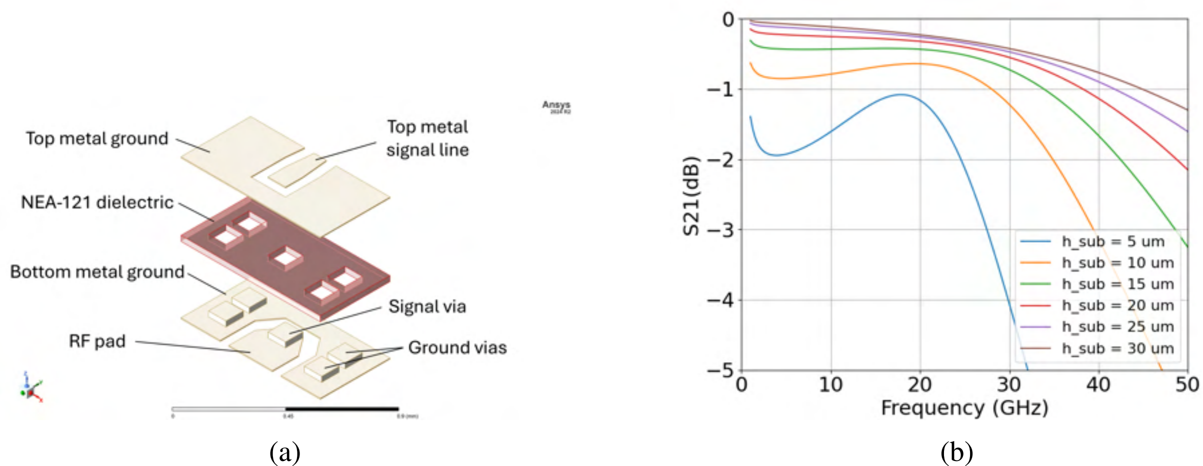


Figure 5.8 An RF pad model using a via transition. (a) Exploded model view for via visibility. (b) S-parameter simulations of an RF pad for a range of dielectric layer thicknesses.

A model of the RF pad structure is shown in Fig. 5.8, along with S-parameter simulation results. The thickness of the pad layer dielectric was varied from 5μm to 30μm to find the minimum thickness possible in an attempt to minimize the thermal resistance under the die. This showed the best performance at 30μm substrate thickness for the RF pads.

5.3.2 Interconnect Layer

The interconnect layer contains both the interconnect lines from the package pads the die pads and the die itself. The two key design aspects are the interconnect line format (MS, CPWG, SIW, etc.) including the losses induced by bends in the line due to vertical travel, and the die attach layer geometry. As the die attach was addressed in Ch. 3, here we will look at the losses due to interconnect bending. CPWG lines were chosen for their lower loss at mmWave frequencies as compared to MS lines.

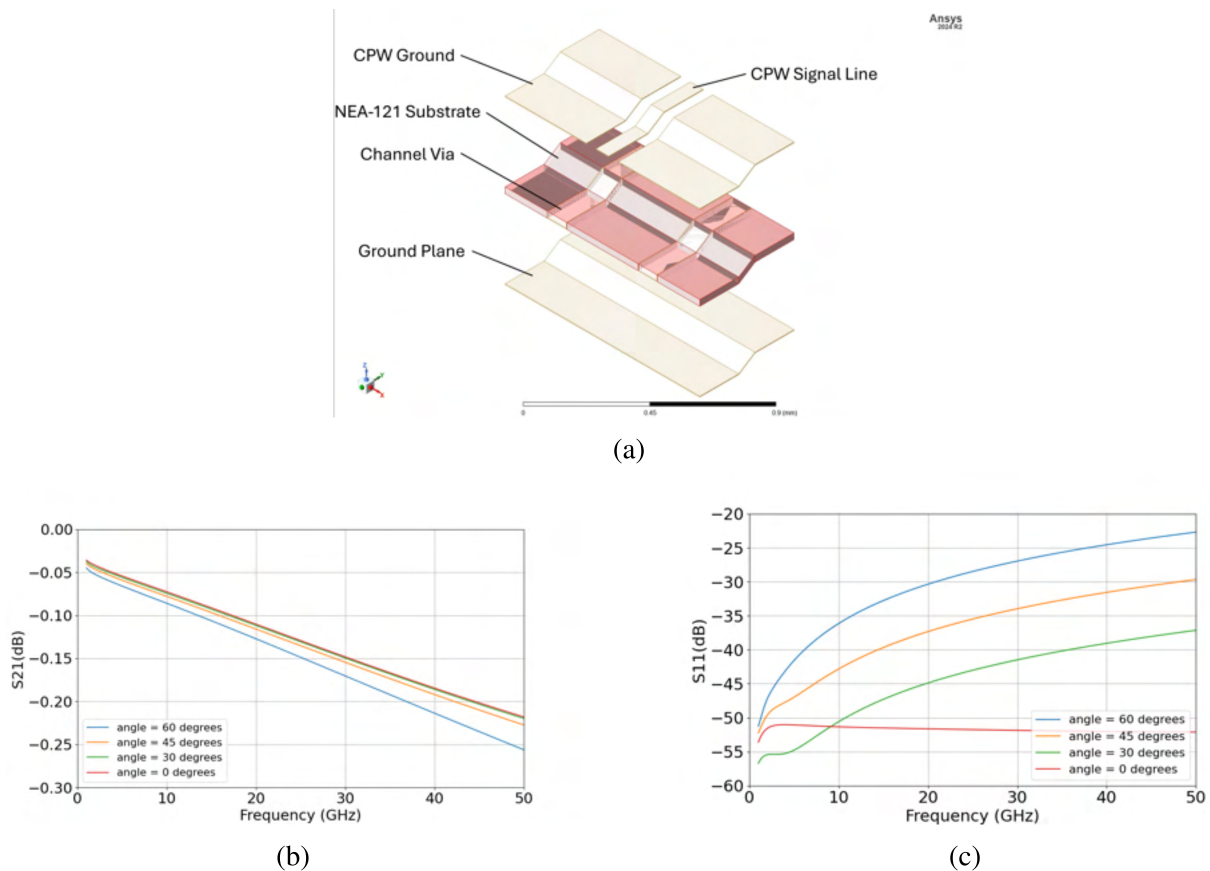
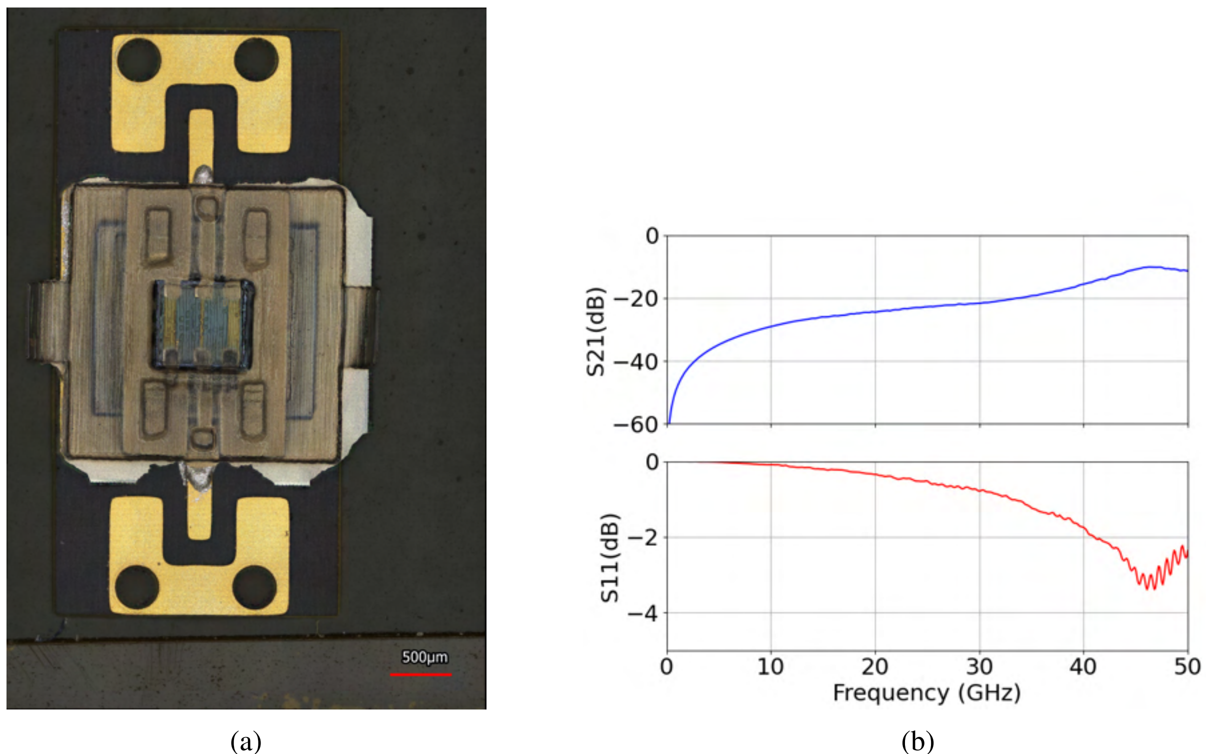


Figure 5.9 (a) An exploded view of the ramp interconnect model. (b) S21 simulation data and (c) S11 simulation data. The model shows minimal variation between ramp angles. 0° corresponds to a flat CPWG line.

A simulation was run to determine the effect of varying the angle, the model and results of which are given in Fig. 5.9. The effects of varying this angle reduce the signal by around 0.01dB in the 1-50GHz frequency range, indicating that the ramp is very tolerant to this sort of vertical bending.

5.3.3 0dB Attenuator Package Design

A 0dB attenuator package was designed and fabricated using the components modeled above and transferred onto a polyimide substrate flex PCB for measurement using a PNA. The completed package and measurements of the first attempt are shown in Fig. 5.10.



(a) (b)

Figure 5.10 (a) A 0dB attenuator die package after transfer onto a polyimide substrate flex PCB. (b) S-parameter measurements of the transferred die.

The mechanical aspects of the package transfer were again successful, with proper alignment and attach of the package with no significant damage due to the procedure. Again, a failure mode of the AJP process degraded the RF performance of the package, this time being an error in the method that the die interconnect ramps were formed. A large gap on one side of the die caused a break in the interconnect line, greatly reducing the performance. This will have to be addressed in

the future by developing methods such as dam-and-fill techniques for the printed NEA-121 material or improved repair strategies for bridging any remaining gaps around the packaged die.

5.4 Current State of the Transferred Packages

A process for transferring mmWave die packages has been baselined with all the key elements in place. It is clear from this work that with additional process development significant improvements in the electrical performance can be achieved to make this technologically competitive in the future. These packages, once functional, will bring much needed flexibility into AJP process space by providing the means for individual verification of system building blocks. The reduction in post-processing related thermal cycling will allow for greater yield on larger systems, while also allowing the use of AJP materials with otherwise incompatible host surfaces such as ABS plastics. While there is remaining work to be done, it is all related to AJP process and post-processing conditions, and is not inherent to the package transfer method itself.

CHAPTER 6

CONCLUSION

In this work, a variety of AJP techniques were investigated with a range of applications to RF and mmWave package design. The application of AJP to CiP packaging demonstrated the ability to produce functional Ku-band systems that mix both traditional PCB manufacturing and SMD technology with printed die fill materials and interconnects. Techniques to leverage AJP for improving these processes, such as the application of printed die attach layers, were also explored in order to ease issues such as die leveling or material compatibility. A transfer process was developed in which a PDMS stamp was used to move printed parts from the printing substrate to a target surface, be that a PCB or other surface, which brought the benefits of reducing the thermal stress of post processing on the target surface and lower layers in a stacked layer design. This transfer process was then applied to full IC packages in order to combine the benefits of AJP package manufacturing with traditional PCB manufacturing. These transfer packages lay the ground work for fabricating IC packages at higher frequencies than were previously possible, making W-band and above packaging theoretically achievable with this technique.

6.1 Future Work

6.1.1 LNA Transferred Package

The next step with the transferred package process is to package an active die. An LNA is a good candidate as it benefits from low loss interconnects and does not generally produce a large amount of waste heat. The printed package design (Fig. 6.1) can include any biasing network components such as SLCs, provided they are roughly on the order of the die in thickness.

Measurements of interest include small signal gain and noise figure, both of which are directly influenced by the loss introduced by package interconnects.

6.1.2 Functionalized Die Cover Layers for System-on-Package Assemblies

Looking forward, the application of transferable layers to printed packages provides an interesting route to SoP devices where the cover layer of the package may be functionalized, allowing for very compact system assemblies. The most obvious of these involve mounting either a filter or

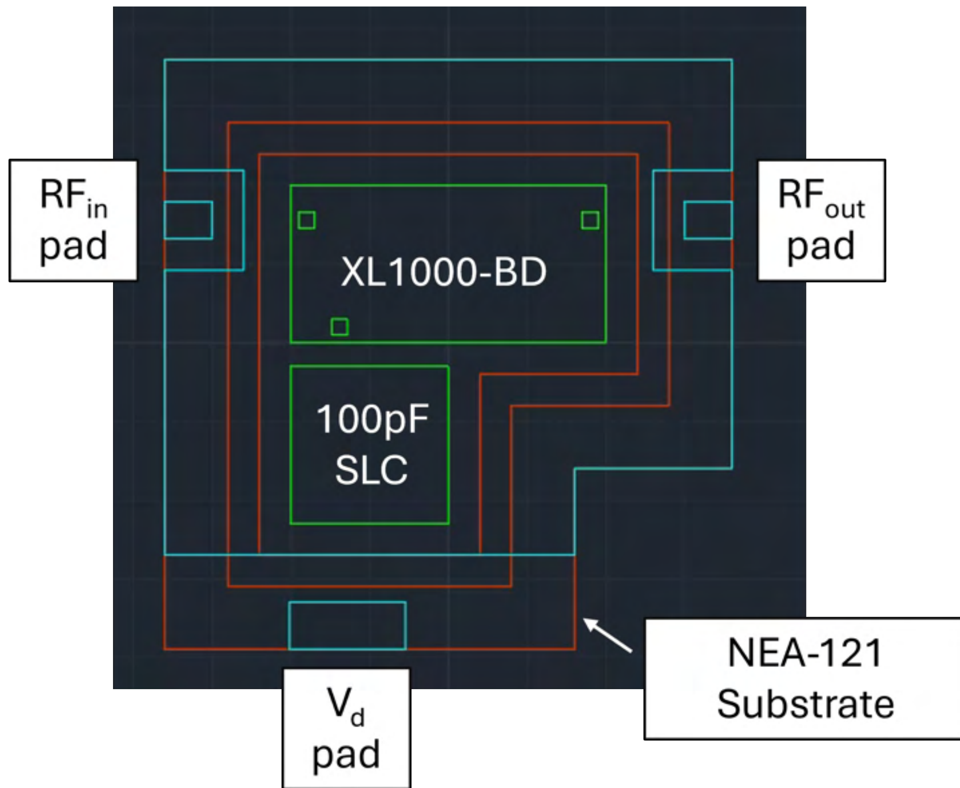


Figure 6.1 A layout sketch of the proposed LNA package including an XL1000-BD LNA die and an SLC.

antenna element to the top of the package in order to minimize the distance between these elements and the IC. This would also allow for more routing options, as package interconnects could be run through the cover layer to a pad on the opposite side without requiring a close proximity jump over intersecting RF or high current DC lines. Such a capability would go a long way towards generalizing certain package pad layouts for multiple IC designs without sacrificing the flexibility that comes with AM.

Additionally, low power dies without a significant thermal output could be stacked above any amplifiers on the carrier plate level, potentially minimizing the system size to the area of the largest die footprint. The biggest challenges with such setups would be the vertical interconnect strategy. Whether these take the form of 90° bends in printed MS or CPWG lines or some sort of resonant coupled structure remains to be investigated. Additional routing between separate die stacks could potentially be performed above the carrier level by transferring suspended transmission line substrates to well aligned die stacks using flexible materials such as PI or NEA-121. Overall, the

transfer process opens many doors to potential applications for AJP without the need for developing suspended printing processes or materials with extra gentle post processing procedures.

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APPENDIX A

AJP MATERIALS

AJP materials are primarily organized into dielectric and conductive materials. Due to the nature of AJP manufacturing, many of the deposited materials do not have identical properties to what is listed by the manufacturers for bulk materials. Several techniques were investigated for relevant material parameter extraction, the most useful of which will be described here.

A.1 Conductive Inks

The parameter of interest for our silver inks is conductivity. In order to measure this, a series of 4-point structures were deposited on either glass or a polyimide laminate film as in Fig. A.1.

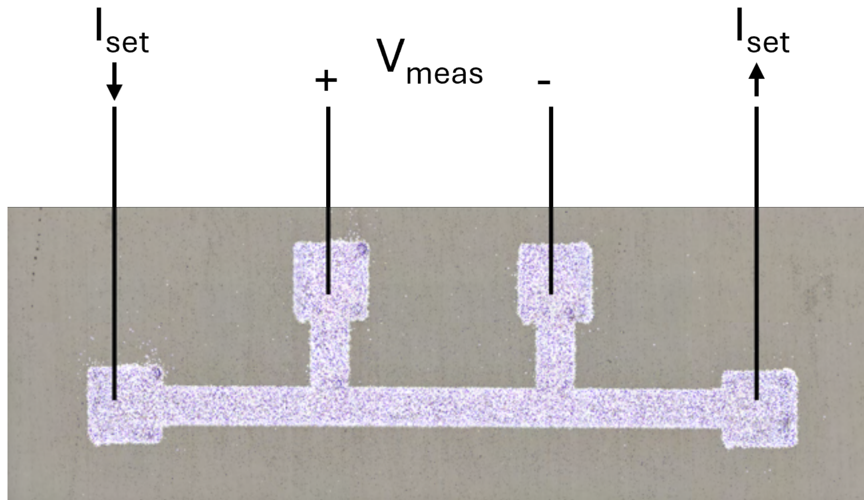


Figure A.1 A 4-point conductivity measurement structure used to extract the conductivity of printed metals.

A constant current is applied to the I_{set} terminals and voltage measurements are taken at the V_{meas} terminals. Each structure has a slightly different spacing between the V_{meas} terminals in order to obtain multiple data points.

Once the resistance is calculated from the slope of these measurements, the conductivity can be approximated for a line of uniform thickness using

$$\sigma = \frac{lI_{set}}{V_{meas}A} \tag{A.1}$$

where l is the length between voltage pads and A is the cross sectional area. The silver inks used in this work have a measured conductivity of 15-20% bulk silver.

Another important aspect of the conductors for RF and mmWave frequencies is skin depth. This is the distance into the material that most of the microwave power is carried in, and is given by [46]

$$\delta_s = \sqrt{\frac{2}{\omega\mu\sigma}}. \tag{A.2}$$

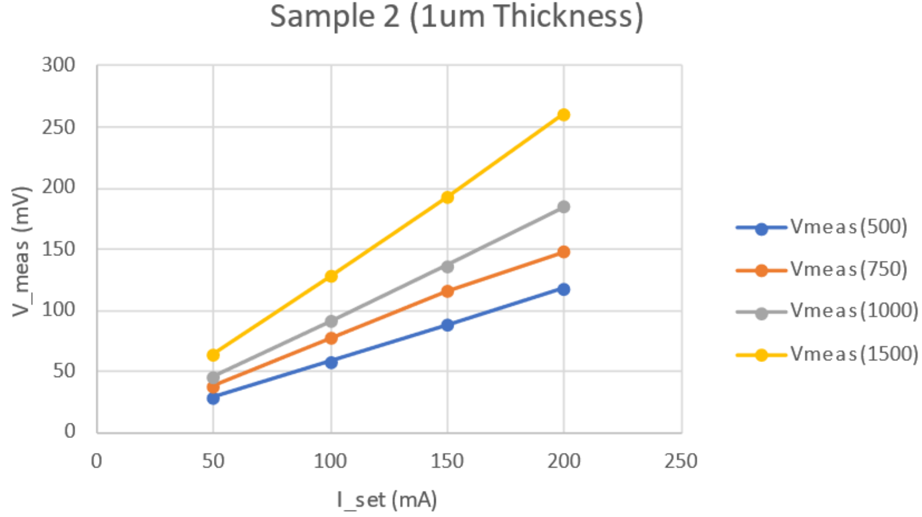


Figure A.2 Measurements taken from the structure in Fig. A.1 for Prelect TPS50G2 silver nanoparticle ink.

This sets a minimum limit on the thickness of printed metals for a given frequency. In practice, the printed metals should be thick enough to compensate for the large amount of surface roughness inherent to AJP deposited materials.

A.2 Dielectric Inks

The properties of the dielectric materials that are interesting are the permittivity and the RF loss tangent. Since it is very difficult to untangle all of the other sources of loss, mainly the conductor loss which is dominate in our printed structures, and since dielectric loss is only a minor effect in the frequency ranges of interest, only the permittivity will be extracted here.

Two methods were attempted to achieve this. The first was to use a printed gap coupled ring resonator as shown in Fig. A.3.

The ring resonator is weakly coupled to the RF port by the coupling arms and produces a set of resonant peaks when measured, given by the equation

$$f_n = \frac{nc}{2\pi r\sqrt{\epsilon_{eff}}}. \tag{A.3}$$

where ϵ_{eff} can be approximated for an MS line as

$$\epsilon_{eff} = \frac{\epsilon_r + 1}{2} + \frac{\epsilon_r - 1}{2}\frac{1}{\sqrt{1 + 12\frac{d}{W}}}. \tag{A.4}$$

Using these, we can calculate the expected first resonant frequency for a given ring radius and compare with the measurements to find the difference in the actual dielectric constant of the AJP material and the listed dielectric constant for the bulk material.

The ring must be weakly coupled, and the S21 measurement is very close to the instrument noise floor as seen in Fig. A.4. This, combined with the uncertainty in the gap width due to variable printer line width, makes the structure somewhat less attractive for this sort of parameter extraction.

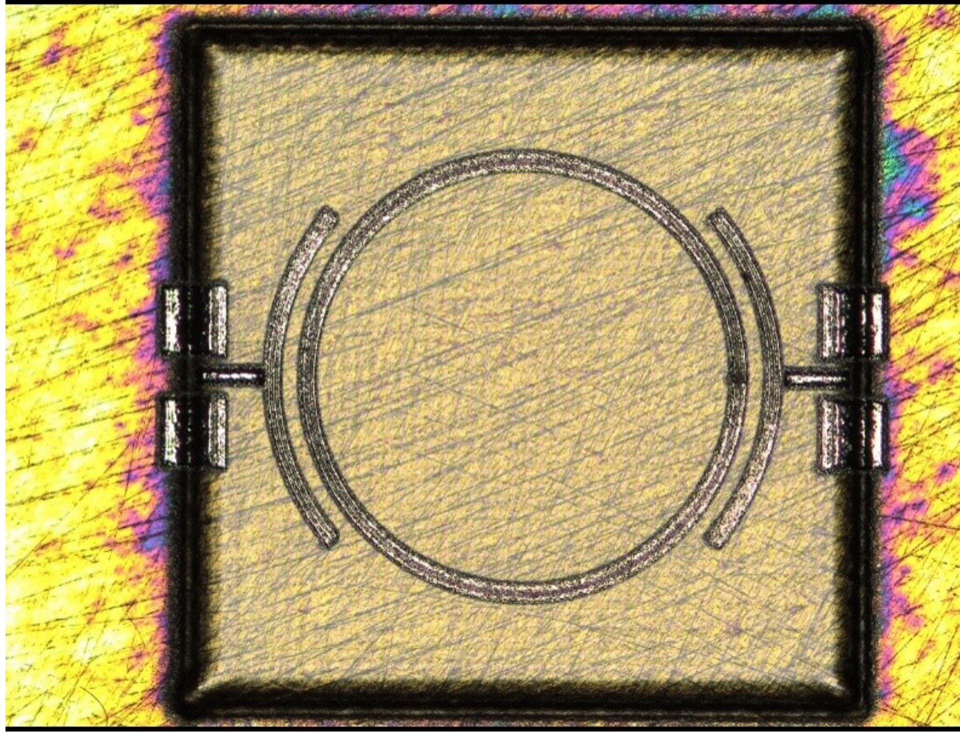


Figure A.3 A gap coupled ring resonator used to extract the dielectric constant of the substrate material at a single frequency.

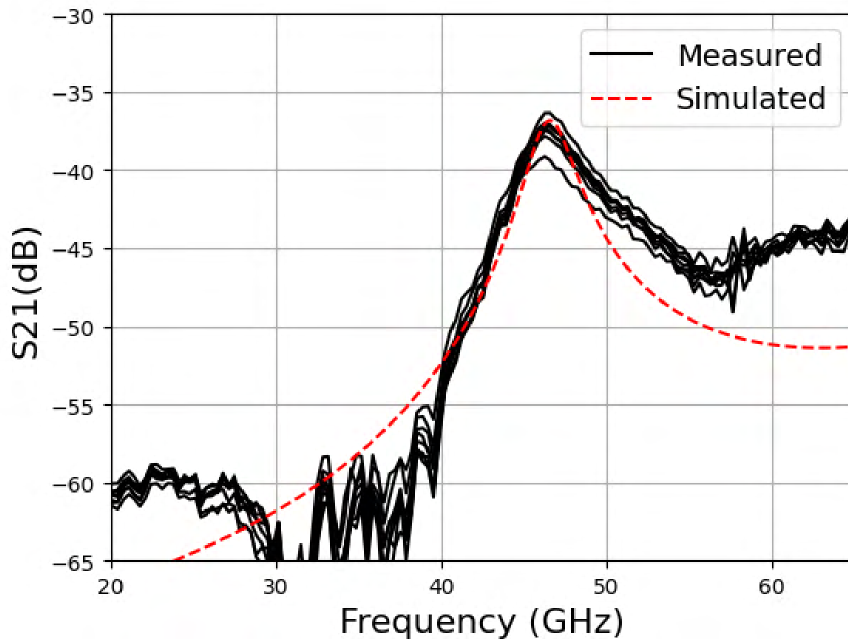


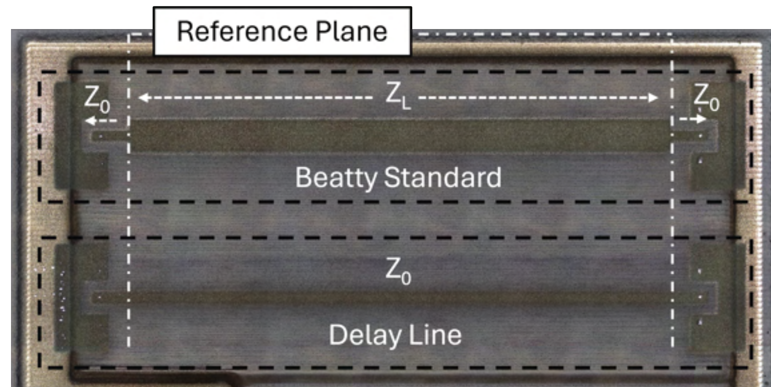
Figure A.4 S21 measurements of the fabricated ring resonators.

Another method to extract the dielectric permittivity is to use a Beatty standard MS line [42].

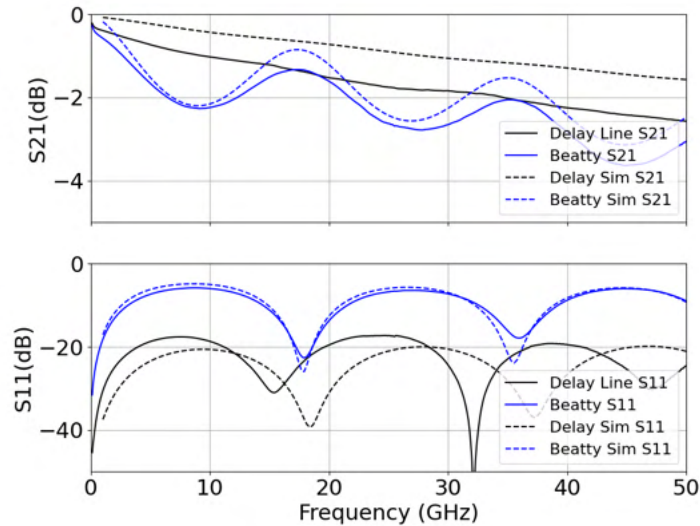
This method involves creating a transmission line structure which contains an electrically long, low impedance segment in the center to create a resonant effect which will be measurable in the S-parameter data. It is often helpful to compare these measurements with a delay line of equal length to ensure that the Beatty Standard is behaving as expected. Fig. A.5 shows the lines that were used to characterize NEA-121, where the low impedance segment Z_L is 3 times the width of the 50Ω impedance segments indicated by Z_0. The resonant frequencies for this structure can be estimated by [47]

$$f_n = \frac{nc}{2L\sqrt{\epsilon_{eff}}} \tag{A.5}$$

where L is the length of the low impedance segment.



(a)



(b)

Figure A.5 (a) The Beatty standard and delay line used for dielectric constant extraction of NEA-121 from 0-50GHz. (b) S-parameter measurements of the lines compared to a simulated model. The adjusted dielectric constant from frequency peak matching is $\epsilon_r = 3.6$.

By comparing a simulated Beatty line with the measurements from the printed Beatty line, we can match the resonant peaks by varying ϵ_r in the simulation's material model. Fig. A.5.b shows the results of this process for NEA-121, where the model ϵ_r was adjusted from 4.04 to 3.60 to match the measurements.

A.3 Material Interactions

One final consideration for AJP materials is what happens when you stack several materials on top of one another. This is common in multi-layer structures, where typically a metal plane will be deposited onto a dielectric resin or vice versa. Aside from the potential adhesion issues laid out in Ch. 4, there may also be chemical interactions between the solvents or solutes of any combination of inks. For example, Fig. A.6 shows the interaction between nanoparticle silver and reactive silver inks when an interconnect repair attempt was made. Depositing the nanoparticle ink onto the already present reactive ink caused the interconnects to peal and ribbon curl. Material interactions should always be verified before they are used in an assembly involving AJP processing.

Figure A.6 Printed silver line pealing effect caused by mixing nanoparticle ink with reactive ink.

APPENDIX B

AJP PROCESS PARAMETERS AND DEVELOPMENT PROCEDURE

Developing process parameters for AJP starts with ink selection. Every ink will have different behaviors based on viscosity, solvent content, and print surface interaction. Some materials may need to have one or more of these parameters adjusted by heating, stirring, or surface treatment. Proper surface preparation can make the difference between a part that fails 7 steps in and a part that functions perfectly at the end of the print. For example, polyimide ink has a very high failure rate if used as the first layer on glass without first treating that glass with a thorough acetone/isopropanol rinse and properly mixed adhesion promoter. Even with this, the high solvent content can still cause inter-layer bubble formation if the curing cycle is not ramped at the slow rate of 2°C per minute.

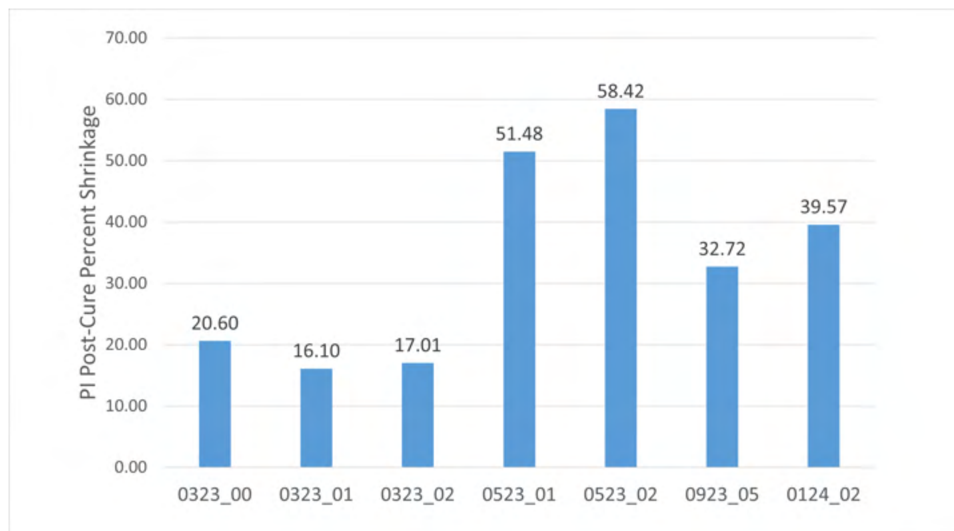


Figure B.1 A chart plotting PI post cure shrinkage for several parts fabricated using the ink over the course of a year. Tracking down the source of this variability is often difficult for inks with volatile solvents, leading to a high rate of ink turn over without actual use.

Solvent content also significantly effects the final dimensions of the post processed parts, sometimes in less than predictable ways. For example, the PI ink used in this work has a high NMP solvent content of approximately 60%. The post cure thickness was often as much as 50% of the measured thickness before curing. Fig. B.1 shows the shrinkage from a set of samples taken over the course of a year. The source of this variance is difficult to pin down, with contributing factors including uneven solvent mixing, solvent evaporation during atomization, or even variable room atmosphere conditions.

With all these things in mind, it should come as no surprise that developing the process inputs for AJP is a highly ink dependent endeavor. A list of process inputs and post-processing recommendations for various inks used in this work are given here. While these inputs are representative of what was used during fabrication in the work, it should be known that they are highly variable from machine to machine and may even drift significantly over the course of a print session.

EI-615 post-processing steps:

Table B.1 Typical Process Parameters for EI-615 reactive silver ink using a platen temperature of 60°C and a Process Speed of 1.5mm/sec

Tip Diameter (μm)	Sheath Flow (SCCM/psi)	UA Flow (SCCM/psi)	Measured Linewidth (μm)
150	45/0.45	14/0.42	30
250	90/0.20	12/0.17	50
300	100/0.11	11.5/0.02	100

1. Cure on hotplate at 150°C for 15 minutes every 5μm deposited or before covering with another material
2. Bake in oven at 150°C for 1 hour after printing for the part is completed

Table B.2 Typical Process Parameters for Prelect TPS50G2 silver nanoparticle ink using a platen temperature of 23°C and a Process Speed of 1.5mm/sec

Tip Diameter (μm)	Sheath Flow (SCCM/psi)	UA Flow (SCCM/psi)	Measured Linewidth (μm)
150	65/1.03	23/2.31	30
200	65/0.39	35/0.66	60

Clariant Prelect TPS50G2 post-processing steps:

1. Bake in oven at 180°C for at least 3 hours before covering with another material

Note: Back filling the oven with an inert gas will prevent the material from curing properly and result in low conductivity.

Table B.3 Typical Process Parameters for PI AJP ink using a platen temperature of 50°C and a Process Speed of 2mm/sec

Tip Diameter (μm)	Sheath Flow (SCCM/psi)	PA Flow (SCCM/psi)	EX Flow (SCCM/psi)	Measured Linewidth (μm)
300	100/0.25	850/3.85	800/0.28	80

PI post-processing steps:

1. Dehydration bake on a hot plate at 200°C for 5 minutes every 10μm of thickness deposited
2. Cure in oven at 300°C for 1 hour, limiting the temperature ramp to 2°C per minute

Note: Back fill the oven with nitrogen or other inert gas as the presence of oxygen will affect the RF properties of the cured material.

BCB post-processing steps:

Table B.4 Typical Process Parameters for Cyclotene 3022-35 using a platen temperature of 50°C and a Process Speed of 2mm/sec

Tip Diameter (μm)	Sheath Flow (SCCM/psi)	PA Flow (SCCM/psi)	EX Flow (SCCM/psi)	Measured Linewidth (μm)
200	60/0.39	650/3.05	625/0.0.38	40

1. Allow this material to sit on the heated platen for at least 60 seconds between printed layers to avoid excessive sloshing of the material during deposition
2. Cure in oven at 250°C for 1 hour, or 200°C for 10 hours depending on the limitations of other printed materials on the part

Note: If an electrically large area of BCB is being used as a dielectric substrate, it may be wise to back fill the oven with an inert gas such as nitrogen to preserve the RF properties of the material.

Table B.5 Typical Process Parameters for NEA-121 UV resin using a platen temperature of 60°C and a Process Speed of 2mm/sec

Tip Diameter (μm)	Sheath Flow (SCCM/psi)	PA Flow (SCCM/psi)	EX Flow (SCCM/psi)	Measured Linewidth (μm)
250	90/0.28	1100/7.12	1050/0.31	70
300	100/0.18	1000/4.80	930/0.21	100

NEA-121 post-processing steps:

1. Select a UV intensity appropriate to the desired outcome when using UV light during printing (see note)
2. Curing may be completed by either exposing the material to 365nm UV light at 200W/linear inch for 5-30 seconds
3. Curing may also be completed by baking the material in an oven at 120°C for 10 minutes

Note: A higher UV intensity will help with the edge definition of printed parts but will increase surface roughness. If a smoother surface finish is desired, lowering the UV intensity for the final printed layer can help achieve this at the cost of edge definition.