POWER-AREA EFFICIENT RAPID-RESPONSE CMOS FRONTEND FOR HIGH-THROUGHPUT ION-CHANNEL SENSOR ARRAY MICROSYSTEMS

By

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ABSTRACT

POWER-AREA EFFICIENT RAPID-RESPONSE CMOS FRONTEND FOR HIGH-THROUGHPUT ION-CHANNEL SENSOR ARRAY MICROSYSTEMS

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From the dawn of the nineteenth's century, pioneers such as Faraday have been studying the effects and consequences of charge transfer on chemical reactions. This field is now widely recognized as electrochemistry. The fact that thanks to electrochemistry tracking a reaction and imposing one has become so feasible has spawned a new wave of electrochemical enabled sensors for various applications from personal health tracking to mine safety monitoring. The next logical leap for electrochemical sensing would be to expand to single molecule detection and control. However, fundamental limiting factors in electrochemistry such as probe size and noise impose restrictions on the number of individual tracked molecules. One way to mitigate this issue is through the use of nano-sized holes that allow for the target molecule to pass through them called nano-pores. This dissertation discusses the principals of nano-pore sensing with a focus on interfacing requirements and principals and provide the reader with a solution for interfacing ion-channels (a sub-category of nano-pores) in an array form. The goal is to understand the conditions that would facilitate proper detection and the CMOS approach that would help us do so. Section 1 will focus on varieties of nano-pores and the definition and operation principals of ion-channels. Section 2 will focus on challenges interfacing these ion-channels and solutions from literature. Section 3 will focus on an array challenges implementing an array of ion-channels and provide unique solutions. Chapter 4 describes a test chip implemented to test the solution proposed in chapter 3 and provide users with test results supporting our claims.

Dedicated to my adorable nieces Anil, Sevilay and Lara.

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1. Introduction to nano-pore sensing

1.1. The definition of nano-pores and their significance literature

Recently great research effort has been put into chemistry-enabled sensing systems such as air pollutant detectors, biosensors for antibody detection as well as more complex emerging areas such as silicon nano-wires [1] and carbon nano-tubes [2]. All these methods are subsets of a greater family called electrochemical sensors. Electrochemical sensors utilize tracking and exploit charge transfer in chemical reactions for discovering a sensing target. In recent years, new opportunities for mainstream utilization of these techniques are emerging throughout the literature. For example, electrochemical sensing has received a lot of attention in developing biosensors in the recent years [3][4]. They are also being used in fields such as environmental sensing, safety monitoring and clinical diagnosis in both stationary and portable systems. The popularity of electrochemical sensors is due to reliability, simplicity, low cost, and portability of these systems [5]. Electrochemical bio-sensors are a subset that associate with and detect a biological event or a marker using charge transfer. Amperometric electrochemical biosensors detect this event by receiving the said charge through an electrode, and transducing it into a current signal.

The information retrieved from electrochemical biosensors is usually integrated over a large number of charge transfers and integrated over time from individual electrodes [6]. This is however, contrary to the growing demand for tracking the charge transfer of individual molecules in a quantitative manner. This is not possible with traditional electrochemical systems due to the fact that electrochemical electrodes form a layer of charge known as double layer capacitance on their surface shared with the solution. This capacitance is noisy and thus masks the passing of low doses of charge created by a single molecule electrochemical event [6].

To enable single molecule electrochemical detection, several methods have been proposed including redox cycling, Nano-particles and nano-pores. A nano-pore is basically a nano-scale sized path for charged or neutral particle transfer with well-defined flow characteristics [7]. The operation principles of nano-pores revolve around the fact that an open pore can demonstrate constant ion flow under the right circumstances and any disruption to this flow would be detectable. One way to utilize this configuration for detecting particles is to observe the changes in charge flow through the nano-pore due to the presence of particles with certain sizes. Furthermore, this method can also be utilized to observe the behavior of the nano-pore under certain environmental and internal stimulation conditions, enabling characterization of the pore. Nano-pores have been reported for use in fields including single molecule bio-sensing and protein detection and ultrafast label free DNA sequencing [8][9] as well as more specific aplications such as detection of microRNAs [10], measurement of molecular forces [11] and identifying Anthrax toxins [12]. As the demand to bring these technologies to the mainstream advances, there is a growing need for better understanding of nano-pores and their interfacing circuitry. The next sections of this chapter discuss the structure of nano-pores, especially ion-channel proteins, and overview some of the challenges in developing electronic interfaces for nano-pores.

1.2. Nano-pore types and introduction to ion-channels

Two main types of nano-pores are currently being used for amperometric measurements: ion-channels and solid-state nano-pores. The first practical implementation of nano-pores was detection of single stranded DNA molecules by passing them through a staphylococcal α-haemolysin ion-channel protein acting as a nano-pore gate [13]. An ion channel is a pore-forming membrane protein that form on cell's bilayer lipid membrane (BLM). A BLM is a continuous sheet that forms a barrier around the cell and is populated with membrane proteins that are responsible

for communication with the outside world. A typical BLM populated by various membrane proteins where each is performing a specific function is depicted in Figure 1-1. The bulk of BLM is composed of amphiphilic phospholipids that are hydrophilic on one tail and hydrophobic on the other side. Accompanying these cells are the membrane proteins that are anchored to the surface and perform various tasks. Ion channels are one class of membrane protein, and they are the fundamental excitable elements in most cell jobs include establishing a resting membrane potential and enabling action potentials by gating ions through the BLM. Thus, they are responsible for regulating cell volume and controlling ion flow across secretory and epithelial cells. Due to their rich history and ease of implementation, ion-channels are going to be the main focus of the presented thesis. Further details about the principals of sensing using ion-channels will be discussed in the coming chapters.

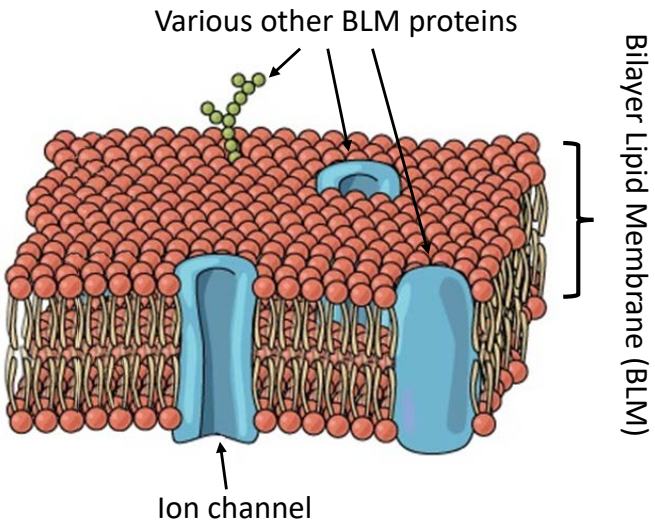

Figure 1-1 Typical BLM populated with various membrane proteins source.

Solid-state nano-pores are another approach to nano-pore sensing. Due to recent advancements in microfabrication techniques, it is possible to implement micro-fabricated solid-state pores with nano-meter sized openings. An example of a nano-pore created on a silicon nitride

surface is discussed in [14] and shown in Figure 1-2. These pores are typically implemented in dielectric materials such as glass, silicon dioxide (SiO_2), silicon nitride (Si_3N_4) and polymers [15] and shown in Two example methods for creating these openings are ion-bean sculpting to create pores at a Si_3N_4 substrate [16] and implementation of precise nano-pores in a SiO_2 substrate by shrinking a large hole (~20 nm – 200 nm) to single nano-meter precision using the surface tension created by high energy electron beam together with a visual feedback [17]. In terms of electrical properties and performance, there is not much difference between an ion channel and a micro-fabricated pore. Thus, throughout this chapter, the term nano-pores will generally refer to either of these structures.

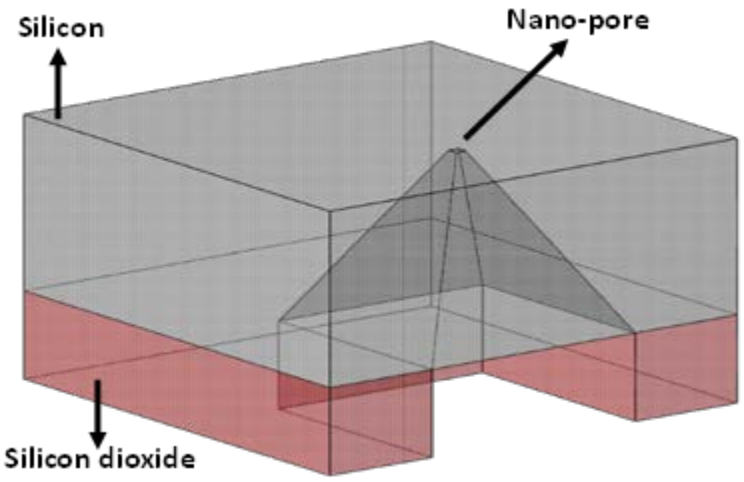

Figure 1-2 Solid-state nano-pore fabricated on a silicon substrate.

Ion-channels have been receiving a lot of attention within the last two decades [18]. It is worth stating that 15% of world's 100 top selling drugs target ion-channels [5]. Serious research is being put into turning such ion-channels into sensor modules due to them being capable of providing sensing continuously and label free with electrochemical techniques [19]. There are various instances of research is being conducted using ion-channels as a mean of sensing. [20] and

[21] are examples of efforts to utilize ion-channels on BLMs. Hence, the presented dissertation will primarily focus on methods for utilization and instrumentation of ion-channels.

1.3. Challenges in ion channel based sensing

Nano-pores transduce bio/chemical events into variations in ionic current flow that can vary in magnitude depending on factors such as the pore dimensions, viscosity of the analytes, capacitances stemming from the isolating layers or the electrodes, etc. Typically these ionic currents have an amplitude in pA region with timing characteristics, e.g. pulse width, as short as tens of microseconds. This imposes stringent limitations on the nano-pore interface system since the noise floor should at least be 10 dB lower than the signal level for it to be detectable. Hence a typical noise floor of fA levels is required for effective nano-pore sensing. For example, sodium ion channels typically have a conductance of 100 pS resulting in a current in the order of 10 pA when excited with a biasing voltage of 100 mV. As a result, they require a root-mean-square (r.m.s) noise level of less than 100 fA in a 1 kHz bandwidth [22]. Another example is a micro-fabricated glass and polyethylene terephthalate membrane that demonstrates an r.m.s. noise ranging from 5 pA to 25 pA, depending on membrane resistance, at a bandwidth of 40 kHz [23]. The benchmark instrument for current sensing in electrophysiology is the Axon Axopatch 200B, which provides a noise floor of 25 fA r.m.s. at 1 kHz frequency (0.7 fA/$\sqrt{\text{Hz}}$ until 1 kHz) [22]. However, this device is bulky, expensive and designed for specific lab environments and experienced users. The limited existing instrumentation has created an obstacle for the development of nano-pores sensor that exploit their capabilities for precision measurement and single-molecule detection. However, as discussed in the next section of this chapter, recent advancements in CMOS technology and microfabrication techniques have enabled the opportunity to utilize custom CMOS circuitry for

high-speed, low-noise, and cost effective customizable alternatives to interfacing with nano-pore sensors.

1.4. Thesis goals, planned contributions

The goals of this dissertation revolve around solutions for characterization of ion-channels and sensing ion-channel events with a focus on addressing the challenge of facing interfacing these ion channels through CMOS design. To drive this point home, through dissertation ion channel working principals and conditions, methods of utilizing these ion-channels from a physical and structural point of view, and the most effective readout methods will be studied. Scientific contributions are expected in the area of electrochemical instrumentation of ion-channels.

1.5. Thesis outline

Chapter 2 will focus on interfacing principals of ion-channels. Their electrochemical model and popular CMOS interfacing mechanisms will be discussed. Utilizing ion-channels in an array format as well as the CMOS challenges of interfacing ion channels will be focused on. Chapter 3 reports a unique solution for the CMOS challenges of interfacing high counting arrays of ion-channels with a focus on noise, area and power consumption. Chapter 4 will focus on a CMOS chip built to test the ideas presented in chapter 3 and provide the reader with detailed explanation of our testing methods and results to support any claims made. Chapter 5 presents contribution and future work.

2. Ion-channels structure and sensing methods

The following section dives into details about physical methods which ion-channels are being implemented and studied. This would entail the methods in which ion-channels are physically utilized in a sensing environment. This is a challenge because ion channels are nano-meter sized proteins that would require a surface or an isolating layer to operate. Later, some of the non-electrochemical methods that use ion-channels will be briefly discussed. Sections 2.2 & 2.3 will discuss electrochemical properties of ion-channels and discuss the possibility of using them in an array format. Section 2.4 will give a brief glimpse into the CMOS challenges of interfacing ion-channels and conduct a literature research on works trying to solve this issue.

2.1. Interfacing ion-channels

2.1.1. Tethering mechanisms for studying ion-channels

Studying ion-channels in a physical format would obviously require the investigator to physically have access to the BLM layer. After all, ion-channels are only viable when operating along an isolating layer which is usually a BLM. Hence, in order to study ion-channel functionality the researchers need to bring the sensing equipment to the living BLM surface. Thus there is a need for proper tethering mechanism for studying ion-channels and other membrane proteins. There are two prominent methods of doing so, patch-clamp and synthetic BLM. The patch-clamp method is shown in Figure 2-1. As indicated, a small heat-polished pipette is pressed against the BLM containing an ion-channel. The glass edges and the cell membrane form an isolating layer with a resistance of the order of 50 MΩ effectively building a “patch” [24]. The seal restricts ion flow across BLM only through the ion-channels located inside the seal. Despite patch-clamp being one of the easiest and most implemented methods for studying BLM since 1970s, there are major

drawbacks to this method such as lack of control over captured protein and lipid composition and being extremely laborious and slow.

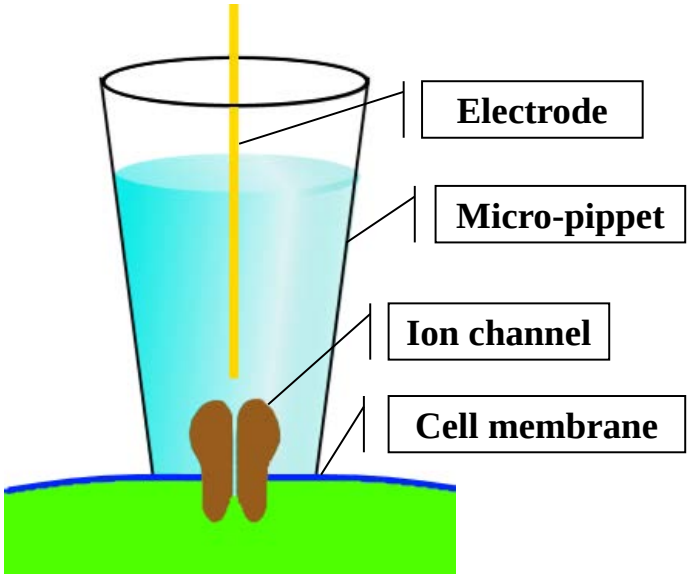

Figure 2-1 Conceptual illustration of patch-clamp ion channel tethering.

As shown in Figure 2-2, an alternative method of tethering ion-channels is forming a synthetic membrane over a nano-sized chamber containing a controlled number target membrane proteins, or in this case only ion-channels[25]. Synthetic BLMs have a simple structure and well-defined electrical characteristics. There are certain drawback to this method as well. Chances of forming a fully sealed and operative BLM with the desired number of ion-channels are currently very low [26].

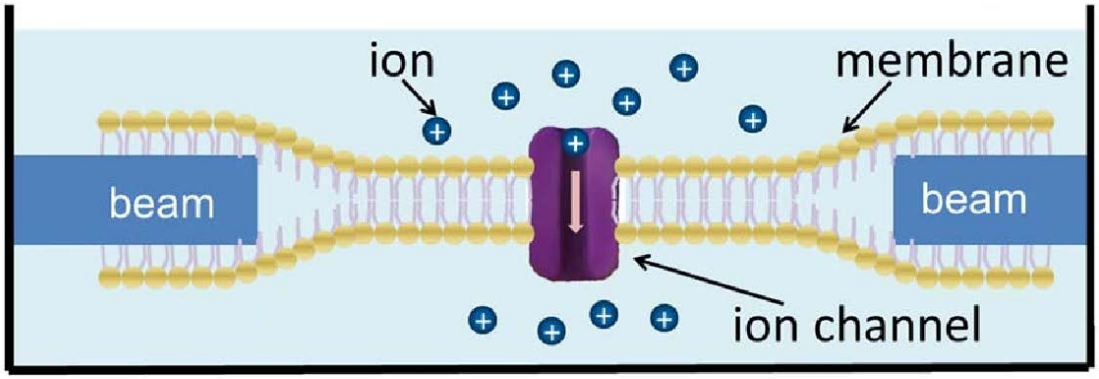

Figure 2-2 Synthetic BLM containing an ion channel formed over artificial beams presented in [26].

2.1.2. Methods for studying ion-channels

There are various ways of integrating biological sensors. It is possible to classify these methods into four categories of electrochemical, optical, mechanical, and magnetic. Since the main duty of ion-channels is transporting ions across membrane and detecting an event when this ion flow is interrupted, electrochemical measurement methods are preferred for interfacing ion-channels. This is due to the fact that electrochemistry revolves around observing and measuring electric charges that may be produced by a chemical reaction or are readily available in the solution delivered to an electrode [27]. Optical methods utilize light based techniques such as Surface plasmon [28] [29], fluorescence and ELSIA [30]. Mechanical methods include using quartz crystals [30] microbalance and resonant cantilever [29]. Magnetic methods use magnetic particles as elements of sensing as discussed in [31]. The discussions in this theses will be conducted over electrochemical sensing.

2.2. Electrochemical modeling and instrumentation of ion-channels

Electrochemical sensing measures changes in current (amperometry and voltammetry), voltage (potentiometry), and impedance resulting from a chemical reaction that either transfers or separates electric charge with reasonable selectivity and sensitivity [27]. Among these methods Amperometric sensors measure a current that is proportional to the concentration of the analytes available. Hence, amperometric method is a perfect solution for characterizing the actions of an ion-channel passing ion active analytes from one isolated chamber to another.

It is entirely possible to estimate the electrical behavior of a conducting ion channel as electrical components even though the component values would vary based on the overall nano-pore working conditions. The electrical model is valuable for understanding the basic behavior of ion channels under a given input voltage. The circuit equivalent of an ion channel implanted on a membrane is shown in Figure 2-3 (left). The parallel capacitance and resistance depicts a low-pass filter-like operation with a time constant of $R_{ch}C_M$, where R_{ch} represents the voltage-current behavior of the channel and C_M represents the capacitance of the exposed cell membrane area. Based on empirical evidence, C_M has a typical capacitance of 1 $\mu F/cm^2$ if the target nano-pore is an ion-channel with a typical BLM structure [32].

A model for the voltage to current relationship of the conducting ion channel shown in Fig. 2.1 under equilibrium conditions is given by Figure 2-3 under equilibrium conditions is given by [32].

$$I_{ion} = g_{ch}(E - E_{ion}) \qquad (2\text{-}1)$$

where I_{pore} is the total ionic current passing through the nano-pore under a given input voltage of E, g_{ion} is the total channel conductance and E_{pore} is the equilibrium potential of the conducting

nano-pore. By definition, if the nano-pore is conducting only a certain type of ion, E_{pore} would be the total voltage gradient created inside the nano-pore due to the presence of ions passing through it, i.e. if the net voltage over the nano-pore is E_{pore} then the flux of ions through the pore will be zero. Notice that (2-1) only represents the equilibrium state of nano-pore operation and does not factor in the time constant RchCM. Furthermore the current-voltage relationship of nano-pores is non-linear. For example, in case of an ion-channel, the relationship is affected by variables such as diffusion currents due to higher concentration of permanent ions on one side of the pore.

The current response of a typical ion channel on a synthetic BLM layer formed on a silicon structure is depicted in Figure 2-3 (top). Depending on the membrane size and type as well as the electrolyte conditions, ion channel event responses may vary in amplitude from ~1 pA to 200 pA with an offset depending on the aperture size and other environmental variables. For ion channels, the incident pulse length can be anywhere between 1 µs to 1 ms [33], and the incidents generally occurs in a pulse-like format that indicates the opening and closing events of the ion channel or particle passing through. The analog interface for ion-channel incidents must have proper performance characteristics to accurately measure such fast changing and small amplitude signals.

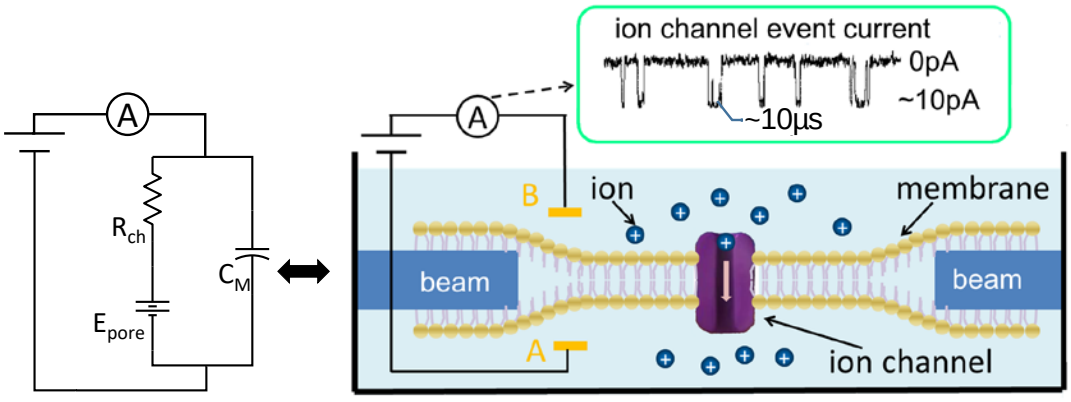

Figure 2-3 Example current response of an ion channel.

2.3. Nano-pore and ion-channel instrumentation and challenges

2.3.1. Amperometric sensing with nano-pores

One of the most prevalent electrochemical detection methods is amperometry. First used in ion chromatography, amperometry is accomplished in the presence of a target analyte by applying a voltage between a working and auxiliary (reference) electrode in a two electrode system or a working and reference electrode in a three electrode system. The response is signified by a current that passes through the working electrode. This current is directly proportional to the mole concentration of the analyte oxidized or reduced on the electrode surface at a given input voltage, as described by Faraday's law [34]:

$$i_t = \frac{dQ}{dt} = nF\frac{dN}{dt} \tag{2-2}$$

where i_t is the current generated at the working electrode surface at the time t, Q is the charge stored at the electrode surface in form of a double layer capacitance, t is time, n is the number of electrons transferred per mole of analyte, N is the number of moles of analyte oxidized or reduced, and F is the Faraday constant (96 485.33 C/mol). In a normal electrochemical reaction, selectivity is achieved through selection of an input voltage that causes oxidation or reduction of different target analytes.

Performing amperometry in nano-pores is slightly different from the normal process in that the input voltage between the working and reference electrodes does not aim to oxidize or reduce analytes. Rather, this voltage is used to facilitate the electrostatic transportation of ions through the nano-pore. For some ion-channels, this voltage may also impact the behavior of the pore, for example the open or closed state of a voltage-gated channel. Regardless, the basic amperometry function is the same: measure a response current at a given working electrode potential. Thus, the working electrode is usually connected to a buffer state that performs two fundamental actions: it

controls the voltage on working electrode through a feedback loop and converts the Faraday response current into an electrically viable signal.

The most widely used amperometric readout circuit is a trans-impedance amplifier (TIA). A TIA consists of a standard operational amplifier with a negative feedback element that regulates the negative input of the operational amplifier without saturating the op-amp output voltage. The most commonly used feedback element is a resistor in parallel with a capacitor for stability. Thus, the output voltage to input current ratio would be equal to (–R). TIAs are widely used as amperometric sensor interfaces due to their simplicity, linearity and input-output voltage isolation [35]. Figure 2-4 depicts a standard TIA structure with a resistive and capacitive feedback interfacing to an equivalent nano-pore circuit model. This model will be used as the basis for noise discussion below.

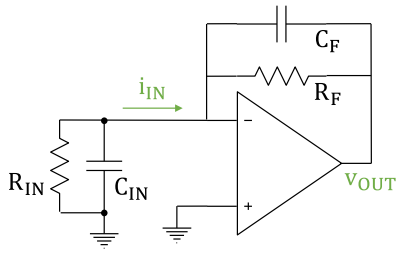

Figure 2-4 A standard TIA structure with a resistive and capacitive feedback interfacing a standard electrical model for an ion channel.

2.3.2. Noise limitations in amperometric interfacing of nano-pores

The amperometric current produced by a nano-pore is small and has a short duration. The bandwidth required for the interface circuit to be able to capture these fast transitioning signals spans from DC to hundreds of kHz. Thus, the interface circuit is susceptible to both low frequency

noise element such as flicker noise as well as high frequency noise elements. Consequently, the interface circuit must demonstrate exemplary noise performance.

The ideal input-output relationship of the resistive and capacitive feedback shown in Figure 2-5 can be expressed as:

$$v_{OUT} = -\frac{R_F}{1+j2\pi f R_F C_F} \times i_{IN} \tag{2-3}$$

where R_f and C_f are the feedback elements, v_{OUT} and i_{IN} are the output and input elements of the TIA and f is the system frequency. The feedback capacitance acts as a low-pass filter, ensuring interface circuit stability in higher frequencies given the presence of an input capacitance C_{IN} [35]. A detailed noise model of Figure 2-4 circuit is shown in Figure 2-5 where C_{IN} represents the sum of the equivalent nano-pore capacitance (C_M from Figure 2-3) and any parasitic capacitance at the input.

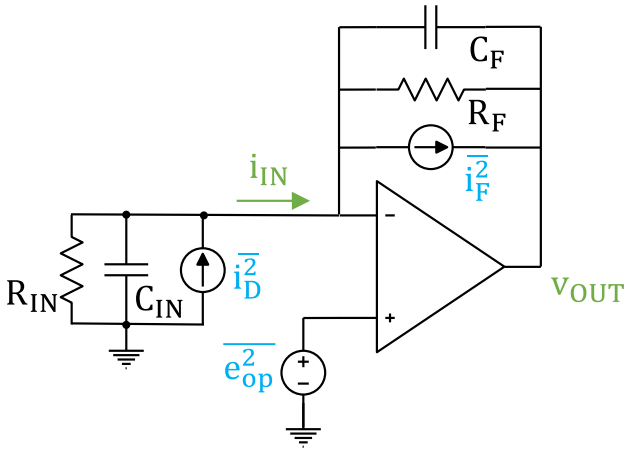

Figure 2-5 A classic TIA amplifier with resistive feedback and all possible noise sources. The terms i_{IN} and v_{OUT} represent the input-referred and output total noise.

The total noise observed at the input, $i_{n\text{-}IN}$, is composed of three main elements:

$$\overline{\iota_{n-IN}^2} = \overline{\iota_D^2} + \overline{\iota_F^2} + \overline{\iota_{op}^2} \tag{2-4}$$

where i_D^2 represents noise created by environmental elements and the sensor itself, $\overline{\iota_F^2}$ represents the noise created by the feedback loop and i_{op}^2 is the input-referred noise created by the op-amp circuitry $\overline{e_{op}^2}$. For resistive feedback, the term $\overline{\iota_F^2}$ can be written as:

$$\overline{\iota_F^2} = \frac{4kT}{R_F} \tag{2-5}$$

where k is the Boltzmann constant and T is temperature in Kelvin. If $\overline{v_{op-out}^2}$ the total output voltage noise created by $\overline{e_{op}^2}$, it can be inferred that:

$$\overline{v_{n-out}^2} = \overline{e_{op}^2} \times \left|1 + \frac{Z_F}{Z_{IN}}\right| = \overline{e_{op}^2} \times \frac{(R_{IN}+R_F)^2+4\pi^2 f^2 R_F^2 R_{IN}^2 (C_F+C_{IN})^2}{R_{IN}^2(1+4\pi^2 f^2 R_F^2 R_{IN}^2)} \tag{2-6}$$

where Z_F and Z_{IN} represent the total feedback and input impedance seen on the feedback loop and input node, respectively. (2-6) can be simplified to:

$$\overline{v_{n-out}^2} = \overline{e_{op}^2} \times \frac{(1+{}^{R_F}/_{R_{IN}})^2+4\pi^2 f^2 R_F^2 (C_F+C_{IN})^2}{1+4\pi^2 f^2 R_F^2 R_{IN}^2} \tag{2-7}$$

where the term with R_F/R_{IN} dictates the interface circuit noise performance at lower frequencies. Hence, a high input resistance is very beneficial to the interface circuit at lower frequencies. For nano-pore interfaces, R_{IN} can generally be assumed to be much greater than R_F, which permits the input-referred current noise generated by the op-amp to be expressed as:

$$\overline{\iota_{op}^2} = \frac{\overline{v_{op-out}^2}}{|Z_F|^2} = \overline{e_{op}^2} \times \left[\frac{1}{R_F^2} + (2\pi f)^2 (C_F + C_{IN})^2\right] \tag{2-8}$$

Thus, the total input referred noise at input I_{IN} is:

$$\overline{\iota_{n-IN}^2} = \overline{\iota_D^2} + \frac{4kT}{R_F} + \overline{e_{op}^2} \times \left[\frac{1}{R_F^2} + (2\pi f)^2 (C_F + C_{IN})^2\right] \tag{2-9}$$

The noise spectrum seen at the output of a typical TIA system interfacing with a nano-pore is depicted in Figure 2.6 [36]. The flicker noise and dielectric loss are produced by the input capacitance. The dielectric loss noise is due to thermal dissipation in lossy dielectric materials [36]

which has a direct correlation with frequency. The white noise and the capacitive noise are, however, caused by $\overline{e_{op}^2}$. The interface circuit bandwidth should be on the order of hundreds of kHz, which means that the capacitive noise created by the terms containing f^2 will definitely hinder the sensitivity of the interface circuit and is a common concern in the nano-pore interface circuit literature [37].

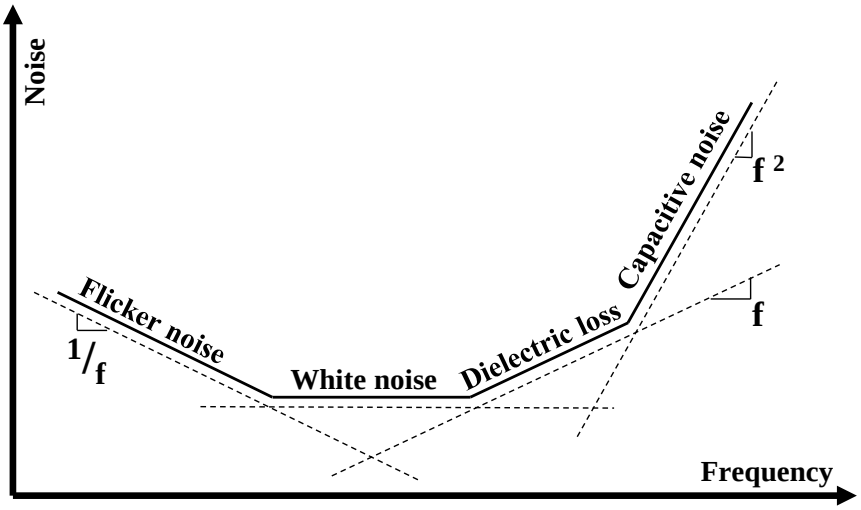

Figure 2-6 Noise spectrum and the contributing elements obseved with nano-pore interface circuits adapted from [36].

Based on (2-9), the two best ways to solve the capacitive noise issue using a TIA are to decrease $\overline{e_{op}^2}$ or to decrease the overall capacitance seen at the TIA input. The term $\overline{e_{op}^2}$ can be improved by dedicating more circuit area and/or power to the TIA or using novel op-amp techniques. Decreasing the capacitance can usually be achieved by system miniaturization. Generally, miniaturization of sensor area and electrode dimensions is desirable because it reduces the parasitic capacitances as well as the double layer capacitance formed on the electrode [37].

Furthermore, reducing sensor dimensions decreases the impact of electrolyte resistance on amperometric instrument noise performance [27].

2.3.3. Other limitations for amperometric sensing

Noise performance is one of the main challenges to interfacing nano-pores, but other major issues must also be addressed. One of the main issues is input offset currents. As mentioned before, nano-pores monitor ionic current flow and variations in current due to the presence of target molecules. The background ionic current can have constant or variable amplitude and can be as much as 10× the amplitude of sensing event currents. This background current creates and input offset that can challenge coherent sensing of the nano-pore event. Most modern amperometric interface circuits utilize a TIA with capacitive feedback due to its simplicity, low use of hardware resources, and good noise performance [37]. However, a large input offset can saturate a basic TIA interface circuit. For example, a large input offset will force a switched-capacitor interface circuit to dramatically increase its clock rate, compromising the SNR performance of the system.

2.4. Multichannel nano-pore arrays

Due to recent advances in microfabrication and biological science techniques, a trend has developed to use microarrays for parallel sensing [38][39]. These structures accelerate the development time by quickly extracting valuable experimental data. Similarly, combining nano-pores with microfluidic delivery systems offers great potential for enabling parallel recording of biological signals. Integrated arrays are especially suitable for ion-channels formed on a BLM structure due to their self-assembling nature that enables them to automatically form in designated spots within a microfluidic system [40]. Parallel array implementation is also appealing to overcome the inherently low yield in forming functional nano-pore interfaces, especially ion-channels. The patch-clamp extraction method for ion channels is very laborious and time

consuming with low odds of extracting the correct target ion channels. Even using synthetic BLMs, the chances of successfully forming an interface with the desired number of functional ion-channels is very low [41]. Hence, a logical use for self-forming ion channel nano-pores would be in the form of an array where a large number of nano-pore are implemented simultaneously, increasing the odds of successful formation of ion-channels.

Electrically interfacing with arrays of nano-pore introduces a new set of design challenges that need to be addressed. The works presented in [42] and [43] demonstrate parallel recording functionality with very limited number of array channels and sub kHz bandwidth. These systems are not able to detect single molecule events due to the plethora of parasitic capacitances and lack of noise fine-tuning. These challenges could be overcome by integrating the sensing circuitry within a microfluidic system containing the nano-pores through an approach dubbed lab-on-CMOS [19]. Implementing array sensing by integrating CMOS interface circuitry in close proximity of a nano-pore array system [44] can greatly reduce environmental and wiring noise. However, this high level of integration sets severe limitations in terms of the power and area consumed by the CMOS nano-pore interface circuitry. These limitations are thoroughly discussed in [44] and [26] which seek to implement arrays of hundreds of ion-channel in a microfluidic system implemented on the surface of a CMOS interface chip. In both these works, each nano-pore is assigned to a pixel amplifier stage that is in very close physical proximity to mitigate the effects of excessive input capacitance. As a results, the pixel amplifiers have very strict limitations in terms of the area they consume. Furthermore, because this approach enables hundreds of pixel amplifier stages right beneath (microns away from) the ion channel sensors, the potential for the CMOS circuitry to heat or even thermally denature the nano-pores must be considered. As a result, strict power consumption limitations must be met by the CMOS pixel circuitry.

2.5. CMOS instrumentation for ion-channel sensing

The idea of implementing ion-channels in a self-assembled array format for parallel sensing of multiple well-formed channels over very small pixels has been discussed so far. Despite the enormous potential impact of such approach, there is no report of implementation of such idea throughout the literature. This can be attributed to the physical challenges in interfacing such an array of ion-channels. The primary issue is the fact that the ion-channel amperometric signal is fast and has a low amplitude in a very noisy environment which is a departure from norms of traditional electrochemistry. Based on our calculations the signal we are expecting to receive from an ion-channel event is a pulse shaped signal with an amplitude of about 10 pA and a pulse-width of 10 µS. This would not be hard to address as is shown later in the literature review section. However, the signal shape issue is corroborated by the fact that addressing this level of noise would require a lot of resources which is not desirable in an array format implementation. Consequently, the purpose of this work is to address the practical implementation of the suggested array of ion-channels from a CMOS standpoint addressing the noise limits of the interface in a resource limited environment.

Although the development of interface circuits for both solid-state and ion-channel nano-pores is a relatively new field of study [37], several prominent works have already been reported in the literature with a focus on three main issues: offset cancelation, noise performance and array implementation. Based on (2 9) there are only a few options for improving noise performance in a classic TIA structure. However, many approaches have been reported to improve noise by stepping away from the classic TIA structure. To begin analyzing these, let’s express (2 9) in a simplified and more generalized form as:

$$\overline{\iota_{IN}^2} = \overline{\iota_D^2} + \overline{\iota_F^2} + \overline{e_{op}^2} \times \left[\frac{1}{R_F^2} + (2\pi f)^2 (C_{IN})^2\right] \quad (2\text{-}10)$$

Based on (2-10), the methods for improving nano-pore interfacing noise can be classified as:

- Improving $\overline{\iota_F^2}$ and increasing R_F^2 by enhancing feedback constructs such as capacitive feedback, enhanced feedback and active feedback amplifiers
- Decreasing total input-referred noise of the op-am ($\overline{e_{op}^2}$)
- Decreasing total input capacitance, C_{IN}, and $\overline{\iota_D^2}$ by using a Lab-on-CMOS approach

The capacitive feedback approach forgoes the feedback resistor to avoid resistive feedback noise, effectively making the value of RF approach infinity at DC. Assuming that R_{IN} also has a large value, capacitive feedback would decrease the noise floor significantly and save the circuit area of a large feedback resistor. Note that the feedback capacitance should be significantly lower than the total input capacitance to avoid introducing another noise performance factor. The area saved by eliminating the feedback resistor can be utilized for noise reduction on the CMOS circuitry. However, implementing capacitive feedback will leave the interface vulnerable to input DC offset signals that could saturate the op-amp if left unchecked [37]. One solution to this issue is to incorporate an input current DC offset canceling mechanism as shown in Figure 2-7 [45]. This is an integrator structure with periodic reset switching to stop the integrator from saturating, followed by a gain stage and a low-pass filter. The circuit was designed for measuring DNA strands passing through a silicon-based nano-pore implemented in a 0.5µm bulk CMOS technology. While this circuit displays exemplary performance for its intended purpose, the periodic reset limits its bandwidth to a maximum of 10 kHz, which is not ideal for nano-pores with faster transition times. This integrating structure consumes 1.5 mW of power and 0.1386 mm^2 for each channel.

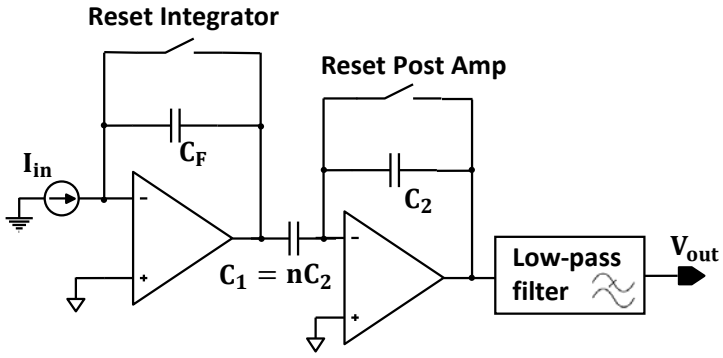

Figure 2-7 Capacitive interfacing of amperometric current using reseting switches adapted

A popular method for enhancing the basic TIA noise performance is to use a feedback with a relatively small resistance coupled with an active current attenuator as shown in Fig. 2.6.

2.6. High throughput array implementation, opportunities and challenges

Due to recent advancements in microfabrication techniques and biological sciences, using microarrays for parallel sensing is developing into a new trend [38][39]. These structures accelerate the development time and extracted valuable data in various scientific instrumentations. Nano-pores in conjugation with microfluidic delivery systems demonstrate great potential for enabling parallel recording of biological signals. This is especially the case for ion-channels formed on a BLM structure due to their self-assembling nature that enables them to automatically form in designated spots in a microfluidic system [25]. A Flip side of this case is the fact the chances of successfully forming a BLM with appropriate number of functional ion channels is very low [46]. Alternative methods suffer from the same fate as well. A patch-clamp extraction method for ion channels would be very laborious and time consuming without having better odds of extracting the correct target ion channels. Hence, a logical use for self-forming ion channel

Nano-pores would be in form of an array where a large number of Nano-pore are implemented simultaneously, increasing the odds of successful formation of ion-channels.

Interfacing with Nano-pore arrays brings about a new set of design challenges that need to be addressed. The works presented in [42] and [43] both demonstrate parallel recording functionality with very limited number of arrays and sub kHz bandwidth. Thus they are not able to detect single molecule events. This is due to the fact that the sensing circuitry is not integrated within the microfluidic system containing the Nano-pres. Consequently, the results are obscured due to the plethora of parasitic capacitances and lack of noise fine-tuning. There exists a push to bring about a lab-on-CMOS approach to array sensing by integrating CMOS readout circuitry in close proximity of a Nano-pore array system [44]. Doing so would produce limitations in terms of the power and area consumed by the Nano-pore interface circuitry.

A prime example of these limitations is evident in the work presented in [44] and [26]. These papers seek to implement arrays of hundreds of Ion-channel in a microfluidic system implemented on the chip surface. Each Nano-pore has a pixel amplifier stage in close proximity to mitigate the effects of excessive input capacitance. As a results, the pixel amplifiers have very strict limitations in terms of the area they consume. Furthermore, since there are hundreds of pixel amplifier stages right beneath the ion channels, there is the possibility of the CMOS circuitry heating up the pores and thus destroying hem in the process. As a result, strict power consumption limitations are to be implemented for the CMOS buffer circuitry.

A solution to this issue is presented in [44] and [26] in form of a shared op-amp structure. This concept was first presented in a body of work for bio-sensing presented in [47] where multiple OP-amps working in a TIA configuration with a set positive terminal input. The solution is to share the positive segment and only use half of the op-amp body for each TIA structure. As a result, the

saved power and area resources act as a resource that can be allocated to enhancing noise performance or ensuring system feasibility.

2.7. Conclusion

All in all, there is much being done in the field of bio-electrochemistry. This is true especially in the field of nano-pore and ion-channel interfacing for DNA detection, protein characterization, etc. Even though most work in this field present novel ideas and approaches to solve numerous issues, none are compatible with the vision that is introduced for a lab-on-CMOS mass ion-channel arrays. Most of the work presented usually focus on single target detection and have no concern for circuit area or power consumption. Next chapter will attend this and try to solve the noise, power and area issues that stem from mass implementation of ion-channels on the lab-on-CMOS platform.

3. A CMOS current amplifier for high throughput ion-channel arrays

So far, the nature of ion-channels located in synthetic BLMs and their electrical characteristics have been discussed so far in this thesis. It is evident that a new CMOS topology is needed for a full system implementation of arrays of synthetic BLMs. The works conducted in the field so far have all been concentrating on a single nano-pore structures. Hence, this chapter will focus on defining the challenges of implementing arrays of ion-channels and propose solutions for a successful Implementation.

3.1. An array solution for ion-channel sensing

Despite the recent advancements in proteomics and tethering mechanisms there are still major issue that need to be addressed. Even though the patch-clamp method is a scientific community favorite since 1970s, the process is laborious. The patch-clam user does not have any control over what membrane proteins are clamped from the cell. Hence, performing a successful test would be a laborious experience with long waiting and testing times. Although still in experimental phase, synthetic membrane formation suffers from similar issues. The odds of forming an effective membrane layer are extremely low. Hence performing a characterization test on a synthetic BLM regarding their membrane proteins and lipid composition may take a tens of hours [48]. However, synthetic BLM formation has a certain advantage over patch-clamp methods. It is entirely possible to form these synthetic BLMs in an array format in presence of microfluidic channels and electrodes. Hence, the idea of implementing and characterizing synthetic BLMs in arrays presents itself [26].

Due to their nature, implementing and tethering synthetic BLMs would require a self-assembling technique with a microfluidic approach. One of the earlier approaches in doing so,

involves flowing lipid solutions across an aperture containing a BLM chamber with a 500 µm hole through a glass slide in a microfluidic structure [49]. More recent techniques try to eliminate the use of heavy non-volatile solvents by passing an aqueous solution with a thin layer of phospholipid stock solution at the gas-lipid interface on both sides of the chamber. Doing so would merge the phospholipid monolayers, forming a BLM across the aperture. The formed devices have microfluidic channels on one or both sides of the substrate containing the aperture [50][51].

A design using these principals is depicted in Figure 3 1. It is composed of multiple independent microfluidic channels each containing hundreds of chambers that are called pixels. Each pixel houses a single synthetic BLM, an isolated electrolyte solution and WE electrode. There is a shared RE electrode in each microfluidic channel that acts as a common analog ground potential. The analog chip beneath the microfluidic channels interfaces each pixel and senses any ion movement through the ion channels existing on pixel synthetic BLM layer using the WE electrode. The analog chip is implemented using AMI C5N 0.5 µm technology. This system is designed to be high throughput with the goal of housing ~100 synthetic BLM pixels on a single chip. This brings about one of the biggest issues for the feasibility of this project. Aside implementation of the synthetic BLMs and the microfluidic channel, placing ~100 pixels on a 2.5mm × 2.5mm chip would bring about a serious CMOS design challenge. Later sections would try to shine light on some of these issues.

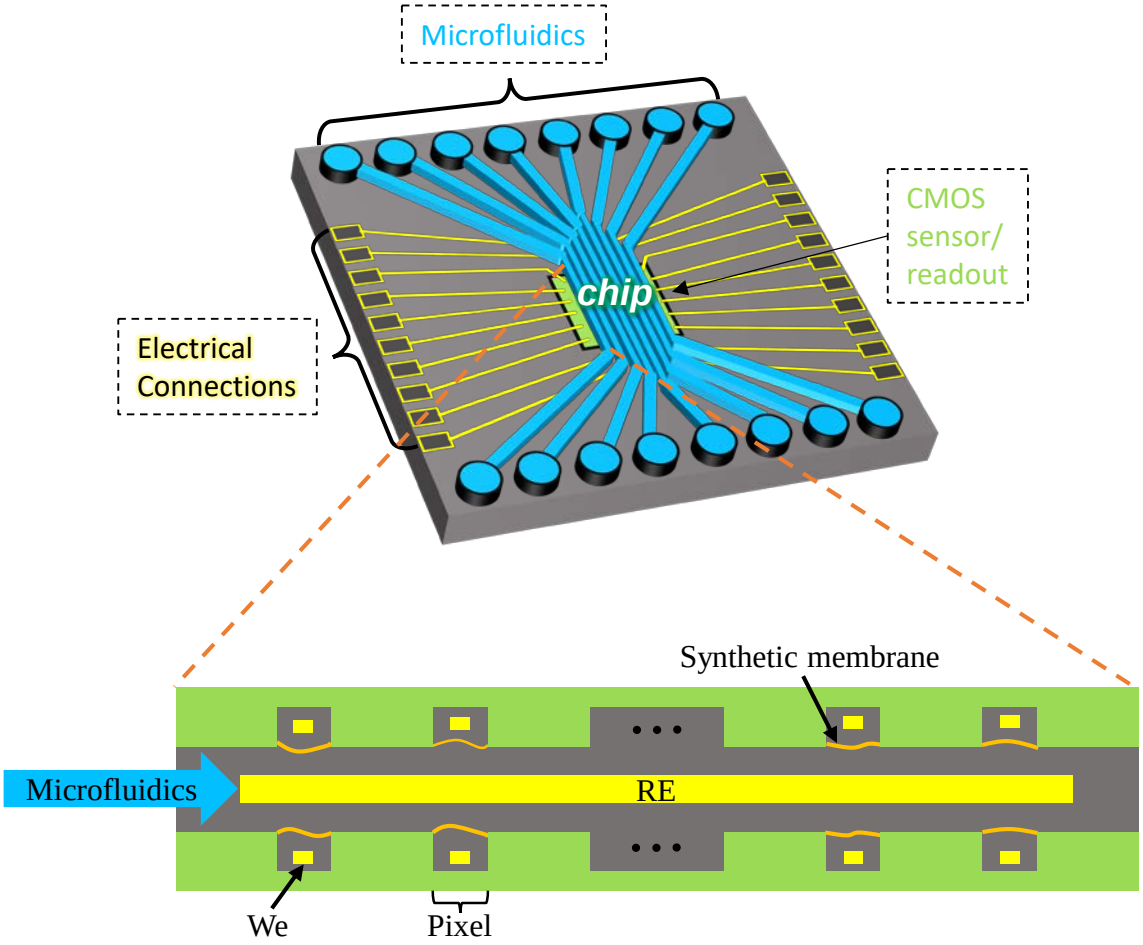

Figure 3-1 An array of BLMs implemented over pixels adjacent to a microfluidic chamber built on a CMOS chip for direct readout of the ion channel incidents with minimal noise.

3.2. Noise limitations for interfacing ion-channels

The signal that is generated through membrane protein is in pA levels and has a very short duration [52]. The bandwidth required of the circuit for it to be able to capture the fast transitioning signals spans from DC to hundreds of kHz. What this means is that the system is susceptible to low frequency noise such as flicker as well as high frequency noise elements. Consequently, it is expected of the system to demonstrate exemplary performance in terms of noise. One of the benchmark instruments for current sensing in electrophysiology is Axon Axopatch 200B. It has an

r.m.s. noise floor of 25fA at 1 kHz frequency (0.7fA/√Hz until 1 kHz) [53]. However, the presented instrument is bulky, expensive and used under specific laborious conditions. The ideal input-output relationship of a resistive and capacitive feedback as shown in Figure 2-6 TIA can be formulated as:

$$v_{OUT} = -\frac{R_F}{1+j2\pi f R_F C_F} \times v_{IN} \tag{3-1}$$

where R_F and C_F are the TIA feedback elements. The capacitance acts as a low-pass filter, ensuring system stability in higher frequencies given the presence of an input capacitance C_{IN}

Given the noise spectrum dependency on input capacitance, implementing the idea of an array of synthetic BLMs poses a new challenges. Interfacing hundreds and thousands of electrodes over the chip surface would not be possible without producing excessive parasitic input capacitances for the amperometric readout circuit endangering system feasibility. Our lab has proposed a solution in [40] in which a very small CMOS circuit is place beneath the synthetic membrane as shown in Figure 3-4. Each chamber containing a WE electrode and a synthetic membrane is called a pixel. As shown in Figure 3-2, each pixel is encapsulate by a WE electrode and a planar BLM containing an ion-channel. The global RE electrode maintains the microfluidic potential, providing the system with electrolytes that can travel through the ion-channel. The target microfluidics are passes through the channel and interact with the membranes and their ion-channels. Placing the CMOS buffer right beneath the corresponding pixel has two significant advantage. It minimizes the interface and wiring capacitance, reducing the noise requirement on the first stage buffer by a large margin. Moreover, due to the fact that the synthetic BLM has a fairly predictable capacitance, it would be easier to match the CMOS interface with the noise requirements for interfacing the pixel. The implemented CMOS pixel interface also amplifies the low input current enough so that

it would be connected to less noise sensitive components like multiplexers and gain-focused amplifiers. This makes multiplexing thousands of pixels into a few clear outputs possible.

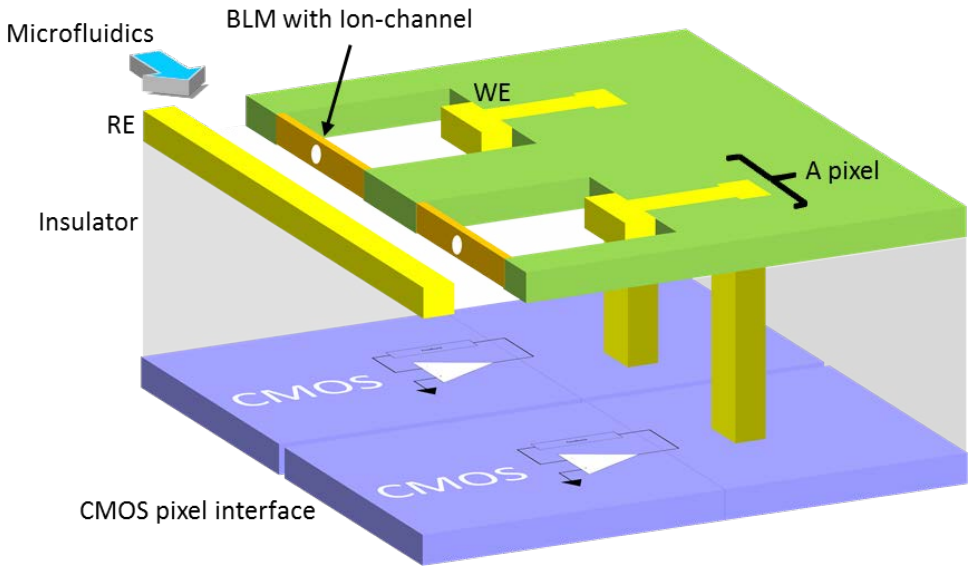

Figure 3-2 3D view of the proposed pixels for the proposed lab-on-CMOS concept.

3.3. Area and power limitations for interfacing a high throughput ion-channel arrays

So far, it has been suggested to put a CMOS interface circuit under each pixel to mitigate the effects of unwanted noisy capacitances. However, doing so is not an easy task mainly due to the fact that placing the interface right beneath the pixel would impose area, power and noise restrictions on the circuit. These issues are not going to hinder the feasibility of the proposed concept however, they will cause major circuit challenges. Hence, design limits and trade-offs are needed to be considered before designing the CMOS circuitry. Unfortunately, challenges arising from a lab-on-CMOS approach are a very niche field in the area of membrane characterization or nano-pore studies. As a result, not a lot of literature has been focused on solving the challenge introduced in Chapter 2.4.

A big limitation in terms of CMOS realization of the system proposed in Figure 3-2 is the maximum area dedicated to each pixel amplifiers. The CMOS will be implemented in AMI 0.5 µm technology with dimensions bigger than 25mm^2. Since currently we are planning to put a 1000 of pixels in this chip area, approximately 0.025 mm^2 of space would be dedicated to each pixel which is enough for the physical pixel area. As depicted in Figure 3-2 the maximum area dedicated to each pixel amplifier is not going to be greater than the corresponding pixel. Hence, not considering the complementary circuit blocks such as bias and MUX, the approximate area dedicated to each pixel amplifier is estimated to be 0.025 mm^2. It is worth noting that this area limitation is imposed on AMI 0.5µm technology. There are only three metal layer available in the said technology with limited use on metal 3 layer due to the possibility of it causing difficulties implementing the microfluidic channels.

Limitations on power consumption are another factor than need to be considered moving forward with the design. As indicated before, each pixel is equipped with an interface circuit placed right beneath it. This is due to the fact the interface circuit has the potential to act as a heater for the pixel. Too much power consumption on each circuit would mean that the pixel will be locally heated. High temperature has a chance to damage the synthetic BLM at the gate of the pixel. As pointed out in [54] a heat flux of 80 mW/mm^2 has the chance to damage the BLM tissue. Hence, for a hypothetical area of 0.025 mm^2 for a pixel that is surrounded by 5 other ones as shown in Figure 3-3, the maximum allowable power consumption by each pixel can be deduced as:

$$P_{max} = 80\frac{mW}{mm^2} \times 0.025mm^2 \div 5 = 400\mu W \quad (3\text{-}2)$$

Hence the each pixel interface has a maximum allowable power consumption of 400 µW. Having such low maximum power consumption and area would result in stringent limitations on circuit design aspects.

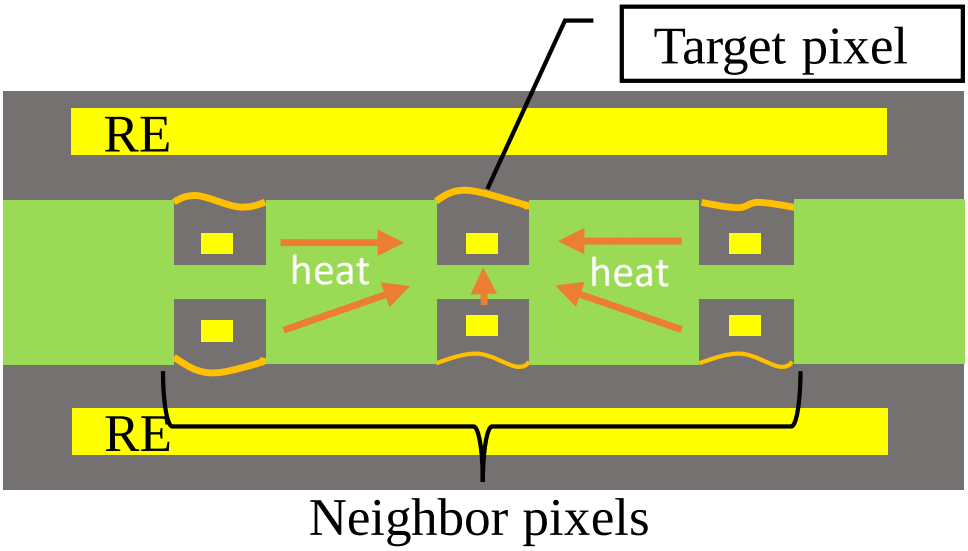

Figure 3-3 Local heating of pixels due to power consumed in the target pixel and it's adjacent pixels.

3.4. A CMOS current amplifier design

So far it has been established that we wish to implement synthetic BLMs containing a particular number of ion-channels in an array format. The fact that the signal current indicating ion-channel action is very short and fast has been discussed. Since a typical ion-channel event would be a 10 pA pulse spanning 10 µs, system noise performance becomes critical because noise is directly correlated with input capacitance, as established in Figure 3-2, it was decided to place the interface circuit right beneath the chamber. As a result, the power and area performance of the

system are added to the challenges that need to be answered. This section will proposed a solution to the said issues.

3.4.1. Fundamental noise limitations of an op-amp

There are four main contributors to overall system noise which consist of flicker noise created by the pore, flicker and white noise created by electrical components, dielectric noise created by the input capacitance and the capacitive noise, which is most potent in higher frequencies. The dielectric and the capacitive noise are mitigated adopting the proposed lab-on-CMOS structure, reducing the stray capacitances as much as possible. However, the noise stemming from the circuitry still remains to be addressed, especially since this noise is intermingled with capacitive noise according to (3.7). In order to understand the basics of circuit noise, it is always good to study the noise elements in a basic amplifier, one as such depicted in Figure 3-4 with all the possible noise sources. The total input referred noise of the amplifier from Figure 3-4 can be expressed as shown below [55]:

$$\overline{v_{eqT}^2} = \overline{v_{eq1}^2} + \overline{v_{eq2}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)\left(\overline{v_{eq3}^2} + \overline{v_{eq4}^2}\right) \tag{3-3}$$

where $\overline{v_{eq}^2}$ represents the overall input referred noise of each transistor shown as a voltage source at their gate and the term g_m is the transconductance of the corresponding transistor. The presented formula assumes that transconductances on matching pairs are similar. It is clear that in order to negate the effects of transistors M3 and M4, their transconductances should be significantly lower than that of M1 and M2. The transistor input referred noise can be presented as:

$$\overline{v_{eq}^2} = 4kT\left(\frac{2}{3g_m}\right)\Delta f \tag{3-4}$$

where k is the Boltzmann constant, T is the temperature and Δf represents bandwidth.

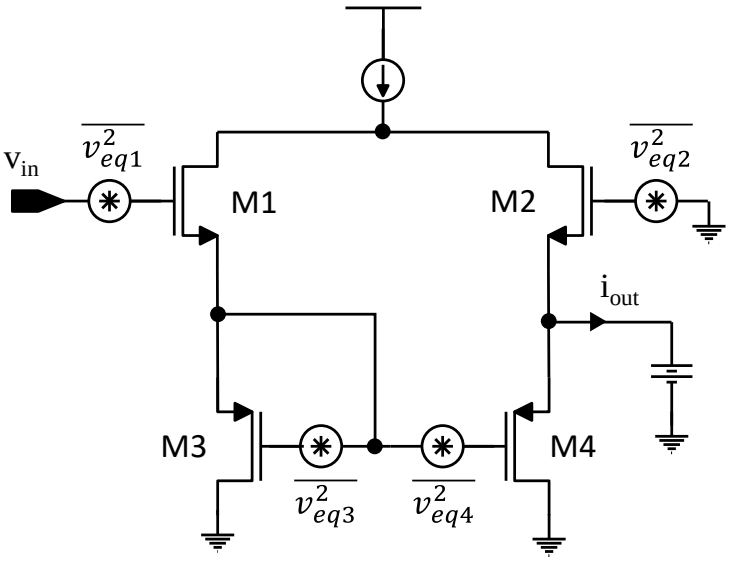

Figure 3-4 Noise sources influencing a typical amplifier circuit.

It is clear that the only way to decrease the thermal noise is to increase g_m as much as possible. The term g_m can be represented as:

$$g_m = \sqrt{2\mu C_{ox} {}^{W}/_{L} I_D} \tag{3-5}$$

where μ is the corresponding charge carrier mobility, C_{ox} is the MOSFET gate oxide capacitance, W and L are the width and length of the transistor, and I_D is the bias current of the transistor. Hence to increase the g_m of M1 and M2, the width and the bias currents are to be increased as much as possible. Doing so would decrease the input equivalent thermal noise. The electrical flicker noise is another issue that needs to be addressed. The input referred thermal noise of each transistor at their gate can be presented as:

$$\overline{v_{1/f}^2} = \frac{K_f \Delta f}{C_{ox} W L f} \tag{3-6}$$

where k_f is the flicker noise coefficient. Placing (3.11) in (3.8) the following equation is extracted.

$$\overline{v_{eq-1/f}^2} = \frac{2K_p}{fW_1L_1C_{ox}}\left(\frac{k_n\mu_nL_1^2}{k_p\mu_pL_3^2}\right)\Delta f \quad (3\text{-}7)$$

where K_p and K_n are the flicker noise coefficients for PMOS and NMOS transistors respectively. It is clear that in order to achieve better flicker noise performance, the input transistor needs to be larger and have shorter length compared with subsequent transistors. All in all, it is easy to infer that increasing input transistor area, and current are key to improving noise performance of the amplifier. However, it was stated in previous sections that there is a limit to power and area due to the lab-on-CMOS implementation. Hence, a prominent circuit feature trade-off emerges from this argument. It is desirable to increase the pixel interface circuit area and power consumption as much as possible without crossing the limits placed by the restrains in place due to the lab-on-CMOS approach. It is worth noting that increasing the size of input transistors would also increase the input capacitance of the pixel, meaning that capacitive noise would be made worse.

All in all, there are major trade-offs that need to be addressed moving forward with the pixel interface design. There are certain limitations as to what are the maximum allowable CMOS area and power consumption. However, in order to clearly analyze the pixel currents, noise performance of the circuit needs to be optimized which in return is in conflict with power and area restrains.

3.4.2. An op-amp sharing technique to address the area and power limitations of interfacing high throughput ion channel arrays

A requirement for this project would be to have op-amps working in parallel to interface the pixels as depicted in Figure 3-5 Pixel interfaces for nano-pore current sensing with (a) typical TIA structure and (b) shared TIA structure.Figure 3-5 (a). It is clearly observable that all these op-amp have the same voltage on their positive inputs. This voltage is the analog ground voltage that

is shared globally throughout the whole CMOS chip, keeping WE at the analog ground. The stimulation is done through the RE electrode for clusters of pixels. Now if we are to hypothetically assume that the positive segment of the op-amp could be shared with a local cluster of negative input halves, as shown in Figure 3-5 (b), the power and area consumption of each individual segment would drop by half. There are multitude of benefits arising from such configuration. It would make it possible for all the extra resources to be dedicated to enhancing noise performance or the feasibility of design dimensions. The proposed shared op-amp circuit is depicted in Figure 3-6.

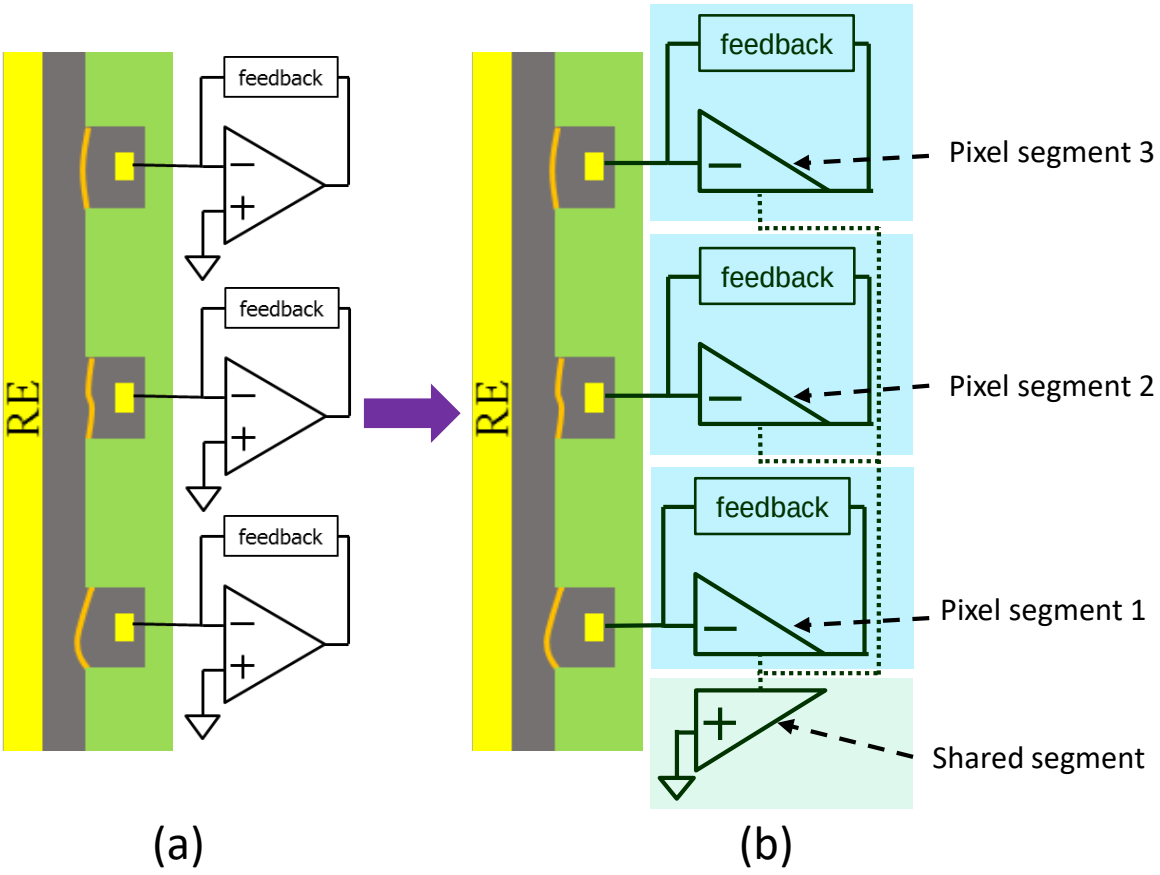

Figure 3-5 Pixel interfaces for nano-pore current sensing with (a) typical TIA structure and (b) shared TIA structure.

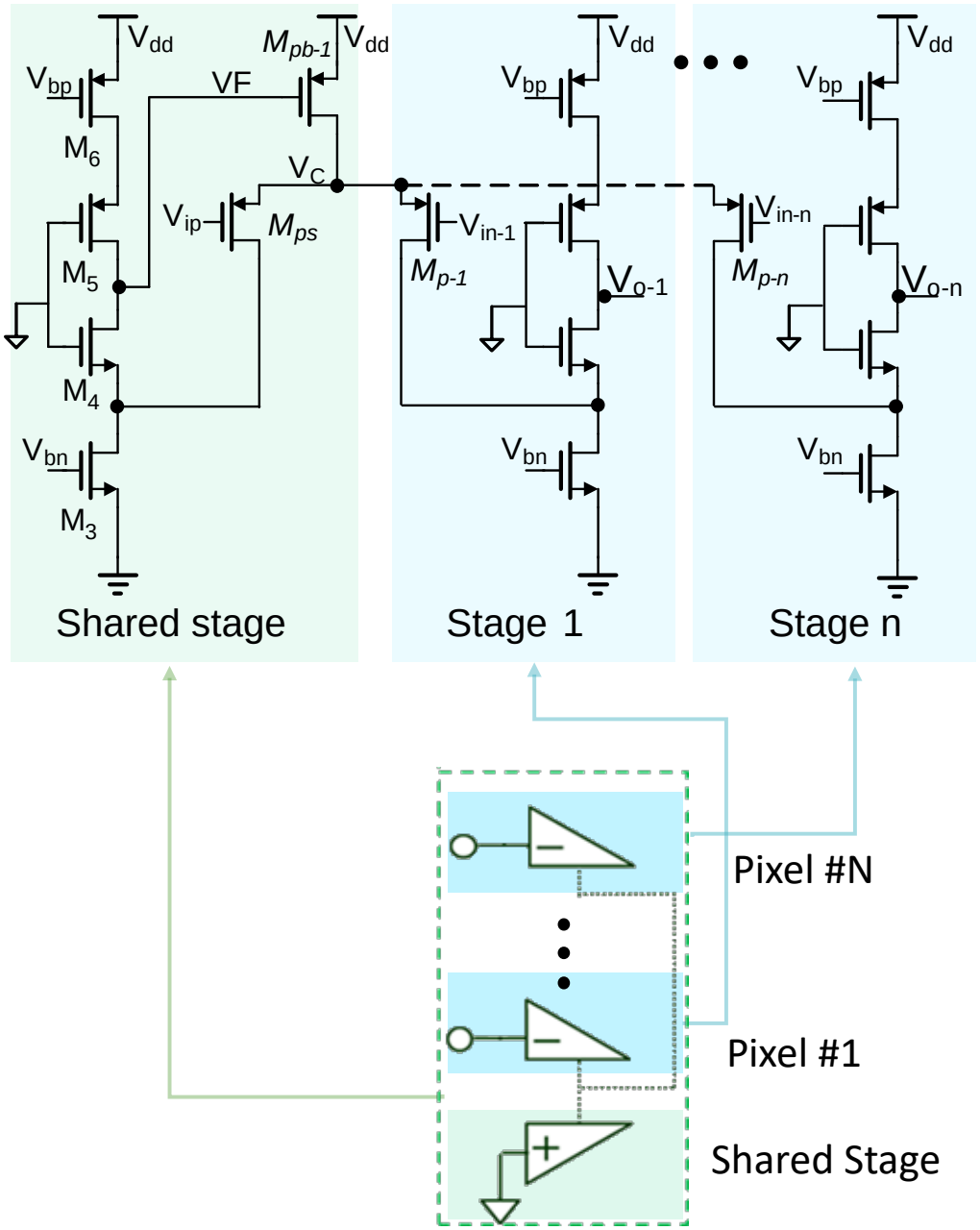

Figure 3-6 Shared op-amp structure circuitry and the corresponding op-amp elements.

The shared stage shown in Figure 3-6 is essentially the positive segment of the n shared stages. It provides them with a voltage, V_C, which helps maintain the semi-differential status of the system. The voltage at V_C is constant as shown below:

$$V_C = V_{th-Mps} + \sqrt{I_b / \mu C_{ox} W/L} \tag{3-8}$$

where $V_{th\text{-}Mps}$ is threshold voltage of transistor M_{ps}, I_b is the bias current going through M_{ps} and $\mu C_{ox} W/L$ are the characteristics of M_{ps}.

An in depth look at the shared stage indicates that it has an internal feedback loop. The loop is shown in more details in Figure 3-7. The current source I_S can be considered to be the input of this loop while the output node is chosen to be V_C. Hence, the transistors M_{ps}, M_3 and M_4 are considered to be the feedback components. As a result the feedback type can be considered a parallel output, parallel input with $\beta = g_c$. As a result, the open loop feedback can is as follows:

$$A_O = \frac{V_C}{I_S} = g_c R_{s-ps} R_{in} \tag{3-9}$$

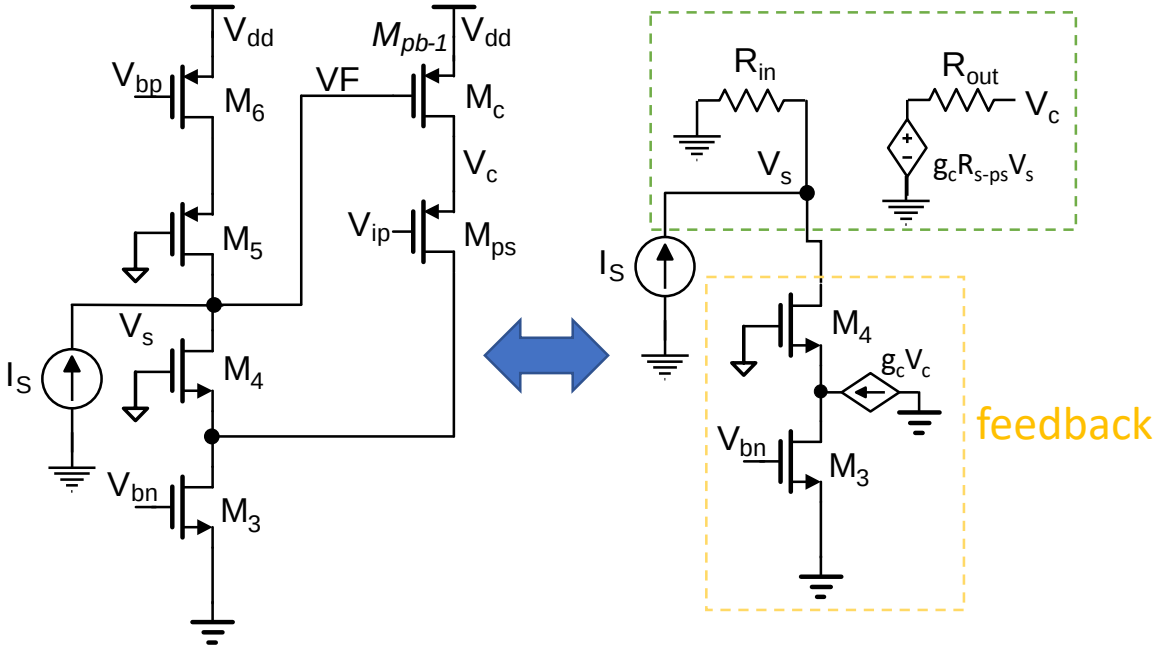

Figure 3-7 Equivalent circuit structure for the internal feedback loop placed within shared segment of proposed op-amp.

where R_{in} is the resistance seen on the drain of M_5 which is a great number because M_5 and M_6 are in parallel. $R_{s\text{-}ps}$ is the total resistance seen at the node V_c which is equal to the source resistance of M_{ps} and g_c is the trans-conductance of M_c. As a result, the feedback overall gain is:

$$A_F = \frac{V_C}{I_S} = \frac{g_c R_{in}}{1+g_c R_{in}} R_{s-ps} \tag{3-10}$$

Furthermore, the output resistance seen at node V_c is:

$$R_{OUT-F} = \frac{R_{s-ps}}{1+g_c R_{in}} \tag{3-11}$$

Which means that the resistance seen at node Rs is extremely small due to the fact that both g_c and R_{in} are a big trans-conductance and resistance. Thus the voltage V_C is held constantly by feedback loop present at the shared stage. This is because V_C is a node with a very low resistance connected to a voltage source. Hence, the resistance in the node V_C is so small that every shared stage can act as fully differential stage without affecting the other op-amp stages.

As a result, each shared stage sees a very small resistance at the source of their input transistors and operate as a single op-amp with their positive input fixed to a certain voltage. If a pixel amplifier has a feedback as shown on Figure 3-8, if $M_{p\text{-}1}$ and M_{ps} are matched, it would try to equate $I_{b\text{-}ps}$ and $I_{b\text{-}p1}$ since $I_{b\text{-}bp}$ and $I_{b\text{-}bn}$ are similar. As a result, the loop will try to make $V_{in\text{-}1}$ be equal to V_{ip}.

If a current input signal i_{in} is injected to stage n among N stages is called i_{mn} then it is easy to infer that:

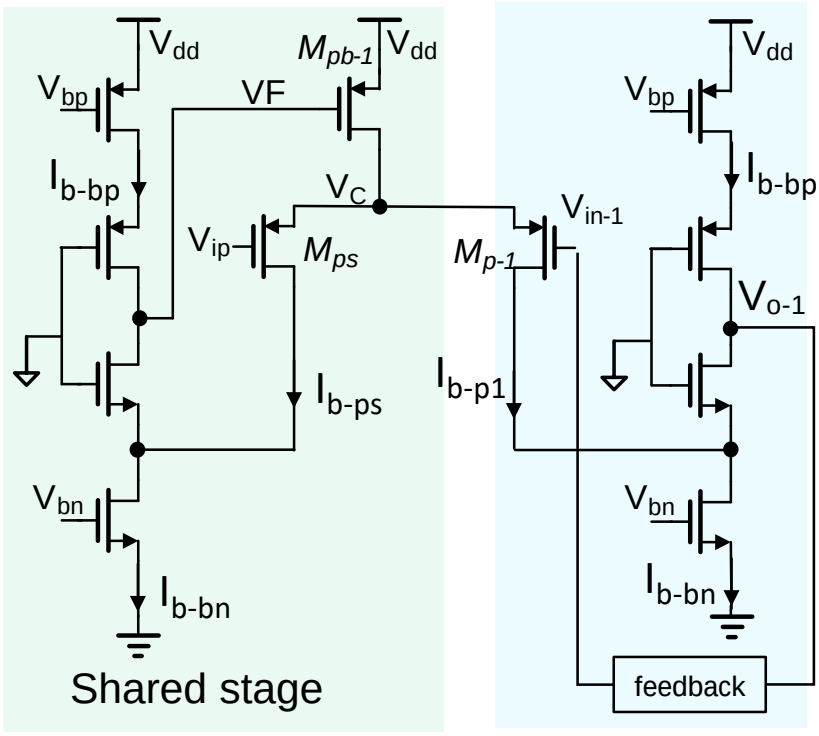

Figure 3-8 Proposed shared op-amp with only one gain stage and a negative feedback loop.

$$\frac{i_{mn}}{i_{in}} = \frac{1}{1+N+g_c R_{in}} \tag{3-12}$$

which is due to the fact that i_{in} is shared among N stages and a very low feedback output resistance which takes a huge chunk of the current. As a result, the total noise injected by another shared stages to a sample stage, n is as follows:

$$\frac{\overline{\iota_{mn}{}^2}}{\overline{\iota_{noise}{}^2}} = \frac{1}{(1+N+g_c R_{in})^2} \tag{3-13}$$

Where i_{noise} is produced by another shared stage. As a result it is possible to infer that it is possible to infer that N-1 other shared stages have the following effect on stage n:

$$\frac{\overline{\iota_{mn}{}^2}}{\overline{\iota_{noise}{}^2}} = \frac{N-1}{(1+N+g_cR_{in})^2} \tag{3-14}$$

which is completely negligible. As for the shared stage, based on Figure 3-9 which is a simplified version of the shared op-amp structure, the noise injected into stage n from shared stage can be calculated as:

$$\frac{\overline{\iota_{mn}{}^2}}{\overline{\iota_{noise-shared}{}^2}} = \left(\overline{\iota_3{}^2} + \overline{\iota_6{}^2} + \overline{\iota_{ps}{}^2}\right)\frac{(g_cR_{in})^2}{(1+N+g_cR_{in})^2} + \left(\overline{\iota_{pb-1}{}^2}\right)\frac{1}{(1+N+g_cR_{in})^2} \tag{3-15}$$

however since the term g_cR_{in} is very big, it is possible to infer that the effects the shared stage has on any other stage, namely n is as shown below:

$$\frac{\overline{\iota_{mn}{}^2}}{\overline{\iota_{noise-shared}{}^2}} = \overline{\iota_3{}^2} + \overline{\iota_6{}^2} + \overline{\iota_{ps}{}^2} \tag{3-16}$$

which indicates that the shared stage has a similar effect on the shared stage to that of a normal folded cascade.

As a result, the proposed shared circuit reduces the power and area required for implementing an interface op-amp with slightly better noise performance when compared with a typical similar telescopic cascade structure.

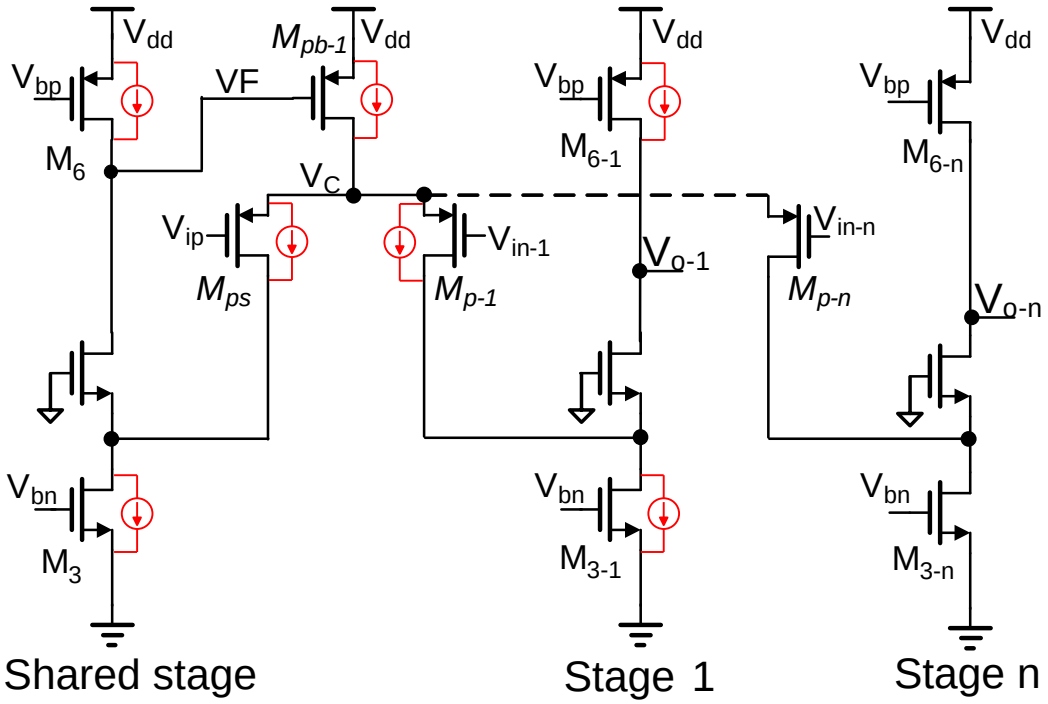

Figure 3-9 Noise and interface sources of the proposed share op-amp structure.

3.4.3. A low-noise compact feedback Structure

As indicated in previous sections the main focus of the pixel amplifier stage is to improve its power, area noise performance as was evident with the choice of adopting shared op-amp structure. Based on the discussions in 2.4.1, , the best option would be to go for a fully active amplifier structure introduced in [56]. The feedback structure would work as a current buffer structure with relatively low gain. However, this would not cause much problems for the implementation since the pixel amplifier stage is not meant to demonstrate such characteristic.

Let's imagine that the feedback loop is as shown in Figure 3-10. If the input current I_{in} is zero, then all feedback transistors M_{p1}, M_{n1}, M_{p2} and M_{n2} are operating in sub threshold region since their gate-source voltage (overdrive voltage) is normally zero [57]. Hence they are not contributing to system noise. It is worth noting that the input current is always considered to be

zero since there is no ionic current flowing through membrane while the ion-channel is closed. However, despite the fact that the feedback transistors are operating in sub-threshold region the input voltage on the WE node is always equal to the analog ground since the current that the feedback loop is required to provide is very small and does not affect the feedback transistors extensively. Now if there was an input current I_{in} present, depending on the polarity of the input current, the voltage V_{o1} would vary the overdrive voltage of feedback transistors M_{p1} and M_{n1} so that they would produce a current equal to I_{in}. As a result, the transistors would uphold their duty as feedback components, keeping the positive and negative inputs of op-amp equal. The relationship between the op-amp output voltage V_{o1} and the input current can be expressed as:

$$V_{od} = \mp nV_T \ln\left(\frac{I_{in}}{I_{D0}}\right) \tag{3-17}$$

where V_T is the thermal voltage, V_{od} is the overdrive voltage, I_{D0} is the drain current at $V_{od} = 0$, and n is:

$$n = 1 + {}^{C_D}/_{C_{OX}} \tag{3-18}$$

where C_D is the capacitance of the depletion layer and C_{OX} is the capacitance of the oxide layer. The transistors M_{n2} and M_{p2} are exactly Z times bigger than M_{n1} and M_{p1} in terms of transistor width. However, the overdrive voltage, V_{od}, they see is the same as M_{p1} and M_{n1}. As a result the I_{D0} and subsequently I_D on transistors M_{n2} and M_{p2} is Z times bigger than input current I_{in}. Since the drain-source voltage on all the transistors is the same, it is safe to assume that the gain of this circuit is exactly Z. As a result, the proposed structure acts as a current buffer with a gain of Z. It should be noted that the transistors only operate well in lower frequency ranges [56]. Hence, the capacitances C_1 and C_2 are incorporated to maintain the gain Z at higher frequency ranges.

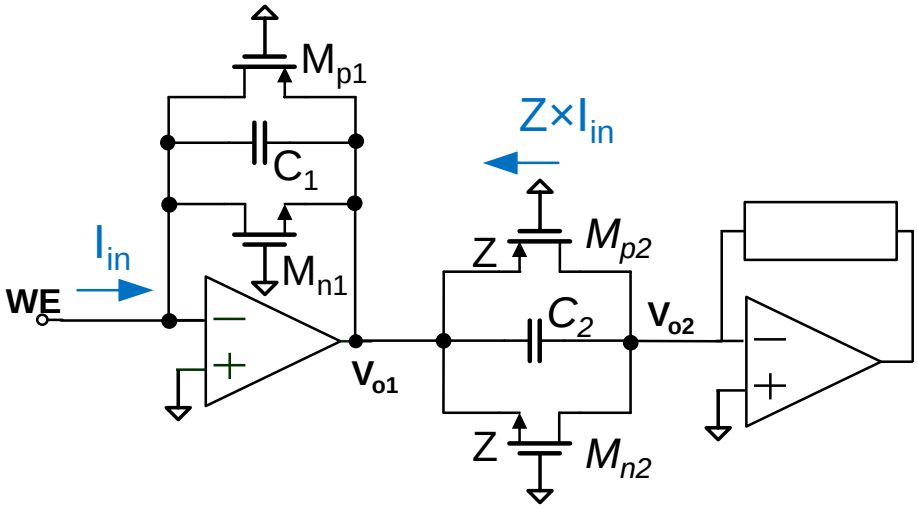

Figure 3-10 The implemented active feedback network for nano pore current interfacing.

An inherent benefit of the proposed structure is the fact that the op-amp output voltage has a logarithmic relationship with input current as indicated in $V_{od} = \mp nV_T \ln(\frac{I_{in}}{I_{D0}})$ (3-24). As a result, the circuit is able to interface a wide range of input currents. It is worth noting that it is preferred for the feedback transistors to stay in sub-threshold region through the entirety of the input current range. However it is not possible to uphold this at very high input currents. Ideally, it is preferred to make the input transistors very long so that they would be able to interface larger currents without turning on. As for extremely large input currents, the system performance at such great input currents is not critical. Hence, the transistors are allowed to turn on.

As mentioned earlier, there are major benefits in adopting the active transistor only feedback architecture introduced in 2.4. These benefits include saving power and area due to the fact that the contrary to the literature, the active feedback structure does not require any passive components, supporting circuitry or active power consumption. Moreover, this architecture

displays exemplary noise performance due to the fact that the feedback transistors are operating in sub-threshold region.

Despite all the discussed benefits, there are issues that need to be mentioned. The biggest issues may be classified as gain certainty and output data format. Due to the fact that transistors M_{p2} and M_{n2} are Z times bigger than M_{p1} and M_{n1}, it is very challenging to match the said transistors perfectly especially if the transistor sizes are close to the technology minimum. As a result, it is very difficult to obtain a consistent gain Z over a multitude of stages. This is corroborated by the fact that the positive and negative gains demonstrated by the pMOS and nMOS transistors may differ. The reason is that pMOS transistors only handle the negative input currents while the nMOS transistors only interface the positive input currents and it is very hard to completely match pMOS and nMOS area ratios individually. This issue can be solved by making the feedback transistors bigger, sacrificing power. As a result, there is a trade-off between pixel amplifier area and gain accuracy. Fortunately, the gain required of the first stage is only about 20 dB. As a result, it would be much easier to match transistor ratios correctly with such low gain limits. Another issue that arises from this implementation is the fact that depending on feedback transistor operation region the op-amp output voltage V_{o1} is correlated to input current logarithmically or linearly and thus, is not usable for data acquisition. Other stages are needed to turn the output current into a coherent readable signal. These stages and the topology required to run them are discussed in the next section.

3.5. A shared amplifier topology for optimum area usage

So far the principals of the circuit being implemented have been established. This section will be concentrating on the topology that our team came up trying to implement this architecture. Let’s imagine that our desired gain is 100. If the topology suggested in Figure 3-11(a) is used, the

total area consumed by the feedback transistors would be $101\times M_{p1}$. In C5N technology the minimum legal transistor width and length 1.5 µm and 600 nm respectively. However, the minimum size is opted for 6 µm of width and 1.2 µm of length due to the fact that the system gain is dependent on the ratio of these transistors and we would prefer avoid any possible mismatch due to minimum sizing. The fact that such big transistors exist in every pixel amplifier would rob the design of its area budget. One way to mitigate this issue is using multiple gain stages in cascade as shown in Figure 3-11(b). Assuming M_{p1} and M_{p3} have the same sizes, the total area consumed by gain transistors is reduced to $22\times M_{p1}$.

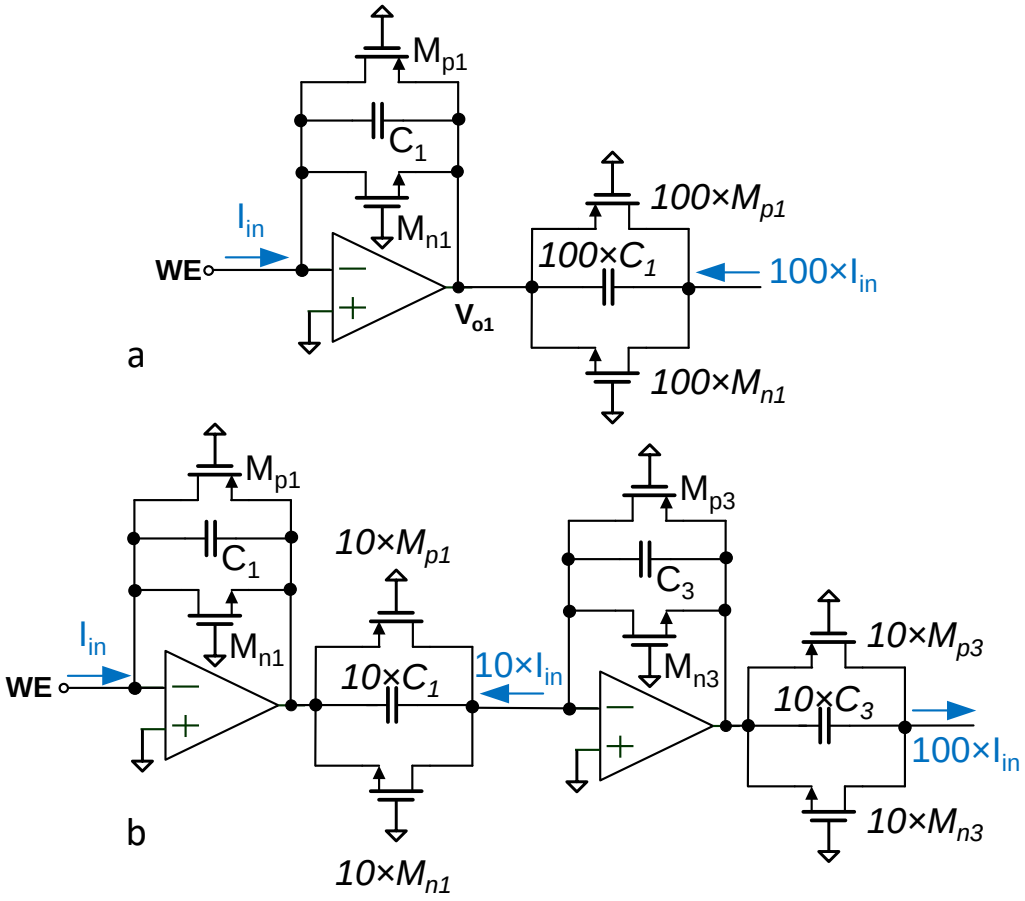

Figure 3-11 The difference between having a single stage with a gain of 100 and having two stages with two stages with a gain of 10 resulting in a total gain of 100.

Upon further investigation, the only truly essential part of the circuit depicted in Figure 3-11(b) is the first stage. This is due to the fact that this stage is responsible for isolating the input capacitance caused by the membrane capacitance, keeping the noise levels low. Hence, the second stage can be further shared to optimize the system area. A suitable topology to implement these changes is shown in Figure 3-12. The topology is divided into independent clusters which contain M stages of N pixel interfaces. Each stage of N pixel interfaces are multiplexed. The resulting M signals are fed to a gain stage that multiplexes this signals to an off-chip signal processing unit. Implementing the system with this topology opens the way for putting great numbers of pixel amplifiers in a single chip. The total number of pixel amplifiers implemented with this method is M×N×K. If each of these parameters is 8, the total pixel amplifiers covered would be 512 which is more than enough for an initial implementation.

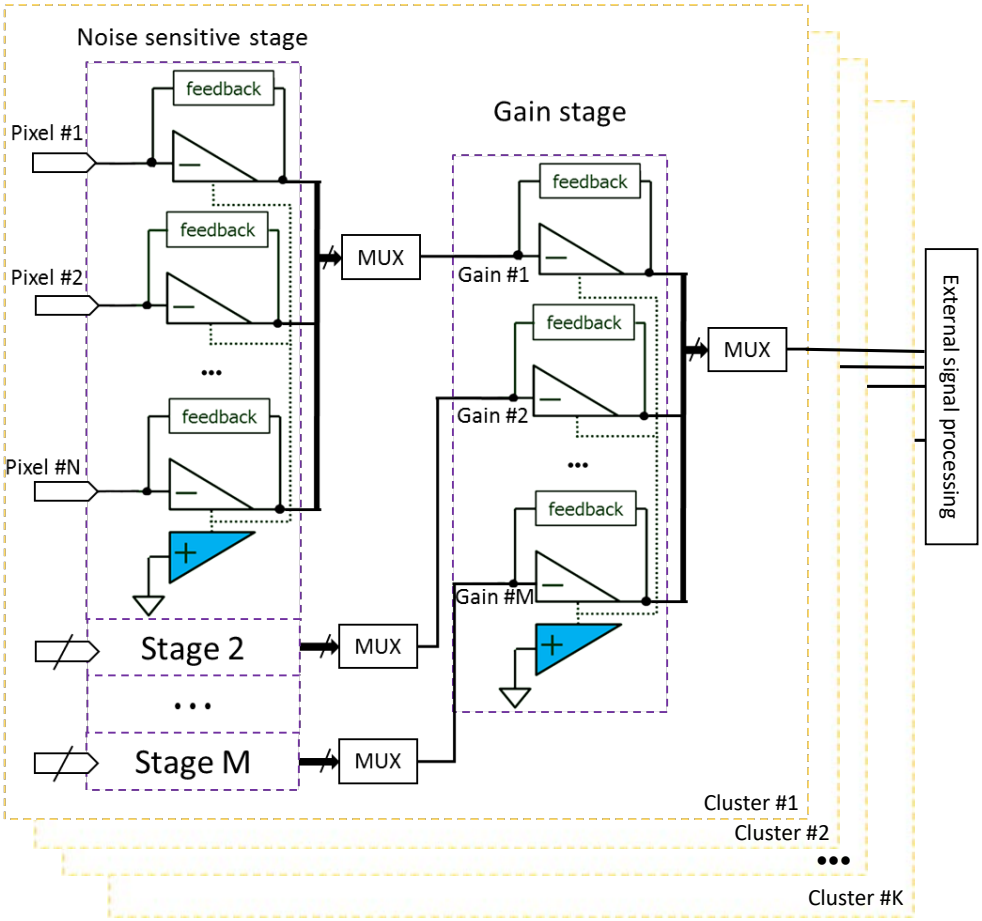

Figure 3-12 The topology in which pixel amplifiers would be implemented to interface a large number of pixels.

All in all, the presented op-amp structure and topology seem to be suitable for interfacing an array of ion-channels. However, before any practical efforts are made implementing a lab-on-CMOS approach implementing this system, the functionality of the proposed CMOS solution needs to be tested in a real-world test environment. As a result, a chip for evaluate and verification of the proposed CMOS approach is fabricated in standard ON C5N technology and tested. Chapter 4 will cover this topic extensively.

4. Evaluation of current amplifier performance

So far it's been established that with the use of nano-pores such as ion-channels, the issue of single molecule detection reduces to a simple instrumentation issue. A solution is discussed with a shared op-amp structure and a subthreshold transistor-only feedback structure. To prove that this architecture would perform adequately under an array of ion-channels, the architecture needs to be tested in a real world environment. Thus, a test chip was fabricated in AMI 0.5 µm C5N CMOS technology incorporating some variations of the proposed architecture which will be discussed in this chapter.

4.1. CMOS test chip contents and functionalities

Various functionalities of the proposed design need to be tested. This include the viability of the share op-amp as a basic block, the possibility of sharing these op-amps, the functionality of the transistor-only feedback and system's ability to tolerate a membrane input capacitive noise while interfacing ionic current. To this end, as shown in Figure 4-1, a test chip containing various blocks has been fabricated and tested in AMI 0.5 µm C5N CMOS technology. The main test target in the chip would be the shared block with the gain of 1000 and a capacitive input. This block is composed of 4 shared stages followed by a gain stage as is used to confirm that all the aspects of the proposed circuit work well together. The capacitive input is only for isolation of input from any external capacitance and will be discussed in detail later. Other segments include a shared stage without capacitive input, single op-amp interface stages as well as bias circuit and a test op-amp. Figure 4-2 sheds more light about the placement of stages in a shared structure. The shared op-amp is places in the middle of four gain stages to minimize op-amp mismatch and offset between the stages. The resulting signals are passed through a very small MUX stage that connects the output to an additional gain stage resulting in a grand total gain of 1000. Segments 3 and 4

have an input capacitance of 5 pF which is an estimated value for a BLM cell with an ion-channel over a 5 um wide channel [40].

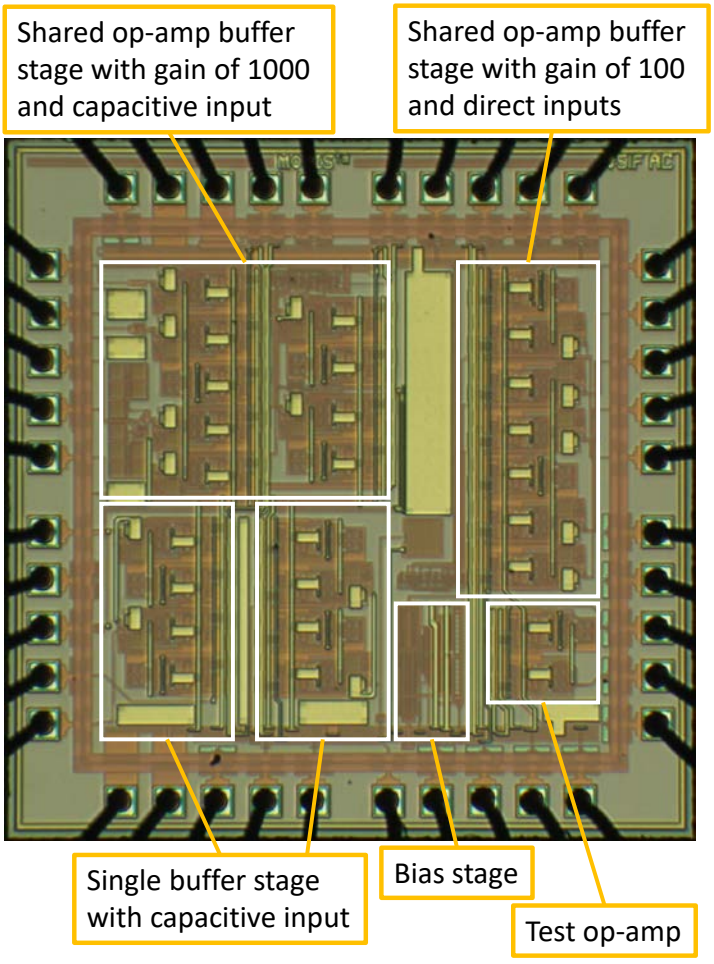

Figure 4-1 The fabricated test chip with all the various blocks implemented.

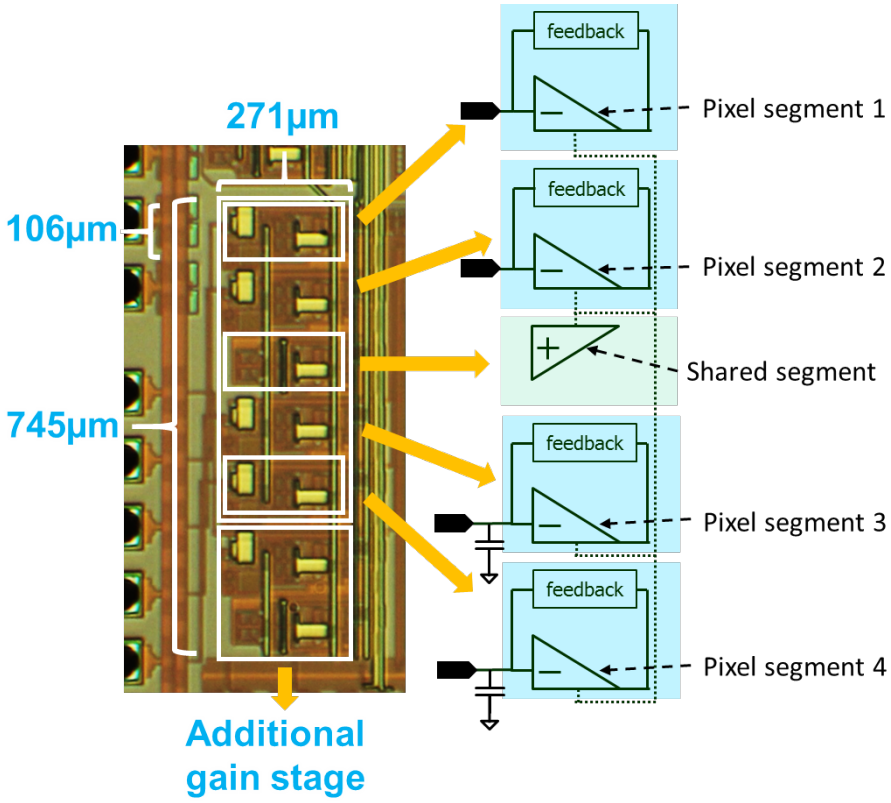

Figure 4-2 The shared op-amp stages and how they are placed within the test chip.

4.2. A testing platform for the extremely sensitive instrumentation circuit

The implemented circuit is designed to be able to read amperometric input currents under a maximum input load capacitances of 5 pF which is the estimation of a BLM layer's capacitance over a 5 µm wide chamber gate. As a result, any input capacitance over this limit would limit the functionality of the circuit. Thus, this makes connecting any test probes directly to the input gate impossible. The reason is that connecting any current source probes would create an excessive amount of parasitic capacitances that would impair the functionality of the amperometric current reader. This would make any direct test impossible. The solution embedded on the chip is as shown in Figure 4-3. The input to the current buffer is isolated from the input port by a very small

capacitance C_{iso} (100 fF). As a result, any external capacitance connected to the input port would be in series with C_{iso} and will be automatically ignored. The input membrane capacitance is modeled with the capacitance C_{mem}. This capacitive input method has been implemented for all input channels mentioned in Figure 4-1 except for the ones dubbed direct input.

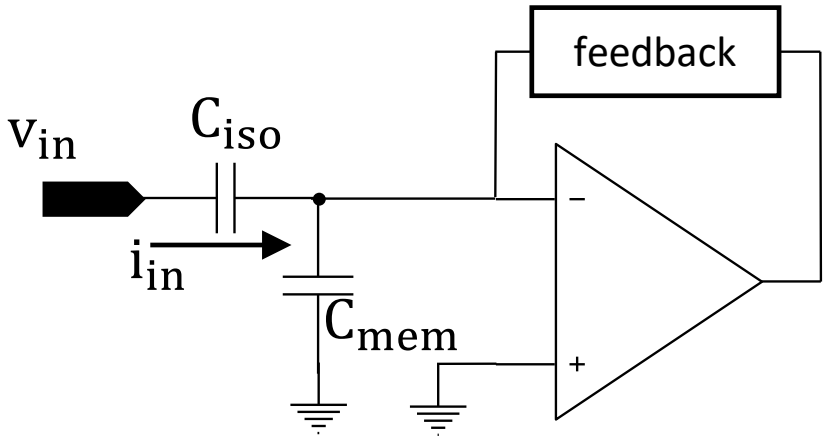

Figure 4-3 The test configuration for input parasitic noise compensation.

The input current is generated from input voltage V_{in} as shown below:

$$i_{in} = C_{iso} \frac{\Delta V_{in}}{\Delta t} \tag{4-1}$$

Where ΔV_{in} is the amplitude of input pulse signals and Δt is the pulse rising/falling time. With Δt of 10 μsec and a pulse amplitude of 1 mV over, a 100 fF capacitance, it is possible to generate a clean current input pulse of 10pA. If a sin input is being used, the current will be shaped as shown below:

$$i_{in} = A_{sin} C_{iso} 2\pi f \cos(2\pi f t) \tag{4-2}$$

Where A_{sin} is the input sinusoidal signal amplitude and f represents frequency. As a result, it is clear that the input capacitance and signal capacitance play a major role in determining input current amplitude. As a result, two different C_{iso} capacitances were utilized, a 10 fF and a 100 fF.

Their input operation range for generating a steady 100 pA input sinusoidal current is as shown below:

Table 1 the input sinusoidal range for various isolation capacitances

Frequency	**100 fF**	**10 fF**
100 Hz	A_{sin}= 1.591 V	A_{sin}= 15.91 V
1 kHz	A_{sin}= 159.1 mV	A_{sin}= 1.591 V
10 kHz	A_{sin}= 15.91 mV	A_{sin}= 159.1 mV
100 kHz	A_{sin}= 1.591 mV	A_{sin}= 15.91 mV

Based on Table 1, the amplitudes 1.591 mV and 15.91 V are impossible to implement. This is due to it being very difficult to produce a clean 1.591 mV input sinusoidal current and 15.91 V being way above the tolerable voltages that AMI 0.5 µm C5N CMOS technology allows. A combination of both these input capacitances needs to be implemented. Hence, pixel segment 1 and 3 are equipped with a 10 fF metallic capacitance while 2 and 4 have a 100 fF poly capacitance.

4.3. Test results

The first step in testing the implemented chip would be to evaluate overall chip functionality and measure the response of the implemented buffer under various DC input currents. To do so, the input to one of the direct input current buffers, i.e. the ones not isolated from input through an isolating capacitance, is used. The test setup is as depicted in Figure 4-4.

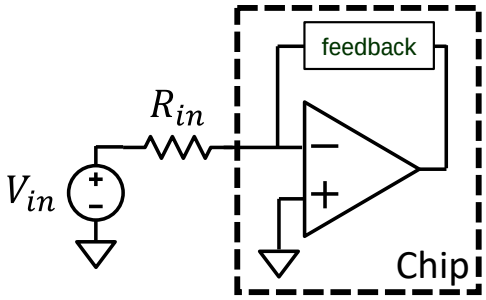

Figure 4-4 Test setup for input DC response test.

R_{in} is a 1 GΩ resistor with an accuracy of less than 1%. The input voltage deviates from the analog ground in multiples of 10 mV steps. As a results, the variation is in increments of 10 pA. The system response to the input resistance is very noisy due to the parasitic capacitance present due to the probe connection and the structure of the resistance. The direct mode current buffer has a gain of 100. Hence, the output current is passed through a The results are passed through a low-pass filter and averaged over 1024 cycles using an Agilent Technologies DSO-X 2012A oscilloscope device. The results are shown in Figure 4-5. The response is linear whether the input stimuli is positive or negative, however, there is a difference between the slopes of the responses under positive and negative imputs as shown in Figure 4-6. This is due to the fact that based on the feedback structure introduced in Figure 3-11, the positive input currents are handled through a set of NMOS transistors while the negative inputs are handled but the input PMOS pair. Hence the two slopes do not necessarily have to match. The reason for the variations in the slopes could be attributed to the differences in threshold voltages and systematic mismatches between similar MOS transistors. It should be noted that the function that this circuit is designed to perform is merely detecting input pulses. Hence, the linearity matching between positive and negative inputs is of no consequence for the scope of this project. The results shown indicate that the system is functional and ready for high-frequency testing.

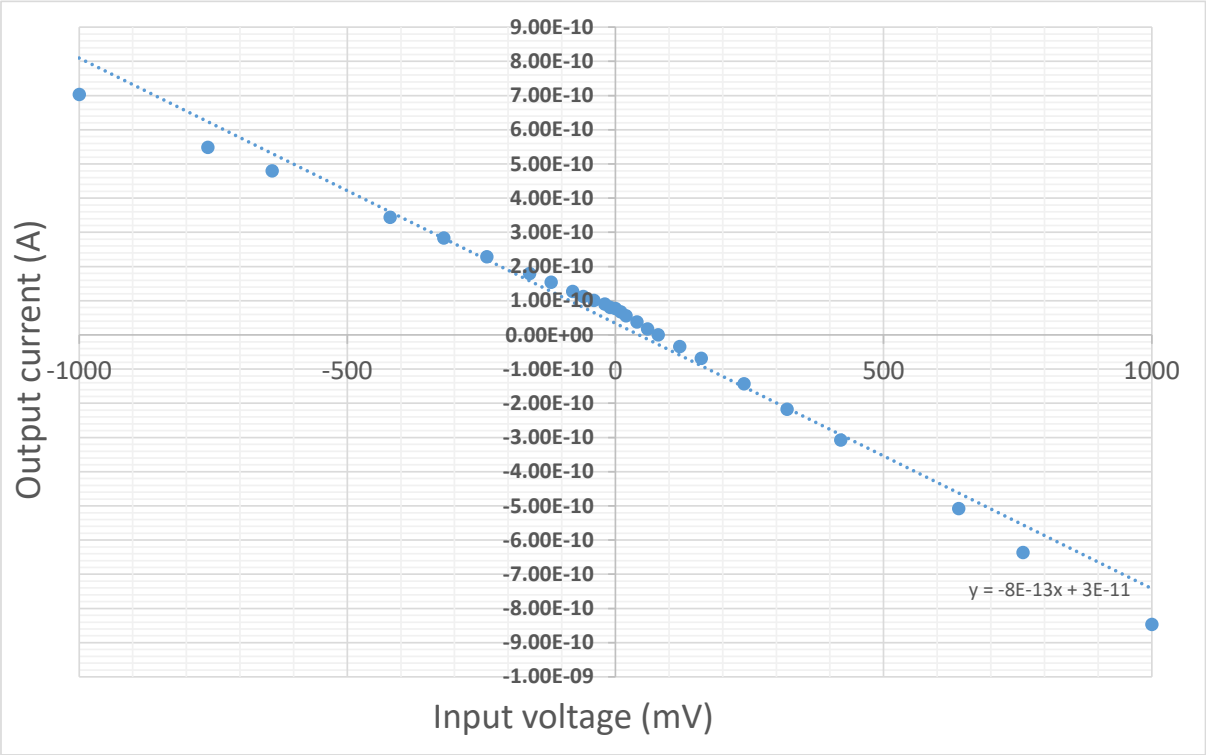

Figure 4-5 The circuit response to a DC input current.

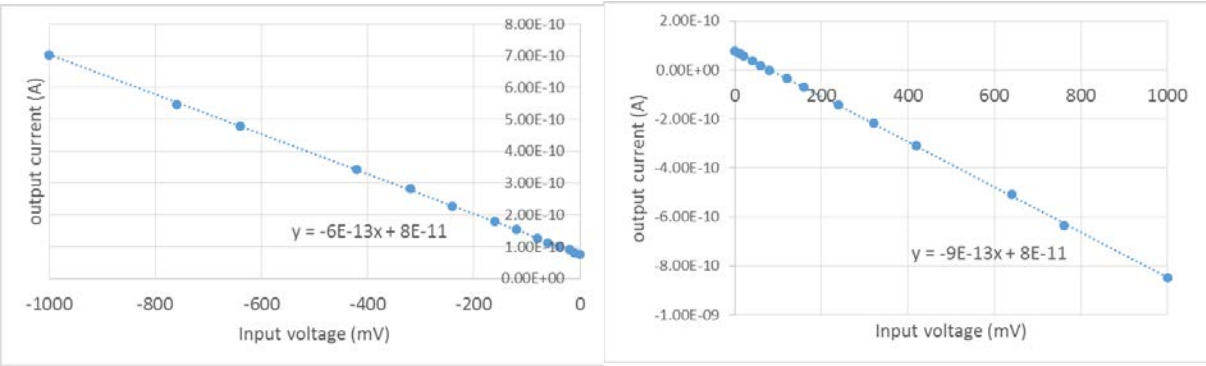

Figure 4-6 The circuit response to individual positive and negative stimulation.

After establishing system functionality, the next priority falls in proving the noise performance required to interrogate ion-channels established BLMs over the 100 kHz bandwidth. To do so, a sinusoidal input waveform is played over the input isolation capacitance in a shared

stage with a total current gain of 1000. The results are converted to a voltage signal through a trans-impedance stage and passed through a second order filter with a 3-dB frequency of 50 kHz. This value is chosen due to simulations trying to find the best filtering scheme trying to observe a 100 kHz pulse input signal. The output voltage is recoded with a keysight spectrum analyzer over 100 kHz with a sampling interval of 10Hz. Two sets of input sinusoidal frequency is given to the system, a 1 kHz signal and a 10 kHz signal. The sin signal amplitude is selected based on the values shown in Table 1 for a 10 fF input capacitance. The results are shown in Figure 4-7. As suggested in Figure 3-2, the increase in noise power over frequency spectrum due to the addition of the input 5 pF capacitance is observed by the difference in the shape of the response spectrum as suggested in Figure 4-7.

The system noise performance can be evaluated using waveforms in Figure 4-7. The input current amplitude is 50 pA. Hence, the peak signal values in all waveforms in Figure 4-7 are the result of the 50 pA sinusoidal input. This opens the path to calculating the noise floor by calculating the SNR and acquiring noise power through the following formula:

$$N_{rms} = \frac{{(A_{sin})^2}/_2}{SNR} \tag{4-3}$$

Where A_{sin} is the input current signal amplitude and N_{rms} is the r.m.s. noise power. The spectrum shown in Figure 4-7 is composed of discrete frequency elements. Each value E depicted in this figure is an average of all signal powers over the frequency step df, which is 10 Hz in this case. As a result, the depicted signal power is E_{peak}df and the total noise power is calculated through the following formula:

$$N = \int_0^{100\ kHz} Sdf = \sum Sdf \tag{4-4}$$

Where S represents the signal values presented in Figure 4-7. The Total SNR can be calculated using the following formula:

$$SNR = \frac{E_{peak}df}{\sum Sdf} = \frac{9.1900\times10^{-6}}{6.8475\times10^{-7}} = 13.421 \tag{4-5}$$

The total signal value and N for a 1 kHz input spectrum are 9.19e-6 and 6.85e-7 respectively. Hence, the total noise power can be calculated as follows:

$$N_{rms} = \frac{{(A_{sin})^2}/_2}{SNR} = \frac{{(50\ pA)^2}/_2}{13.421} = 9.3138 \times 10^{-23} \tag{4-6}$$

Hence, the total input-referred noise current 9.65 pA which is very close to the simulation estimated current of 3 pA. This proves that the presented system is capable of observing 10 pA pulse inputs at a 100 kHz bandwidth with the presence of a 5 pF input capacitance.

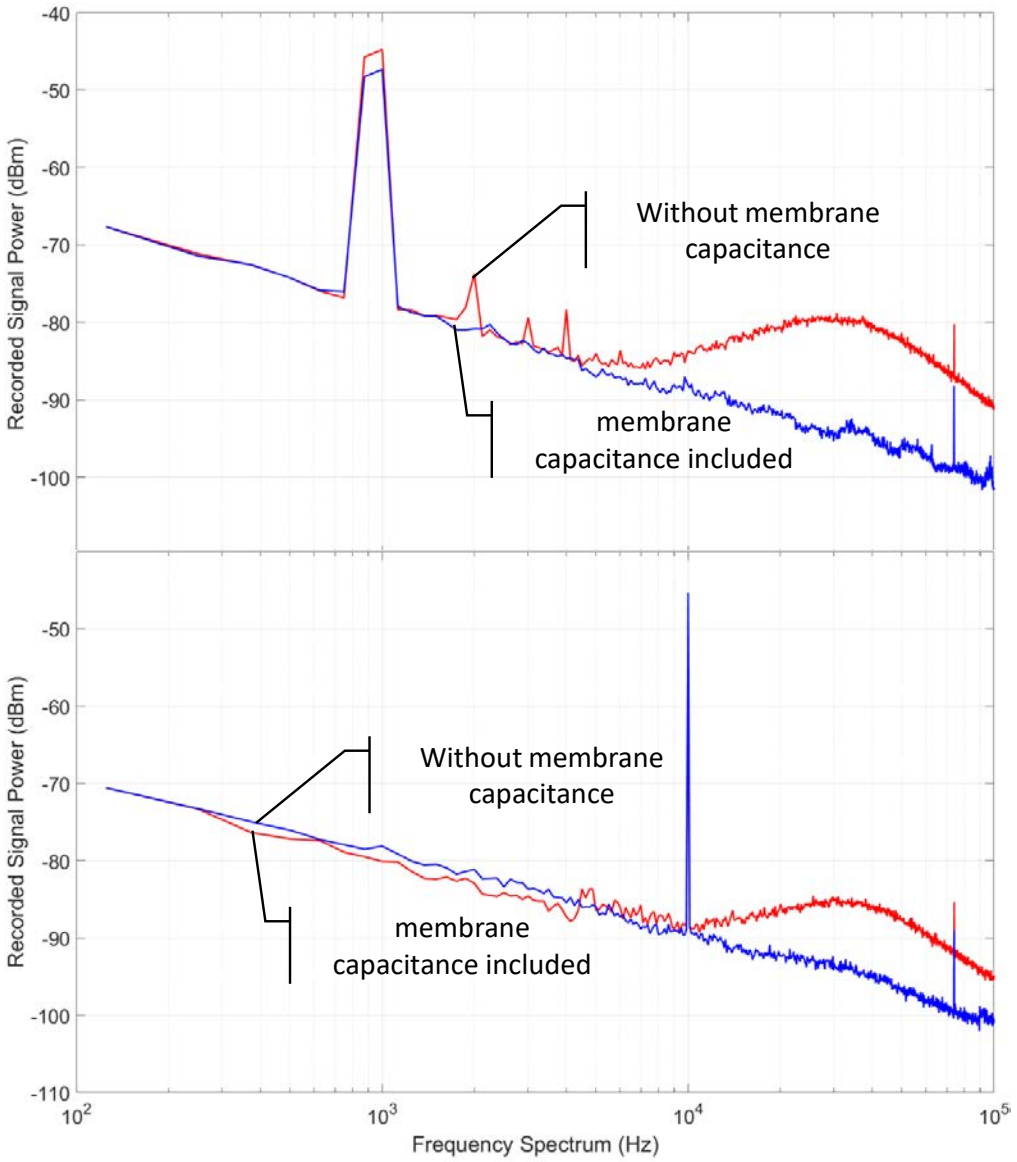

Figure 4-7 System frequency response to incoming input sinusoidal current at 1 kHz and 10 kHz frequencies with and without input membrane capacitance.

To confirm overall system functionality, a pulsed input current that mimics that of an ion channel event is given to the input channels with isolation capacitances of 100 fF. The pulse amplitude needed to test this phenomenon should be about 10 pA which is possible to produce thanks to the isolation input capacitances. Using (4-1) with a pulsed input voltage amplitude of 1

mV and a rising/falling time of 10 µs, it is possible to produce the desired 10 pA input current pulses as suggested in Figure 4-7.

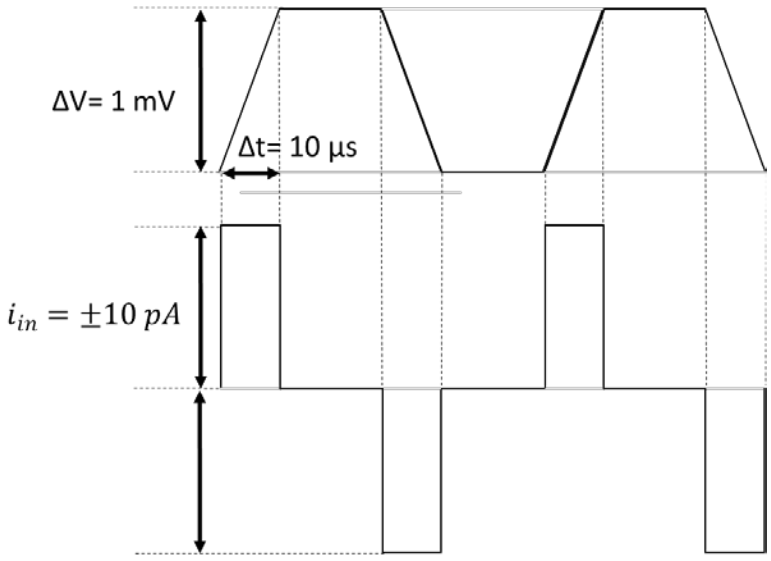

Figure 4-8 The pulsed input scheme for creating clean 10 pA pulse currents for feeding the circuit.

The input pulsed waveform is generated with an Agilent 33120A series function generator and decimated with a precise voltage divider resistive scheme. The system response to this input is shown Figure 4-9. The results are captured and stored using an Agilent DSO-X 2012A Oscilloscope. These results are recorded with the presence of a 5 pF input capacitance emulating a BLM layer with an ion-channel embedded inside and they indicate that the presented system is capable of observing pulses as small as 10 pA with a width of 10 µs. A comparison of the results and circuit dimensions are shown in Table 2. The presented circuit has comparable specs in terms of bandwidth and noise performance to the works presented in literature. However, the strength of this work relies in the fact that the area and power consumption of the presented circuit is much lower than what is usually presented in the literature despite the fact that this work has been

implemented in a much bigger technology. As a result, the presented buffer topology is suitable for interfacing arrays and ion channels in a lab-on-CMOS configuration.

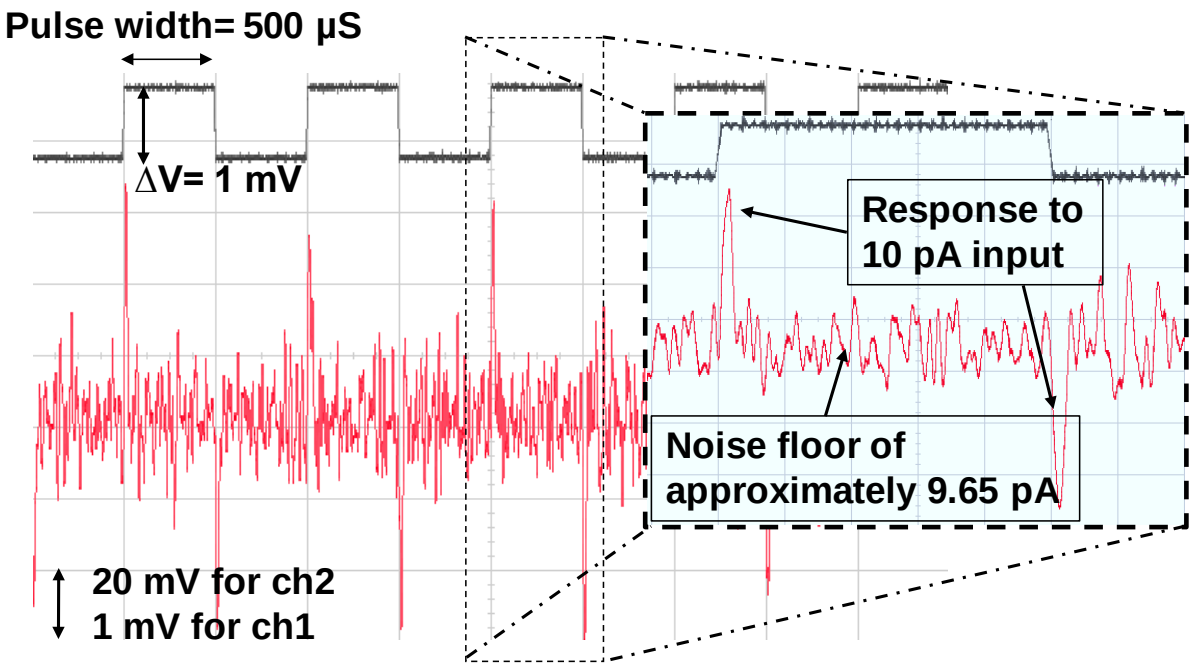

Figure 4-9 The input pulse waveform recorded from channel 1 (ch1) and the system response to the pulsed input current in channel 2 (ch2).

Table 2 Comparison of the state of art pore interface circuit performance.

	[59]	[60]	[61]	[62]	[56]	**This Work**
Membrane Capacitance	-	<20 pF	750 pF	<6 pF	10 pF	5 pF
Bandwidth	10 kHz	10 kHz	100 kHz	100 kHz	100 kHz	100 kHz
Area	0.3 mm^2	<1.25 mm^2	-	0.2 mm^2	-	0.05 mm^2
Power	502 µW	40 mW	-	5 mW	-	380 µW
RMS noise	4.2 pA@10 kHz	1.2 pA@10 kHz	90 pA@100 kHz	3.2 pA@100 kHz	7.57 pA@100 kHz	9.65pA @ 100kHz
Technology	0.35µm	0.35µm	-	0.13µm	0.35µm	0.5µm

4.4. Conclusion

This chapter presents a CMOS cheap for testing an instrumentation circuit that is aimed for interfacing ion-channels. Circuit characterization results show that the presented circuit presents adequate noise performance to interface an ion-channel with an estimated input capacitance of 5 over a bandwidth of 100 kHz with pA level input range.

5. Summary and Future work

5.1. Summary

A lab-on-CMOS design concept for high throughput analysis of ion channel proteins was described. A CMOS electrochemical interface circuit was presented to simultaneously achieve stringent requirements in terms of resolution, speed, power and area. The circuit is aimed to be used in a array structure of thousands of isolated chambers each containing a BLM layer with an ion-channel nano-pore embedded inside. The BLM layer has an intrinsic capacitance that creates a noise element that increases with frequency. This issue combined with the fact that there are stringent limitations on interface circuit area and power creates a unique challenge that has not been addressed in literature. The presented work provides a unique solution to this issue through a technique called op-amp sharing together with a transistor-only feedback structure and a unique op-amp placement topology. A test chip was implemented in AMI 0.5 µm C5N CMOS technology to test the presented design before it is implemented in an actual biological environment. The results suggest that the presented interface is capable to detect pulsed input currents in a noisy environment with the presence of input capacitance while keeping the total are and power to a minimum.

5.2. Contribution

This dissertation bridges the gap between the world of electrochemistry, especially the effort to detect single molecule events through ion-channels, and the world of microelectronics. This innovative approach can be worded as:

- *Developed a new CMOS current sensing instrumentation circuit with **superior** area, power performance over works presented in literature with adequate noise performance and bandwidth to interface ion channels*

A new CMOS instrument is designed that addresses the existing challenges in interfacing high throughput arrays of ion channels implemented on a bio-sensor chip. This circuit is able to read single molecule events on an ion-channel with an estimated BLM capacitance of 5 pf that are as low as 10 pA and as fast as 10 µs. Compared to circuits made for similar purposes, the presented design has superior performance in area and power while having a comparable accuracy and bandwidth. At its current state this new circuit would enable building a high throughput (over 500) ion-channels on a biosensor chip with the interface circuit situated right below each ion-channel. This method can be used to address the disadvantages of traditional ion-channels by helping characterize massive arrays or help detect molecules in a microfluidic solution such as DNA strands.

5.3. Future work

The future work for this project would involve perfecting the technique required for implementing the ion-channels efficiently over a lab-on-chip platform so this instrumentation technique would be used for observing the variations in ion-channel current and possibly characterizing these nano-pores.

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