

A HIGH VOLTAGE DC-DC CONVERTER FOR APPLICATIONS IN HARSH ENVIRONMENTS

By

Matthew Lee Gebben

A THESIS

Submitted to
Michigan State University
in partial fulfillment of the requirements
for the degree of

MASTER OF SCIENCE

Electrical Engineering

2012

ABSTRACT

A HIGH VOLTAGE GAIN DC-DC CONVERTER FOR APPLICATIONS IN HARSH ENVIRONMENTS

By

Matthew Lee Gebben

The constant evolution of the use of power electronics today is bringing sensitive electrical devices into harsher environments than ever before. Today, the energy and automotive industries, among others, are seeking to utilize power electronics to increase the performance and efficiency of the systems in use. This often involves using converters in close proximity to sources of heat, such as internal combustion engines or photovoltaic panels. These situations also usually require small size and low weight. The result is a need for a high efficiency converter capable of operating in high temperatures with minimal size and weight. This paper seeks to explore the options available to achieve this when considering a typical photovoltaic system. In order to meet the above conditions while operating as a micro-converter attached to the solar panels, an additional requirement for high voltage gain is added. This limits the number of existing topologies capable of being used, and has resulted in the development of a new design, detailed in this paper, that seeks to meet all of the aforementioned constraints. To make the case of the new converter, other topologies are investigated in terms of their features and costs in order to determine their best and worst attributes. This involves discussion of their operation, calculation of their relative costs, and simulations to confirm their behavior. This is followed by a look at the NX dc-dc converter, the new topology, which includes a basic investigation into its operation, followed by an analysis of its behavior and relative cost, plus simulated and experimental results.

DEDICATION

Dedicated to my mother for her constant support and encouragement

Dawn L. Gebben

May 20, 1951 – July 12, 2012

ACKNOWLEDGEMENTS

I would like to express my appreciation for the continual support, encouragement, and love of my parents during my time in graduate school. If not for everything they did, none of this would have happened. I would also like to thank Dr. Fang Z. Peng for his support and guidance during the past few years. Without his help, I never would have been able to conduct this research. Finally, I thank my colleagues at the Power Electronics and Motor Drives Laboratory. I received a great deal of help from everyone, and I can scarcely recall everything they taught me in such a short time.

TABLE OF CONTENTS

List of Figures.....	vii
1. Introduction.....	1
2. Background.....	4
2.1. The DC-DC Boost Converter.....	4
2.2. The Isolated Full-Bridge DC-DC Converter Family.....	7
2.3. The Flying Capacitor DC-DC Converter.....	19
2.4. The Multilevel Modular Capacitor Clamped DC-DC Converter.....	41
3. The NX DC-DC Converter.....	57
3.1. NX DC-DC Converter Details.....	57
3.2. NX Converter Analysis.....	65
3.3. NX Converter ZCS Possibilities.....	72
3.4. 8X Converter Experimental Results.....	79
4. Conclusions.....	88

Bibliography

LIST OF FIGURES

Figure 1. System Configuration.....	3
Figure 2. DC-DC Boost Converter.....	4
Figure 3. Boost Converter Switching Waveforms.....	5
Figure 4. Simulation Results for Boost Converter.....	6
Figure 5. Isolated Full-Bridge DC-DC Buck Converter.....	8
Figure 6. Isolated Buck Converter Model.....	9
Figure 7. Isolated Full-Bridge Buck Converter Waveforms.....	10
Figure 8. Simulated Full-Bridge Buck Converter.....	12
Figure 9. Isolated Full-Bridge DC-DC Boost Converter.....	13
Figure 10. Isolated Boost Converter Model.....	14
Figure 11. Isolated Full-Bridge Boost Converter Waveforms.....	15
Figure 12. Simulated Full-Bridge Boost Converter.....	17
Figure 13. Flying Capacitor DC-DC Converter.....	20
Figure 14. Flying Capacitor Switching State I.....	21
Figure 15. Flying Capacitor Switching State II.....	22
Figure 16. Flying Capacitor Switching State III.....	23
Figure 17. Flying Capacitor Switching State IV.....	24
Figure 18. Simulated Flying Capacitor DC-DC Converter Waveforms.....	26
Figure 19. The 3X DC-DC Converter.....	29
Figure 20. 3X Converter 1X Switching State.....	31
Figure 21. 3X Converter 2X Switching State I.....	32

Figure 22. 3X Converter 2X Switching State II.....	33
Figure 23. 3X Converter 3X Switching State I.....	34
Figure 24. 3X Converter 3X Switching State II.....	35
Figure 25. 3X Converter 3X Switching State III.....	36
Figure 26. 1X to 2X Transition with 10 nH Stray Inductance.....	37
Figure 27. 1X to 2X Transition with 100 nH Stray Inductance.....	38
Figure 28. 2X to 3X Transition with 10 nH Stray Inductance.....	40
Figure 29. 2X to 3X Transition with 100 nH Stray Inductance.....	40
Figure 30. The MMCCC.....	42
Figure 31. The MMCCC Module.....	42
Figure 32. MMCCC Switching State I.....	43
Figure 33. MMCCC Switching State II.....	44
Figure 34. MMCCC Simulation Results.....	47
Figure 35. ZCS-MMCCC.....	48
Figure 36. ZCS-MMCCC Switching State I.....	49
Figure 37. ZCS-MMCCC Switching State II.....	50
Figure 38. ZCS-MMCCC C4 Voltage Example.....	53
Figure 39. ZCS-MMCCC Simulation Output Voltage and Inductor Currents.....	54
Figure 40. ZCS-MMCCC Simulation Capacitor Voltages.....	54
Figure 41. ZCS-MMCCC Input Current.....	55
Figure 42. ZCS-MMCCC 4-Phase Input Current.....	56
Figure 43. The 6X DC-DC Converter.....	58
Figure 44. The Modular 6X DC-DC Converter.....	58

Figure 45. The NX Converter Module.....	59
Figure 46. 6X Switching State I.....	60
Figure 47. 6X Switching State II.....	61
Figure 48. 6X Simulation Input and Output Voltages.....	63
Figure 49. 6X Simulation Capacitor Voltages.....	64
Figure 50. The ZCS 6X Converter.....	73
Figure 51. ZCS 6X Converter Switching State I.....	74
Figure 52. CS 6X Converter Switching State II.....	74
Figure 53. ZCS 6X Simulation Input and Output Voltages.....	77
Figure 54. ZCS 6X Simulation Inductor Currents.....	77
Figure 55. ZCS 6X Simulation Capacitor Voltages.....	78
Figure 56. The 1-kW 8X prototype (For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis).....	81
Figure 57. 8X Prototype Converter Waveforms with $V_{in}=10\text{ V}$ (Channel 1: V_{gs}, 20 V/div; Channel 2: V_{ds}, 10 V/div; Channel 3: V_{ds}, 10 V/div; Channel 4: I_s, 5 A/div).....	82
Figure 58. Simulated 8X I_s Current Waveform.....	83
Figure 59. 8X Prototype Converter Waveforms with $V_{in}=10\text{ V}$ (Channel 1: V_{gs}, 20 V/div; Channel 2: V_{out}, 25 V/div; Channel 3: V_{in}, 5 V/div; Channel 4: I_s, 5 A/div).....	84
Figure 60. 8X Prototype Converter Waveforms with $V_{in}=18\text{ V}$ (Channel 1: V_{gs}, 20 V/div; Channel 2: V_{out}, 50 V/div; Channel 3: V_{in}, 10 V/div; Channel 4: I_s, 10 A/div).....	85
Figure 61. 8X Prototype Converter Waveforms with $V_{in}=20.4\text{ V}$ (Channel 1: V_{gs}, 20 V/div; Channel 2: V_{out}, 50 V/div; Channel 3: V_{in}, 10 V/div; Channel 4: I_s, 10 A/div).....	85
Figure 62. 8X Prototype Converter Waveforms with $V_{in}=35\text{ V}$ (Channel 1: V_{gs}, 20 V/div; Channel 2: V_{out}, 100 V/div; Channel 3: V_{ds}, 25 V/div; Channel 4: I_s, 10 A/div).....	86

Figure 63. 8X Prototype Converter Waveforms with $V_{in}=37\text{ V}$ (Channel 1: V_{gs} , 20 V/div ; Channel 2: V_{out} , 100 V/div ; Channel 3: V_{ds} , 25 V/div ; Channel 4: I_{ls} , 10 A/div).....86

Figure 64. Efficiency vs. Output Power for the 8X Prototype.....87

1. Introduction

Today, power electronics are making an ever greater impact on all areas of industry. As energy costs climb and greater control is desired, the drive for greater efficiency fuels the growth of the power electronics field. In the automotive industry, vehicles are increasingly reliant on power electronics for supplying their drive-trains and other systems; in the aerospace industry, the need to maximize fuel economy has led to a desire for both maximized efficiency and minimized weight. The energy sector is also seeing rapid growth in the use of power electronics. The proliferation of solar and wind power has led to a need for more power electronics circuits operating on the grid than ever before. Solar power, in particular, raises issues in common with those in the other aforementioned industries. Like other areas, great importance is placed on efficiency, reliability, and environmental tolerance. Photovoltaic (PV) modules present an interesting set of design challenges.

In many situations, the voltage supplied by photovoltaic modules is too low to be of much use by itself. Furthermore, the module only supplies direct current electricity, so it needs to be inverted for many systems. This state of affairs makes power electronics vital for the use of PV modules. PV modules, such as the Mitsubishi Electric PV-MJT250GB, have maximum output voltages of roughly 40 V [1]. Although it may be tempting to suggest placing multiple panels in series to achieve a higher voltage, the reliability would be adversely affected and the current capabilities would be low. From this point of view, it is necessary to place multiple panels in parallel to maximize reliability and current (power) capability. This necessitates the use of a high voltage gain dc-dc converter to boost the voltage to a more useful level. Considering this, several options are available; either one high power converter can be used to

convert the voltage from all the cells together, or multiple smaller converters can be used with each module to boost the voltage. Furthermore, the task of regulating the voltage can fall to either the dc-dc converter, or to the inverter. These choices make for a high degree of freedom when designing power electronics systems for PV sources. This means some assumptions must be made in order to focus on a more manageable set of options.

One aspect of design that engineers should always consider is cost. In situations involving mass production or the installation of a large number of facilities, the cost of the electronics used must be minimized. With this in mind, the cost of employing one high power converter could easily outweigh the price of using multiple low power converters. Furthermore, the use of small dc-dc converters coupled to each PV module would increase the system's overall reliability; even if one converter was to fail, the dc-bus voltage would still be useable. Cost and reliability make an excellent case for the use of low power dc-dc micro-converters fixed to each PV panel. However, this still leaves many options available. From the standpoint of cost and reliability, the traditional topologies are easily obtained on the commercial market and have been used for many years. Furthermore, most of these designs are capable of regulating the voltage of the dc bus. Nevertheless, as will be shown, they may not be the best choices for this situation, where high voltage gain and high temperature capabilities are a must. More recent topologies, such as the many switched-capacitor designs out there, are capable of high voltage gain and have designs well-suited for operation at high temperatures. However, the number of components can easily be larger, and the option of voltage regulation is not always available. Before getting into the finer details, it is important to examine the overall situation.

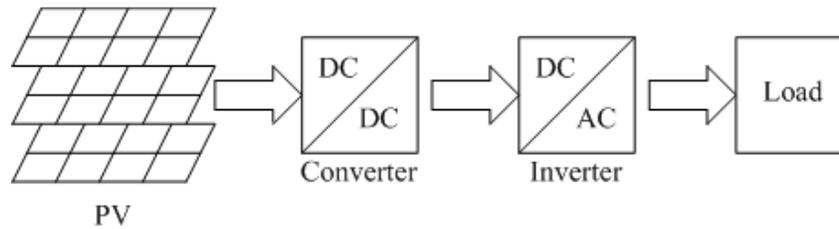


Figure 1. System Configuration

Consider the general situation described in Figure 1. The PV module is connected to a dc-dc converter, which is then connected to the load through an inverter. Here, due to the nature of solar cells, bi-directional power flow is unnecessary. Ignoring the inverter, the options for the dc-dc converter have already been made clear. To make a clear progression to the latest converter technologies, it is important to start by introducing the older circuits. In this fashion, the case for each design can be more easily made. With that in mind, the oldest and most basic design to consider is obviously the traditional boost converter. From this, further exploration will be done by examining the traditional isolated topologies, such as the isolated full-bridge converter, which is likely one of the most popular designs currently in use. Having looked at the older designs, the switched capacitor designs can be explored; this study can begin with the flying capacitor topology and can work its way up to the multilevel modular capacitor-clamped converter (MMCCC). This provides an excellent base from which the merits of the new topology can be expounded upon.

As alluded to before, a new switched-capacitor dc-dc converter design has been developed, and its positive and negative features will be detailed in later sections. The design seeks to achieve both the high voltage gain and high temperature operation capabilities without many of the drawbacks suffered by other designs.

2. Background

The situation as described in Figure 1 leaves many options available. Focusing on the dc-dc converter, voltage regulation, isolation, and the use of magnetic components are factors to consider. Nevertheless, the inverter can, to a degree, regulate the voltage output of the system, and the necessity of galvanic isolation is debatable. Before a complete discussion of a new dc-dc converter topology is possible, a thorough understanding of the other options is necessary. To this end, it makes sense to begin with one of the oldest and most basic of the dc-dc converters: the boost converter.

2.1. The DC-DC Boost Converter

Consisting of only two switching devices, an inductor and a capacitor, the dc-dc boost converter is the most basic converter to consider for this application.

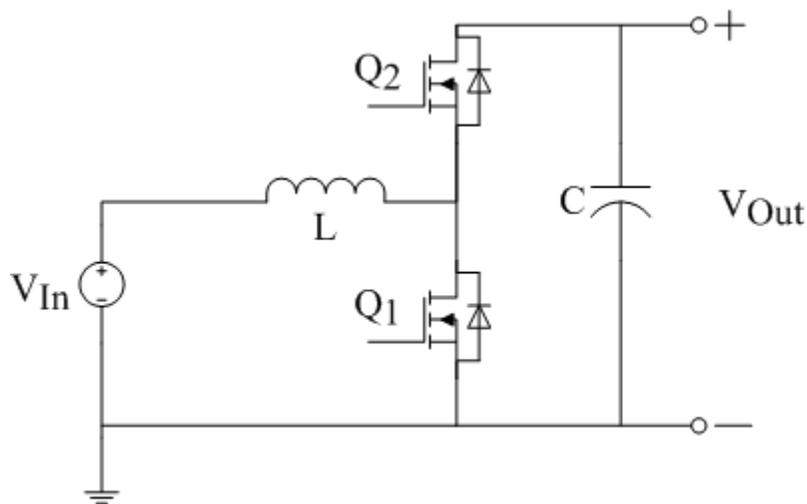


Figure 2. DC-DC Boost Converter

In Figure 2 the dc-dc boost converter circuit can be seen. Although depicted using MOSFETs, any suitable switch would work. This converter also lacks isolation, although that is only a problem if isolation is required. As suggested by the name, the converter boosts the input

voltage to any higher voltage. In theory, the voltage gain could even be infinity, but the truth is much less phenomenal. In this converter, Q_1 and Q_2 function as a complementary pair; while Q_1 is on, Q_2 is off and vice-versa. The time that Q_1 is on versus the total switching period is referred to as the duty cycle, D . It is this D that controls the output voltage. The switching behavior along with the inductor waveforms, can be seen in Figure 3.

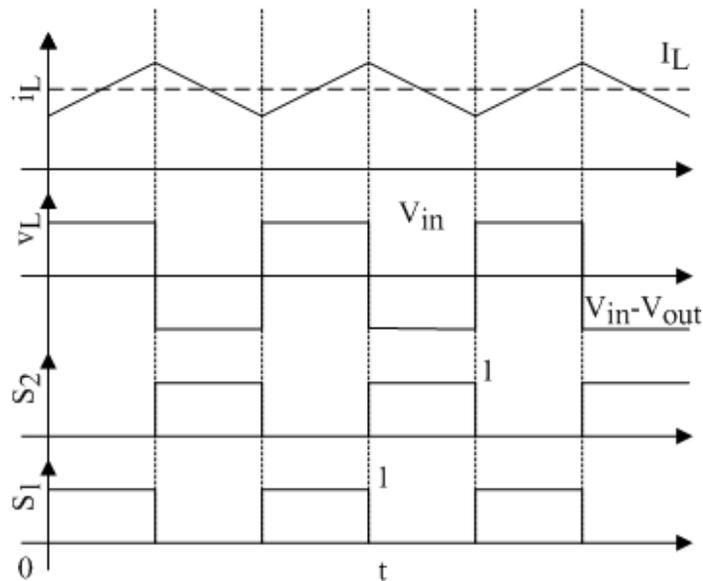


Figure 3. Boost Converter Switching Waveforms

When S_1 is equal to 1, Q_1 is on and Q_2 is off; likewise, when S_2 equals 1, Q_2 is on and Q_1 is off.

So the voltage across the inductor is equal to the input voltage while Q_1 conducts, and is equal to the input voltage minus the output voltage while Q_2 is conducting. Since the voltage across the inductor must average to zero, the following situation occurs.

$$\begin{aligned}
V_L = 0 &= V_{in}D + (V_{in} - V_{out})(1 - D) \Rightarrow \\
0 &= V_{in}D + V_{in} - V_{out} - V_{in}D + V_{out}D \Rightarrow \\
0 &= V_{in} - V_{out} + V_{out}D = V_{in} + (D - 1)V_{out} \Rightarrow \\
-V_{in} &= (D - 1)V_{out} \Rightarrow \\
V_{in} &= (1 - D)V_{out} \Rightarrow \\
\frac{V_{out}}{V_{in}} &= \frac{1}{1 - D}
\end{aligned}
\tag{2.1.1}$$

As seen in (2.1.1), the voltage gain theoretically increases as D goes from 0 to 1; (2.1.1) approaches infinite as D approaches 1. To better illustrate an example of this, a simulation was performed using Saber Simulator. The switching frequency was 100 kHz , using a $50\text{ }\mu\text{H}$ inductor, a $100\text{ }\mu\text{F}$ output capacitor, and a $20\text{ }\Omega$ load resistor. The input voltage was 20 V , with a duty cycle of 40% . The results can be seen in Figure 4.

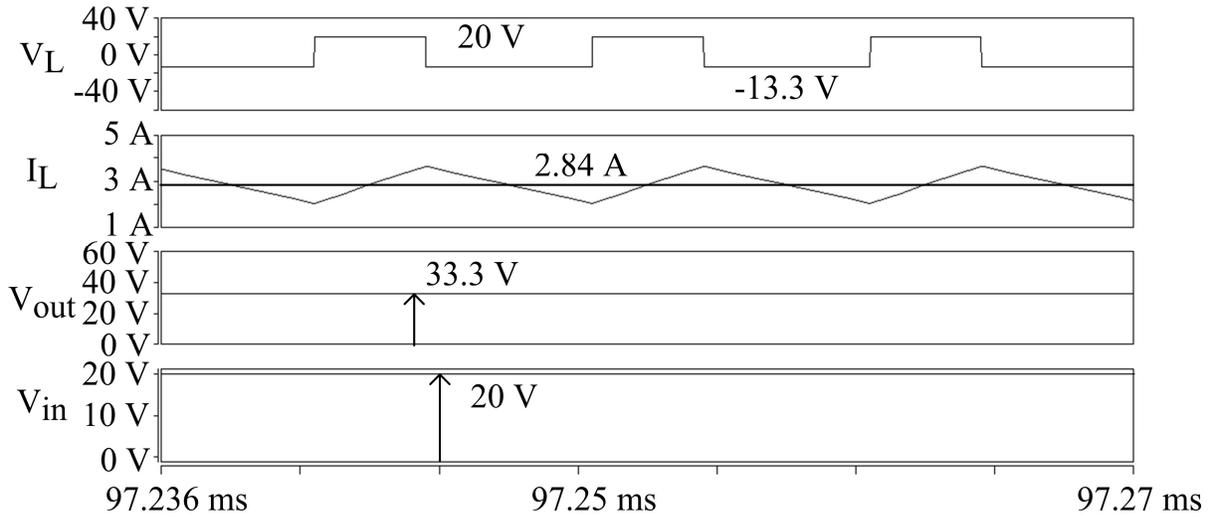


Figure 4. Simulation Results for Boost Converter

The results were slightly off from their ideal values, due to losses in the switches on-resistances. Nevertheless, the results match up very nicely to expectations for these conditions. However, as this suggests, losses in the switches and inductor would greatly limit the actual capabilities of the converter [2]. All analysis will be based of the assumption that the converter is in continuous-

conduction mode (CCM). Consider the total device stress ratio of the boost converter, a relative measure of the cost of the semiconductor devices. First, assume the converter is lossless ($P_{in}=P_{out}$), and set P_{out} , V_{out} and I_{out} to 1 p.u. (per unit). The result is that:

$$\bar{R}_S = 2 \times V_{out} \times I_{in} = 2 \times \frac{P_{out}}{1-D} = 2 \times 1 \text{ p.u.} \times \frac{1 \text{ p.u.}}{1-D} = \frac{2}{1-D} \text{ p.u.} \quad (2.1.2)$$

In (2.1.2), \bar{R}_S is the total device stress ratio using the average values of the circuit's voltages and currents. There are two switches, and each must be able to block the output voltage and pass the input current. This led to the above result, which shows a major flaw in this converter's use in this application; as the voltage gain increases, the device stresses also increase, asymptotically approaching infinity as D goes to 1. Even for a relatively low duty cycle, like 0.5, the stress ratio would already be 4 p.u. This converter would not be practical for applications requiring very high voltage gains, such as photovoltaic arrays. Furthermore, the switch utilization factor of the boost converter, defined as the output voltage divided by the switch power rating, is:

$$\frac{P_{out}}{P_S} = \frac{1 \text{ p.u.}}{\frac{1 \text{ p.u.}}{1-D}} = (1-D) \quad (2.1.3)$$

This is the same for each switch, and it is clear that the switch utilization becomes increasingly poor as the voltage gain is increased. This again suggests that the boost converter, despite its initially apparent high voltage gain capabilities, is, in fact, not suited to this application.

2.2. The Isolated Full-Bridge DC-DC Converter Family

The isolated full-bridge dc-dc converter family consists of some of the most commonly employed topologies. These converters are simply slightly evolved versions of their older buck and boost converter cousins. As the name would suggest, these converters are isolated, through

the use of a transformer, and use a full-bridge configuration of four active switches. Whether or not the system's inductor is before the active switches or after the rectifier determines the type of converter. Thus, there are two configurations to consider in this topology family: the voltage-fed buck converter and the current-fed boost converter. Of these two circuits, the isolated full-bridge buck converter is the most commonly employed. However, either circuit could be viewed as applicable for this PV application. The converter has galvanic isolation via the transformer, which also offers the possibility of high gain through the use of a large turn ratio. The operations of these converters vary slightly from their simpler predecessors.

Starting with the more common of the two converters, the isolated full-bridge buck converter can be seen in Figure 5 below. This is basically just an extended version of the buck converter.

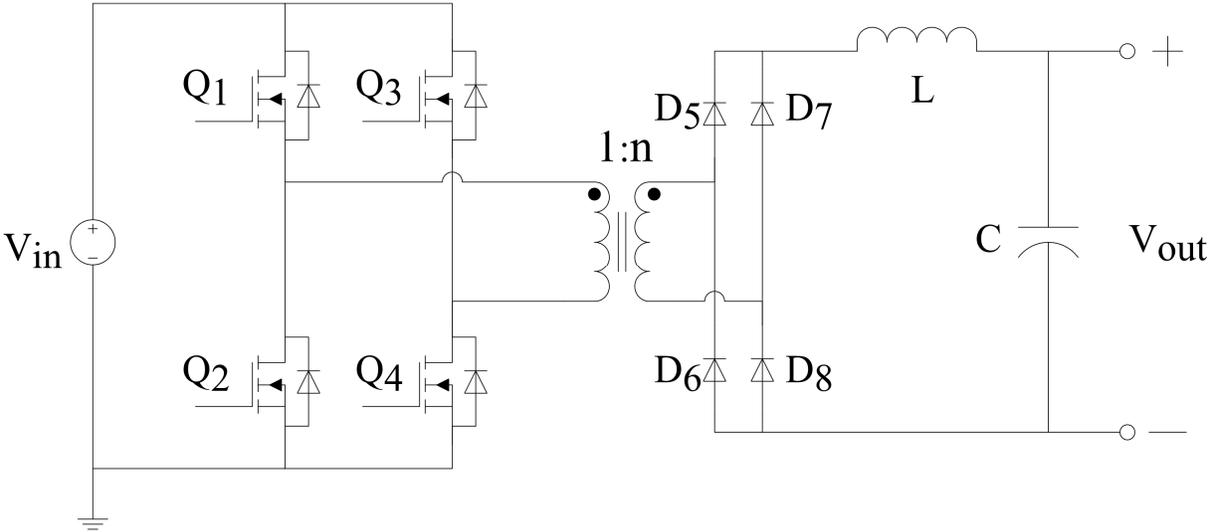


Figure 5. Isolated Full-Bridge DC-DC Buck Converter

The switching pattern of this converter is slightly different than that of its non-isolated cousin, however. This converter switches $[Q_1, Q_4]$ and $[Q_2, Q_3]$ in pairs, but it does not do so complementarily; instead, this circuit makes extensive use of the dead-time between the two

switching states. The topology's operation can be better understood through the use of a roughly equivalent model. Seen in Figure 6, it is assumed that the transformer is nearly ideal; in other words, leakage inductances are not considered and the magnetizing inductance is very large.

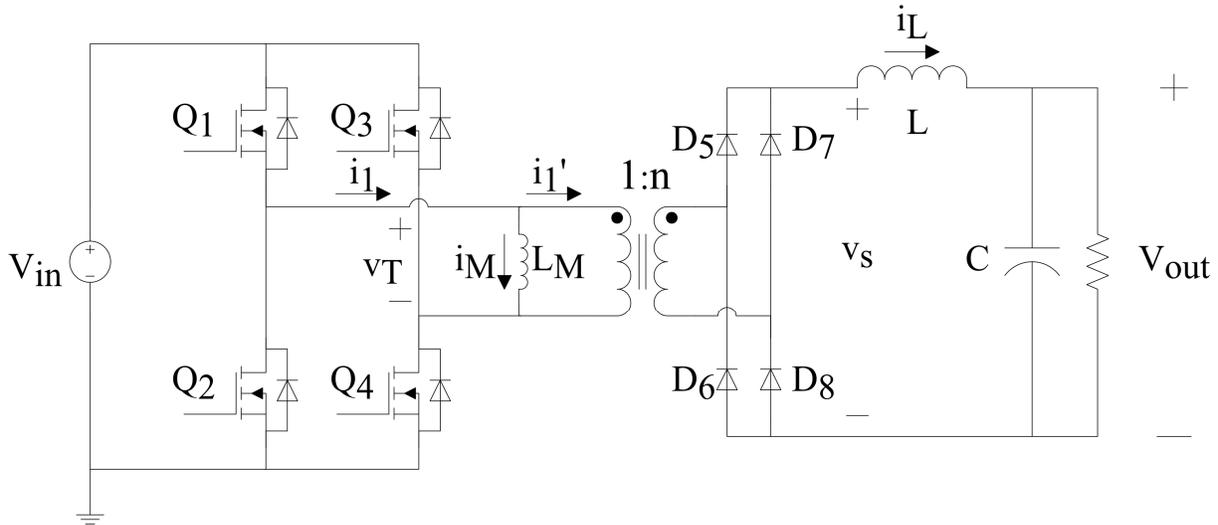


Figure 6. Isolated Buck Converter Model

Here the magnetizing inductance, L_M , is visible before the ideal transformer with its turn ratio of n . The voltage across the magnetizing inductance and the transformer itself is called v_T , while the voltage seen across the rectifier output is called v_S . It is this voltage, v_S , that works to determine the inductor current, i_L . During this analysis, it is assumed that the inductor current is always continuous, and that the diodes are ideal; no forward voltage drops across the diodes are considered. The switches are also considered ideal, and transformer characteristics such as hysteresis and saturation are never modeled. This greatly simplifies the analysis without much distortion from the actual function. To begin, note the eight waveforms graphed in Figure 7 below; these describe the action of the ideal converter in detail [3].

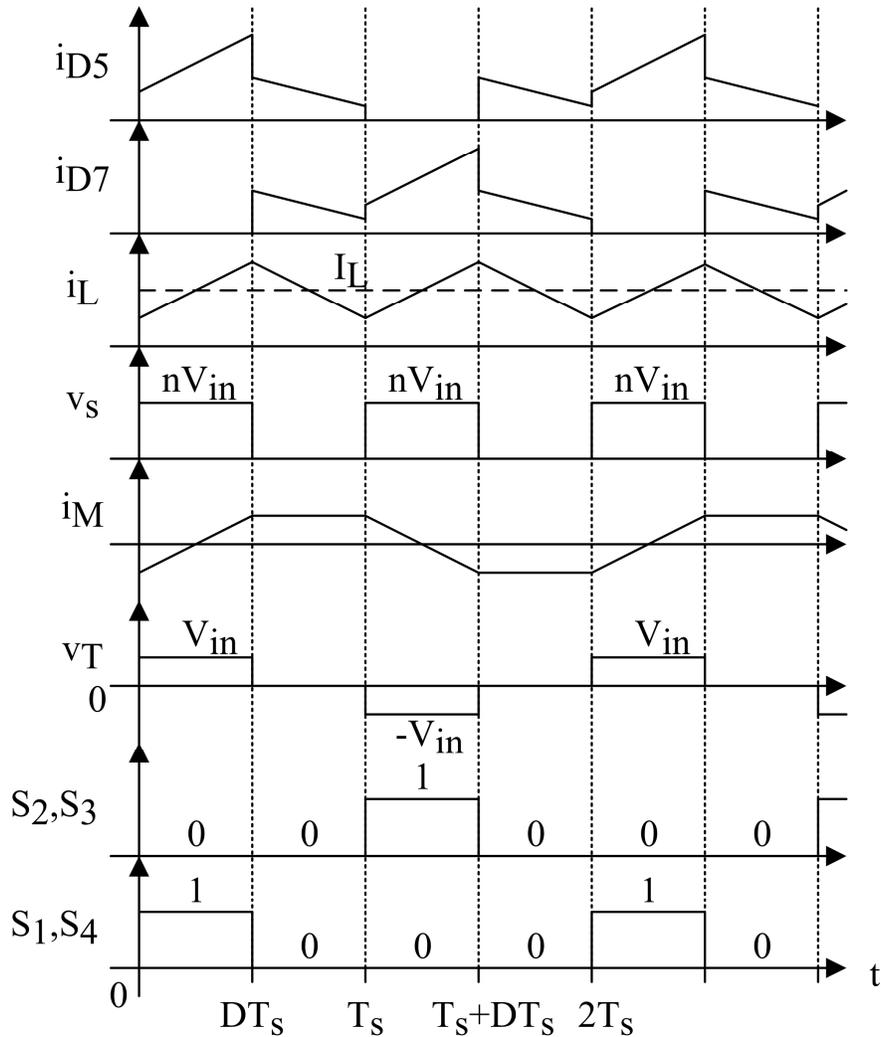


Figure 7. Isolated Full-Bridge Buck Converter Waveforms

Drawn with a 50 percent duty cycle in mind, these ideal waveforms show how the isolated buck converter functions. Note that the duty cycle itself is defined slightly differently from before, however; now the duty cycle, D , refers to the amount of time one pair of switches is turned on during one switching cycle, with this pair alternating each cycle. For instance, during the period $0 < t < DT_s$, the switches Q_1 and Q_4 are on. In this situation, the voltage across the transformer magnetizing inductance, v_T , is raised to V_{in} , and the magnetizing current (i_M), which should be

small, ramps up. Thus nV_{in} appears across the transformer's secondary winding, and diodes D_5 and D_8 conduct the inductor current, i_L . Because the voltage across the inductor is now positive, the current there also ramps up. This pattern of events is repeated in a symmetric fashion while Q_2 and Q_3 conduct during the period $T_s < t < T_s + DT_s$. However, the period $DT_s < t < T_s$ is slightly different. During this time, none of the active switches conduct, and the transformer voltage drops to zero. Thus the secondary voltage is also zero. However, the inductor current is still flowing, so all of the rectifier diodes conduct it; the current is evenly divided between the two rectifier legs. Nevertheless, this period of time keeps the output inductor current under control. From all of this, the relationship between the input and output voltages can be derived.

Since the voltage across an inductor must, on average, be zero, it is clear that the average output voltage, V_{out} , is equal to the average rectifier output voltage, v_s . From the fact that v_s equals nV_{in} for a fraction D of the total switching period, T_s , it is clear that this average must be equal to nDV_{in} . Thus, it is clear that:

$$V_{out} = nDV_{in} \quad (2.2.1)$$

In order to prove the validity of this analysis beyond what is simply described in a textbook, a simulation was performed with Saber Simulator. The test used a 50% duty cycle as defined above, but the simulation software finds it difficult to implement the use of a transformer. To this end, a simple one to one ratio was assumed and a large inductor was placed where the magnetizing inductance would be found. The results of the simulation, which very closely match the idealized waveforms presented above, can be found in Figure 8 below.

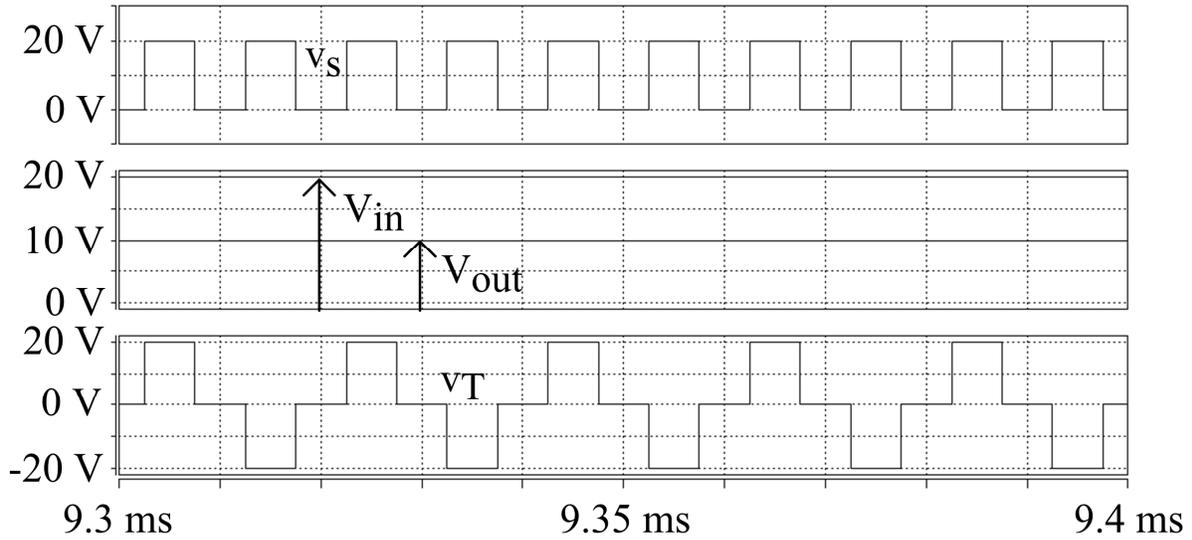


Figure 8. Simulated Full-Bridge Buck Converter

As expected, with a duty cycle of 0.5 and a unity turns ratio, the output is half of the input. To better get a feel for the usefulness of this topology, however, further analysis is required. Because the current through the magnetizing inductance is very small, the current that each switch must conduct is equal to the inductor current reflected across the transformer. Thus it can be said, on average, the active switch current is equal to nI_{out} . Each switch must also block the input voltage. Assuming that the cost of a diode is significantly less than that of an active switch, the device stress of the rectifier diodes will be ignored. Then the following is obtained.

$$\bar{R}_S = 4 \times nI_{out} \times \frac{V_{out}}{nD} = \frac{4P_{out}}{D} = 4 \times 1 \text{ p.u.} \times \frac{1 \text{ p.u.}}{D} = \frac{4}{D} \text{ p.u.} \quad (2.2.2)$$

This assumes that the output voltage and current each equal 1 per unit, and the converter is considered lossless. The positive side of this result is that the total device stress is relatively low if the converter were used in this boosting application, as most of the boosting would be accomplished through the transformer. This seems a rather inefficient method of doing things, however. It quickly follows that the switch utilization factor is:

$$\frac{P_{out}}{P_S} = \frac{1 p.u.}{\frac{1 p.u.}{D} \times 1 p.u.} = \frac{1}{\frac{1}{D}} = D \quad (2.2.3)$$

The switch utilization factor in this case would be fine, but it would require the transformer for the entirety of the boosting. This situation is less than ideal. Although this voltage-fed topology is more common than its current-fed cousin, it may not be the isolated full-bridge dc-dc boost converter best suited to this task.

The isolated full-bridge dc-dc converter was derived from the standard boost converter in much the same way that the isolated full-bridge buck converter came from the buck converter. The system circuit looks very much like its voltage-bucking cousin, but the operation itself is slightly different, as will be shown. The circuit can be seen in Figure 9 below.

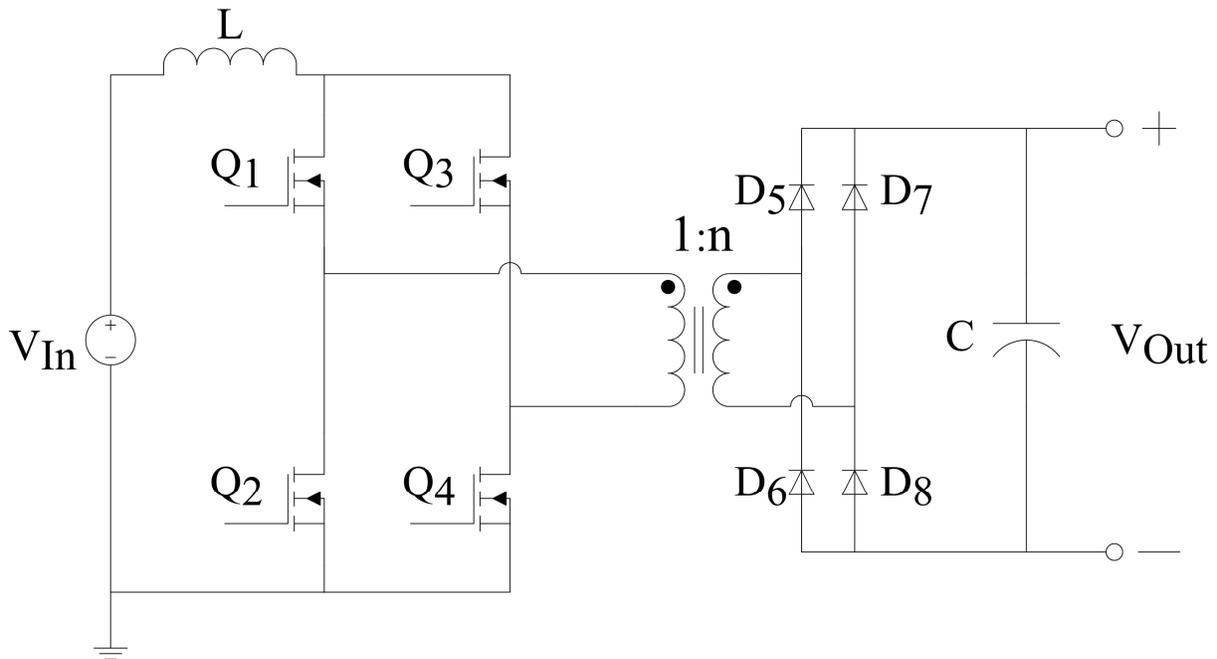


Figure 9. Isolated Full-Bridge DC-DC Boost Converter

The primary difference between this and the buck converter in Figure 5 is that the inductor location has been changed; the inductor has been shifted from being by the output to being by the input, making this a current fed converter. As such, it is obvious that the previously used

switching schemes must be ignored, since no dead-time can be allowed with the source supplying a continuous input current to the H-bridge. Any dead-time at all would cause a massive voltage overshoot across the inductor, likely leading to a damaged or inoperable converter. This necessitates a good deal of care when using this converter topology. Before analyzing the circuit, it is important to define the variables of interest. To this end, refer to the revised circuit schematic in Figure 10.

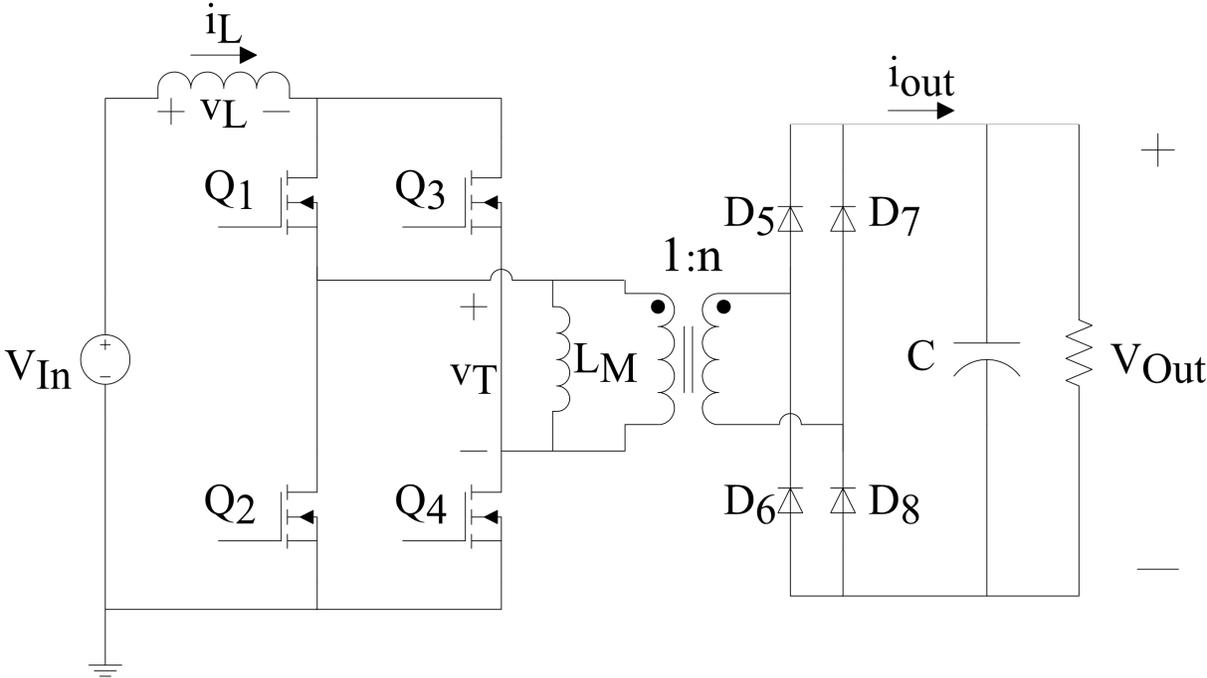


Figure 10. Isolated Boost Converter Model

The input and inductor current are now one and the same, and it is referred to, once again, as i_L . The voltage across the inductor is v_L and the voltage across the transformer and its magnetizing inductance is yet again v_T . The current leaving the rectifier is called i_{out} , despite the fact that the current that the load resistor sees is slightly different. So long as the output capacitor is large enough, the load current is continuous. As previously stated, it is obvious that at least one pair of

H-bridge switches, either $[Q_1, Q_4]$ or $[Q_2, Q_3]$, must be on at all times. Now, instead of having dead-time, it is apparent that shoot-through states for the H-bridge are needed instead; in other words, all of the switches need to be turned on at times. In order to better visualize the situation at hand, consider the waveforms illustrated in Figure 11. These give a general idea of how the converter operates [3].

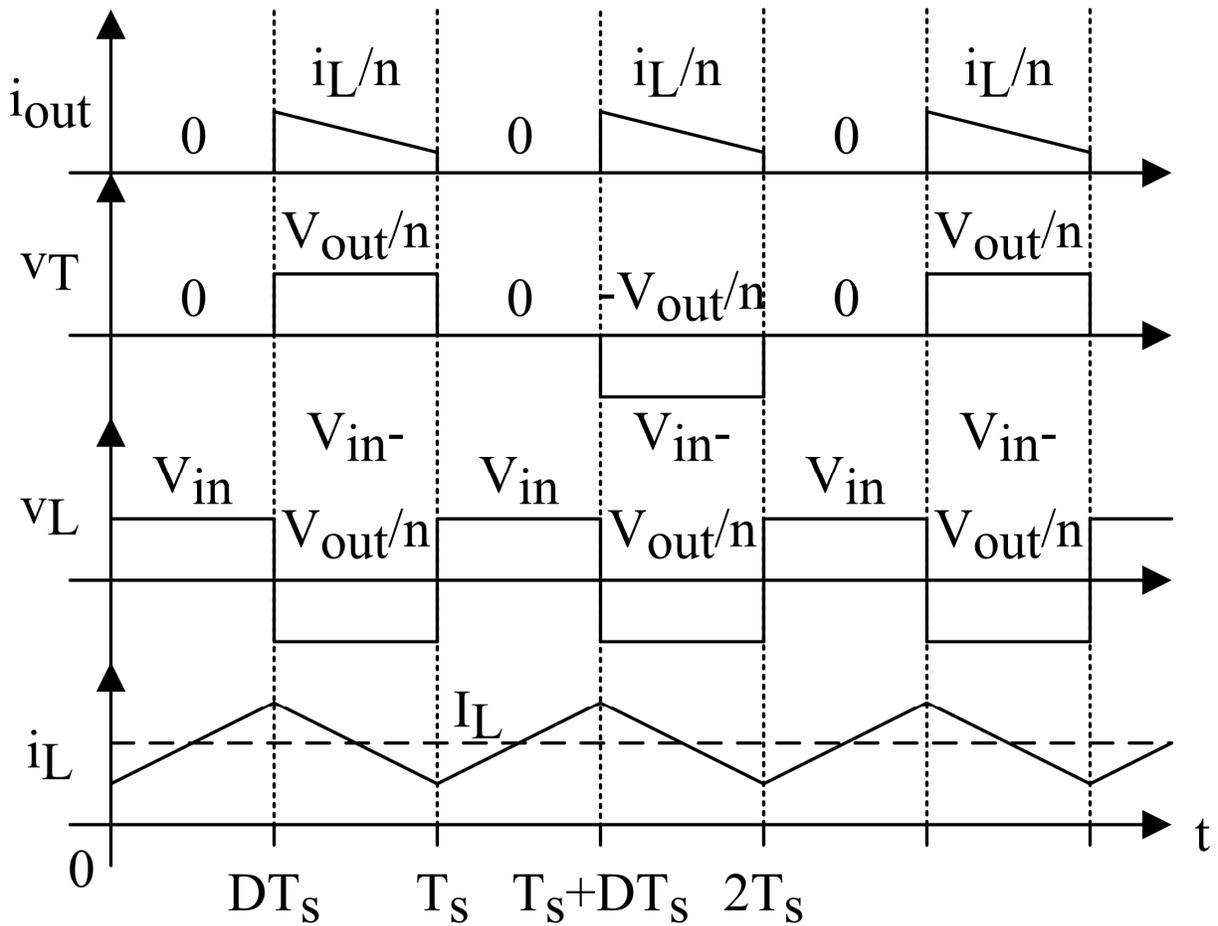


Figure 11. Isolated Full-Bridge Boost Converter Waveforms

Here the behavior of the converter can clearly be seen. During the first period of time, $0 < t < DT_s$, all of the H-bridge switches are turned on. This drives v_T to zero and throws the input voltage,

V_{in} , across the inductor. Because the transformer primary is seeing zero volts, the secondary is also at zero potential, and i_{out} is zero. The load current must be supplied by the capacitor during this period of time. In the meantime, the inductor current ramps up from the positive voltage across it. This pattern of events is repeated whenever all of the active switches are turned on, repeating each switching period for a time of DT_S . Now consider the period $DT_S < t < T_S$. During this length of time, the H-bridge pair $[Q_1, Q_4]$ is turned on and $[Q_2, Q_3]$ is off. Now the output voltage, V_{out} , is reflected back to the primary, so v_T equals V_{out} divided by the turns ratio, n . Because V_{out} is assumed to be larger than the input by a good margin, the inductor voltage drops into the negative and the inductor current ramps down. Furthermore, because D_5 and D_8 are now forward biased, the current i_{out} is equal to the input inductor current divided by n . These events are mirrored later on when the switch pairs' rolls are reversed. The end result is a continuous pattern like that in Figure 11. Again, using the concept of volt-second balance in the inductor to recognize that the voltage across it is, on average, zero, the following relationship can be derived:

$$\begin{aligned}
0 &= DV_{in} + (1-D)\left(V_{in} - \frac{V_{out}}{n}\right) = DV_{in} + V_{in} - DV_{in} - \frac{V_{out}}{n} + \frac{DV_{out}}{n} \\
\Rightarrow 0 &= V_{in} - (1-D)\frac{V_{out}}{n} \Rightarrow \frac{V_{out}}{n}(1-D) = V_{in} \\
\Rightarrow \frac{V_{out}}{V_{in}} &= \frac{n}{1-D}
\end{aligned} \tag{2.2.4}$$

Like the standard boost converter, (2.2.4) makes it clear that the isolated full-bridge boost converter provides an identical voltage gain multiplied further by the transformer turns ratio. This implies that truly high boost ratios can be obtained. In order to confirm the function of this converter, a simple simulation was again performed using Saber while assuming a unity turns ratio and a 50% duty cycle. The results can be seen in Figure 12 below.

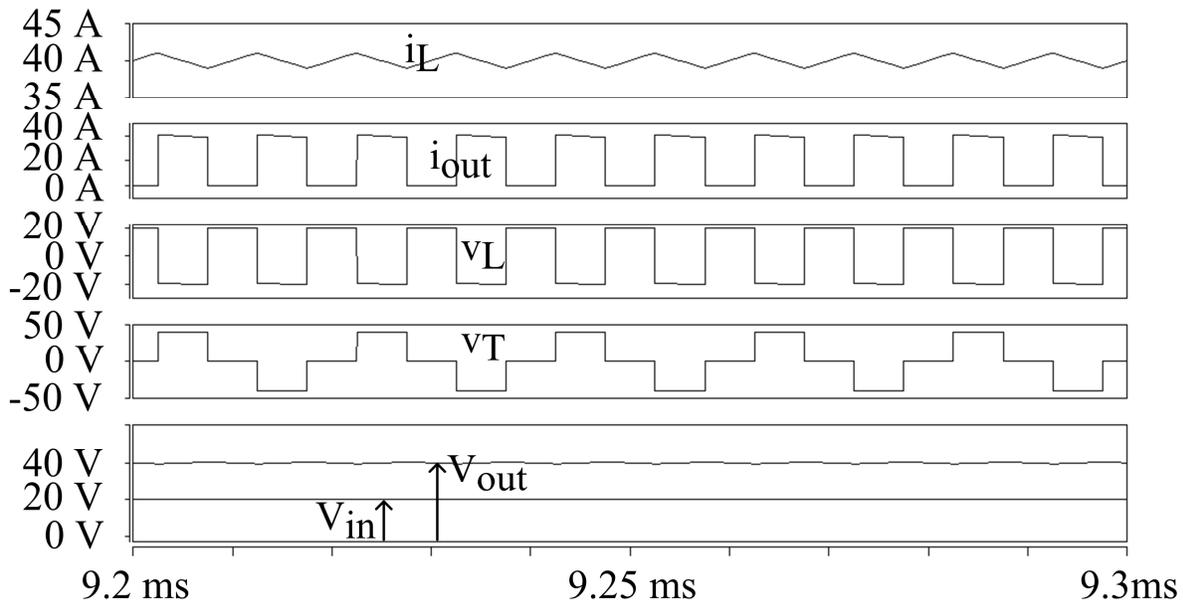


Figure 12. Simulated Full-Bridge Boost Converter

The results are exactly what one would expect given the simulation settings. Given the previously used definitions, the switching frequency was 50 kHz . The input inductance was $50\ \mu\text{H}$ while the output capacitor was set to $100\ \mu\text{F}$. Despite this rather large output capacitor, there is still noticeable ripple in the output voltage even with this poor resolution. The trickiness of avoiding major voltage overshoots on the input side plus the required large size of the output capacitor offer reasons for this converter's relative lack of use. Before passing any final judgment, however, an examination of the relative cost is necessary.

In order to obtain a decent measure of the cost of this converter, the total device stress ratio is needed. This can be derived from a quick look at the switches voltage blocking and current passing requirements. Note that, once again, the diodes have been ignored in this calculation. It is obvious that the switches must be able to handle the input current and block the transformer voltage. With this in mind, and considering the average voltages and currents, the total device stress ratio is:

$$\bar{R}_S = 4 \times \frac{V_{out}}{n} \times \frac{n \times I_{out}}{1-D} = \frac{4P_{out}}{1-D} = 4 \times 1 \text{ p.u.} \times \frac{1 \text{ p.u.}}{1-D} = \frac{4}{1-D} \text{ p.u.} \quad (2.2.5)$$

Again, the stress ratio gets increasingly larger as the boost ratio is increased. This suggests that the transformer should be used for much of the voltage boosting and the duty cycle should be adjusted to regulate it around some point. However, what about the switch utilization factor? From the above analysis, it becomes clear that:

$$\frac{P_{out}}{P_S} = \frac{1 \text{ p.u.}}{1 \text{ p.u.} \times \frac{1 \text{ p.u.}}{1-D}} = \frac{1}{\frac{1}{1-D}} = 1-D \quad (2.2.6)$$

Again, the switch utilization decreases with greater boosting. These results effectively limit the actual amount of boosting the switching action can accomplish, relegating most of the voltage multiplying to the transformer.

The two isolated full-bridge converters are quite popular, but their drawbacks for the application being discussed are numerous. First, most of the voltage boosting would have to be accomplished using the transformer's turn ratio to limit the converter cost. Second, both converters used both an inductor and a transformer, greatly increasing the size and weight of the unit. Finally, the magnetic cores that the inductor and transformer use have the tendency to see their magnetic permeability drop off with increasing temperature. In this high temperature application, the saturation of the magnetic cores becomes a real possibility. This would distort

the behavior of the magnetic components, and lead to outputs nonlinearly related to the input, making effective control very difficult. With these aspects of the isolated converters in mind, it is obvious that better topologies must be sought. In order to find them, it is necessary to consider a whole different type of dc-dc converter: the switched capacitor converter.

2.3. The Flying Capacitor DC-DC Converter

The effort to reduce or eliminate bulky magnetic components from electronic converters has taken many forms over the years. In order to achieve this goal, engineers have developed many types of circuits consisting of only switching devices and capacitors, sometimes with small inductances capable of being realized without magnetic cores. These types of circuits are often referred to as switched capacitor converter, also known as charge pumps or sometimes multilevel dc-dc converters, depending on the topology used. As a starting point in this large family of dc-dc converters, consider the so-called flying capacitor dc-dc converter discussed in [4]. Originally developed with the aim of acting as a sort of dc voltage transformer or multiplier, this converter is quite simple in its layout. The basic concept here is that the capacitors, along with the input source, charge one another, boosting the potential up to the desired output. The topology's circuit diagram can be seen in Figure 13 below. In this particular example, eight active switching devices are used, achieving an output voltage of four times the input. From here on, the following definition will be used:

$$\frac{V_{out}}{V_{in}} = N \quad (2.3.1)$$

The number N , given in (2.3.1) above, is simply a statement of the boost factor achieved in these switched capacitor converters. Since the boost factor for the converter pictured in Figure 13 is four, N is defined as being equal to four. Thus, it follows that the flying capacitor converter requires $2N$ switches in order to obtain a boost factor of N .

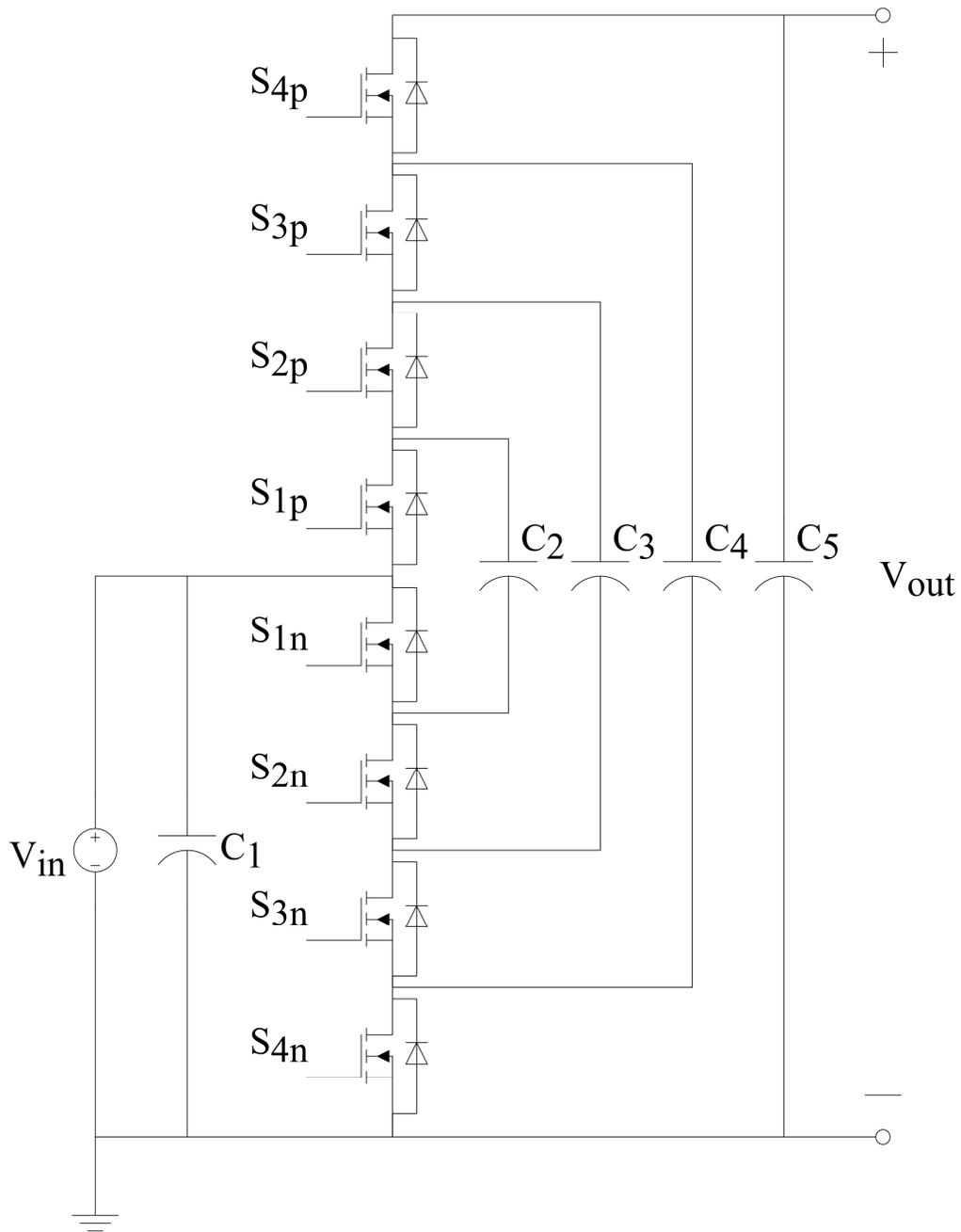


Figure 13. Flying Capacitor DC-DC Converter

Here, the capacitor C_1 is simply the input dc-bias capacitor, while capacitors C_2 through C_5 are the main power stage capacitors. In order to better understand this circuit, however, a quick run-

through of the switching states is required. Beginning with what is arbitrarily defined as switching state I, switch S_{1p} is on, while the other upper switches are off.

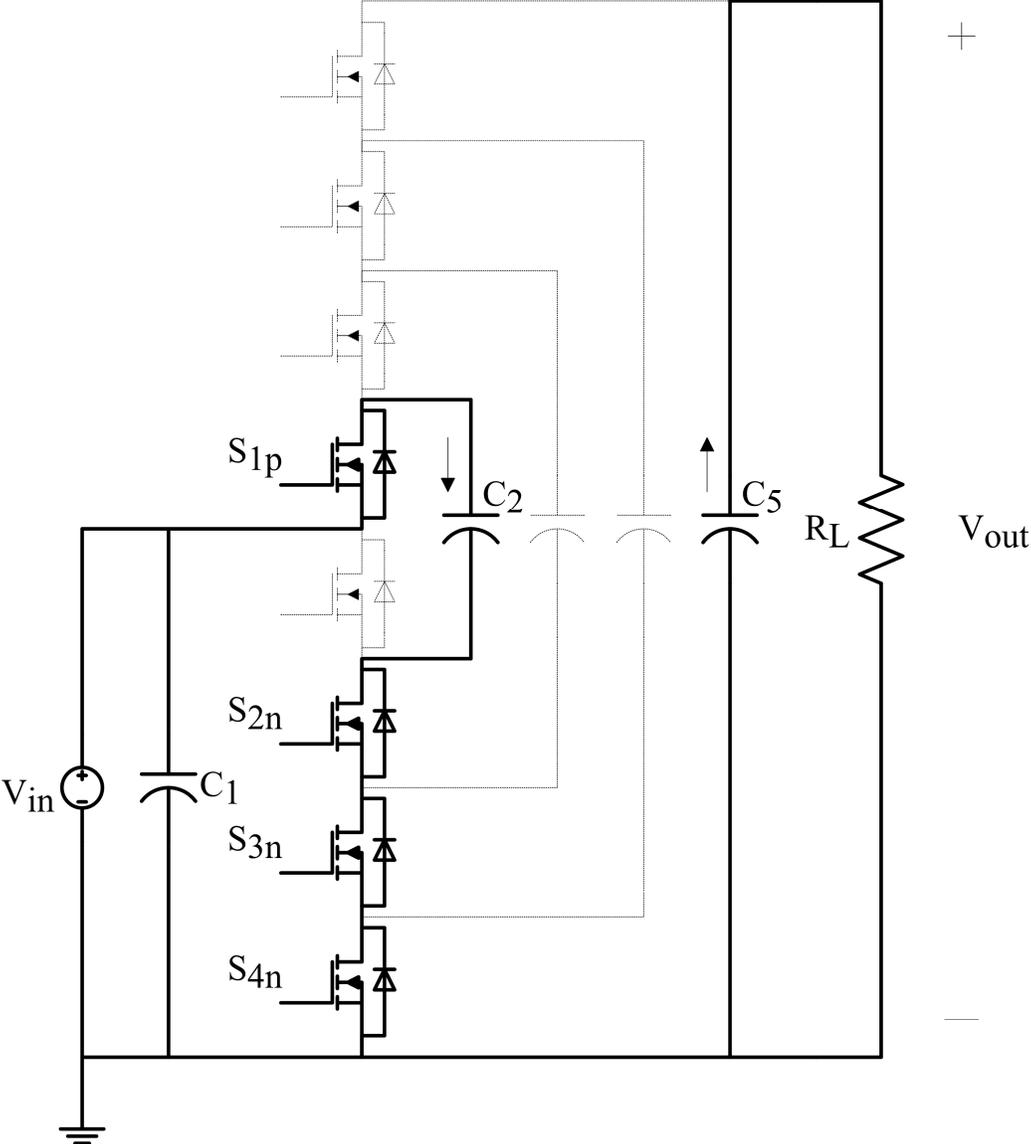


Figure 14. Flying Capacitor Switching State I

Note that the upper and lower switches are complementary; while the upper switch is on, its lower counterpart is turned off and vice versa. In this first switching state, only two of the capacitors are being used. C_2 is being charged by the source, and is brought to a voltage equal to

V_{in} . Meanwhile, the load is supplied with current from the output capacitor, C_5 . With C_2 now charged to the input voltage, the next switching state can be started.

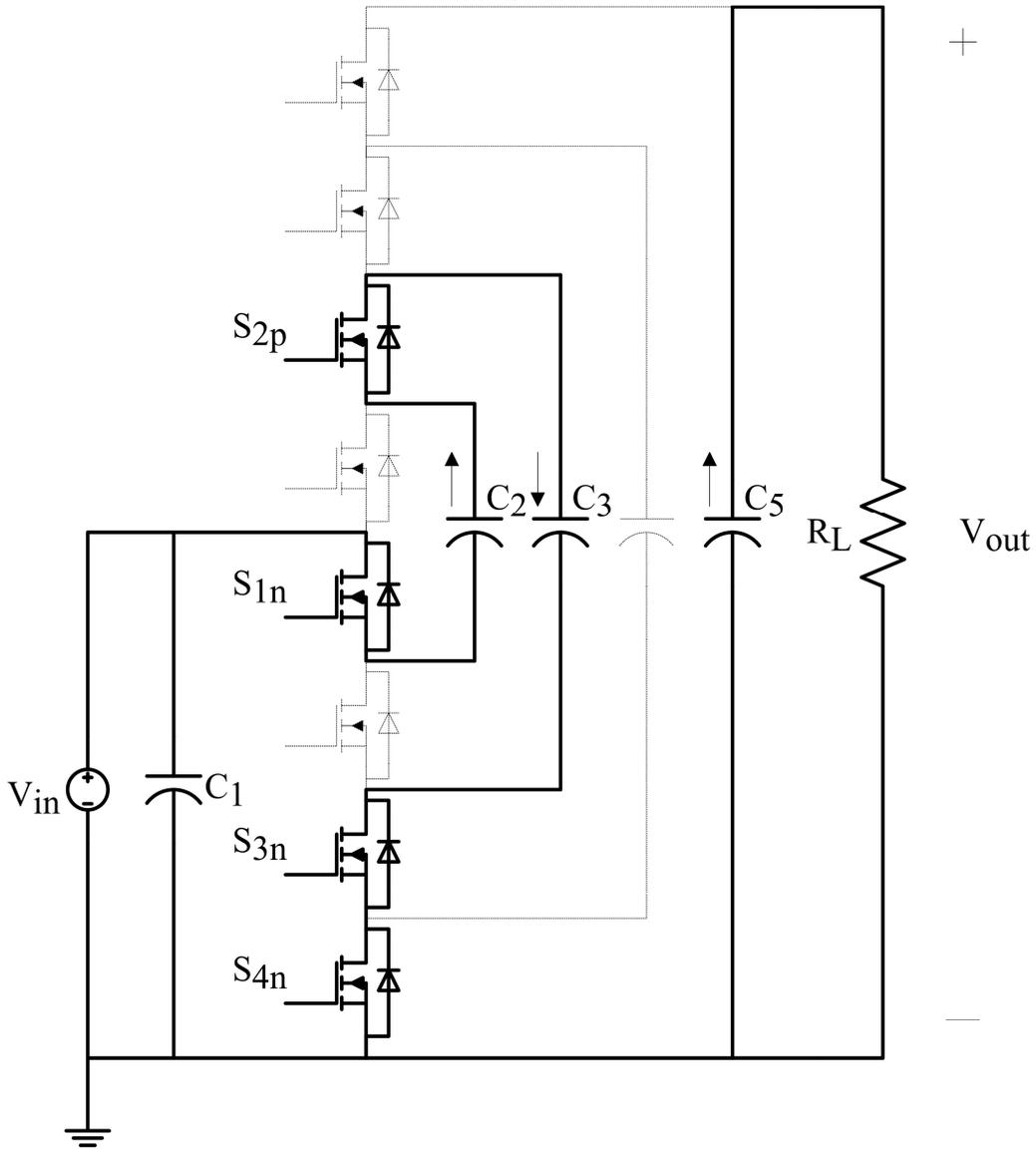


Figure 15. Flying Capacitor Switching State II

In Figure 15, now S_{2p} is the only upper switch that is on. This changes the charge loops, placing C_3 in series with both C_2 and the source. Because both the source and C_2 are at V_{in} , the

voltage that C_3 is charged up to is $2V_{in}$. Like before, the load is supplied entirely by C_5 . With this process ending, the transition to the third switching state can begin.

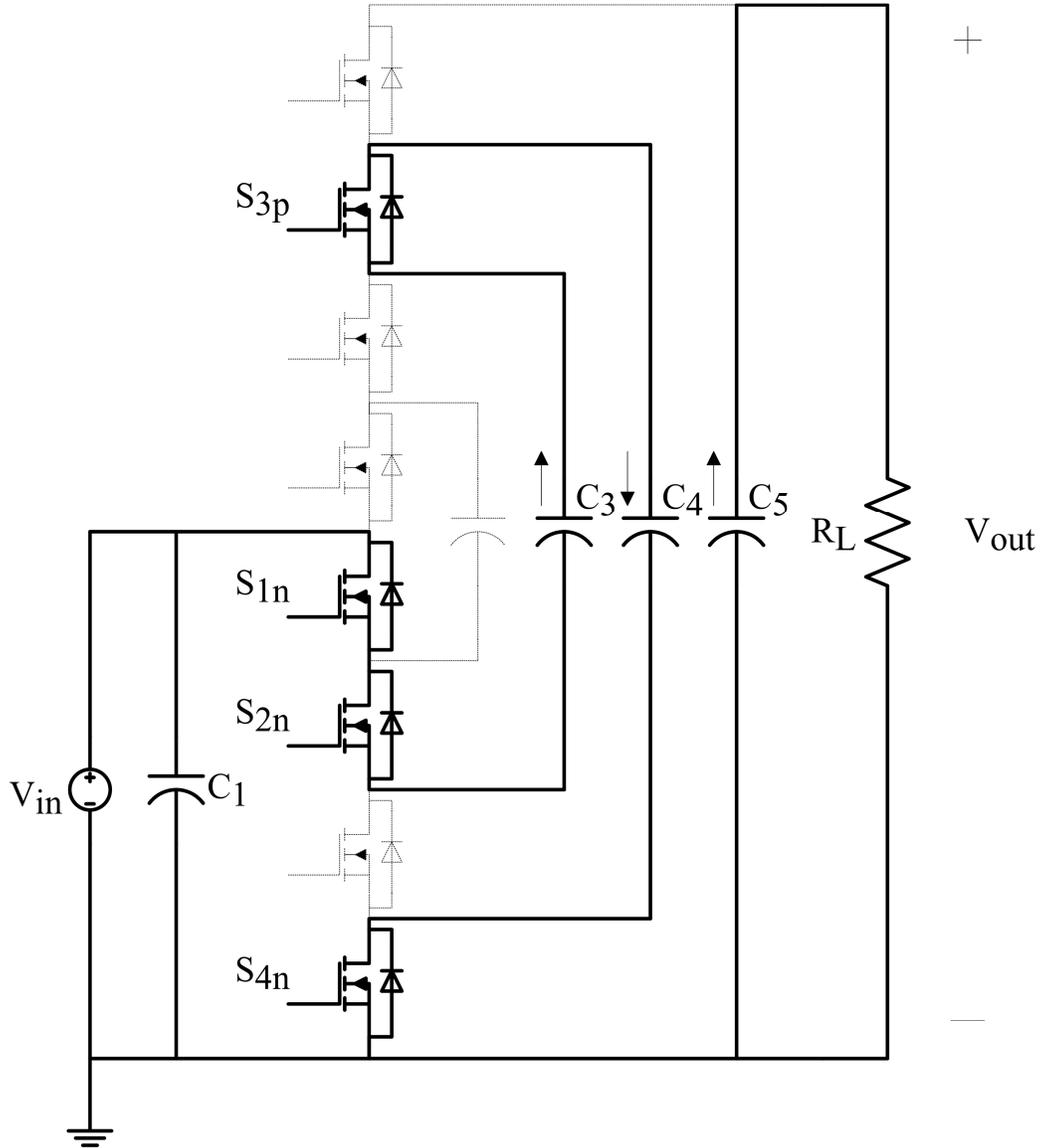


Figure 16. Flying Capacitor Switching State III

In Figure 16, switching state III can be seen. Here, yet again, the current loops have changed as S_{2p} was turned off and S_{3p} was switched on. Now, C_3 , which was charged up to $2V_{in}$, is placed in series with the source and C_4 . This action charges C_4 up to $3V_{in}$, while C_5 yet

again supplies the load current. With the end of this stage, S_{3p} is turned off and S_{4p} is turned on, entering the fourth switching state.

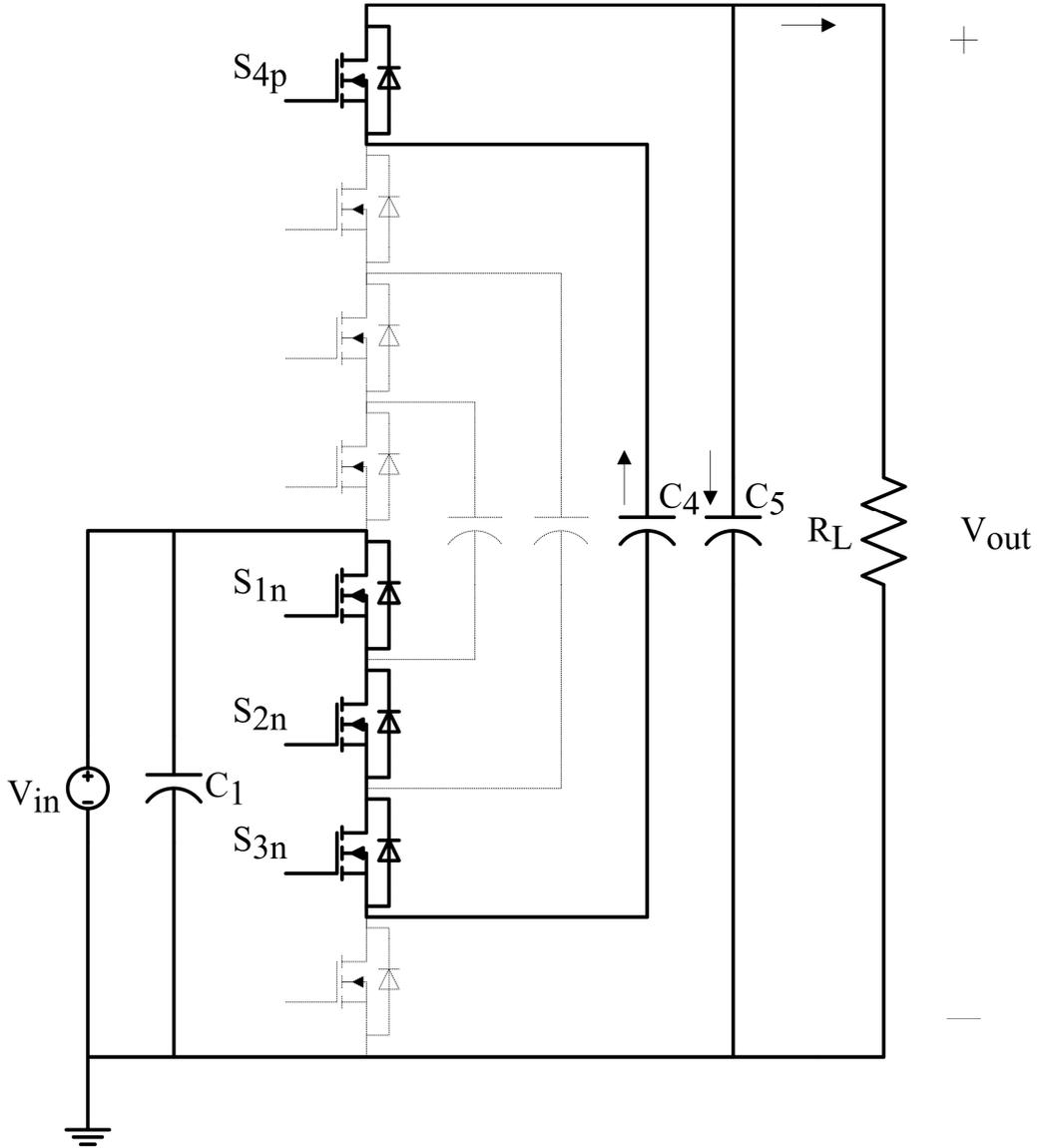


Figure 17. Flying Capacitor Switching State IV

Figure 17 shows the flying capacitor dc-dc converter's fourth switching state. This is the final switching state for this particular 4X converter, but the number of switching states is equal to N . Notice that now the source and C_4 charge C_5 to $4V_{in}$ while now helping to supply the load.

With this the flying capacitor converter's behavior can be better understood, and several points can be made concerning the topology

As was previously alluded to, this topology requires a number of switching states equal to the boost factor. This implies a control complexity that increases directly in proportion to the boost factor. Another point to note here is that these switching states divide the switching period evenly between themselves. Further increasing the flying capacitor's drawbacks is the fact that the number of switches in the charge path is also equal to the boost factor N . Since the active components are likely to provide a good deal of the resistance in this circuit, this means that the conduction losses will also increase with N . If the required boost factor is very high, this converter would likely be rather inefficient. Furthermore, the converter itself is incapable of regulating its output voltage, so the inverter would have to be used to accomplish that task. It is also important to note how the capacitors are used here, especially the output capacitor. Since it has to be able to supply the load most of the time, the output capacitance would have to be quite high, necessitating a physically large capacitor. Still, according to [5], the flying capacitor converter possesses several advantages over other similar converters. Assuming that the stage capacitors are quite large, the rate of change of the voltage across the switches would not be high, reducing the generated electromagnetic interference (EMI). Before moving on, however, several other points must be made about this converter.

Notice the basic layout of the circuit pictured in Figure 13. In essence, the only components present during one switching state end up being either resistors or capacitors, leading to the circuit's RC-circuit properties being dominant. This can be most clearly seen in the waveforms depicted in Figure 18. These show the results of a 4X flying capacitor converter

simulated in Saber with a switching frequency of 100 kHz , an input voltage of 20 V , and all the capacitors being equal to $100\text{ }\mu\text{F}$.

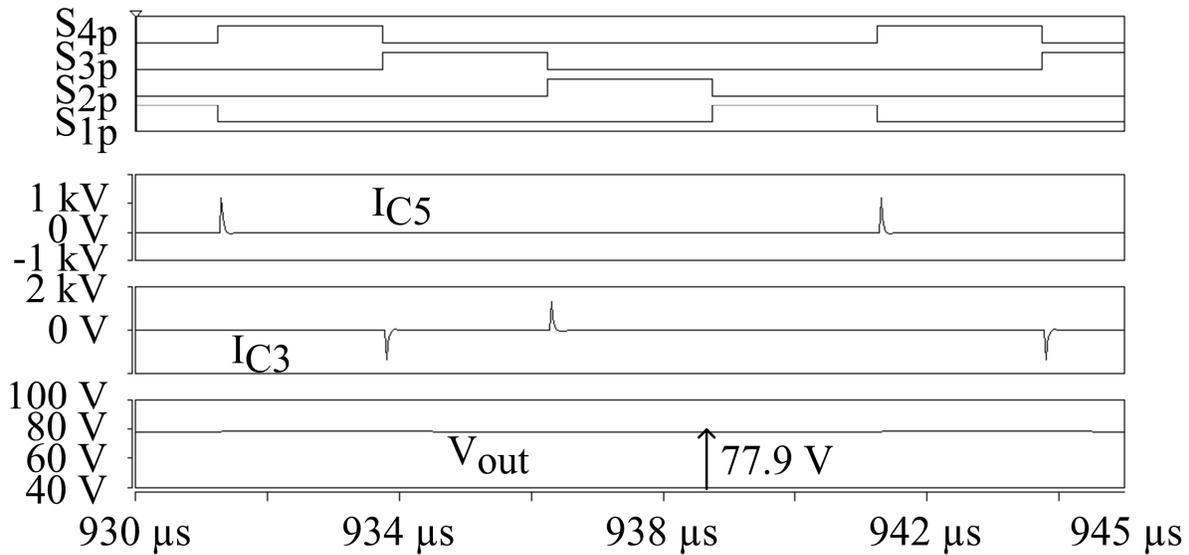


Figure 18. Simulated Flying Capacitor DC-DC Converter Waveforms

The output voltage, V_{out} , averages to around 77.9 V , which is only slightly less than the predicted 80 V . The output power was approximately 506 W , and the load resistor had a value of $12\text{ }\Omega$. Note the spiked form of the current; that is caused by the RC time constant being quite low, as this simulation had unreasonably low values for the device resistances. Notice that C_5 only gets one spike of charge each switching cycle, and then it must supply the load with current for the remainder of the switching period. Although impossible to see due to the scale, the current in C_5 is negative for most of the switching period. Consider what this means, on average, for the switches. For three-fourths of the switching period, C_5 supplies I_{out} , the load current, to the load resistor. In order to have the average current through that capacitor equal to zero, this means that switch S_{4p} must be passing $4I_{out}$ to re-charge C_5 and supply the load. Tracing this

series of events back step-by-step, the conclusion that each switch handles I_{in} on average can be reached. Furthermore, a quick glance at Figure 13 reveals that each switch must be able to block the input voltage. Assuming that the system is lossless, and the output power is 1 p.u., it follows that:

$$\bar{R}_S = 2N \times V_{in} \times I_{in} = 2N \times P_{out} = 2N \text{ p.u.} \quad (2.3.2)$$

The total device stress ratio is directly related to the boost factor N . This implies that the cost of the flying capacitor converter would increase quickly. Fortunately, the switch utilization factor is quite good:

$$\frac{P_{out}}{P_S} = \frac{1 \text{ p.u.}}{V_{in} \times I_{in}} = \frac{1 \text{ p.u.}}{1 \text{ p.u.}} = 1 \quad (2.3.3)$$

It is clear that the fixed duty cycle comes in handy in (2.3.3). This seems as good a time as any to introduce the topic of losses in switched capacitor converters, although the subject will not be brought up again until later.

In a switched capacitor dc-dc converter, it can generally be assumed that losses can be broken down in four components: gate drive loss, capacitor charging loss, conduction loss, and switching loss. In regards to the gate drive loss, it can be assumed to be negligible in most cases, so it will be ignored for now. Like in other topologies, the conduction loss refers to the losses in components while they are conducting current, and these losses can be caused either by resistances or by voltage drops. Likewise, the switching losses are caused by the switching devices while they transition from the on-state to the off-state and vice versa; for a short period during these transitions, both the voltage across and the current through these devices are non-zero, resulting in losses that are dependent on the switching frequency. However, the capacitor charging loss is something different [6]. During each switching state, two capacitors with

different voltages are put into series, often with the source. In [6], the case where two capacitors with a voltage difference of ΔV are connected together is used to illustrate the phenomenon. In this loop, the only resistances realistically included would be the capacitors' ESR, the MOSFET on-resistances and the resistance of the traces or wires. The result of the calculations can be seen in (2.3.5) below.

$$M = \left(\frac{\frac{T_{on}}{R_{loop} \cdot C_{loop}}}{1+e} \right) \left(\frac{T_{on}}{R_{loop} \cdot C_{loop}} \right) \quad (2.3.4)$$

$$P_{chg} \approx \frac{(C_A + C_B) P_{CA-CB}^2}{2 \cdot C_A \cdot C_B \cdot V^2 \cdot f_s} \cdot M \quad (2.3.5)$$

The terms in the previous two equations are defined as follows: R_{loop} is the total resistance in the loop, C_{loop} is the total capacitance in the loop (equal to $C_A C_B / (C_A + C_B)$), C_A and C_B are the two capacitors in question, T_{on} is the time in this switching state, f_s is the switching frequency, P_{CA-CB} is the power transferred from the capacitor with the higher voltage to the other, and V is the voltage both capacitors would be at without the voltage difference. (2.3.5) gives a good idea of how the losses from charging the capacitors behaves. If the converter in question is a flying capacitor circuit with a boost factor of N , then T_{on} equals $I/(N f_s)$. If the RC time constant τ , which equals $R_{loop} C_{loop}$, is much less than the on time, T_{on} , then M from (2.3.4) goes to unity. In that case, the effect of the switching frequency on (2.3.5) is quite clear; a higher switching frequency should reduce the voltage ripple and thus the charging loss. Likewise, larger

capacitances can reduce the charging loss. However, the situation becomes muddled with the addition of M , which is frequency dependent. Therefore, when designing circuits of this type, care should be given when deciding on an optimum balance between the capacitor size and the switching frequency. Before continuing with other topologies, there is another use for the flying capacitor converter that may be useful.

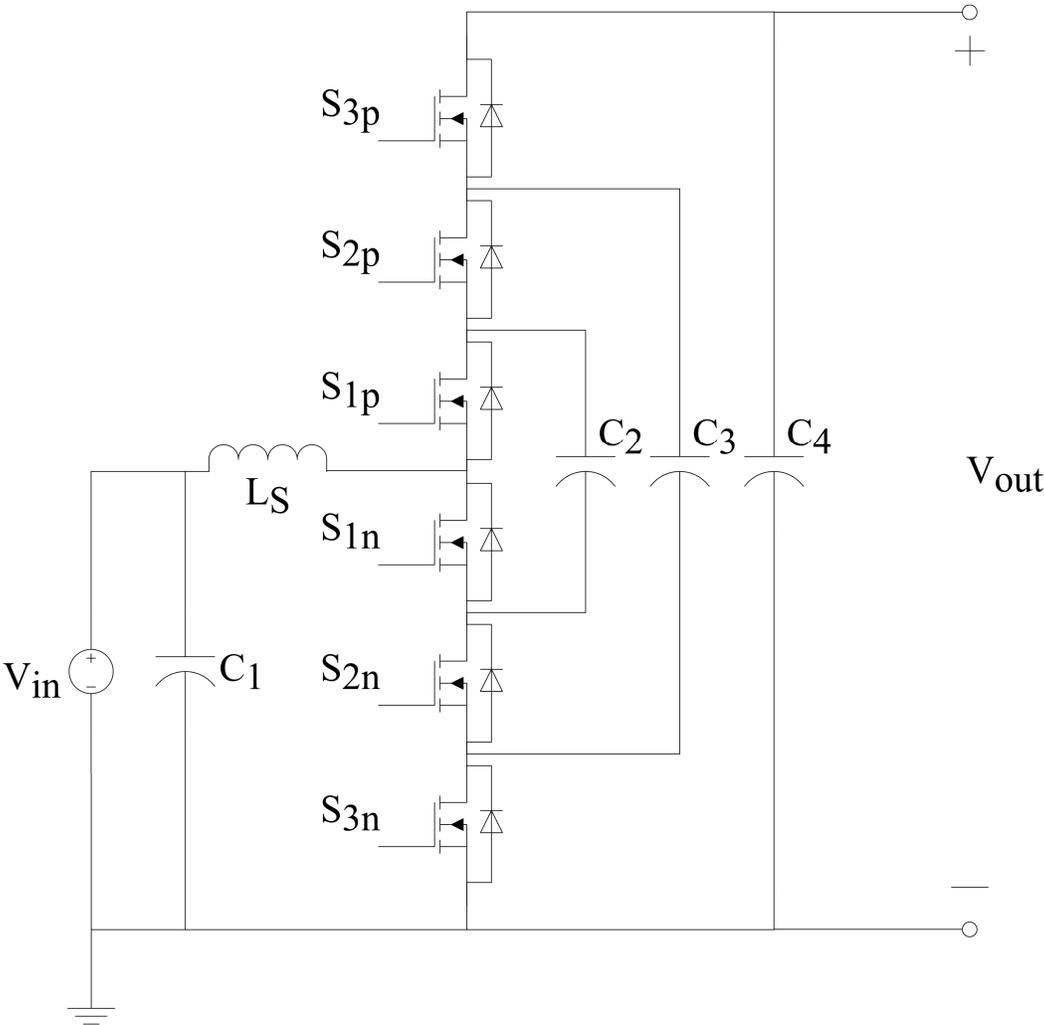


Figure 19. The 3X DC-DC Converter

One problem the flying capacitor converter may pose in a high voltage gain application like the PV system discussed earlier is that it cannot regulate its output voltage. This means that the inverter would have to be controlled to do so, and that may result in less than optimal

performance. However, a slight modification to the control of the flying capacitor dc-dc converter in its 3X configuration allows for a sort of pseudo-regulation. In [7]-[8], the 3X configuration of the flying capacitor topology was explored for its use as a switched capacitor converter with the ability to change its output voltage from one level to another. In this case, a method for shifting the output voltage from one multiple of the input to another is described, with three times the input being the maximum output voltage. To begin, observe the circuit in Figure 19 above; this is obviously no different than the 3X flying capacitor converter, except for the inclusion of some stray inductance, L_S , near the input. This inductance can be ignored for the time being. Although the structure is the same, the operation is worth considering due to its ability to adjust the output voltage. In order to obtain a better understanding of what this converter does, the switching states and the transitions between them will be explored.

The steady state operation of the 3X converter is quite similar to that of the flying capacitor converter. First, consider the 1X operating mode, where the output voltage equals the input voltage. In this situation, the converter only needs one switching state, which can be seen in Figure 20 below. This state is very straightforward, and no actual switching is needed. The voltage across C_2 , C_3 and C_4 is fixed to the input voltage, V_{in} ; thus, the output voltage is also fixed to the input voltage. Next, consider the case where two times the input voltage, or 2X, is desired.

When twice the input voltage is needed, the 3X converter can shift from either the 1X or the 3X modes to the 2X state. The 2X operation mode has two switching states that evenly divide the switching period into two halves. These two switching states are described in Figure 21 and Figure 22 below.

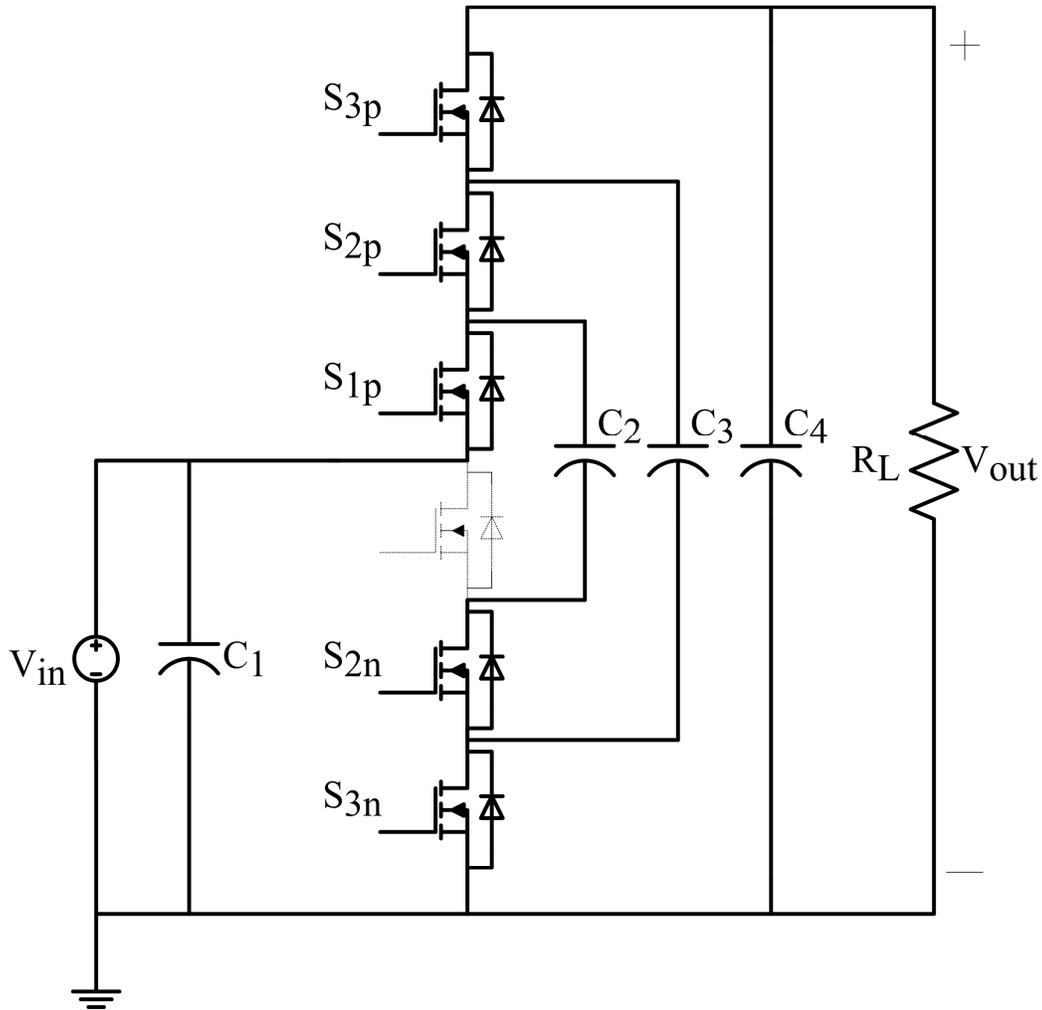


Figure 20. 3X Converter 1X Switching State

In Figure 21, the first switching state of the 2X mode is depicted. Here, S_{2p} and S_{1n} are the only two switching devices in the off state. This has the effect of placing the input voltage across C_2 , charging it up to $1V_{in}$. Meanwhile, the load is supplied entirely by C_3 and C_4 . Once half of the switching period has finished, the converter switches to its second switching state. This state is shown in Figure 22. To transition between these two states, S_{2p} and S_{1n} are turned on while S_{1p}

and S_{2n} are switched off. This has the effect of placing the source and C_2 in series, putting a voltage equal to $2V_{in}$ across the load, charging both C_3 and C_4 to that voltage.

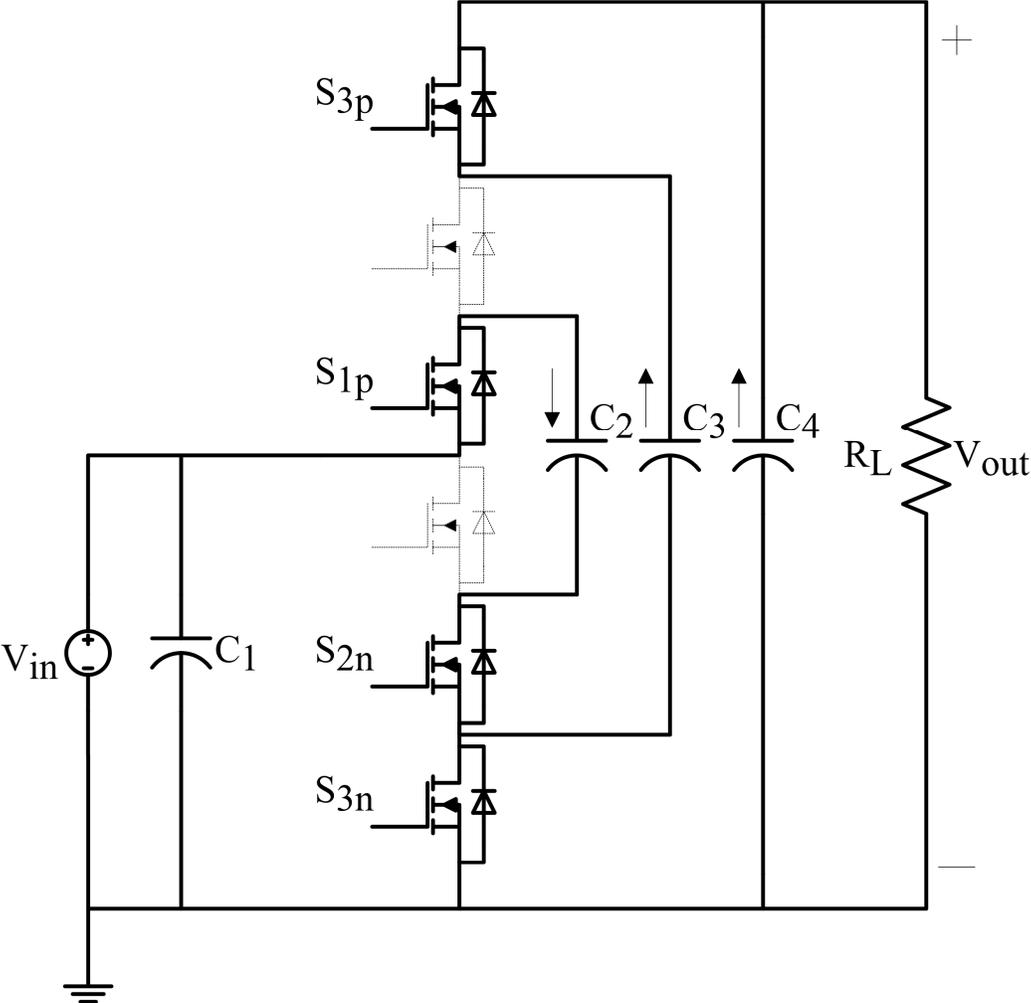


Figure 21. 3X Converter 2X Switching State I

By transitioning back and forth between these two switching states, the 3X converter is able to maintain a voltage of $2V_{in}$ across the load. However, if $3V_{in}$ is desired as an output, that can easily be accomplished.

Just like before with the flying capacitor converter, the 3X uses an identical method to produce a $3V_{in}$ output. In the 3X mode, the 3X converter divides the switching period evenly into three distinct switching states, with the active devices switching in complementary pairs.

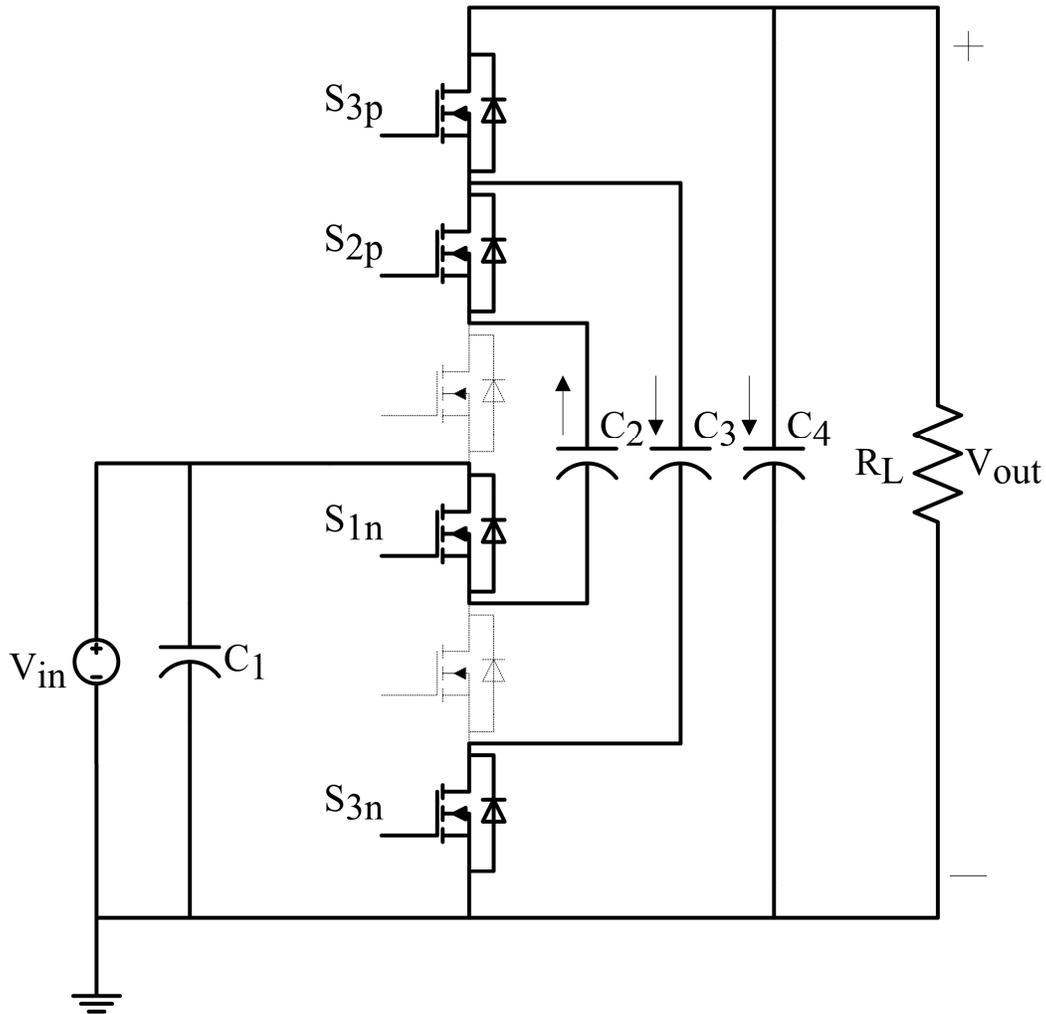


Figure 22. 3X Converter 2X Switching State II

In the first state, shown in Figure 23, S_{1p} is the only upper switch to be closed. This has the effect of charging C_2 up to $1V_{in}$ using the source. Meanwhile, C_3 is left unused, and C_4

supplies the load. The output capacitor must be large enough to supply the load current during two-thirds of the switching period, as will be shown.

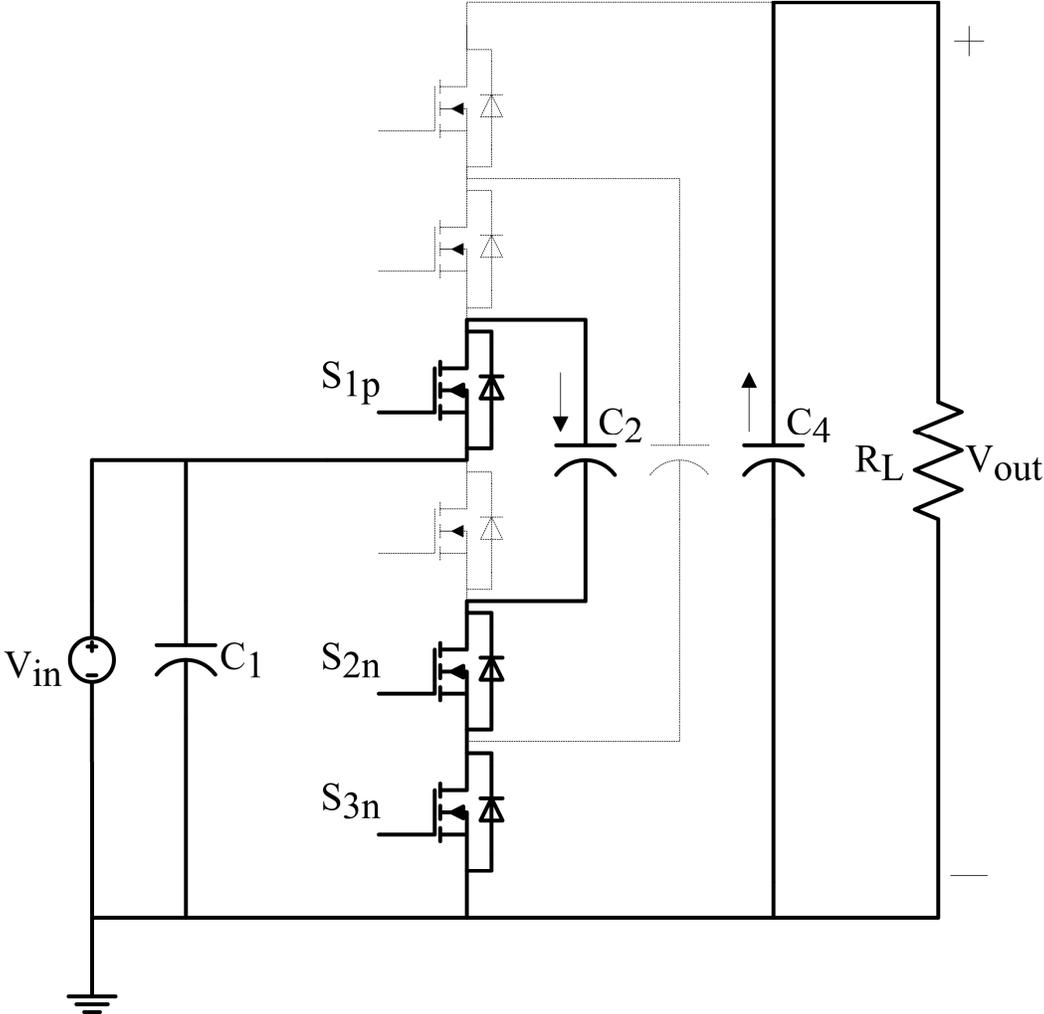


Figure 23. 3X Converter 3X Switching State I

Once this third of the switching period has finished, the 3X converter goes on to the second switching state. To do so, S_{1p} is opened and S_{2p} is turned on. The new circuit configuration can be seen in Figure 24 below. Now, the source and C_2 are in series, and they charge C_3 up to $2V_{in}$ together. Once again, for the second third of the switching period, C_4 maintains the load voltage;

this explains the need for a relatively large output capacitor if the voltage ripple on the output is to be kept manageable.

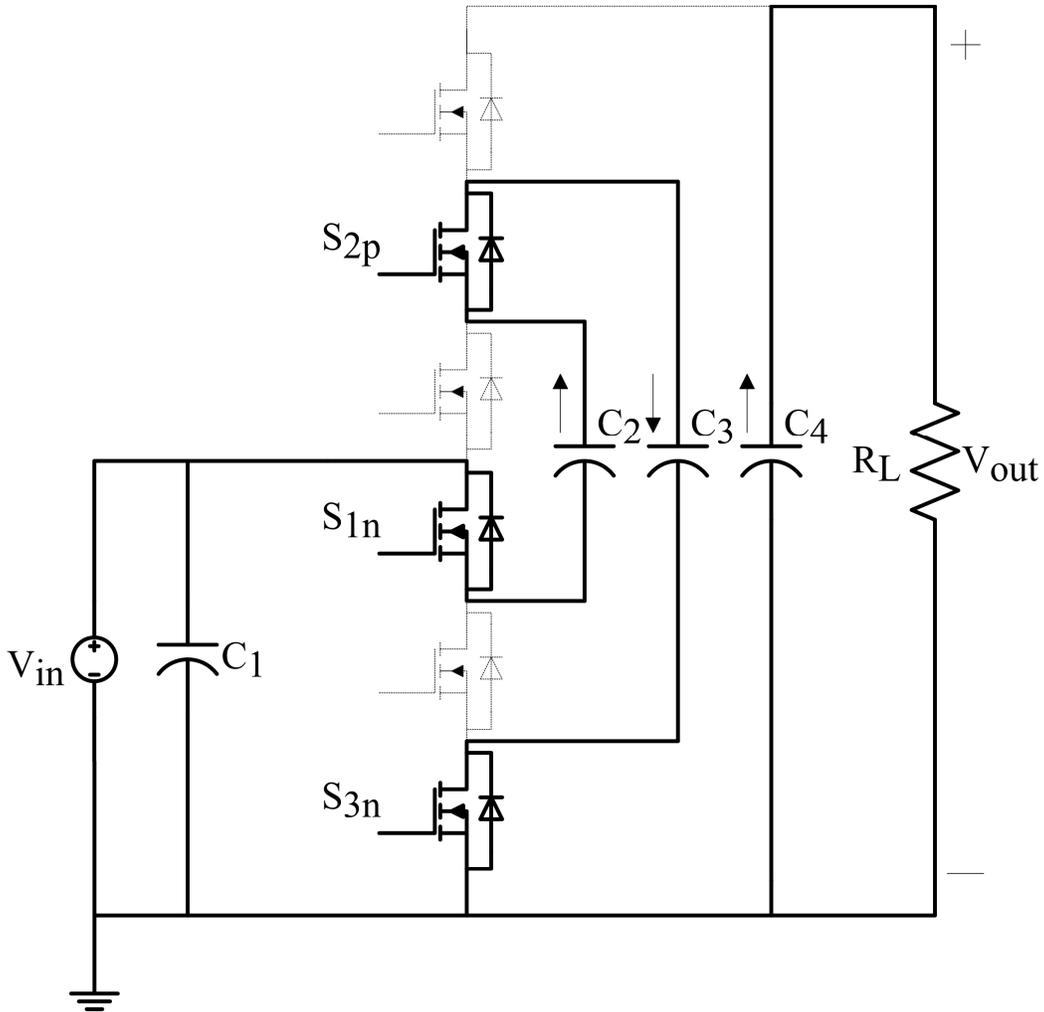


Figure 24. 3X Converter 3X Switching State II

Finally, as the second switching state reaches its conclusion, the converter enters its third switching state. This is depicted in . This time, S_{2p} is opened and S_{3p} is closed to enter the last switching state. This effectively removes C_2 from the circuit and puts C_3 in series with the source to charge C_4 . This brings to voltage across C_4 back up, maintaining the $3V_{in}$ output for another switching cycle. A quick glance back to when the general flying capacitor converter was

discussed reveals that this 3X mode of the 3X converter is identical to that of the 3X flying capacitor converter. However, the other modes are different, and they present a technique to transition between one output to another in discrete steps.

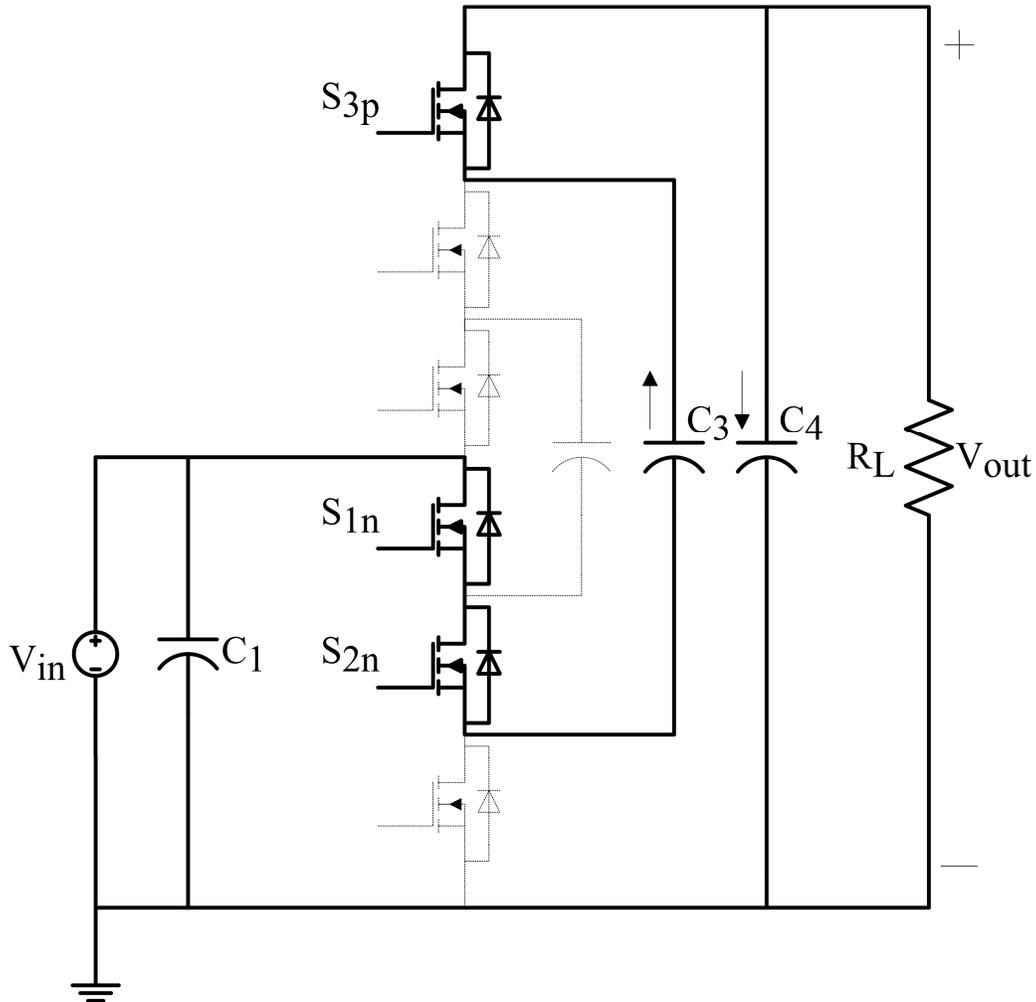


Figure 25. 3X Converter 3X Switching State III

The duty cycles in each mode are fixed, and this allows for the easy and smooth transition from one integer multiple of the input voltage to another, up to 3X. Beginning with the simplest example, consider the transition from the 1X mode to the 2X mode. In the 1X mode, all of the switches aside from S_{1n} , which is off, are being used; the upper diodes are fully utilized. In both modes, the third upper and lower switches are always on, and therefore do not

require any changes. However, the pairs of switches, (S_{1p}, S_{2n}) and (S_{2p}, S_{1n}) , are switched on and off in the 2X mode with a duty cycle equal to 50%. Therefore, a gradual shift from the fixed state of the 1X mode to the more dynamic behavior of the 2X mode is required. If, as in [7], the definition of the duty cycle D is changed to refer to the time that C_4 is charged by the series combination of C_2 and the source over the total switching period, then the transition can be easily defined. In the 1X mode, D would be zero, since C_4 is never charged by the aforementioned combination. However, in the 2X mode, this type of charging occurs for half of the period, resulting in a duty cycle of 0.5. Under this definition, simply shifting D from zero to 50% would accomplish the 1X to 2X transition. In order to show this, a simulation of the 3X circuit was performed using Saber, with a load of $12\ \Omega$ having been arbitrarily chosen. The results can be seen in Figure 26 below.

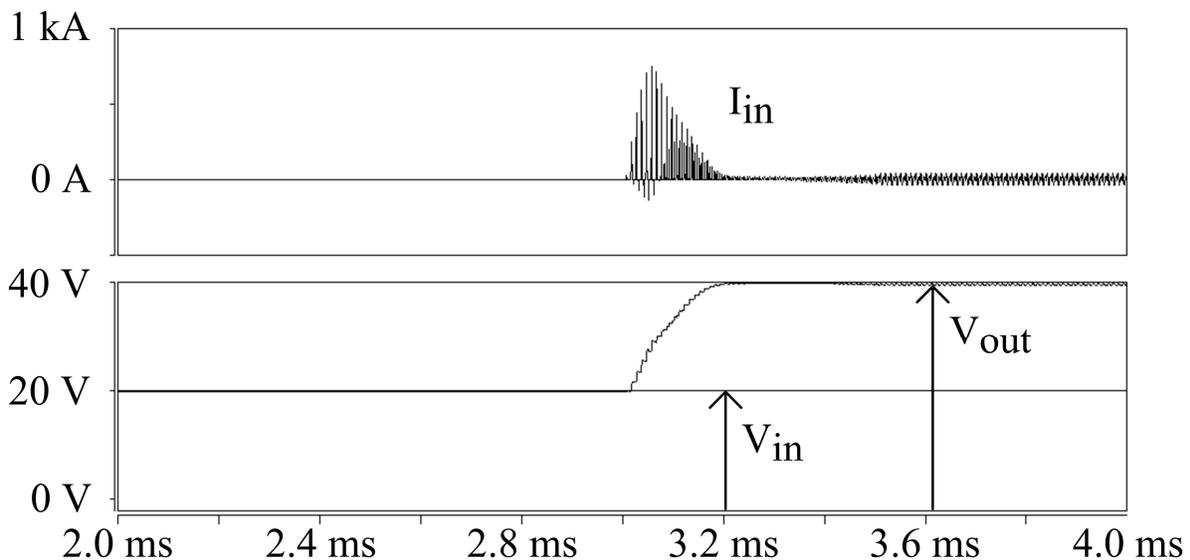


Figure 26. 1X to 2X Transition with 10 nH Stray Inductance

The simulation was performed with a switching frequency of 100 kHz , and a stray inductance of 10 nH was first implemented. Here, the effect of the stray inductance, which has been ignored up to now, can be clearly seen. With 10 nH , the inrush current during the transition has very large peaks just less than 1 kA in magnitude. Furthermore, the transition between 1X and 2X in the output voltage was quite quick. This simulation was performed once more, this time with a stray inductance of 100 nH . The results are shown in Figure 27.

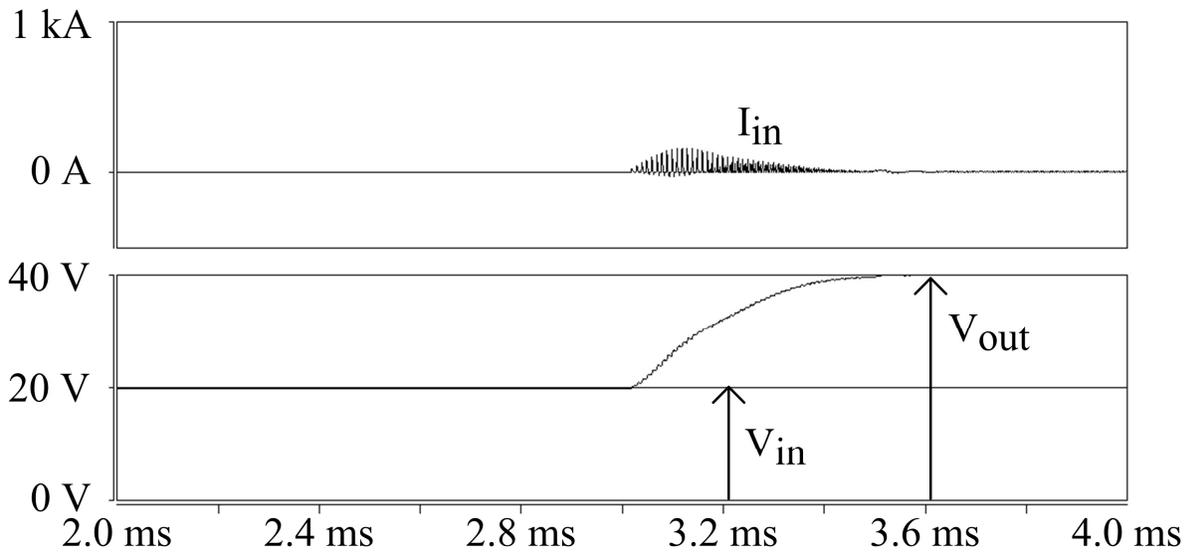


Figure 27. 1X to 2X Transition with 100 nH Stray Inductance

With the increased stray inductance, the inrush current has been greatly reduced, but the actual transition itself takes a significantly longer period of time, despite no change to the control. This illustrates one of the trade-offs in the 3X converter's design. Another thing to note is that, during the transition itself, the switch diodes are being used for a period after each active switching state, since all the active switches are off during this increasingly short period of time. Indeed, this so-called freewheeling state was used to derive the control for the transition periods. With the 1X to 2X transition covered, it might be good to briefly discuss the 2X to 3X transition as well.

In the 2X to 3X transition, the number of freewheeling states increases to three. This is simply because there are now three active states and the three freewheeling states exist between them. At this time, it may be more illustrative to adjust the definition of the duty cycle D once again. In [8], D is defined as the amount of time S_{jn} is conducting divided by the total switching period. While this differs slightly from the previously used definition, it does make the 2X to 3X transition more understandable. During the 2X state, S_{1n} and S_{2n} are complementary with a fifty percent duty cycle; meanwhile, S_{3n} is always on. In the 3X state, S_{1n} , S_{2n} and S_{3n} have duty cycles of two thirds arranged so that their upper, complementary partners divide the switching period evenly into thirds. Obviously, the transition is slightly more complex than the previously discussed one. Here, not only must S_{1n} and S_{2n} see their duty cycles go from roughly 0.5 to 0.667 , but they also need to distribute their on-times differently to accommodate the addition of S_{3n} 's on-time to the switching period. Furthermore, S_{3n} must get to a duty cycle of 0.667 from 1.0 , but this leaves two options: either transition directly or first go to 0.5 and then up to 0.667 . For the simulations performed using Saber, the latter method was employed, just like in the source papers themselves. In other words, although the transition up to the 3X duty cycle arrangement may be smooth and continuous, the start of the transition is not. This resulted in transient behavior that varied significantly from what was observed in the 1X to 2X transition simulation. The simulation was performed using the exact conditions as the previously simulated transition, using both 10 nH and 100 nH input stray inductances. The results of these

two simulations can be seen in Figure 28 and Figure 29 below. For the sake of brevity, only I_{in} ,

V_{in} and V_{out} are displayed.

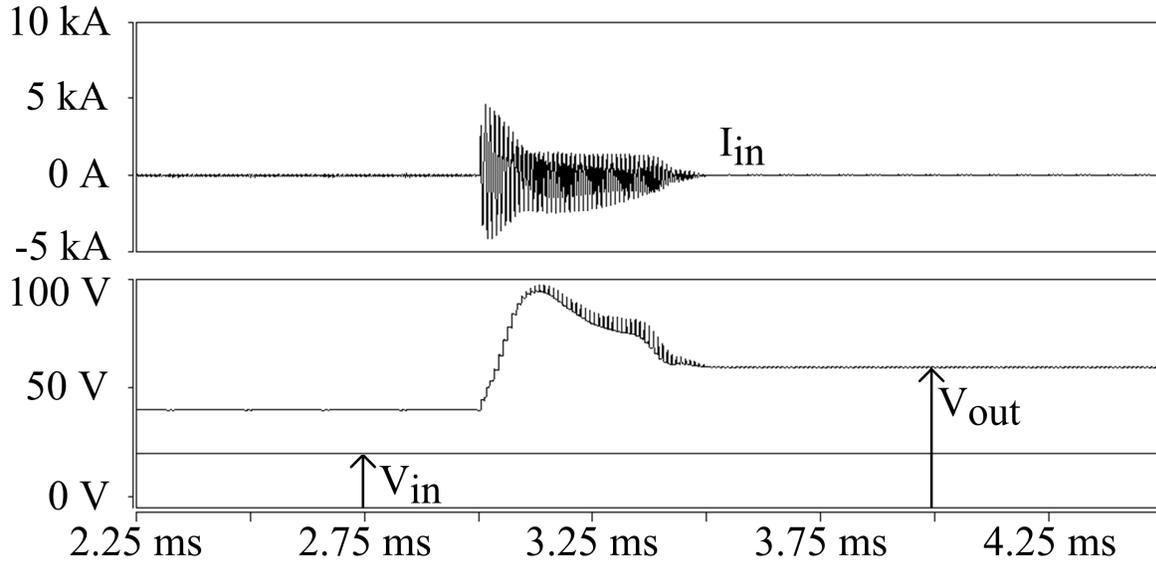


Figure 28. 2X to 3X Transition with 10 nH Stray Inductance

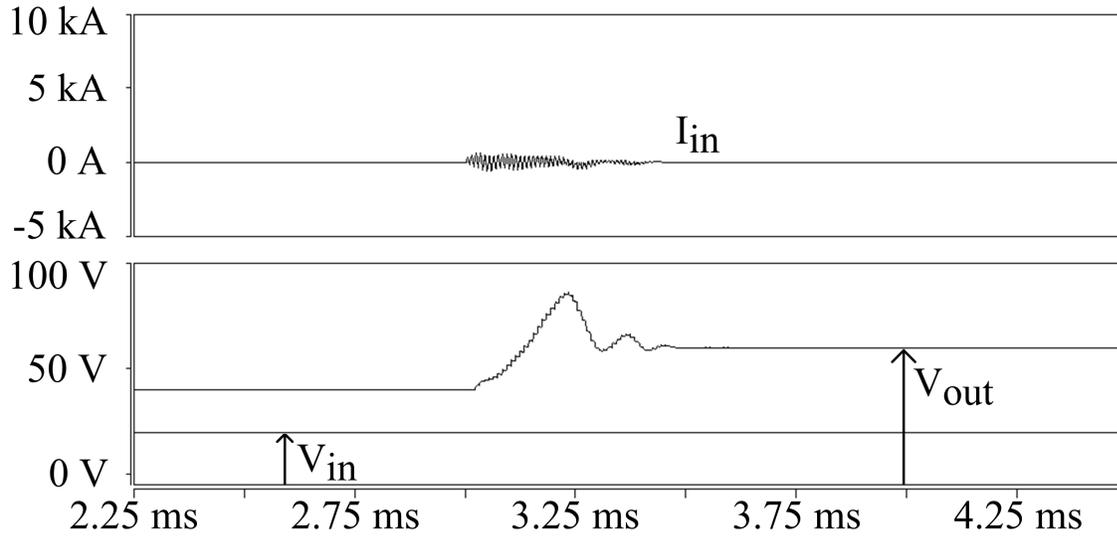


Figure 29. 2X to 3X Transition with 100 nH Stray Inductance

The step down transitions will be ignored in order to shorten this section. Notice, however, in the above figures, that the effect of the stray inductance seems to be more about dampening the voltage overshoot rather than lengthening the transition time. Both transitions finish in roughly the same time, but the 100 nH case has a significantly lower overvoltage. Nevertheless, both simulations achieved the desired result, and conclusions about the flying capacitor and 3X converters can be drawn.

In the end, the flying capacitor converter and its variant, the 3X converter, performed their voltage boost functions quite admirably. However, multiple drawbacks are already apparent. First, the larger the required boost is the more losses will be incurred from the increased number of devices in the charge pump paths. Second, the control becomes more complex with the boost ratio. Third, while this is not a big problem in the system under examination, the converters are incapable of true voltage regulation. Finally, the flying capacitor structure is not modular, meaning that a fundamental, fully functioning unit of the circuit cannot be made and then placed in series with other units to achieve whatever boost ratio is desired. Until more similar converters are discussed, these issues offer the greatest argument against the use of the flying capacitor topology in situations involving high voltage gain. Other converters have, however, been developed in order to try and overcome these drawbacks.

2.4. The Multilevel Modular Capacitor Clamped DC-DC Converter

Beginning in 2007, the multilevel modular capacitor clamped dc-dc converter (MMCCC), otherwise known as the multilevel modular switched-capacitor dc-dc converter (MMSCC), was developed and researched by engineers from two universities [9]-[14]. This topology represents an attempt to surpass the flying capacitor converter's performance, and it does in several areas. First, it should be noted that this is yet another switched-capacitor dc-dc converter. However,

unlike the flying capacitor converter, the control is very simple and the design is modular. An example of the converter can be seen in Figure 30 below, showing a four-level converter with an output equal to four times the input.

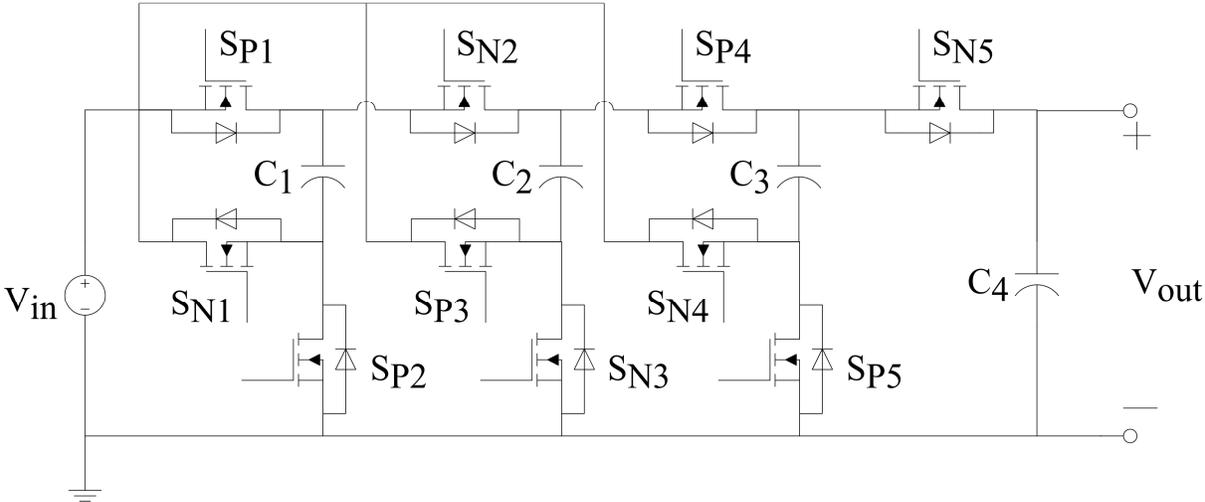


Figure 30. The MMCCC

The converter’s operation is simple enough. Using the converter from Figure 30 as an example, consider the converter as being made up of the modules shown in Figure 31.

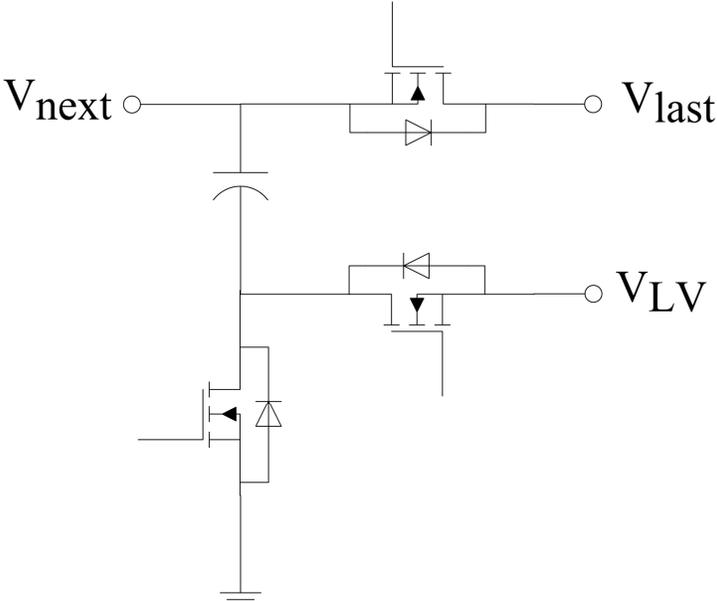


Figure 31. The MMCCC Module

Focusing on the first module, the three switches in question are SP_1 , SN_1 , and SP_2 . In each module, the switches equivalent to SP_1 and SP_2 act as a pair, and switch complementary to the equivalent of SN_1 . The following module switches in the opposite manner to the one before it. For example, when SP_1 and SP_2 are on, so is SP_3 , while SN_1 , SN_2 and SN_3 are off. This pattern repeats, creating two switching states that evenly divide the switching period between themselves. For the sake of consistency, consider the switching states shown in Figure 32 and Figure 33 below.

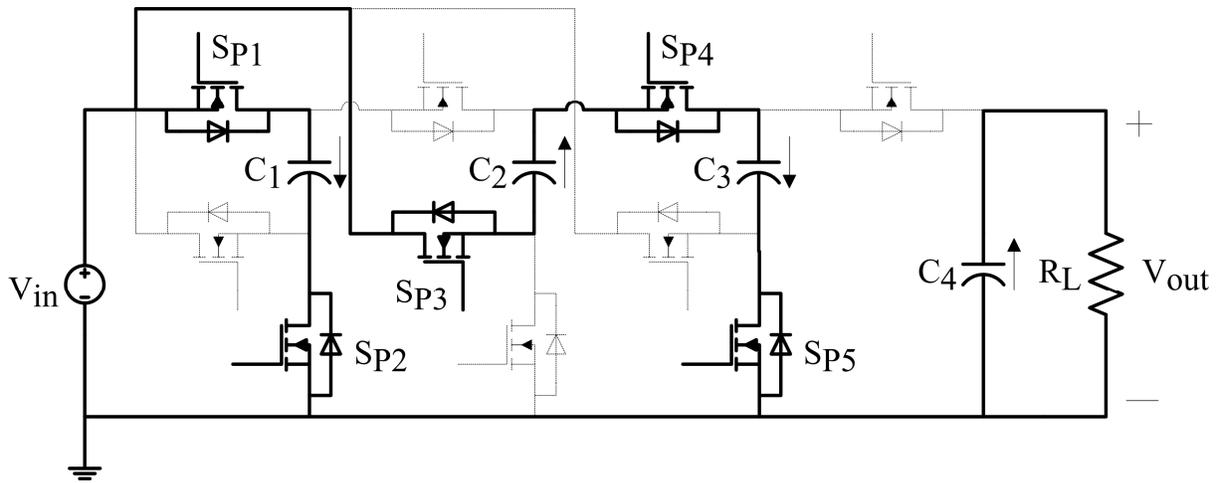


Figure 32. MMCCC Switching State I

In the above figure, switching state I has been defined as that where SP_1 and SP_2 are closed, and the other switches follow the previously mentioned rules. In the following figure, state II is defined as that where SN_1 is turned on. With this standard set, a closer examination of what is actually occurring can begin.

In Figure 32, during switching state I, SP_1 and SP_2 close in order to put the input voltage across capacitor C_1 . This charges C_1 up to $4V_{in}$. Meanwhile, SP_3 puts C_2 in series with the source in order to charge C_3 up to $3V_{in}$. This happens because, as shall be shown, the voltage of C_2 averages around $2V_{in}$. In the meantime, C_4 supplies the load current.

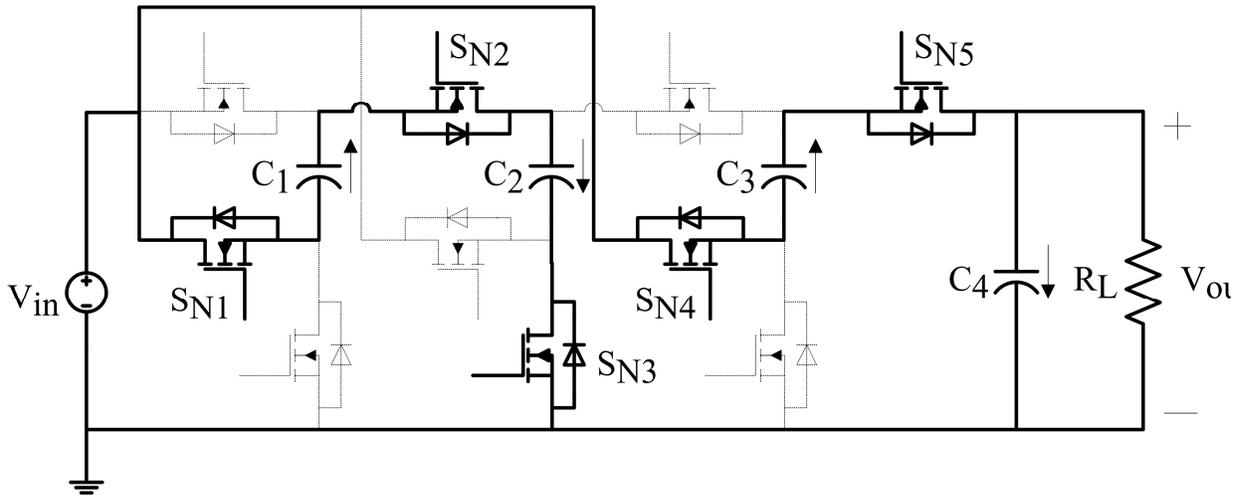


Figure 33. MMCCC Switching State II

Once that half of the switching period has completed, the converter switches to state II, detailed in Figure 33. Now, SN_1 is closed, putting C_1 in series with the source and charging C_2 up to $2V_{in}$. At the same time, SN_4 puts C_3 in series with the source to charge C_4 up to $4V_{in}$, the output voltage. These two switching states act together to give the desired output. There are some other important things in this circuit to take a closer look at, however.

As has been done to this point, one important measure of a converter's usefulness that needs to be calculated is the total device stress ratio. As always, R_S is a measure of the relative cost of the converter in terms of the silicon needed. Examining the converter more closely, it is

clear that C_4 , on average, supplies I_{out} , the load current, for half of the switching period. In order to have an average current of zero through the capacitor over the whole period, it follows that the capacitor's charging current must also average I_{out} . Furthermore, since the capacitor is not supplying the load during its charging period, the current flowing through S_{N5} must be $2I_{out}$ while it is on. Following this methodology down the line, the current each switch must be able to handle is, on average, the output current. The voltage stress of each switch, however, is bit different than before. Using the example from Figure 30 and extending it to a more general situation, it can be shown that each of the lowest switches, S_{P2} , S_{N3} , and S_{P5} , only block the input voltage, V_{in} . Likewise, S_{N1} , S_{P3} and S_{N4} block V_{in} , since the switches mentioned in the previous sentence are on while these switches are off; thus their source voltages are pulled to ground, and their drains are fixed to the input. Next, consider S_{P1} . When it blocks, its source is fixed to the input, while its drain voltage is equal to the source plus the voltage of C_1 , $2V_{in}$. Using the same reasoning with S_{N5} , it is apparent that S_{P1} and S_{N5} only have to block V_{in} . The final two switches to consider, S_{N2} and S_{P4} , are different from the rest, however. Since their circumstances are the same, consider S_{N2} . When it is off, its source sees IV_{in} . However, the drain sees $3V_{in}$ because S_{P4} is conducting, making the drain share the same node as C_3 . Thus, S_{N2} sees a drain-source voltage of $2V_{in}$ across it, as does S_{P4} . Generalizing these results, it is

clear that $N-2$ of the switches must block twice the input voltage, while the remaining $2N$ switches need only block IV_{in} . With all of this information clarified, the total device stress ratio

can now be calculated, again assuming input and output powers of $1 p.u.$

$$\begin{aligned}
\bar{R}_S &= (N-2) \times 2I_{out} \times 2V_{in} + 2N \times 2I_{out} \times V_{in} \\
\Rightarrow \bar{R}_S &= (4N-8) \times I_{out} \times \frac{V_{out}}{N} + 4NI_{out} \frac{V_{out}}{N} \\
\Rightarrow \bar{R}_S &= \frac{4NP_{out} - 8P_{out} + 4NP_{out}}{N} \\
\Rightarrow \bar{R}_S &= \left(\frac{8N-8}{N} \right) \times P_{out} = \frac{8N-8}{N} p.u.
\end{aligned} \tag{2.4.1}$$

Compared to the flying capacitor topology, it's clear that the total device stress ratio of the MMCCC is lower for any boost ratio greater than two, which practically means it would be lower for all boost applications. One drawback, however, is that the number of devices needed has increased to $3N-2$ rather than the $2N$ that the flying capacitor converter requires. Another factor to note is the switch utilization factor, of which there are two separate ones in this topology. First, consider the $2N$ switches that block IV_{in} .

$$\left(\frac{P_{out}}{P_S} \right)_{2N} = \frac{P_{out}}{\frac{2P_{out}}{N}} = \frac{N}{2} p.u. \tag{2.4.2}$$

Here it can be seen that (2.4.2) quickly climbs above 1 . Likewise, for the other $N-2$ switches:

$$\left(\frac{P_{out}}{P_S} \right)_{N-2} = \frac{P_{out}}{\frac{4P_{out}}{N}} = \frac{N}{4} p.u. \tag{2.4.3}$$

In these switched capacitor converters with fixed boost ratios and fixed duty cycles, however, the utility of the switch utilization factor is doubtful, since it is just maximized by increasing the

boost factor. Thus, for a given design, the switch utilization factor is always at its maximum. In order to better demonstrate the converter's behavior, a simulation was performed.

A simulation of the converter seen in Figure 30 was performed once again with Saber. The parameters used were a switching frequency of 100 kHz , stage capacitances of $100\text{ }\mu\text{F}$, and a load of $100\text{ }\Omega$. No dead-time was considered. Several waveforms from the simulation are illustrated in Figure 34 below.

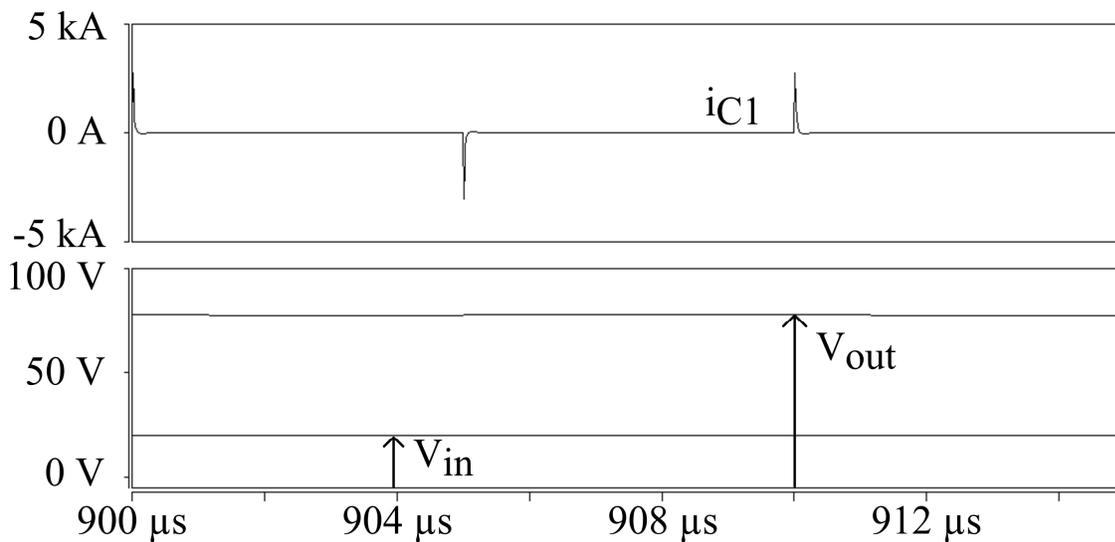


Figure 34. MMCCC Simulation Results

With an input voltage of 20 V , the output voltage is just under 80 V , meaning that the output is the expected four times the input, minus some voltage drops across switches and capacitor ESR. Notice the current for the first stage capacitor, C_1 . This shows how the current behaves like a typical RC circuit during each switching state; the current exponentially decays from an initial value determined by the voltage and circuit resistance. While the peak current is very high, this is sustained only for a very short while, and the RMS current during each switching state is much more reasonable. In fact, the RMS current that C_1 sees during switching state I in this simulation

was just under 150 A ; while not small, it is certainly much lower than the peak current. The average current was approximated as 11.9 A , which was nearly twice the output current of around 6.49 A . In the end, the simulation matches up quite well with the expectations from the previous discussion. Nevertheless, improvements to the MMCCC operation can be made.

In [12]-[14], several suggestions for improvements to the MMCCC were put forth. In [12] and [13], a method of achieving soft-switching in the MMCCC was discussed. This type of soft-switching, known as zero-current-switching (ZCS), not only reduces the switching losses to nearly zero, but it also, in theory, reduces the transient spikes of the converter, mitigating any electromagnetic noise. The downside to this type of operation, as shall be shown, is the tuning. To begin, consider the modified circuit diagram of the MMCCC shown in Figure 35 below.

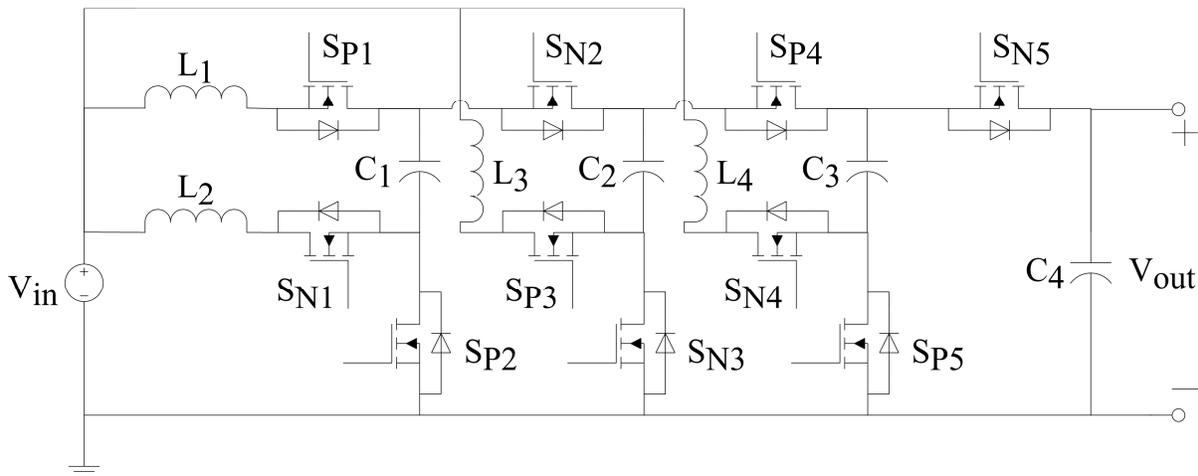


Figure 35. ZCS-MMCCC

Here it can be seen that several inductances have been introduced near the source, despite earlier discussion of avoiding magnetic components. Luckily, these inductances are just representations of input stray inductance; even printed circuit boards can have a significant amount of parasitic inductance distributed throughout their layout. In this case, the inductance being considered is likely to be the most significant. With the addition of these small inductances, however, the

circuit's behavior will change drastically. Although the output will still be $4V_{in}$, the currents flowing through the circuit will no longer follow trajectories of exponential decay. Instead, as will be shown, the currents will behave like sine waves.

The control of the ZCS-MMCCC is no different than that of its standard version. There are two switching states, each taking up half of the switching period. In order to understand what is happening, consider the two switching states.

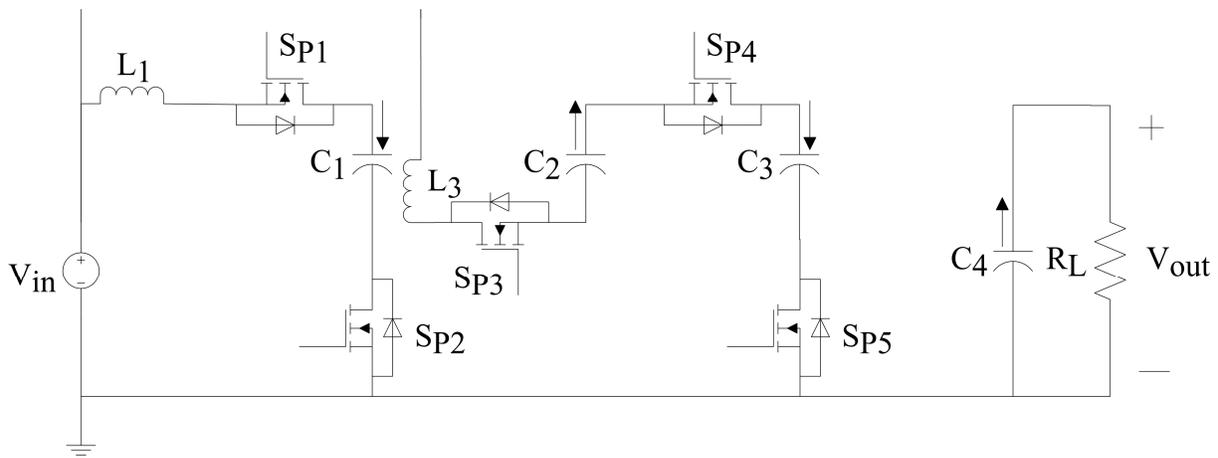


Figure 36. ZCS-MMCCC Switching State I

In Figure 36, it is clear that the converter can be broken down into three separate circuits. The inductor currents and capacitor voltages are the values desired here, and it is vital to ZCS that the inductor currents pass through zero at the moment the switching state changes. In that way, ZCS is achieved. Fortunately, a quick glance at Figure 36 shows that the circuit is mostly made up of separate series-resonant LC loops. So long as the resonant frequency of each loop is equal to the switching frequency, ZCS should be achieved. From simulations, one assumption that can be made fairly safely is that the load can be modeled as a constant current source, with a value of I_{out} , rather than a resistor. This change simplifies the solutions while not drastically affecting the accuracy. Another pair of assumptions to be made, for simplicity, are that all the capacitors

have capacitances of C and the inductances are adjusted for their accompanying components. In other words, if L_1 equals L , then L_2 and L_3 equal $2L$ and L_4 equals $2xL$, where x is some parameter to be determined. So, for the first switching state, the loop equations are:

$$V_{in} = L \frac{di_{L1}}{dt} + v_{C1} \quad (2.4.4)$$

$$i_{L1} = C \frac{dv_{C1}}{dt} \quad (2.4.5)$$

$$V_{in} = 2L \frac{di_{L3}}{dt} - v_{C2} + v_{C3} \quad (2.4.6)$$

$$i_{L3} = -C \frac{dv_{C2}}{dt} = C \frac{dv_{C3}}{dt} \quad (2.4.7)$$

$$I_{out} = -C \frac{dv_{C4}}{dt} \quad (2.4.8)$$

Here are six equations and six unknowns, but the boundary conditions must be determined from knowledge of the circuit's average values and the desired values at specific times. Furthermore, deriving these boundary conditions requires information about the second switching state of the converter. This is depicted in Figure 37 below.

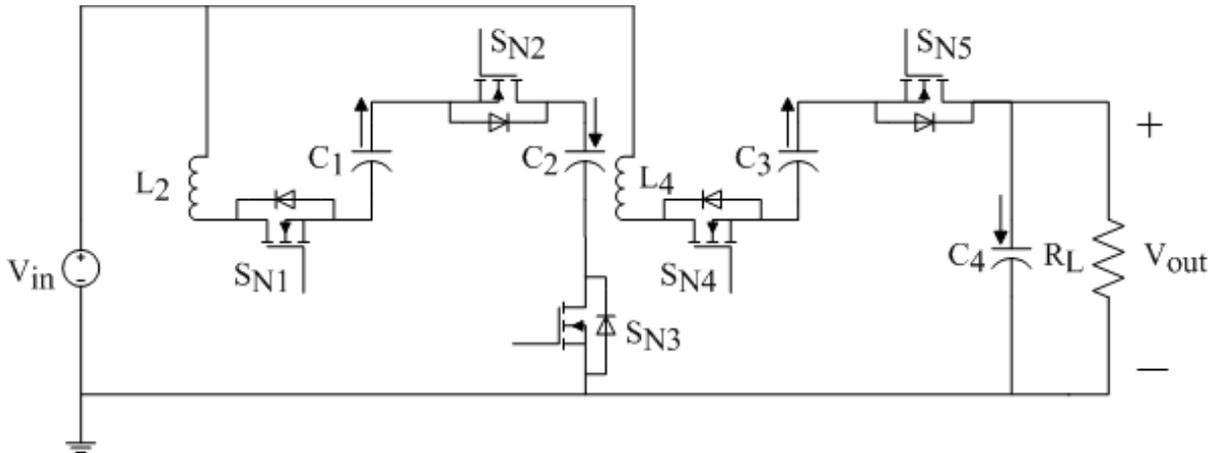


Figure 37. ZCS-MMCCC Switching State II

Once again, the same series resonant circuits are formed during the converter's second switching state. However, note the fact that the load is now connected in parallel with C_4 . This will drastically alter the behavior of the capacitor voltages in C_3 and C_4 during state II, along with the current flowing through L_4 . To begin, examine the loop equations.

$$V_{in} = 2L \frac{di_{L2}}{dt} - v_{C1} + v_{C2} \quad (2.4.9)$$

$$i_{L2} = -C \frac{dv_{C1}}{dt} = C \frac{dv_{C2}}{dt} \quad (2.4.10)$$

$$V_{in} = 2xL \frac{di_{L4}}{dt} - v_{C3} + v_{C4} \quad (2.4.11)$$

$$i_{L4} = -C \frac{dv_{C3}}{dt} \quad (2.4.12)$$

$$i_{L4} - I_{out} = C \frac{dv_{C4}}{dt} \quad (2.4.13)$$

A time shift will have to be introduced into the solutions of these equations in order for them to mesh with the equations from the previous period. In the above equations, however, one can see some deviation from the equations presented in [12]; this was done in order to obtain a better degree of accuracy when compared to simulation results. To make a long story short, the solutions for the currents and voltages in the first switching state are:

$$i_{L1}(t) = \pi I_{out} \sin(\omega t) \quad (2.4.14)$$

$$v_{C1}(t) = V_{in} - \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (2.4.15)$$

$$i_{L3}(t) = \pi I_{out} \sin(\omega t) \quad (2.4.16)$$

$$v_{C2}(t) = 2V_{in} + \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (2.4.17)$$

$$v_{C3}(t) = 3V_{in} - \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (2.4.18)$$

$$v_{C4}(t) = 4V_{in} + \frac{\pi I_{out}}{2} \sqrt{\frac{L}{C}} - \frac{I_{out}}{C} t \quad (2.4.19)$$

$$\omega = \frac{1}{\sqrt{LC}} = \frac{2\pi}{T_{sw}} \quad (2.4.20)$$

These equations describe the behavior of the circuit's capacitor voltages and inductor currents during switching state I, defined as being from $0 < t < T_{sw}/2$. Aside from (2.4.19), these equations don't differ much from those described in [12]. The differences really come out in state II.

The changes to the circuit made in switching state make several large changes to the behavior of the capacitor and inductor waveforms. To better discuss this, first examine the solutions below.

$$i_{L2}(t) = -\pi I_{out} \sin(\omega t) \quad (2.4.21)$$

$$v_{C1}(t) = V_{in} - \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (2.4.22)$$

$$v_{C2}(t) = 2V_{in} + \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (2.4.23)$$

$$i_{L4}(t) = \frac{I_{out}}{2} - \frac{I_{out}}{2} \cos\left(\frac{\omega}{\sqrt{x}} t - \frac{\pi}{\sqrt{x}}\right) + \frac{3\pi I_{out}}{4\sqrt{x}} \sin\left(\frac{\omega}{\sqrt{x}} t - \frac{\pi}{\sqrt{x}}\right) \quad (2.4.24)$$

$$v_{C3}(t) = -\frac{I_{out}}{2C} \left(t - \frac{\pi}{\omega}\right) + 3V_{in} + \frac{\pi I_{out}}{4} \sqrt{\frac{L}{C}} + \frac{3\pi I_{out}}{4} \sqrt{\frac{L}{C}} \cos\left(\frac{\omega}{\sqrt{x}} t - \frac{\pi}{\sqrt{x}}\right) + \frac{I_{out} \sqrt{x}}{2} \sqrt{\frac{L}{C}} \sin\left(\frac{\omega}{\sqrt{x}} t - \frac{\pi}{\sqrt{x}}\right) \quad (2.4.25)$$

$$v_{C4}(t) = -\frac{I_{out}}{2C} \left(t - \frac{\pi}{\omega}\right) + 4V_{in} + \frac{\pi I_{out}}{4} \sqrt{\frac{L}{C}} - \frac{3\pi I_{out}}{4} \sqrt{\frac{L}{C}} \cos\left(\frac{\omega}{\sqrt{x}}t - \frac{\pi}{\sqrt{x}}\right) - \frac{I_{out}\sqrt{x}}{2} \sqrt{\frac{L}{C}} \sin\left(\frac{\omega}{\sqrt{x}}t - \frac{\pi}{\sqrt{x}}\right) \quad (2.4.26)$$

$$x \approx 0.79821687 \quad (2.4.27)$$

These equations are, in a way, much uglier than the previously used ones, but they model the circuit's behavior much better. The parameter x , given a value in (2.4.27), was determined using (2.4.24) set to zero at $t=T_{SW}$. To give an example of what (2.4.19) and (2.4.26) might look like for some arbitrary conditions, MATLAB was used to plot an example, seen in Figure 38.

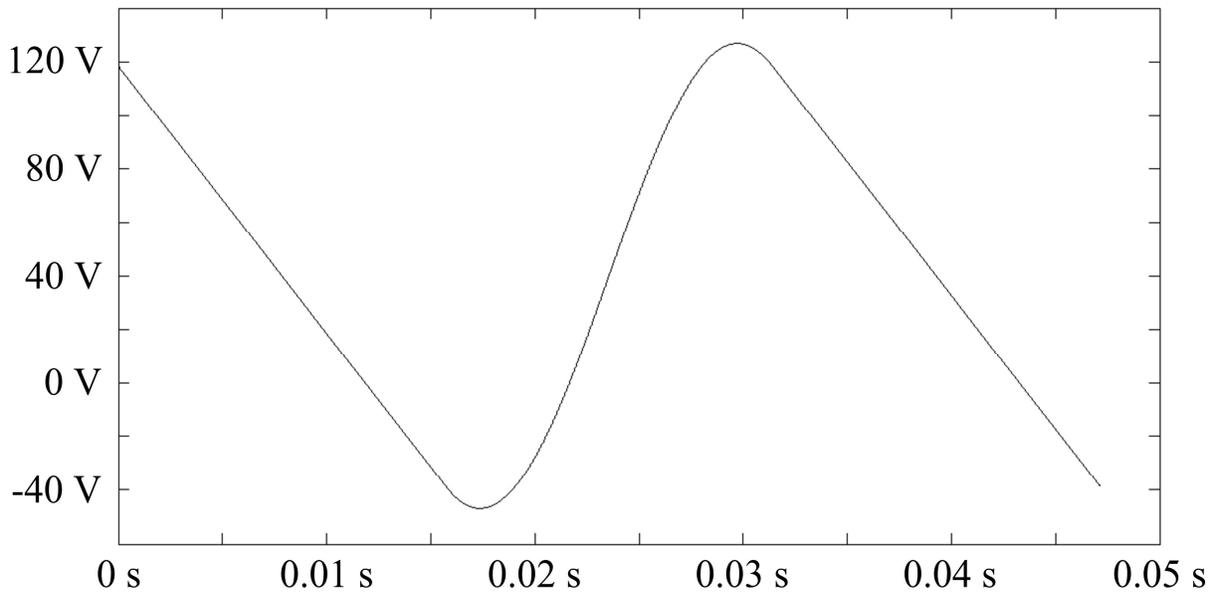


Figure 38. ZCS-MMCCC C_4 Voltage Example

Here, the general nonlinear pattern of the final capacitor's voltage can readily be seen, and a comparison between the results from the equations and a simulation can now be drawn.

For the simulation of the ZCS-MMCCC, Saber was again used with a switching frequency of 100 kHz , a standard capacitance C of $100 \mu\text{F}$, a base inductance L of 25.33 nH , and

a load of 100Ω . Running the simulation until the initial transient behavior has died off, the steady state results can be seen in Figure 39 and Figure 40 below.

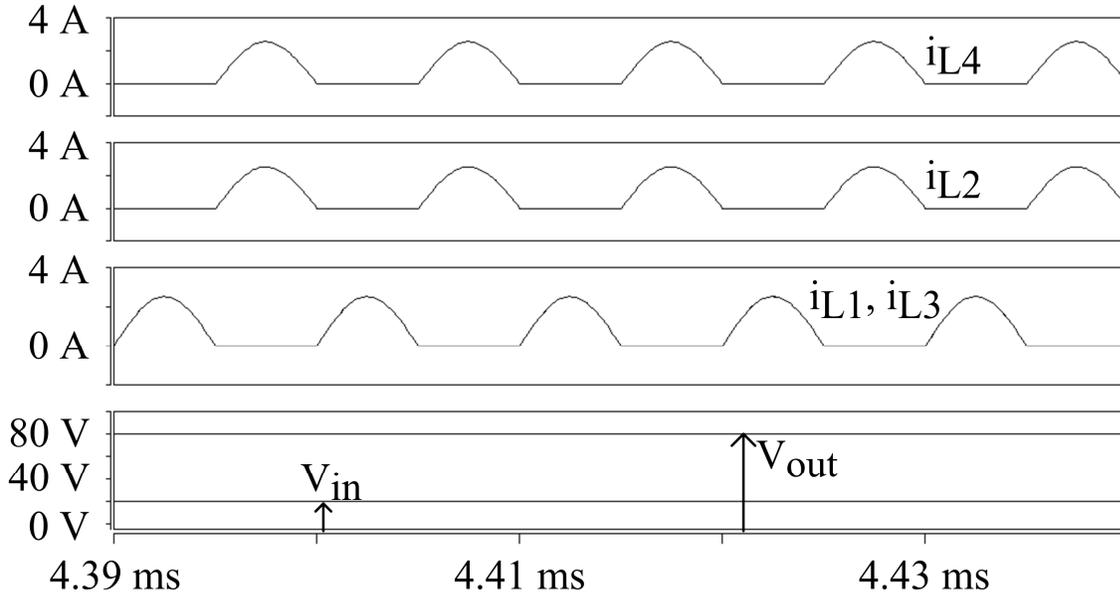


Figure 39. ZCS-MMCCC Simulation Output Voltage and Inductor Currents

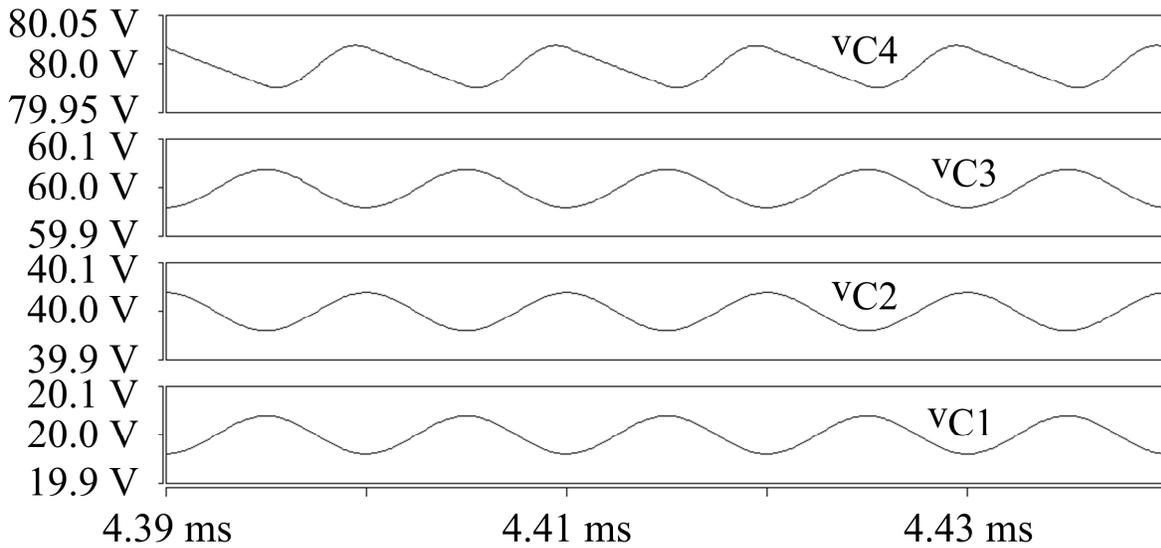


Figure 40. ZCS-MMCCC Simulation Capacitor Voltages

These simulations not only verify the veracity of the previous analysis, but also confirm the zero-current-switching of the converter. While quite convenient in simulation and on paper, actually

implementing this design can be tricky. Since the calculation of stray inductance is difficult and is highly dependent on the geometry of the physical design, it is helpful to consider the use of long wires capable of acting as air-core inductors when tuning this type of converter. Another improvement on top of this one was suggested, however.

In [14] it was noted that the ZCS-MMCCC does have an issue regarding its input current. Normally, the converter has significant ripple in its input current, to the extent that it becomes discontinuous. This also means that any input capacitor used would have to be quite large and would suffer from significant losses. Using Saber once again, an example of this input current can be seen in Figure 41 below.

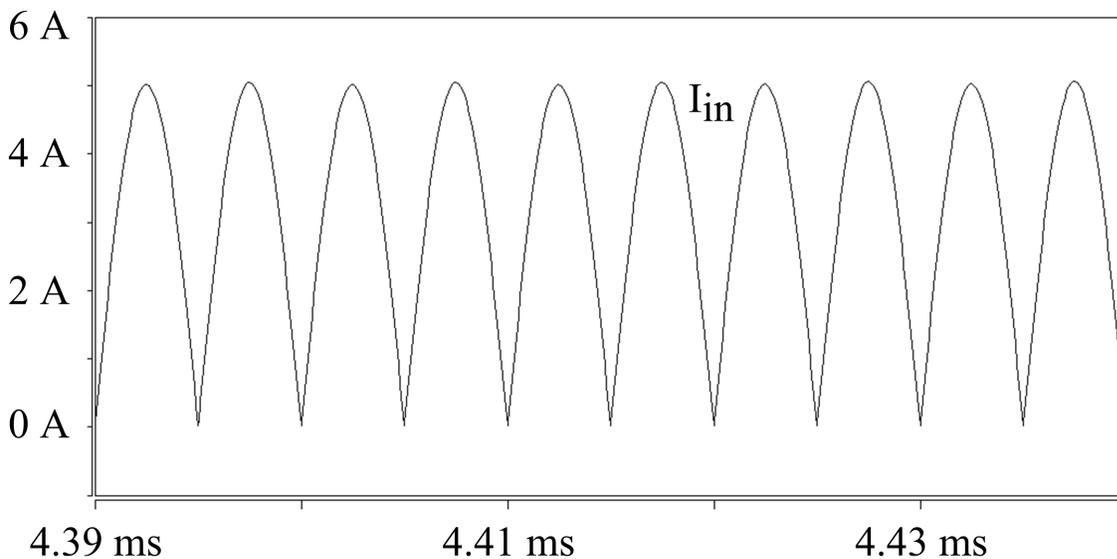


Figure 41. ZCS-MMCCC Input Current

This amount of ripple is undesirable due the burden it places on the input capacitor. In order to mitigate this, along with decreasing output voltage ripple, [14] introduced the concept of using multiple ZCS-MMCCC converters in parallel with one source and one load. By incorporating a phase shift in the control of each individual converter such that the switching signals of each are staggered, the input current and output voltage can be reduced. For example, such a converter

that employed four separate converters would use a 90° phase shift in their control; in other words, the switching signals of each converter are 90° out of phase from each other. In order to quickly illustrate this point, Saber was used to simulate and plot this situation.

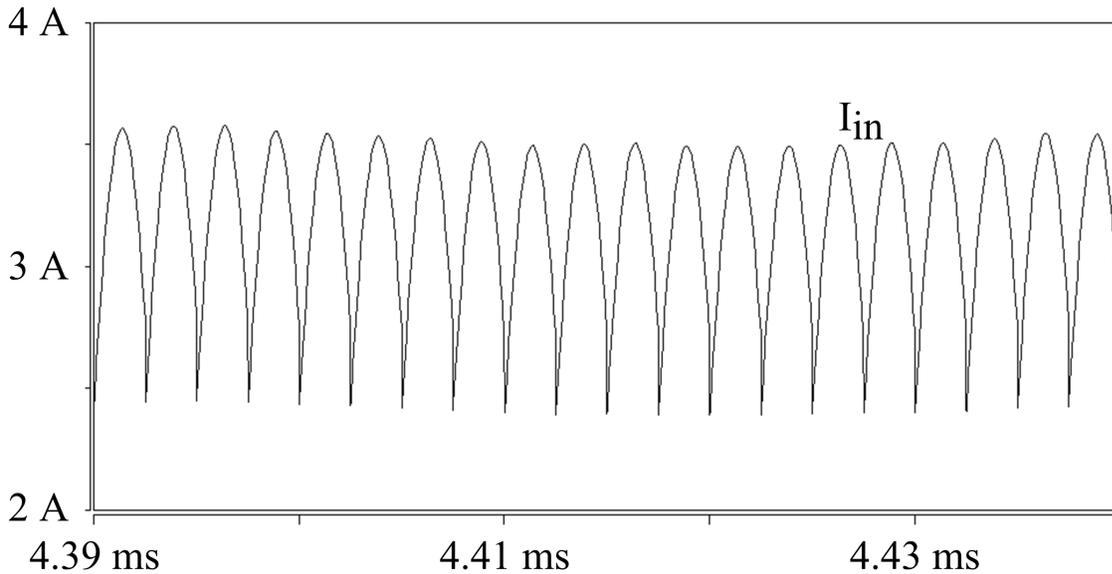


Figure 42. ZCS-MMCCC 4-Phase Input Current

In Figure 42 above, it is clear to see the effect of using four parallel ZCS-MMCCC converters with the appropriate phase shifts. Rather than having discontinuous current with a peak-to-peak value of nearly 5 A, the input current is now continuous with a peak-to-peak value of just over one ampere. This is with the same load, source and switching frequency. While this does divide the load among the converters, it does increase the actual number of components needed.

In the end, however, the MMCCC family of designs still has its drawbacks. It requires a large number of switches for a given voltage boost, and $N-2$ of the switches need to handle higher voltage stresses. Nevertheless, it has many advantages over the flying capacitor converter. With this in mind, it was desired to create a converter capable of meeting the requirements of the overall system while combining the benefits of both previous switched capacitor designs.

3. The NX DC-DC Converter

At this point it would be best to remember the situation at hand. The system being considered consists of a PV panel, followed by a dc-dc converter and an inverter. Due to the desire to integrate the power electronics onto the panel itself, it is desired to reduce the size and weight of the total package and it has to be able to handle the high temperatures experienced on a PV panel. Because of this, components requiring magnetic cores are out of the question, since they are bulky and become unstable at high temperatures. Focusing on the dc-dc converter, there are several features that would be advantageous to have. A high voltage gain must be achievable while keeping the component count and control complexity down. Furthermore, device stresses and the number of devices in each current loop should be minimized. While the flying capacitor converter and the MMCCC both have aspects that meet a few of these goals, neither meets them all. With that in mind, a new topology called the NX dc-dc converter was developed, designed and tested.

3.1. NX DC-DC Converter Details

The NX dc-dc converter, like the last two converters discussed, is a type of switched capacitor or multilevel converter [18]. It uses no magnetic components, and the operation relies on the transfer of charge from one capacitor to another, stepping up the voltage along the way. This makes for a simple circuit consisting just of capacitors and semiconductors, in theory. To begin introducing the new design more in-depth, consider the 6X schematic shown in Figure 43. In many ways, this circuit resembles the flying capacitor circuit and the MMCCC, but it has several major differences. The first thing that may come to mind while observing the schematic in Figure 43 is that the converter does appear to be modular. In truth, a simple re-configuration of the drawing itself, without any changes to the circuit, shows this to be false.

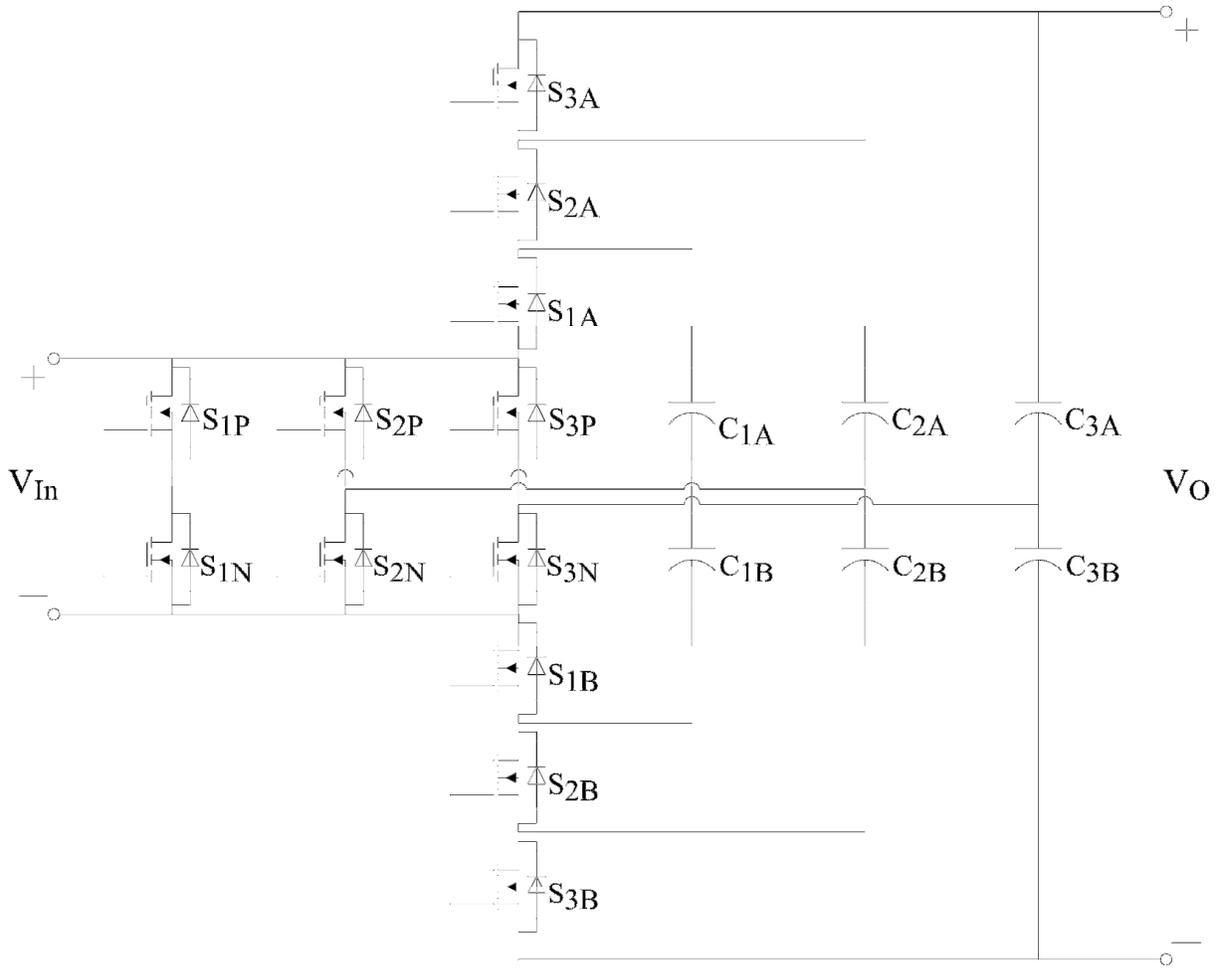


Figure 43. The 6X DC-DC Converter

The re-drawn 6X converter, shown in Figure 44 below, reveals the modular nature of the design.

This means that the boost factor can be increased simply by adding additional modules.

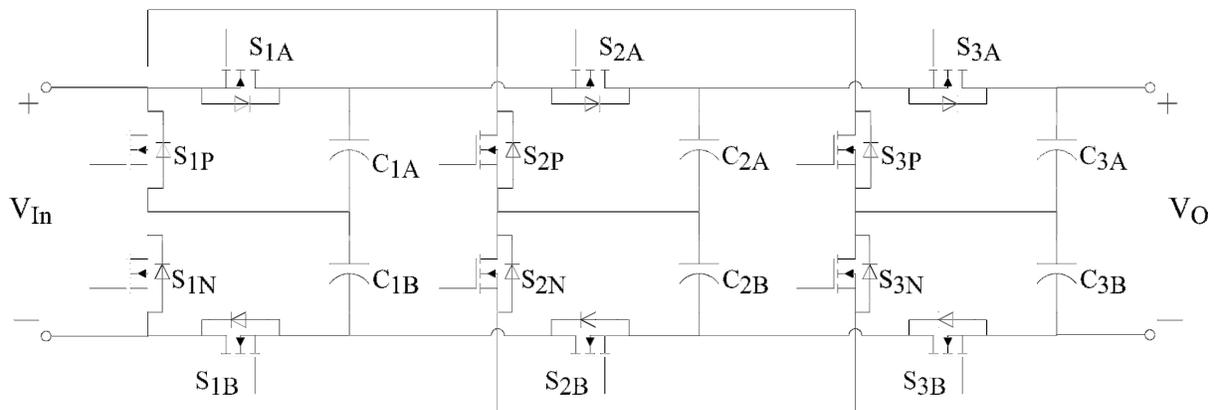


Figure 44. The Modular 6X DC-DC Converter

Splitting up the schematic shown in Figure 44 into individual modules gives the basic structure, shown in Figure 45.

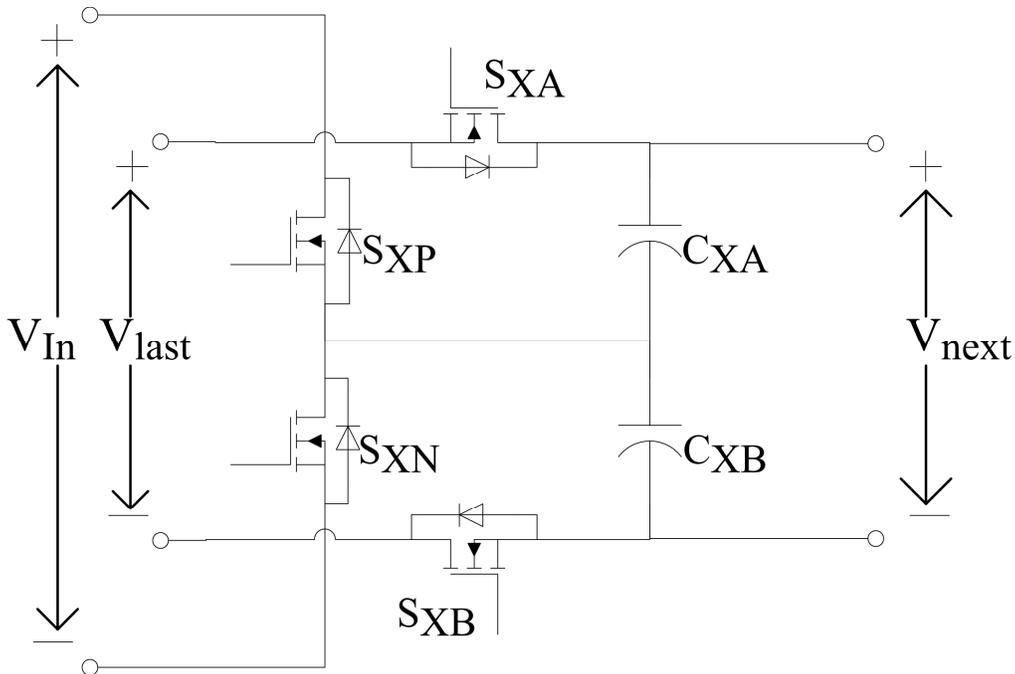


Figure 45. The NX Converter Module

Here, V_{in} is defined as it always has been, while V_{last} and V_{next} refer to the output voltage of the last module and the output of the current module respectively. These modules can be put end to end as many times as needed, and each gives an additional $2V_{in}$ to the output voltage. With this, the NX converter already has an improvement over the flying capacitor converter; while the flying capacitor converter was not modular in design, the NX converter is. This makes it easy to decrease or increase the boost factor. Having established this feature, a closer look at the converter's operation is in order.

Like the MMCCC, the NX converter is both modular and has only two switching states. This greatly simplifies the control required to drive the converter. These switching states are achieved through the utilization of the NX converter's switches as complementary pairs. The

two half-bridge switches, S_{XP} and S_{XN} , where X refers to the module number, form one complementary pair, while S_{XA} and S_{XB} form the other. Furthermore, S_{XP} and S_{XB} are either on or off simultaneously, as are S_{XN} and S_{XA} . The modules themselves are also complementary from their adjoining modules; that is, if S_{1P} and S_{1B} are on in the first module, then S_{2N} and S_{2A} are on in the second. The effect that this has is illustrated in the following two figures using the 6X converter as an example.

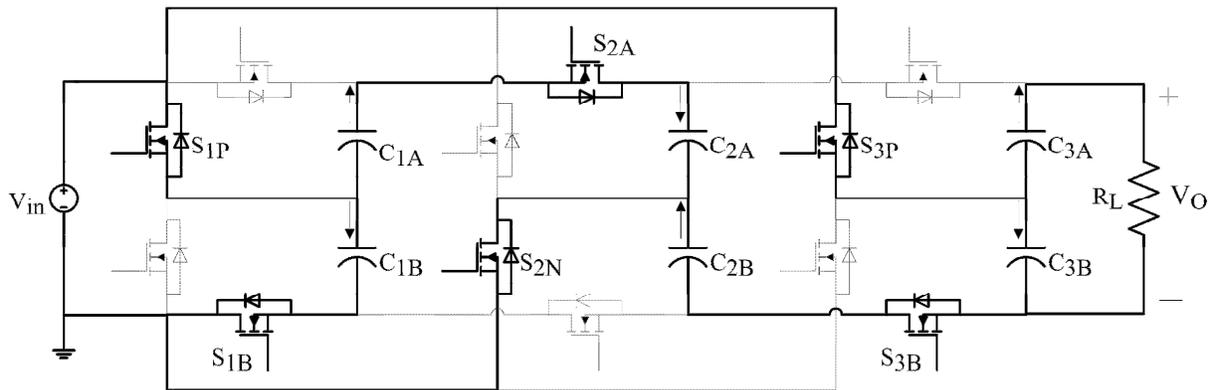


Figure 46. 6X Switching State I

Defining the switching configuration shown in Figure 46 as switching state I, several things become apparent. One thing to point out before continuing is that the two switching states divide the switching period evenly, so the duty cycle is 50%. Notice that in the first module, C_{1B} is placed in parallel with the source, raising its voltage to $1V_{in}$. In the meantime, C_{1A} is placed in series with the source in order to charge C_{2A} up to $2V_{in}$. The source is also in series with C_{2B} , and together they bring the voltage across C_{3B} up to $3V_{in}$. However, both C_{3A} and C_{3B} are

supplying current to the load. This process completes at time $T_{SW}/2$, and the converter transitions over to its second switching state.

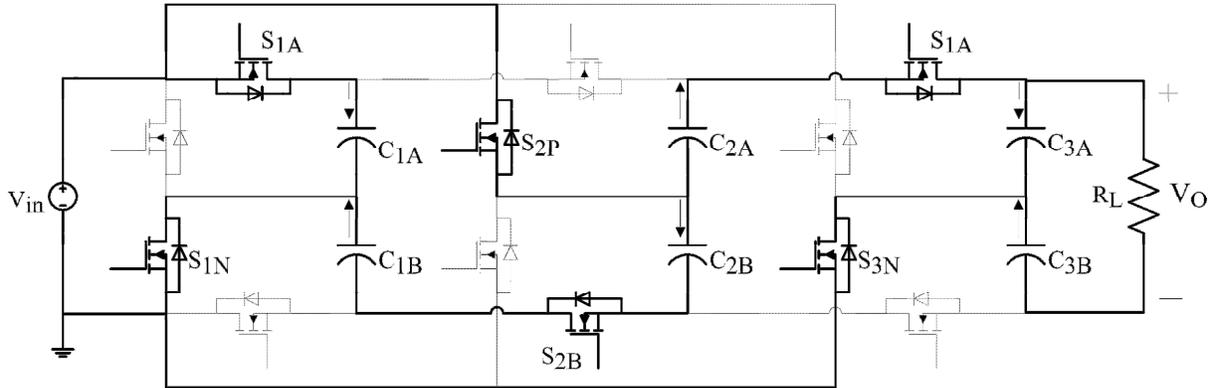


Figure 47. 6X Switching State II

Switching state II, shown in Figure 47 above, occupies the second half of the switching period. Here, the capacitors basically switch roles. Now C_{1A} is parallel with the source and is charged up to $1V_{in}$. The capacitor C_{1B} , rather than being charged, discharges through C_{2B} , charging it up to $2V_{in}$ since the source is now in series with both capacitors. Likewise, C_{2A} is placed in series with V_{in} in order to charge C_{3A} up to $3V_{in}$. Like before, both C_{3A} and C_{3B} must supply the load current. Now it is clear how the output voltage is achieved; both C_{3A} and C_{3B} are charged up to $3V_{in}$ on average, so the voltage across them together averages to $6V_{in}$. Notice the number of switches it takes the 6X to do this; there are twelve active switching devices in the 6X dc-dc converter, suggesting that it generally takes $2N$ devices to achieve a boost ratio of N with this topology. Indeed, this turns out to be the case, so the NX converter matches the flying capacitor converter on switch count, defeating the MMCCC in that area. In

other words, the NX converter combines the modular structure and simple control of the MMCCC with the greater voltage gain and lower switch count of the flying capacitor converter. Some extra information would be useful, however.

Examining the circuit in Figure 47, it is clear that S_{3A} must conduct a current that both supplies the load and charges C_{3A} . Since C_{3A} had to supply an average current of I_{Out} during state I, it needs to be supplied with an average current of I_{Out} during state II. Together, this shows that S_{3A} has to conduct $2I_{Out}$, as do S_{3P} , S_{3N} and S_{3B} . Following the current paths, it becomes obvious that the other half-bridge switches have to conduct $4I_{Out}$ while the A and B switches conduct an average of $2I_{Out}$. As for voltage blocking, all the switches in the first module only have to block IV_{in} , while only the half-bridge switches do thereafter. The other module's A and B switches need to be able to block at least $2V_{in}$. Taking this information, it is possible to derive the total device stress ratio.

$$\begin{aligned}
\bar{R}_S &= (N-2) \times 4I_{Out} \times V_{in} + 2 \times 2I_{Out} \times V_{in} + (N-2) \times 2I_{Out} \times 2V_{in} + 2 \times 2I_{Out} \times V_{in} \\
\Rightarrow \bar{R}_S &= \frac{1}{8} (4NP_{Out} - 8P_{Out} + 4P_{Out} + 4NP_{Out} - 8P_{Out} + 4P_{Out}) \quad (3.1.1) \\
\Rightarrow \bar{R}_S &= \frac{8N-8}{8} \times P_{Out} = \frac{8N-8}{8} p.u.
\end{aligned}$$

The final part of (3.1.1) assumes that $P_{in}=P_{out}=1 p.u.$ Thinking back, (3.1.1) is clearly identical to (2.4.1), the total device stress ratio for the MMCCC. In other words, the NX converter's silicon should cost no more than that of the MMCCC's for a given voltage boost factor. Since

the switch utilization factor was found to be pointless for these types of converters, it will be skipped for this converter. So far, the NX converter topology has shown itself to be a formidable competitor to the flying capacitor converter and the MMCCC, as it combines the best of both. Yet another advantage it has is the limited number of active devices in each current loop. An examination of Figure 46 and Figure 47 shows that three is the maximum number of switches in each loop, and this holds for any boost factor N . This puts less resistance in each loop, increasing the efficiency of the converter. This feature is shared by the MMCCC, but not by the flying capacitor converter. Before any in-depth analysis, a confirmation of the operation via simulation is in order.

Once again using Saber, the 6X converter was simulated using mostly the same parameters as the previous simulations. The stage capacitors were all $100 \mu F$, the switching frequency was 100 kHz , the input voltage was 20 V , and, this time, the load was 20Ω . The simulation results can be seen in the following two figures.

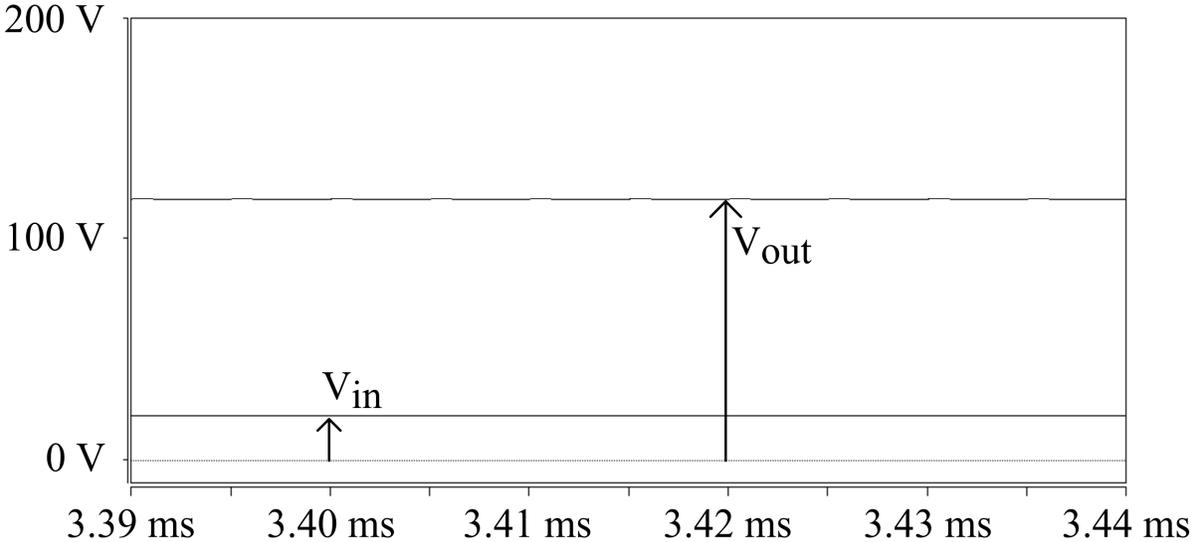


Figure 48. 6X Simulation Input and Output Voltages

In this simulation, the output voltage averaged to around 117.6 V , which is just under the predicted 120 V . This small deviation is the result of voltage drops across the various resistances in the circuit. To get visual feel for the circuit's behavior, examples of the capacitor voltage were also plotted in Figure 49.

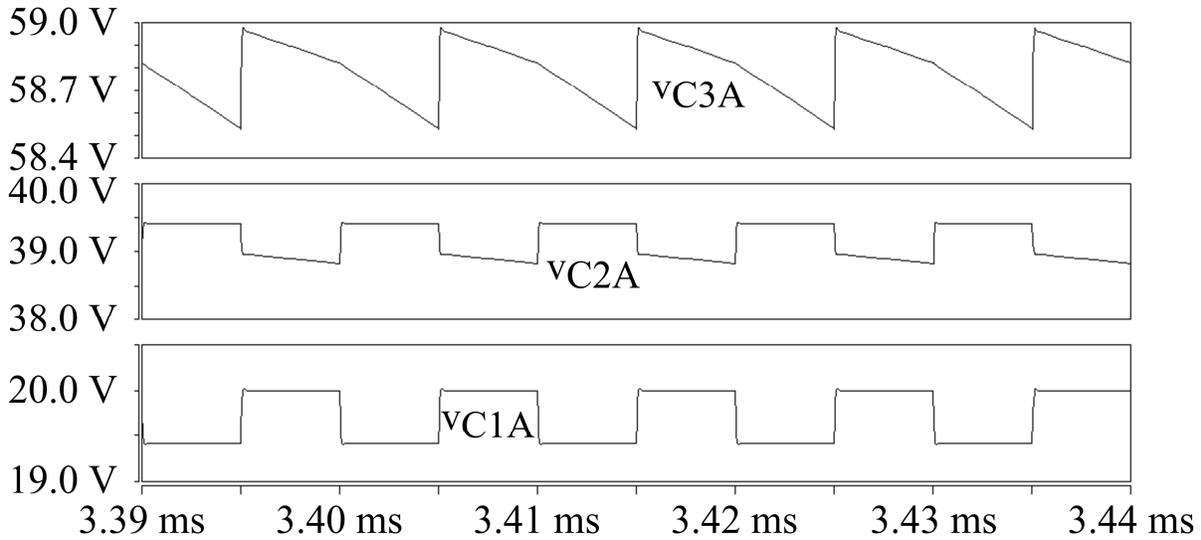


Figure 49. 6X Simulation Capacitor Voltages

In this figure, voltages from capacitors in each module are displayed, and the behavior is quite clear. For C1A and C2A, the voltage mostly appears like a square wave, but looks are deceiving. Although not very visible here, there is a small fluctuation at the beginning of each capacitor's charging period. This is caused by the capacitors charging up according to the RC time constant, which is not very large in this case. In fact, for most cases, the RC time constant will be very small because the component's resistance is only on the order of a few milliohms and the capacitors are, in practical circuits, rarely larger than $100\ \mu\text{F}$ or so. This makes the exponential component of the capacitor voltage and current fleeting so long as the frequency is not too high. If the frequency gets into the megahertz range, then the exponential behavior will start to have an effect, but that sort of operating condition is currently unusual for this topology. It can safely be

assumed, for this converter and its analysis, that $T_{SW} \gg RC$. Before continuing, notice the behavior of C_{3A} . It seems to be mostly linear in both sections of the switching period, aside from its charging; this is because the load current is always running through the output stage capacitors, and this is what makes it behave differently.

3.2. NX Converter Analysis

In order to get a practical analytical understanding of this converter, a closer look at Figure 46 and Figure 47 is needed. Because the circuits are symmetric, solutions for only one switching state can easily be applied to the other. Using Figure 46, it can be seen that it breaks down into three separate current loops. Making the safe assumption that the resistances and capacitors in each module are identical and that the output current is constant, some general equations describing the system can be written.

$$V_{in} = R_1 i_1(t) + v_{C1B}(t) \quad (3.2.1)$$

$$i_1(t) = C_1 \frac{dv_{C1B}}{dt} \quad (3.2.2)$$

$$V_{in} = R_2 i_2(t) - v_{C1A}(t) + v_{C2A}(t) \quad (3.2.3)$$

$$i_2(t) = C_2 \frac{dv_{C2A}}{dt} = -C_1 \frac{dv_{C1A}}{dt} \quad (3.2.4)$$

$$V_{in} = R_3 i_3(t) - v_{C2B}(t) + v_{C3B}(t) \quad (3.2.5)$$

$$i_3(t) = -C_2 \frac{dv_{C2B}}{dt} = C_3 \frac{dv_{C3B}}{dt} + I_{out} \quad (3.2.6)$$

$$I_{out} = -C_3 \frac{dv_{C3A}}{dt} \quad (3.2.7)$$

In these equations, the subscripts in the resistances and the capacitances refer to the number of the loop in question. From these equations, it is easy to recognize that the currents and voltages will mostly follow the standard forms for RC circuits, but (3.2.5)-(3.2.7) throw off the simplicity of the standard form. In order to solve these equations, the boundary conditions have to be specified; however, in order to have the correct boundary conditions, the general solutions must be used in conjunction with things already known about the circuit, especially the average current through the capacitors during a given half-period. In order to shorten the equations, the boundary conditions are given the following designation: V_{CXAI} refers to the capacitor voltage of C_{XA} at the beginning of the first switching state. V_{CXB2} refers to the voltage of C_{XB} at the beginning of state II, where X refers to the module number. These values will be valuable for designing the converter.

The generalized solutions for the previous equations are as follows:

$$\tau_1 = R_1 C_1 \quad (3.2.8)$$

$$i_1(t) = \frac{(V_{in} - V_{C1B1})}{R_1} e^{-t/\tau_1} \quad (3.2.9)$$

$$v_{C1B}(t) = V_{in}(1 - e^{-t/\tau_1}) + V_{C1B1} \times e^{-t/\tau_1} \quad (3.2.10)$$

$$C_{2X} = \frac{C_1 C_2}{C_1 + C_2}, \quad \tau_2 = R_2 C_{2X} \quad (3.2.11)$$

$$i_2(t) = \frac{(V_{in} + V_{C1A1} - V_{C2A1})}{R_2} e^{-t/\tau_2} \quad (3.2.12)$$

$$v_{C1A}(t) = \left(\frac{1}{C_1 + C_2} \right) \left(\begin{array}{l} C_2 V_{in} (e^{-t/\tau_2} - 1) + V_{C1A1} (C_1 + C_2 e^{-t/\tau_2}) \\ + C_2 V_{C2A1} (1 - e^{-t/\tau_2}) \end{array} \right) \quad (3.2.13)$$

$$v_{C1A}(t) = \left(\frac{1}{C_1 + C_2} \right) \left(\begin{array}{l} C_1 V_{in} (1 - e^{-t/\tau_2}) + C_1 V_{C1A1} (1 - e^{-t/\tau_2}) \\ + V_{C2A1} (C_1 e^{-t/\tau_2} + C_2) \end{array} \right) \quad (3.2.14)$$

$$C_{3X} = \frac{C_2 C_3}{C_2 + C_3}, \quad \tau_3 = R_3 C_{3X} \quad (3.2.15)$$

$$i_3(t) = \frac{1}{R_3 (C_2 + C_3)} \left(\begin{array}{l} (C_2 + C_3) (V_{in} + V_{C2B1} - V_{C3B1}) e^{-t/\tau_3} \\ + I_{out} R_3 C_2 (1 - e^{-t/\tau_3}) \end{array} \right) \quad (3.2.16)$$

$$v_{C2B}(t) = \frac{1}{(C_2 + C_3)^2} \left(\begin{array}{l} C_2^2 V_{C2B1} + C_3^2 (V_{in} + V_{C2B1} - V_{C3B1}) e^{-t/\tau_3} \\ - C_3 (I_{out} t + C_3 V_{in} - C_3 V_{C3B1}) - C_2 I_{out} t \\ + C_2 C_3 I_{out} R_3 (1 - e^{-t/\tau_3}) + C_2 C_3 V_{in} (e^{-t/\tau_3} - 1) \\ + C_2 C_3 V_{C2B1} (e^{-t/\tau_3} + 1) + C_2 C_3 V_{C3B1} (1 - e^{-t/\tau_3}) \end{array} \right) \quad (3.2.17)$$

$$v_{C3B}(t) = \frac{1}{(C_2 + C_3)^2} \left(\begin{array}{l} C_2^2 ((1 - e^{-t/\tau_3}) (V_{in} + V_{C2B1} - I_{out} R_3) \\ + V_{C3B1} e^{-t/\tau_3}) + C_3^2 V_{C3B1} - C_3 I_{out} t \\ + C_2 (C_3 (V_{in} + V_{C2B1} + V_{C3B1}) - I_{out} t) \\ - C_2 C_3 (V_{in} + V_{C2B1} - V_{C3B1}) e^{-t/\tau_3} \end{array} \right) \quad (3.2.18)$$

$$v_{C3A}(t) = V_{C3A1} - \frac{I_{out}}{C_3} t \quad (3.2.19)$$

Due to the effect that the load has on the last stage's capacitors, the equations became somewhat ugly. However, for the most part the boundary conditions are much simpler and, perhaps, are more useful. Using the fact that the averages of (3.2.9), (3.2.12), and (3.2.16) are all $2I_{out}$, plus the assumption that the exponential terms die off after a half-period, the boundary conditions were accurately found to be:

$$V_{C1A1} = V_{C1B2} = V_{in} \quad (3.2.20)$$

$$V_{C1B1} = V_{C1A2} = V_{in} - \frac{I_{out}T_{sw}}{C_1} \quad (3.2.21)$$

$$V_{C2A1} = V_{C2B2} = 2V_{in} - \frac{I_{out}T_{sw}}{C_{X2}} \quad (3.2.22)$$

$$V_{C2B1} = V_{C2A2} = 2V_{in} - \frac{I_{out}T_{sw}}{C_1} \quad (3.2.23)$$

$$V_{C3B1} = V_{C3A2} = 3V_{in} - \frac{I_{out}T_{sw}}{C_1} \quad (3.2.24)$$

$$-\frac{1}{C_2C_3} (I_{out}T_{sw}(C_2 + C_3) - C_2I_{out} \frac{T_{sw}}{2} + I_{out}R_3 \frac{C_2^2C_3}{C_2 + C_3})$$

$$V_{C3B2} = V_{C3A1} = \frac{1}{(C_2 + C_3)^2} \left(\begin{array}{l} C_2^2(V_{in} + V_{C2B1} - I_{out}R_3) \\ + C_3^2V_{C3B1} - C_3I_{out} \frac{T_{sw}}{2} \\ + C_2(C_3(V_{in} + V_{C2B1} + V_{C3B1}) - I_{out} \frac{T_{sw}}{2}) \end{array} \right) \quad (3.2.25)$$

Using MATLAB to compare these equations to the values derived from simulation, the voltages were accurate to within one-thousandth of a volt. Furthermore, this allows for the easy calculation of the capacitor voltage ripple.

$$\Delta V_{C1} = V_{C1B2} - V_{C1B1} = \frac{I_{out}T_{sw}}{C_1} \quad (3.2.26)$$

$$\Delta V_{C2} = V_{C2A2} - V_{C2A1} = \frac{I_{out}T_{sw}}{C_2} \quad (3.2.27)$$

These voltage ripples are peak-to-peak values. However, the voltage ripple for the output stage capacitors is not so easily calculated, as their maximum voltage occurs during the charging phase just slightly after the beginning of the half-period. This is a value best calculated numerically, if it is needed. As a rule of thumb, however, it may be better to go with:

$$\Delta V_{C3} \approx \frac{I_{out} T_{sw}}{2C_3} \quad (3.2.28)$$

This is an approximation of the peak-to-peak voltage ripple on the final module capacitors, but it may be more valuable for designing the converter from the standpoint of being easy to use. Nevertheless, equations representing the currents and voltages at work within the 6X converter, and extending to any NX converter, have been derived. However, that leaves the converter's efficiency to be analyzed.

The power losses within the NX dc-dc converter can be broken down into four parts: the capacitor charging loss, the conduction loss, the switching loss, and the gate drive loss. Since the gate drive loss is likely the smallest component, and is often powered separately from the converter's main supply, it can be neglected for now. That still leaves the other three components. In regards to multilevel converter circuits, this subject was already covered in [6] and [15], but its work can easily be extended to the NX converter. When discussing the subject of losses, it is best to begin by discussing that which is most familiar first.

The switching loss refers to the power losses incurred while the semiconductor devices go through their transition from on to off and vice versa. This happens because the switch, considered to be a MOSFET in this case, does not turn on or off instantaneously. In fact, as soon as the gate threshold voltage is reached, the MOSFET will begin to conduct current, but the drain-source voltage will not begin to drop until the gate-source capacitor is completely charged [16]. This sort of behavior can be somewhat difficult to model, and a less accurate but more easily utilized method to model it can be found in [17]. According to this paper, the commonly used formula for the estimation of a MOSFET's switching losses is:

$$P_{sw} = \frac{1}{2} V_{DS} I_D (t_{on} + t_{off}) f_{sw} + \frac{1}{2} C_{OSS} V_{DS}^2 f_{sw} \quad (3.2.29)$$

This equation assumes a linear transition of the drain-source voltage, V_{DS} , and the drain current, I_D , during the turn-on and turn-off times, t_{on} and t_{off} . The first term represents the energy from the changing voltage and current multiplied by the switching frequency, f_{sw} , giving the power. The second term accounts for the energy stored in the MOSFET's output capacitance, C_{OSS} . Multiplying this by the frequency again gives the power losses from this effect. (3.2.29) estimates the switching losses for one MOSFET, so the inputs to the equation have to be changed for each device with different switching conditions or component parameters and power lost in each switch should be added up. Another thing to note in (3.2.29) is the direct dependence on the switching frequency; as the switching frequency increases, so does the associated switching loss. This would put an upper bound on the switching frequency of the converter. However, the actual behavior of the voltages and the currents during the switching transition cannot really be expected to behave in this fashion. To that end, (3.2.29) can be used only as a very rough estimation. Luckily, switching loss is not the main source of loss in most switched capacitor converters. The conduction loss and capacitor charging loss provide most of the losses.

Conduction loss, in the case of switched capacitor converters, refers to the losses suffered due to the load current passing through the resistance within the circuit. These currents, described in 3.1 near (3.1.1), are based off of the average currents that must be passing through the various components of the system during each switching state. The resistance comes primarily from the semiconductors' on-resistances, but the capacitors' ESR and the trace resistance also contribute somewhat to the losses. For any analysis of these losses, the trace resistance will be ignored, and the ESR is expected to be low, as each individual capacitor's ESR

is small and multiple capacitors in parallel are used for each stage capacitance. However, thanks to the symmetry of the circuit, the conduction loss should be the same during both switching states. Using state I of the 6X as an example, the conduction loss could be expressed as:

$$P_{cond} = (4I_{out})^2(R_{S1P} + R_{S2N}) + (2I_{out})^2(R_{S1B} + R_{C1A} + R_{C1B} + R_{S2A} + R_{C2A} + R_{C2B} + R_{S3P} + R_{S3B}) + (I_{out})^2(R_{C3A} + R_{C3B}) \quad (3.2.30)$$

This should give an estimation of the conduction loss in the 6X converter, and is easily extendable to any NX converter. As seen in (3.2.30), it is purely dependant on the output current and the parasitic resistance. Lowering the circuit's resistances should minimize this type of loss. Finally, only the capacitor charging loss remains.

The capacitor charging loss is likely the largest source of power loss in a converter of this type. Whenever two capacitors are placed in series and one discharges into the other, a certain amount of energy is lost. The amount of energy stored in a capacitor is given by:

$$E_{cap} = \frac{1}{2}CV^2 \quad (3.2.31)$$

At first, the two capacitors are at completely different voltages, but they reach equilibrium by the end of the half period. However, an energy loss is associated with this process. For example, consider two capacitors, both with capacitance C , separated by a resistor. One capacitor has voltage $V+\Delta V$ and the other only V . The total energy in this setup is initially:

$$E_{start} = \frac{1}{2}C(V^2 + \Delta V^2 + 2V\Delta V) + \frac{1}{2}CV^2 \quad (3.2.32)$$

Assuming that the RC time constant is very small compared to the switching period, the total energy at the end becomes:

$$E_{end} = \frac{1}{2}C(2V^2 + 2V\Delta V + \frac{1}{2}\Delta V^2) \quad (3.2.33)$$

Thus, the energy lost in the transfer is equal to the difference between the two energies. In this example, it becomes:

$$E_{start} - E_{end} = \frac{1}{4} C \Delta V^2 \quad (3.2.34)$$

An easy way of applying this to any other system, like the 6X, is just calculating the energy lost by looking at the starting and ending energy of a two capacitor system and subtracting. The voltages given in (3.2.20)-(3.2.25) are useful for accomplishing this task. The power loss from this can be derived simply by taking the energy lost and multiplying by the switching frequency. Overall, the use of the RMS currents to calculate the overall resistive losses might provide a more direct means of calculating the efficiency. The NX converter still has other possibilities, however.

3.3. NX Converter ZCS Possibilities

The similarities of the NX converter and the MMCCC suggest the possibility of achieving zero-current-switching to decrease the switching losses. It was already mentioned that ZCS reduces switching losses virtually to zero by forcing the switch current to zero during both the turn-on and turn-off transitions. Using [12] and [13] as a starting point, [19] suggested using ZCS in the NX converter. However, several of the results found in [19] have flaws capable of quick correction using the results shown in section 2.4 for the ZCS MMCCC. It can be easily shown that the ZCS version of the NX converter breaks down into circuits identical to those found in the MMCCC.

To begin, it should be noted that all circuits have some amount of parasitic inductance in them. Wherever current loops exist in an electric circuit, and all circuits must possess them, stray inductance can be found. This is simply a result of Maxwell's laws, and, although the

geometry can be carefully designed so as to minimize the stray inductance, it can never be reduced to zero. With that in mind, this stray inductance can be utilized to form the resonant circuits needed to achieve ZCS. Consider the slightly modified circuit in Figure 50 below.

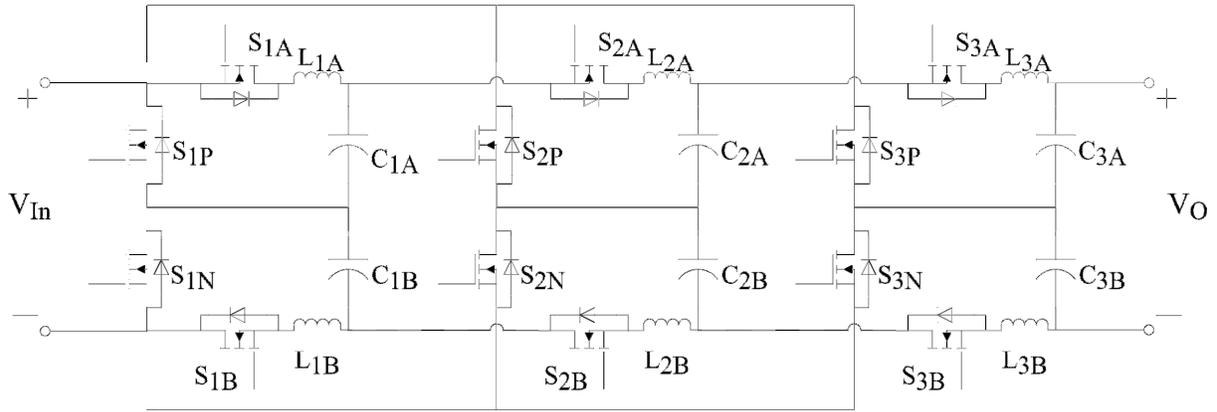


Figure 50. The ZCS 6X Converter

This circuit is the same as that shown in Figure 44 before, but now stray inductances are included in each module. Once again, the aim is to design and tune the circuit so that the resonant frequency of each series resonant loop equals the converter's switching frequency. To analyze the behavior of the circuit, however, the circuit's loop equations must be derived. To this end, it is important to examine the converter's two switching states. Switching states I and II can be seen in Figure 51 and Figure 52 below. It is easy to see that each state can be broken down into three individual circuits that can be solved for and made to fit the circuit's general behavior using the average currents and voltages.

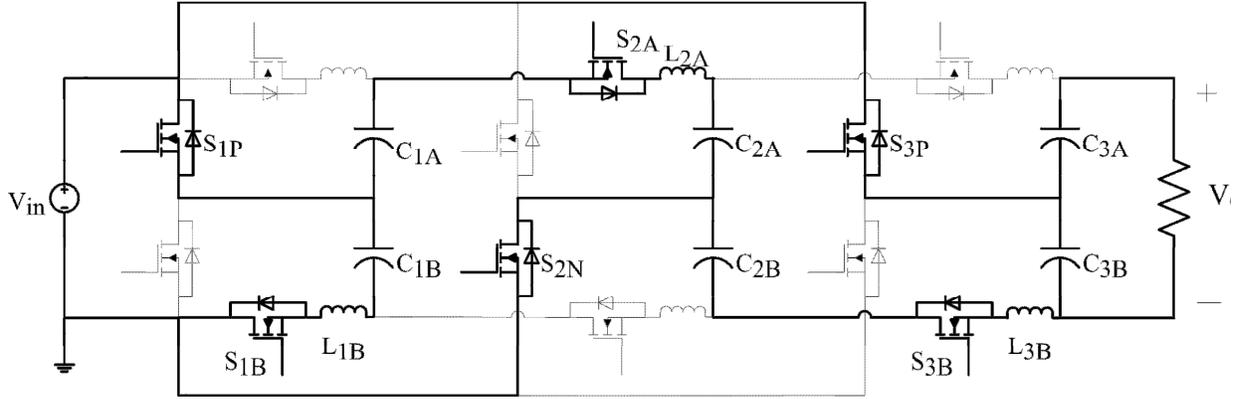


Figure 51. ZCS 6X Converter Switching State I

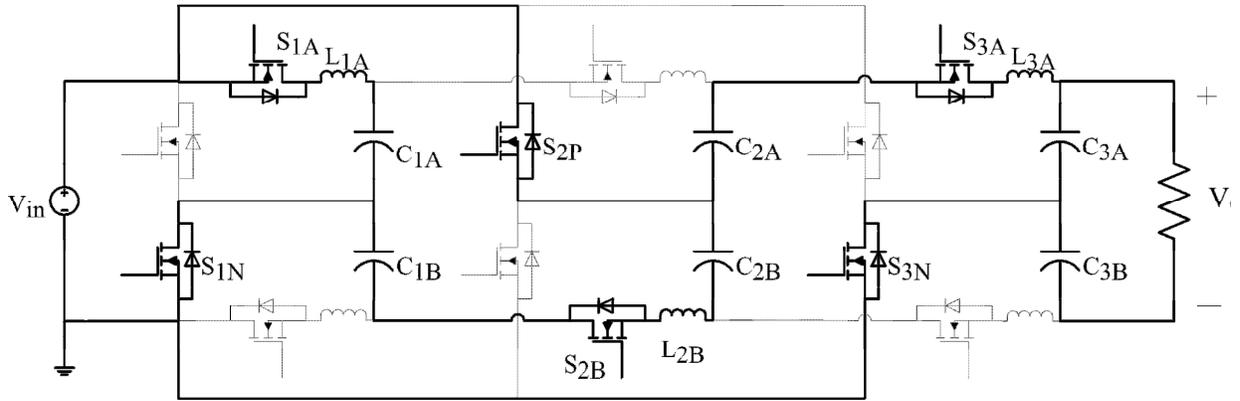


Figure 52. CS 6X Converter Switching State II

The individual circuits end up being identical in behavior to those shown in Figure 36 and Figure 37 from earlier. Since states I and II are symmetric, the solutions for the inductor currents and capacitor voltages will be the same, but with a time shift equal to half of the switching period. Making note of that, consider the equations governing the behavior of switching state I.

$$V_{in} = L_{1B} \frac{di_{L1B}}{dt} + v_{C1B} \quad (3.3.1)$$

$$i_{L1B} = C_{1B} \frac{dv_{C1B}}{dt} \quad (3.3.2)$$

$$V_{in} = L_{2A} \frac{di_{L2A}}{dt} - v_{C1A} + v_{C2A} \quad (3.3.3)$$

$$i_{L2A} = -C_{1A} \frac{dv_{C1A}}{dt} = C_{2A} \frac{dv_{C2A}}{dt} \quad (3.3.4)$$

$$V_{in} = L_{3B} \frac{di_{L3B}}{dt} - v_{C2B} + v_{C3B} \quad (3.3.5)$$

$$i_{L3} = -C_{2B} \frac{dv_{C2B}}{dt} = C_{3B} \frac{dv_{C3B}}{dt} + I_{out} \quad (3.3.6)$$

$$I_{out} = -C_{3A} \frac{dv_{C3A}}{dt} \quad (3.3.7)$$

The similarities between (3.3.1)-(3.3.7) and (2.4.4)-(2.4.13) are striking. Since the average voltage across each individual capacitor in each module is the same as in the MMCCC, the results will be the same. Once again, it is assumed that all capacitors equal C and the inductors follow the rule where $L_{1A}=L_{1B}=L$, $L_{2A}=L_{2B}=2L$ and $L_{3A}=L_{3B}=2xL$. With this, the solutions for the inductor currents and capacitor voltages in state I are as follows.

$$\omega = \frac{1}{\sqrt{LC}} = \frac{2\pi}{T_{sw}} \quad (3.3.8)$$

$$i_{L1B}(t) = \pi I_{out} \sin(\omega t) \quad (3.3.9)$$

$$v_{C1B}(t) = V_{in} - \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (3.3.10)$$

$$v_{C1A}(t) = V_{in} + \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (3.3.11)$$

$$v_{C2A}(t) = 2V_{in} - \frac{\pi I_{out}}{C\omega} \cos(\omega t) \quad (3.3.12)$$

$$v_{C2B}(t) = -\frac{I_{out}}{2C} t + 3V_{in} + \frac{\pi I_{out}}{4} \sqrt{\frac{L}{C}} + \frac{3\pi I_{out}}{4} \sqrt{\frac{L}{C}} \cos\left(\frac{\omega}{\sqrt{x}} t\right) + \frac{I_{out} \sqrt{x}}{2} \sqrt{\frac{L}{C}} \sin\left(\frac{\omega}{\sqrt{x}} t\right) \quad (3.3.13)$$

$$i_{L3B}(t) = \frac{I_{out}}{2} - \frac{I_{out}}{2} \cos\left(\frac{\omega}{\sqrt{x}} t\right) + \frac{3\pi I_{out}}{4\sqrt{x}} \sin\left(\frac{\omega}{\sqrt{x}} t\right) \quad (3.3.14)$$

$$v_{C3A}(t) = 4V_{in} + \frac{\pi I_{out}}{2} \sqrt{\frac{L}{C}} - \frac{I_{out}}{C} t \quad (3.3.15)$$

$$v_{C3B}(t) = -\frac{I_{out}}{2C} t + 4V_{in} + \frac{\pi I_{out}}{4} \sqrt{\frac{L}{C}} - \frac{3\pi I_{out}}{4} \sqrt{\frac{L}{C}} \cos\left(\frac{\omega}{\sqrt{x}} t\right) - \frac{I_{out} \sqrt{x}}{2} \sqrt{\frac{L}{C}} \sin\left(\frac{\omega}{\sqrt{x}} t\right) \quad (3.3.16)$$

$$x \approx 0.79821687 \quad (3.3.17)$$

These solutions are just like the MMCCC, but the each switching state is symmetric. In other words, the solutions for state II are identical to (3.3.8)-(3.3.17) except that the module capacitor and inductor to which they apply are reversed and a time shift is used. As for using these equations, several points can quickly be made. For the first and second modules, the capacitor voltage ripple is seen to be:

$$\Delta v_{C1,2} = \frac{2\pi I_{out}}{C\omega} \quad (3.3.18)$$

This value is a peak-to-peak voltage, and it is easily shown to be the same as (3.2.26) or (3.2.27) for a fixed set of capacitance, output power, and switching frequency. Furthermore, the voltage behavior of the output stage capacitors is not different enough from the others to warrant the use of a totally different equation for calculating the voltage ripple. The third module's capacitor's voltage ripples can be safely estimated as:

$$\Delta v_{C3} \approx \frac{\pi I_{out}}{C\omega} \quad (3.3.19)$$

This takes into account the effect of the two capacitors also being in series, reducing the ripple in half. In order to prove that this concept is possible, a simulation was performed.

Using Saber Simulator once again, the ZCS 6X converter was simulated using conditions that should already be familiar. The switching frequency was *100 kHz*, the input voltage was *20*

V , the load was 20Ω , and the stage capacitors were all $100 \mu F$. The inductors for the first, second and third modules were 25.33 nH , 50.66 nH and 40.4377 nH respectively. Switch resistances and diode voltages were kept very low to estimate ideal conditions, and no dead-time was utilized. The results of the simulation are shown in the following figures.

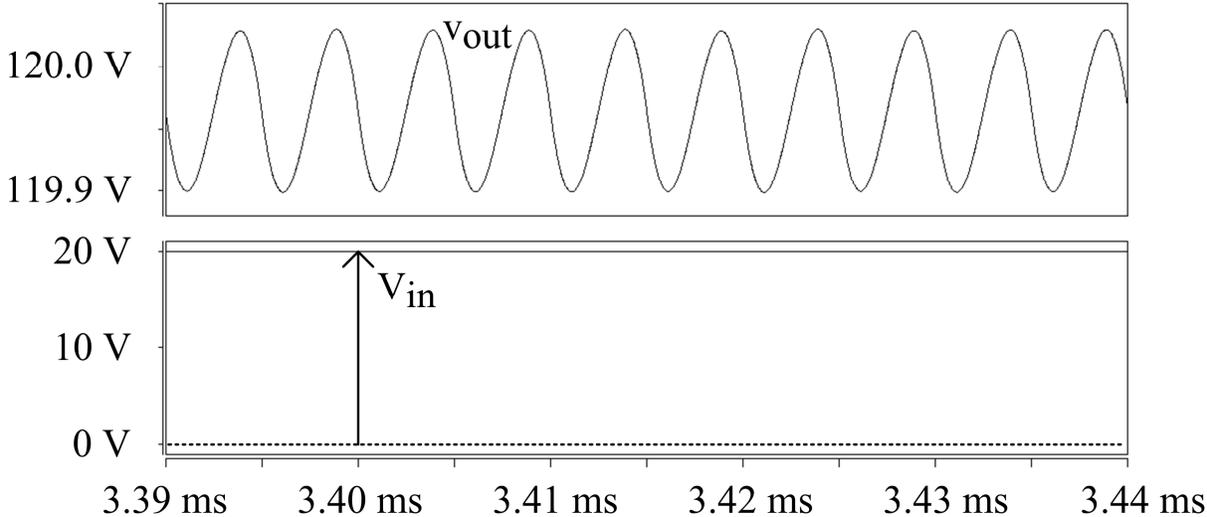


Figure 53. ZCS 6X Simulation Input and Output Voltages

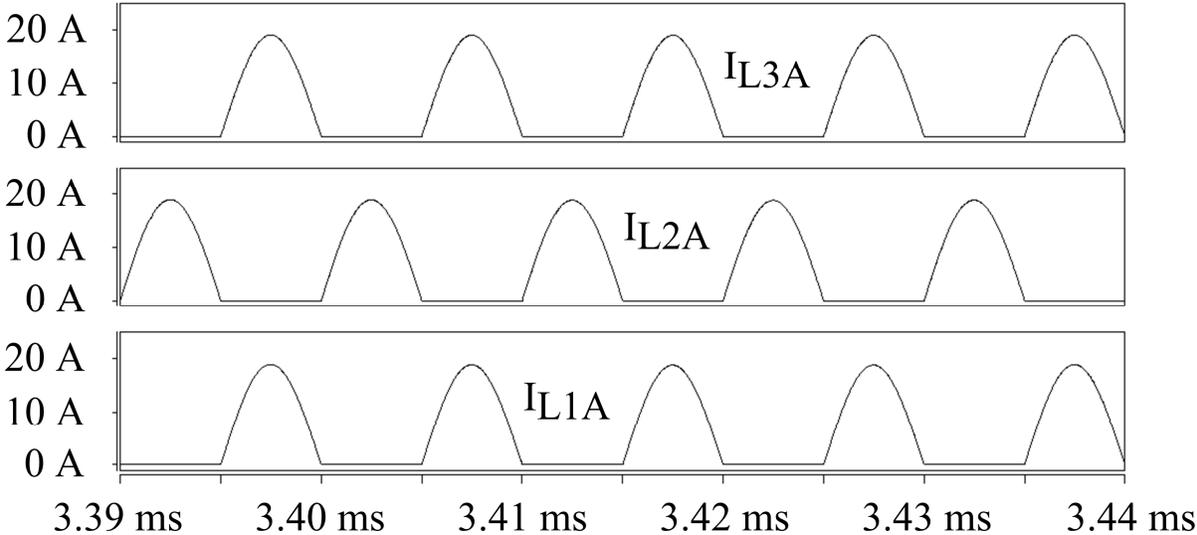


Figure 54. ZCS 6X Simulation Inductor Currents

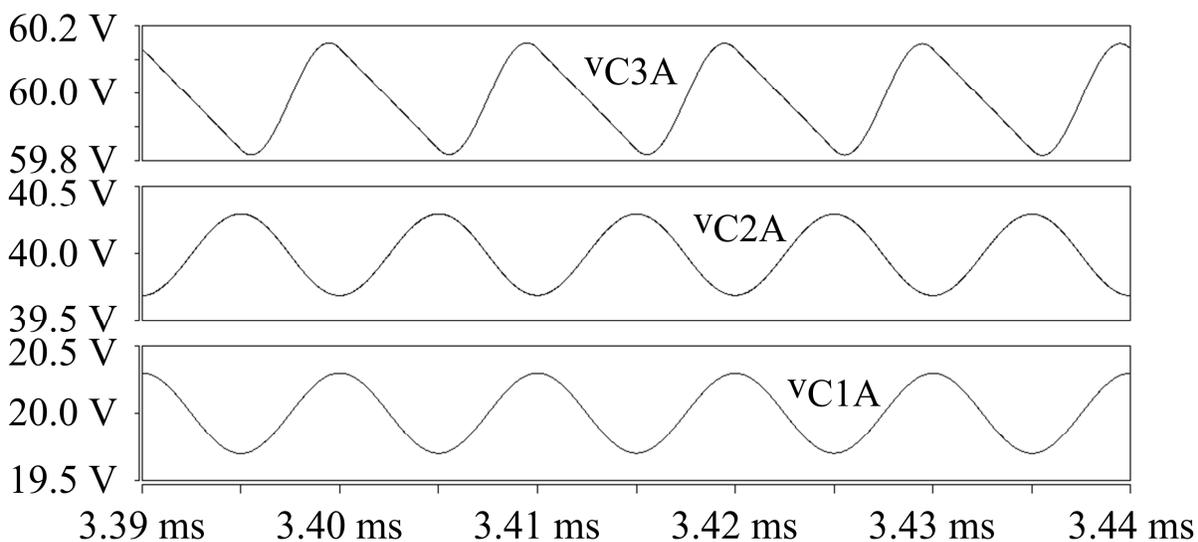


Figure 55. ZCS 6X Simulation Capacitor Voltages

In Figure 53 it can be seen that the output voltage is, on average, very close to eight times the input. Furthermore, the voltage ripple now behaves very much like a cosine function. The inductor currents depicted in Figure 54 illustrate the zero-current-switching that is achieved with this setup. Finally, Figure 55 shows the validity of (3.3.11), (3.3.12), (3.3.15) and (3.3.16), and it gives a graphic example of what behavior to expect. Although all of this seems to suggest that the ZCS NX converter is a viable option, there are drawbacks.

During all the preceding analysis, the circuits were considered to be either composed entirely of resistances and capacitances or capacitances and inductances. In reality, all three co-exist in the physical design, and the parasitic circuit elements are distributed throughout the layout. This means not only that the voltage and current behavior should deviate substantially from the previously predicted cases, but that tuning the circuit for ZCS would be extremely difficult. One area in particular to note on the NX converter topology is the node connecting the half-bridges' center points to the capacitors, as seen in Figure 44. The current through this region is alternating current, so it can be referred to as the ac node. Currents from two loops that

were, up to now, considered separate flow through this area. If inductance is located here, it will not only have an effect on the resonant behavior of the circuit, but it will also couple the current loops together. This has the effect of making the circuit nearly impossible to tune without adjusting everything all at once, as well as making the solutions for the currents and voltages significantly more complicated. While it may very well be that this effect cannot be ignored in a real circuit, it is perhaps not terribly significant in the larger scheme of things. However, with the general idea of the stray inductance having an effect on the converter's behavior, more sense can now be made about the experimental results.

3.4. 8X Converter Experimental Results

In order to test the actual capabilities of the NX converter topology, an 8X *1-kW* converter was designed, built and tested. The operating input voltage range was between *20 V* and *40 V*, and it was decided to use the hard-switching design rather than spend so much time trying to tune a circuit that could, in all likelihood, be incapable of being properly tuned. In order to make this circuit, the following choices were made.

Since the input voltage can be as high as *40 V*, MOSFETs capable of blocking at least one or two times that were needed. Using a multiplication factor of *1.5* for safety, half of the MOSFETs needed to be rated for *60 V* and the other half for *120 V*. This limited the selection available considerably, and the decision was made based on a combination of low on-resistance and low gate charge. The result was the choice to use the IPB017N06N3 G and the IPB036N12N3 G from Infineon Technologies, which were rated at *180 A* and *60 V* and *120 V* respectively. As for the stage capacitors, choices were even more limited. Due to their small size, high-temperature capabilities, low ESR and ESL, multilayer ceramic capacitors (MLCC) were selected as the optimal choice. However, finding MLCCs with both voltage ratings and

capacitances that were high enough made the range of options smaller yet. In the end, two types of capacitors were purchased: the $100\text{-V } 15 \mu\text{F}$ C5750X7S2A156M, and the $250\text{-V } 2.2 \mu\text{F}$ C5750X7T2E225K. Both capacitors are manufactured by TDK Corporation. Initially, the C5750X7S2A156M was going to be used in the first module, but the C5750X7T2E225K ended up being used for the stage capacitors in all the modules; the C5750X7S2A156M was relegated to supporting the dc input voltage. Six capacitors were used in place of each stage capacitor illustrated in Figure 44 due to size constraints. Before continuing, however, an interesting feature of MLCCs should be mentioned.

The materials used to produce MLCCs possess properties that cause the device's capacitance to change with the dc voltage across it. While the ratings may state $2.2 \mu\text{F}$ as the capacitance, it is important to note that this is the case only at 0 V . As the voltage increases from zero, the capacitance of the device decreases rapidly. This makes the stage capacitances even smaller than their rated values, and makes ZCS applicable only at a single input voltage without specialized control. Since the stage capacitors experience one, two, three and four times the input voltage, the amount of the capacitance drop changes from stage to stage as well. This needs to be taken into account when performing simulations of any real circuits.

The circuit was constructed on a four-layer printed circuit board (PCB) using the top layer for the power circuitry, the bottom for the control electronics, and the middle two layers as power and ground planes to the control layer. Due to the layout, wires were used when connecting the ac node together, so some inductance on the order of a few tens of nanohenries should be in that area. The circuit itself is depicted in Figure 56 below. Although not depicted, the circuit was controlled using a pulse width modulation (PWM) chip made by Texas Instruments called the UC3525. The external components connected to this chip determine the

switching frequency, duty cycle and dead-time produced by the IC, and the operating range of these variables is also determined by them.

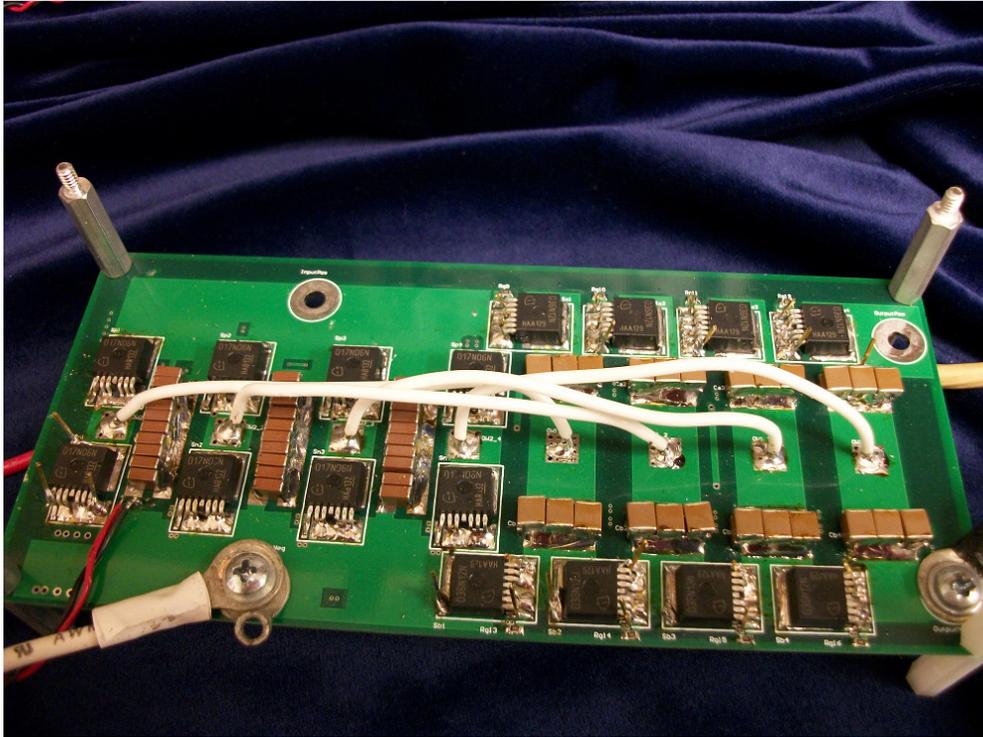


Figure 56. The 1-kW 8X prototype (For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis)

In Figure 56, the top layer of the 8X prototype can be seen. This is where all the components of the power circuit are located. The MOSFETs are the small black boxes with metal leads, and the four pairs of them on the board's left-hand side are the circuit's half-bridges. The white wires are what were previously called the AC nodes, and they are made of wires in order to allow the use of a current sensor. The light brown squares are the MLCCs; the right-hand sets of MLCCs comprise the stage capacitors. The dimensions of the board are about 3 inches wide by seven inches long, making the converter quite small in size. All of this had the effect of increasing the power density. With this new board at hand, tests were performed to both confirm its function as well as determining its efficiency.

Once debugging was concluded, consecutive tests were performed under conditions of increasing input voltage to confirm the circuit's proper functioning and its durability. These tests were performed using a switching frequency of 164 kHz , a dead-time of 500 ns as determined by the PWM chip, and a load of $200\ \Omega$. The first results of this testing can be seen in Figure 57.

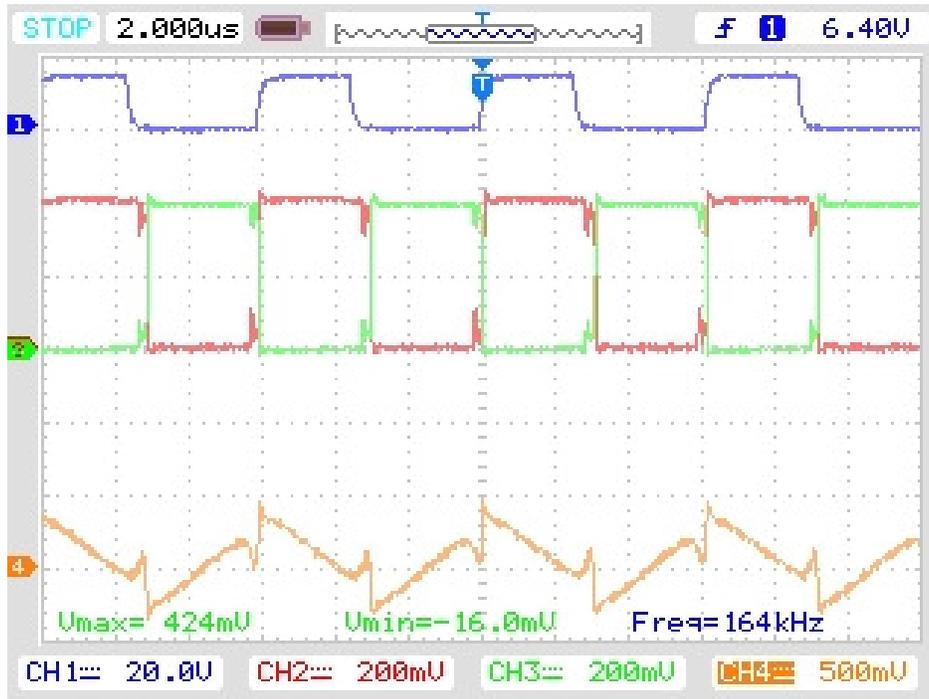


Figure 57. 8X Prototype Converter Waveforms with $V_{in}=10\text{ V}$ (Channel 1: V_{gs} , 20 V/div ; Channel 2: V_{ds} , 10 V/div ; Channel 3: V_{ds} , 10 V/div ; Channel 4: I_{Is} , 5 A/div)

In Figure 57, channel 1 displays the gate-source control signal to half of the MOSFETs (V_{gs}), while channels 2 and 3 show two of the MOSFET's switching voltages (V_{ds}). Channel 4 shows a current waveform, I_{Is} , which is the current passing through the so-called AC node between the half-bridges and the stage capacitors. As can be seen in the above figure, the overall behavior of the converter is, in reality, quite unlike the ideal cases. Instead, simulation has shown that a more complex situation exists where the effects of stray inductance cannot be ignored. Using

capacitances and resistances roughly equal to those within the circuit, along with estimations for the stray inductance, the following current can be simulated.

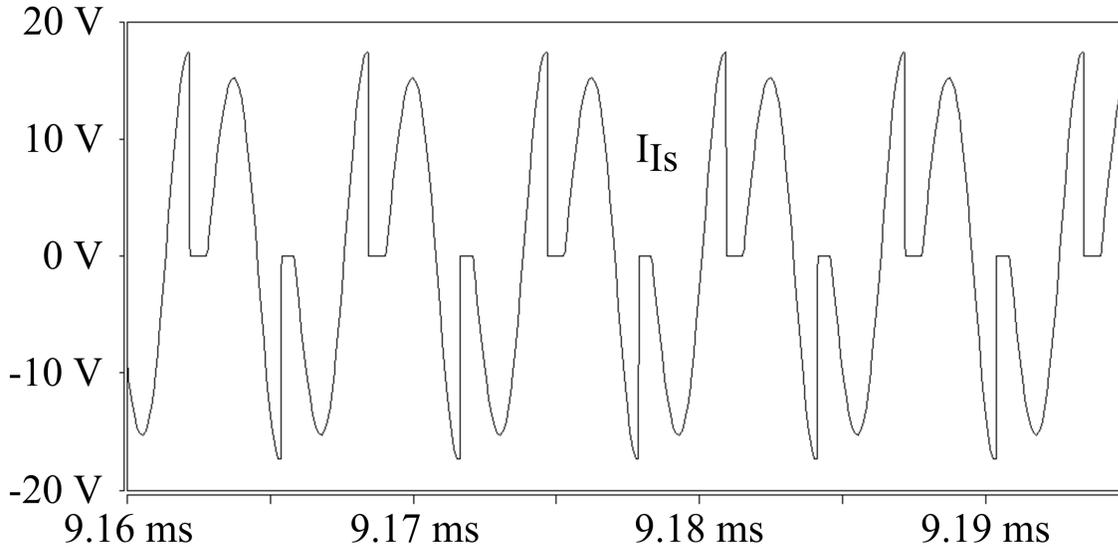


Figure 58. Simulated 8X I_{Is} Current Waveform

To be more specific, the stage capacitors, C_1 , C_2 , C_3 , and C_4 , are $12.9 \mu F$, $11.6 \mu F$, $10.2 \mu F$, and $8.8 \mu F$, respectively; this assumes an input voltage of $20 V$, but that will have little impact on the basic shape of I_{Is} . Using the datasheets for estimations, the capacitors' ESR was $730 \mu\Omega$, and the $60 V$ and $120 V$ MOSFET on-resistances were $1.7 m\Omega$ and $3.6 m\Omega$, respectively. The stray inductance placed at the AC portion of the converter was $10 nH$. In both Figure 57 and Figure 58, the effect of the dead-time can be seen each time the current is forced back to zero, breaking up the otherwise sinusoidal waveform. Despite these results, testing progressed successfully.

At the same operating point as Figure 57, the 8X function was also confirmed, as can be seen in Figure 59 below.

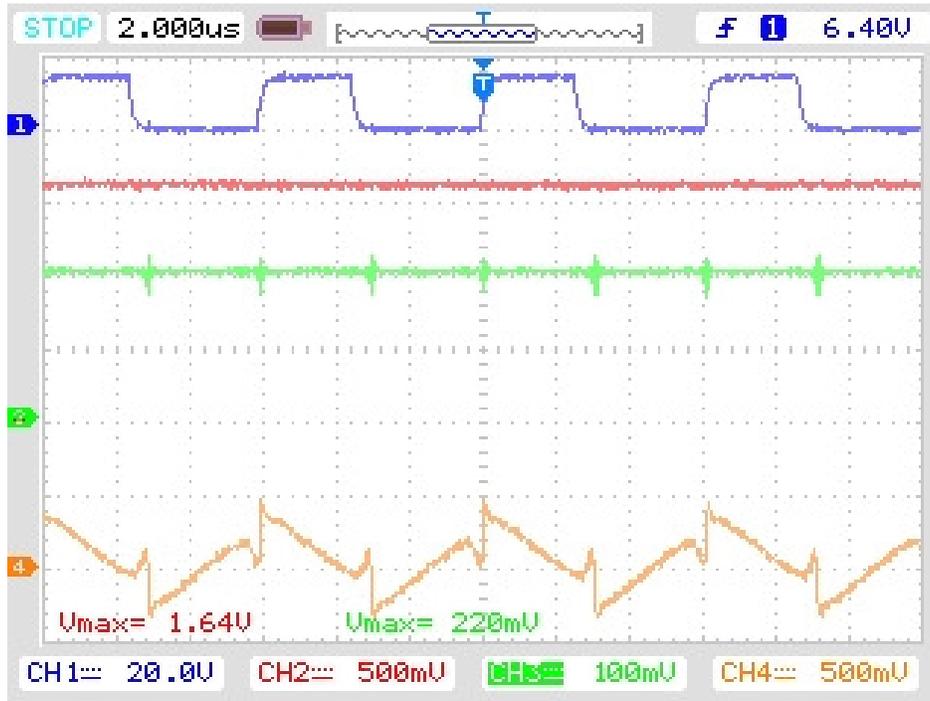


Figure 59. 8X Prototype Converter Waveforms with $V_{in}=10\text{ V}$ (Channel 1: V_{gs} , 20 V/div ; Channel 2: V_{out} , 25 V/div ; Channel 3: V_{in} , 5 V/div ; Channel 4: I_{IS} , 5 A/div)

As expected, the output voltage is very close to being eight times the input voltage. Continuing on, the input voltage was gradually increased in order to confirm the converter's safe operation. In Figure 60, the input voltage was 18 V , while Figure 61 shows the same waveforms with the input increased to 20.4 V , finally entering the nominal operating range. No trouble was encountered, so the voltage was further increased. In Figure 62, the input was increased to 35 V , and the MOSFETs were more closely monitored to ensure that they were still functioning correctly. Continuing this trend, the voltage was raised to 37 V , as seen in Figure 63, where the DC supply's limit was reached, limiting further voltage increases. Nevertheless, no problems were encountered, and the output voltage was measured to be 288 V with the input of 37 V , just slightly lower than the expected 296 V . This small voltage drop is representative of larger losses

experienced at this power level, but it is still good.

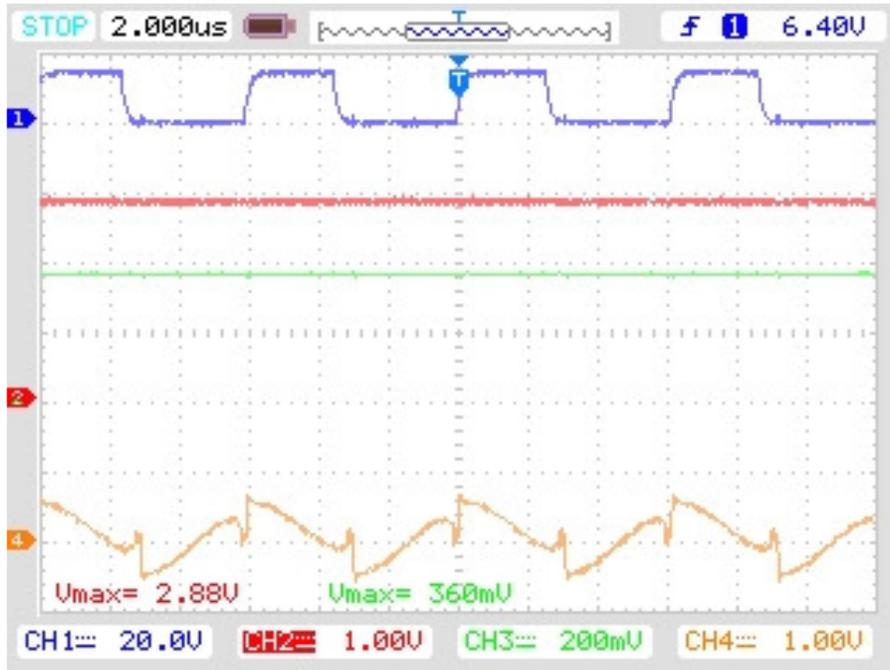


Figure 60. 8X Prototype Converter Waveforms with $V_{in}=18 V$ (Channel 1: V_{GS} , 20 V/div; Channel 2: V_{OUT} , 50 V/div; Channel 3: V_{IN} , 10 V/div; Channel 4: I_{IS} , 10 A/div)

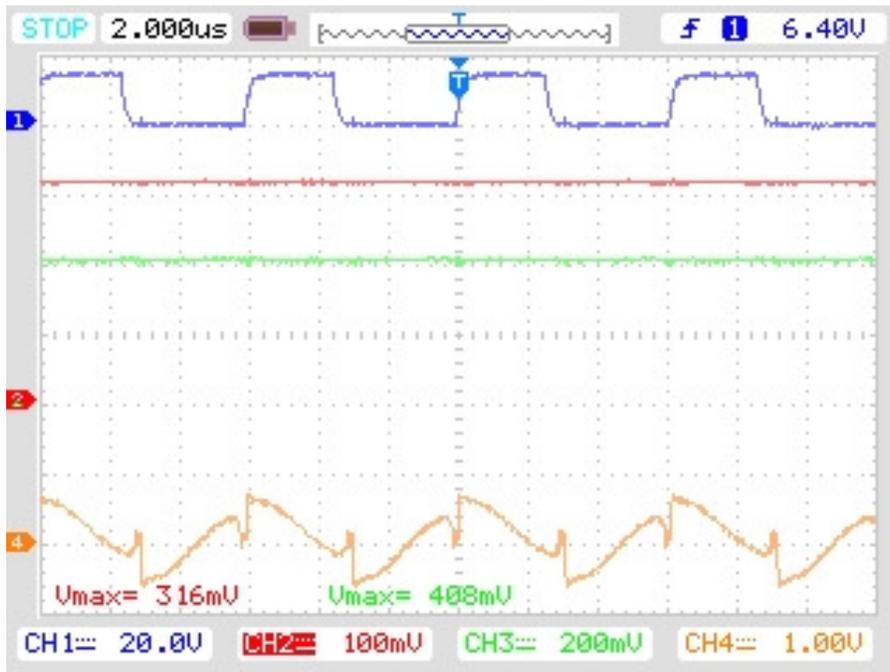


Figure 61. 8X Prototype Converter Waveforms with $V_{in}=20.4 V$ (Channel 1: V_{GS} , 20 V/div; Channel 2: V_{OUT} , 50 V/div; Channel 3: V_{IN} , 10 V/div; Channel 4: I_{IS} , 10 A/div)

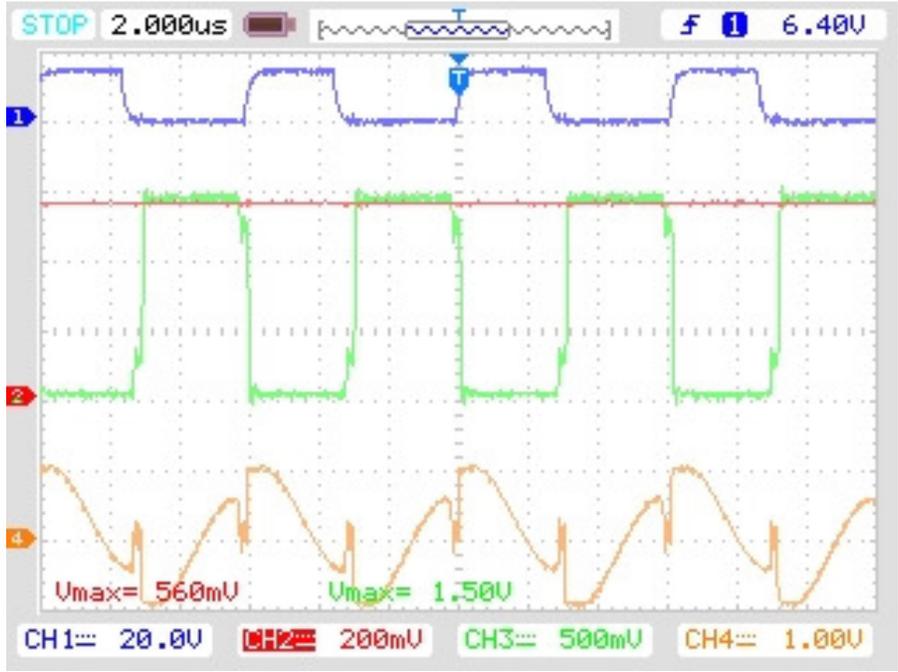


Figure 62. 8X Prototype Converter Waveforms with $V_{in}=35\text{ V}$ (Channel 1: V_{GS} , 20 V/div; Channel 2: V_{OUT} , 100 V/div; Channel 3: V_{DS} , 25 V/div; Channel 4: I_{LS} , 10 A/div)

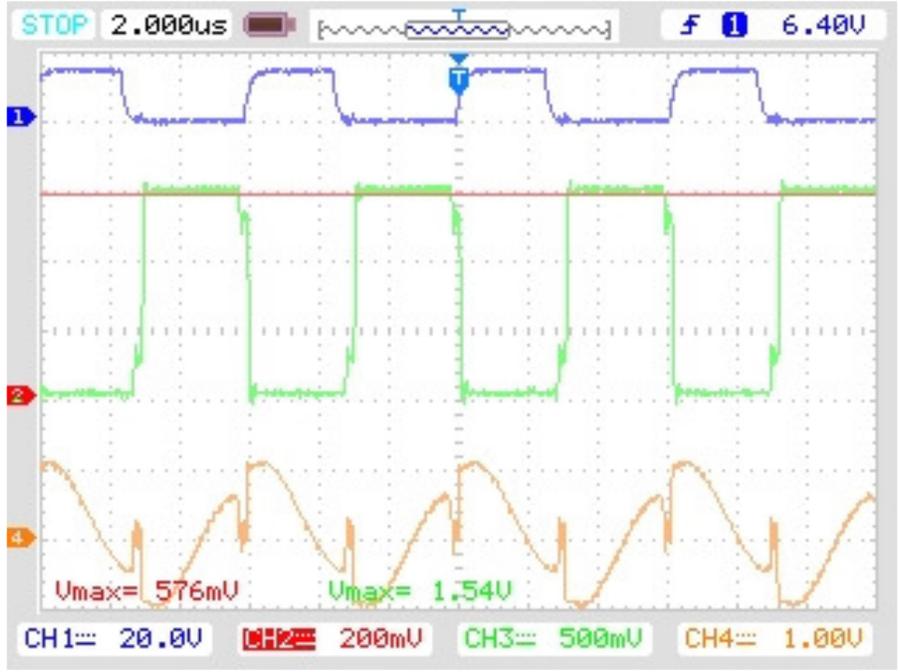


Figure 63. 8X Prototype Converter Waveforms with $V_{in}=37\text{ V}$ (Channel 1: V_{GS} , 20 V/div; Channel 2: V_{OUT} , 100 V/div; Channel 3: V_{DS} , 25 V/div; Channel 4: I_{LS} , 10 A/div)

With the correct operation confirmed, the efficiency of the converter became a concern.

In order to measure the efficiency, two tests were performed, each at a slightly different switching frequency. In this case, the input voltage was held constant at 20 V , while the load resistance was changed. The output power and efficiency were measured at each point using a power meter, and this test was performed at both 156 kHz and 165 kHz . These frequencies are close, but the operating frequency range of the converter was limited by the PWM chip's passive components. The results of the test can be seen in Figure 64.

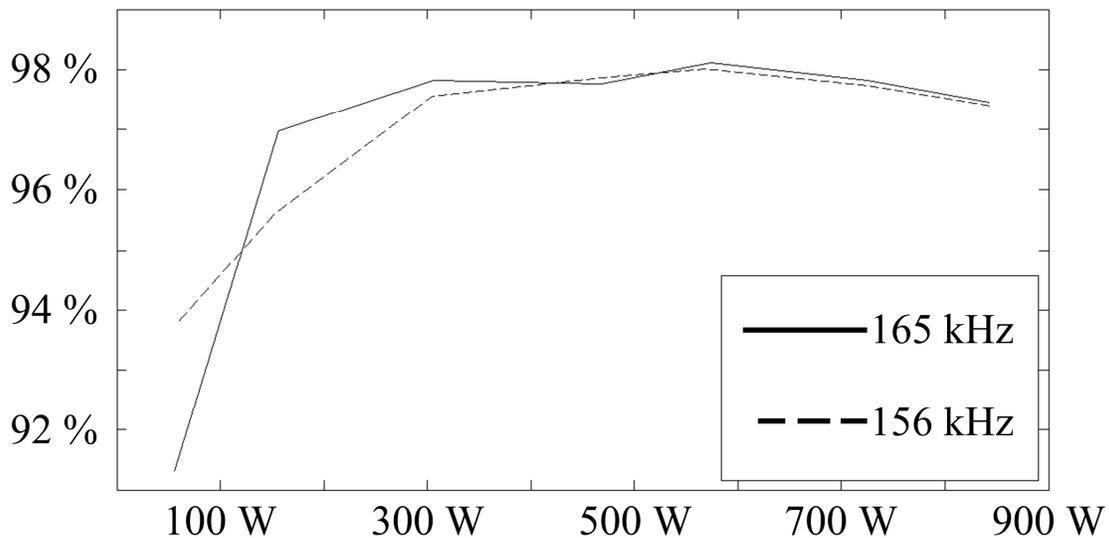


Figure 64. Efficiency vs. Output Power for the 8X Prototype

This curve matches the curve seen in many other similar converters using MOSFETs, starting out low, increasingly rapidly to a maximum, and finally slowly declining with increased power. As can be seen, the two frequencies tested were too close to clearly illustrate the effects of frequency on the efficiency, but it seems likely that the 165 kHz operation is marginally better. This would likely be the result of reduced voltage ripple on the capacitors, reducing the voltage differences between them and lowering the transient currents experienced in the circuit. All things considered, however, the efficiency is fairly high. Efficiencies greater than 98% were

measured at several points during testing, confirming the converter's viability as a candidate for use in high-temperature environments requiring both high efficiency and small size.

4. Conclusions

In the end, it is important to consider the system under consideration once again. When the power produced by a photovoltaic panel must be conditioned for use in other applications, such as the one described in Figure 1, several issues must be considered. First, the PV panel's voltage must be boosted and inverted, but many options are available to accomplish this. The traditional boost and isolated full-bridge converters could boost and regulate the panel's voltage for use by the inverter, but they cannot achieve a very high boost ratio and their magnetic components not only increase their size and weight but also limit their temperature operation range. In order to achieve the desired high voltage gain, efficiency and power density, switched capacitor topologies represent an attractive option. While not really capable of regulating the DC voltage fed to the inverter, the inverter itself could be adjusted via its modulation index to achieve the desired AC output. As was shown, the flying capacitor converter had a low number of active devices, but it was not modular, has efficiency that is inversely related to the boost factor, and has a relatively complicated control scheme. On the other hand, the MMCCC is modular, has a simple control scheme, and has an efficiency not affected by the boost factor, but it requires more devices for a given voltage gain and some of those switches need to sustain greater voltage stresses. In order to overcome these negative aspects, the NX dc-dc converter was developed.

The NX converter has many of the advantages of its relatives, but only a few of the drawbacks. It is a modular design, making it easy to increase the boost factor. The control is also simple, just using a complementary 50% duty cycle to control all of the semiconductors

involved. While nearly half of the active devices do have to be able to sustain twice the input voltage, the overall switch count has been reduced to the same as the flying capacitor topology. Finally, the charge paths have a maximum of three active devices, limiting the resistive losses and eliminating any dependency of the efficiency on the boost factor like the flying capacitor converter. These features combine to make the NX converter well-suited for use as a micro-converter in PV systems.

BIBLIOGRAPHY

BIBLIOGRAPHY

- [1] Mitsubishi Electric, “MJT Series,” L-175-1-B8778-C datasheet, Jul. 2011 [Revised Mar. 2012].
- [2] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics: Converters, Applications, and Design*. New York, NY: John Wiley & Sons, Inc., 1995, pp. 172-178.
- [3] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. New York, NY: Springer Science + Business Media, LLC, 2001, pp. 149-167.
- [4] F. Z. Peng, F. Zhang and Z. Qian, “A novel compact dc-dc converter for 42 V systems,” in *IEEE 34th Annual Power Electronics Specialist Conference*, 2003, pp. 33-38.
- [5] F. Zhang, F. Z. Peng and Z. Qian, “Study of the multilevel converters in dc-dc applications,” in *IEEE 35th Annual Power Electronics Specialist Conference*, 2004, pp. 1702-1706.
- [6] Z. Pan, F. Zhang and F. Z. Peng, “Power losses and efficiency analysis of multilevel dc-dc converters,” in *Twentieth Annual IEEE Applied Power Electronics Conference and Exposition*, 2005, pp. 1393-1398.
- [7] W. Qian, F. Z. Peng, M. Shen and L. M. Tolbert, “3X dc-dc multiplier/divider for HEV systems,” in *Twenty-Fourth Annual IEEE Applied Power Electronics Conference and Exposition*, 2009, pp. 1109-1114.
- [8] W. Qian, H. Cha, F. Z. Peng and L. M. Tolbert, “55-kW variable 3X dc-dc converter for plug-in hybrid electric vehicles,” *IEEE Transactions on Power Electronics*, vol. 27, no. 4, Apr., pp. 1668-1678, 2012.
- [9] F. H. Khan and L. M. Tolbert, “A multilevel modular capacitor clamped dc-dc converter,” in *Conference Record of the 2006 IEEE Industry Applications Conference*, 2006, pp. 966-973.
- [10] F. H. Khan and L. M. Tolbert, “5 kW multilevel dc-dc converter for hybrid electric and fuel cell automotive applications,” in *Conference Record of the 2007 IEEE Industry Applications Conference*, 2007, pp. 628-635.
- [11] F. H. Khan and L. M. Tolbert, “A multilevel modular capacitor clamped dc-dc converter,” *IEEE Transactions on Industry Applications*, vol. 43, no. 6, Nov.-Dec., pp. 1628-1638, 2007.
- [12] D. Cao and F. Z. Peng, “Zero-current-switching multilevel modular switched-capacitor dc-dc converter,” in *IEEE Energy Conversion Congress and Exposition*, 2009, pp. 3516-3522.

- [13] D. Cao and F. Z. Peng, "A family of zero current switching switched-capacitor dc-dc converters," in *2010 Twenty-Fifth Annual IEEE Applied Power Electronics Conference and Exposition*, 2010, pp. 1365-1373.
- [14] D. Cao and F. Z. Peng, "Multiphase multilevel modular dc-dc converter for high current high gain TEG application," in *2010 IEEE Energy Conversion Congress and Exposition*, 2010, pp. 4230-4237.
- [15] F. Z. Peng, "A generalized multilevel inverter topology with self voltage balancing," *IEEE Transactions on Industry Applications*, vol. 37, no. 2, Mar.-Apr., pp. 611-618, 2001.
- [16] International Rectifier, Appl. Note AN-1084, pp. 1-13.
- [17] Y. Xiong, S. Sun, H. Jia, P. Shea and Z. J. Shen, "New physical insights on power MOSFET switching losses," *IEEE Transactions on Power Electronics*, vol. 24, no. 2, Feb., pp. 525-531, 2009.
- [18] W. Qian, D. Cao, J. Cintron-Rivera, M. Gebben, D. Wey and F. Z. Peng, "A switched-capacitor dc-dc converter with high voltage gain and reduced component rating and count," *IEEE Transactions on Industry Applications*, vol. 48, no. 4, Jul.-Aug., pp. 1397-1406, 2012.
- [19] M. Gebben, J. G. Cintron-Rivera, W. Qian, D. Cao, X. Pei and F. Z. Peng, "A zero-current-switching multilevel switched capacitor dc-dc converter," in *2011 IEEE Energy Conversion Congress and Exposition*, 2011, pp. 1291-1295.