MODULARIZED MULTILEVEL AND Z-SOURCE POWER CONVERTER AS RENEWABLE ENERGY INTERFACE FOR VEHICLE AND GRID-CONNECTED APPLICATIONS

By

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ABSTRACT

MODULARIZED MULTILEVEL AND Z-SOURCE POWER CONVERTER AS RENEWABLE ENERGY INTERFACE FOR VEHICLE AND GRID-CONNECTED APPLICATIONS

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Due the energy crisis and increased oil price, renewable energy sources such as photovoltaic panel, wind turbine, or thermoelectric generation module, are used more and more widely for vehicle and grid-connected applications. However, the output of these renewable energy sources varies according to different solar radiation, wind speed, or temperature difference, a power converter interface is required for the vehicle or grid-connected applications.

Thermoelectric generation (TEG) module as a renewable energy source for automotive industry is becoming very popular recently. Because of the inherent characteristics of TEG modules, a low input voltage, high input current and high voltage gain dc-dc converters are needed for the automotive load. Traditional high voltage gain dc-dc converters are not suitable for automotive application in terms of size and high temperature operation. Switched-capacitor dc-dc converters have to be used for this application. However, high voltage spike and EMI problems exist in traditional switched-capacitor dc-dc converters. Huge capacitor banks have to be utilized to reduce the voltage ripple and achieve high efficiency. A series of zero current switching (ZCS) or zero voltage switching switched-capacitor dc-dc converters have been proposed to overcome the aforementioned problems of the traditional switched-capacitor dc-dc converters. By using the proposed soft-switching strategy, high voltage spike is reduced, high EMI noise is restricted, and the huge capacitor bank is eliminated. High efficiency, high power density and high temperature switched-capacitor dc-dc converters could be made for the TEG

interface in vehicle applications. Several prototypes have been made to validate the proposed circuit and confirm the circuit operation.

In order to apply PV panel for grid-connected application, a low cost dc-ac inverter interface is required. From the use of transformer and safety concern, two different solutions can be implemented, non-isolated or isolated PV inverter. For the non-isolated transformer-less solution, a semi-Z-source inverter for single phase photovoltaic systems has been proposed. The proposed semi-Z-source inverter utilizes only two switching devices with doubly grounded feature. The total cost have been reduced, the safety and EMI issues caused by the high frequency ground current are solved. For the transformer isolated solution, a boost half-bridge dc-ac micro-inverter has been proposed. The proposed boost half-bridge dc-dc converter utilizes only two switching devices with zero voltage switching features which is able to reduce the total system cost and power loss.

Dedicated to:
my wife, Ying Ding
and our unborn baby

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1
Introduction and Motivation

Due the energy crisis and increased oil price, renewable energy sources are used more and more widely for automotive and residential application.

Thermoelectric generation (TEG) modules are solid state energy conversion device that can convert the temperature gradient into electricity or vise versa. TEG has quiet, compact, harsh environmental tolerance features; it has been used in deep space satellite application for many years. The cost and the thermo energy conversion efficiency are the major barriers that limit its application. The energy conversion efficiency of TEG modules has been increased significantly due to the newly developed materials recently. Therefore, utilizing TEG modules in hybrid electric vehicle has drawn more attentions of automotive industry recently. However, to utilize TEG modules in the automotive industry, several challenges need to be solved. Because of the inherent low output voltage and high output current characteristics of high efficient TEG modules, special dc-dc converter interface is required for the automotive applications such as battery charging. This dissertation will first concentrate on proposing and developing a high efficiency, high power density, high input current, high voltage gain step-up dc-dc converter as the interface circuit for TEG modules in automotive application.

Photovoltaic (PV) cells are also solid state energy conversion device than can convert the sun radiation into electricity. The output voltage and power of PV panel will change according to the sun radiation and temperature. In order to apply PV panel for residential application, a low cost dc-ac inverter interface is required. For the traditional full bridge inverter, the total device cost is relatively high, and the ground current caused by the parasitic capacitance of PV panel will cause

safety and EMI issue. Therefore, a low cost PV inverter with doubly grounded features is necessary for residential application. This dissertation will then concentrate on proposing and developing a semi-Z-source inverter for single phase photovoltaic systems. The proposed semi-Z-source inverter utilizes only two switching devices with doubly grounded features, which is appropriate for residential application. This semi-Z-source inverter can also be used as a dc-dc converter for dc motor drive and zero voltage electronic load.

The following discussion starts with the background information introduction of TEG modules, literature review of the traditional step-up dc-dc converters and their application limits for the automotive application, conventional switched-capacitor dc-dc converters for automotive applications, and their limitations. [1]

1.1 Background

1.1.1 TEG Modules Basic Structures and Potential Automotive Applications

Thermoelectric modules (thermoelectric devices) are solid state devices that can convert thermal energy from a temperature gradient into electric energy as power generators or vice versa (convert electrical energy into a temperature gradient across the modules) for cooling

[1] This chapter was presented in part at the 39th IEEE Power Electronics Specialists Conference, Island of Rhodes, Greece, Jun.15-19, 2009

applications [1]. Unlike the thermocouples used for temperature measurement, the TEG modules can generate enough electricity for many applications [2]. Compared to other energy conversion methods, TEG modules are reliable without any noise or vibration and are attracting more attention as renewable energy sources where temperature gradients are available. Because of the low efficiency and cost issues, previously the TEG modules have been restricted to special applications, such as powering the onboard electronics of a satellite in deep space, and providing electricity from nuclear heat for a submarine in deep waters [3, 4]. Recently, due to environmental concern and global warming issues, TEG modules have received more attention as a method to convert wasted heat to electricity. For example, converting the waste heat from the exhausting pipe of antomobiles to power accessory electric loads such as air condioner in a vehicle or put the energy back to the wheel to increase efficiency [3, 4]. Many new materials have also been developed to increase the heat to electricity conversion efficiency of TEG modules [5-7].

Thermoelectric modules consist of *p*-type and *n*-type semiconductors connected electrically in series and thermally in parallel as shown in Figure 1.1 and Figure 1.2 [8]. Figure 1.1(a) shows a *pn* module used for cooling applications while (b) shows the same device being used for power generation. By the Seebeck effect, heat flow through this thermoelectric material will tend to move the charge carriers in the same direction as the heat flow. As shown in Figure 1.2, TEG modules for power generation usually consist of an array of 2N pellets (n- and p- type semiconductor thermoelements) that make up N thermoelectric couples thermally in parallel and electrically in series to achieve high output voltage and high power [8]. Usually these pellets are connected by high conductive metal strips and sandwiched between thermal conducting while

electrically insulating metalized ceramic plates. The pellets, tabs and substrates thus form a layered assembly, which is shown in the Figure 1.3 [9].

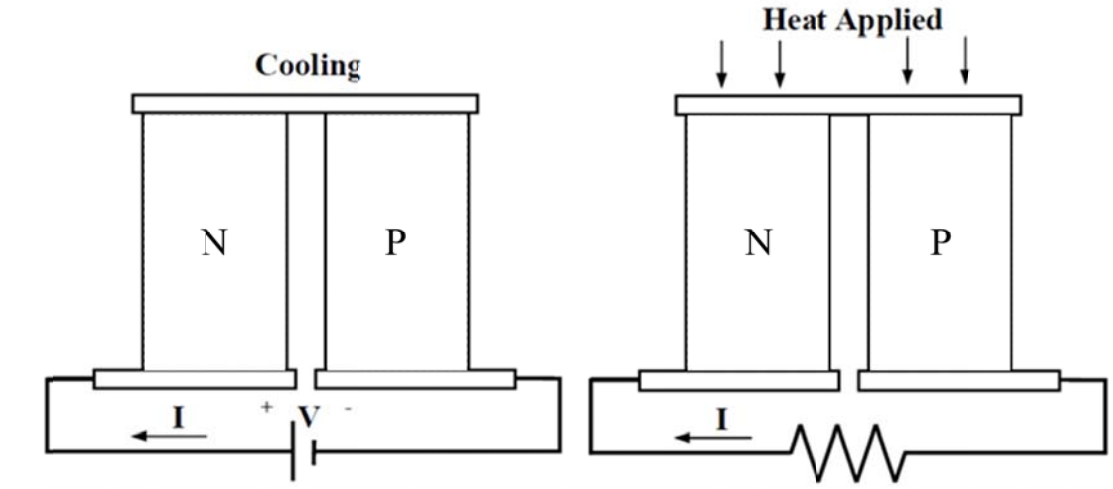


Figure 1.1 PN Thermoelectric modules. (a) Cooling applications. (b) Power generation.

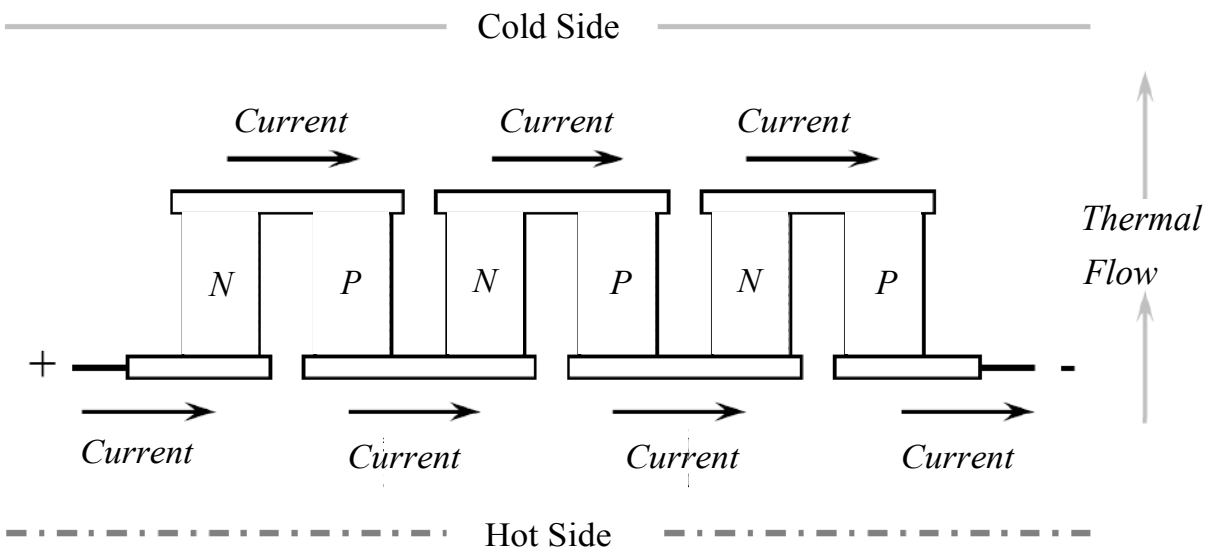


Figure 1.2 TEG module configuration.

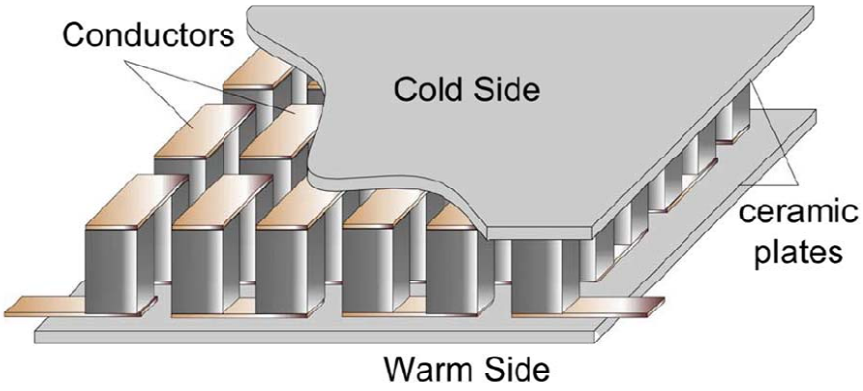


Figure 1.3 Typical TEG module assembly.

(For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this dissertation)

By adding TEG modules around the car exhausting pipe, the waste heat energy can be converted into electricity shown in Figure 1.4 The new developed materials for TEG modules has about 10% electricity conversion efficiency, which means 10% waste heat energy can be converted into electricity. In this case, more than 5% of fuel can be saved. The generated electricity by the TEG modules is around 500 W~ 1kW in some big truck. And this depends on how many TEG modules are put around the exhausting pipe.

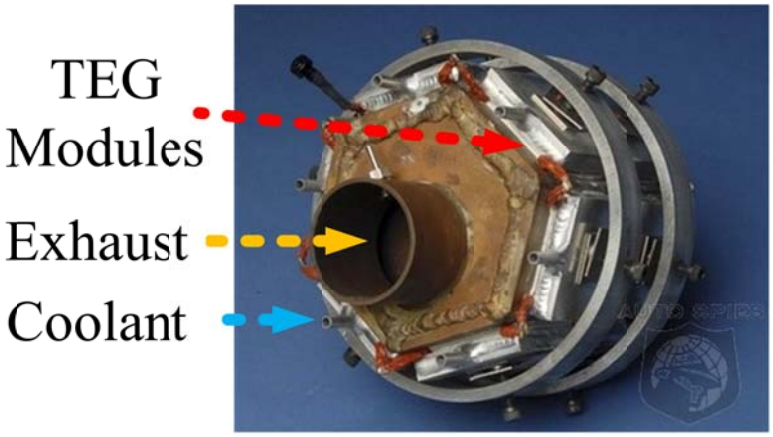


Figure 1.4 TEG modules around the exhausting pipe

1.1.2 TEG Modules Electrical Characteristics

In order to apply TEG modules to automotive application, electrical characteristics of TEG modules has to be modeled.

At present, the power conditioning technology was majorly based on the high frequency switching DC-DC converter design, with high frequency (50 KHz~1 MHz) switching device (MOSFET, IGBT etc.) used. So the high frequency characteristics and dynamic response of TEG module are becoming major concerns in the outside power conditioning circuit design. In order to design a suitable switching dc-dc converter special for the TEG module usage, the high frequency electrical characteristics of TEG module in steady state and in transient procedure have to be known. In the following parts, a method will be proposed to test the TEG module outside electrical characteristics in steady state and in transient procedure, and a high frequency electrical model will be put forward to help design the switching power supply DC-DC converter.

To characterize TEG modules, a heat exchanger capable of outputting 100 W electrical power was designed and fabricated. Figure 1.5 shows the decomposed structure of the heat exchanger. Heat elements are distributed evenly within the hot plate to generate a uniform hot side temperature. A total of twenty TEG modules, G1-1.4-219-1.14, from Tellurex Corp. shown in Figure 1.6 [10], are installed on both sides of the hot plate, ten pieces on the top of the hot plate and ten pieces on the bottom of it. Two radiators are clamped on both sides to cool the TEG modules' cold surface. When a temperature gradient exists between the hot plate and the radiator, electric power is generated by the TEG modules as a result of heat flow through them. Thermal couple was used as temperature sensor that was installed in the hot plate and the heat sink to monitor the temperature between hot side and cold side during the tests.

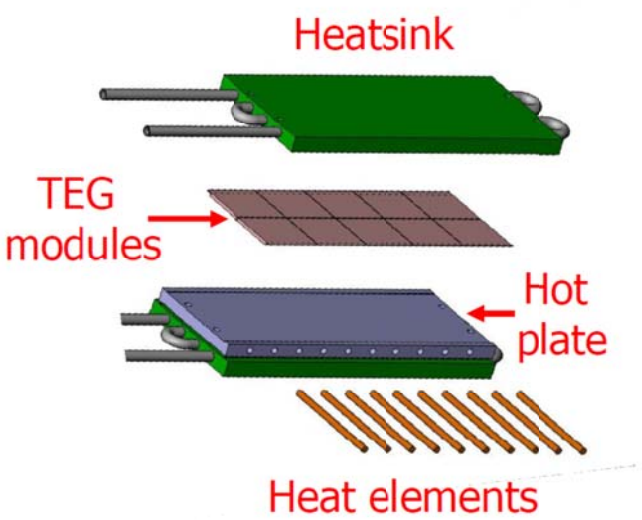


Figure 1.5 Heat exchanger configurations

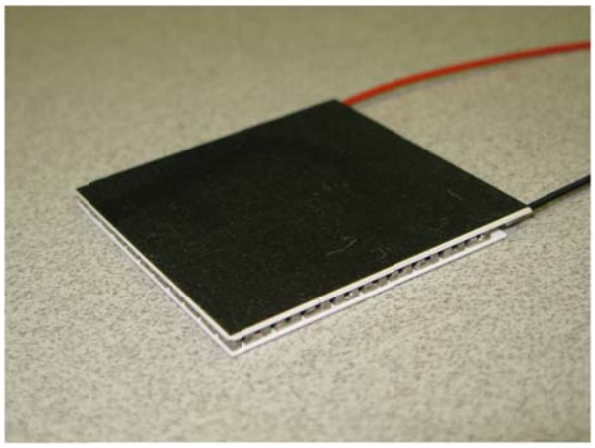


Figure 1.6 One TEG module G1-1.4-219-1.14 from Tellurex Corp

Figure 1.7 shows the TEG module heating and testing system flowchart. And this system was used to measure the steady-state and dynamic response of TEG modules. By taking advantage of thermo-coupler as the temperature sensor, a temperature PID controller can be used to adjust a solid state contactor to control the power flow from the AC power supply to the heating elements of the TEG modules. And in this way, the temperature of the hot plate accurately controlled. By using this temperature close loop control, stable hot plate temperature could be achieved when the steady state and dynamic response of TEG modules are tested.

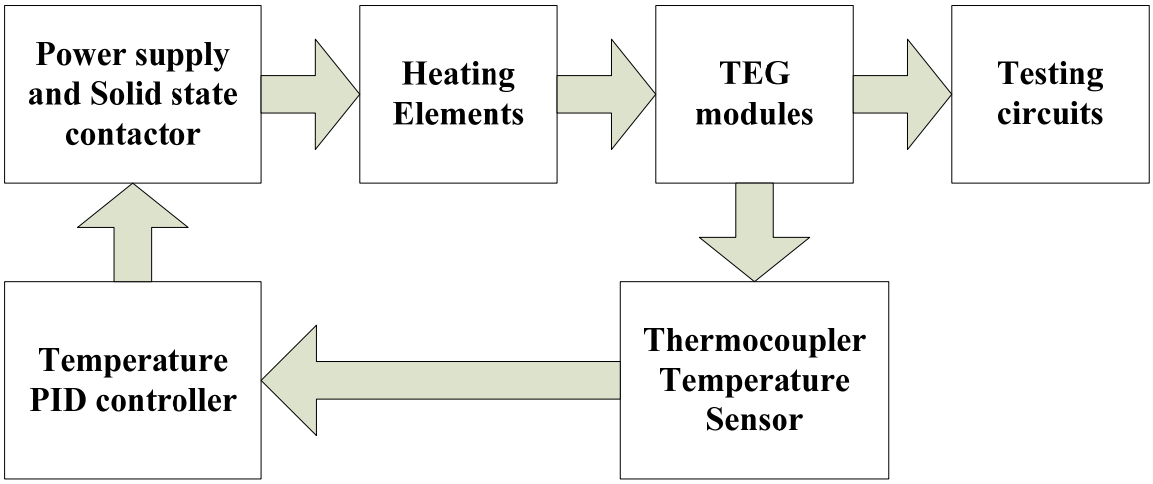


Figure 1.7 TEG module heating and testing system

Figure 1.8 shows the measured steady-state electrical output characteristics of a single TEG module. Three thermal conditions were tested and the V-I curves are plotted. During tests, the heat exchanger hot plane temperature is controlled to 150°C, 115°C, 79°C; the heatsink temperature are 27°C, 29°C, and 31°C, respectively. From the three curves shown in Figure 1.8, the internal resistances of the TEG modules under those thermal conditions are calculated and are 3.5Ω, 3.9Ω, and 4.2Ω, respectively. The maximum power output of a single module at 150 °C is about 4.5 W. From the plotted V-I curve of the TEG module, the TEG module can be modelled as a ideal voltage source with internal resistance shown in Figure 1.9

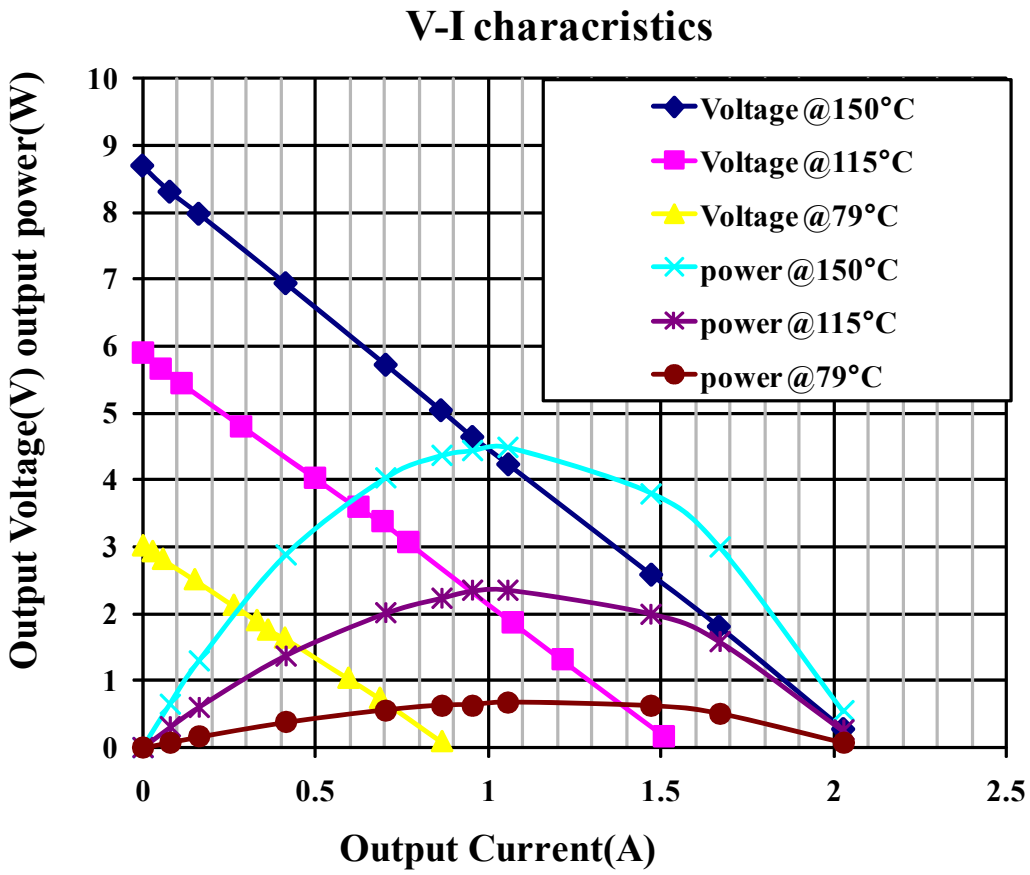


Figure 1.8 TEG module steady-state testing results

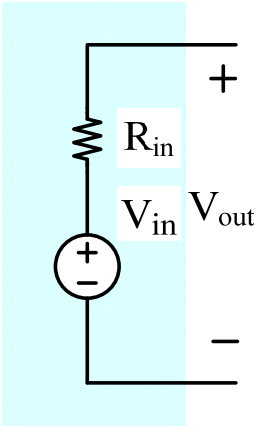


Figure 1.9 Electrical equivalent circuit of one TEG module.

Figure 1.10 shows the test circuit of the electrical characteristics of the TEG module's dynamic behaviors. Figure 1.11 shows the captured single TEG module output voltage and

current waveforms. Test results reveal that the TEG module has a very fast dynamic response and it will not influence the converter design. Because the TEG module output current can increase in the range of nanoseconds and the switching speed of DC-DC converter is usually in the range of 50K~1MHz, the switching period will be 1us~20us. So, the ideal voltage source with the internal resistance model can represent the TEG steady state and dynamic model very well.

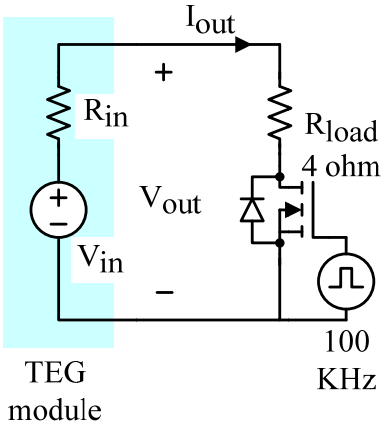


Figure 1.10 TEG module dynamic test circuit

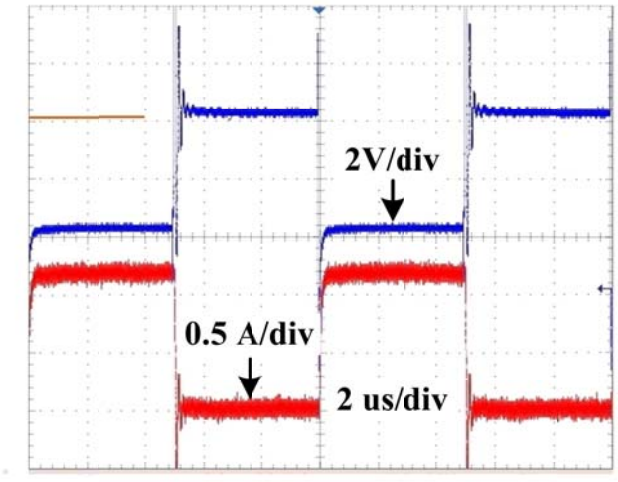


Figure 1.11 TEG module output waveforms

1.2 Power Electronic Challenges for TEG

Initially, the TEG module output voltage and power will change distinctly with the temperature gradient, which means it cannot output stable voltage or constant current. In order to utilize the TEG modules as the power source, a power conditioning circuit as interface between the TEG module and loads is needed. In order to solve this problem, the electrical characteristic of the TEG module should be modeled for circuit anaylsis and design. Some modeling method has been previously proposed [11]. Some DC-DC converter circuits have been investigated to output stable voltage and improve the TEG module power condition for more applications [12, 13]. And some control methods such as Maximum Power Point Tracking (MPPT) and constant voltage control have also been investigated to apply to the TEG module [14]. The TEG modules have also been used for battery charging applications reported in [15].

Moreover, due to the inherent characteristics of the materials making TEG modules, bigger pellets with larger heat conduction areas can produce high output current with the same output voltage compared to the smaller pellets with smaller conduction areas [5, 7, 8]. At the same time, by using the same amount of materials to manufacture TEG modules, it is much easier to manufacture bigger pellets. That means, in order to output the same amout of power, it is much easier to produce a TEG module with low output voltage and high output current than a low output current and high output voltage version. The reliability and the total heat-electricity conversion efficiency of the high output current and low output voltage module is also much higher than the low output current and high output voltage version, because the latter one needs more small pellets in series. By putting more pellets in series means more electric connectors are needed, which will cause the increase of the internal resistance of the whole TEG module, and the reliability of the whole module will also reduce accordingly. Therefore, the low output voltage with high output current TEG modules are preferred in the manufacturing process and

application. And this features add special challenges to the power electronics interface circuit design. Following provides the power electronics circuit reqirements for the TEG module interface and some challenges in the circuit design for automotive application:

TEG module interface circuit reqirements:

- Maximum power point tracking control
- Constant output voltage or current control

TEG module interface circuit design challenges for automotive application

- Low input voltage
- High input current
- High voltage conversion ratio
- High temperature operation
- High efficiency
- Small size

Among these challenges, the low input voltage, high input current, and high voltage conversion ratio are the requirements from TEG modules, and high temperature operation and small size are the features preferred by the automotive application. And high efficiency is always a preferred feature.

In order to meet all these requirements, traditional step-up dc-dc converter with a transformer or coupled inductor for high voltage conversion ratio applications are reviewed in the following discussions. Switched-capacitor dc-dc converter topologies for the automotive application are also summarized; drawbacks of each circuit are addressed.

1.3 Summary of Previous Works

1.3.1 Traditional Step-up DC-DC Converter

Traditional step-up dc-dc converter utilizes the inductor charging and discharging to boost the voltage. We will discuss the basic step-up circuit topology from the very beginning to the improvements of them proposed recently.

1.3.1.1 Boost dc-dc converter

Figure 1.12 shows the traditional boost dc-dc converter. There are several benefits of the traditional boost converter. The structure of the traditional boost converter is simple. There are only one switch S, one diode D_o, one inductor L, and one capacitor C_o. The control and gate drive of this circuit is also very simple, only one switch needs to be controlled and gate drive shares the same ground with the input voltage source. The input current ripple is small; the total cost of the circuit is also relatively low. Because of these good features of traditional boost circuit, it has more and more applications in normal dc-dc step-up applications with voltage gain less than three and power factor correction (PFC) circuit [16, 17].

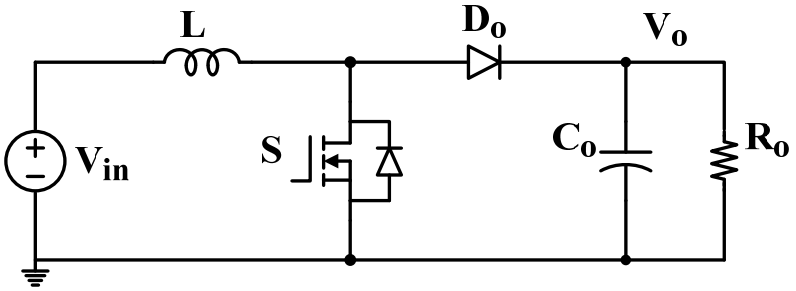


Figure 1.12 Traditional boost dc-dc converter.

Theoretically, the traditional boost dc-dc converter has infinite voltage gain, but considering the internal resistance of switch and inductor, the voltage gain of the boost converter is limited [18]. Figure 1.13 shows the boost converter circuit configuration considering the internal resistance of the inductor R_L. Actually, R_L is also can be considered as the whole circuit power

loss equivalent resistance. By considering the internal resistance of the boost converter, the new voltage gain can be expressed as follows:

$$V_{gain} = \frac{V_o}{V_{in}} = \frac{1}{(1-D)(1+\frac{R_L}{R_o(1-D)^2})} \tag{1.1}$$

Figure 1.14 shows the voltage gain curve vs. duty cycle considering the internal equivalent resistance describe as equation (1.1). With the increase of the equivalent resistance to the load resistance ratio, the voltage gain of the boost converter reduced accordingly. When the $R_L / R_o = 0.01$,which means the total power loss of the converter is 1%, the boost converter can achieve five times voltage gain. In the real application, the equivalent resistance is usually larger the 1%, which means for a regular boost converter, it is nearly impossible to achieve a voltage gain higher than five.

In order to solve the hard switching problem of the traditional boost converter and reduce the switching loss and solve the reverse recovery problem of the diode. Some soft switching strategies have been proposed [19-23]. Adding an active clamp circuit or passive clamp circuit to achieve the soft switching of the main switch can reduce the switching loss and improve the converter efficiency. The diode reverse recovery current is also restrained effectively. But these improvements are only for the boost converter in regular applications. The voltage gain of these converters is not improved.

Moreover, if the power rating of the boost converter is increased, or if the input current rating is increased, a huge inductor with high current rating has to be used; more devices have to be put in parallel to meet the current rating requirements. However, because of the negative temperature coefficient of the diode and IGBT, when many devices are paralleled together, the current will not equalize with each other. Some of the devices may flow more and more current than others

until burn out. Therefore, In order to increase the input current rating of the boost converter, interleaving strategy has to be used.

1.3.1.2 Interleaved boost dc-dc converter

Interleaved boost dc-dc converter are proposed to increase the input current rating and power rating of the boost converter [24-31]. Figure 1.15 shows the two-phase interleaved boost dc-dc converter with higher input current rating. By the interleaving several phase of boost converter together, the current can be shared with each phase equally automatically, the input current ripple could also be reduced significantly. The converter dynamic response could be increased. The input inductor size could also be reduced accordingly [29, 32-35]. Figure 1.16 shows ripple reduction effect as a function of duty cycle [34]. For an N-phase boost dc-dc converter, the current ripple cancellation effect K_I can be qualified as:

$$K_I = \frac{\Delta I_L}{\Delta I_{LS}} = \frac{N(D - \frac{m}{N})(\frac{m+1}{N} - D)}{D(1-D)} \tag{1.2}$$

where $m = floor(ND)$ is the maximum integer that does not exceed the ND. N is the number of phase interleaved together, and D is duty cycle. At some of the duty cycle point, the current ripple of multi-phase boost converter can be eliminated.

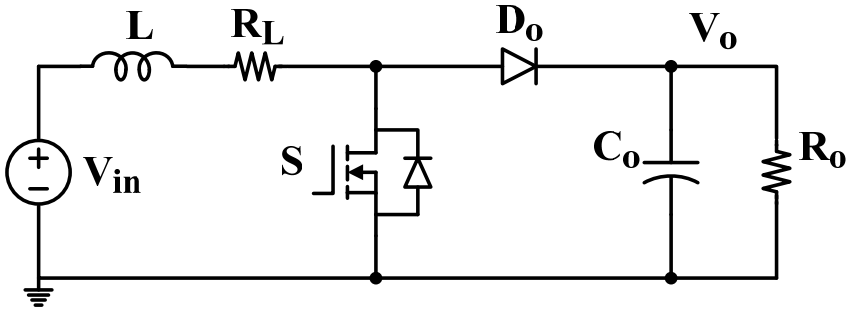


Figure 1.13 Boost converter considering internal resistance.

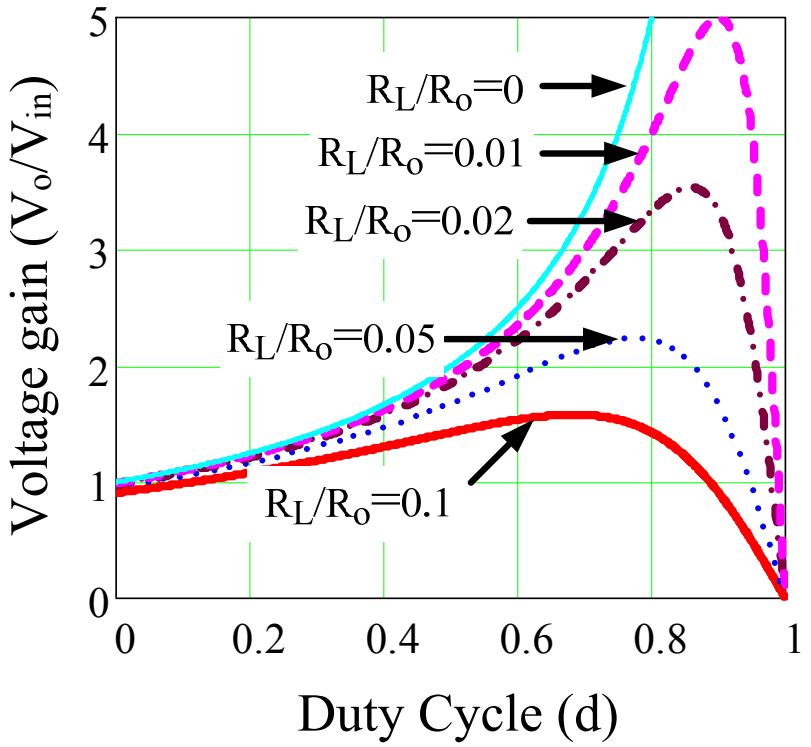


Figure 1.14 Voltage gain vs. duty cycle considering power loss.

For a traditional boost dc-dc converter, the current ripple can be expressed by:

$$\Delta I_{LS} = \frac{V_{in} D}{L f_S} \tag{1.3}$$

where V_{in} is the input voltage, L is the inductance value, f_S is the switching frequency and ΔI is the current ripple. The current ripple is poor when a very large duty cycle is present. The large duty cycles further increase the input current ripples by increasing the individual inductor current ripples, as can be seen from equation (1.3). Substituting equation (1.3) into equation (1.2) , the magnitude of the output current ripples for multiphase boost converters can be easily derived, as follows:

$$\Delta I_L = K_I \Delta I_{LS} = \frac{V_{in}}{L f_S} \frac{D(1-\frac{m}{N})(\frac{m+1}{N} - D)}{D(1-D)} \tag{1.4}$$

By setting $\frac{V_{in}}{Lf_S}$ equal to 1, we can derive the normalized input current ripple equation. Figure 1.17 shows the relationship of normalized input current ripple curve with duty cycle and number of phase interleaved in equation (1.4). It can be shown from the curve that, even for the four-phase interleaved boost dc-dc converter, the best operation point is around 0.75 duty cycle. When the duty cycle is increased for the high voltage gain application, the input current ripple will increase accordingly. And the benefits of the interleaved strategy will disappear too. Besides, for the traditional interleaved boost dc-dc converter, the main switches still switch with hard switching, the switching loss of the main switch is still quite huge, and the diode also have sever reverse recovery problem. And the efficiency of the whole converter is low.

In order to increase the efficiency of the interleaved boost dc-dc converter, reduce the switching loss and solve the voltage spike problem of the diode caused by the diode reverse recovery. Some soft-switching strategy has been proposed [36].

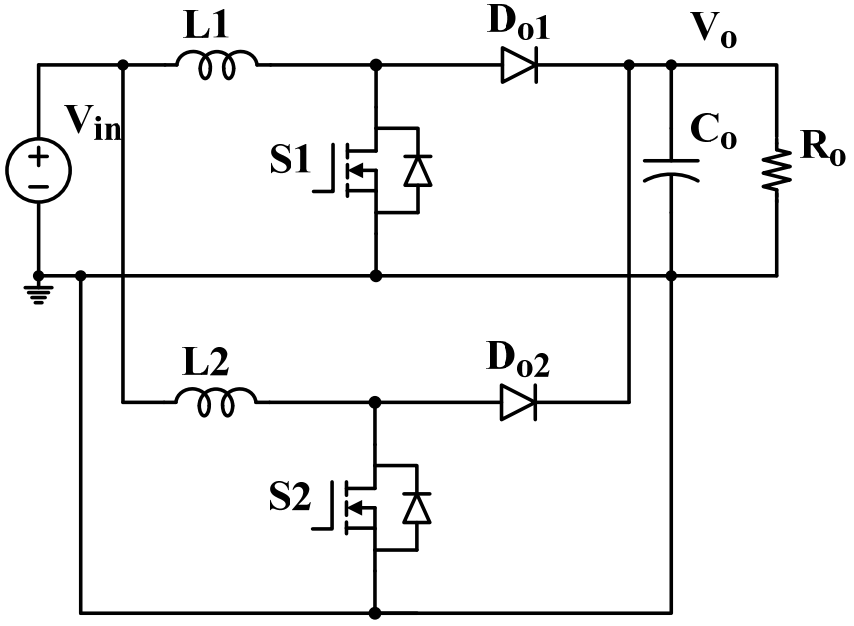


Figure 1.15 Two-phase interleaved boost dc-dc converter.

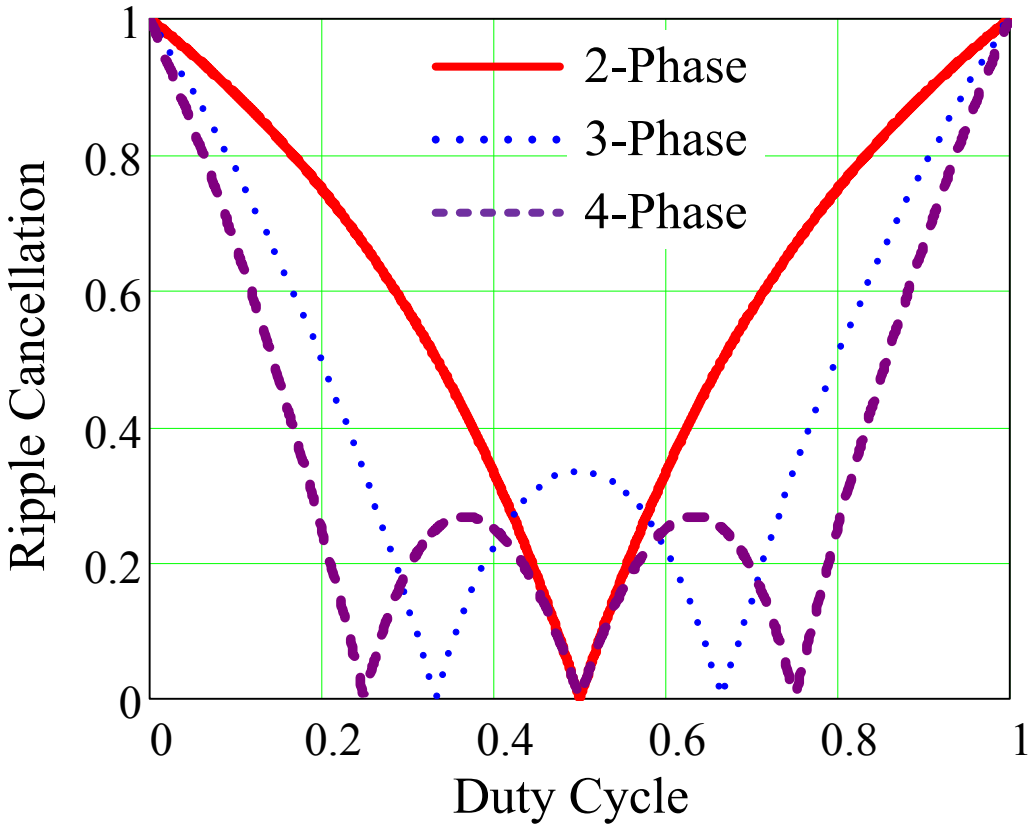


Figure 1.16 Current ripple cancellation in multiphase boost converters.

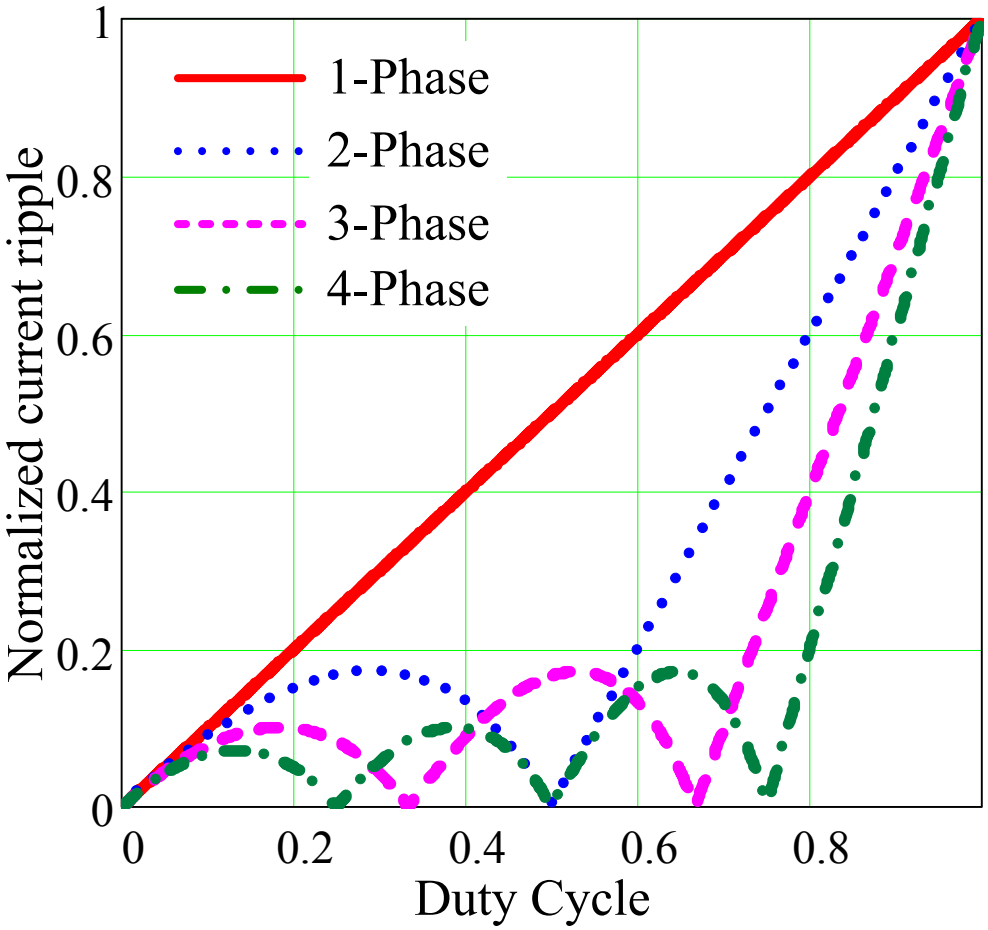


Figure 1.17 Normalized input current ripple with duty cycle and the number of interleaved phase.

Figure 1.18 shows the two-phase interleaved boost converter with an active clamp resonant zero current transition (ZCT) network [36]. By using an active switch with an inductor and a capacitor, the main switch can achieve zero current turn on using critical conduction mode. Zero current and zero voltage during turn off can be achieved using the resonant network. In this case the main switch voltage stress is reduced. The output diode reverse recovery problem can also be solved using the resonant network. However, in order to maintain the critical conduction operation, switching frequency has to be changed accordingly. This will obviously increase the control complexity and increase difficulty of the EMI filter design

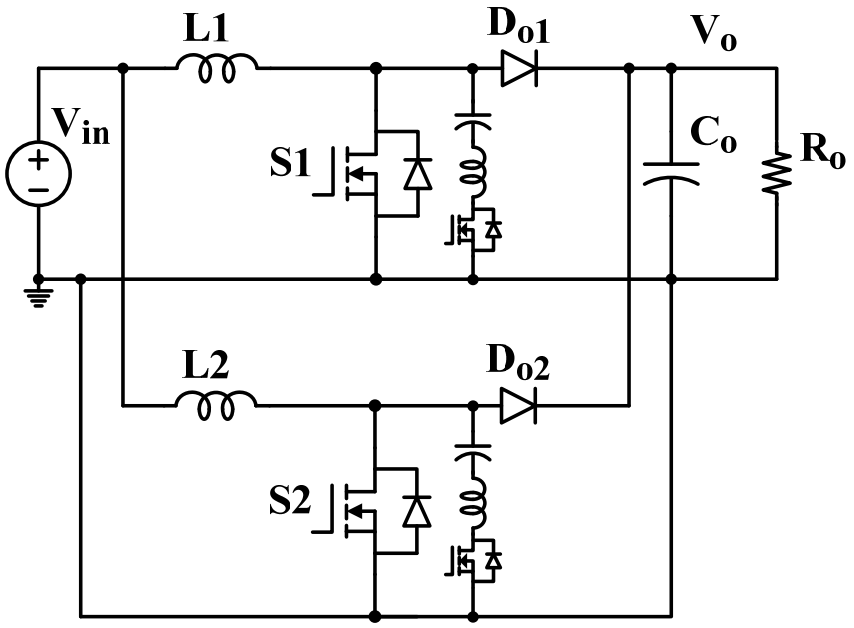


Figure 1.18 Two phase interleaved boost converter with active clamp ZCT network.

Using coupled inductor for the interleaved boost dc-dc converter can reduce the inductor size, and achieve the main switch zero current switching and suppress the diode reverse recovery current [29, 31-33, 35, 37-40]. There are two different coupling method, common mode coupling and differential mode coupling shown in Figure 1.19 and Figure 1.20. Both method could realize the zero current turn on of the main switch, and solve the reverse recovery problem of output diode. The common mode coupled method could reduce the current ripple of main switch, and reduce the conduction loss of the switch. But the main switch turn off at hard switching, which will have high switching loss. The differential mode coupled method has larger current ripple, because the circuit operates at discontinuous mode. This will increase the conduction loss of the main switch. But the main switch can achieve zero current switching when the switch turns off. These two different coupling methods have their own features, and which coupling method should be chosen depends on the specific application and circuit design trade off.

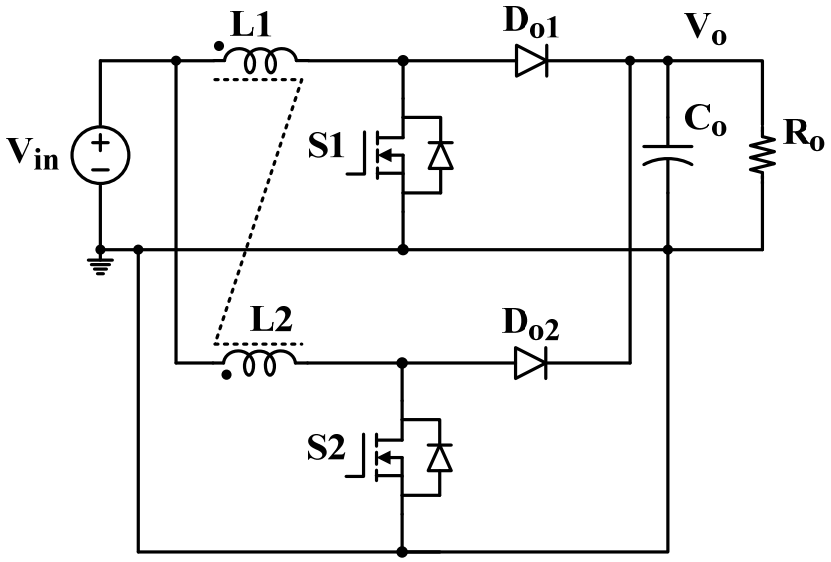


Figure 1.19 Common mode coupled interleaved boost dc-dc converter.

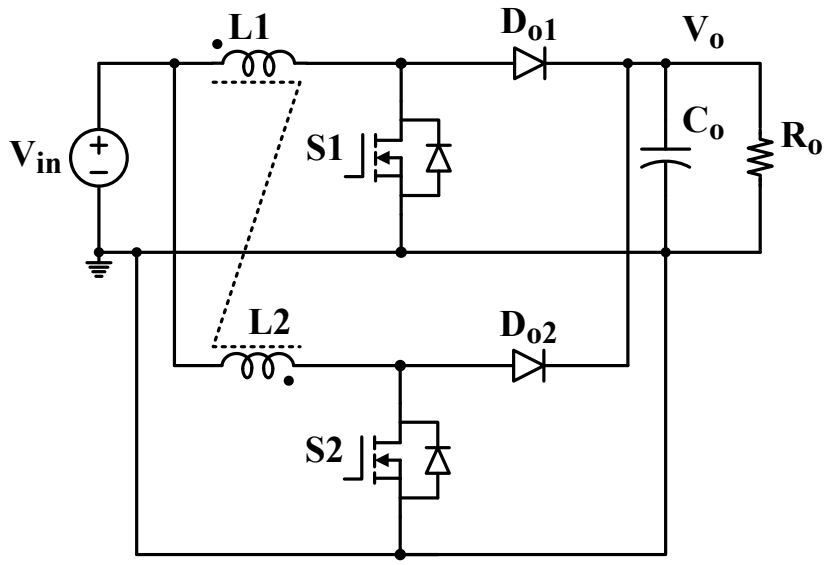


Figure 1.20 Differential mode coupled interleaved boost dc-dc converter.

In order to maintain the low conduction loss features of common mode couple interleaved boost dc-dc converter and overcome the hard switching turn off problem. An active clamp soft switching strategy has been proposed recently [31, 41-43]. Figure 1.21 shows the common mode coupled inductor interleaved boost dc-dc converter with active clamp circuit. By using two active clamp switches, the main switch can achieve zero voltage turn off. The introduction of the active

clamp switch also reduces the voltage stress of the main switch. The active clamp switch can achieve zero voltage turn on and turn off, no inductor need to be added too. The control and gate drive of the active clamp switch is also easy to implement. This circuit is suitable for regular voltage boost operation with normal voltage gain.

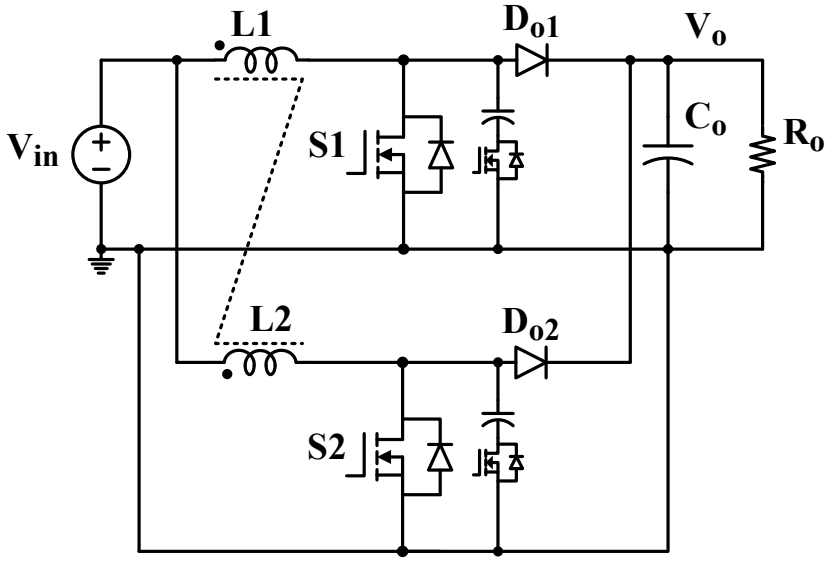


Figure 1.21 common mode coupled inductor interleaved boost dc-dc converter with active clamp.

The interleaved boost dc-dc converter can increase the input current rating and the converter power rating effectively. The input current ripple can be reduced significantly by choosing proper duty cycle and the number of interleaved phase. By using the coupled inductor strategy, the inductor size can also be reduced. However, the interleaving technique does not increase the converter voltage gain; other techniques have to be used to increase the converter conversion ratio.

1.3.1.3 Multilevel boost dc-dc converter

In order to reduce the voltage stress of main switch and increase voltage gain of the boost converter. Three-level boost dc-dc converter and N-level boost dc-dc converter are proposed [44-49]. Figure 1.22 shows the three-level boost dc-dc converter. Figure 1.23 shows the N-level dc-

dc boost converter. In the high voltage output application, using multilevel structure can reduce the voltage stress of each switch, where low voltage devices could be used.

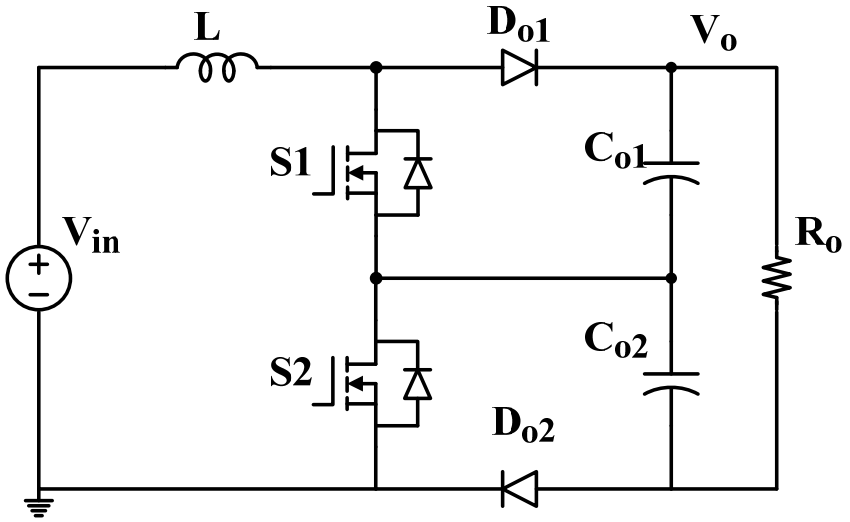


Figure 1.22 Three level boost dc-dc converter.

However, by using the multilevel structure will not increase the voltage gain of the converter assuming $\frac{R_L}{R_o}$ is the same. In reference [48], the voltage gain equation considering the influence of R_L has been mentioned as follows:

$$V_{gainN} = \frac{1}{\frac{1-D}{N_L} + \frac{N_L}{1-D}\frac{R_L}{R_o}} \tag{1.5}$$

Where N_L is number of levels.

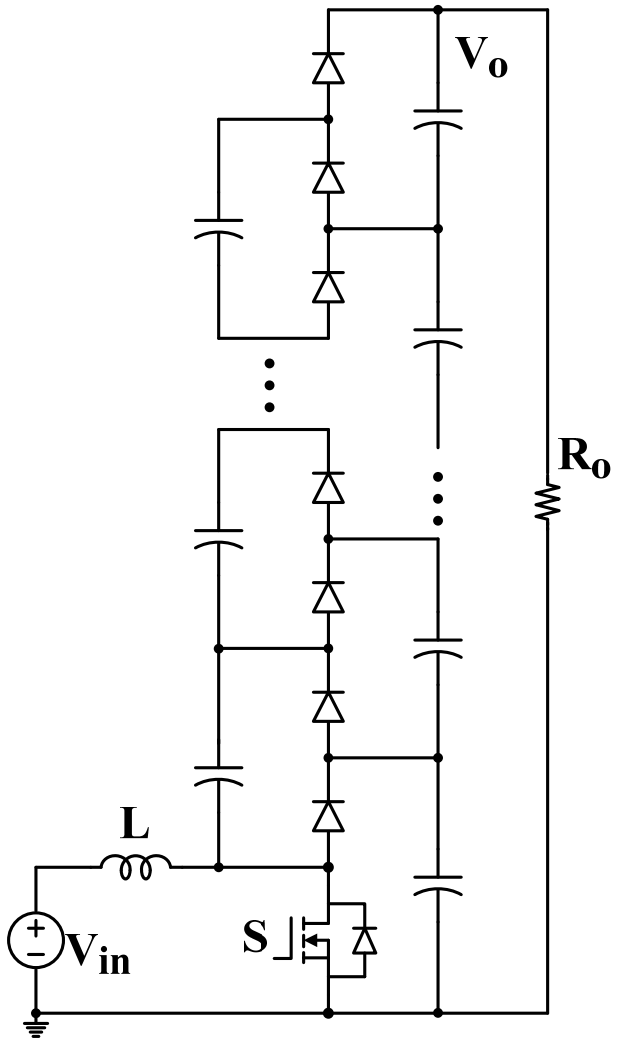


Figure 1.23 N-level boost dc-dc converter.

Figure 1.24 shows the voltage gain curve by change number of level and duty cycle described in equation (1.5) assuming $\frac{R_L}{R_o} = 0.01$. It can be seen from the curve that, with the increase of number of levels, the maximum voltage gain will not change. The duty cycle of maximum output voltage has been reduced, which will increase the dynamic response of the converter.

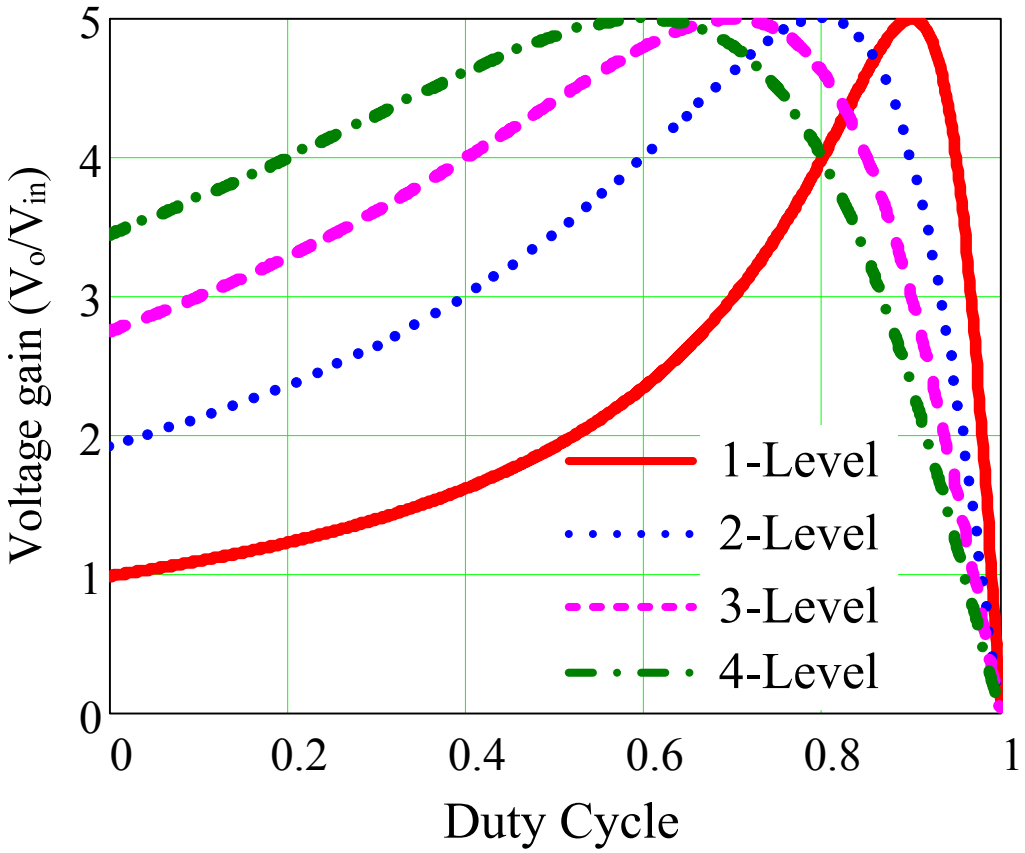


Figure 1.24 Multilevel boost dc-dc converter voltage gain curve considering internal resistance.

In order to achieve high efficiency, and minimize the switching loss, several soft-switching strategies have been proposed by adding an auxiliary circuit [50-52]. However, because of the inherent characteristics of multilevel boost converter, the voltage gain of the converter is not increased, and not suitable for high voltage gain application. By cascading multilevel boost converter, some other converter topologies have been proposed [53]. Figure 1.25 shows the cascade three level boost dc-dc converter. By cascading two boost dc-dc converters together, the voltage conversion ratio is doubled obviously, and the device voltage stress of the first stage is reduced, the device current stress of the second stage is also reduced. However, the cascaded boost converter needs two sets of power devices, two inductors, and two sets of control circuits.

The control signal of the two different control chips has some difference, the total system may have stability problem [54, 55].

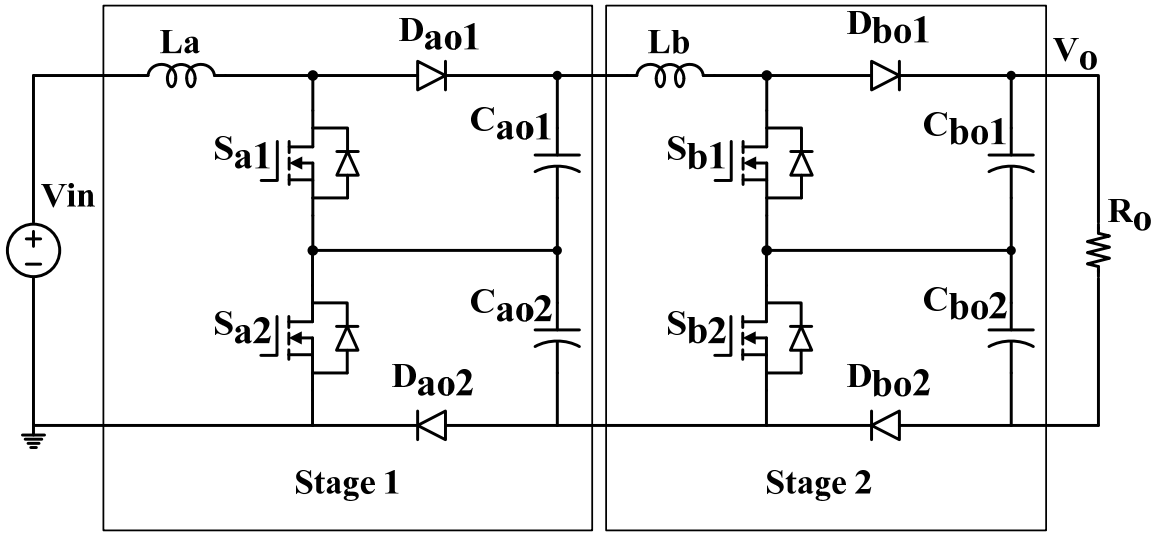


Figure 1.25 Cascaded three level boost dc-dc converter.

The multilevel boost dc-dc converters reduce the device voltage stress by using multilevel technique, but the voltage gain is not increased as expected considering the internal resistance. In order to increase the voltage gain of the boost converter, other techniques, such as coupled inductor have to be used.

1.3.1.4 Coupled inductor boost dc-dc converter

Flyback transformer actually is a coupled inductor. If the circuit does not require the isolation, a non-isolated flyback transformer or coupled inductor could be used. By adding a non-isolated flyback dc-dc converter with a boost converter. A high voltage gain coupled inductor boost dc-dc converter can be derived [56-63]. Figure 1.26 shows the boost flyback step-up dc-dc converter. The output voltage is the sum of a flyback converter which consists of L1/L2, D1, C1 and S, and a boost converter which consists of L1, S, D2, and C2. Since the flyback output is $V_o = V_{in}\frac{nD}{1-D}$ and boost output is $V_o = V_{in}\frac{1}{1-D}$, the total output voltage is $V_o = V_{in}\frac{1+nD}{1-D}$. Here, n is the

turns ratio between the secondary and primary, and D is the switch duty cycle. When the switch S is turned on, the energy is stored in L1, and when S is turned off, the energy is released to charge both C1 and C2 through diodes D1 and D2. The problem is when S turns on these diodes need to be turned off, and a parasitic capacitance across D1 and the leakage inductance can cause severe ringing and additional voltage stress on D1.

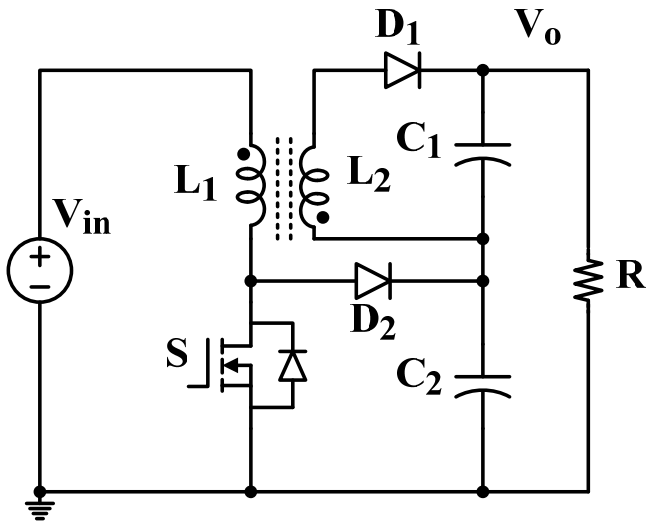


Figure 1.26 Boost flyback step-up dc-dc converter.

In order to solve the diode voltage spike problem of boost flyback step-up dc-dc converter, some other topologies have been proposed using capacitor coupling or charge pump circuits [63-67]. Figure 1.27 shows the improved boost flyback dc-dc converter with coupling inductor between the primary side and secondary side of the transformer. A diode is added between boost output and secondary of the flyback winding to circulate the energy, as shown in Figure 1.27. The added capacitor, C1, stores the energy when the switch S is turned on and maintains a constant voltage related to the turns ratio n, duty cycle D, and input voltage Vin. During switch-off state during which D1 and D3 conduct, C1 energy is released to output, and the output voltage equals the sum of the two capacitor voltage and the secondary winding voltage. If the

leakage inductance is negligible, then the output voltage equals $V_o = V_{in}\frac{2+n}{1-D}$. Compared with the version with combination of flyback and boost converters, this circuit allows a higher-voltage boost ratio, and thus the turns ratio or duty cycle can be reduced for the same output voltage.

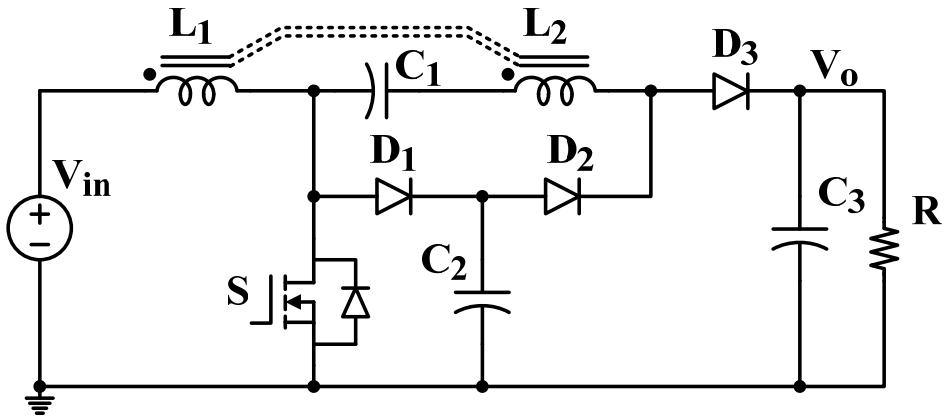


Figure 1.27 Improved boost flyback dc-dc converter with capacitor coupling.

The circuit shown in Figure 1.27 has the problem to filter out the low frequency ripple in the input side if a large inductor is not used in the high voltage dc link. Another improvement of boost flyback dc-dc converter has been proposed by combining the boost flyback with a charge pump circuit shown in Figure 1.28. Compared to the circuit shown in Figure 1.27, this circuit sacrifice some voltage gain to achieve the wide input voltage range operation. Moreover, this circuit have to insert a small inductor to limit the inrush current of the charge pump. The output voltage of this circuit is $V_o = V_{in}\frac{2+nD}{1-D}$.

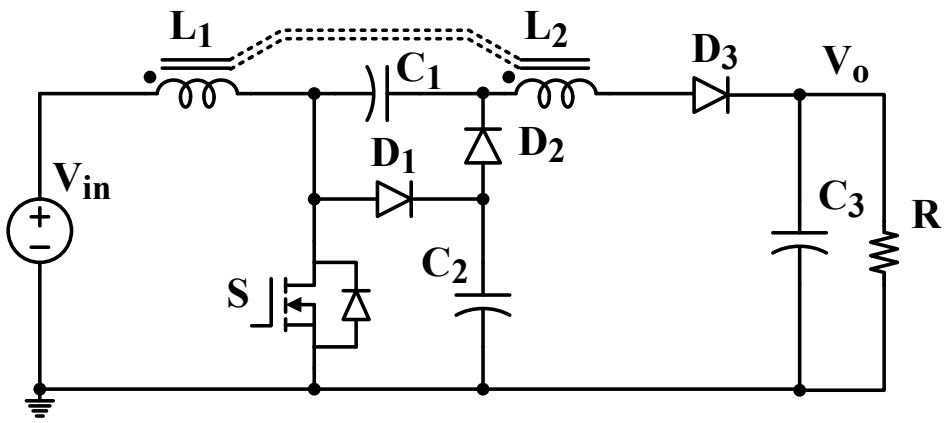


Figure 1.28 Improved boost flyback dc-dc converter with charge pump.

In order to increase the input current rating of the boost flyback dc-dc converter, an interleaved three coupled inductor boost dc-dc converter are proposed [31, 68-72] shown in Figure 1.29. The extra inductor is added in order to simplify the circuit small signal mode to a boost converter, and the close loop control circuit design is becoming easy.

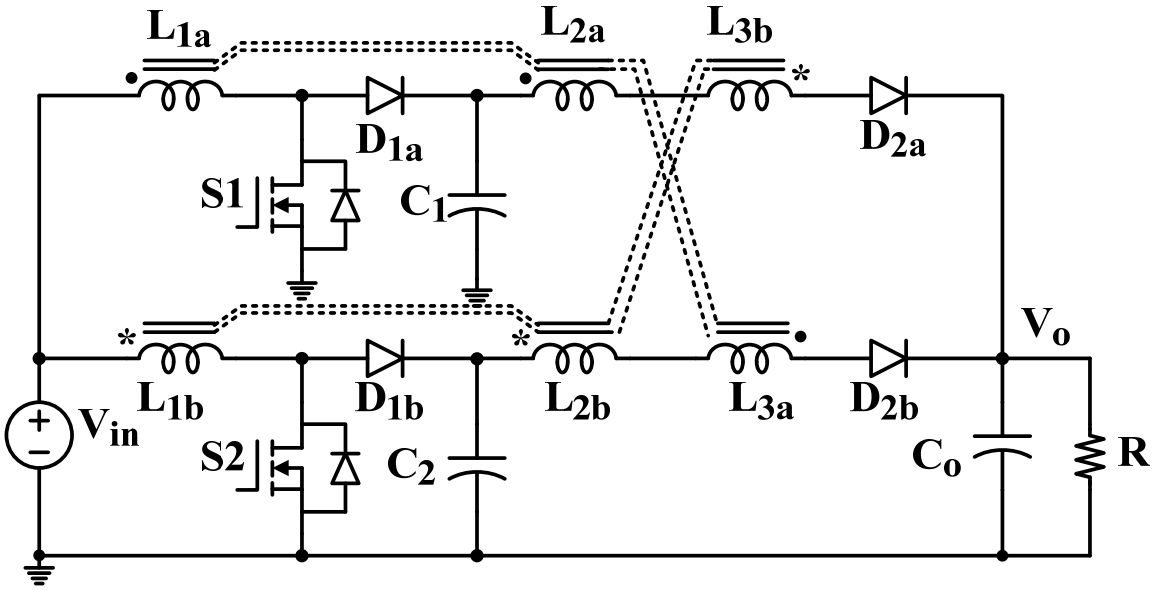


Figure 1.29 Interleaved three coupled inductor boost flyback dc-dc converter

Figure 1.30 shows the ideal voltage gain curve of boost flyback and its improvements when the transformer conversion ratio n=3. By using a coupled inductor the voltage gain of the converter can be improved significantly.

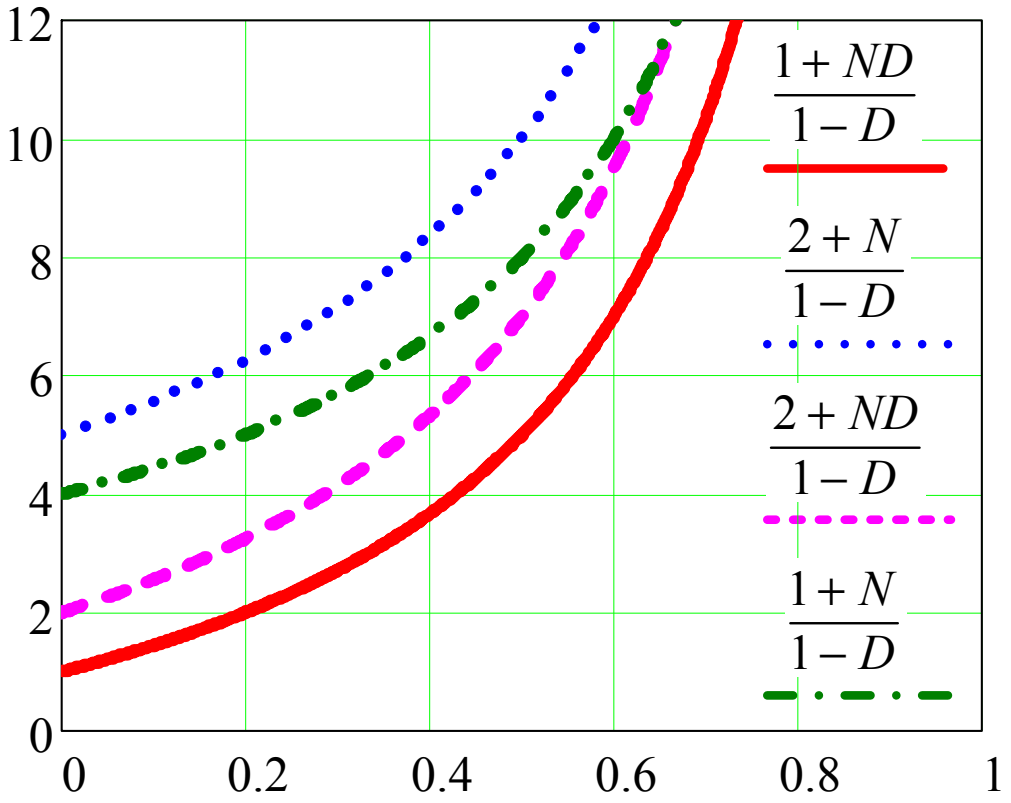


Figure 1.30 Ideal voltage gain curve of boost flyback and its improvements.

In conclusion, for the traditional step-up dc-dc converter, there are several limitations related to the high voltage gain and high current applications. Coupled inductor has to be used in order to increase the converter voltage gain. Interleaved strategy has to be used in order to increase the converter input current rating. Active-clamp or passive devices clamp strategies have to be used to ease switching, reduce the switching loss and increase the converter efficiency. Moreover, if the converter input current rating is increased, more and more interleaved circuits have to be use, which will obviously increase the complexity of the control and gate drive. Besides, more and more inductors in parallel are hard to couple and increase the difficulty of circuit layout. And because of the leakage inductance and the internal resistance of the coupled inductor, the converter voltage gain will be limited too.

Furthermore, all the traditional step-up dc-dc converters have to utilize coupled inductors or transformers for the high voltage gain application. And the magnetic components are usually the most bulky and lossy part in the converter. Also, in high temperature automotive application, the magnetic parts become dysfunctional. So, in order to achieve small size, high efficiency dc-dc converters with high temperature operation features, magnetic-less switched-capacitor dc-dc converter is needed to be considered. Traditional switched-capacitor dc-dc converter is going to be reviewed in next section. Problems related to the traditional switched-capacitor dc-dc converter will be addressed and discussed. New soft-switching strategy will be proposed to solve the traditional circuit limitations and improve the circuit performances in next three chapters.

1.3.2 Switched-Capacitor DC-DC Converter

Switched-capacitor dc-dc converters have been proposed since 1970s due to their integration capability and small size, light weight features. The three basic structures of switched capacitor dc-dc converter will be discussed in detail in the following parts. The advantages and disadvantages of each structure will be addressed and discussed. The appropriate structure for high voltage gain and high current TEG application will be summarized.

1.3.2.1 Marx converter type switched-capacitor voltage multiplier

Figure 1.31 shows the traditional switched-capacitor voltage multiplier structure [73-75]. The control signal of switched-capacitor voltage multiplier is complementary, and duty cycle can be set as 50% duty cycle or other value to achieve some voltage regulation. The voltage stress of the capacitor $C_1 \sim C_{N-1}$ is the input voltage. When the conversion ratio is high, low voltage rating capacitor can be used, which can reduce the converter size. The current stress of the capacitor $C_1 \sim C_{N-1}$ is the same, which means same current rating capacitor could be used. The current stress of all the switching devices is also the same, which means the same current rating

switching devices could be used. However, the voltage stress of the switching devices increases as the conversion ratio increases. When the output voltage is low (less than 60 V), this is not a problem. However, when the output voltage is high, high voltage rating devices have to be used in the output side. However, the turn on resistance of high voltage switching devices is much higher than the low voltage devices, so this structure is not suitable for the high output voltage applications.

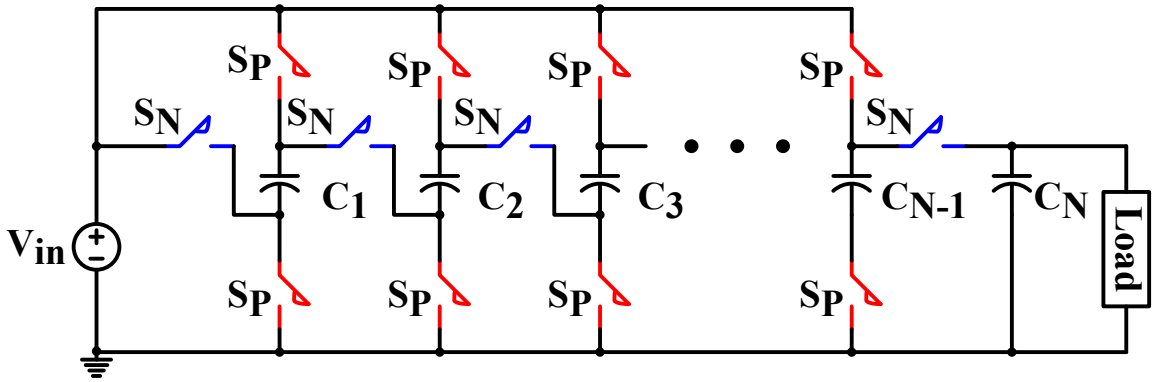


Figure 1.31 Traditional switched-capacitor voltage multiplier.

1.3.2.2 Dickson charge pump type multilevel modular switched-capacitor dc-dc converter

Figure 1.32 shows the traditional Dickson charge pump type multilevel modular switched-capacitor dc-dc converter [76-80]. The control signal of this type converter is complementary with 50% duty cycle which is very easy to implement. The current stress of all the switches and capacitors are the same, which means same current rating device could be used. And when the current rating of the converter is increased, the current through each devices could be equally distributed thus making this converter especially suitable for the high current application. The voltage stress of the switches is one or twice the input voltage, which is also relatively low, when the conversion ratio is high. However, for this converter, the capacitor voltage stress is increased with the increasing of converter voltage gain. When the output voltage is high, a high voltage

stress capacitor has to be employed. Therefore, this structure is suitable for the relatively low output voltage (less than 100 V), high current, high voltage gain application.

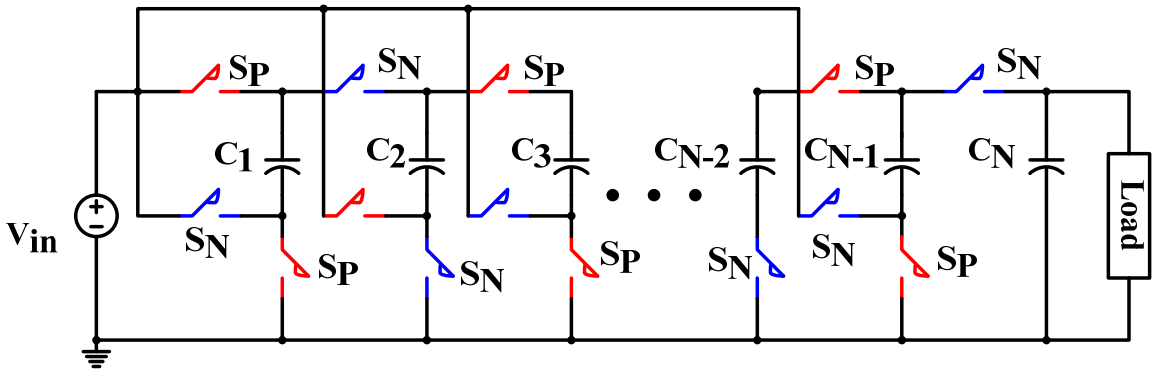


Figure 1.32 Traditional multilevel modular switched-capacitor dc-dc converter.

1.3.2.3 Generalized multilevel switched-capacitor dc-dc converter and the derivative circuits

Figure 1.33 shows the generalized multilevel switched-capacitor dc-dc converter [81-83].

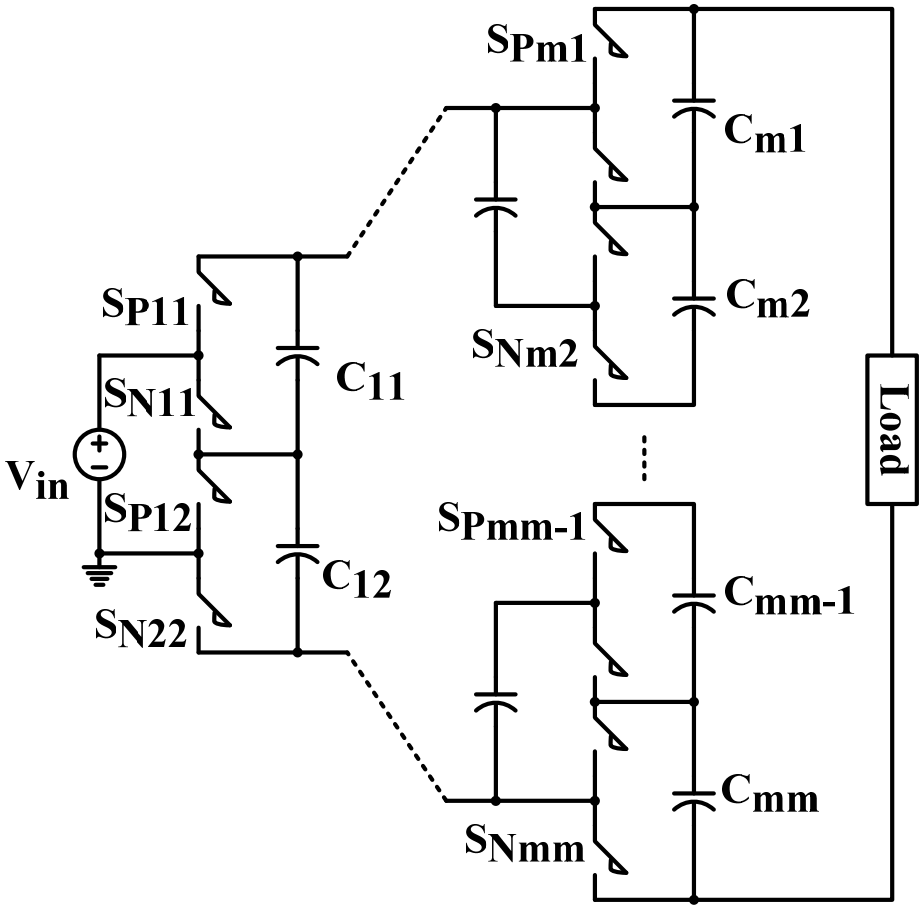


Figure 1.33 Traditional generalized multilevel switched-capacitor dc-dc converter.

Figure 1.34 shows the one three level generalized multilevel converter derivation circuit. Figure 1.35 shows some other derivation by reducing the capacitor and switch numbers. The device voltage stress of the generalized switched-capacitor dc-dc converter is as the same as the input voltage. The capacitor voltage stress of circuit shown in Figure 1.33, Figure 1.34 and Figure 1.35(b) are also the same, which is the input voltage. The structure shown in Figure 1.35(b) is also known as the Cockcroft-Walton generator. The capacitor voltage stress of the derivation circuit shown in Figure 1.35(a) increases with the conversion ratio. Because of the low voltage stress features of the generalized switched-capacitor dc-dc converter, this type of converter is suitable for the very high output voltage application. However, the current stress of this type of converter is not equal, and the control signal is very complex with the increase of

voltage level except the derivation shown in Figure 1.35(b) with complementary control signal. Consequently, this type of converter is not suitable for high current and high voltage gain application.

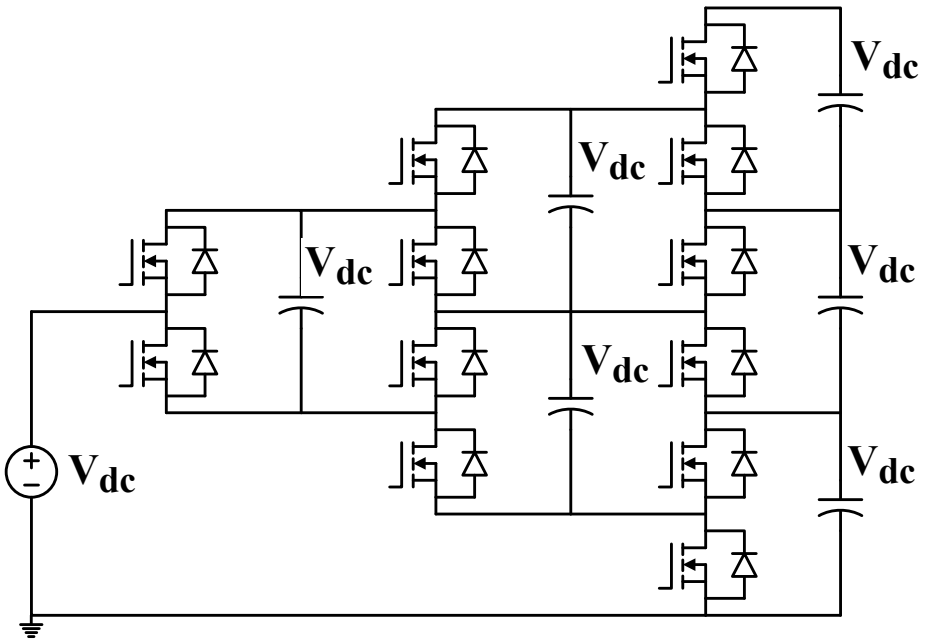


Figure 1.34 Three level generalized multilevel converter derivation.

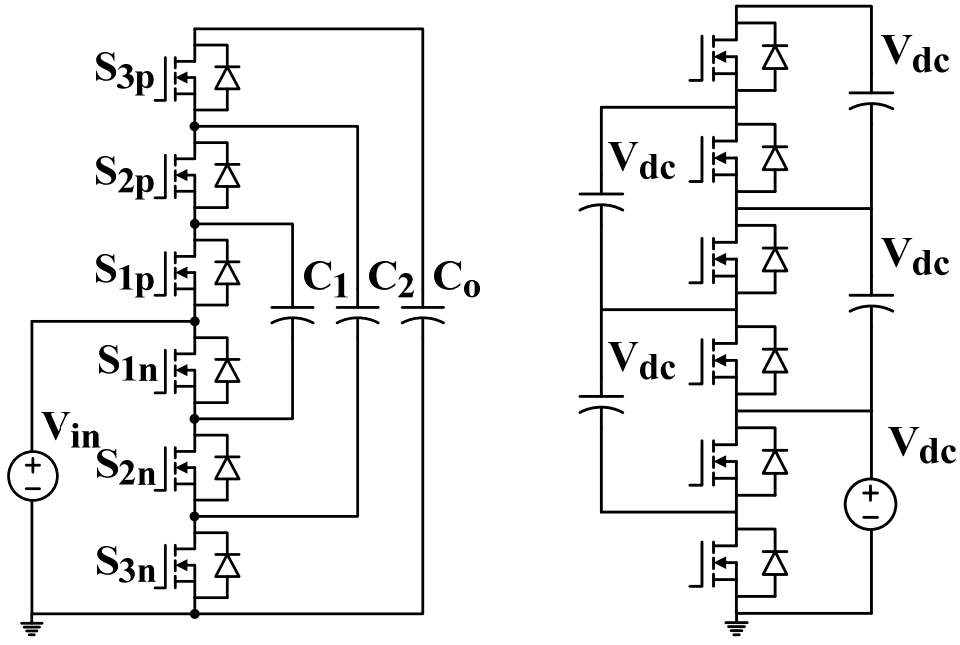


Figure 1.35 Some other three level generalized multilevel converter derivations.

In summary, the Marx converter type and charge pump type switched-capacitor circuits are suitable for the high current, high voltage gain application with output voltage relatively low. And the generalized multilevel type is more suitable for the high output voltage, low voltage gain, and low current application.

1.3.2.4 Traditional Zero current switching (ZCS) switched-capacitor dc-dc converter

But these traditional switched-capacitor dc-dc converter circuits have some common problems such as high voltage spike, high switching loss and EMI problem. In order to reduce the switching loss, high voltage spike and EMI, several ZCS switched-capacitor dc-dc converter have been proposed to solve the problem by inserting an inductor in series with the capacitor to achieve the ZCS of the main switches [84-88].

Figure 1.36 shows a four level switched-capacitor resonant converter as an example. By inserting an inductor L_r resonating with the capacitor C_{2a}, the ZCS of the main switches S_1 and S_2 can be achieved. The switching loss can be minimized, the voltage overshoot across the switching devices can be reduced and the EMI noise is also restricted. However, by inserting a relatively big inductor in the switched-capacitor circuit is a contradiction by itself which means many good features of switched-capacitor circuit will lose, such as good integration capability and high temperature operation. So the traditional ZCS method is not practical, new method need to be proposed.

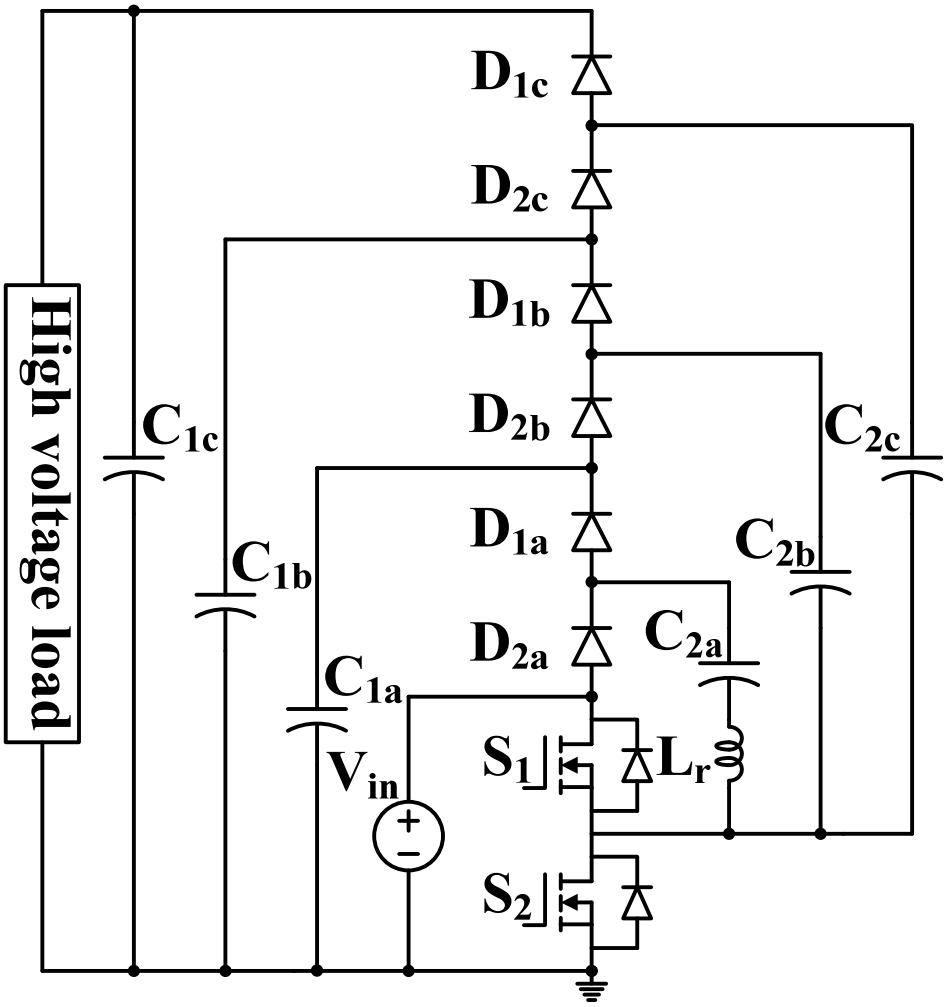


Figure 1.36 Four level switched-capacitor resonant converter main circuit.

1.4 Outline of Dissertation

The goal of this research is to develop a high efficiency, small size, high voltage gain dc-dc converter with low input voltage and high input current features especially for TEG modules in automotive application, and to develop a low cost inverter without ground current for single phase PV application. In this dissertation, a new soft-switching strategy of realizing ZCS for switched-capacitor dc-dc converter has been proposed. By utilizing the stray inductance distributed in the circuit to resonate with the capacitor, the ZCS of all the switching devices can be achieved. By applying this strategy to the traditional switched-capacitor dc-dc converter,

switching loss is minimized, huge di/dt, dv/dt and EMI noises are reduced, high voltage spike problem is also solved. In this case, the efficiency and reliability of traditional switched-capacitor dc-dc converter would be improved. In order to solve the high input current ripple and increase the total power rating of switched-capacitor dc-dc converter, multiphase ZCS switched-capacitor dc-dc converters have been proposed and analyzed. In order to achieve the high efficiency MMSCC, an optimal design method has been proposed, to design the MMSCC in the under-damped case with ZCS is proved to be more efficient and with small size. In order to reduce the capacitor voltage stress, a double-wing multilevel modular capacitor-clamped dc-dc converter (DW-MMCCC) is proposed. The peak capacitor voltage stress is reduced by half. ZCS can also be achieved for all the switching devices of DW-MMCCC.

Chapter 2: A ZCS multilevel modular switched-capacitor dc-dc converter (MMSCC) for high input current high voltage gain TEG application is proposed. By using the proposed ZCS strategy for MMSCC, the capacitor size is reduced, voltage overshoot is eliminated and EMI noise is restricted. Prototypes are designed and built. Simulation and experiment results are provided to validate the proposed topology.

Chapter 3: A family of ZCS switched-capacitor dc-dc converters is proposed and analyzed. By using the ZCS strategy, very high power density (above 300 W/in^3) with high efficiency switched-capacitor dc-dc converters could be made by eliminating the lossy magnetic cores and bulky capacitor bank. Simulation and experiment results are provided to confirm the operation of proposed circuits.

Chapter 4: In order to increase the power rating of ZCS-MMSCC and reduce the input capacitor size and loss. Other circuit improvements for the ZCS switched-capacitor dc-dc converter are proposed and analyzed. By using the proposed multiphase ZCS switched-capacitor

dc-dc converter topologies, interleaved operation of ZCS switched-capacitor dc-dc converters become possible. The input current of ZCS switched-capacitor dc-dc converters becomes continuous due to the interleaving operation. In this case, the input capacitor size could be reduced significantly. Continuous input current is also preferable by many renewable energy sources. Simulation and experiment results are provided to validate the proposed topologies.

Chapter 5: In order to design the MMSCC with highest efficiency with smallest size. The optimal design method of MMSCC is proposed. By considering the stray inductance in the circuit, MMSCC can be designed at over-damped case or under-damped case. In over-damped case, the MMSCC can be designed to achieve high efficiency, but a huge capacitor bank has to be utilized, which will increase the converter size. In under-damped case, the low capacitance MLCC can be used with high efficiency and small size target achieving at the same time.

Chapter 6: The capacitor voltage stress of MMSCC is still too big, in order to reduce the capacitor voltage stress and keeping all the features of MMSCC, a DW-MMCCC has been proposed. The total device number, capacitor number, and device voltage stress of DW-MMCCC can be considered the same with the traditional MMSCC or single-wing MMSCC. ZCS can also be achieved for all the devices of DW-MMCCC. The efficiency and power density of DW-MMCCC can be increased further.

Chapter 7: In order to achieve the voltage regulation of the proposed DW-MMCCC, a phase-shift method has been proposed without scarifying significant power loss. The zero voltage switching can also be achieved by using the proposed method.

Chapter 8: In order to achieve a low cost dc-dc converter with positive and negative output features, a Z-source dc-dc converter is proposed. By only utilizing two switching devices, Z-

source dc-dc converter is able to output positive and negative voltage at the same time. It could be used for dc motor drive and zero voltage electronic load.

Chapter 9: Since the previous proposed Z-source dc-dc converter can output positive and negative voltage at the same time, a proper modulation strategy can be used for the Z-source dc-dc converter to output sinusoid voltage. Semi-Z-source dc-ac inverter with only two active switching devices is proposed accordingly. The semi-Z-source inverter also has doubly grounded features, which will eliminate the ground current issues of traditional full-bridge inverter.

Chapter 10: Since the micro-inverter integrated with a PV panel becomes more popular in residential application, a low cost high efficiency transformer-isolated micro-inverter for grid-connected application is proposed. By using the proposed micro-inverter to integrate with the PV panel, an AC output PV panel with MPPT can be achieved, which makes the PV panel application more flexible.

Chapter 11: conclusion of the dissertation. Contributions are summarized, suggestions for future work are provided.

CHAPTER 2
Zero Current Switching Multilevel Modular Switched-Capacitor DC-DC Converter

This chapter presents a quasi-resonant technique for multi-level modular switched-capacitor dc-dc converter (MMSCC) to achieve zero current switching (ZCS) without increasing cost and sacrificing reliability. This ZCS-MMSCC employs the stray inductance distributed in the circuit as the resonant inductor to resonate with the capacitor and provide low dv/dt and di/dt switching transition for the device. The ZCS-MMSCC does not utilize any additional components to achieve ZCS, and meanwhile solves the current and voltage spike problem during the switching transition, thus leading to reliable and high efficiency advantages over traditional MMSCC. Furthermore, the ZCS-MMSCC reduces the capacitance needed in the circuit to attain high efficiency. In this case, the bulky capacitor bank with high capacitance in traditional MMSCC to reduce voltage difference and achieve high efficiency is not necessary any more. A 150 W four-level ZCS-MMSCC prototype has been built. Simulation and experimental results are given to demonstrate the validity and features of the proposed soft switching switched-capacitor circuit.[2]

2.1 Introduction

In order to obtain the light weight, small size, high efficiency, high power density and integrated dc-dc converter, switched-capacitor circuits have been investigated since 1970s [76, 89]. Conventional switched-capacitor dc-dc converters have some common drawbacks: 1) weak

[2] This work was presented in part at the first annual IEEE Energy Conversion Congress and Expo, San Jose, CA USA, Sep.20 – Sep.24 2009 and an extended paper titled "Zero Current Switching Multi-level Modular Switched-Capacitor DC-DC Converter for TEG Applications" has been published in IEEE Transactions on Industry Applications.

output regulation ability and structurally determinate voltage conversion ratio; 2) pulsating input current and high current spike; 3) high voltage spike across the switching device; 4) high electromagnetic interference (EMI); 5) unidirectional power conversion ability. Many approaches have been proposed to achieve voltage regulation by using duty cycle control [75, 89, 90]. But all this methods have to sacrifice efficiency to achieve the voltage regulation, which is only acceptable in low power conversion field. Several ZCS techniques by inserting an inductor to switched-capacitor circuit have been proposed to solve the voltage spike, current spike and EMI problem [84, 87, 88, 91]. However, by adding a relatively big resonant inductor into the switched-capacitor circuit to achieve ZCS is a contradiction by itself. Switched-capacitor circuit with a magnetic core is not a switched-capacitor circuit any more, and the good features such as, high temperature operation, good integration, and small size will be lost [92, 93].

Another type of switched-capacitor circuit, flying capacitor multi-level dc-dc converter (FCMDC) has become more and more popular recently because of the potential automotive application [83, 94-97]. But there are several limitations of FCMDC, such as non-modular structure, complex control strategy and high conversion ratio unreachability. When the conversion ratio is larger than five or more than five levels have to be used, the control of FCMDC is becoming very complex. The high current stress of the switching device of FCMDC also prevents it from high current application.

In order to solve the problems of FCMDC in high voltage conversion ratio, high current automotive application, multi-level modular switched-capacitor dc-dc converter (MMSCC) was proposed recently, shown in Figure 2.1 [78]. MMSCC has modular structure, complementary control scheme, capability of reaching high voltage gain and reduced switch current stress. It shows good potential in automotive application [98]. Nevertheless, because MMSCC still use

hard switching, there still exist several problems limiting its power rating, such as high current spike, high voltage spike, high switching loss and severe EMI noise. With the increasing of power rating or current rating of the MMSCC, the voltage spike and switching loss problems become more and more serious. Also, in order to increase the total system efficiency by reducing voltage difference between capacitors, higher capacitance electrolytic capacitors have to be used [78, 79, 96, 98]. The current rating of the electrolytic capacitor is small to some extent. In order to meet the high current ripple requirement, a huge electrolytic capacitor bank has to be used, which will increase the size of the converter significantly. Multi-layer chip type ceramic (MLCC) capacitor has much better performance than the electrolytic capacitor, such as equivalent series resistance (ESR), life time, and size in terms of current rating. But the capacitance of MLCC capacitor is very small, so it is not feasible to use MLCC capacitor for the traditional MMSCC.

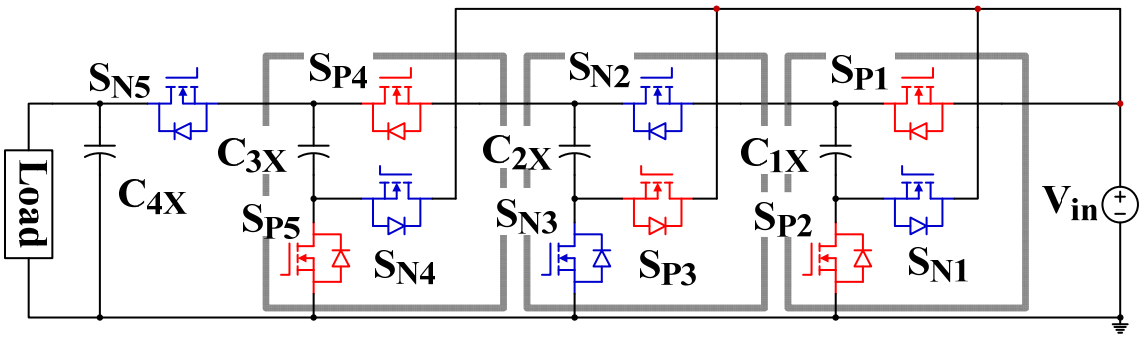


Figure 2.1 Four-level MMSCC with three modular blocks

This chapter presents a quasi-resonant technique for MMSCC that is able to achieve ZCS without increasing cost and sacrificing reliability. The proposed ZCS strategy employs the distributed stray inductances present in each module of the circuit resonating with the capacitors to provide zero current turn-on and turn-off to the devices. Because the MMSCC is especially suitable for high voltage gain with high input current application [78-80, 98-100], the ZCS version also inherit all the benefits from it. By using the ZCS, the switching loss of the

traditional MMSCC is minimized, current spike, voltage spike and EMI is reduced. Besides the benefits gained from ZCS and MMSCC, the proposed ZCS-MMSCC has other special features:

- Different from other soft-switching techniques, this ZCS strategy does not use additional active devices or passive components, thus making it reliable and cost efficient.
- Because of the module structure, the required resonant inductance is quite small for each module, thus making it feasible to be realized by the distributed stray inductance existing in the circuits.
- The ZCS-MMSCC doesn't need high capacitance to achieve high efficiency like traditional MMSCC. In this case, small capacitance, high current rating, low ESR and small size MLCC capacitor could be used. The total size of the converter is reduced significantly, the power density and the converter current rating is increased correspondingly.

Hence, the proposed ZCS-MMSCC solves aforementioned problems of traditional MMSCC and achieves ZCS without inserting big magnetic cores. For the same current rating and voltage gain, the ZCS version of MMSCC is smaller, higher power density, and higher efficiency than the traditional MMSCC. So the proposed ZCS-MMSCC is especially suitable to the high current high voltage gain automotive application. A 150 W four-level ZCS-MMSCC prototype was built to confirm the operation. Simulation and experimental results are given to demonstrate the validity and features of proposed ZCS-MMSCC.

2.2 Proposed Circuit Topology

Figure 2.2 shows the proposed four-level ZCS-MMSCC as an example. The circuit works as a four times step-up converter. Figure 2.3 shows the proposed ZCS-MMSCC converter modular block. The capacitor and the switch label is the same as the Figure 2.1 shown before.

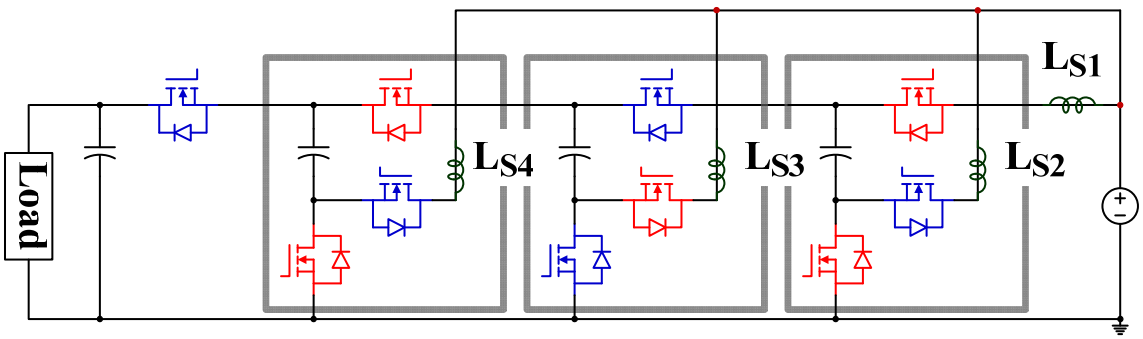


Figure 2.2 Four-level ZCS-MMSCC with three modular blocks

By using n-1 modular blocks, a switch and a capacitor, n-level ZCS-MMSCC with n times voltage gain can be generated. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in each module of the circuit. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_{1X} to C_{4X} are the capacitors with the average voltage from one time to four times of input voltage. L_S does not have to be in the position drawn in Figure 2.2, it could be distributed anywhere in series with switches or capacitors in the circuit shown in Figure 2.4. L_S is the sum of the connection wire parasitic inductance L_{SW}, capacitor parasitic inductance L_{ESL} and the MOSFETs package parasitic inductance L_{Sp}. Usually the connection wire parasitic inductance L_{SW} is the major part of the stray inductance. Because all the stray inductance is in series when the current flows through. In each simplified equivalent circuit discussed in the next section, only one equivalent L_S is needed to represent the total stray inductance present in the circuit.

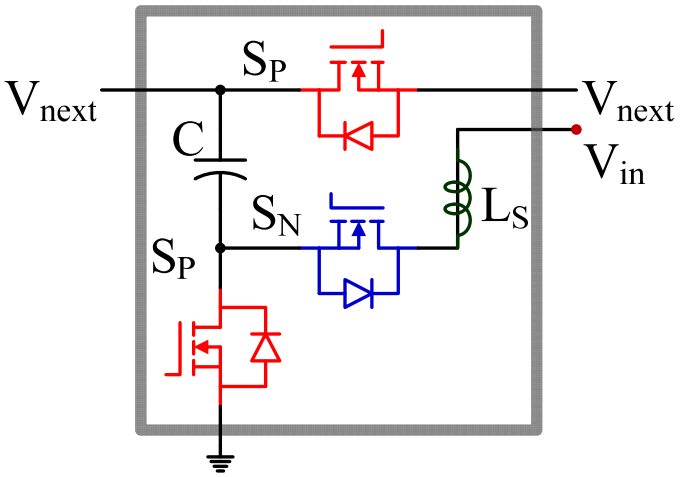


Figure 2.3 proposed ZCS-MMSCC modular block

Due to the modular structure of the circuit, and the stray inductance is distributed equally in each module. The required stray inductance for resonant is more than 100 times smaller (2 nH~13.5 nH) than other ZCS strategies using the same switching frequency [84-88]. In case the stray inductance is not sufficiently large or equally distributed in each module, a small air core could be utilized to promise each module have the same stray inductance for resonant.

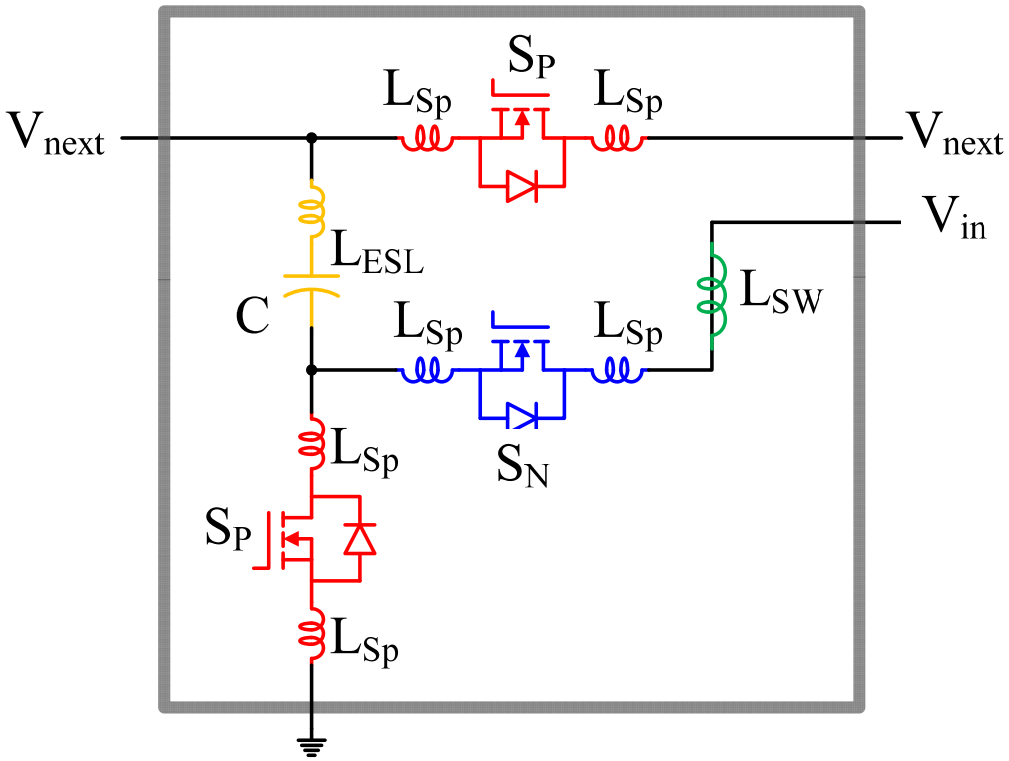


Figure 2.4 ZCS-MMSCC modular block with all the stray inductance.

For traditional MMSCC in high power and high current application, a huge capacitor bank has to be employed in order to sustain current and increase efficiency, which increases the converter size in a significant manner. The huge switching loss and voltage spike caused by the large turn-off current is another problem. Considering the stray inductance present in each module of MMSCC, the capacitance can be designed to resonate with the stray inductance at switching frequency to provide the zero current switching to the devices. In this case, small size, low ESR, high current rating and high temperature rating MLCC capacitor with relatively small capacitance can be utilized. The switching loss of device is minimized, capacitor conduction loss and EMI is also reduced accordingly. Smaller size and higher efficiency is achieved by using ZCS in MMSCC. Hence, ZCS-MMSCC is more suitable to high power, high current and high temperature application.

2.3 Operation Principle

Figure 2.5 shows the idealized waveform of proposed ZCS-MMSCC under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assuming the input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switch is turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switch S_P, S_N and stray inductance will decrease to zero when the switch is turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of the switch is achieved in both turn on and turn off. The capacitor is charged in half-period with the sinusoidal current waveform and discharged in another half-period also in the sinusoidal shape. So, the current through the capacitor is the sum of the current through the switch, which is a sinusoidal waveform. When the capacitor is charged, the current is positive; when the capacitor discharges, the current is negative. The voltage across the capacitor has a dc offset with a sinusoidal ripple. The dc voltage offset is determined by the capacitor position in the circuit from one time input voltage to n times input voltage. The voltage ripple is determined by the capacitor current and capacitance. The operation of the circuit can be described in two states as shown in Figure 2.6 and Figure 2.7 with different switch turned on.

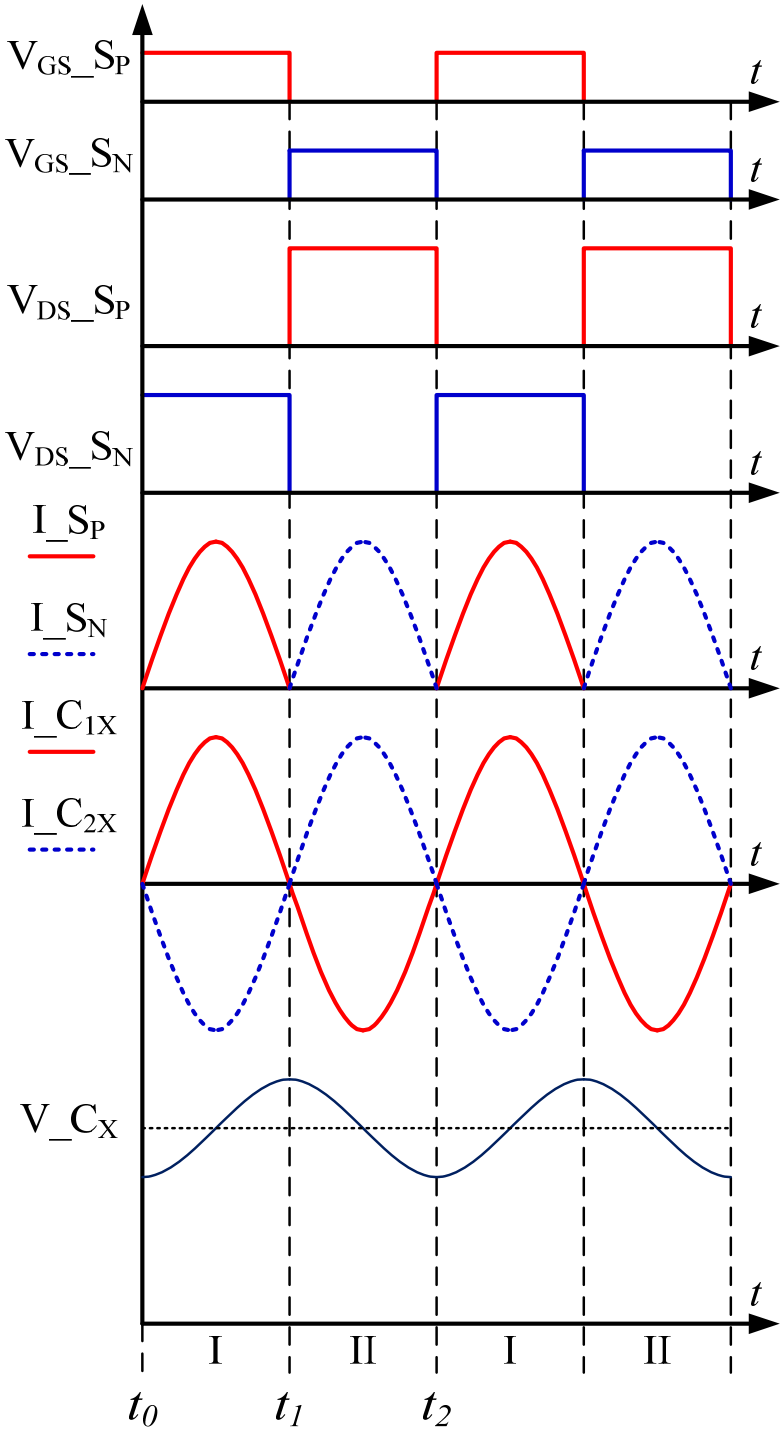


Figure 2.5 Typical waveforms of proposed ZCS-MMSCC

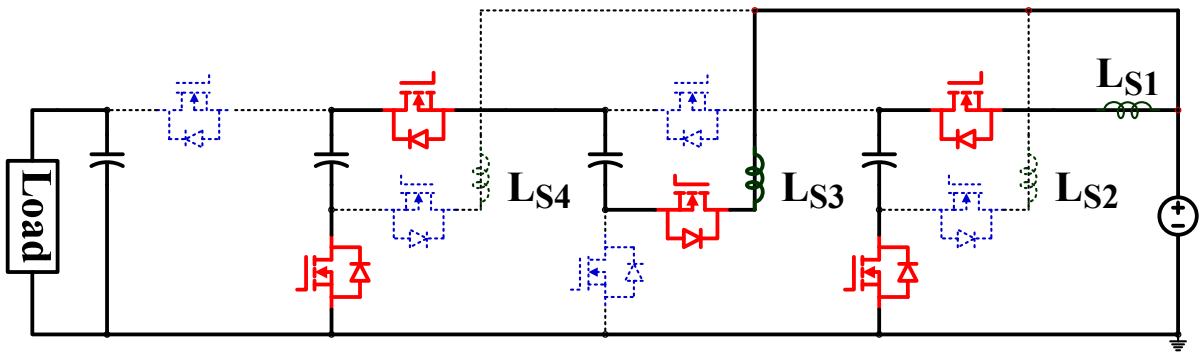


Figure 2.6 Operation modes State I S_P is on

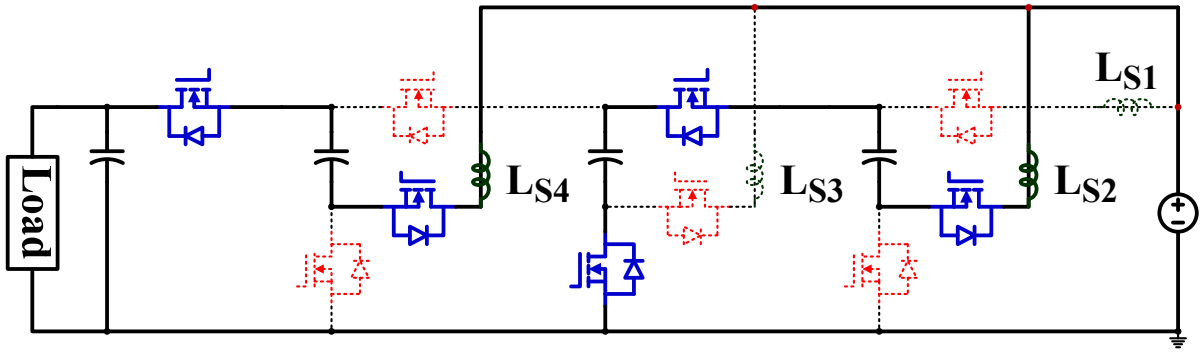


Figure 2.7 Operation modes State II S_N is on

2.3.1 State I

Figure 2.6 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_{1X} is charged by V_{in}. C_{3X} is charged by V_{in} and C_{2X} in series. Figure 2.8 and Figure 2.9 show the two simplified equivalent circuits of state I. Figure 2.8 shows the situation when V_{in}, L_{S1}, S_{P1}, C_{1X} and S_{P2} form a resonant loop. Figure 2.9 shows the situation when V_{in}, L_{S3}, S_{P3}, C_{2X}, S_{P4}, C_{3X} and S_{P5} form a resonant loop. Because of the presence of the equivalent stray inductance L_S, before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. For the case shown in Figure 2.8, after L_{S1} and C_{1X} resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2}

should be turned off at this point, so that the switches are turned off at zero current. For the case shown in Figure 2.9, after L_{S3} resonate with C_{2X} and C_{3X} in series for half cycle, the current through S_{P3}, S_{P4} and S_{P5} will decrease to zero too. So, zero current turn off is also realized on these switches. For the situation shown in Figure 2.8, there is only one capacitor in the equivalent circuit other than two capacitors in series in other equivalent circuits. The required stray inductance value is two times smaller than the other circuits assuming the capacitance are the same. This will not be a problem in the real circuit design and layout; one only need to pay attention to make sure the stray inductance of all the other loops is twice as large as that of the first resonant loop.

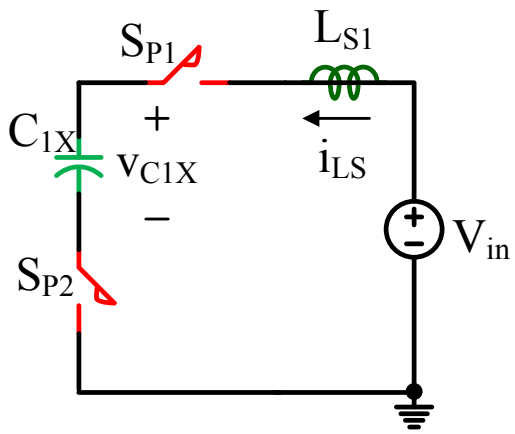


Figure 2.8 Simplified equivalent circuits of state I (a)

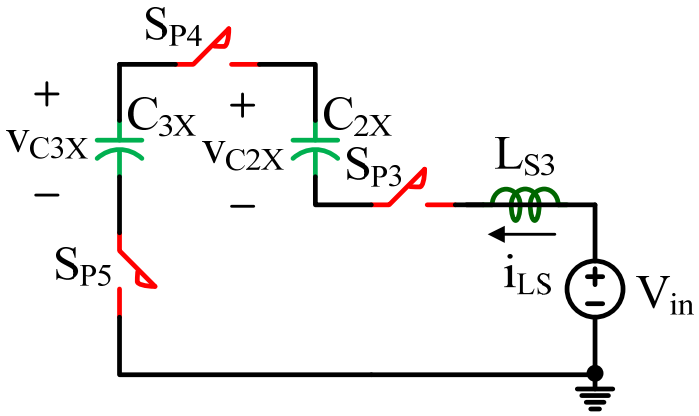


Figure 2.9 Simplified equivalent circuits of state I (b)

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assuming $C_{1X} = C_{2X} = C_{3X} = C_{4X}$, so in order to have the same resonant frequency, $L_{S2} = L_{S3} = L_{S4} = 2L_{S1}$. The state equations of simplified equivalent circuit shown in Figure 2.8 are

$$V_{in} = L_{S1}\frac{di_{L_{S1}}}{dt} + v_{C1X} \tag{2.1}$$

$$i_{L_{S1}} = C_{1X}\frac{dv_{C1X}}{dt} \tag{2.2}$$

The solutions are:

$$i_{L_{S1}}(t) = \frac{\pi P_o}{4V_{in}}\sin\omega_r t \tag{2.3}$$

$$v_{C1X}(t) = V_{in} - \frac{\pi P_o}{4V_{in}C_{1X}\omega_r}\cos\omega_r t \tag{2.4}$$

Where V_{in} is the value input voltage, L_{S1} is the value of stray inductance, ω_r is the resonant frequency equals to $1/\sqrt{L_{S1}C_{1X}}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to

$$v_{C1X}(t_1) = V_{in} + \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \tag{2.5}$$

The capacitor C_{1X} voltage ripple is

$$\Delta v_{C1X} = \frac{\pi P_o}{4V_{in}C_{1X}\omega_r} \tag{2.6}$$

The state equations of simplified equivalent circuit shown in Figure 2.9 are

$$V_{in} = L_{S3}\frac{di_{L_{S3}}}{dt} + v_{C3X} - v_{C2X} \tag{2.7}$$

$$i_{LS3} = C_{3X} \frac{dv_{C3X}}{dt} \tag{2.8}$$

$$i_{LS3} = -C_{2X} \frac{dv_{C2X}}{dt} \tag{2.9}$$

Plug (2.17) into (2.7)and (2.9) to solve the equations

$$i_{LS3}(t) = \frac{\pi P_o}{4V_{in}} \sin \omega_r t \tag{2.10}$$

$$v_{C3X}(t) = 3V_{in} - \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \cos \omega_r t \tag{2.11}$$

The capacitor C_{3X} voltage ripple is

$$\Delta v_{C3X} = \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \tag{2.12}$$

2.3.2 State II

Figure 2.7 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state, C_{2X} is charged by the V_{in} and C_{1X} in series; C_{4X} is charged by V_{in} and C_{3X} in series. Figure 2.10 and Figure 2.11 show the simplified equivalent circuits of state II. Figure 2.10 shows the situation when V_{in}, L_{S2}, S_{N1}, C_{1X}, S_{N2} C_{2X} and S_{N3} form a resonant loop. And Figure 2.11 shows the situation when V_{in}, L_{S4}, S_{N4}, C_{3X}, S_{N5} and C_{4X} form a resonant loop. Because of the presence of the L_S, the current through S_N will also increase its value from zero in a resonant manner. The zero current turn-on of S_N is achieved. For the case shown in Figure 2.10, after L_{S2}, C_{1X} and C_{2X} resonate for half cycle at $t = t_2$, S_{N1}, S_{N2} and S_{N3} will have a zero current turn-off when the current through them decreases to zero. For the case shown in Figure 2.11, after L_{S4} resonate with C_{3X} and C_{4X} in series for a half cycle, the

current through S_{N3}, S_{N4} and S_{N5} will also decrease to zero. Hence, zero current turn off is also realized on these switches.

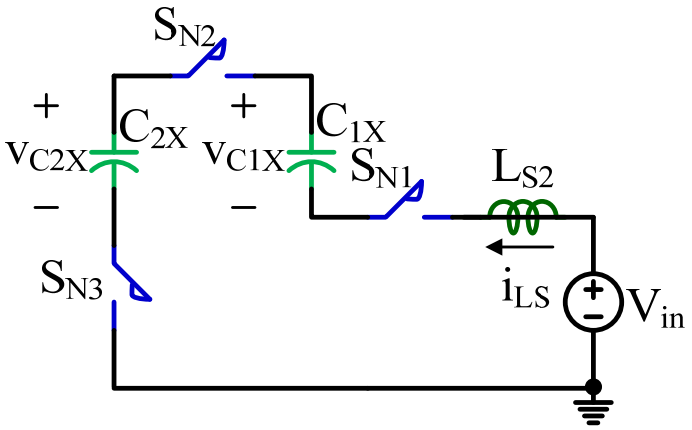


Figure 2.10 Simplified equivalent circuits of state II (a)

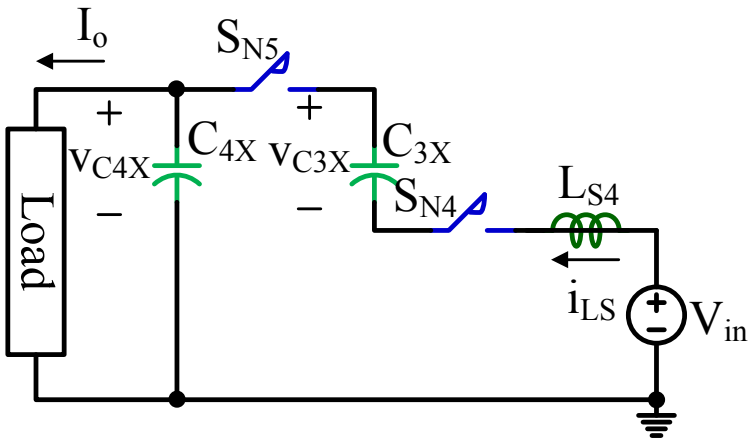


Figure 2.11 Simplified equivalent circuits of state II (b)

The state equations of simplified equivalent shown in Figure 2.10 are:

$$V_{in} = L_{S2}\frac{di_{LS2}}{dt} + v_{C2X} - v_{C1X} \tag{2.13}$$

$$i_{LS2} = C_{2X}\frac{dv_{C2X}}{dt} \tag{2.14}$$

$$i_{LS2} = -C_{1X}\frac{dv_{C1X}}{dt} \tag{2.15}$$

Plug (2.4) into (2.13) and (2.15) to solve the equations

$$i_{LS2}(t) = -\frac{\pi P_o}{4V_{in}} \sin \omega_r t \tag{2.16}$$

$$v_{C2X}(t) = 2V_{in} + \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \cos \omega_r t \tag{2.17}$$

The capacitor C_{2X} voltage ripple is

$$\Delta v_{C2X} = \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \tag{2.18}$$

The state equations of simplified equivalent shown in Figure 2.11 are

$$V_{in} = L_{S4} \frac{di_{LS4}}{dt} + v_{C4X} - v_{C3X} \tag{2.19}$$

$$i_{LS4} = C_{4X} \frac{dv_{C4X}}{dt} + I_o \tag{2.20}$$

$$i_{LS4} = -C_{3X} \frac{dv_{C3X}}{dt} \tag{2.21}$$

Where I_o is the output current. Since this converter is a four times boost circuit $V_o = 4V_{in}$, so $I_{in} = 4I_o$. Plug (2.11) into (2.19) and (2.21) to solve the equations

$$i_{LS4}(t) = -\frac{\pi P_o}{4V_{in}} \sin \omega_r t \tag{2.22}$$

$$v_{C4X}(t) = 4Vin + \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \cos \omega_r t \tag{2.23}$$

The capacitor C_{4X} voltage ripple is

$$\Delta v_{C4X} = \frac{\pi P_o}{4V_{in} C_{1X} \omega_r} \tag{2.24}$$

The soft switching conditions in both states is $f_s = f_r$, where f_s is the switching frequency and f_r is the resonant frequency.

2.4 Design Guidelines

The 150 W four-level ZCS-MMSCC design procedure is shown here as an example. The specification of the prototype converter is V_{in}=5 V, V_o=20 V, P_o=150 W, f_s=45 kHz.

2.4.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{4V_{in}\Delta v_C \omega_r} \tag{2.25}$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the input current, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the first capacitor from resonating to the negative region and lose the zero current switching. That means, the first capacitor should have a positive dc voltage offset. Actually because of the special structure of the converter the output voltage is n times of input voltage, even when the voltage ripple is as large as the input voltage, the voltage ripple on the last capacitor is still $1/n$. When the conversion ratio is large, the ripple will be small enough in the output side. And high capacitance is not needed to reduce the output voltage ripple.

The output ripple is chosen around 9% of output voltage. According to the (2.25), the capacitance is chosen 47 μF in the prototype. Another parameter to determine the capacitance value is the current rating of the capacitor, if the current rating of the capacitor is too small to meet the current requirements, then more capacitors in parallel have to be used. In this prototype, high current rating MLCC capacitors are used. Ten 100 V 4.7 μF C5750X7R2A475K capacitors from TDK are used in parallel. The current rating of each capacitor is around 3 A each.

2.4.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. In case the stray inductance is not equal or large enough, a small air core can be inserted to equalize the stray inductance of each module. The switching frequency should be adjusted according to the stray inductance present in the circuit if the circuit layout is already fixed. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 2.8.

$$L_{S1} = \frac{1}{C_{1X}\left(2\pi f_S\right)^2} \tag{2.26}$$

When the resonant capacitance is 47 μF, Figure 2.12 shows the curve of switching frequency vs. stray inductance.

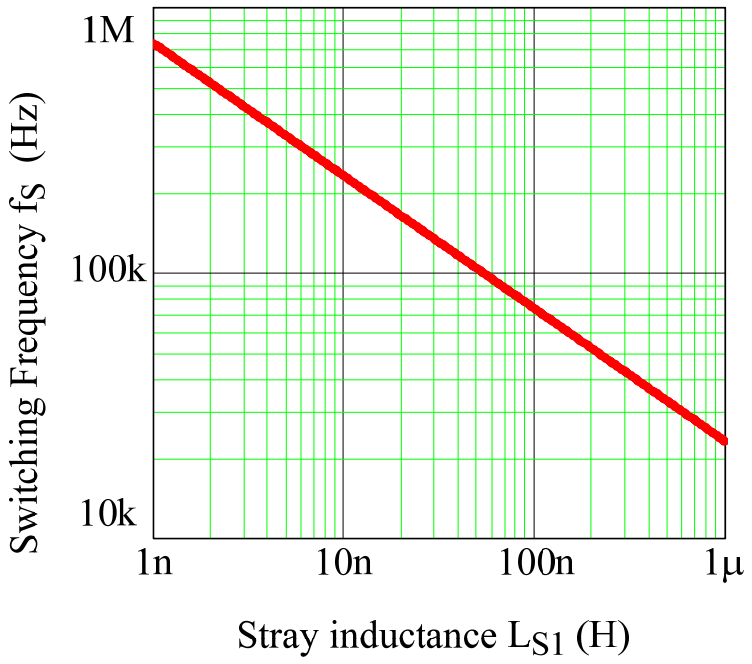


Figure 2.12 ZCS stray inductance and switching frequency

Table 2.1 shows the relevant required stray inductance according to the switching frequency, when the capacitance is 47 μF. When the switching frequency is large than 200 kHz, the required stray inductance is already smaller than the regular circuit layout stray inductance.

Table 2.1 Required stray inductance according to switching frequency

Switching Frequency f_s	Stray inductance L_{S1}
500kHz	2.15 nH
400 kHz	3.37 nH
300 kHz	6 nH
200 kHz	13.5 nH
100 kHz	54 nH
50 kHz	215 nH

Obviously, for other equivalent circuits shown in Figure 2.9, Figure 2.10, Figure 2.11, the stray inductance values of L_{S2}, L_{S3}, L_{S4} for resonant needs to be doubled. The capacitance value becomes half when two capacitors are connected in series in these equivalent circuits. The switching frequency can be easily determined by the actual stray inductance in the circuit. Around 100 kHz and 200 kHz, the most often used switching frequency in dc-dc converter, the needed stray inductance for resonating is less than 55 nH. This is value is small enough to be realized by the stray inductance in the circuit layout or by a small air core. The inductance of a 10 cm long wire or air core inductor is already about 50 nH. Only about 2 nH stray inductances are needed when the switching frequency is increased to 500 kHz. But the stray inductance inside a normal MOSFETs package such as TO-220, is already about 1~2 nH, when several MOSFETs are connected in series, this value could be higher considering the stray inductance of

MOSFET leg which means the switching frequency does not need to be higher than 500 kHz to achieve ZCS.

2.4.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the stray inductance of each module is equalized. The switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

2.5 Power Loss Analysis

2.5.1 Power device loss

2.5.1.1 Conduction loss

Assume the input power is P_{in}, power device turn on resistance is R_{on}, the RMS value of switch current is I_{S_RMS}, the average value of input current is I_{in_ave}, the conversion ratio of the converter is N_T, the conduction loss of power device is P_{S_con}. So the power device conduction loss equation can be derived as follows:

$$I_{in\_ave} = \frac{P_{in}}{V_{in}} \tag{2.27}$$

$$I_{S\_RMS} = \frac{I_{in\_ave}}{N_T}\frac{\pi}{2} \tag{2.28}$$

$$P_{S\_con} = I_{S\_RMS}{}^2 R_{on} \tag{2.29}$$

Plug (2.27) and (2.28) to (2.29), the conduction loss can be derived:

$$P_{S\_con} = \frac{\pi^2 P_{in}{}^2}{4 N_T{}^2 V_{in}{}^2} R_{on} \tag{2.30}$$

2.5.1.2 Gate drive loss

Assume the gate drive voltage is V_{GS}, gate total charge is Q_g, the gate drive loss of power device is P_{S_drv}. So the power device gate drive loss can be derived using the following equation:

$$P_{S\_drv} = V_{GS} Q_g f_s \tag{2.31}$$

2.5.2 Capacitor conduction loss

2.5.2.1 Resonant capacitor conduction loss

Assume the capacitor RMS current is I_{C_RMS}, the capacitor ESR is R_{ESR}, the capacitor conduction loss is P_{C_con}. So the capacitor conduction loss can be derived using the following equation:

$$I_{C\_RMS} = \frac{\pi I_{in\_ave}}{\sqrt{2} N_T} \tag{2.32}$$

$$P_{C\_con} = I_{C\_RMS}{}^2 R_{ESR} \tag{2.33}$$

Plug (2.32) into (2.33),

$$P_{C\_con} = \frac{\pi^2 I_{in\_ave}{}^2}{2 N_T{}^2} R_{ESR} \tag{2.34}$$

Plug (2.27) into (2.34),

$$P_{C\_con} = \frac{\pi^2 {P_{in}}^2}{2{N_T}^2 {V_{in}}^2} R_{ESR} \tag{2.35}$$

2.5.2.2 Input capacitor conduction loss

Assume the RMS value of input current is I_{in_RMS}, the capacitor ESR is R_{ESR_in}, the conduction loss of input capacitor is P_{Cin_con}. The input current can be shown Figure 2.13

$$I_{in\_RMS} = \frac{\pi I_{in\_ave}}{2\sqrt{2}} \tag{2.36}$$

$$P_{Cin\_con} = {I_{in\_RMS}}^2 R_{ESR\_in} \tag{2.37}$$

Plug (2.36) into (2.37) one can get,

$$P_{Cin\_con} = \frac{\pi^2 {I_{in\_ave}}^2}{8} R_{ESR\_in} \tag{2.38}$$

Plug (2.27) into (2.38) one can get,

$$P_{Cin\_con} = \frac{\pi^2 {P_{in}}^2}{8{V_{in}}^2} R_{ESR\_in} \tag{2.39}$$

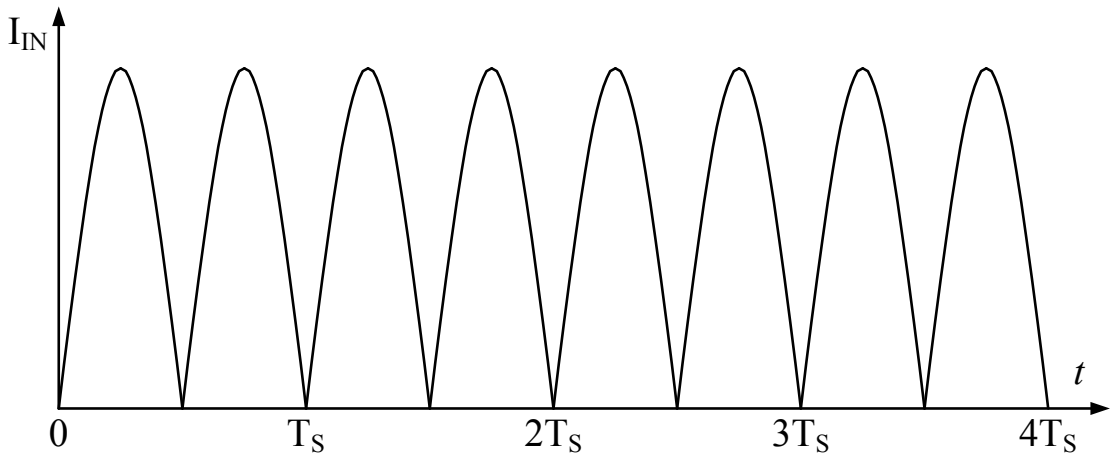


Figure 2.13 Ideal input current waveform

2.5.3 Total power loss

There are $3N_T - 2$ switching devices and N_T capacitors in a N_T level ZCS-MMSCC, so the total power loss P_{loss} is:

$$P_{loss} = (3N_T - 2)(P_{S\_con} + P_{S\_drv}) + N_T P_{C\_con} + P_{Cin\_con} \tag{2.40}$$

Plug (2.30), (2.31), and (2.34) into (2.40), one can get

$$P_{loss} = (3N_T - 2)(\frac{\pi^2 {P_{in}}^2 R_{on}}{4{N_T}^2 {V_{in}}^2} + V_{GS} Q_g f_s) + \frac{\pi^2 {P_{in}}^2 R_{ESR}}{2N_T {V_{in}}^2} + \frac{\pi^2 {P_{in}}^2 R_{ESR\_in}}{8{V_{in}}^2} \tag{2.41}$$

Assume η is the converter efficiency

$$\eta = \frac{P_{in} - P_{loss}}{P_{in}} \tag{2.42}$$

Plug (2.41) into (2.42), one can get:

$$\eta = \frac{P_{in} - (3N_T - 2)(\frac{\pi^2 {P_{in}}^2 R_{on}}{4{N_T}^2 {V_{in}}^2} + V_{GS} Q_g f_s) - \frac{\pi^2 {P_{in}}^2 R_{ESR}}{2N_T {V_{in}}^2} - \frac{\pi^2 {P_{in}}^2 R_{ESR\_in}}{8{V_{in}}^2}}{P_{in}} \tag{2.43}$$

2.6 Simulation and Experiment Results

2.6.1 A 150 W four-level ZCS-MMSCC prototype

Figure 2.14 shows saber simulation waveforms of a 150 W four-level ZCS-MMSCC, where Vgs_Sp and Vgs_Sn are the switch gate-source control voltage, Vds_Sp1 and Vds_Sn2 are the switch drain-source voltage, Id_Sp1 and Id_Sn2 are the switch drain-source current. The input voltage is 5 V. Switching frequency is about 45 kHz. Capacitance is 47 μF and stray inductance L_{S1} is about 250 nH and 500 nH for others. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

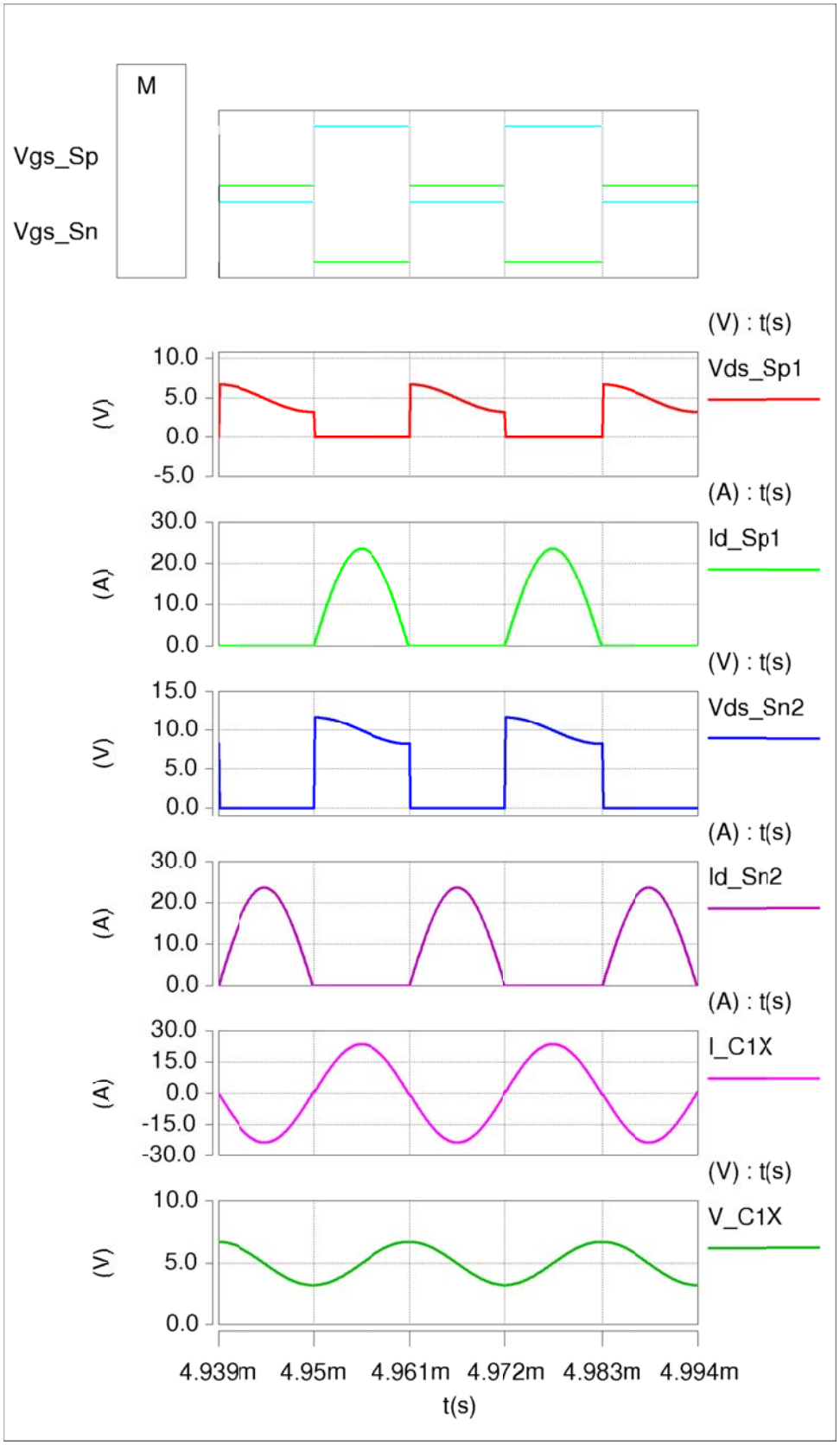


Figure 2.14 Simulation waveforms of 150 W four-level ZCS-MMSCC

In the 150 W 4-level ZCS-MMSCC prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 µF MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are fourteen 6.3 V 470 µF conductive polymer aluminum solid electrolytic capacitors PLE0J471MDO1from nichicon connected in parallel. Gate drive voltage is 15 V. Figure 2.15-Figure 2.18 shows the experiment waveforms of the 150 W 4-level ZCS-MMSCC prototype with the parts mentioned above. Figure 2.15 shows the complementary gate drive signals of S_P and S_N with duty cycle about 48% due to some dead time. V_{GS_SP} and V_{GS_SN} are the complementary gate-source control voltage.

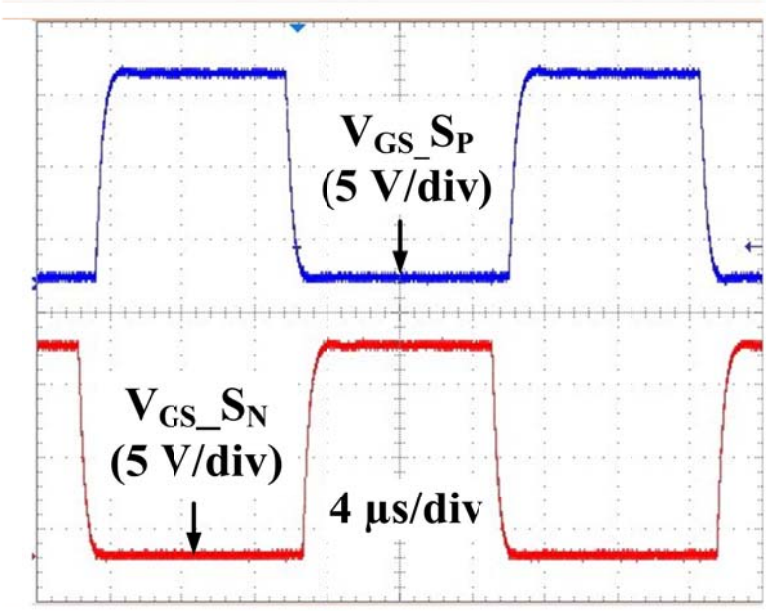


Figure 2.15 Gate drive signal of S_P and S_N

Figure 2.16 shows the voltage and current waveforms of S_{P1}. V_{GS} is the gate-source voltage of S_{P1}, V_{DS} is the drain-source voltage of S_{P1} and I_D is drain-source current of S_{P1}.The resonant current waveform realizing ZCS is shown. Figure 2.17 shows the zoomed in waveforms

of the switch S_{P1} turn off transient, which indicates that the switch achieves ZCS during turn off. From the experiment results, we can derive that the switch S_{P1} can achieve ZCS in both turn on and turn off. Other switches have the voltage and current waveforms similar to S_{P1} which will not shown here.

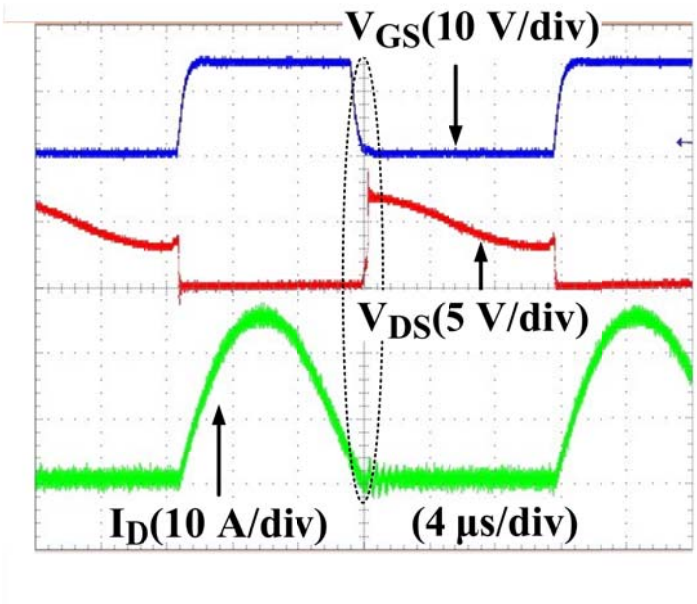


Figure 2.16 Voltage and current waveform of S_{P1}

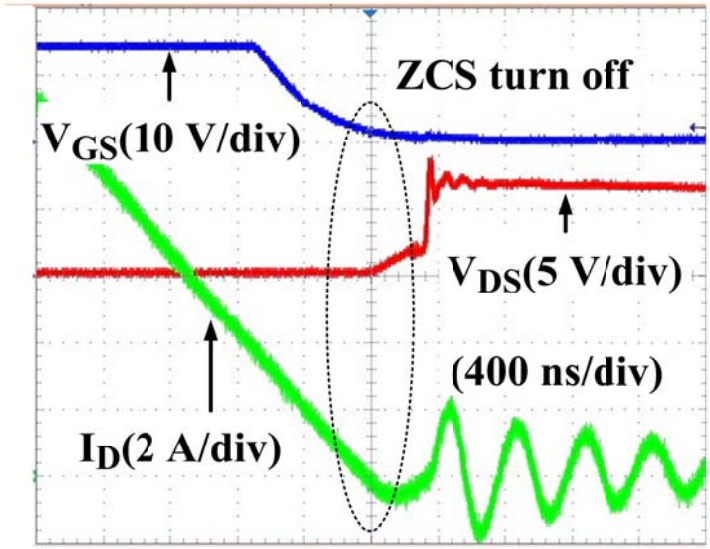


Figure 2.17 Zoomed in voltage and current waveforms of S_{P1}

Figure 2.18 shows the measured efficiency curve using Yokogawa WT1600 digital power meter of proposed ZCS-MMSCC and the calculated efficiency using (2.43). And the efficiency is above 97% which is a big improvement than traditional MMSCC.

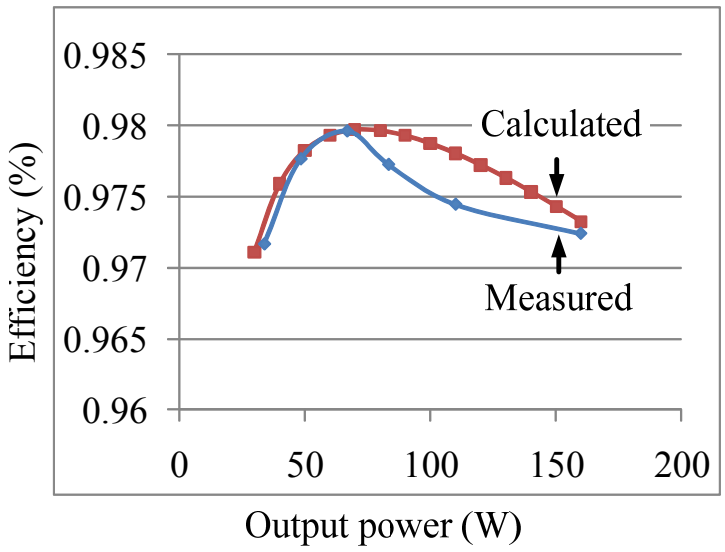


Figure 2.18 Measured Efficiency and Calculated Efficiency

2.7 Conclusion

The presented ZCS-MMSCC has all the advantages of ZCS and MMSCC. And it has some special features besides the features got from ZCS and MMSCC. All the features can be concluded as follows:

- reduces dv/dt, di/dt and EMI because of ZCS;
- reduces the switching loss which improves efficiency;
- uses simple control strategy and possesses modular structure and bidirectional power conversion;
- increases the potential power rating by using MLCC capacitor;
- reduces the capacitance and capacitor size, which lowers the cost
- utilizes distributed stray inductance to achieve ZCS which improves reliability.

A new soft-switching operation strategy to the existing MMSCC has been proposed and validated by both simulation and experiment results. A 150 W, 5 V input four-level converter prototype for automotive application has been built and tested based on proposed circuit. And the efficiency of the prototype is higher than 97%. The ZCS-MMSCC overcomes the current and voltage spike problems of traditional MMSCC and provides a technically viable soft-switching strategy with circuit layout stray inductance. This technique could also be applied to the switched-capacitor circuits on a semiconductor chip with very small stray inductance in the circuit without pushing the switching frequency to megahertz. The proposed ZCS-MMSCC also shows great potential to high voltage gain and high input current applications.

CHAPTER 3
A Family of ZCS Switched-Capacitor DC-DC Converters

This Chapter presents a new zero current switching technique for a family of switched-capacitor dc-dc converters. Compared to the traditional ZCS switched-capacitor dc-dc converter by inserting a relatively big inductor in the circuit, these new ZCS switched-capacitor dc-dc converters employ the stray inductance present in the circuit as the resonant inductor and provide soft-switching for the devices. These ZCS switched-capacitor dc-dc converters do not utilize any additional components to minimize switching loss and reduce current and voltage spike, thus leading to high efficiency and reliable benefit over traditional switched-capacitor dc-dc converters. Moreover, the bulky capacitor bank existing in traditional switched-capacitor circuits for high power high current application to achieve high efficiency was reduced significantly. So, small size, low capacitance, low ESR, high current rating and high temperature rating ceramic capacitors can be employed. Therefore, by using proposed ZCS technique, smaller size, higher power density, higher efficiency, higher temperature rating, and higher current rating switched-capacitor dc-dc converter could be built. Simulation and experimental results are given to demonstrate the validity and features of the soft switching switched-capacitor dc-dc converters.[3]

3.1 Introduction

With the technological development of silicon carbide (SiC) and ceramic materials, very high temperature (250 °C) SiC switching devices and ceramic capacitors will be available. But the

[3] This work has been present in part at the 25nd annual IEEE Applied Power Electronics Conference and Exposition, Palm Spring, CA USA, Feb. 21 – Feb. 25 2010.

magnetic cores become dysfunctional at very high temperature. Therefore, magnetic-less switched-capacitor dc-dc converters operating at very high temperatures become possible and attractive with the adoption of natural air cooling by eliminating bulky heat sinks and magnetic cores. There are three main basic structures of switched-capacitor of dc-dc converters that is most popular, Marx generator type voltage multiplier shown in Figure 3.1 [73-75], charge pump type multi-level modular switched-capacitor dc-dc converter shown in Figure 3.2 [76, 78], and generalized multi-level type switched-capacitor dc-dc converter shown in Figure 3.3 [81-83, 96, 101].

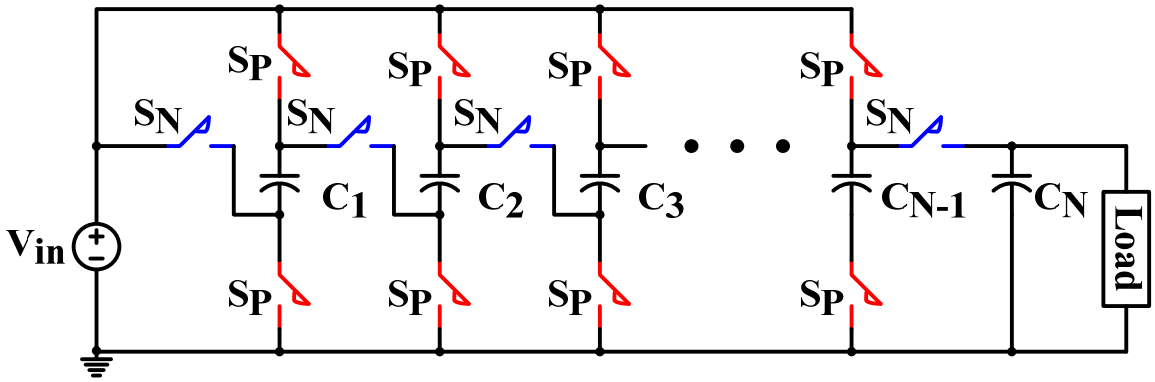


Figure 3.1 Voltage multiplier

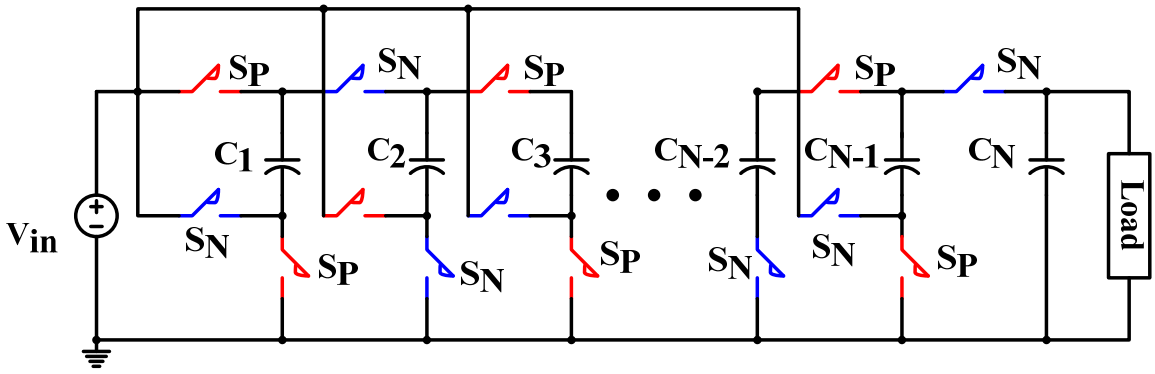


Figure 3.2 Multilevel modular switched-capacitor dc-dc converter.

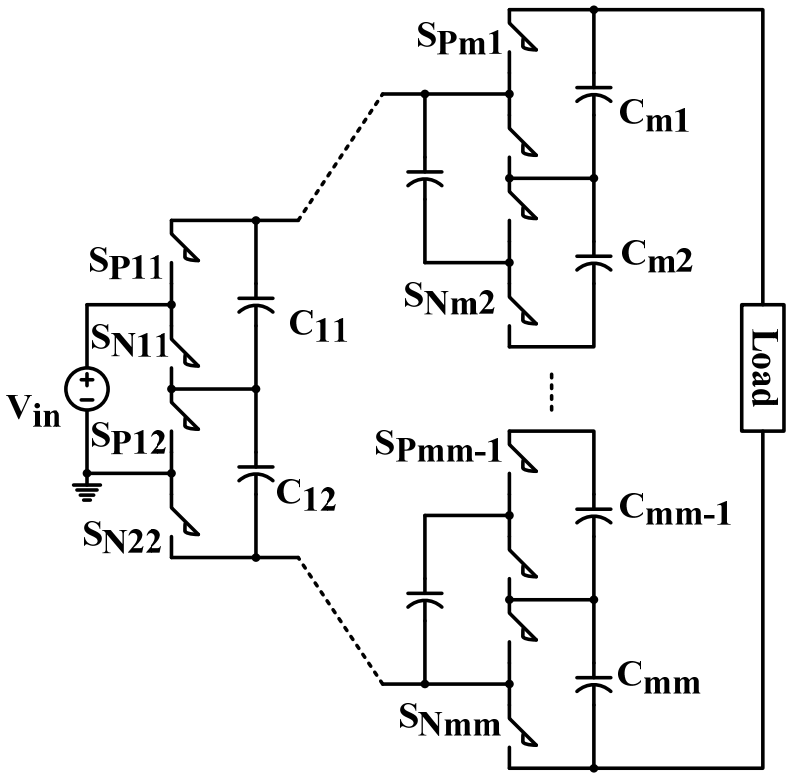


Figure 3.3 Generalized multi-level switched-capacitor dc-dc converter.

However, there are many common drawbacks in traditional switched-capacitor dc-dc converters in high power and high current automotive application. A huge capacitor bank with high capacitance has to be utilized in order to reduce the voltage ripple of the capacitors and achieve high efficiency, which will undoubtedly increase the size of the converter [82, 94, 95, 102]. Besides, with the increase of switching frequency, the switching loss of the device becomes more and more unneglectable. Moreover, huge current spikes, big voltage overshoot caused by large turn off current and EMI problems caused by the di/dt and dv/dt generated during the switching transient are undesirable in automotive applications. In order to reduce the switching loss, voltage spikes, current spikes and EMI, several ZCS methods have been proposed [84-88, 103]. But adding a relatively big resonant inductor in the switched-capacitor circuit to achieve ZCS is a contradiction by itself. Also, by using the methods mentioned above, switching frequency has to be pushed to tens of megahertz to utilize parasitic inductance which is not

technically feasible [92, 93, 104]. A charge pump type ZCS multi-level modular switched-capacitor dc-dc converter has been proposed recently. By utilizing the distributed parasitic inductance present in the circuit, switching frequency need not to be increased to megahertz, no big inductors are needed to be inserted [105]. By applying the ZCS strategy proposed in [105] to the existing switched-capacitor circuits, a family can be generated.

This chapter presents a family of ZCS switched-capacitor dc-dc converters that is able to overcome the aforementioned drawbacks of traditional switched-capacitor dc-dc converters without inserting big magnetic cores or increasing switching frequency. This new strategy can achieve the ZCS of all the switches without losing the good features of switched-capacitor circuit compared to the traditional ZCS strategy. This ZCS strategy employs the distributed parasitic inductance in the circuit resonating with the capacitors to provide low di/dt and dv/dt to the switching devices. So, the switching loss is minimized, current spike and voltage spike are reduced and EMI is limited. In case the stray inductance is not sufficiently large or equalized, small air core inductors (less than 100n) can be used to meet the requirement of the stray inductance. The power loss is only related to the conduction loss and gate drive loss of switching devices and capacitors by considering the influence of stray inductance. Therefore, bulky capacitor banks with high capacitance are no longer needed to achieve high efficiency, while small MLCC capacitors with low ESR and low capacitance can be adopted to increase efficiency reduce the size. No extra components are added in the presented soft switching strategy, thus making it reliable and low in cost. A 630 W twelve-level ZCS charge pump type switched-capacitor dc-dc converter and a 480 W ZCS voltage doubler were built to confirm the operation.

3.2 Proposed ZCS Switched-Capacitor DC-DC Converter Family

Figure 3.4, Figure 3.5, and Figure 3.6 show the proposed ZCS switched-capacitor family utilizing the distributed parasitic inductance existing in the circuit. Figure 3.4 shows the N-level ZCS voltage multiplier. Figure 3.5 shows the N-level ZCS MMSCC which has already been discussed in detail in chapter 3. Figure 3.6 shows the N-level ZCS generalized multi-level switched capacitor dc-dc converter.

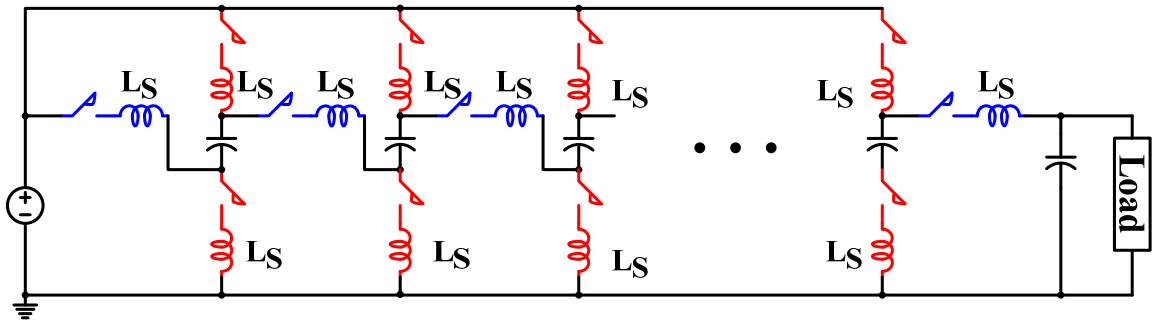


Figure 3.4 ZCS voltage multiplier

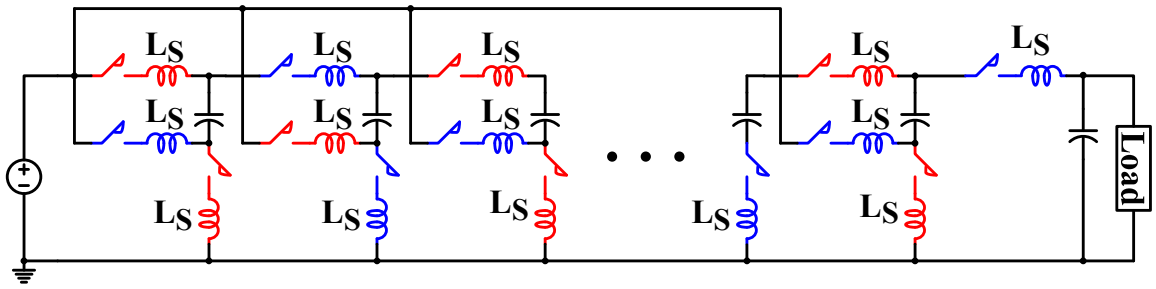


Figure 3.5 ZCS multi-level modular switched-capacitor dc-dc converter

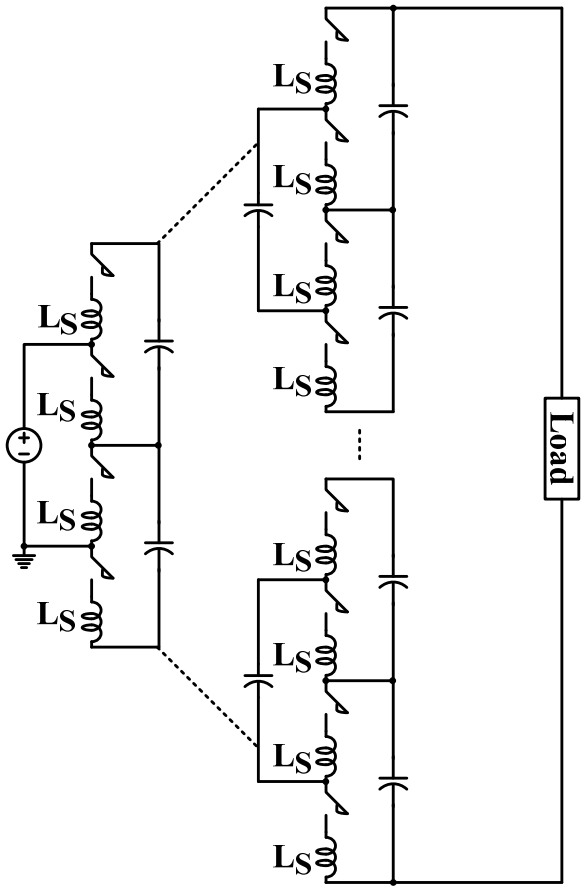


Figure 3.6 ZCS generalized multi-level switched-capacitor dc-dc converter.

The parasitic inductance mainly includes the stray inductance due to the circuit layout, MOSFETs package parasitic inductance and the capacitor ESL. The stray inductance caused by circuit layout is usually the dominant part. By designing the circuit layout specially or inserting specific length of wires which is an air core inductor in the circuit, the inductance needed for resonant is achieved. Because resonant inductors or the inserted wires are distributed in the circuit properly, only small resonant inductance is needed for resonant. Therefore, ZCS of all the switching devices can be achieved by the resonant of the capacitor and the circuit layout stray inductance or inserted wires. In the following parts, two examples of proposed ZCS switched-capacitor dc-dc converters are analyzed, simulation and experimental results are given.

3.3 Operation Principle

Since ZCS-MMSCC has already been discussed in detail in chapter 3, only ZCS voltage multiplier and ZCS generalized switched-capacitor dc-dc converter is going to be discussed here.

3.3.1 ZCS voltage multiplier

Figure 3.7 shows the four-level ZCS voltage multiplier as an example. Similar to the four-level ZCS-MMSCC, this circuit also works as a four times step-up dc-dc converter. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in the circuit. L_{S2}, L_{S4} and L_{S6} are the equivalent stray inductance when the capacitor is charged in parallel. L_{S1}, L_{S3}, L_{S5} and L_{S7} are the equivalent stray inductance between each capacitor when the capacitor discharges in series. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_1 to C_3 are the capacitors with the average voltage of input voltage, while C_4 has the average voltage of four times of input voltage. L_S does not have to be in the position drawn in Figure 3.7, it could be distributed anywhere in series with switches or capacitors in the circuit shown in Figure 3.4 or similar to Figure 2.4. Similar to the ZCS-MMSCC, the total stray inductance could be sum of the connection wire parasitic inductance L_{SW}, capacitor parasitic inductance L_{ESL} and the MOSFETs package parasitic inductance L_{Sp}. Usually the connection wire parasitic inductance L_{SW} is the major part of the stray inductance. For the analysis convenience, only one equivalent L_S is used to represent the total stray inductance present in each parallel resonant loop. And one equivalent L_S is used between two capacitors in the series resonant loop.

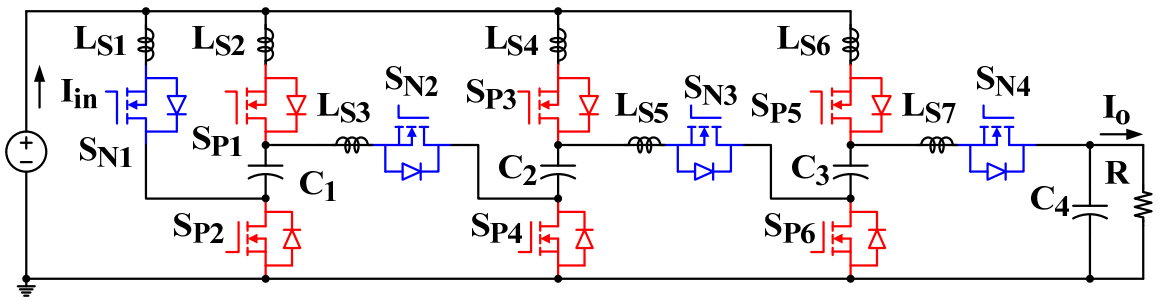


Figure 3.7 Four-level ZCS voltage multiplier main circuit.

Figure 3.8 shows the idealized waveform of proposed ZCS voltage multiplier under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assume input voltage is an ideal voltage source. By considering the stray inductance present in the circuit, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches S_P, S_N and stray inductance will decrease to zero when the switches are turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. The capacitor C_1 C_2 and C_3 are charged in parallel in half-period with the sinusoidal current waveform when S_P is on. And they are discharged in series with the input voltage source in another half-period also in the sinusoidal shape when S_N is on. So, the current through the capacitor C_1, C_2, and C_3 is the sum of the current through the switch, which is a sinusoidal waveform.

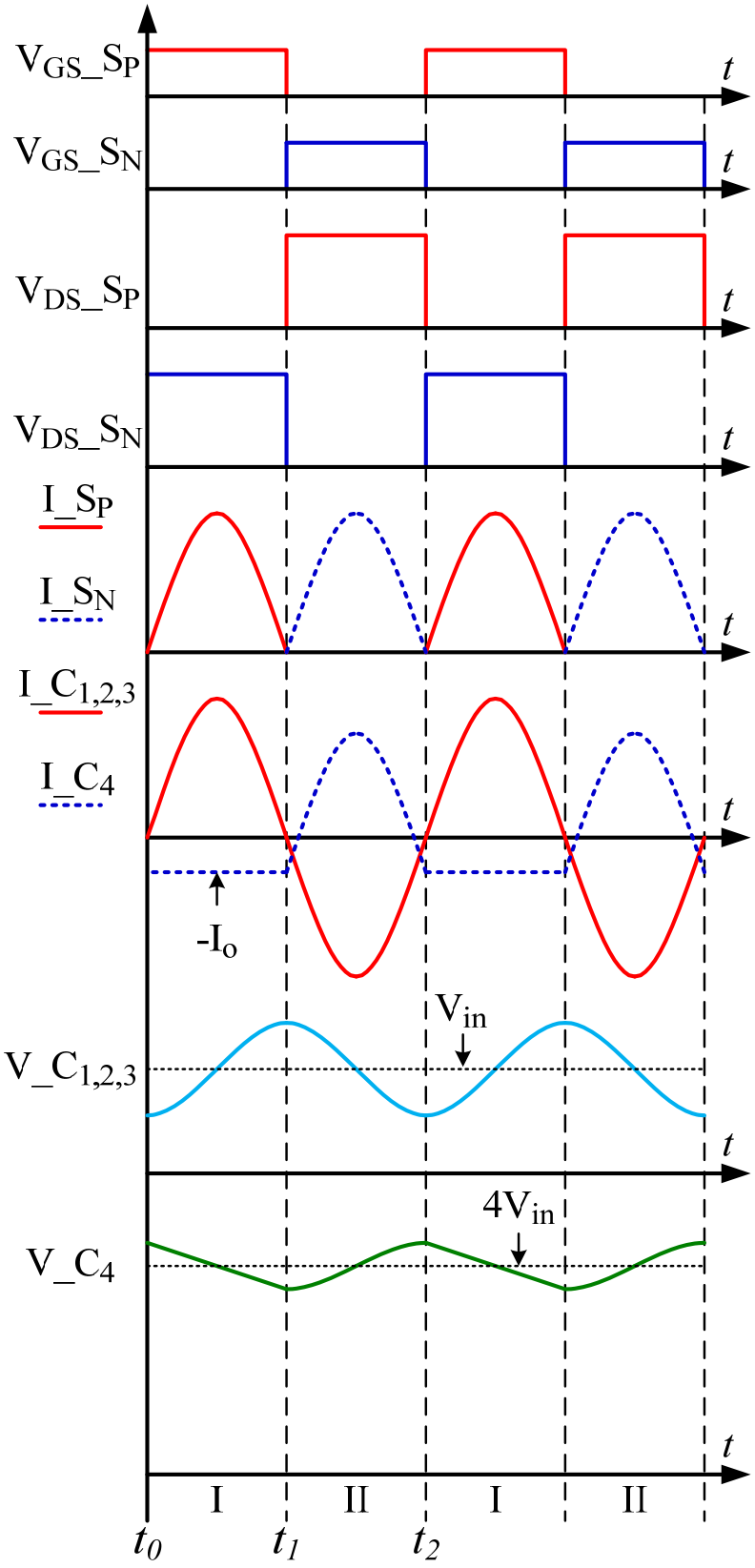


Figure 3.8 Ideal waveforms of four-level ZCS voltage multiplier.

The capacitor C_4 is charged when other capacitors are in series with input voltage. And it is discharged to the load. So the current through capacitor C_4 is a sinusoid waveform when S_N is on with a negative dc output current offset. When S_P is on, the current through C_4 is the load current. When the capacitor is charged, the current is positive; when the capacitor discharges, the current is negative. The voltage across the capacitor C_1, C_2 and C_3 has a dc offset of input voltage with a sinusoidal ripple. The voltage ripple is determined by the capacitor current and capacitance. The voltage across the capacitor C_4 has a dc offset of four times input voltage with voltage ripple also determined by the capacitor current and capacitance. The operation of the circuit can be described in two states as shown in Figure 3.9 and Figure 3.10 with different switch is turned on.

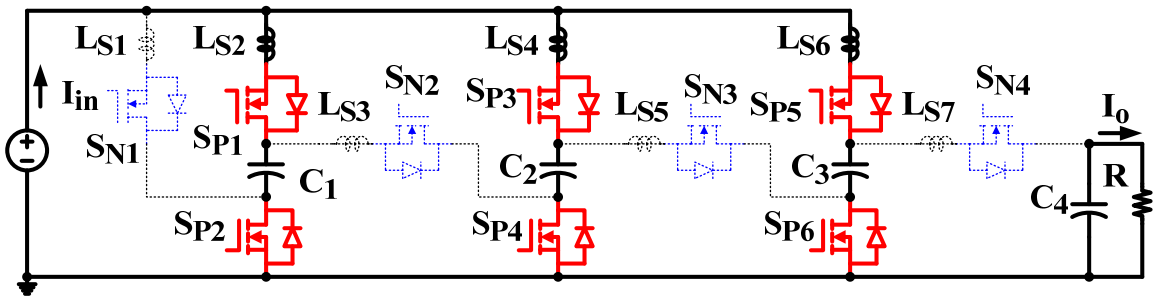


Figure 3.9 Operation modes state I S_P is on.

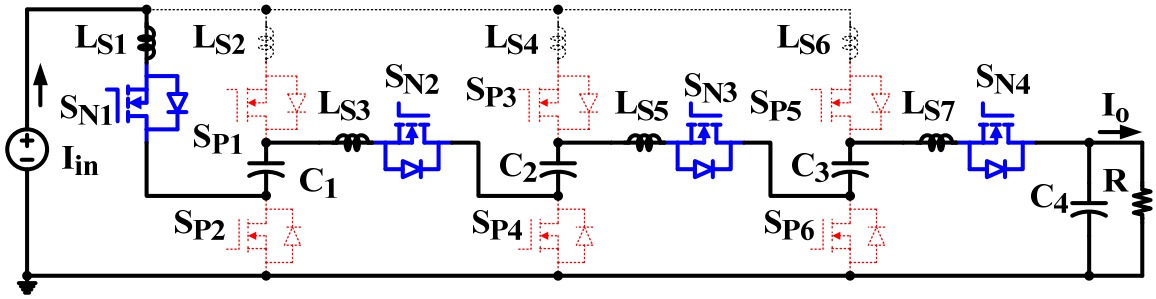
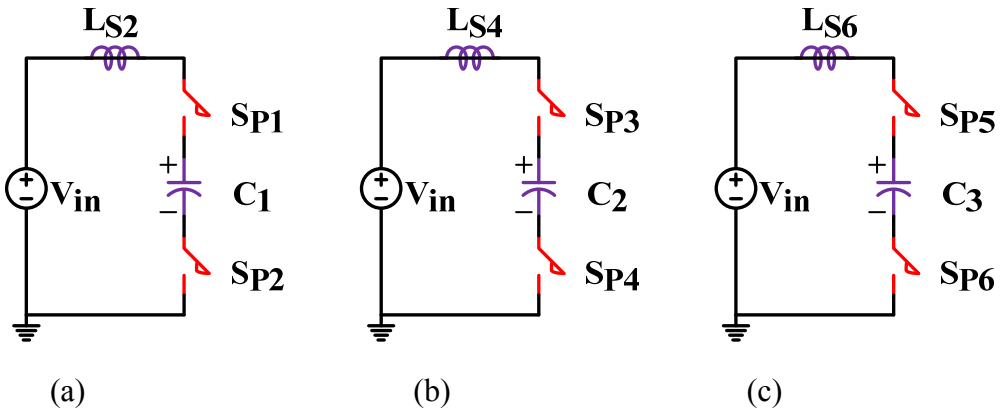


Figure 3.10 Operation modes state II S_N is on.

3.3.1.1 State I [t_0,t_1]

Figure 3.9 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_1, C_2 and C_3 are charged by V_{in}. Figure 3.11 shows the three simplified equivalent circuits of state I. Figure 3.11(a) shows the situation when V_{in}, L_{S2}, S_{P1}, C_1 and S_{P2} form a resonant loop. Figure 3.11(b) shows the situation when V_{in}, L_{S4}, S_{P3}, C_2 and S_{P4} form a resonant loop. Figure 3.11(c) shows the situation when V_{in}, L_{S6}, S_{P5}, C_3 and S_{P6} form a resonant loop. Because of the presence of the stray inductance L_S, before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. For the case shown in Figure 3.11(a), after L_{S2} and C_1 resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} turn off at zero current. Similarly, for the case shown in Figure 3.11(b) and Figure 3.11(c) the current through S_{P3}, S_{P4}, S_{P5} and S_{P6} will realize zero current turn on and turn off too. So, ZCS is achieved on all the switches. The required stray inductance value is the same for the three circuit and is easy to be achieved by the circuit layout due to the symmetry of the circuit, assuming the capacitance are the same.

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assuming $C_1 = C_2 = C_3 = C_4$, so in order to have the same resonant frequency, $L_{S1} = L_{S2} = L_{S3} = L_{S4} = L_{S5} = L_{S6} = L_{S7}$.



(a) (b) (c)

Figure 3.11 Simplified equivalent circuits of state I

The state equations of Figure 3.11(a) are

$$V_{in} = L_{S2}\frac{di_{L_{S2}}}{dt} + v_{C_1} \tag{3.1}$$

$$i_{L_{S2}} = C_1\frac{dv_{C_1}}{dt} \tag{3.2}$$

The solutions are:

$$i_{S2}(t) = \frac{\pi P_o}{4V_{in}}\sin\omega_r t \tag{3.3}$$

$$v_{C_1}(t) = V_{in} - \frac{\pi P_o}{4V_{in}C_1\omega_r}\cos\omega_r t \tag{3.4}$$

Where V_{in} is the value input voltage, L_{S2} is the value of stray inductance, ω_r is the resonant frequency equals to $1/\sqrt{L_{S1}C_1}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to:

$$v_{C_1}(t_1) = V_{in} + \frac{\pi P_o}{4V_{in}C_1\omega_r} \tag{3.5}$$

The capacitor voltage ripple is:

$$\Delta v_{C_1} = \frac{\pi P_o}{4V_{in}C_1\omega_r} \tag{3.6}$$

The state equations of Figure 3.11(b) and Figure 3.11(c) are similar to the state equations of Figure 3.11(a). The voltage across C_2 and C_3 are exactly the same as the voltage across C_1. The voltage ripple of C_2 and C_3 are also the same as Δv_{C_1}.

3.3.1.2 State II [t_1,t_2]

Figure 3.10 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state, C_4 is charged by the V_{in} C_1 C_2 and C_3 in series. Figure 3.12 shows the simplified equivalent circuits of state II. It shows the situation when V_{in}, L_{S1}, S_{N1}, C_1, L_{S3}, S_{N2}, C_2, L_{S5}, S_{N3}, C_3, L_{S7}, S_{N4}, and C_4 form a resonant loop. Similar as the last state, because of the presence of the L_S, the current through S_N will also increase its value from zero in a resonant manner. The zero current turn-on of S_N can be achieved. After stray inductance L_{S1}, L_{S3}, L_{S5} and L_{S7} in series resonate with capacitor C_1, C_2, C_3 and C_4 in series for half cycle at $t = t_2$, S_{N1}, S_{N2}, S_{N3} and S_{N4} will have a zero current turn-off when the current through them decreases to zero. Hence, zero current switching can be achieved on these switches.

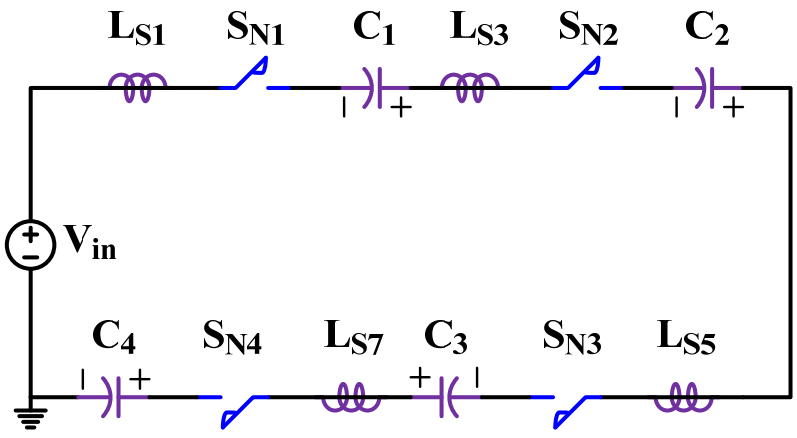


Figure 3.12 Simplified equivalent circuits of state II

The state equations of Figure 3.12 are:

$$V_{in} + v_{C_1} + v_{C_2} + v_{C_3} = 4L_{S1}\frac{di_{L_{S1}}}{dt} + v_{C4} \tag{3.7}$$

$$i_{L_{S1}} = C_4\frac{dv_{C_4}}{dt} \tag{3.8}$$

The solutions are:

$$v_{C4}(t) = 4V_{in} - \frac{\pi P_o}{4V_{in}C_4\omega_r}\cos\omega_r t \tag{3.9}$$

$$i_{L_{S1}}(t) = \frac{\pi P_o}{4V_{in}}\sin\omega_r t \tag{3.10}$$

After half cycle, the capacitor voltage is charged to

$$v_{C_4}(t_2) = 4V_{in} + \frac{\pi P_o}{4V_{in}C_4\omega_r} \tag{3.11}$$

The capacitor voltage ripple is:

$$\Delta v_{C_4} = \frac{\pi P_o}{4V_{in}C_4\omega_r} \tag{3.12}$$

All the capacitors have the same voltage ripple and the voltage ripple depends on the output power, input voltage, capacitance and the resonant frequency.

3.3.2 ZCS voltage doubler

Figure 3.7 shows the two-level ZCS generalized multi-level switched-capacitor dc-dc converter an example. This circuit can be also called as the ZCS voltage doubler in short, because this circuit works as a two times step-up dc-dc converter. V_{in} represents the ideal input voltage source. L_S represents the equivalent stray inductance present in the circuit. L_{S1}, L_{S2} L_{S3} and L_{S4} can be considered as the stray inductance in series with the switch during the circuit layout. S_P and S_N are the same switching devices controlled complementary at 50% duty cycle. C_1 and C_2 are the capacitors with the average voltage the same as the input voltage.

Because of the symmetry of the circuit, the distributed stray inductance L_{S1}, L_{S2} L_{S3} and L_{S4} can be replaced with an equivalent stray inductance L_S in the input side shown in Figure 3.14 for the analysis convenience. Only one equivalent stray inductance L_S is needed to represent the total stray inductance in two resonant loop.

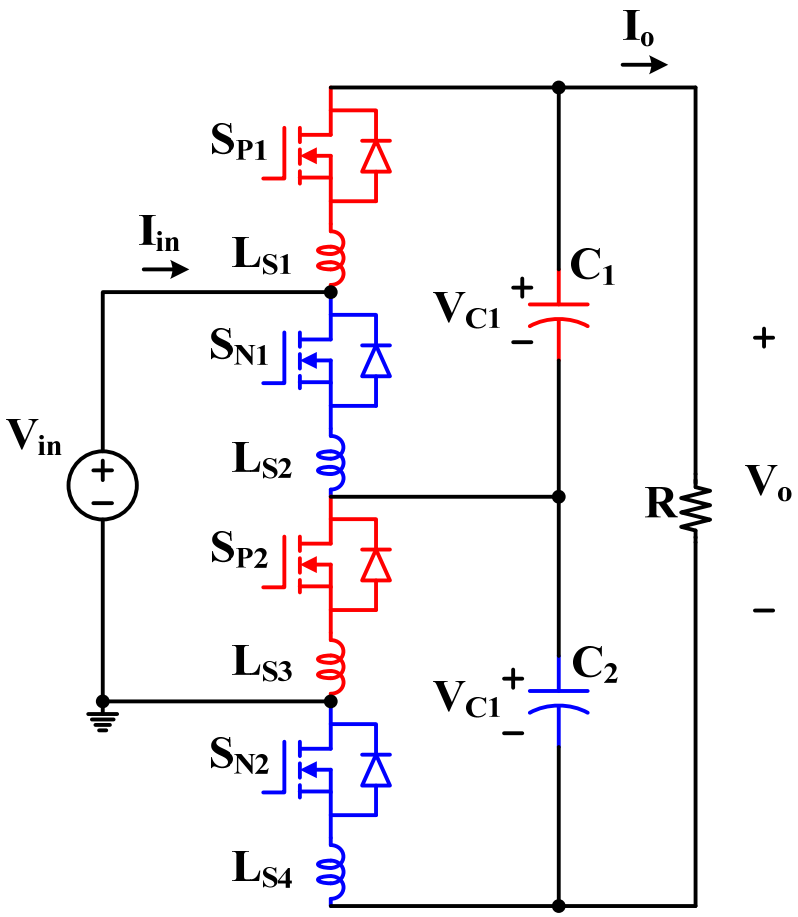


Figure 3.13 ZCS voltage doubler main circuit.

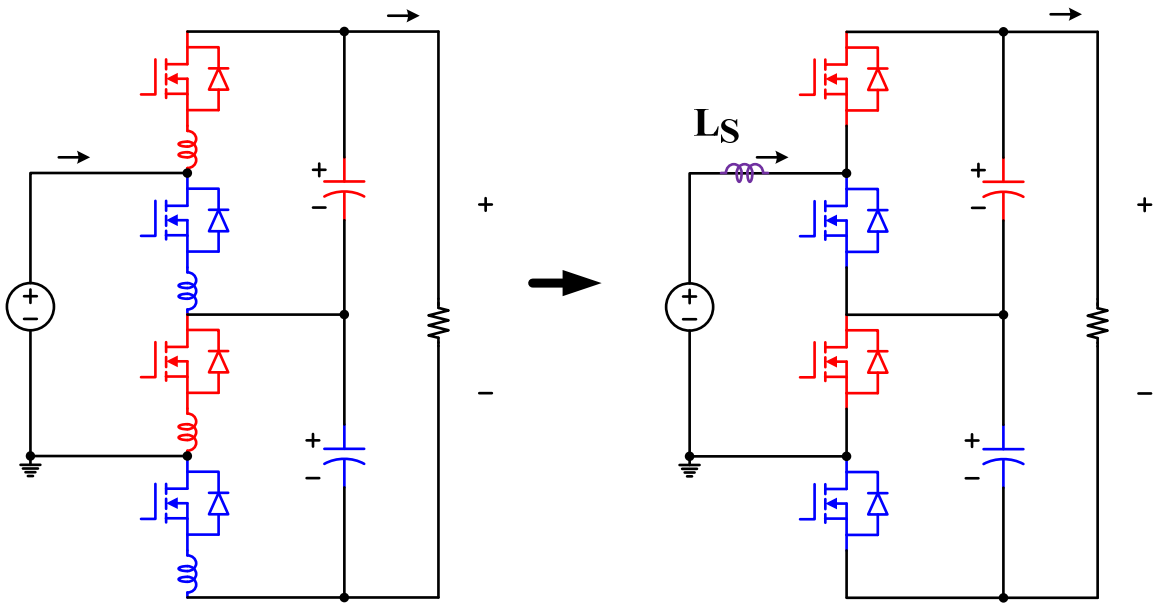


Figure 3.14 ZCS voltage doubler topology simplification.

Figure 3.15 shows the idealized waveform of proposed ZCS voltage doubler under steady-state conditions. The gate signal of switch S_P and S_N is complementary, and duty cycle is 50%. Assume input voltage is an ideal voltage source. By considering the equivalent stray inductance in the input side, when the switches are turned on, the current through the stray inductance, capacitors and the switch will begin to resonate from zero. By adjusting switching frequency to the resonant frequency, the current through switches S_P, S_N and stray inductance will decrease to zero when the switches are turned off, which is the half period of the sinusoidal waveform. Therefore, the ZCS of all the switches is achieved in both turn on and turn off. The capacitor C_1 and C_2 are charged in each half-period with the sinusoidal current waveform when S_P or S_N is on. And they are always discharged in series So, the current through the capacitor C_1, and C_2, is the current through the switch subtracts the output current. The output voltage ripple is half of the voltage ripple of the capacitor, because of the 180 degree phase shift of the capacitor voltage ripple. The capacitor voltage ripple will cancel with each other. The operation of the circuit can

be described in two states as shown in Figure 3.16 and Figure 3.17 with different switch is turned on.

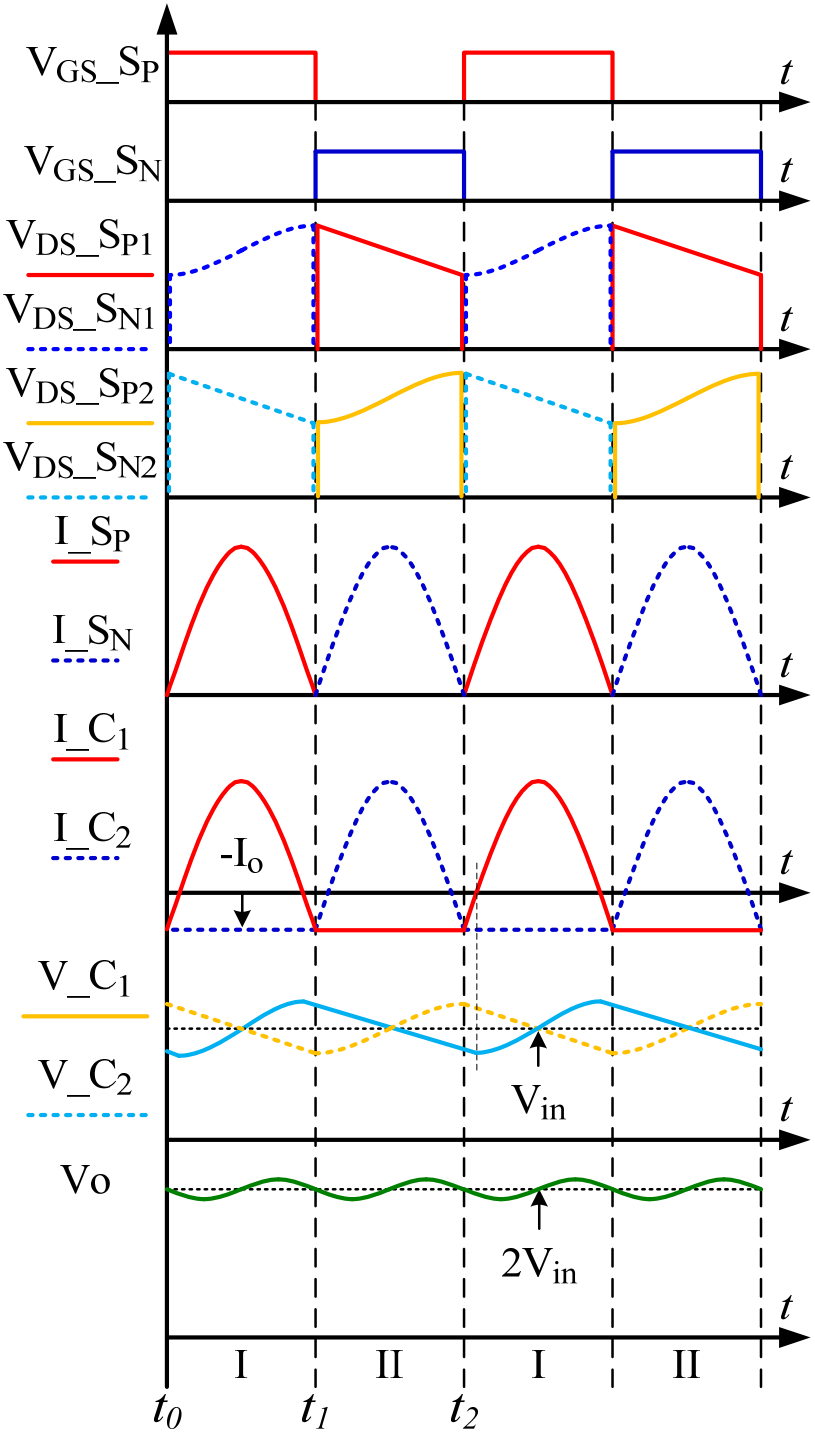


Figure 3.15 Ideal waveforms of ZCS voltage doubler.

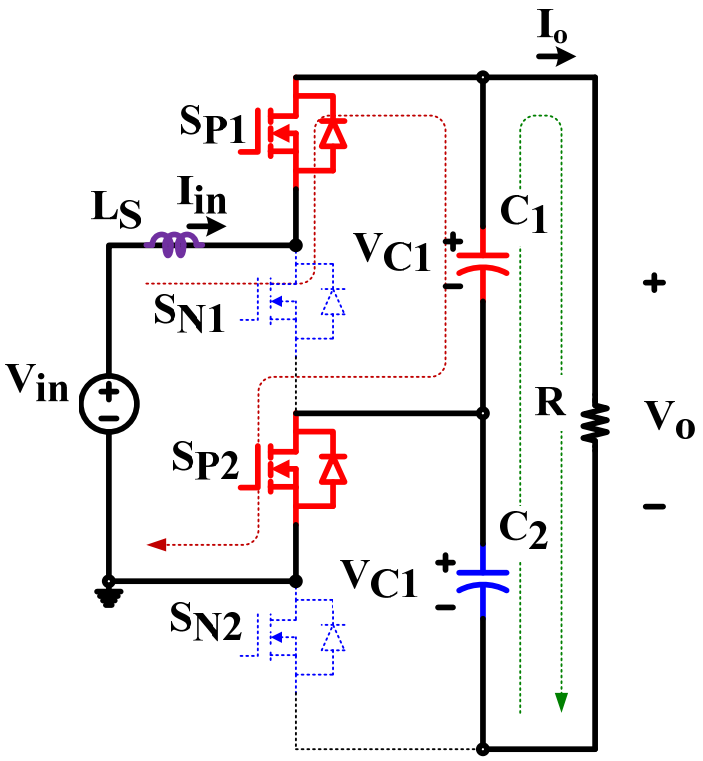


Figure 3.16 Operation modes of state I when S_P is on.

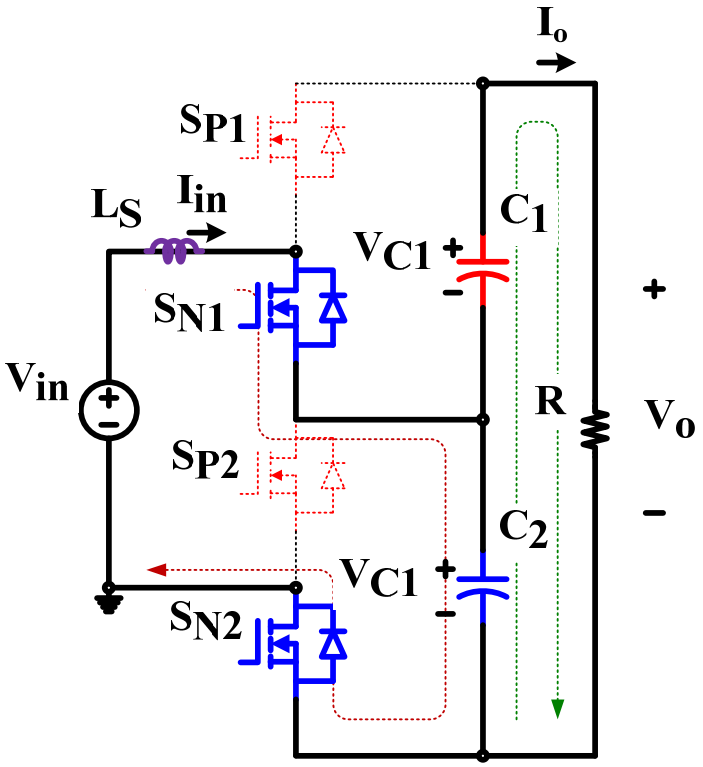


Figure 3.17 Operation modes of state II when S_N is on.

3.3.2.1 State I [t_0,t_1]

Figure 3.16 shows the state when S_P is turned on at $t = t_0$ while S_N is off. During this state C_1 is charged by V_{in}. Figure 3.18 shows the simplified equivalent circuits of state I. It shows the situation when V_{in}, L_S, S_{P1}, C_1 and S_{P2} form a resonant loop. Because of the presence of the stray inductance L_S, before the switch is turned on, the current through L_S already decreases to zero. The current through S_P will increase from zero when the switch is turned on, so S_P is turned on at zero current. After L_S and C_1 resonate for half cycle, the current through S_{P1} and S_{P2} falls to zero. Therefore S_{P1} and S_{P2} turn off at zero current. So, ZCS is achieved on all the switches.

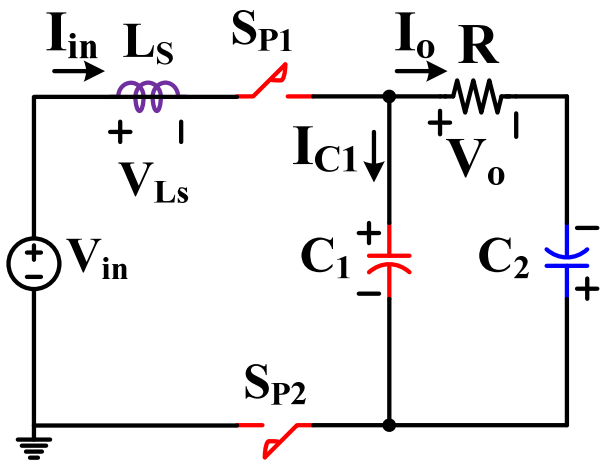


Figure 3.18 Simplified equivalent circuits of state I

Without loss of generality, the following assumptions have been made for the analysis: all the switches are ideal, i.e. no conduction resistance is considered; input voltage source is ideal, i.e. constant and no internal impedance; the capacitor ESR is zero. Assume $C_1 = C_2$. The state equations of Figure 3.18 are:

$$V_{in} = L_S \frac{di_{LS}}{dt} + v_{C1} \tag{3.13}$$

$$i_{L_S} = C_1 \frac{dv_{C1}}{dt} + I_o \tag{3.14}$$

$$-I_o = C_2 \frac{dv_{C2}}{dt} \tag{1.15}$$

$$I_o = \frac{P_o}{2V_{in}} \tag{1.16}$$

And the solutions are:

$$v_{C_1}(t) = V_{in} - \frac{\pi P_o}{2V_{in}C_1\omega_r}\cos\omega_r t \tag{3.17}$$

$$v_{C_2}(t) = -\frac{P_o}{2V_{in}C_2}t + V_{in} + \frac{\pi P_o}{2V_{in}C_2\omega_r} \tag{1.18}$$

$$i_{L_S}(t) = \frac{\pi P_o}{2V_{in}}\sin\omega_r t \tag{3.19}$$

Where V_{in} is the value input voltage, L_S is the value of stray inductance, ω_r is the resonant frequency equals to $1/\sqrt{L_S C_1}$, and P_o is the output power. After half cycle, the capacitor voltage is charged to:

$$v_{C_1}(t_1) = V_{in} + \frac{\pi P_o}{2V_{in}C_1\omega_r} \tag{3.20}$$

The capacitor voltage ripple is:

$$\Delta v_{C_1} = \frac{\pi P_o}{2V_{in}C_1\omega_r} \tag{3.21}$$

3.3.2.2 State II [t_1,t_2]

Figure 3.17 shows the state when S_N is turned on at $t = t_1$ while S_P is off. During this state C_2 is charged by V_{in}. C_1 and C_2 in series form the output current. Figure 3.19 shows the simplified equivalent circuits of state II. It shows the situation when V_{in}, L_S, S_{N1}, C_2 and S_{N2}

form a resonant loop. Because of the presence of the stray inductance L_S, before the switch is turned on, the current through L_S already decreases to zero. The current through S_N will increase from zero when the switch is turned on, so S_N is turned on at zero current. After L_S and C_2 resonate for half cycle, the current through S_{N1} and S_{N2} falls to zero. Therefore S_{N1} and S_{N2} turn off at zero current. So, ZCS is achieved on all the switches. The state equations of Figure 3.19 are:

$$V_{in} = L_S \frac{di_{L_S}}{dt} + v_{C_2} \tag{3.22}$$

$$i_{L_S} = C_2 \frac{dv_{C_2}}{dt} + I_o \tag{3.23}$$

And the solutions are:

$$v_{C_2}(t) = V_{in} - \frac{\pi P_o}{2V_{in}C_1\omega_r}\cos\omega_r t \tag{3.24}$$

$$i_{L_S}(t) = \frac{\pi P_o}{2V_{in}}\sin\omega_r t \tag{3.25}$$

After half cycle, the capacitor voltage is charged to:

$$v_{C_2}(t_2) = V_{in} + \frac{\pi P_o}{2V_{in}C_1\omega_r} \tag{3.26}$$

The capacitor voltage ripple is:

$$\Delta v_{C_2} = \frac{\pi P_o}{2V_{in}C_1\omega_r} \tag{3.27}$$

The soft switching conditions in both states is $f_s = f_r$, where f_s is the switching frequency and f_r is the resonant frequency.

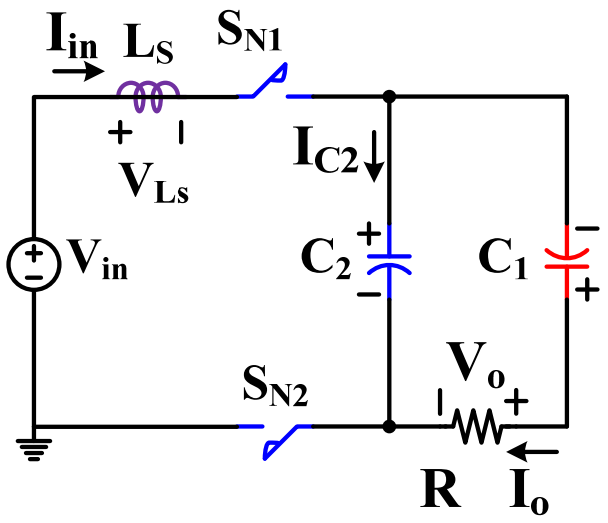


Figure 3.19 Simplified equivalent circuits of state II

3.4 Design Considerations

3.4.1 ZCS voltage multiplier

The 160 W four-level ZCS voltage multiplier design procedure is shown here as an example. The specification of the prototype converter is V_{in}=5 V, V_o=20 V, P_o=160 W, f_s=70.4 kHz.

3.4.1.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{4V_{in}\Delta v_C \omega_r} \tag{3.28}$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the output power, input voltage, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the capacitor from resonating to the negative region and lose the zero current switching. That means, the capacitors should have a positive dc

voltage offset. The output voltage ripple is two times smaller than the capacitor voltage ripple because of the 180 degrees phase shift operation of switches.

The output ripple is chosen around 6% of output voltage. So the capacitor voltage ripple is 12% of the capacitor voltage. According to the (3.28), the capacitance is chosen 47 μF in the simulation.

3.4.1.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. In case the stray inductance is not equal or large enough, small air cores can be inserted to equalize the stray inductance. The switching frequency can be adjusted according to the stray inductance present in the circuit if the circuit layout is already fixed. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 3.11.

$$L_{S2} = \frac{1}{C_1(2\pi f_S)^2} \tag{3.29}$$

Considering the output current influence, required stray inductance for L_{S1}, L_{S3}, L_{S5} and L_{S7} are a little bit smaller than the stray inductance of L_{S2}, L_{S4} and L_{S6}. So in the design, attention should be paid in order to achieve the ZCS of all the switches.

3.4.1.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used, and the stray inductance of all the parallel charging loop is equalized. The stray inductance for the series loop is also chosen properly. The switching

frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

3.4.2 ZCS voltage doubler

The 480 W ZCS voltage doubler design procedure is shown here as an example. The specification of the prototype converter is V_{in}=12 V, V_o=24 V, P_o=480 W, f_s=44.2 kHz.

3.4.2.1 Capacitance

Capacitance value should be chosen according to the voltage ripple.

$$C = \frac{\pi P_o}{2V_{in}\Delta v_C \omega_r} \tag{3.30}$$

Because of the special structure of the circuit, the voltage ripple across all the capacitors is the same. And the value of the voltage ripple is determined by the output power, input voltage, capacitance and the resonant frequency. The capacitor voltage ripple should be chosen smaller than the input voltage to prevent the voltage across the capacitor from resonating to the negative region and lose the zero current switching. That means, the capacitors should have a positive dc voltage offset. The output voltage ripple is two times smaller than the capacitor voltage ripple because of the 180 degrees phase shift operation of the switches.

The output ripple is chosen around 8% of output voltage. So the capacitor voltage ripple is 40% of the capacitor voltage. According to the (3.30), the capacitance is chosen 47 μF in the simulation.

3.4.2.2 Stray inductance

The circuit layout should be designed carefully, in order to make the stray inductance of each equivalent circuit equal. Assume all the stray inductance in the circuit is equalized. And the

required stray inductance can be satisfied by using proper input inductance. Required stray inductance for ZCS can be determined by the following equation, using the equivalent circuit shown in Figure 3.18.

$$L_S = \frac{1}{C_1(2\pi f_S)^2} \tag{3.31}$$

3.4.2.3 Switching frequency

Switching frequency should be set the same as resonant frequency in order to promise the zero current switching. Usually, the stray inductance of the circuit is already determined when the circuit layout is finished. The capacitance is also determined by the required voltage ripple. Assume the air core inductor is used for the input inductance, and the switching frequency can be determined by the input inductance value. If the input inductance is determined, he switching frequency can be twisted by monitoring the power device current when the switch is turned off. The switching frequency should be set exactly at the point when the switch current resonates to zero when the switch is turned off.

3.5 Simulation and Experiment Results

3.5.1 ZCS voltage multiplier

Figure 3.20 shows saber simulation waveforms of a 160 W four-level ZCS voltage multiplier, where Vp and Vn are the switch gate-source control voltage, Vds_Sp and Vds_Sn are the switch drain-source voltage, I_Sp and I_Sn are the switch drain-source current. I_C1,2,3 is the current through capacitor C_1, C_2 and C_3. I_C4 is the current through capacitor C_4. V_C1,2,3 is the voltage across the capacitor C_1, C_2 and C_3. Vin is the input voltage. Vo is the output voltage or the voltage across the capacitor C_4. The input voltage is 5 V. Switching frequency is about 70

kHz. Capacitance is 47 μF and stray inductance $L_{S2} = L_{S4} = L_{S6} = 108$ nH $L_{S1} = L_{S3} = L_{S5} = L_{S7} = 98$ nH. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

3.5.2 ZCS voltage doubler

Figure 3.21 and Figure 3.22 shows saber® simulation waveforms of a 480 W ZCS voltage doubler, where Sp and Sn are the switch gate-source control voltage, Vds_Sp1, Vds_Sn1, Vds_Sp2, Vds_Sn2 are the switch drain-source voltage of switch S_{P1}, S_{N1}, S_{P2} and S_{N2}. I_Sp1 and I_Sn1 are the switch drain-source current of switch S_{P1} and S_{N1}. The current through S_{P2} is the same as S_{P1}, the current through S_{N2} is the same as S_{N1}. Iin is the current through the input stray inductance L_S. I_C1 and I_C2 are the current through capacitor C_1 and C_2. V_C1 and V_C2 are the voltage across the capacitor C_1 and C_2. Vin is the input voltage. Vo is the output voltage. The input voltage is 12 V. Switching frequency is about 44 kHz. Capacitance is 52.6 μF and stray inductance $L_S = 110$ nH. The simulation results is consistent with the theoretical analysis, which verifies the above analysis.

In the 480 W ZCS voltage doubler prototype, the switching devices are two 30 V 180 A MOSFETs IPB009N03L from infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 μF MLCC capacitors C5750X7R2A475K from TDK connected in parallel. Input capacitor are twelve 16 V 470 μF conductive polymer aluminum solid electrolytic capacitors PLG1C471MDO1 from nichicon connected in parallel. Gate drive voltage is 7 V.

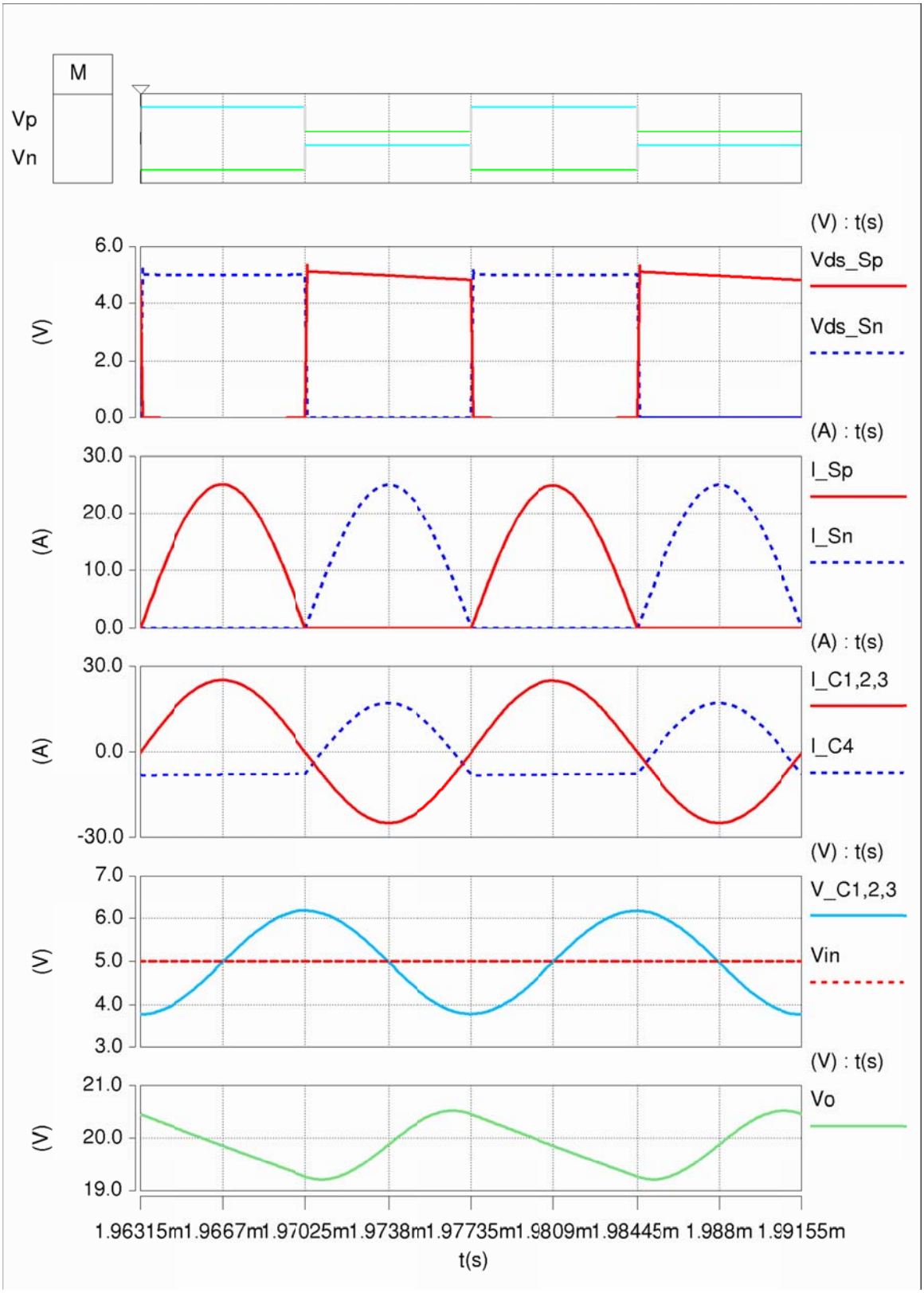


Figure 3.20 Simulation results of 160 W ZCS voltage multiplier.

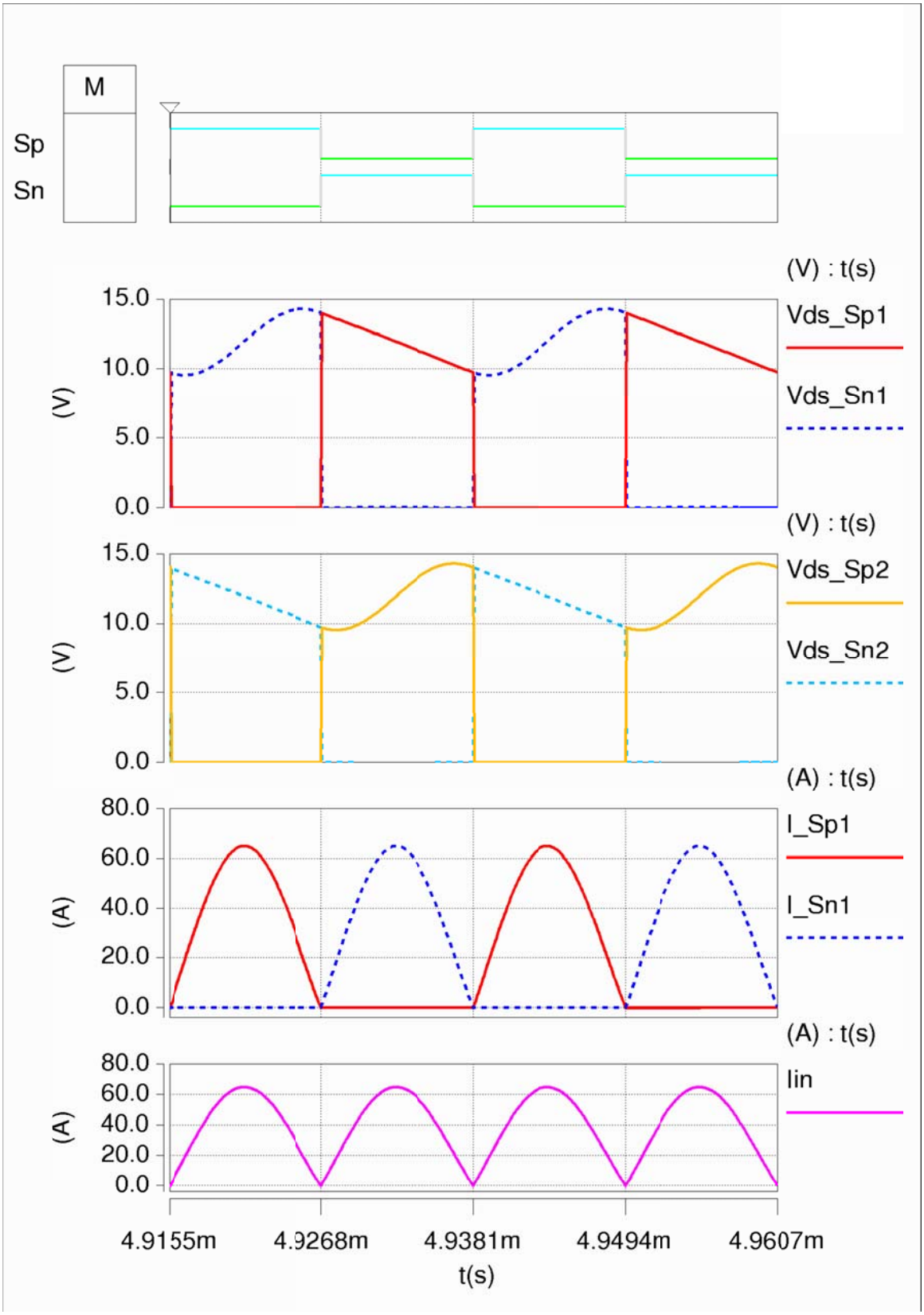


Figure 3.21 Simulation results of 480 W ZCS voltage doubler.

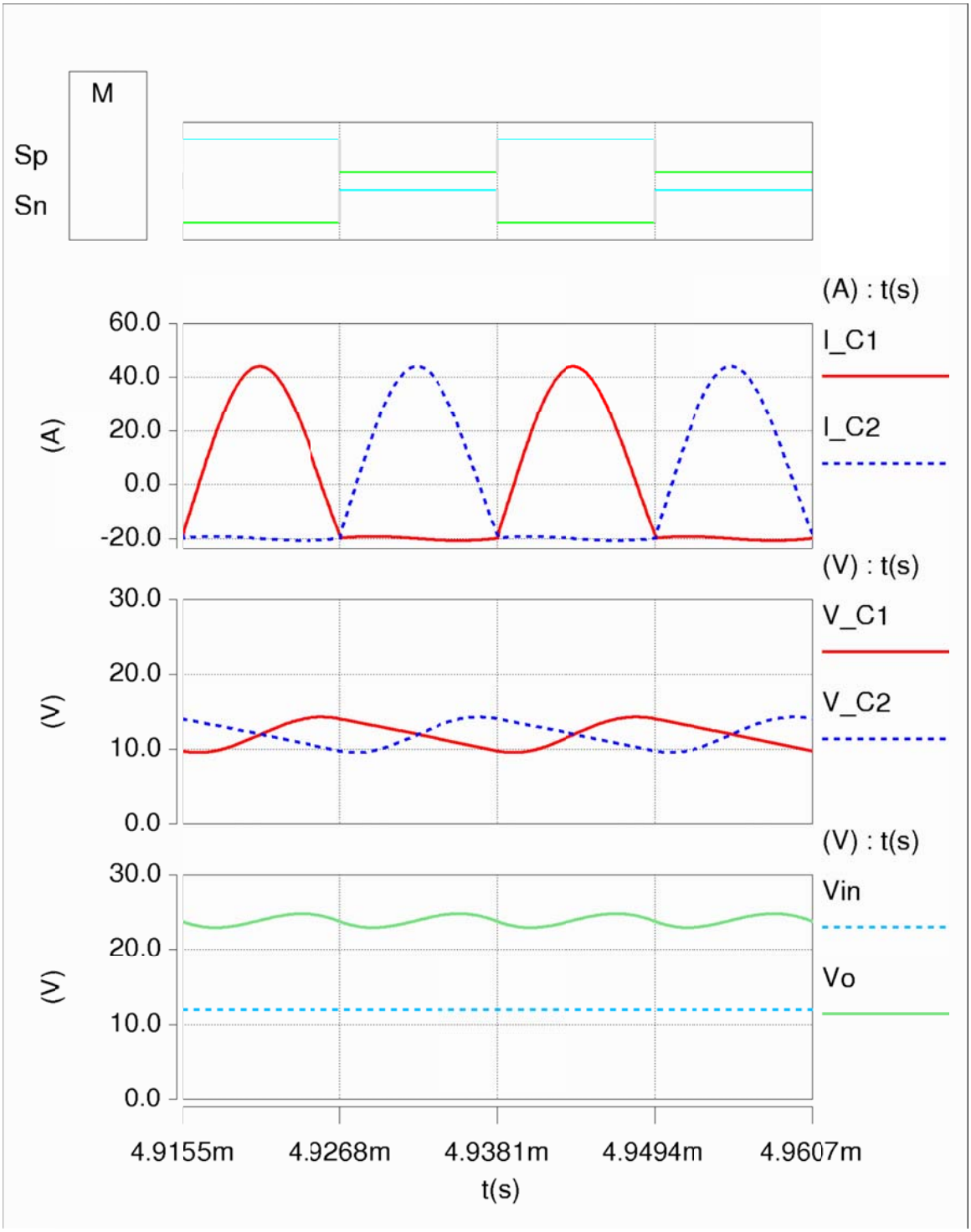


Figure 3.22 Simulation results of 480 W ZCS voltage doubler.

Figure 3.23 and Figure 3.24 show the experiment waveforms of the 480 W ZCS voltage doubler prototype with the parts mentioned above. Figure 3.23 shows the complementary gate

drive signals of S_P and S_N with duty cycle about 49% due to some dead time. V_{GS_SP} and V_{GS_SN} are the complementary gate-source control voltage.

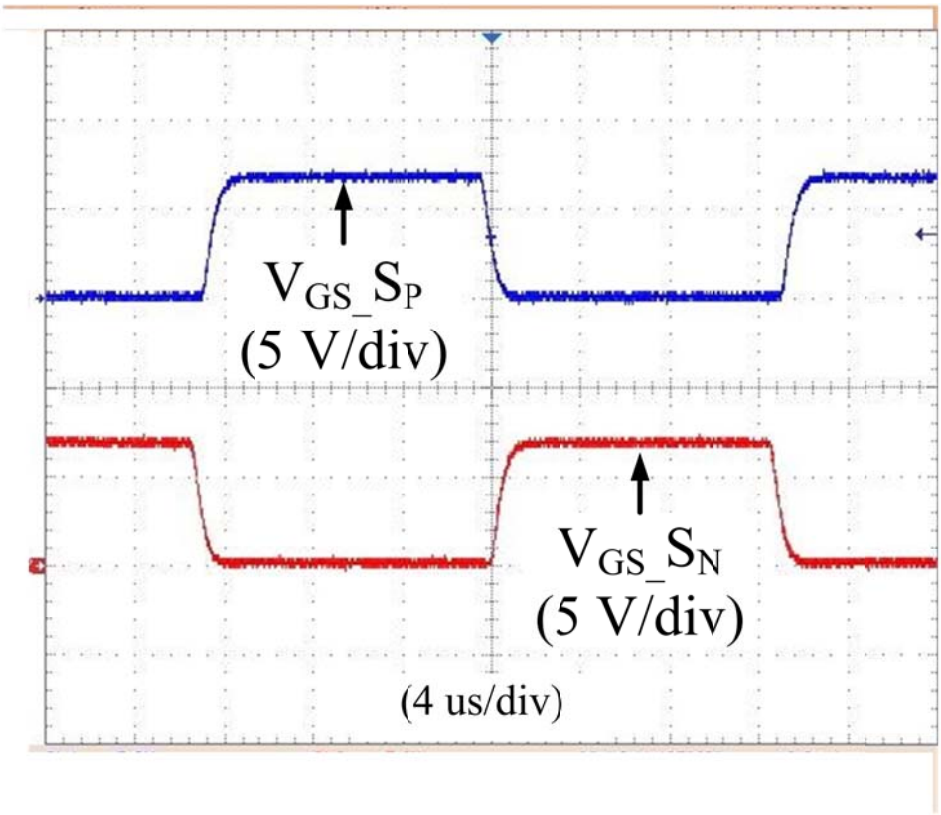


Figure 3.23 Gate drive signal of ZCS voltage doubler

Figure 3.24 shows the voltage waveforms of S_{P2} and input current waveforms. $V_{GS\_S_P}$ is the gate-source voltage of S_{P2}, $V_{DS\_S_P}$ is the drain-source voltage of S_{P2} and I_{IN} is the current through input stray inductance L_S. The resonant current waveform realizing ZCS is shown. Because the sum of the switch current is input current and the input current is critical discontinuous sinusoid waveform, the switch current is also zero when the switches are turned on and turned off. From the experiment results, we can derive that all the switches can achieve ZCS in both turn on and turn off.

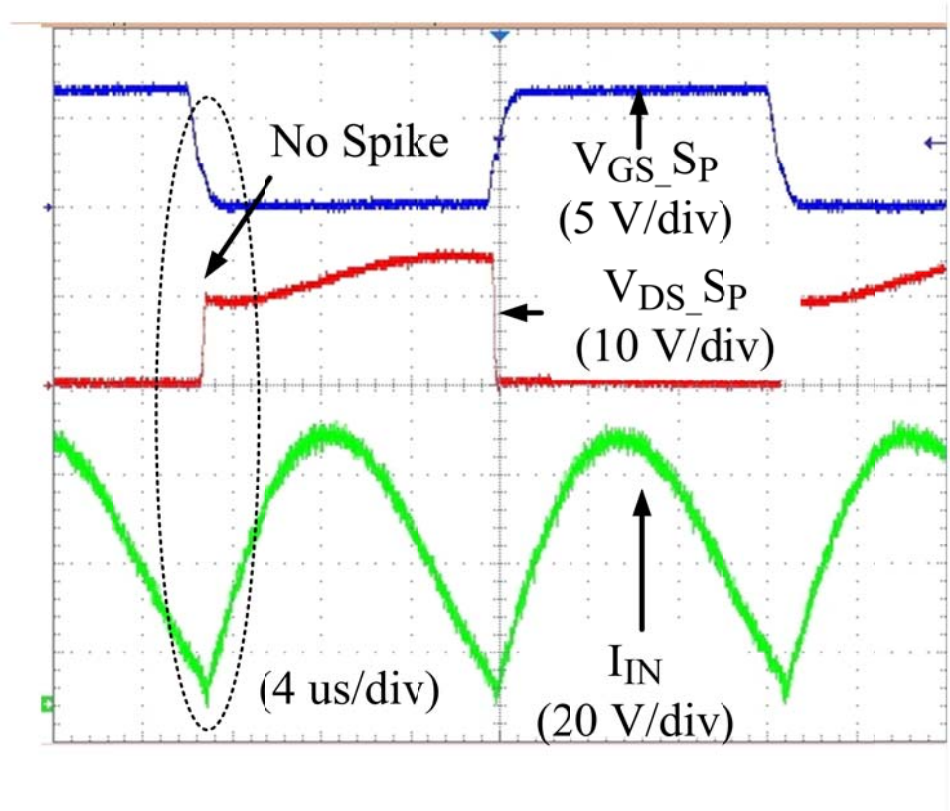


Figure 3.24 Switch voltage and input current waveform of ZCS voltage doubler

3.6 Conclusion

In this chapter, A Family of zero current switching switched-capacitor dc-dc converters has been proposed. By eliminating the bulky, lossy inductive component with a magnetic core, the converter is able to operate at very high temperatures with high efficiency. By using a soft-switching strategy, switching loss has been minimized and EMI has been restricted; the size of capacitors has been reduced, making the converter small and light. Owing to the proposed utilization of distributed stray inductance or distributed air core inserting technique, the big inductor is avoided to achieve ZCS. Hence, the proposed ZCS switched-capacitor converter family shows great potential in high temperature, high power future automotive applications.

CHAPTER 4
Multiphase Multilevel Modular DC-DC Converter for High Current High Gain TEG Application

This chapter presents a family of high efficiency zero current switching (ZCS) switched-capacitor (SC) dc-dc converters for high current high voltage gain TEG application. Compared with the traditional hard switching switched-capacitor circuits, the proposed circuit achieves ZCS for all the switches; thus minimizes the switching loss and EMI noise. The huge electrolytic capacitor bank existing in the hard switching SC circuit, which is used to reduce the voltage ripple and achieve high efficiency, is eliminated. The low capacitance ceramic capacitor is utilized instead. Different from other ZCS SC circuits that insert a magnetic core, the proposed circuit utilizes stray inductance present in the circuit to achieve ZCS, thus leading to small size, low cost and high reliability features. The proposed circuit also owns continuous input current and low output voltage ripple features. So the power loss related to the input capacitor can be minimized. By using the proposed topology, high efficiency and high power density SC dc-dc converters could be made for high current and high voltage gain TEG application. Simulation and experimental results are given to demonstrate the validity and features of the proposed topology.[4]

4.1 Background

[4] This work has been presented in part in *Energy Conversion Congress and Exposition, 2010. ECCE 2010. IEEE*, Atlanta, 2010. And published in part in *IEEE Transactions on Industry Application*

Thermoelectric (TE) module is a solid-state energy conversion device. It can convert thermal energy from a temperature gradient into electric energy as a power generator, which is usually called thermoelectric power generator (TEG). On the other hand, it can also generate a temperature gradient across the module when the electric power source is added, which can be used for cooling applications. This chapter will concentrate on the applications of TEG module. Since the 1960s, TEG module has been applied to the satellite power system in deep space [106-108], because it has long life, high reliability and small size features. But high cost and low conversion efficiency issues limited its application at that time. Recently, the high heat-to-electricity conversion efficiency TE materials [6, 7] have been developed. Due to the energy crisis, the efficient recycle of waste heat energy by TEG modules attracts more attention, especially in automotive industry [109]. By placing TEG modules around the exhaust pipe, the waste heat can be harvested and recycled to power the accessory electric loads of the vehicle, such as air conditioner, etc.

TE couple is the basic structure of a TEG module, it is composed of a *p*-type and an *n*-type semiconductor pellet connected together. One TEG module usually consists of N pairs of TE couplers connected electrically in series and thermally in parallel. Figure 4.1 shows the basic structure of one typical TEG module in a waste heat harvest system with two TE couplers connected in series. Exhaust pipe and heat sink can be applied across the TEG module to provide the temperature gradient. Electrically isolated and thermally conducted ceramic material should be inserted between these things, as shown in Figure 4.1. As a result, current can be generated through the TEG module to power the external load. The electrical model of TEG module can be treated as a voltage source with internal resistance [9, 110]. Figure 4.2 shows the typical steady-state voltage and power versus current curve of TEG module in three temperature gradient

situations. With the increase of temperature difference, the output voltage and output power of TEG module will increase.

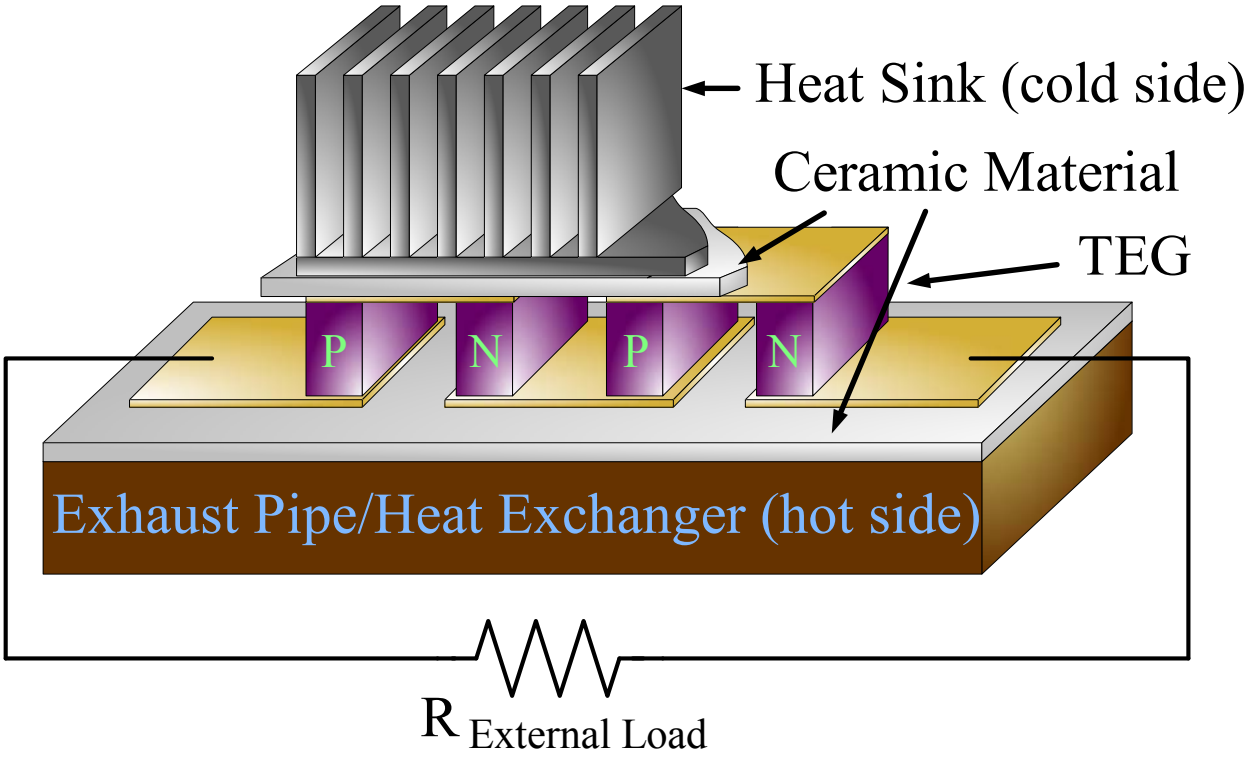


Figure 4.1. One typical TEG module in a waste heat harvest system with two TE couplers connected electrically in series and thermally in parallel.

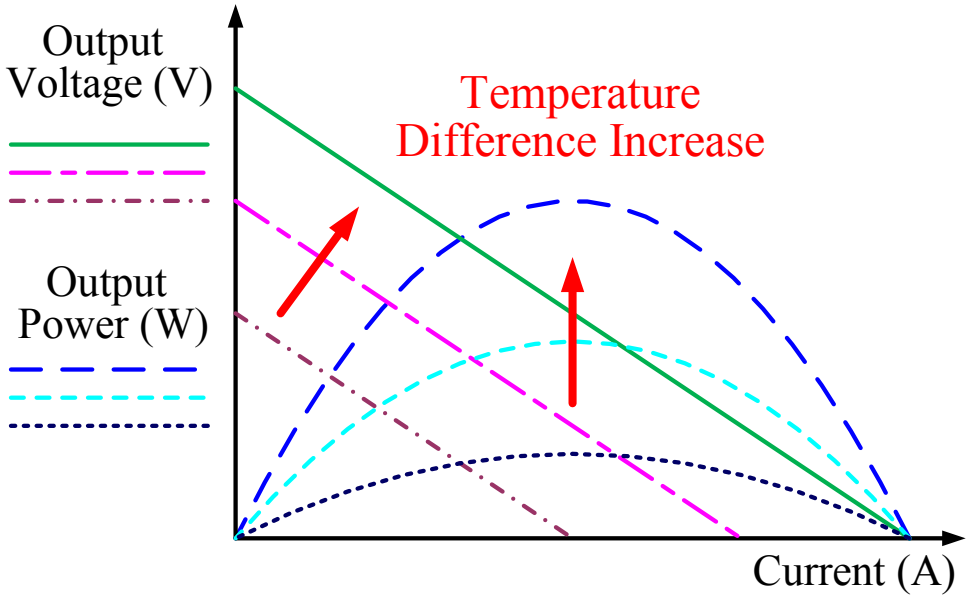


Figure 4.2. TEG module steady state V/I and P/I characteristics in three different temperature gradient

To output the same amount of power, TEG modules could have different output voltage and current combinations. It could output either high voltage with low current or high current with low voltage. Due to the low output voltage of each TE couple, a TEG module with high output voltage and low current means many small semiconductor pellets have to be connected in series. And this will increase the internal impedance of the TEG module and the difficulty of manufacture, which will undoubtedly reduce the reliability of the whole module. At the same time, a TE couple with bigger semiconductor pellet is able to output higher current and is easier to manufacture. Therefore, using bigger semiconductor pellet and less TE couples connected in series to produce TEG module is preferred in industry. This fabrication technique will reduce the internal impedance of the TEG module; increase the conversion efficiency and the reliability. In this case, the produced TEG modules will have high output current and low output voltage features [6, 7].

4.2 Introduction

Recently, TEG module as a renewable energy source for automotive industry is becoming more and more popular. It has low noise, small size and high reliability features. As aforementioned, low output voltage with high output current TEG module is preferred in terms of performance and fabrication. Therefore, to power the automotive load, a low input voltage, high input current with high voltage gain dc-dc converter interface is required. With the development of SiC switching devices and ceramic capacitors, high temperature components will be available (above 250 ℃) except magnetic cores [83]. Magnetic-less high voltage gain SC dc-dc converters are becoming more attractive for the automotive application than the traditional counterparts in terms of size and high temperature operation. Traditional SC dc-dc converters

have been investigated since the 1970s, mainly in low power conversion area [73, 75, 76, 101, 104, 111-113].

However, for traditional SC dc-dc converters, high voltage spike and EMI problems are common. Moreover, when switching frequency is increased, the switching loss becomes more and more serious. In order to solve the voltage spike problem as well as to reduce the EMI and switching loss of SC dc-dc converter, many ZCS type SC dc-dc converters have been proposed, which use an inserted inductor resonating with capacitor [84-88, 103]. The ZCS of the main switching devices can be achieved by the aforementioned method. Nevertheless, inserting a relatively big magnetic core to the SC circuit loses the original intention of developing the magnetic-less, small size high temperature operation converter, which will also limit its application areas [92, 93].

In the high power utility application and medium voltage drive areas, the multilevel inverter have been investigated thoroughly in the last thirty years [114-128]. The basic module of the multilevel inverter can also be considered as a SC circuit. By configuring the multilevel inverter properly, a multilevel dc-dc converter for high power high current automotive application can be achieved [81-83, 94-97, 102]. To reduce the switch current stress and to increase the converter voltage gain, a multilevel modular SC dc-dc converter has been proposed recently [78-80, 98-100, 129-132]. However, for the above multilevel dc-dc converters, huge capacitor banks with high capacitance have to be employed to achieve high efficiency [82, 95, 96, 102]. A ZCS multilevel modular switched-capacitor dc-dc converter (ZCS-MMSCC) has been proposed by utilizing the distributed stray inductance in the circuit to achieve ZCS and reduce the capacitor size [133-135]. But this converter has discontinuous input current with huge current ripple. The power loss related to the input capacitor bank is becoming a major part when the input current is

increased. Besides, this converter cannot be simply put in parallel and operate at an interleaved manner to reduce the input current ripple.

This chapter presents a multiphase NX (with conversion ratio equals to N) ZCS-MMSCC with continuous input current and reduced output voltage ripple. By operating each phase with correct phase shift angle, the input current becomes continuous, which means the input current ripple can be reduced significantly. Therefore, the power loss of the input capacitor can be minimized. The huge input capacitor bank of traditional ZCS-MMSCC, which is used to meet high capacitor ripple current and thermal requirement, could be eliminated. Output capacitor current ripple and voltage ripple are also reduced due to the interleaving operation. By using the proposed circuit, smaller size, higher efficiency with higher input current and higher power dc-dc converter could be built. A 630 W prototype of the proposed circuit has been built to confirm the operation. Simulation and experimental results are given to demonstrate the validity and features of the proposed circuit. Efficiency curve comparison of traditional ZCS-MMSCC and proposed converter is also provided. By using the similar idea, of multiphase ZCS-MMSCC, multiphase ZCS voltage multiplier is also proposed in this chapter. The detailed operation of multiphase ZCS voltage multiplier will not be discussed, since its operation is very similar to multiphase ZCS-MMSCC.

4.3 Proposed Circuit and Operation Principles

4.3.1 Multiphase ZCS-MMSCC with continuous input current

Figure 4.3 shows the circuit diagram of the proposed m-phase NX ZCS-MMSCC. This circuit can be considered as the combination of m phases (m>2) interleaved traditional ZCS-MMSCCs with one extra switch in each phase and one extra output capacitor. The control signal of each phase should be $2\pi/m$ degrees phase shifted from each other. For the current ripple

cancellation purposes, the phase number m should be larger than two. Compared to the traditional ZCS-MMSCC, the input current rating of the proposed circuit can be increased by m times with reduced input current ripple. Therefore, the current stress of the input capacitor C_{in} can be reduced, the huge input capacitor bank existed in traditional ZCS-MMSCC to sustain the huge input current ripple can be avoided. The input current ripple and input capacitor size reduction with different interleaving phases will be discussed in detail in next section. By using one extra switch in each phase with interleaving operation, the output capacitor current ripple can also be reduced. So the output capacitor design can be decoupled with the capacitors in the resonant network. The low capacitance and low ESR multilayer ceramic (MLCC) capacitor could also be used for the output capacitor to achieve low output voltage ripple. Similar to the traditional ZCS-MMSCC, all the switches of the proposed circuit can also achieve ZCS utilizing the stray inductance present in the circuit. The required stray inductance for resonant for the first and last stage is the same, while all the other stages are the same. When the conversion ratio equals to N, the total device number is m(3N-1).

Figure 4.4 shows the four-phase 4X ZCS-MMSCC as an example for detail analysis.

4.3.2 Multiphase ZCS voltage multiplier with continuous input current

Figure 4.5 shows a four-level ZCS voltage multiplier with continuous input current main circuit as an example. Similar to the ZCS-MMSCC with continuous input current this circuit also works as a four times step-up converter. Four phase ZCS voltage multipliers are connected in parallel with the same input voltage source. Each phase is controlled with 90 degrees phase shift. Only four different control signals are needed because of the special structure of the ZCS voltage multiplier. One extra switch is added in each phase of the ZCS voltage multiplier, which are S_{P7},

S_{N11}, S_{B7}, and S_{R11}. The added switches are also controlled with 90 degrees phase shift and ZCS can be also achieved.

One output capacitor with higher capacitance is added to reduce the output voltage ripple. The output capacitor with higher capacitance can be treated as a voltage source considering the resonant of stray inductance of the added switch and original output capacitor of ZCS voltage multiplier to achieve the ZCS of the added switches. The required stray inductance of the extra switch to achieve the ZCS is the same with all the other equivalent stray inductance, for example, $L_{S8} = L_{S1} = L_{S2}$.

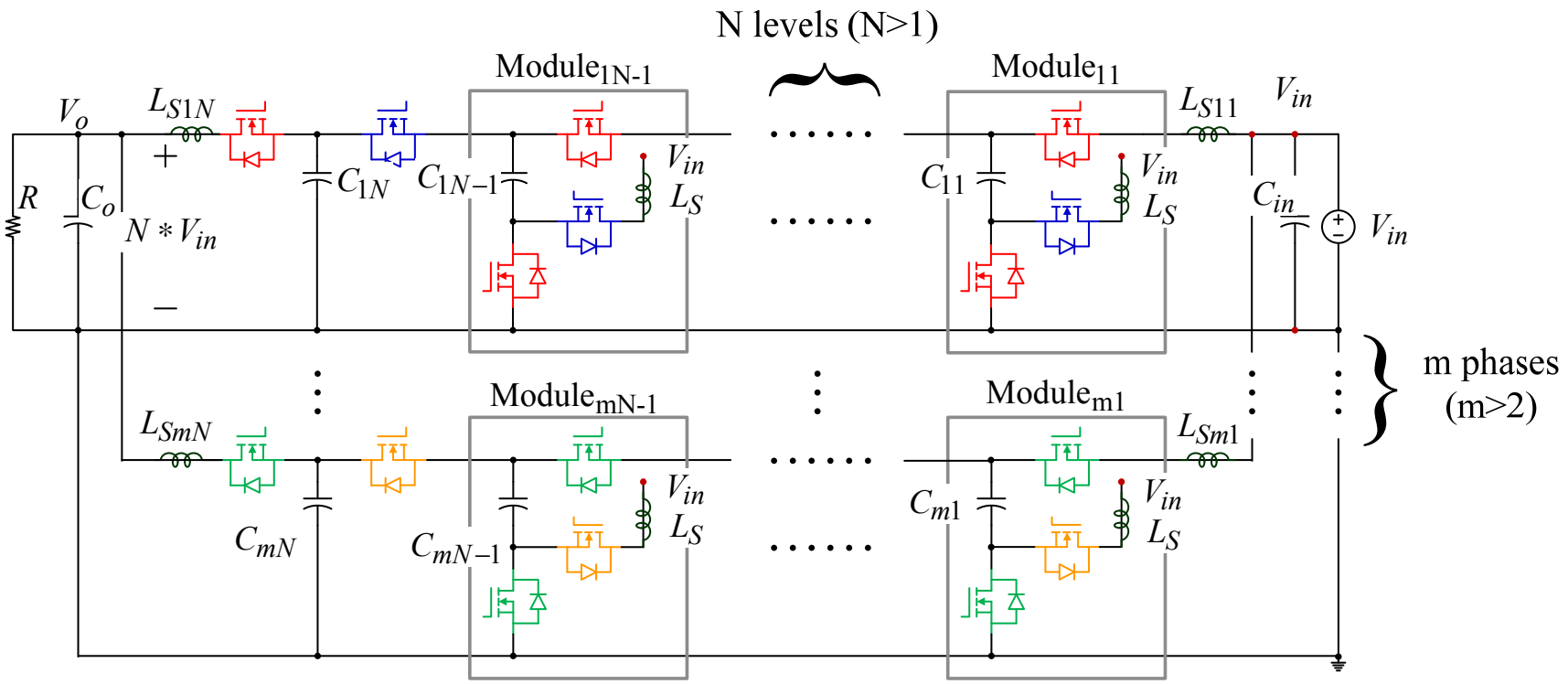


Figure 4.3. Proposed multiphase NX ZCS multilevel modular SC dc-dc converter main structure.

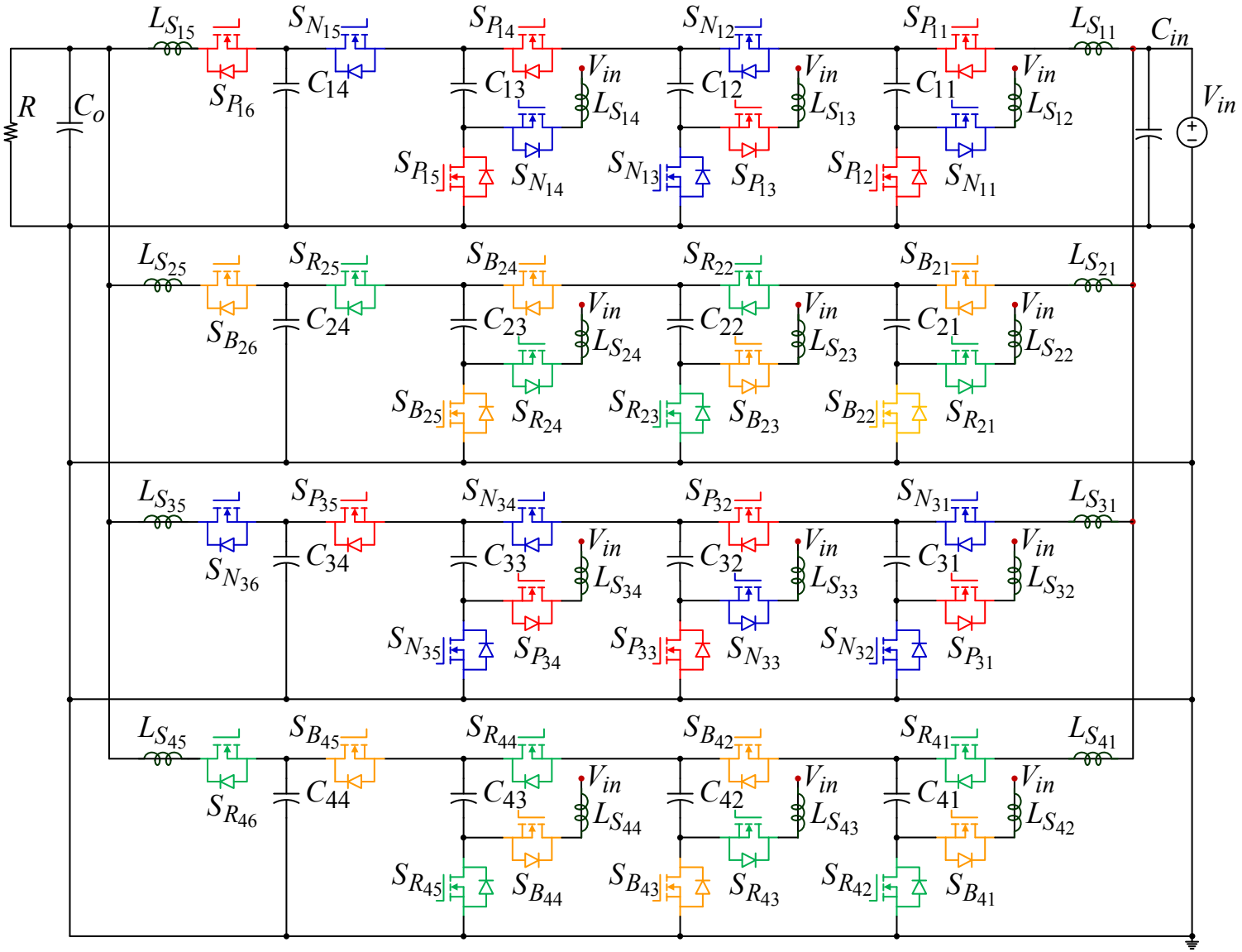


Figure 4.4 Four-phase 4X ZCS multilevel modular SC dc-dc converter main structure.

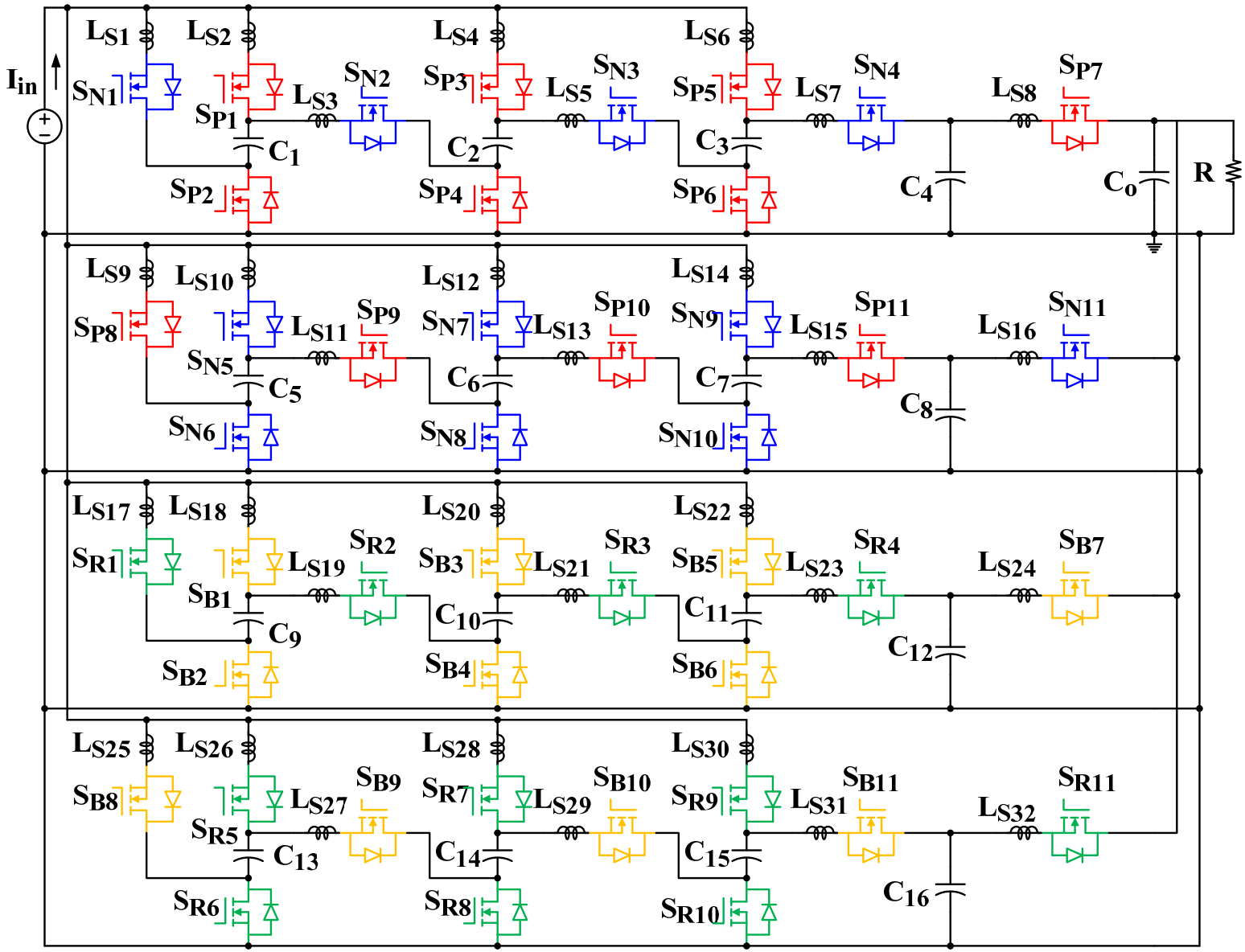


Figure 4.5 Proposed ZCS voltage multiplier with continuous input current main circuit

4.4 Operation Principles

Multi-phase ZCS-MMSCC is used as an example for the operation principles analysis, Figure 4.6 shows the ideal steady state waveforms of the proposed circuit (Figure 4.4).

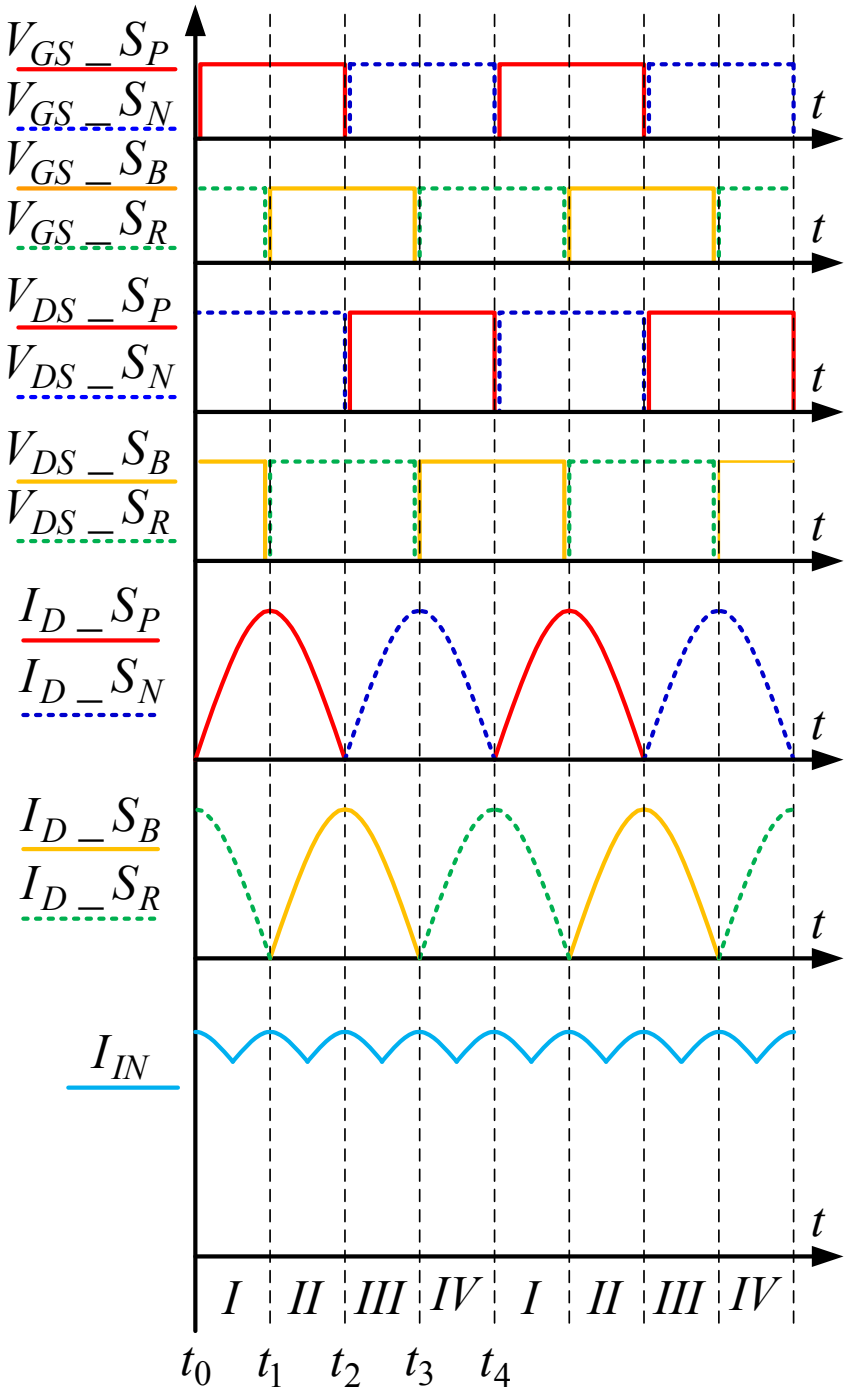


Figure 4.6. Ideal waveforms of proposed four-phase 4X ZCS-MMSCC

The gate signal of switch S_P and S_N is complementary with 50% duty cycle, while the gate signal of switch S_B and S_R is also complementary with 50% duty cycle. The four different gate signals can be generate by one signal with 90 degrees phase shift from each other. $V_{GS\_S_P}$, $V_{GS\_S_N}$, $V_{GS\_S_B}$, and $V_{GS\_S_R}$, as shown in Figure 4.6 are the gate drive signals of the corresponding devices. $V_{DS\_S_P}$, $V_{DS\_S_N}$, $V_{DS\_S_B}$, and $V_{DS\_S_R}$ are the ideal drain to source voltage waveforms of corresponding devices. Assume input and output capacitors to be ideal voltage sources. Assume that the capacitor ESR and the switch turn-on resistance in each loop are small enough to be neglected. When the switches are turned on, the current through the stray inductance present in the circuit, capacitors and the switches will begin to resonate from zero. By adjusting switching frequency to the resonant frequency of the stray inductance L_S and the capacitor, the current through all the switches in the circuit will decrease to zero when the switches are turned off. And the current through the switches forms half period of the sinusoidal waveform. $I_{D\_S_P}$, $I_{D\_S_N}$, $I_{D\_S_B}$ and $I_{D\_S_R}$, as shown in Figure 4.6 are the ideal waveforms of switch drain current. So, the current through the switches in both turn on and turn off transition will be zero. Because the circuit has four phases, in each switching state, there are always two different switches conducting with current waveforms 90 degrees shift from each other. And the input current can be considered as the sum of the current of all the equivalent sub-circuits. Therefore, the input current becomes continuous due to the four-phase interleaving operation, and the input current ripple is reduced by five times. Figure 4.7 and Figure 4.8 show the equivalent sub-circuit of one phase of the proposed circuit, as shown in Figure 4.4. The state equations are similar to ZCS-MMSCC [134, 135], except the stray inductance L_{S15} should be the same with L_{S11}, because only one capacitor is in the resonant loop.

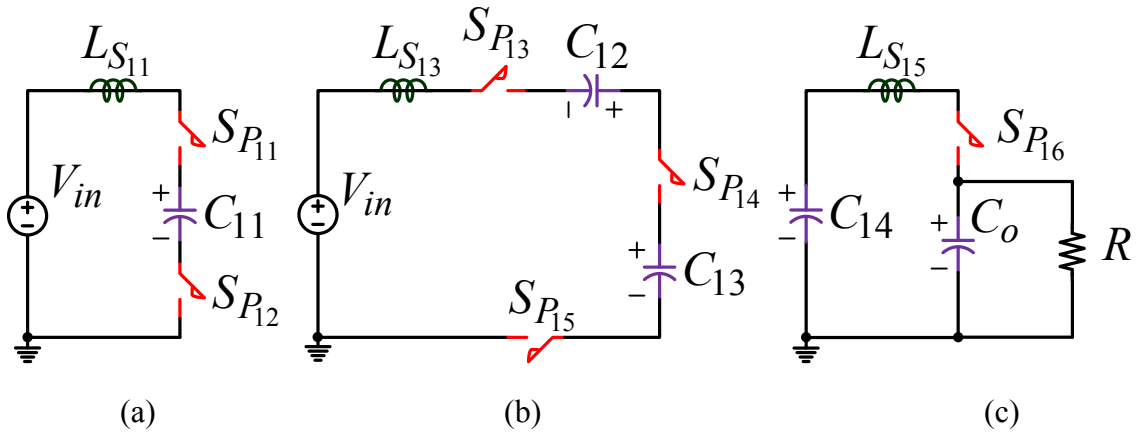


Figure 4.7. Simplified equivalent circuits of state I and II of the first phase with switch S_P turned on.

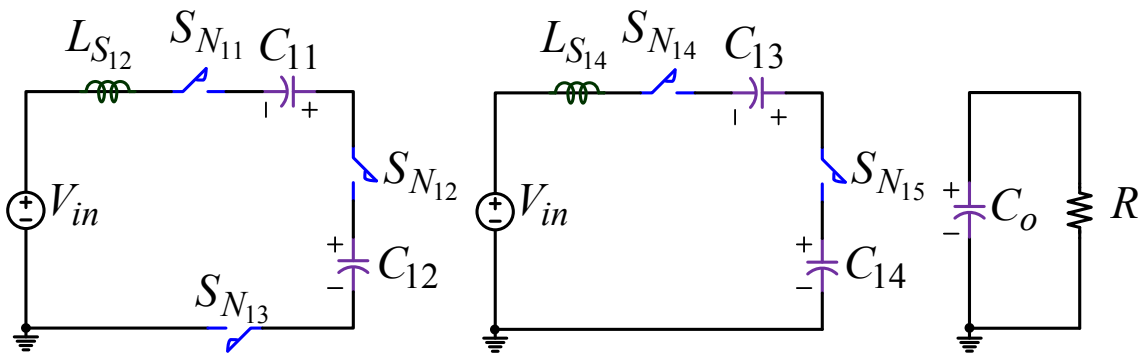


Figure 4.8. Simplified equivalent circuits of state III and IV of the first phase with switch S_N turned on.

4.5 Current Ripple Comparison and Power Loss Analysis

In this section, the input current ripple of traditional ZCS-MMSCC and the proposed multiphase NX ZCS-MMSCC will be calculated and compared. The input capacitor size reduction due to the capacitor RMS current reduction will also be compared and summarized. Finally, the converter efficiency improvement of the proposed circuit will be estimated and compared with the traditional ZCS-MMSCC.

In the following analysis, assume the converter power rating to be 500 W; the input voltage to be 5 V, the input average current to be 100 A and all the components are ideal.

4.5.1 Multiphase ZCS-MMSCC

Assume both converters are 500 W with 5 V input voltage, and all the components are ideal

4.5.1.1 Traditional ZCS-MMSCC input current ripple and the input capacitor power loss calculation.

For the traditional ZCS-MMSCC, the input current can be considered as rectified sinusoid waveform with only positive side [134, 135]. So, the input current can be expressed with the function $I_{in1} = A_1 \sin\theta$, $\theta \in [0,\ \pi]$. Because the average input current is $I_{in1\_ave} = 100\ A$, the input current amplitude can be calculated using integration $\frac{1}{\pi}\int_0^{\pi} A_1 \sin\theta d\theta = 100\ A$. The input current amplitude can be calculated as $A_1 = 50\pi \approx 157\ A$ Because the shape of the input current was sinusoid in half cycle, the input current ripple $I_{in1\_ripple} = A_1 \approx 157\ A$. The current follow into the input capacitor should be the input current minus the dc component, which can be calculated as, $I_{in1\_RMS} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(I_{in1} - I_{in1\_ave}\right)^2 d\theta} = \sqrt{\frac{1}{\pi}\int_0^{\pi}\left(50\pi\sin\theta - 100\right)^2 d\theta} = 48.3\ A$.

So, the power loss of the input capacitor can be calculated, $Loss_1 = I_{in1\_RMS}{}^2 ESR$. ESR is the input capacitor equivalent series resistance.

4.5.1.2 Proposed four-phase NX ZCS-MMSCC input current ripple and the input capacitor power loss calculation.

For the proposed four-phase NX ZCS-MMSCC, the input current is continuous due to the interleaving technique. The input current in a quarter period can be considered as a part of the sinusoid waveform with only top part in the quarter period. So, the input current in a quarter

period can be expressed with the function, $I_{in2} = B_1 \sin\theta,\ \theta \in \left[\frac{\pi}{4},\ \frac{3\pi}{4}\right]$. Because the average current is also $I_{in2\_ave} = 100\,A$, the input current amplitude can be calculated using the integration $\frac{2}{\pi}\int_{\pi/4}^{3\pi/4} B_1 \sin\theta d\theta = 100\,A$, the input current amplitude can be calculated as $B_1 = \frac{50\pi}{\sqrt{2}} \approx 111\,A$. The input current ripple can be calculated as, $I_{in2\_ripple} = B_1\left(\sin\frac{\pi}{2} - \sin\frac{\pi}{4}\right) = \frac{50\pi}{\sqrt{2}}\left(1 - \frac{\sqrt{2}}{2}\right) \approx 32.5\,A$. Similarly, the RMS value of the input capacitor current can be calculated as, $I_{in2\_RMS} = \sqrt{\frac{2}{\pi}\int_{\pi/4}^{3\pi/4}\left(I_{in2} - I_{in2\_ave}\right)^2 d\theta}$. By plug in the number to this equation, the input capacitor current RMS value is $I_{in2\_RMS} = \sqrt{\frac{2}{\pi}\int_{\pi/4}^{3\pi/4}\left(\frac{50\pi}{\sqrt{2}}\sin\theta - 100\right)^2 d\theta} = 9.7\,A$, which is about 20% of I_{in1_RMS}. So, the loss of the input capacitor is $Loss_2 = I_{in2\_rms}{}^2 ESR$. So the power loss related to the input capacitor is reduced to $P_{reduce\_ratio} = Loss_2 / Loss_1 = I_{in2\_rms}{}^2 / I_{in1\_rms}{}^2 = 4\%$.

Hence, by using the proposed four-phase NX ZCS-MMSCC, the input current ripple can be reduced significantly; the RMS value of input capacitor current is reduced to 20%; and input capacitor ESR loss is reduced to 4%, which means much smaller capacitor bank could be adopted. The power loss related to the input capacitor bank is a big part of converter total power loss. By using multiphase interleaving technique, the input capacitor power loss is minimized, so the converter efficiency can be improved significantly. On the other hand, if a small input capacitor bank is employed, the converter power density is increased. The input capacitor design could be a trade-off of efficiency and power density.

4.5.1.3 Input current ripple and input capacitor power loss comparison with different phases.

By using the similar method aforementioned, the input current ripple, input capacitor power loss of single-phase, three-phase, five-phase and six-phase NX ZCS-MMSCC can also be calculated accordingly. Figure 4.9 shows the idealized input current waveforms of proposed multiphase converter with different phases interleaved together. The proposed single phase NX ZCS-MMSCC has the same input current ripple with traditional ZCS-MMSCC, so single-phase NX ZCS-MMSCC is used for input current ripple and input capacitor power loss comparison. Different from the traditional ZCS-MMSCC, the single-phase NX ZCS-MMSCC can achieve bidirectional operation while keeping the ZCS feature, because the output capacitor can be decoupled with the resonant switch-capacitor network. By moving the power source in parallel with the output capacitor, a single-phase NX ZCS-MMSCC step-down circuit can be achieved. However, the traditional ZCS-MMSCC output capacitor joins the resonant, so the power source cannot be added directly in parallel with the output capacitor, while still keeps the ZCS feature of all the switches. By using three phases, four phases, five phases, six phases, seven phases or eight phases, the input current ripple can be reduced to around 8.9%, 20%, 3.2%, 8.9% 1.6% and 5% respectively compared with single phase. The reason why the odd number phases interleaved together have smaller current ripple is because the input current ripple frequency is 2mω, due to the circuit structure. On the other hand, if the circuit has even number phases, the input current ripple frequency is only mω. This is why the 3-phase NX ZCS-MMSCC has 6ω input current ripple, but the 4-phase NX ZCS-MMSCC has only 4ω current ripple. The proper number of phases operating interleaved should be determined by the particular application and input current rating. Obviously odd number phases interleaved NX ZCS-MMSCC has more advantages on

input current ripple and input capacitor power loss reduction. But even number phases interleaved NX ZCS-MMSCC can have less control signals. For a 3-phase NX ZCS-MMSCC, six different control signals are required; for the 4-phase situation, only four different signals are needed, as shown in Figure 4.6. Figure 4.10 shows the input current ripple, input capacitor power loss and input capacitor size comparison with different number of phases parallel together. The single phase situation is set as the base of comparison. The input capacitor power loss comparison, as shown in Figure 4.10 is derived by assuming all the circuits with different phases use the same input capacitor. The input capacitor size comparison, as shown in Figure 4.10 is derived by assuming all the input capacitors of each circuit with different phases have the same current ripple.

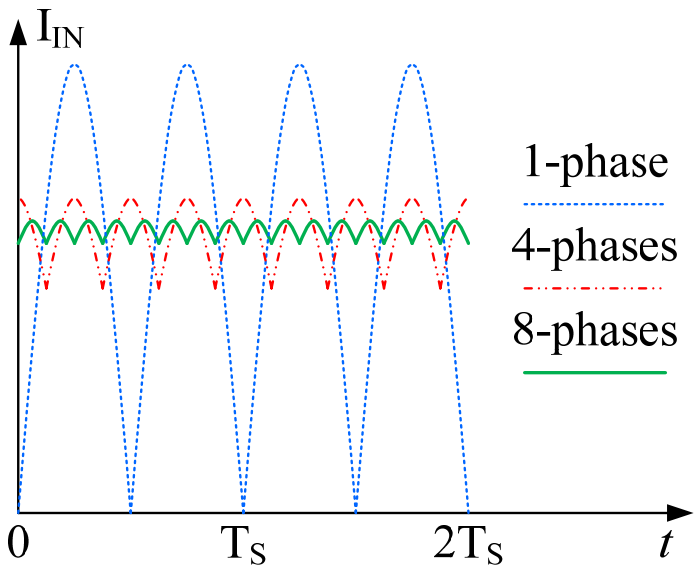


Figure 4.9. Input current ripple comparison with different phases interleaved.

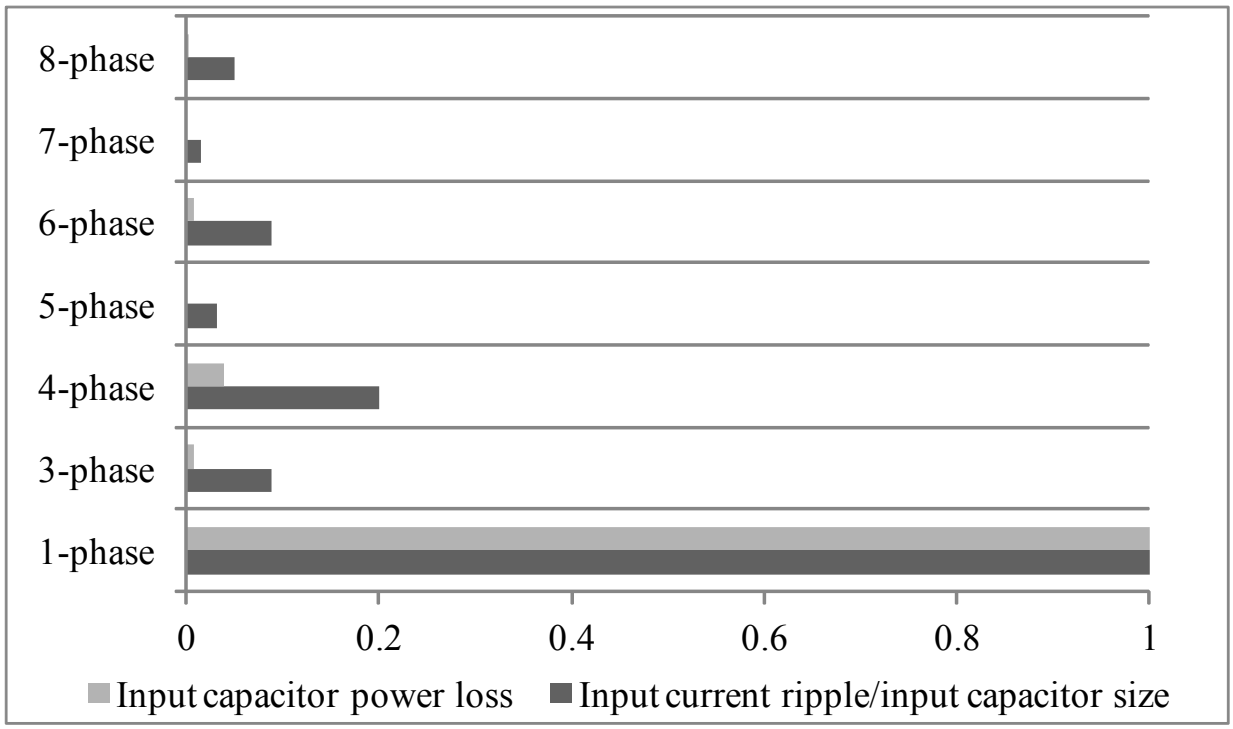


Figure 4.10. Capacitor current ripple, loss and size comparison with different phases interleaved.

4.5.1.4 Converter power loss analysis and efficiency comparison.

Figure 4.11 shows the photo of a 630 W single-phase 12X ZCS-MMSCC prototype of the proposed circuit. The input voltage of the prototype is 5 V. The output voltage is about 60 V. The switching frequency is chosen to be around 70 kHz. The 50% duty cycle complimentary gate signal is generated by using DSP TMS320LF2407A from TI for the debugging convenience purposes. Any analog PWM chips with two channel 50% duty cycle complementary output capability are able to provide the control signal for the circuit. The input capacitor is sixty-five capacitors in parallel, which is PLG1C471MDO1 from nichicon. The rated RMS current ripple of this capacitor is 5.4 A, and the ESR of this capacitor is 11 mΩ in 100 kHz . Two MOSFETs from Infineon (IPB009N03L) are used in parallel as switching devices. The rated voltage of the MOSFET is 30 V, the turn-on resistance is 0.95 mΩ. Ten 4.7 μF MLCC capacitors from TDK (C5750X7R2A475K) are used in parallel as the resonant capacitor. The ESR of this capacitor is

about 4 mΩ at 70 kHz. The stray inductance in the circuit is about 108 nH of the first stage and the last stage, and 216 nH of the other stages. The dimension of the prototype is 22 in*3.5 in* 0.5 in. The gate drive board is separated for circuit debug convenience. The power density of the prototype is about 20 W/in^3. For the debug convenience, the power density of the prototype is designed quite low. The power density of the proposed circuit can be designed much higher up to (300 W/in^3 ~ 2 kW/in^3) [133, 136].

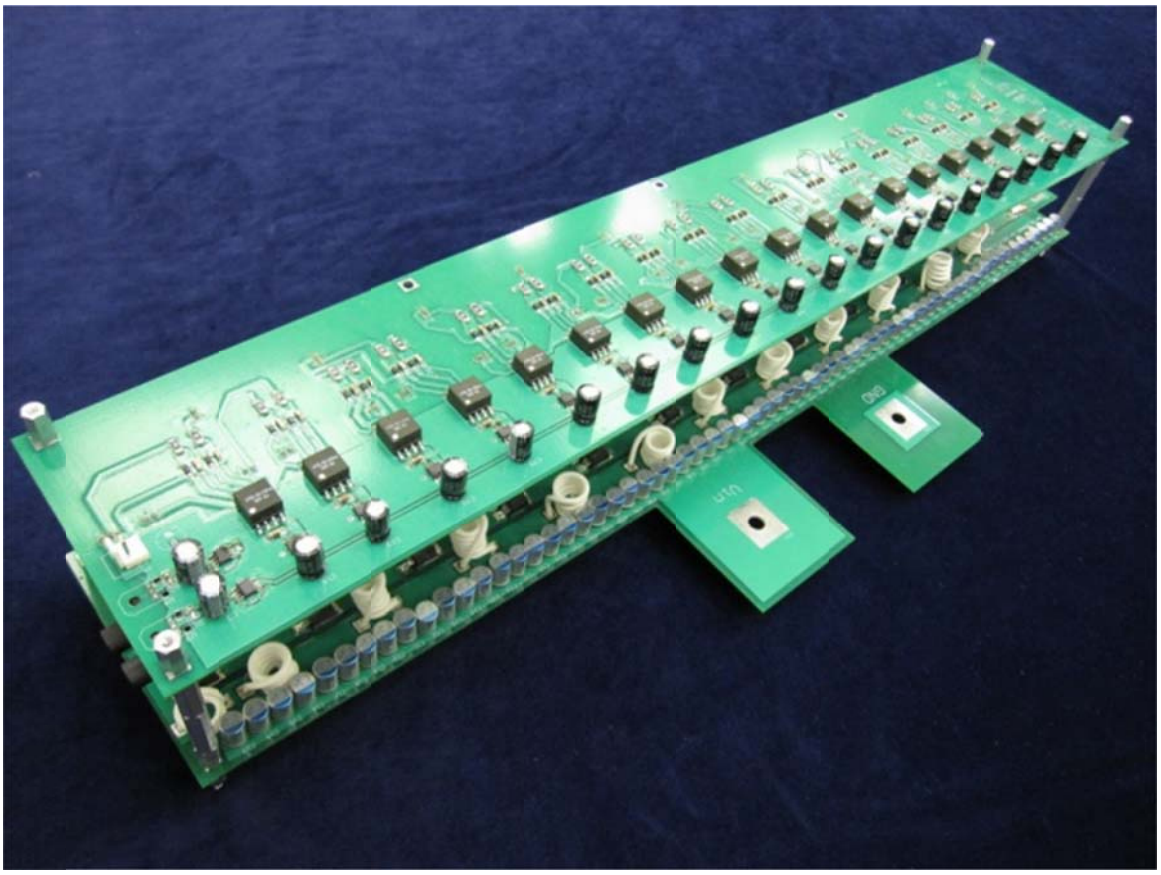


Figure 4.11. The photo of the prototype of proposed circuit

Figure 4.12 shows the 630 W single-phase 12X ZCS-MMSCC prototype power loss estimation by using the power loss equation (4.1). The power loss caused by input capacitor and other parts are separated and marked. The horizontal axis is the output power. The vertical axis is the increase of power loss. It can be shown that, the input capacitor power loss becomes more

and more dominant with the increase of input current rating. The detailed power loss equation derivation and verification have been proposed in [134] of the same author. Where P_{loss} is the total power loss, N_T is the voltage conversion ratio, P_{in} is the input power, R_{on} is the MOSFET turn-on resistance, V_{in} is the input voltage, V_{GS} is the gate drive voltage, Q_g is the total MOSFET gate charge, f_s is the switching frequency, R_{ESR} is the resonant capacitor ESR, R_{ESR_in} is the input capacitor ESR. Figure 4.13 shows the efficiency curve comparison of the 650 W four-phase 12X ZCS-MMSCC converter and traditional ZCS-MMSCC with the same power rating.

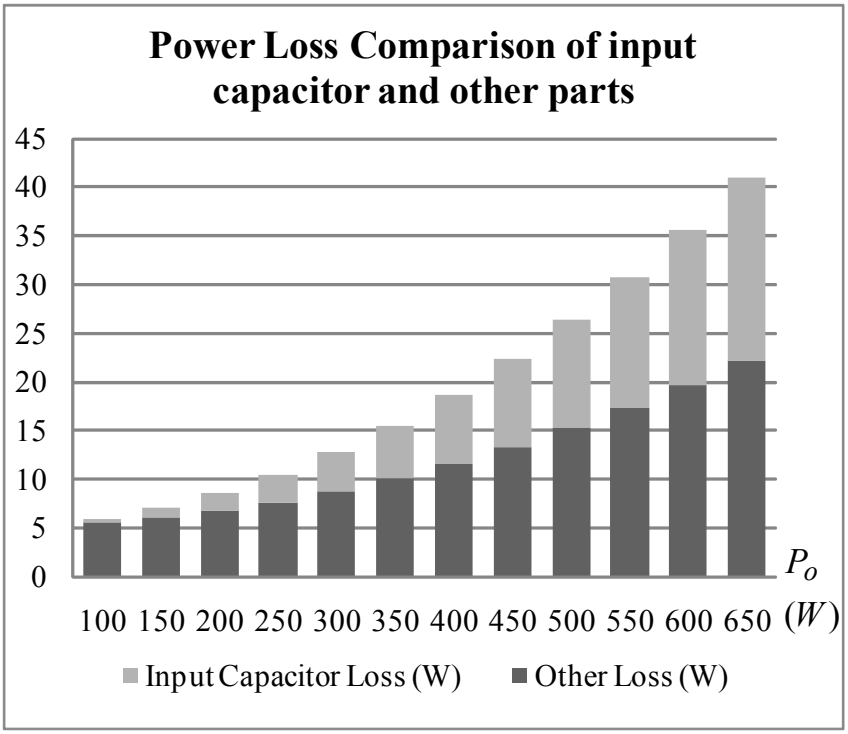


Figure 4.12. Traditional ZCS-MMSCC power loss comparison of input capacitor and other parts.

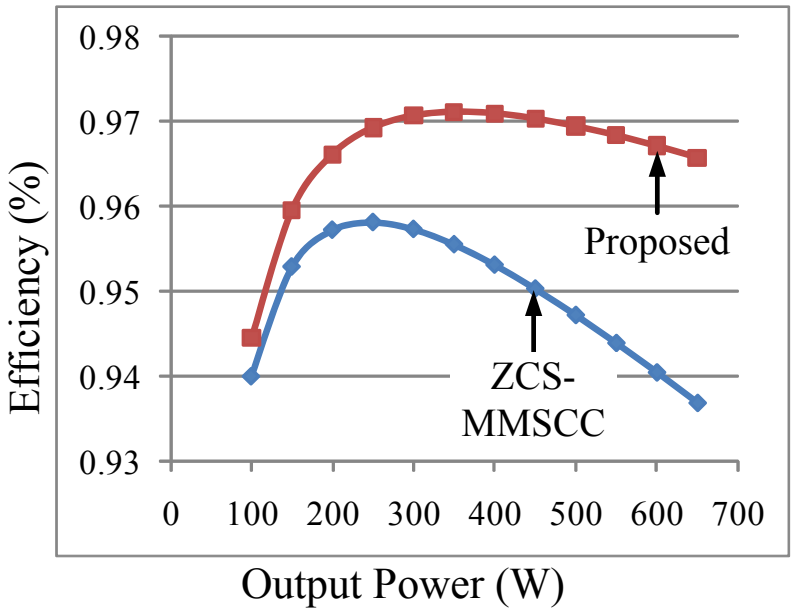


Figure 4.13. Proposed four-phase ZCS-MMSCC and traditional ZCS-MMSCC Efficiency curve comparison.

$$P_{loss} = (3N_T - 1)(\frac{\pi^2 P_{in}{}^2 R_{on}}{4N_T{}^2 V_{in}{}^2} + V_{GS} Q_g f_s) + \frac{\pi^2 P_{in}{}^2 R_{ESR}}{2N_T V_{in}{}^2} + \frac{\pi^2 P_{in}{}^2 R_{ESR\_in}}{8V_{in}{}^2} \qquad (4.1)$$

4.5.2 ZCS voltage multiplier type

4.5.2.1 Single-phase ZCS voltage multiplier input current ripple calculation

Assume $I_{in} = 3A_2 \sin\theta + A_2 \sin\theta$, $(\theta \in [0,\pi], \alpha \in [\pi, 2\pi])$, Because $I_{in\_ave} = 100\ A$ So, $\frac{1}{\pi}\int_0^{\pi} 3A_2 \sin\theta d\theta + \frac{1}{\pi}\int_{\pi}^{2\pi} A_2 \sin\theta d\theta = 100$. $A_2 = 25\pi \approx 78.5$, the input current ripple is $I_{in\_3} = 3A_2 = 235.5\ A$. The RMS value of the input current ripple is $I_{in\_3\_RMS} = \sqrt{\left(\frac{1}{\pi}\int_0^{\pi}(75\pi\sin\theta - 100)^2\, d\theta + \frac{1}{\pi}\int_{\pi}^{2\pi}(-25\pi\sin\theta - 100)^2\, d\theta\right)/2} = 73.6\ A$.

So, the loss of the input capacitor is $Loss_3 = I_{in\_3\_RMS}{}^2 \cdot ESR$.

4.5.2.2 Four-phase ZCS voltage multiplier input current ripple calculation

Assume $I_{in} = B_2 \sin\theta,\ \theta \in [\pi/4, 3\pi/4]$, and $I_{in\_ave} = 100A$. So, $\frac{2}{\pi}\int_{\pi/4}^{3\pi/4} B\sin\theta d\theta = 100$. $B_2 = 50\pi/\sqrt{2}$, the input current ripple is about 32.5 A. The RMS value of the input current ripple is $I_{in\_4\_RMS} = \sqrt{\frac{2}{\pi}\int_{\pi/4}^{3\pi/4}\left(\frac{50\pi}{\sqrt{2}}\sin\theta - 100\right)^2 d\theta}$, $I_{in\_4\_RMS} = 9.7\ A$ which is about 13% of $I_{in\_3\_RMS}$. So, the loss of the input capacitor is $Loss_4 = I_{in\_4\_RMS}{}^2 \cdot ESR$. So the reduced power loss ratio is $P_{reduce\_ratio} = Loss_4 / Loss_3 = I_{in\_4\_RMS}{}^2 \Big/ I_{in\_3\_RMS}{}^2 = 1.7\%$.

Hence, by using four phases interleaved strategy of improved ZCS voltage multiplier, the input current ripple RMS value is reduced by 87%, and Input capacitor ESR loss is reduced by 98.3% which is a huge reduction. Much smaller capacitor bank could be adopted; the converter efficiency and power density is improved significantly.

4.6 Zero Current Switching Realization Discussion in Different Load and Temperature Situation

The ZCS feature of the proposed circuit can be achieved in full load range if the resonant capacitor and inductor value keeps constant. This is different from some traditional soft switching techniques which have difficulties in realizing soft switching in light load situation. In different load situations, the current through the resonant capacitor and inductor varies, which will cause different temperature rise of the components. Because the value of the resonant capacitor or the stray inductance may change due to different temperature rise, the switching frequency has to be adjusted according to the new resonant value. This can be easily implemented in the practical converter design by adding power and temperature feedback to the control chip such as microcontroller. The correct switching frequency to achieve ZCS according

to different power and temperature situations can be measured and tested beforehand and stored in the control chip as a table. The power and temperature feedback information in the real situation can be used to choose the right switching frequency referring to the table.

4.7 Simulation and Experiment Results

4.7.1 Improved ZCS-MMSCC with continuous input current

Figure 4.14 shows the simulation results of proposed four-phase 4X ZCS-MMSCC as shown in Figure 4.4, with output power 500 W and input voltage 5 V. The converter input is an ideal dc voltage source with 5 V output. All the capacitors including the output capacitor are 47 μF with ESR equals to 0.3 mΩ to simulate the ten MLCC capacitors (C5750X7R2A475K) from TDK connected in parallel.

The stray inductance values of L_{S11}, L_{S21}, L_{S31}, L_{S41}, L_{S15}, L_{S25}, L_{S35}, and L_{S45} are 108 nH, other stray inductance values are 216 nH. Switching frequency is 70.4 kHz. The device turn on resistance is set to be 0.35 mΩ to simulate the two MOSFETs (IPB009N03L) from Infineon connected in parallel. Because of the four phase interleaving operation of this converter, the average input current is 100 A, the peak input current is about 110 A, the input current ripple is about 32.2 A, which is about 20% of the value of the traditional or single-phase ZCS-MMSCC as calculated above. The RMS value of the ripple current is about 9.7 A which is also consistent with above calculation. The device with the same control signal drain to source voltage may be slightly different with each other considering the different position of the stray inductance in the circuit.

The steady state characteristics of the TEG module can be modeled as an ideal voltage source with internal resistance, as shown in Figure 4.2. And this chapter concentrates on the

development of the high voltage gain boost dc-dc converter. So, the functionality of the proposed circuit can be verified by using the dc power supply. The Figure 4.15 and Figure 4.16 show the experiment waveforms of the prototype as shown in Figure 4.11. Figure 4.15 shows that the circuit operates as a step up converter with conversion ratio equals to twelve.

As shown in Figure 4.15, V_{in} is the input voltage, which is about 5 V; V_o is the output voltage which is 60 V; I_S is the switching current of one of the switches. All the other switching devices have the same switching current. The current through the switch achieves ZCS as expected. Figure 4.16 shows the voltage and current waveform of one switch as an example of the prototype operating at 650 W. V_{GS} is the gate drive signal of the switch; V_{DS} is the switch drain source signal; I_S is still the switching current. All the other switches have the similar switching waveforms. It can be shown that, the switch turn on and off at zero current condition. Figure 4.17 shows the estimated loss break down of 630 W prototype using equation (4.1), the estimated efficiency is around 96.7%. MOSFET and capacitor conduction loss are still the major part. Because of a huge input capacitor bank is using, the input capacitor conduction loss is not that significant. When the input power rating is increased, the input capacitor conduction loss percentage could be bigger caused by the huge input current ripple in an optimized design. Input current ripple should be reduced in order to reduce the total converter size and increase the efficiency.

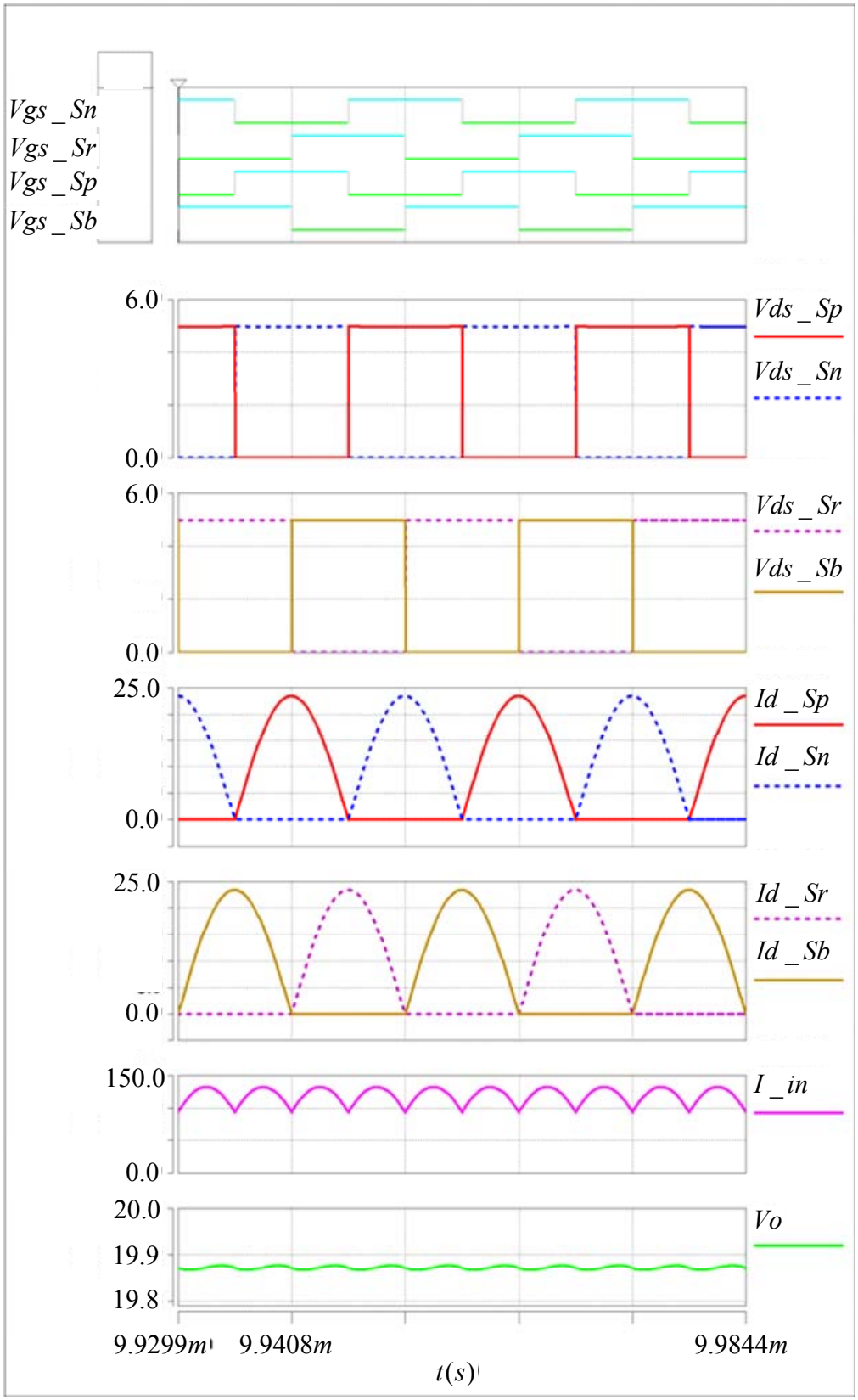


Figure 4.14 Simulation results of a 500 W four-phase 4X ZCS-MMSCC. (V_{in}=5V)

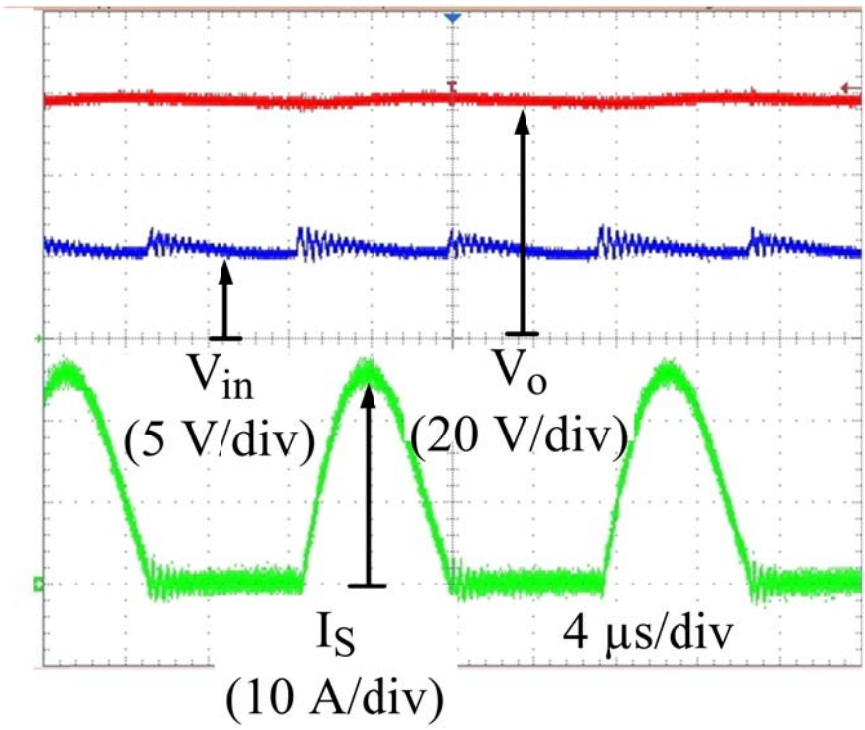


Figure 4.15 Input voltage, output voltage and switch current waveforms.

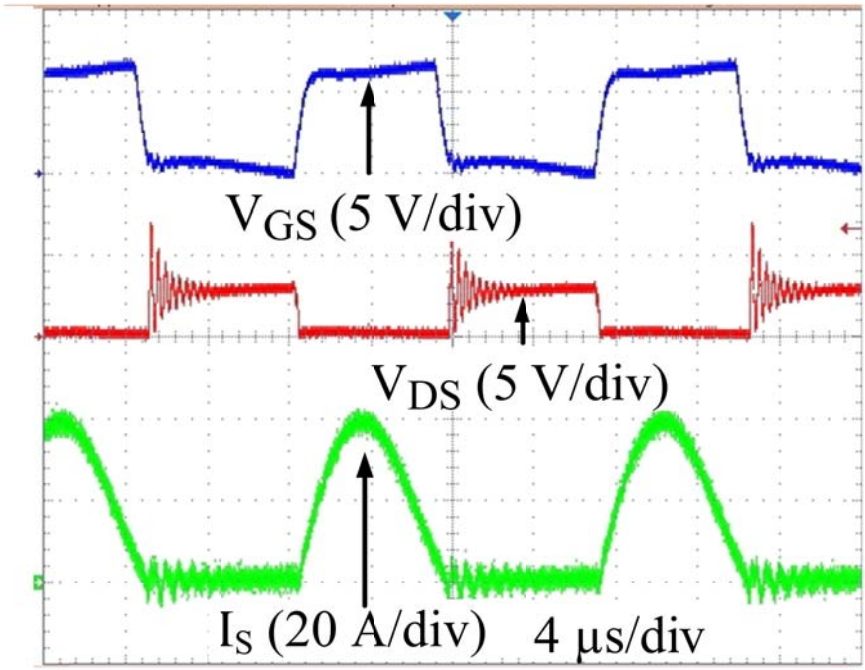


Figure 4.16 One switch gate-source voltage, drain-source voltage and drain-source current at 650 W.

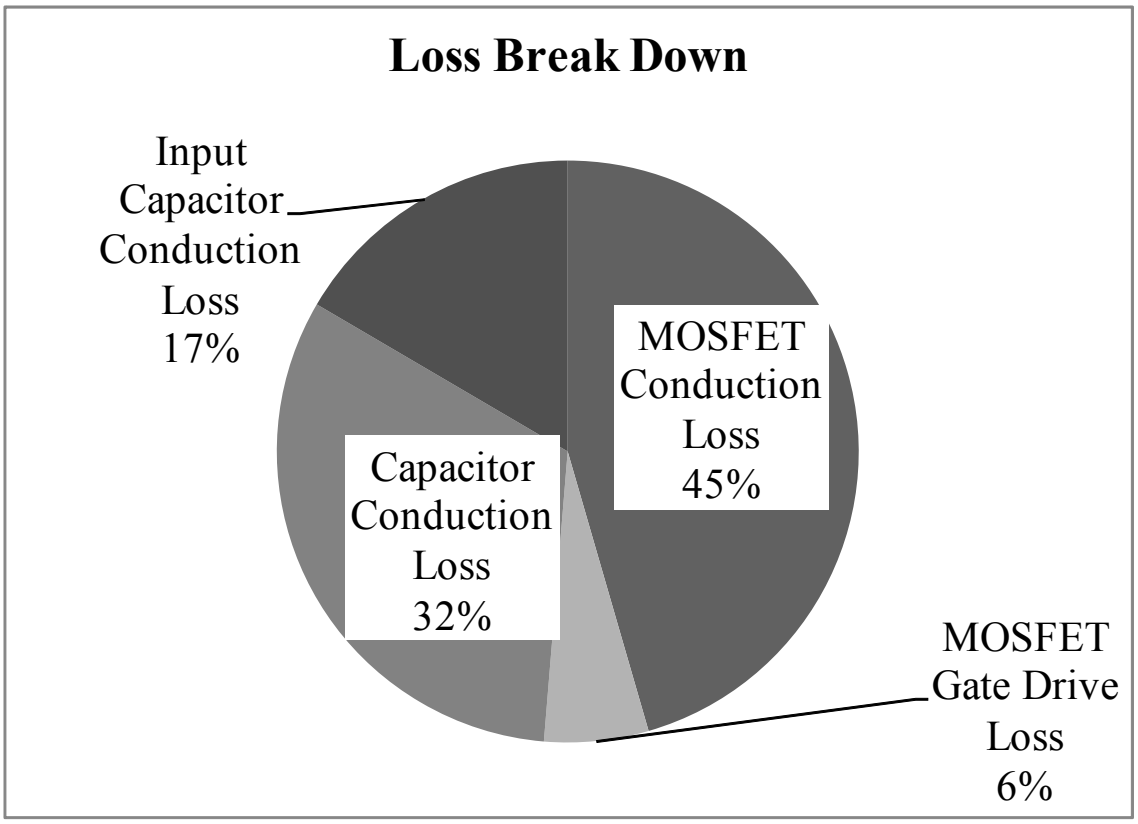


Figure 4.17 Loss break down of the 630 W prototype.

4.7.2 Improved ZCS voltage multiplier with continuous input current

Figure 4.18 shows the simulation results of a 500 W 5 V input 20 V output improved ZCS voltage multiplier with continuous input current waveforms. All the capacitors (C_1 - C_{16}) are 47 μF. Output capacitor C_o is 672 μF. All the stray inductance value are 108 nH ($L_{S1} - L_{S32}$), Switching frequency is 70.4 kHz. The average input current is 100 A. The input current maximum value is about 110 A, the input current minimum value is about 77.8 A, so ripple current is 32.2 A, which is about one seventh of the value of the traditional ZCS voltage multiplier as calculated. The RMS value of the ripple current is about 9.7 A. which is also about 13% of the traditional ZCS voltage multiplier.

4.8 Conclusion

In this chapter, a multiphase NX zero current switching multilevel modular switched-capacitor dc-dc converter with continuous input current and reduced output voltage ripple for TEG application has been proposed. The circuit operation, analysis and features are provided. The input capacitor current ripple and the corresponding power loss is calculated and analyzed. The input current ripple and power loss reduction of proposed circuit are compared with traditional ZCS-MMSCC. The efficiency improvement of the proposed circuit is also estimated. By proper feedback to adjust the switching frequency, the ZCS feature will not lose in different load and temperature conditions. Simulation and experiment result for a 630 W prototype were shown to verify the operation principal. By operating the proposed converter with proper phase shift angle of each phase, the huge input current ripple is cancelled. The huge input capacitor bank can be minimized. The power loss related to the input capacitor ESR can also be minimized, and the converter efficiency is improved accordingly. As a result, smaller size, higher efficiency and higher power density dc-dc converter can be built by using the proposed circuit, which is especially suitable to the high power, high current automotive application.

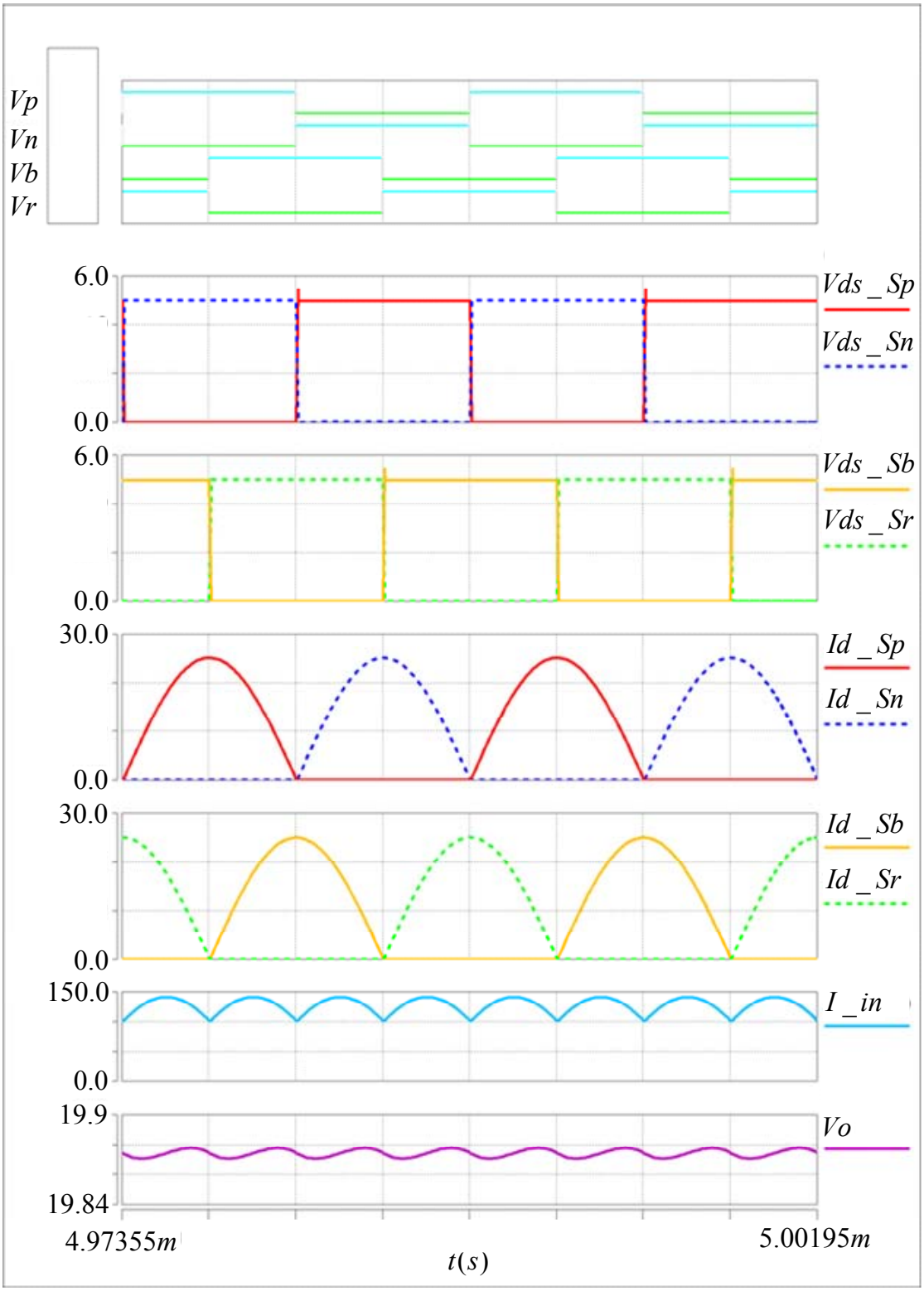


Figure 4.18 Simulation results of ZCS voltage multiplier with continuous input current.

CHAPTER 5
Optimal Design Considerations of Multilevel Modular Switched-Capacitor DC-DC Converter

Magnetic-less multilevel dc-dc converter attracts much attention in automotive application due to its small size and high temperature operation features. Multilevel modular switched-capacitor dc-dc converter (MMSCC) is one of the most promising topologies among them with simple control and reduced switch current stress. This chapter presents an optimal design method for MMSCC to achieve the highest efficiency with smallest size. In order to design the converter with the highest efficiency, the analytical power loss equation of MMSCC should be derived. By considering the stray inductance existing in the circuit, the optimal design point should be considered in two cases, over-damped and under-damped. The converter can be designed to achieve the highest efficiency in both cases. However, in under-damped case, small size multilayer ceramic capacitor can be utilized due to the low capacitance requirement. Although higher switching frequency is required in under-damped case due to practical considerations, zero current switching (ZCS) can be achieved for all the devices. Therefore, the optimal design point of MMSCC with the smallest size and the highest efficiency should be chosen at under-damped case with ZCS. Experimental results of designing MMSCC at under-damped case with ZCS are provided to demonstrate the validity of the proposed method.[5]

5.1 Introduction

[5] This work has been published in part in *Energy Conversion Congress and Exposition, 2011. ECCE 2011. IEEE*, Phoenix, 2011. And it has been accepted by IEEE Transactions on Power Electronics

In recent years, due to the prosperous development of the hybrid electric vehicle (HEV) or electric vehicle (EV) in automotive industry, the high efficiency, high power density, and high temperature operated dc-dc converter is required [137]. The recently developed silicon carbide switching devices and ceramic capacitors are able to operate at very high temperature (above 250 °C) except magnetic cores [138-141]. Therefore, the magnetic-less multilevel switched-capacitor dc-dc converters attract much attention for automotive applications.

Since the 1970s, switched-capacitor dc-dc converters have been investigated due to small size, light weight, and good integration features for power supply on chip [76]. Conventional switched-capacitor dc-dc converters mainly concentrate on the low power conversion area for portable electronic equipment applications [104]. In low power supplies, the output voltage regulation of the switched-capacitor dc-dc converter is the major problem. Many methods to achieve the output voltage regulation have been proposed, but the efficiency has to be sacrificed [73, 89-91, 104, 113, 142-148]. On the other hand, in order to achieve higher efficiency, several zero current switching (ZCS) techniques by inserting a resonant inductor in the switched-capacitor circuits are proposed [84, 87, 88, 149, 150]. However, adding a relatively big magnetic core into the switched-capacitor circuits to achieve soft switching is a contradiction by itself. The small size, good integration and high temperature operation features of the switched-capacitor circuits will be lost [92, 93].

In high power automotive applications, other switched-capacitor circuits, or multilevel dc-dc converters are proposed [82, 95, 96, 138, 151, 152]. The power rating of these multilevel dc-dc converters varies from 1 kW to 55 kW. In order to achieve high efficiency of the multilevel dc-dc converter, many design methods and efficiency analysis have been proposed in the literature [82, 95, 96, 136, 138, 152]. By designing these hard-switched multilevel dc-dc converters

properly, the converter efficiency can achieve up to 98% in 1kW power level to 99% in 10 kW power level. But most of the design methods only consider capacitor charging energy loss, or the influence caused by the capacitor ESR and switch turn-on resistance [82, 96]. The parasitic inductance caused by the circuit layout and the switching device package may influence the converter efficiency significantly [138]. By properly considering the stray inductance, high efficiency multilevel dc-dc converter can be designed [138].

However, the conversion ratio of these multilevel dc-dc converters is limited to two or three times. With the increase of conversion ratio, these multilevel dc-dc converters will suffer high conduction loss, high switching loss, high turn off current and serious voltage overshoot problems. In order to solve the problems of these traditional multilevel dc-dc converter, a multilevel modular switched-capacitor dc-dc converter (MMSCC) is proposed [79, 130-132, 153]. In order to further reduce the switching loss, capacitor size and to achieve high efficiency, the ZCS-MMSCC is proposed by utilizing the stray inductance existing in the circuit [134, 135]. Many other hard switched multilevel dc-dc converters can also utilize the stray inductance to achieve ZCS with the efficiency up to 98% [133, 154]. Although ZCS-MMSCC effectively reduces the switching loss and capacitor size through resonating, it may suffer higher device conduction loss and gate drive loss due to the sinusoidal conduction current and the increased switching frequency than the hard-switched MMSCC. The detailed loss analysis and profound design of hard-switched MMSCC are not addressed in the literature. By considering the stray inductance, high efficiency MMSCC can also be designed. The detailed loss analysis and comparison of the MMSCC and ZCS-MMSCC should be done. Other optimization design methods of switched-capacitor dc-dc converter have also been proposed recently, but none of them considers the stray inductance influence in the circuit [155-157].

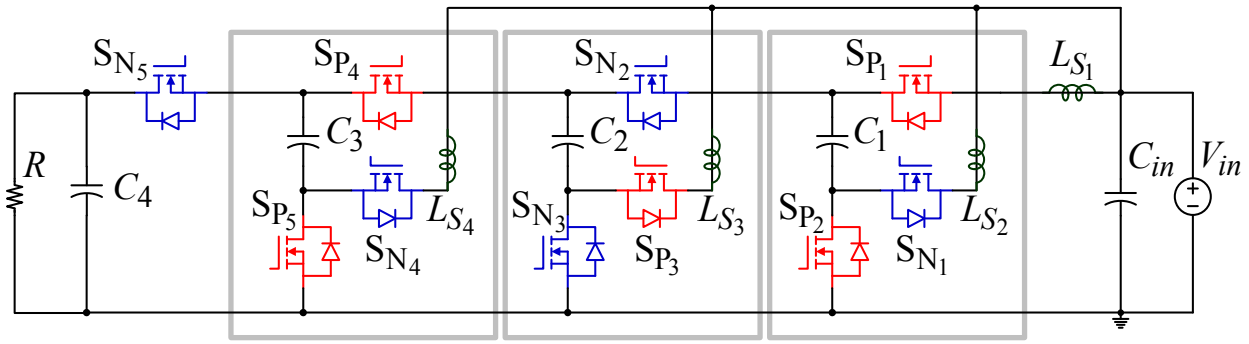
This chapter presents an optimal design method for MMSCC that is able to achieve the most efficient MMSCC design with the smallest size. The power loss analysis of MMSCC considering the switching devices gate drive loss, conduction loss, switching loss and the capacitor conduction loss is proposed; the loss estimation equations are derived. By considering the influence of the parasitic inductance present in the circuit, the equivalent circuits of each switching state of MMSCC become second order series RLC circuits. The minimum power loss can then be determined by four design variables, stray inductance, equivalent resistance, capacitance and switching frequency. The optimal design approach should be divided into two different cases to discuss, overdamped and under-damped. In both cases, there exists an optimal design point with minimal power loss. In over-damped case, the optimal design point happens when the switching current is quasi-square with huge capacitor bank and low switching frequency. In under-damped case, the optimal design point happens when switching frequency equals to the RLC resonant frequency, with all the switches achieving ZCS. The detailed analysis and explanation are provided in the next two sections. The under-damped case with ZCS of all the switches can be considered more optimal than the other case in terms of efficiency and power density. The prototype based on this optimal case has been built; the experimental results with efficiency curves are provided to demonstrate the validity of the proposed optimal design method.

5.2 MMSCC Operation Principle and Power Loss Analysis

In this section, the operation principle of MMSCC is reviewed. The power loss of the switching devices and the capacitor is analyzed. The method of minimizing the total power loss is discussed.

Figure 5.1(a) shows the 4X MMSCC main circuit structure with three module blocks considering the parasitic inductance as an example for operation analysis. The conversion ratio

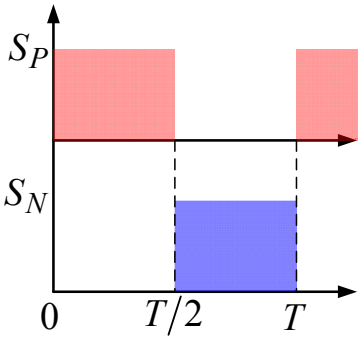
of 4X MMSCC is four. The operation principle can be easily expanded to the NX MMSCC case with N-1 module blocks because of the modular structure of the circuit. Figure 5.1(b) shows the gate signals of the MMSCC. There are only two gate signals of the MMSCC. The two gate signals of the MMSCC are complementary with 50% duty cycle. There are only two switching states of MMSCC. Figure 5.2 shows the simplified equivalent circuits of 4X MMSCC in two switching states. $L_{S1} \sim L_{S4}$ are the equivalent parasitic inductance in each current loop. Figure 5.2(a) shows the case when the switches $S_{P1} \sim S_{P5}$ are turned on. In this switching state, the capacitor C_1 is charged by the input voltage source, the capacitor C_3 is charged by the input voltage source in series with the capacitor C_2. Figure 5.2(b) shows the case when the switches $S_{N1} \sim S_{N5}$ are turned on. In this switching state, the capacitor C_2 is charged by the input voltage source in series with the capacitor C_1, the capacitor C_4 is charged by the input voltage source in series with the capacitor C_3. In the following part, the switching device and the capacitor power loss will be analyzed. The power loss caused by control chip is small enough to be neglected.



(a)

Figure 5.1. 4X MMSCC with three modules main circuit structure considering the stray inductance. (b) Gate signals of the MMSCC with two switching states.

Figure 5.1 cont'd



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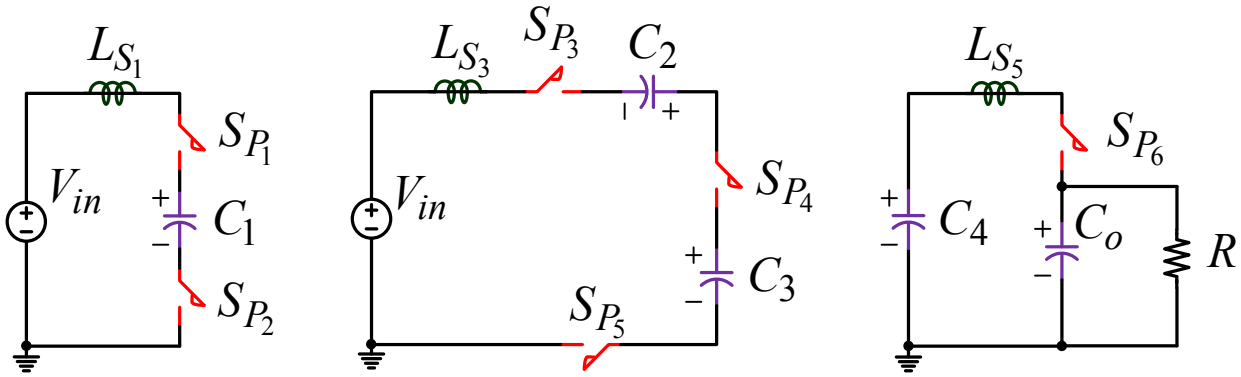
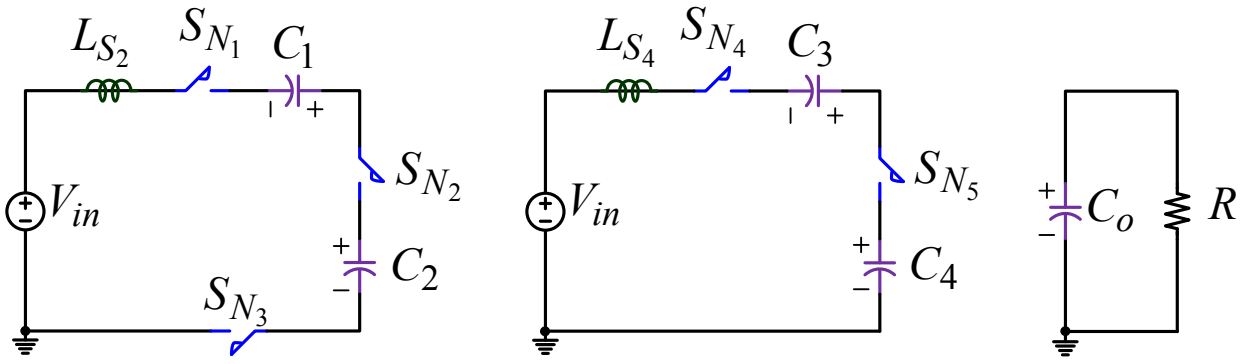


(a)



(b)

Figure 5.2. Simplified equivalent circuits of 4X MMSCC. (a) Switching state I when S_P is on; (b) switching state II when S_N is on

5.2.1 Switching Device Power Loss

5.2.1.1 Conduction loss

Assume all the switching devices are MOSFETs. The conversion ratio is N. The rms value of switch current is I_{S_rms}, the turn-on resistance of the device is R_{on}, and the conduction loss of switching device is P_{S_con}. Thus, the switching device conduction loss can be estimated as follows:

$$P_{S\_con} = I_{S\_rms}{}^2 R_{on} \tag{5.1}$$

5.2.1.2 Gate drive loss

Assume that the gate drive voltage is V_{GS}, switching frequency is f_S, the total gate charge of the device is Q_g, and the gate drive loss of switching device is P_{S_drv}. Thus, the switching device gate drive loss can be estimated using the following equation:

$$P_{S\_drv} = V_{GS} Q_g f_S . \tag{5.2}$$

5.2.1.3 Switching loss

Figure 5.3 shows the device drain-source voltage and drain current for switching loss analysis [158]. Because of the special structure of the circuit, the turn off switching loss can be considered the same as the inductive load. On the other hand, the turn on switching loss should be considered as the LC load. Assume the drain source voltage of the device is V_{DS}, the duration of V_{DS} decreasing to zero is t_1 during the switch turn-on process. This duration t_1 is affected by the miller effect due to the gate resistor R_g and the reverse capacitor C_{rss}. The turn on process ends when V_{DS} reaches zero voltage, and the turn on switching loss of the device is P_{sw_on}. The duration time of V_{DS} increases to the highest value during the switch turn-off process is t_2. The duration t_2 is also caused by the miller effect. After that, the drain current i_D begins to decrease due to the conduction of freewheeling diode. The duration time of i_D decreasing to

zero is t_f, and the turn off switching loss of the device is P_{sw_off}. The total switching loss of the device is P_{sw}. So, the switching loss during turn on and off can be estimated by,

$$P_{sw\_on} = \left(\int_0^{t_1} \left(\frac{I_D}{t_1} t \right) \left(V_{DS} - \frac{V_{DS}}{t_1} t \right) \right) f_S = \frac{1}{6} I_D V_{DS} t_1 f_S \tag{5.3}$$

$$P_{sw\_off} = \left(\frac{1}{2} V_{DS} I_D t_1 + \frac{1}{2} V_{DS} I_D t_f \right) f_S = \frac{1}{2} V_{DS} I_D \left(t_1 + t_f \right) f_S \tag{5.4}$$

$$P_{sw} = P_{sw\_on} + P_{sw\_off} \tag{5.5}$$

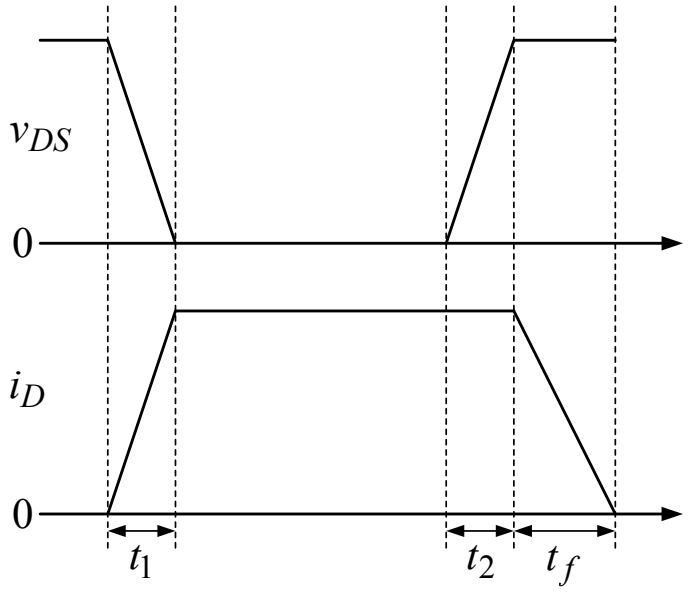


Figure 5.3. MOSFET drain-source voltage and drain current for switching loss analysis.

5.2.2 Capacitor Power Loss

Assume the rms current through the capacitor is I_{C_rms}, the capacitor ESR is R_{ESR}. The capacitor $C_1 \sim C_4$ power loss is P_{C_con}, so the power loss caused by the capacitor ESR can be calculated, as shown in (5.6). The input capacitor C_{in} power loss is P_{Cin_con}. The input capacitor power loss can also be calculated in a similar manner.

$$P_{C\_con} = I_{C\_rms}{}^2 R_{ESR} \tag{5.6}$$

5.2.3 Total Power Loss

The total power loss of the converter is P_{loss}, which is the sum of (3N-2) switching devices power loss, N capacitors power loss with the input capacitor power loss, which can be estimated by

$$P_{loss} = (3N-2)(P_{S\_con} + P_{S\_drv} + P_{sw}) + NP_{C\_con} + P_{Cin\_con} + P_{Co\_con} \quad (5.7)$$

In order to minimize the total power loss, each part of (5.7) should be minimized. The device gate drive loss is related to the gate drive voltage, total gate charge and the switching frequency. The rms value of the switch drain current I_{S_rms}, the switch drain current I_D, and the rms value of capacitor current I_{C_rms} will vary due to the value of capacitance, stray inductance, switching frequency, the switch turn on resistance, and the capacitor ESR. So the device and the capacitor should be chosen properly to minimize the total power loss.

In every switching state, the simplified equivalent circuits of MMSCC can be considered as the series RLC circuit, as shown in Figure 5.4. By using high capacitance electrolytic capacitor and low switching frequency, the MMSCC can be designed in over-damped situation. In this case, the current waveform of the switch is quasi-square, and the switching loss should be considered. By using low capacitance multilayer ceramic capacitor (MLCC) and high switching frequency, MMSCC can be designed in under-damped situation with ZCS. In this situation, the current waveform of the switch is half sinusoid, and the capacitor current waveform is sinusoid. With the same power to be delivered, the sinusoid current has larger rms value than the quasi-square current. So the switch conduction loss is larger in this case. The gate drive loss is also increased due to the increased switching frequency. But the switching loss is eliminated in this case, and MLCC has better performance in terms of ESR than electrolytic capacitor. So, the

conduction loss caused by the capacitor ESR can also be reduced in the under-damped situation. In order to estimate the total power loss of MMSCC correctly, two different cases should be considered and designed respectively to achieve the optimal design of the MMSCC. Detailed design considerations will be discussed in the next sections.

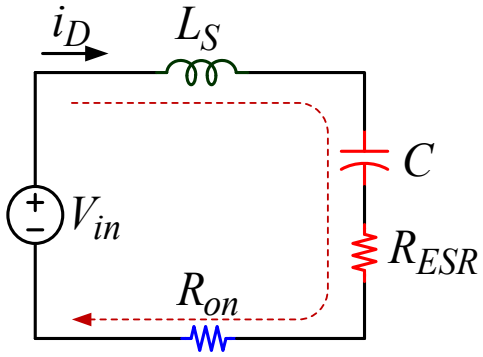


Figure 5.4. The unified equivalent circuit of MMSCC for power loss estimation.

5.3 Optimal Design Considerations

According to the above analysis, the MMSCC can be designed in either over-damped or under-damped situations. By proper design, either of them may achieve high efficiency. In this section, the switching current and corresponding rms value in two different cases will be analyzed and calculated. So, the conduction loss of the two cases can be compared exactly. The total power loss and other design issues will be compared and discussed between the two cases. Figure 5.5 shows the simplified equivalent circuit used for switching current calculation. L can be considered as the sum of the stray inductance, in one switching loop $L = \sum L_S$. C can be considered as the value of all the capacitance in series in one switching loop. R can be considered as the sum of all the turn on resistance and the capacitor ESR in one switching loop, $R = \sum R_{on} + \sum R_{ESR}$. In every switching state, the circuit behavior can be considered as the step response of this series RLC circuit. The initial value of capacitor voltage is V_C , and the initial

value of inductor current is zero. The natural frequency is $\omega_0 = \sqrt{1/LC}$ and the damping ratio is $\zeta = R\sqrt{C/L}/2$. So, the capacitor voltage can be calculated using the following differential equations in (5.8). The value of R, L, and C will vary due to different design. The solution of the above differential equation should be divided into two cases, over-damped case and under-damped case with different types of roots. The critical damped case is similar to over-damped case, which will not be discussed in detail here.

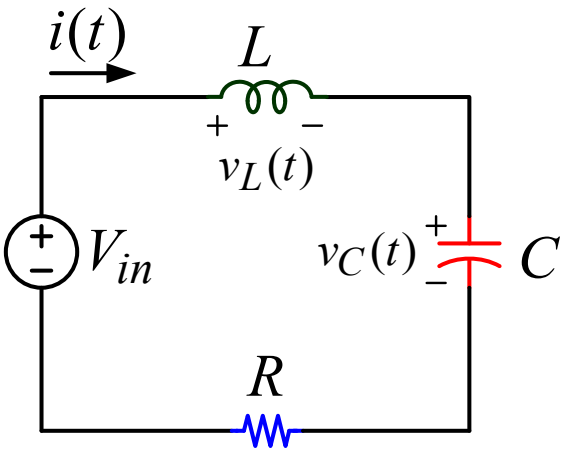


Figure 5.5. Simplified equivalent circuit for switching current calculation.

$$v_C(t) + RC\frac{dv_C(t)}{dt} + LC\frac{d^2v_C(t)}{dt} = V_{in},\ v_C(0) = V_C,\ \frac{dv_C(0)}{dt} = 0 \qquad (5.8)$$

5.3.1 Over-damped Case

($\zeta > 1$, or $R^2C > 4L$)

When the damping ratio of the circuit is larger than 1, the circuit works in over-damped case. So in the over-damped case, the capacitor voltage can be calculated as shown in (5.9). Since the capacitor current in one switching state is the same with the switch current, so the switch current can be calculated as show in (5.10).

$$v_C(t) = \frac{V_C - V_{in}}{2\omega_0\sqrt{\zeta^2-1}}\begin{pmatrix} -\omega_0\left(-\zeta-\sqrt{\zeta^2-1}\right)e^{\omega_0\left(-\zeta+\sqrt{\zeta^2-1}\right)t} \\ +\omega_0\left(-\zeta+\sqrt{\zeta^2-1}\right)e^{\omega_0\left(-\zeta-\sqrt{\zeta^2-1}\right)t} \end{pmatrix} + V_{in} \tag{5.9}$$

$$i_C(t) = i_S(t) = C\frac{dv_C(t)}{dt} \tag{5.10}$$

Plug the capacitor voltage equation (5.9) into the above equation , the capacitor current in one switching period, or the switch current can be calculated as follows,

$$\begin{aligned} i_S(t) = C\frac{dv_C(t)}{dt} &= \frac{C\omega_0}{2\sqrt{\zeta^2-1}}\left(e^{\omega_0\left(-\zeta-\sqrt{\zeta^2-1}\right)t} - e^{\omega_0\left(-\zeta+\sqrt{\zeta^2-1}\right)t}\right) \\ &= \sqrt{\frac{C}{R^2C-4L}}\left(e^{\left(-\frac{R}{2L}-\sqrt{\left(\frac{R}{2L}\right)^2-\frac{1}{LC}}\right)t} - e^{\left(-\frac{R}{2L}+\sqrt{\left(\frac{R}{2L}\right)^2-\frac{1}{LC}}\right)t}\right) \end{aligned} \tag{5.11}$$

In order to design the MMSCC operating in the over-damped case, the stray inductance should be minimized to satisfy the inequality $R^2C > 4L$ and minimize the voltage overshoot. For example, to design a MMSCC in the 100s W~10s kW range, the stray inductance existing in the circuit is in the 1s nH~10s nH range. And the sum of capacitor ESR and switch turn on resistance are in the 1s mΩ range. So in order to satisfy the over-damped condition, the capacitance should be in the 10s mF range, high capacitance electrolytic capacitors have to be used. Figure 5.6(a) shows the normalized switch current with the change of capacitance. With the decrease of capacitance, the switch current will drop faster, which will cause higher rms value of switch current, so the capacitance should be designed as large as possible. Figure 5.6(b) shows the normalized switch current with the change of resistance. With the increase of resistance, the converter power transfer capability will drop. Although R and C can be any value

to meet the $R^2C > 4L$ condition, large capacitance with small resistance is preferred in the converter design.

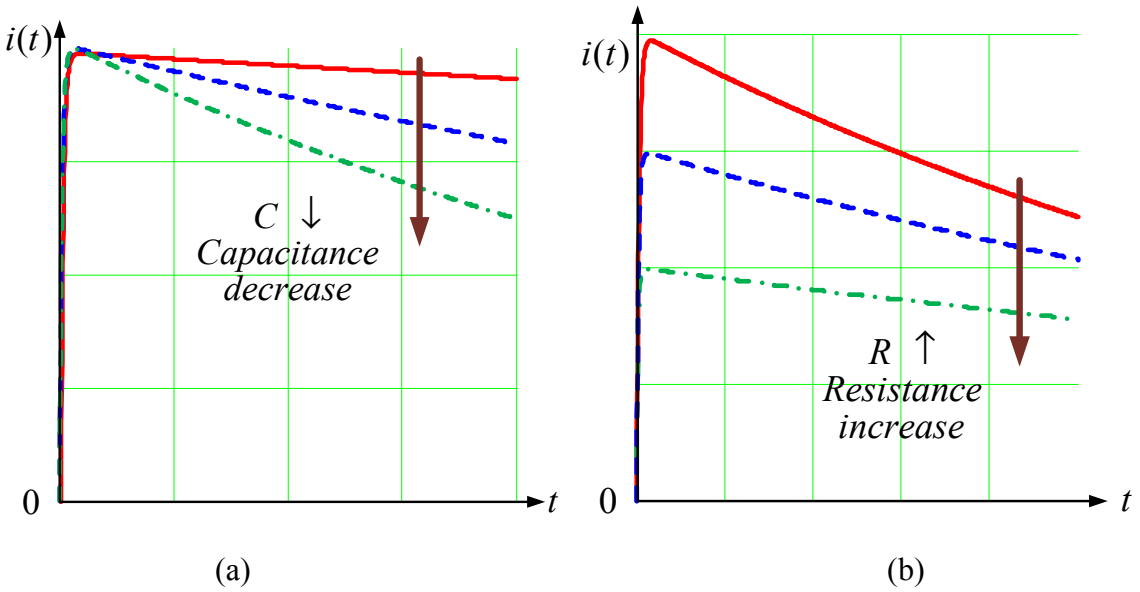


Figure 5.6. (a) Normalized switching current with the decrease of capacitance. (b) Normalized switching current with the increase of resistance.

The switching device average current I_{S_ave} and the rms current I_{S_rms} in one switching period can be calculated as (5.12) and (5.13). T_S is the switching period. For a certain output power, the value of the switch average current is determined, although the shape of the switch current may vary according to different circuit parameters. The value of the switch rms current can determine the total conduction loss of the switch and the capacitor in one switching state. In order to minimize the total conduction loss of the switch and the capacitor, the switch rms current should be minimized. The ratio of rms current over average current is defined as *r*, as shown in (5.14). This ratio can be considered as the normalized switch rms current, which is irrelevant to the output power. By estimating this ratio, the optimal R, L, C parameter and switching frequency with minimum conduction loss can be found. The ratio of switch current over average current is defined as I_{off} , as shown in (5.15). This ratio can be considered as the

normalized switch turn off current, which is related to switching loss. The circuit parameter, R, L, C and switching frequency f_S should be selected carefully to minimize *r* and I_{off} .

$$I_{S\_ave} = \frac{1}{T_S}\int_0^{T_S/2} i_S(t)dt \tag{5.12}$$

$$I_{S\_rms} = \sqrt{\frac{1}{T_S}\left(\int_0^{T_S/2} {i_S}^2(t)dt\right)} \tag{5.13}$$

$$r = \frac{I_{S\_rms}}{I_{S\_ave}} \tag{5.14}$$

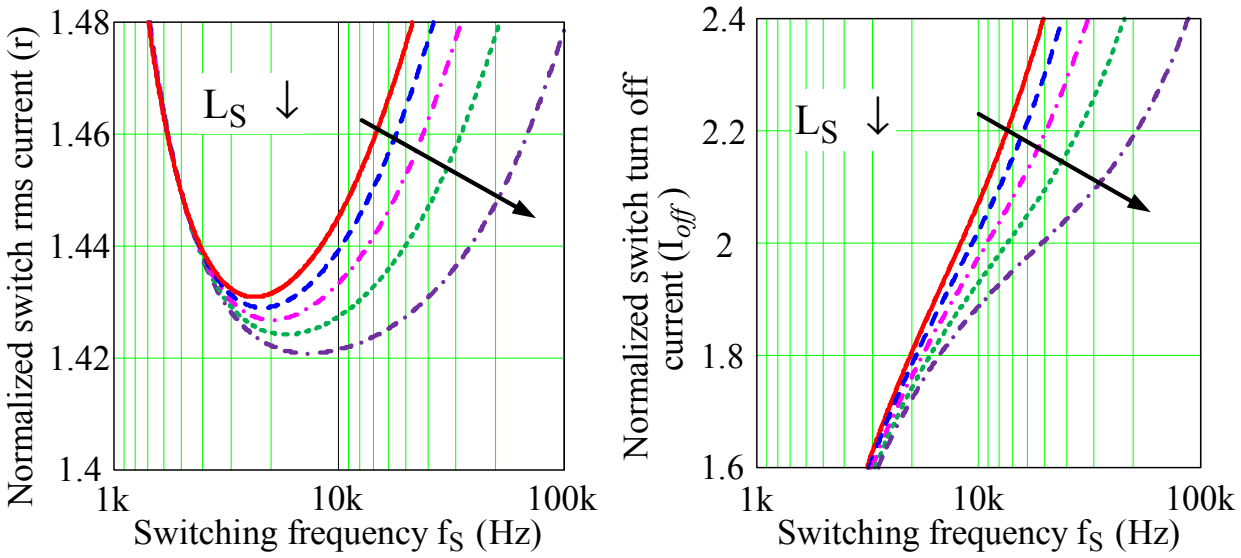
$$I_{off} = \frac{i_S\left(T_S/2\right)}{I_{S\_ave}} \tag{5.15}$$

In order to minimize the total power loss, the total conduction loss, switching loss and gate drive loss have to be minimized. The minimum conduction loss happens when the switching current is quasi-square and r is equal to $\sqrt{2}$. At this time, I_{off} is equal to 2. If r can be designed at about $\sqrt{2}$ by using proper circuit parameter at relative low switching frequency (less than 10 kHz), the conduction loss can be minimized, the switching loss and gate drive loss will not be significant due to the low switching frequency, one of the optimal design points can be achieved. Table 5.1 shows some circuit design parameters for a MMSCC in the 100s W to 10s kW range. In the following analysis, the design comparison will be made using the circuit parameter in Table 5.1.

Table 5.1 Circuit parameter examples for power loss analysis.

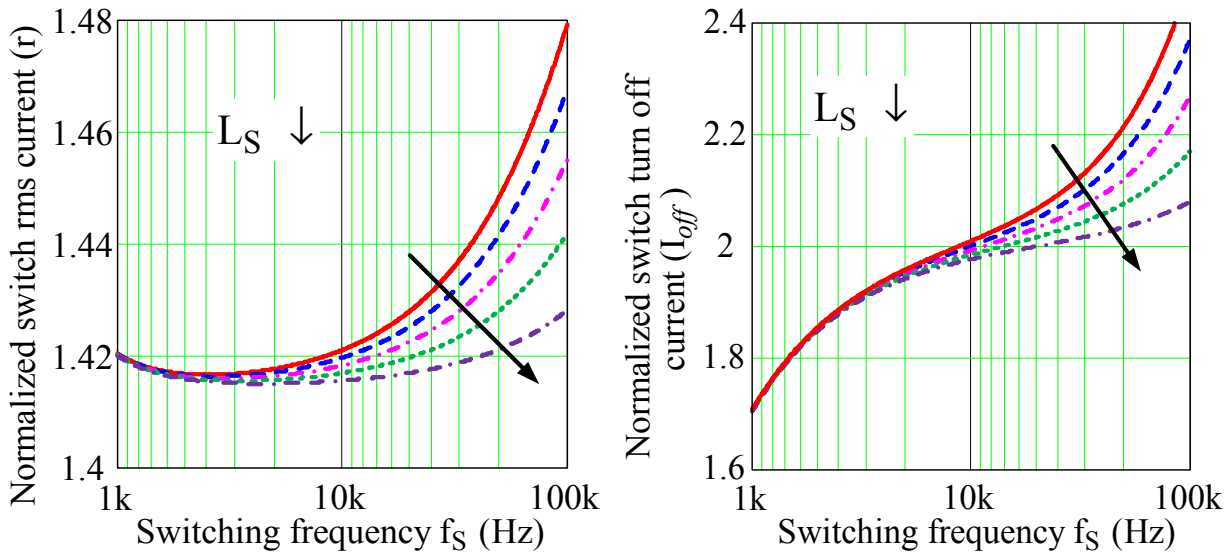
Capacitance	Resistance	Inductance
C1 : 160 mF	R1: 10 mΩ	L1: 10 nH
C2: 80 mF	R2: 8 mΩ	L2: 8 nH
C3: 40 mF	R3: 6 mΩ	L3: 6 nH
C4: 20 mF	R4: 4 mΩ	L4: 4 nH
C5: 10 mF	R5: 2 mΩ	L5: 2 nH

Figure 5.7 shows the normalized switch rms current r and switch turn off current I_{off} versus switching frequency when C = 160 mF, R = 2 mΩ, and Ls changed from 10 nH to 2 nH. When the Ls = 2 nH, the r reach the minimum value. And the minimum value of r does change much when Ls is changed from 10 nH to 2 nH, as shown in Figure 5.7(a). The optimal switching frequency for this case is from 5 kHz to 10 kHz, when the switching frequency is less than 5 kHz, the conduction loss increases very fast. The switch turn off current is also similar in this frequency range, as shown in Figure 5.7(b). Figure 5.8 shows the similar curve as shown in Figure 5.7 by changing the resistance to 10 mΩ. The optimal switching frequency range in this case is extended from 1 kHz to 10 kHz as shown in Figure 5.8(a). And the optimal switching frequency should be designed about 1 kHz or even lower since the switching loss and gate drive loss can be minimized. Although the optimal switching frequency is reduced in this case with relatively low r and I_{off} , the total R in the circuit still needs to be minimized to design MMSCC, since the conduction loss is increased by five times with the increase of R.



(a) (b)

Figure 5.7. (a) Normalized switch rms current (r) and turn off current I_{off} versus switching frequency, when C=160 mF, R=2 mΩ and Ls changed from 10 nH to 2 nH.



(a) (b)

Figure 5.8. (a) Normalized switch rms current (r) and turn off current I_{off} versus switching frequency, when C=160 mF, R=10 mΩ and Ls changed from 10 nH to 2 nH.

Figure 5.9 and Figure 5.10 show the similar case as shown in Figure 5.7 and Figure 5.8 with reduced capacitance. When the capacitance is reduced, high switching frequency has to be used to reach the minimum conduction loss as shown in Figure 5.9(a) and Figure 5.10(a). However, in

this case the switching loss and gate drive loss will be about 10 times higher than the previous case with high capacitance. Since the conduction loss can be designed at similar level with different capacitance, high capacitance is preferred in the design with less switching loss. As shown in Figure 5.9(b), when the switching frequency is less than 9 kHz, the turn off current is almost zero, ZCS may be achieved in this case. However, r is already higher than $\pi/2$, which means the conductional loss in this case will be higher than the under-damped case with sinusoid current waveform. Besides, since the capacitance in over-damped case is in the 10s mF range, electrolytic capacitor has to be used. And more electrolytic capacitors in parallel mean low turn on resistance.

Therefore, to design the MMSCC in over-damped case, many electrolytic capacitors in parallel with high capacitance, low resistance and low stray inductance operating at low switching frequency are preferred in the design to reach high efficiency. However, many electrolytic capacitors in parallel will increase the total converter size which is a major disadvantage to design MMSCC in this case.

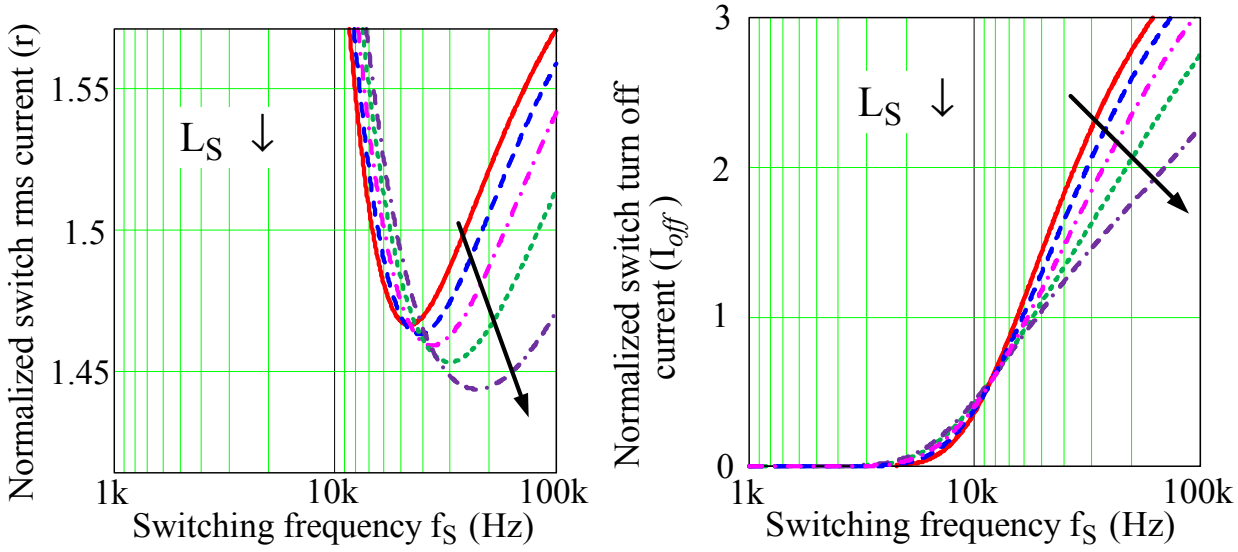


Figure 5.9. (a) Normalized switch rms current (r) and turn off current I_{off} versus switching frequency, when C=10 mF, R=2 mΩ and Ls changed from 10 nH to 2 nH.

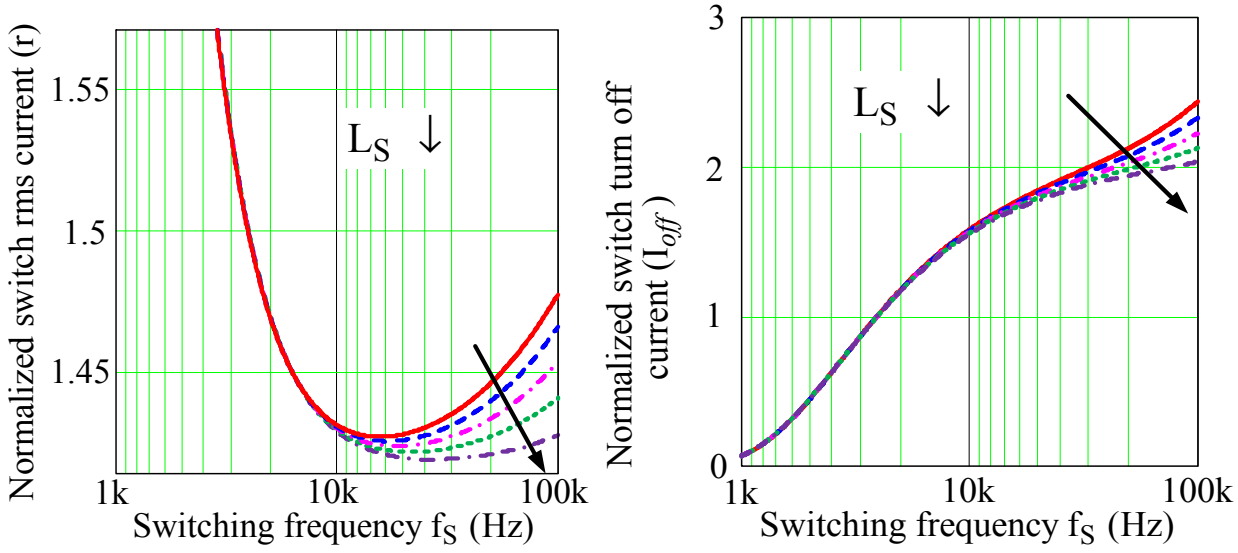


Figure 5.10. (a) Normalized switch rms current (r) and turn off current I_{off} versus switching frequency, when C=10 mF, R=10 mΩ and Ls changed from 10 nH to 2 nH.

5.3.2 Under-damped Case

($\zeta < 1$, or $R^2C < 4L$)

When the damping ratio of the circuit is less than 1, MMSCC can also be designed at the under-damped case with resonate switch current. In this case, the stray inductance does not need to be minimized purposely, and it could be in the range of 10s~100s nH. By proper circuit layout, the stray inductance can be designed with the same value or the convenience of designing other circuit parameters. The resistance should also in the range of several mΩ, the resonant capacitance should be chosen in the 10s μF range, which is very easy to be achieved using MLCC. And the switching frequency is only in the 10s kHz range to match the resonant frequency. In the under-damped case, the capacitor voltage and the switch current can be calculated as shown in (5.16).

$$v_C(t) = e^{-\alpha t}(V_C - V_{in})\left(\cos(\omega_d t) + \frac{\alpha}{\omega_d}\sin(\omega_d t)\right) + Vin \ , \ i_S(t) = C\frac{dv_C(t)}{dt} \qquad (5.16)$$

The switching current is become damped sinusoid waveform, α = R/2L which is the neper frequency, and $\omega_d = \sqrt{\omega_o{}^2 - \alpha^2}$, which is the natural resonant frequency. Figure 5.11~Figure 5.13 shows the switch current in three cases when the switching frequency is smaller, equal to or larger than the resonant frequency. Obviously, with the same average current, the case shown in Figure 5.11 has largest rms value of switch current, because the switch current will resonant to the negative part, which means the power will flow back to the input during this period.

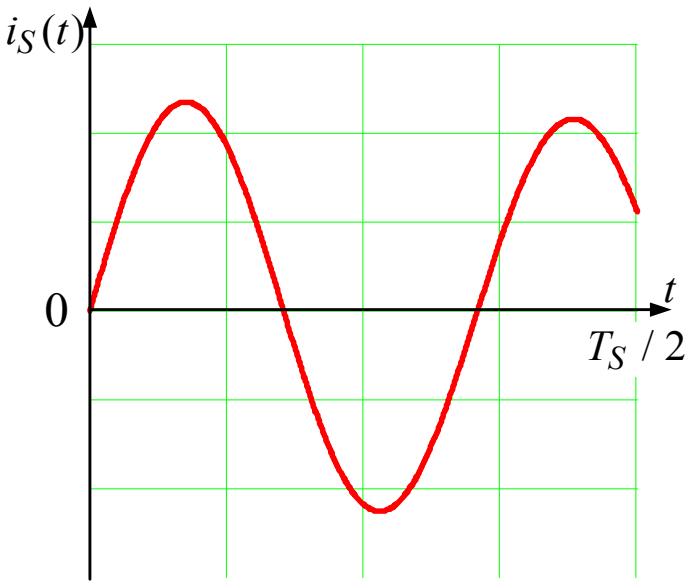


Figure 5.11 Normalized switch current when switching frequency is smaller than resonant frequency.

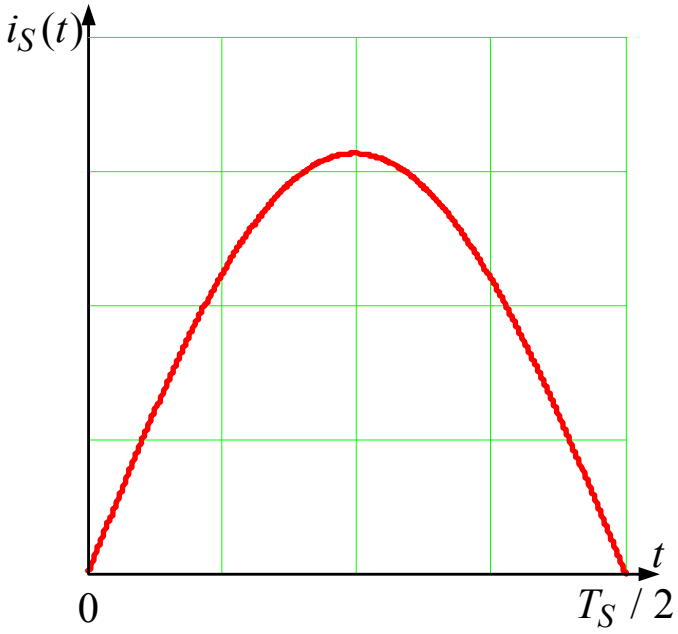


Figure 5.12 Normalized switch current when switching frequency is the same as the resonant frequency.

When the switching frequency is equal to the resonant frequency, ZCS for all the switches can be achieved, as shown in Figure 5.12. The normalized rms current (r) is equal to $\pi/2$ in this case which is only 11% higher than the best case in over-damped condition. The conduction loss

in this case is about 23% larger than the quasi-square current waveform in over-damped condition. However, the switching loss is eliminated in this case, the total power loss in this case may be designed similar to the over-damped case. Since only ceramic capacitors are used in this case, the total converter size is reduced significantly than the over-damped case. By design the MMSCC in under-damped case, the total converter sized can be minimized without increasing total power loss. The EMI can also be reduced.

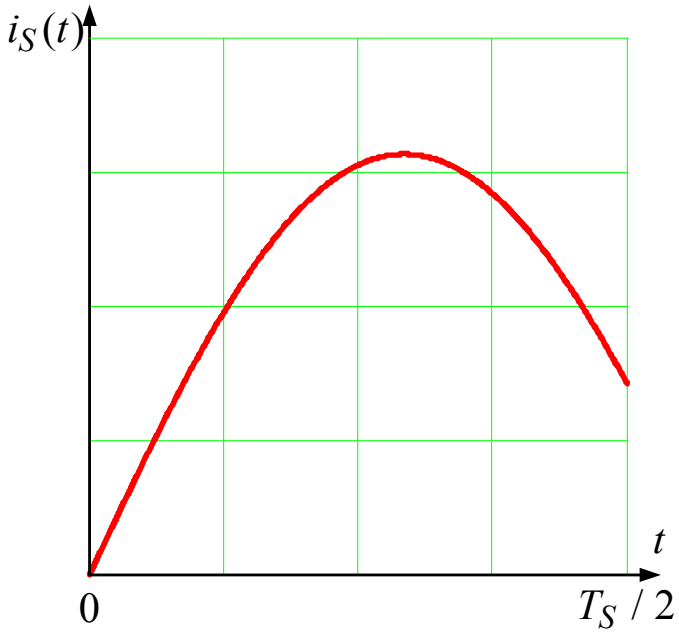


Figure 5.13 Normalized switch current when switching frequency is larger than the resonant frequency.

Although the rms value of the case shown in Figure 5.13 is slight smaller than the case shown in Figure 5.12 using the similar analysis method shown in the over-damped case, the switching loss of the case shown in Figure 5.13 will be significant. Since the stray inductance in under-damped case is relatively large, the energy stored in the stray inductance may cause serious voltage overshoot across the devices. Therefore, the optimal design point of under-damped case should be the case shown in Figure 5.12 with ZCS for all the switching devices.

5.4 Design Example and Experimental Results

A 150 W 5 V~20 V 4X MMSCC prototype operating at under-damped case with ZCS for all switches has been built. The switching frequency is about 45 kHz. The stray inductance L_{S1} =250 nH, $L_{S2} = L_{S3} = 2L_{S1}$, L_{S4} should be designed a little smaller than L_{S2} and L_{S3} due to the influence of the output current. The switching devices are two 30 V 180 A MOSFETs IPB009N03L from Infineon connected in parallel. Resonant capacitor are ten 100 V 4.7 μF MLCC C5750X7R2A475K from TDK in parallel. Input capacitor are fourteen 6.3 V 470 μF conductive polymer aluminum solid electrolytic capacitors PLE0J471MDO1 from nichicon connected in parallel. Gate drive voltage is 15 V. Figure 5.14~Figure 5.16 shows the experimental waveforms of the above mentioned prototype.

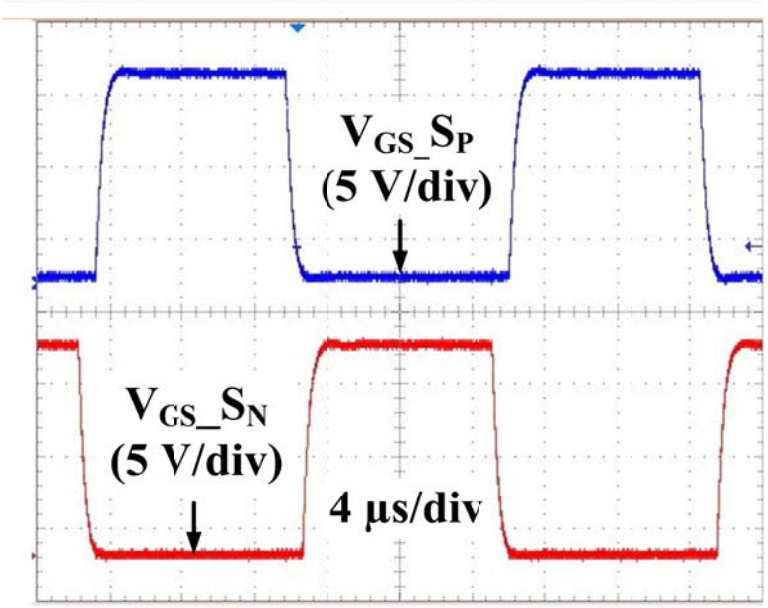


Figure 5.14 Gate drive signals of S_P and S_N.

Figure 5.14 shows the complementary gate drive signals of S_P and S_N with about 49% duty cycle due to some deadtime. Figure 5.15 shows the gate drive voltage, drain-source voltage and switch current of S_{P1}. The ZCS of switch has been achieved.

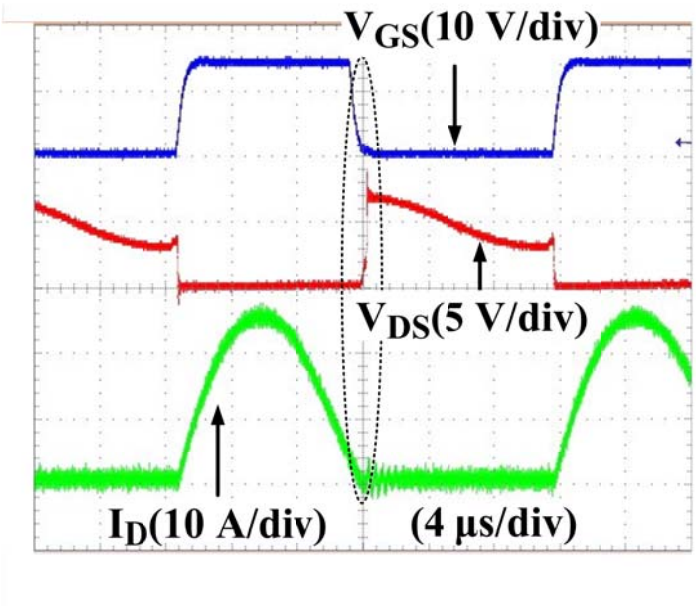


Figure 5.15 Voltage and current waveforms of S_{P1}.

Figure 5.16 shows the zoomed in waveforms of the switch S_{P1} turn off transient, which indicates that the switch achieves ZCS during turn off.

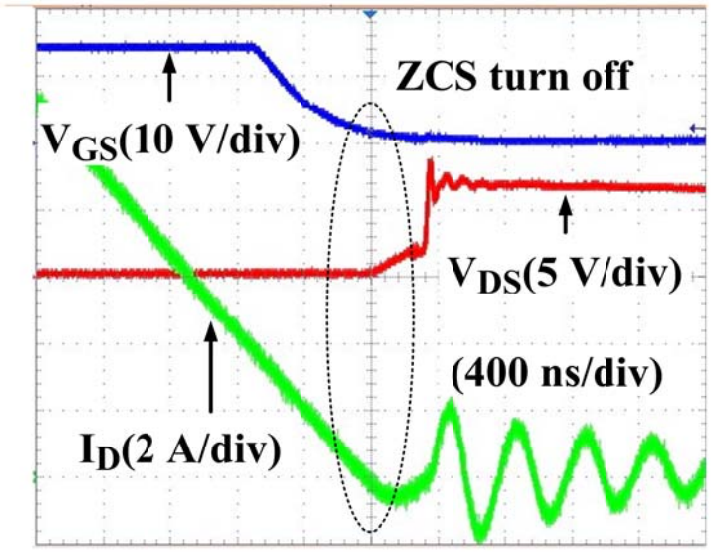


Figure 5.16 Zoomed in voltage and current waveforms of S_{P1}

From the experiment results, we can derive that the switch S_{P1} can achieve ZCS in both turn on and turn off. Other switches have the voltage and current waveforms similar to S_{P1} which

will not be shown here. Figure 5.17 shows the measured efficiency curve using Yokogawa WT1600 digital power meter of 4X MMSCC designed at under-damped case with ZCS, and the estimated efficiency using the power loss analysis of (5.7).

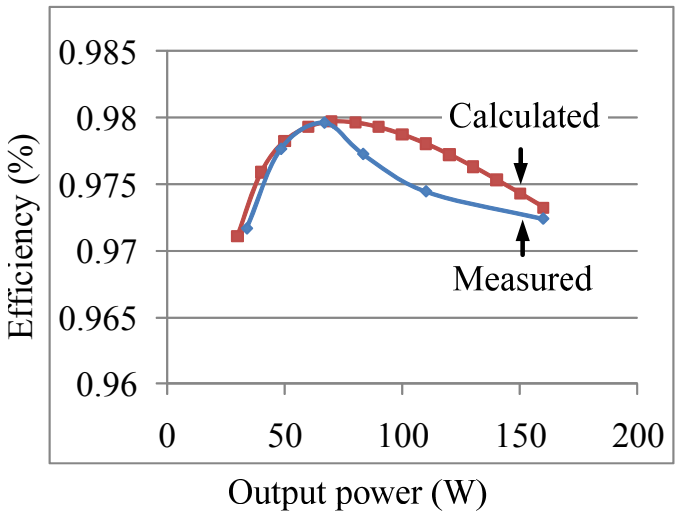


Figure 5.17 Measured and calculated efficiency.

5.5 Conclusion

This chapter presents an optimal design method for MMSCC to achieve the highest efficiency with the smallest size. By considering the influence of the stray inductance properly, the optimal design point should be discussed in two cases, over-damped case and under-damped case. In both cases, the optimal design point with highest efficiency has been achieved. But the over-damped case has to utilize huge capacitor bank with many high capacitance electrolytic capacitors to achieve high efficiency; while in the under-damped case, low capacitance, low ESR, and small size MLCC can be utilized to achieve high efficiency. Although the converter has to operate at higher switching frequency in under-damped case than in over-damped case due to the practical consideration, ZCS can be achieved in under-damped case which eliminates the switching loss. Hence, to design the MMSCC at the under-damped case with MLCC, both high efficiency and small size targets can be achieved. A 150 W MMSCC prototype designed at

under-damped case with ZCS has been built. High efficiency (up to 98%) and high power density (about 300 W / in^3) have been proved to validate the optimal design procedure.

CHAPTER 6
A Double-Wing Multilevel Modular Capacitor-Clamped DC-DC Converter with Reduced Capacitor Voltage Stress

This chapter presents a double-wing multilevel modular capacitor-clamped (DW-MMCCC) dc-dc converter. Compared to the traditional single-wing (SW) MMCCC with the same voltage conversion ratio, the capacitor voltage stress of DW-MMCCC is reduced by half. And the switch and capacitor current stress, the switch voltage stress of the SW-MMCCC and the DW-MMCCC are the same. When the conversion ratio is equal to N, the total device and capacitor number of the even conversion ratio DW-MMCCC is 3N-2 and N, which is the same with the corresponding SW-MMCCC. The total device and capacitor number of odd conversion ratio DW-MMCCC is 3N-1 and N+1 respectively. By using the distributed stray inductance existing in the circuit, zero current switching (ZCS) can be achieved for all the switches of DW-MMCCC. And by using multi-phase DW-MMCCC, the input current ripple and input capacitor size can be reduced significantly. Compared with the traditional multilevel dc-dc converter, the power density of DW-MMCCC could be increased by about ten times. A 100 W three-phase 3X-ZCS-DW-MMCCC prototype has been built and tested. The simulation and experimental results are provided to verify the validity of the proposed converter..[6]

6.1 Introduction

[6] This work has been published in part in *Energy Conversion Congress and Exposition, 2011. ECCE 2011. IEEE*, Phoenix, 2011. And it will be submitted to IEEE Transactions on Power Electronics

With the development of hybrid electric vehicle (HEV) and electric vehicle (EV), high power density and high temperature operated dc-dc converter or dc-ac inverter are required by the automotive industry. The traditional inverter used in the HEV only utilizes the dc-link capacitor and the silicon based switching devices. The enabling technology of silicon carbide (SiC) switching devices and high performance film/ceramic capacitors can effectively reduce the inverter size. However, the traditional dc-dc converter used in the HEV requires an inductor, which is bulky and lossy. In order to achieve high efficiency, high power density dc-dc converter, many magnetic-less multilevel dc-dc converters are proposed [82, 94-96, 102, 138, 151, 152, 159, 160]. For these traditional multilevel dc-dc converters, there are several advantages, such as no magnetic components, high efficiency, low device voltage stress, low device count, etc. But the conversion ratio of these converters is usually limited to two or three times. When the conversion ratio is increased to N times, the conduction loss of these converters is increased significantly, due to the fact that N devices have to be connected in series to conducting the current. The turn off current is also increased to N times of load current, which will cause severe voltage overshoot across the device [151]. Besides, because of the asymmetric charging loop of these converters [94, 96, 151, 152], it's hard to utilize the stray inductance to achieve zero current switching (ZCS) for the switches.

In order to overcome the disadvantages of the traditional multilevel dc-dc converter in high conversion ratio applications, a multilevel modular capacitor-clamped dc-dc converter (MMCCC) is proposed [79, 130-132, 153]. This circuit is referred as single-wing (SW) MMCCC in this chapter, as shown in Figure 6.1. Compared to the traditional multilevel dc-dc converter, the conduction loss and the switching loss of SW-MMCCC are reduced, the control is become simple. At most three devices are connected in series to charge the capacitor. And the conduction

loss will not increase with the increase of the conversion ratio. All the devices of SW-MMCCC are conducted complementary with 50% duty cycle, so the turn off current will not increase according to the conversion ratio. Although the total device number of SW-MMCCC is increased, the current stress and conduction loss of SW-MMCCC are both reduced. So, the total power loss of SW-MMCCC is reduced, which makes it a good candidate for high conversion ratio application. However, similar to the traditional multilevel dc-dc converters, a huge electrolytic capacitor bank with high capacitance has also to be utilized for SW-MMCCC to achieve high efficiency [96]. And all the switches behave hard switching, which will cause high switching loss and voltage overshoot. A ZCS-SW-MMCCC is proposed to solve the problems of SW-MMCCC [133-135]. By utilizing the distributed stray inductance existing in the circuit, ZCS can be achieved for all the switches due to the resonance. In this case, small size, low ESR and low capacitance multilayer ceramic capacitor (MLCC) can be used. By using the soft-switching technique, switching loss can be eliminated; the capacitor ESR loss can be reduced; the capacitor size is also reduced significantly. And the high input current problem of ZCS-SW-MMCCC can be solved by using interleaving technique [154]. However, the capacitor voltage stress of SW-MMCCC/ZCS-SW-MMCCC is the same. The voltage stress of each capacitor is increased from 1 to N times the low side voltage. When the conversion ratio is increased, the capacitors voltage stress is increased accordingly. The peak capacitor voltage stress is the same as the high voltage side output voltage.

This chapter presents a double-wing (DW) MMCCC with all the advantages of SW-MMCCC and reduced capacitor voltage stress. The DW-MMCCC with even number of conversion ratio and odd number of conversion ratio are slightly different, which are referred as even-DW-MMCCC and odd-DW-MMCCC respectively. The control strategy, the switching device current

and voltage stress and the capacitor current stress of the DW-MMCCC are the same as SW-MMCCC. With the same conversion ratio, the total device and capacitor number of even-DW-MMCCC are the same as the SW-MMCCC, while peak capacitor voltage stress is reduced by half. The odd-DW-MMCCC has one extra switching device and capacitor compared to the SW-MMCCC, but the peak capacitor voltage stress is reduced by more than half. When the conversion ratio is high, the total capacitor and switching device number difference of the odd-DW-MMCCC and SW-MMCCC can be neglected. The DW-MMCCC can also utilize the distributed stray inductance to achieve ZCS for all the switches which is the same as the SW-MMCCC. Multiphase DW-MMCCC can also be implemented easily with reduced input current ripple and output current ripple which is more suitable to high current and high power application. A 4X-DW-MMCCC with conversion ratio equals to four is analyzed as an example for hard-switched DW-MMCCC. A 5X-ZCS-DW-MMCCC with conversion ratio equals to five is analyzed as an example for soft-switched DW-MMCCC. For 3X-DW-MMCCC, there are some special features, all the switch and capacitor voltage stress are the same, which is the low side voltage. A three-phase 3X-ZCS-DW-MMCCC is analyzed as an example for the interleaving operation. A three-phase 3X-DW-ZCS-MMCCC prototype is built and tested. Simulation and experimental results are provided to demonstrate the validity of the proposed circuit.

6.2 Proposed Circuit Topology

In this section, two different types of DW-MMCCC are proposed: NX DW-MMCCC and NX ZCS-DW-MMCCC. NX means the conversion ratio is equal to N. The NX DW-MMCCC is the basic DW-MMCCC topology with hard switching, which is similar to the traditional SW-MMCCC. The NX ZCS-DW-MMCCC can be considered as the improved topology of DW-

MMCCC by considering the distributed stray inductance in the circuit, ZCS of all the switches can be achieved, which is similar to the ZCS-SW-MMCCC.

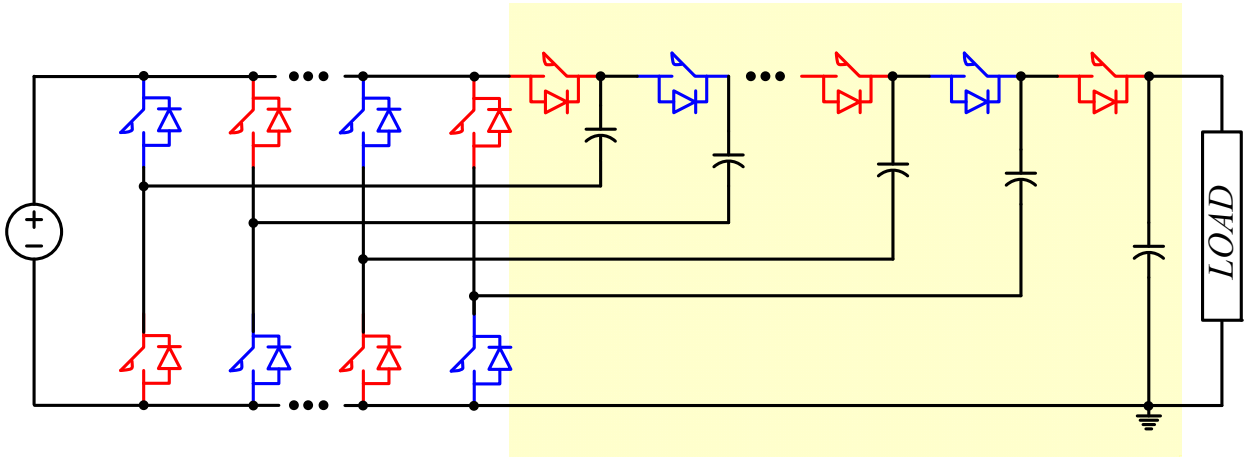


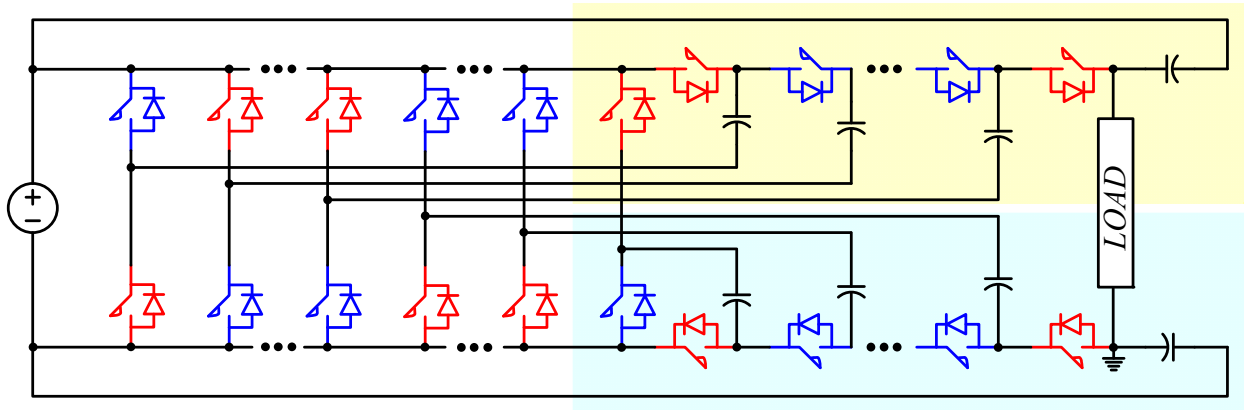
Figure 6.1 Single-wing (traditional) NX multilevel modular capacitor-clamped dc-dc converter (SW-MMCCC) main circuit structure.

6.2.1 NX DW-MMCCC

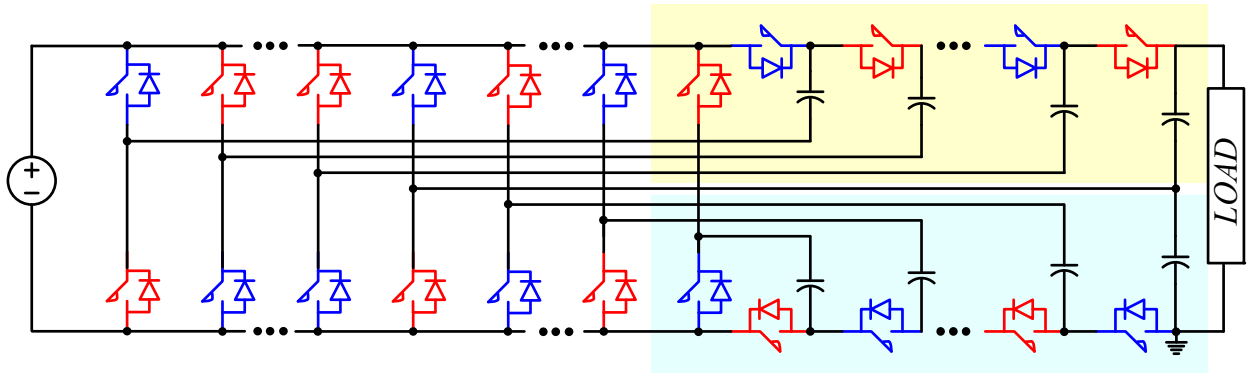
Figure 6.2 shows the proposed DW-MMCCC main circuit structure, when the conversion ratio equals to N. Figure 6.2(a) shows the DW-MMCCC when the conversion ratio is an odd number, with the conversion ratio N can be indicate as N=2n+1, n=1,2,3,…. Figure 6.2(b) shows the DW-MMCCC when the conversion ratio is an even number, with the conversion ratio N can be indicated as N=2n, n=1,2,3…. Different from the traditional SW-MMCCC with all the capacitors connected to the top rail of the switches, the capacitor and the switching devices of DW-MMCCC are separated symmetrically in two sides, with capacitors connected to both top rail and bottom rail of the switches.

Table 6.1 shows the comparison of the SW-MMCCC and proposed DW-MMCCC in terms of the voltage stress, current stress and total number of the capacitor and the switching device. From the table, the stress and device number of the proposed DW-MMCCC are nearly exactly

the same as the SW-MMCCC, but the capacitor voltage stress is reduced by half. The total capacitor voltage stress is defined as the sum of all the capacitor voltage stress. In Table 6.1, the switch voltage stress of DW-MMCCC is shown as Vin or 2Vin, but when the conversion ratio two or three, all the switching and capacitor voltage stress is only Vin which is different from SW-MMCCC. The average switch current stress of SW-MMCCC and DW-MMCCC are the same, which is the load current. The capacitor current stress of the SW-MMCCC and DW-MMCCC is also the same.



(a)



(b)

Figure 6.2. Proposed NX-DW-MMCCC main circuit. (a) Odd conversion ratio. (b) Even conversion ratio.

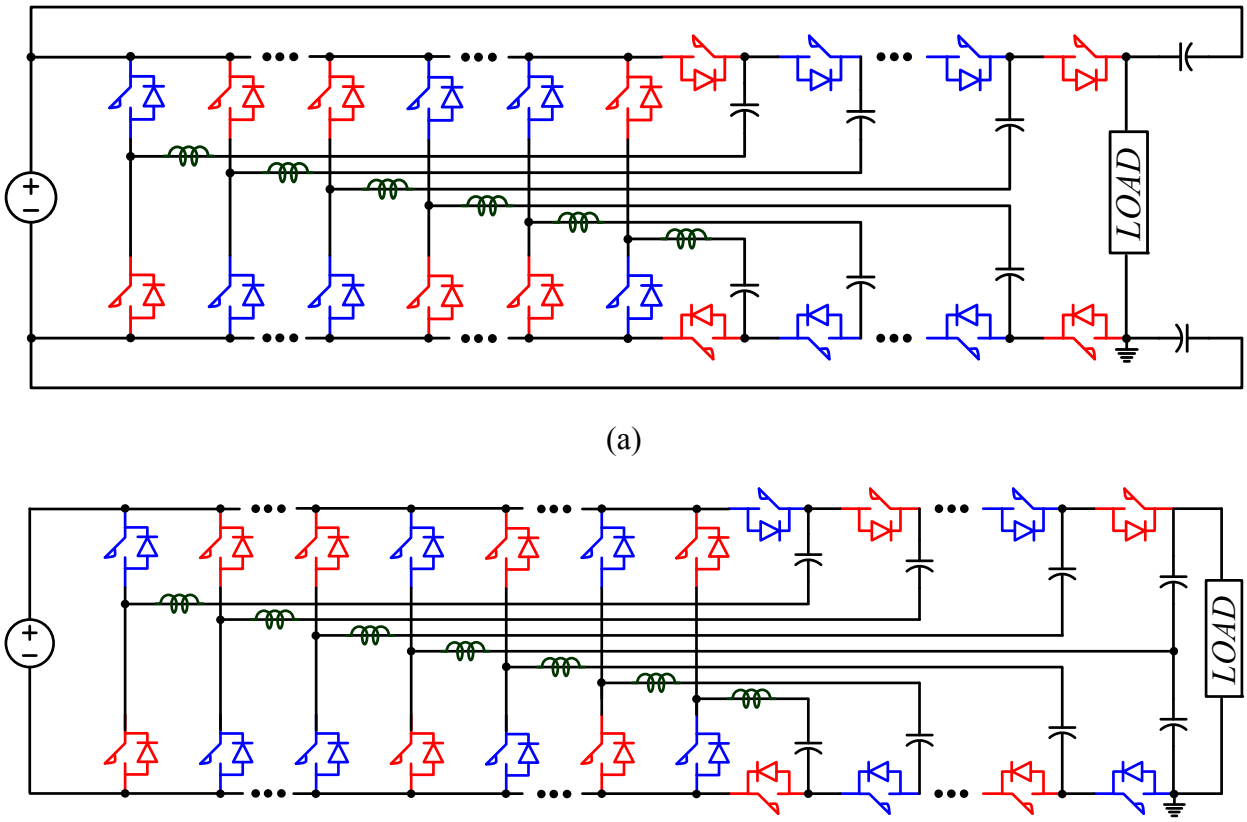
Table 6.1 Comparison of SW-MMCCC and DW-MMCCC

	Single wing MMCCC	Double wing MMCCC (even)	Double wing MMCCC (odd)
No. of Conversion Ratio	N	N (2n)	N (2n+1)
No. of capacitors	N	N	N+1
Peak capacitor voltage stress	NVin	NVin/2	(N-1)Vin/2
Total capacitor voltage stress	N(N+1)Vin/2	N(N+2)Vin/4	(N-1)(N+5)Vin/4
No. of switches	3N-2	3N-2	3N-1
Switch voltage stress N>3	Vin, 2Vin	Vin, 2Vin	Vin, 2Vin
Switch voltage stress 3>N>1	Vin, 2Vin	Vin	Vin
Switch average current stress	Io	Io	Io

6.2.2 NX ZCS-DW-MMCCC

Figure 6.3 shows the proposed NX ZCS-DW-MMCCC main circuit structure considering the distributed stray inductance, when the conversion ratio equals to N. Figure 6.3(a) shows the ZCS-DW-MMCCC when the conversion ratio is an odd number. Figure 6.3(b) shows the ZCS-DW-MMCCC when the conversion ratio is an even number. By considering the distributed stray inductance in the circuit, ZCS-DW-MMCCC can be achieved, which is similar to the ZCS-SW-MMCCC. The distributed stray inductance in the figure can be considered as the equivalent stray inductance in the loop. And it does not need to be in the position as shown in the figure. The capacitor size of ZCS-DW-MMCCC can also be reduced significantly compared to the DW-MMCCC. For the NX DW-MMCCC with odd conversion ratio, multi-phase interleaving operation could be implemented, and the input capacitor current becomes continuous. The input and the output capacitor current ripple, capacitor size, and output voltage ripple can be reduced

compared to the single-phase version. Multiphase ZCS-DW-MMCCC is especially suitable for high voltage gain, and high current automotive application. The power density and efficiency of multiphase ZCS-DW-MMCCC is higher than single-phase version.



(a)

(b)

Figure 6.3. NX ZCS-DW-MMCCC considering the stray inductance. (a) Odd conversion ratio, (b) even conversion ratio.

6.3 Operation Principles

In this section, the operation principle of proposed DW-MMCCC will be discussed. 4X-DW-MMCCC will be used as an example for the even conversion ratio hard switched DW-MMCCC operation analysis. 5X-ZCS-DW-MMCCC will be used as an example for the odd conversion ratio soft-switching DW-MMCCC operation analysis.

6.3.1 4X-DW-MMCCC

Figure 6.4 shows the 4X-DW-MMCCC main circuit structure when the conversion ratio is equal to four as an example for operation analysis. Similar to SW-MMCCC, the switching devices of DW-MMCCC are controlled complementarily with 50% duty cycle. Figure 6.5 shows the two switching states of 4X-DW-MMCCC. In the first switching state, the switches $S_{B1} \sim S_{B5}$ are conducted, the capacitor C1 is charged by the input voltage source Vin, and the capacitor C4 is charged by the input voltage source Vin and the capacitor C2 in series. C3 and C4 are connected in series to charge the load. In the second switching state, the switches $S_{T1} \sim S_{T5}$ are conducted, the capacitor C3 is charged by the input voltage source Vin and the capacitor C1 in series, the capacitor C2 is charged by the input voltage source, and the capacitor C3 and C4 are connected in series to charge the output load. In both switching states, one of the capacitors connected to the load is charged, which reduces the output capacitor voltage ripple.

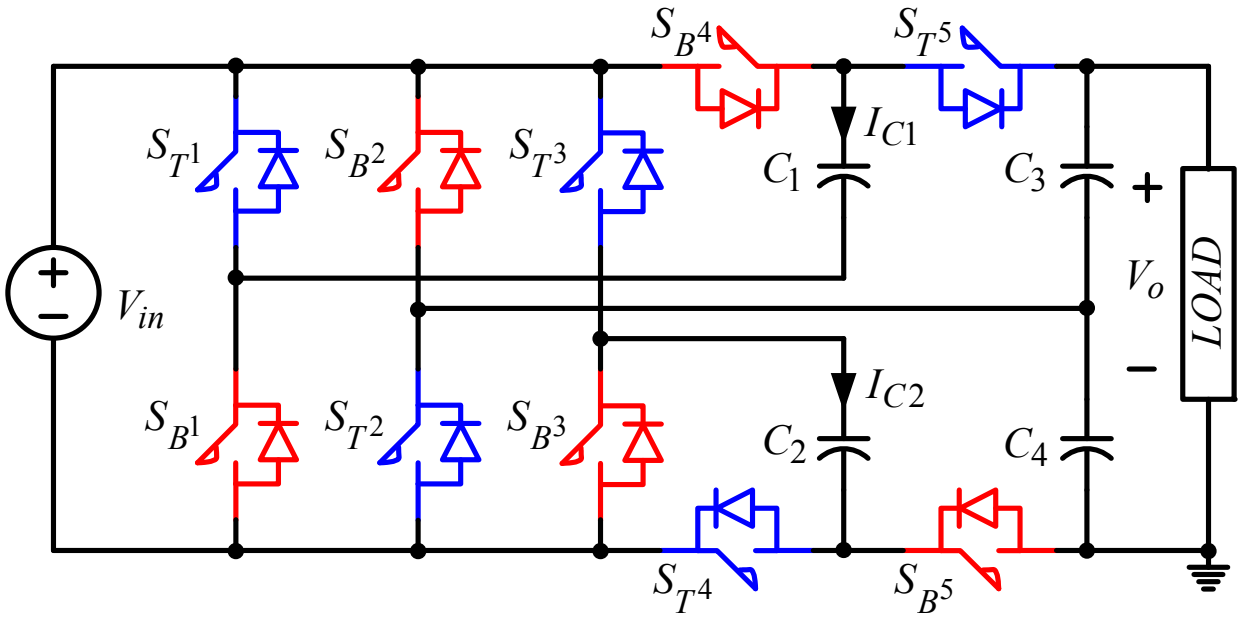
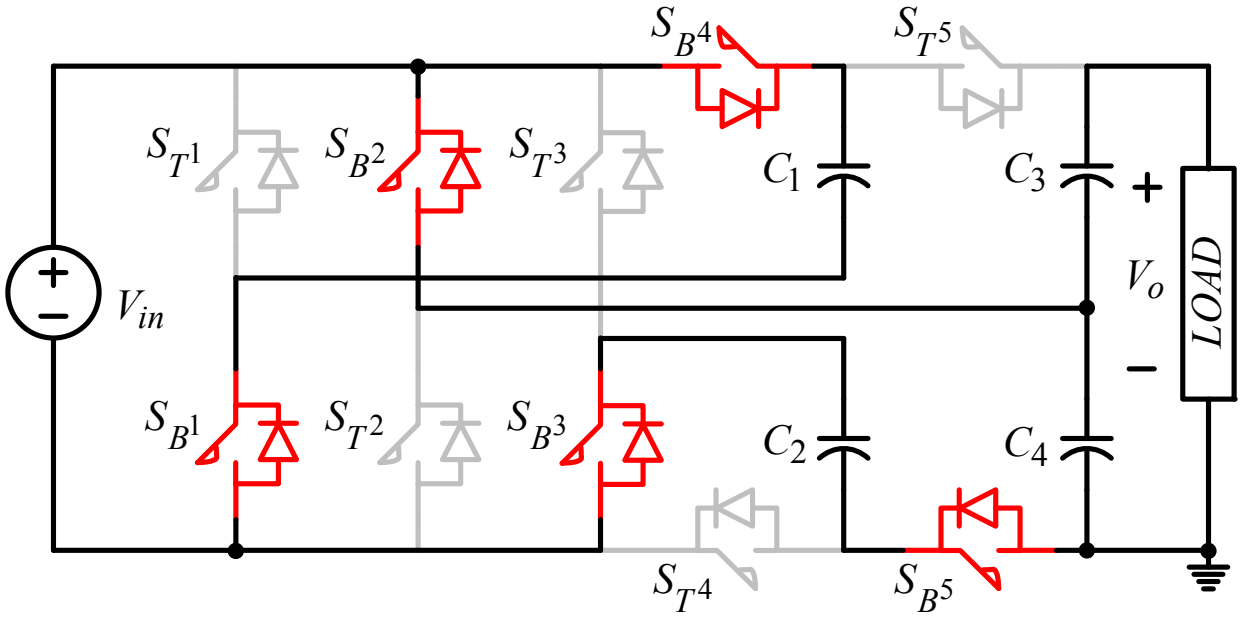
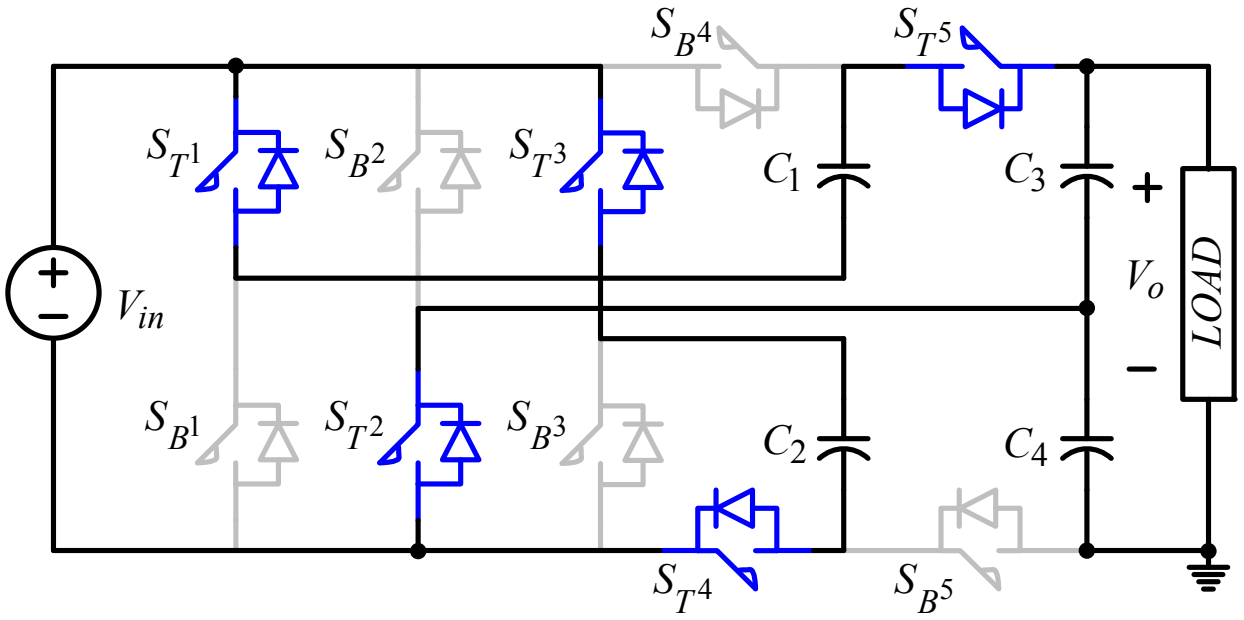


Figure 6.4. 4X-DW-MMCCC main circuit.



(a)



(b)

Figure 6.5. Two switching states of 4X-DW-MMCCC with different switches turned on.

Figure 6.6 shows the ideal waveforms of proposed 4X-DW-MMCCC under steady state conditions. The gate signal of switches S_B and S_T are $V_{GS}\_S_B$ and $V_{GS}\_S_T$, which are

complementary with 50% duty cycle. Assume all the capacitance is big enough, the stray inductance in the circuits is small enough, and the turn on resistance is small. The switch current can be considered as a quasi-square waveform as shown in $I_{D\_}S_B$ and $I_{D\_}S_T$ in Figure 6.6. I_{C1} and I_{C2} are the capacitor charging current, the reference direction has been marked in Figure 6.4. In either switching state, the capacitor charging current is the same with one of the switch current. Table 6.2 shows the detailed capacitor charging and discharging status in either switching states of DW-MMCCC. All the capacitors are utilized fully in two switching states, which means, it either charges other capacitors with input voltage source, or is charged by the input voltage source with other capacitors. The voltage stress of capacitor C1 and C2 are input voltage Vin, the voltage stress of capacitor C3 and C4 are 2Vin. The voltage stress of switches $S_{B1} \sim S_{B4}$, $S_{T1} \sim S_{T4}$ are Vin, the voltage stress of switches S_{B5} and S_{T5} are 2Vin.

Table 6.2 Switching Schemes (Steady State) of DW-MMCCC.

↓ = CHARGING, ↑ = DISCHARGING

Switching State I		Switching State II	
Capacitor charing path	On-state switch	Capacitor charging path	On-state switch
Vin ↑ → C1 ↓	SB1, SB4	Vin ↑ + C1 ↑→ C3 ↓	ST1, ST2, ST5
Vin ↑ + C2 ↑→ C4 ↓	SB2, SB3, SB5	Vin ↑ → C2 ↓	ST3, ST4

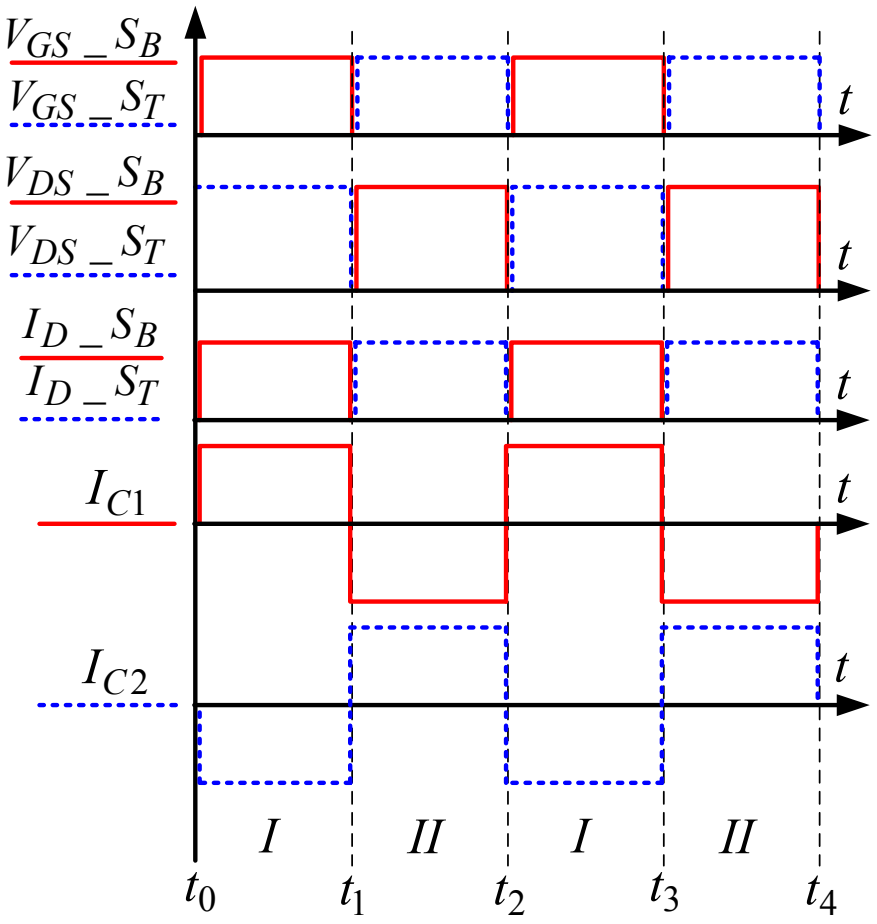


Figure 6.6. Ideal waveforms of 4X-DW-MMCCC.

6.3.2 5X-ZCS-DW-MMCCC

Figure 6.7 shows the main circuit configuration of 5X-ZCS-DW-MMCCC as an example for operation analysis. The conversion ratio of this circuit is equal to five. The switching devices are also controlled in a complementary manner with 50% duty cycle. Figure 6.8 shows the two switching states of 5X-ZCS-DW-MMCCC. Figure 6.9 and Figure 6.10 show the simplified equivalent circuits of two switching states. In the first switching state, as shown in Figure 6.9, the switches $S_{B1} \sim S_{B8}$ are conducted, capacitor C1 and C2 are charged by the input voltage source. The capacitor C5, C6 and the load are charged by the capacitor C3 and C4 respectively. The load can be considered charged by the input voltage source Vin, capacitor C5 and C6 in series. In the

second switching state, as shown in Figure 6.10, the switches $S_{T1} \sim S_{T6}$ are conducted, the capacitor C3 is charged by the input voltage source Vin and the capacitor C1 in series. The capacitor C4 is charged by the input voltage source Vin and the capacitor C2 in series. The load is charged by the capacitor C5, C6 and input voltage source Vin in series. $L_{S1} \sim L_{S4}$ can be considered as the equivalent stray inductance in each loop. And in the real circuit, the stray inductance is distributed in the circuit, it doesn't need to appear at the position as shown in Figure 6.7. By proper design, the stray inductance in each loop can be designed the same, and ZCS can be easily achieved by using the same capacitance value. The output voltage ripple of odd conversion ratio DW-MMCCC is higher than the even conversion ratio DW-MMCCC, since there are no current cancelling effect on the output side. But the multiphase odd conversion ratio DW-MMCCC can reduce both the input capacitor and output capacitor current and voltage ripple by interleaving operation. The converter power rating, efficiency and power density can be increased significantly by using multiphase DW-MMCCC.

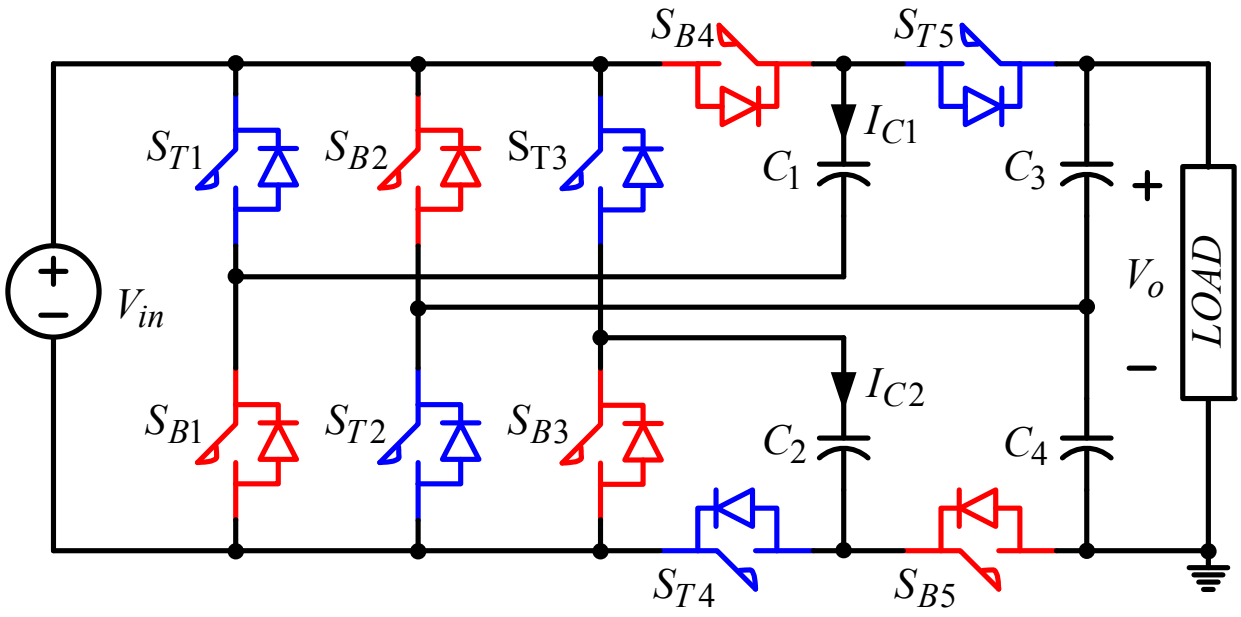
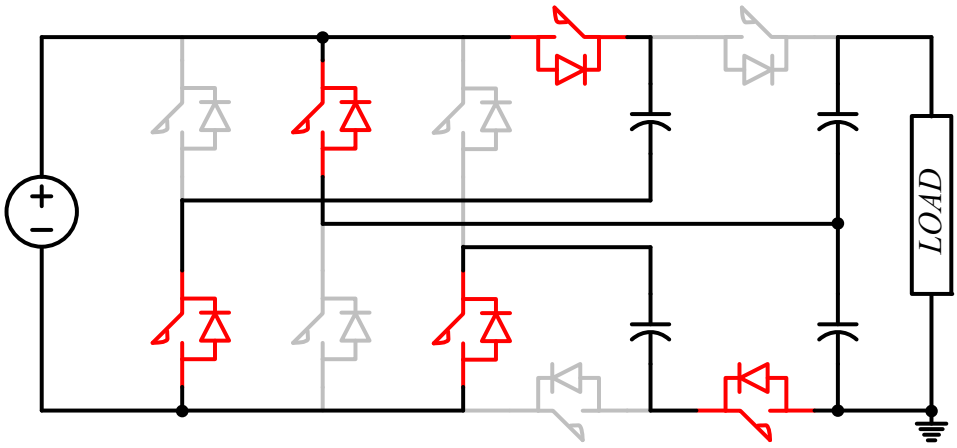
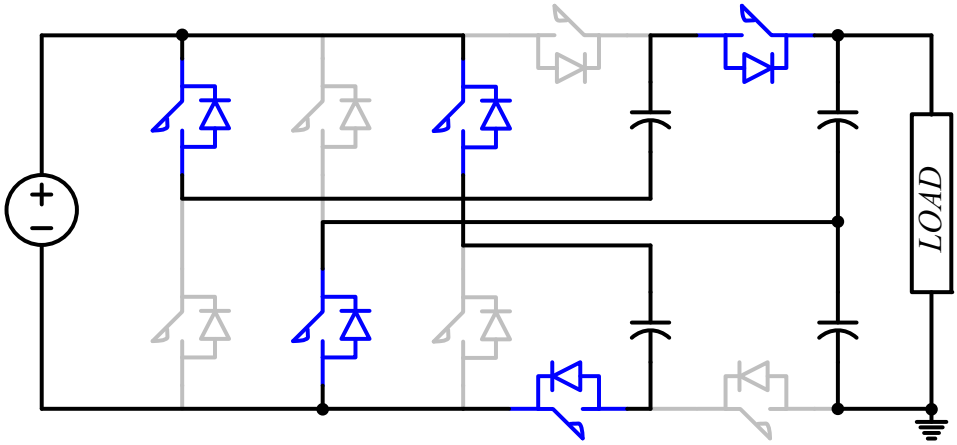


Figure 6.7. 5X-ZCS-DW-MMCCC main circuit.



(a)



(b)

Figure 6.8. Two switching states of 5X-ZCS-DW-MMCCC with different switches turned on.

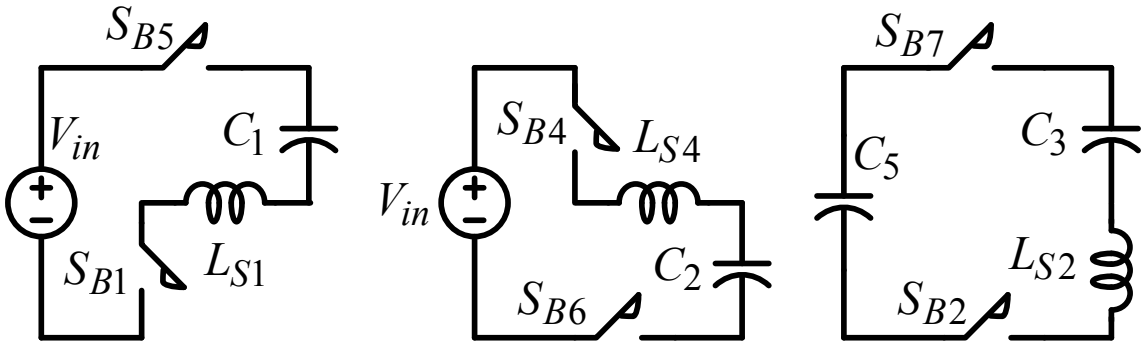


Figure 6.9. Simplified equivalent circuits of state I with switches S_B are turned on.

Figure 6.9 cont'd

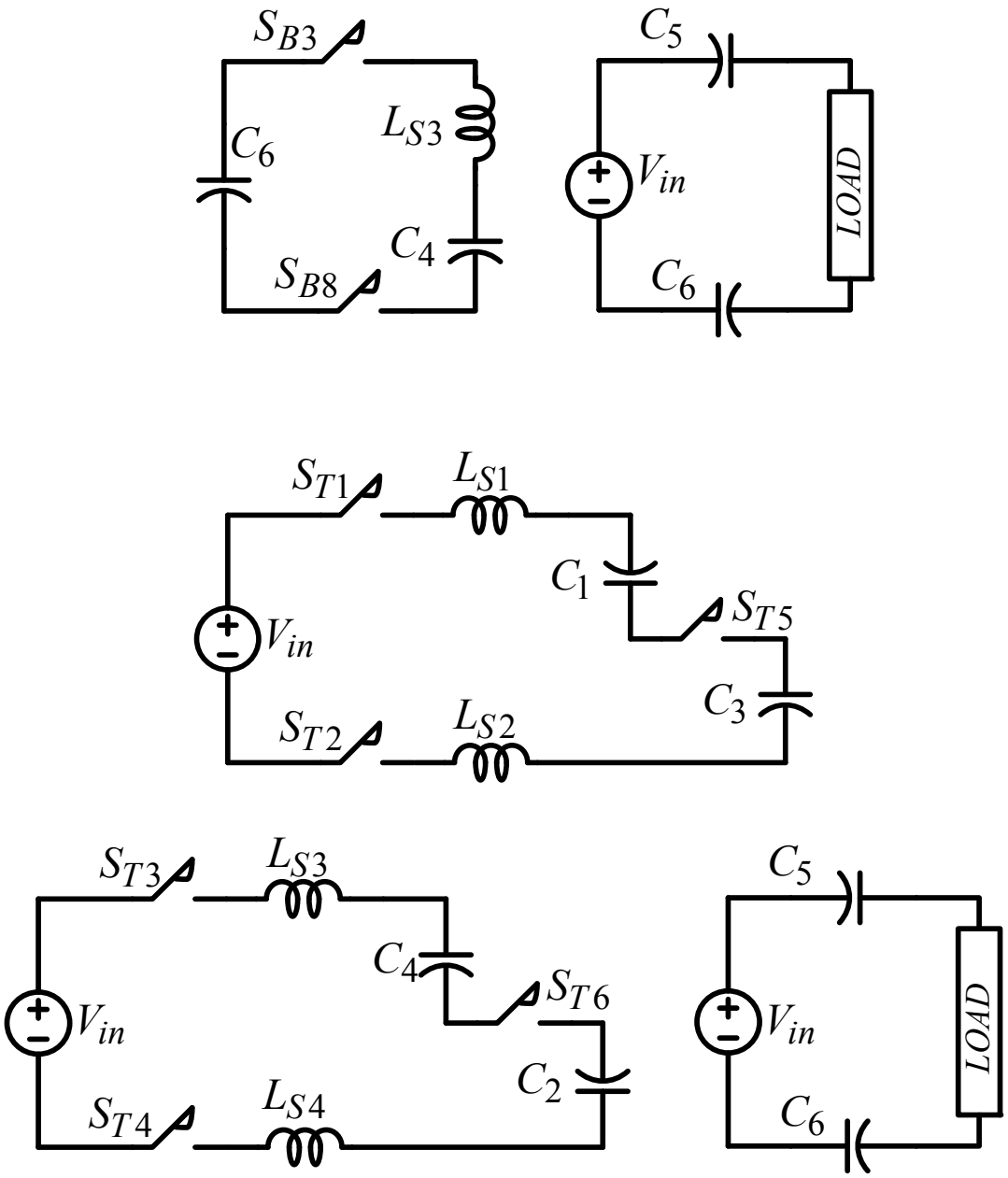


Figure 6.10. Simplified equivalent circuits of state II with switches S_T are turned on.

Figure 6.11 shows the ideal waveforms of 5X-ZCS-DW-MMCCC under steady state conditions. The gate signal of switches S_B and S_T are $V_{GS\_}S_B$ and $V_{GS\_}S_T$, which are complementary with 50% duty cycle. By consideration the distributed stray inductance in the circuit, ZCS for all the switches can be achieved by setting the switching frequency equal to the

resonant frequency. The switch current will be half sinusoid waveform as shown in $I_{D\_}S_B$ and $I_{D\_}S_T$ in Figure 6.11. I_{C1} and I_{C2} are the capacitor charging current, which is a sinusoid waveform, the reference direction has been marked in Figure 6.7. In either switching state, the capacitor charging current is the same with one of the switch current. The input current *Iin* of ZCS-DW-MMCCC is rectified sinusoid waveform with a load current offset, as shown in Figure 6.11. Because of the high input current ripple, the input capacitor current stress is relatively high for single-phase ZCS-DW-MMCCC. By using multiphase ZCS-DW-MMCCC as discussed in the next section, the input current ripple can be reduced significantly. Table 6.3 shows the detailed capacitor charging and discharging status in either switching states of ZCS-DW-MMCCC. All the capacitors are utilized fully in two switching states, which means, it either charges other capacitors with input voltage source, or is charged by the input voltage source with other capacitors. The voltage stress of capacitor C1 and C2 are input voltage Vin, the voltage stress of capacitor C3, C4 C5, C6 are 2Vin. The voltage stress of switches $S_{B1} \sim S_{B6}$, $S_{T1} \sim S_{T4}$ are Vin, the voltage stress of switches $S_{B7} \sim S_{B8}$, $S_{T5} \sim S_{T6}$ are 2Vin.

Table 6.3 Switching Schemes (Steady State) of ZCS DW-MMCCC.

↓= CHARGING, ↑ = DISCHARGING

Switching State I		Switching State II	
Capacitor charing path	On-state switch	Capacitor charging path	On-state switch
Vin ↑ → C1 ↓	SB1, SB5	Vin ↑ + C1 ↑→ C3 ↓	ST1, ST2, ST5
Vin ↑ → C2 ↓	SB4, SB6	Vin ↑ + C2 ↑→ C4 ↓	ST3, ST4, ST6
C3 ↑ → C5 ↓ C4 ↑ → C6 ↓ Vin ↑ + C5 ↑ + C6 ↑ → Load ↓	SB2, SB3, SB7, SB8	Vin ↑ + C5 ↑ + C6 ↑ → Load ↓	

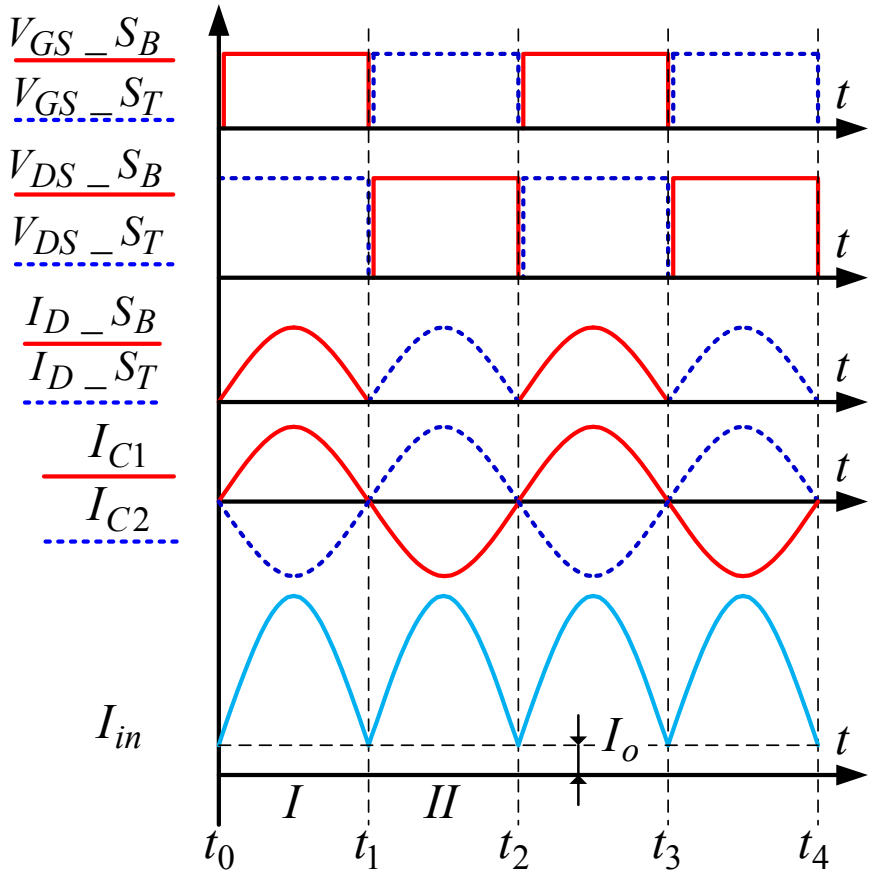


Figure 6.11. Ideal waveforms of 5X-ZCS-DW-MMCCC.

6.4 Multiphase DW-MMCCC

For the DW-MMCCC with odd conversion ratio, the multiphase interleaving operation is easily to be achieved. Figure 6.12 shows the three-phase 3X ZCS-DW-MMCCC main circuit structure as an example for the operation analysis. Figure 6.13 shows the ideal waveform for three-phase 3X-ZCS-DW-MMCCC. $V_{GS\_S_{AB}}$ and $V_{GS\_S_{AT}}$ are the gate signals of the switching devices in phase A. $V_{GS\_S_{BB}}$, $V_{GS\_S_{BT}}$, $V_{GS\_S_{CB}}$ and $V_{GS\_S_{CT}}$ are the gate signals of the devices in phase B and phase C. Each phase is operated 120 degrees phase shift from each other. And two different gate signals in each phase are complementary with 50% duty cycle. $I_{D\_S_{AB}}$, $I_{D\_S_{AT}}$, $I_{D\_S_{BB}}$, $I_{D\_S_{BT}}$, $I_{D\_S_{CB}}$, and $I_{D\_S_{CT}}$ are the drain-source

currents of each switching device. All the switch currents can achieve zero current switching with half sinusoid waveforms. I_L_{AS}, I_L_{BS} and I_L_{CS} are the currents through the stray inductance L_{AS}, L_{BS} and L_{CS}. And the stray inductance currents are sinusoid waveforms. I_{in} is the input current with 6ω current ripple which is continuous. And the input current ripple becomes 8.9% compared to the single-phase version which is similar to the case mentioned in [161]. So input the capacitor power loss can be reduced to 0.8% compared to the single-phase version. By using multiphase DW-MMCCC high-power high-current and high power density multilevel dc-dc converter can be built.

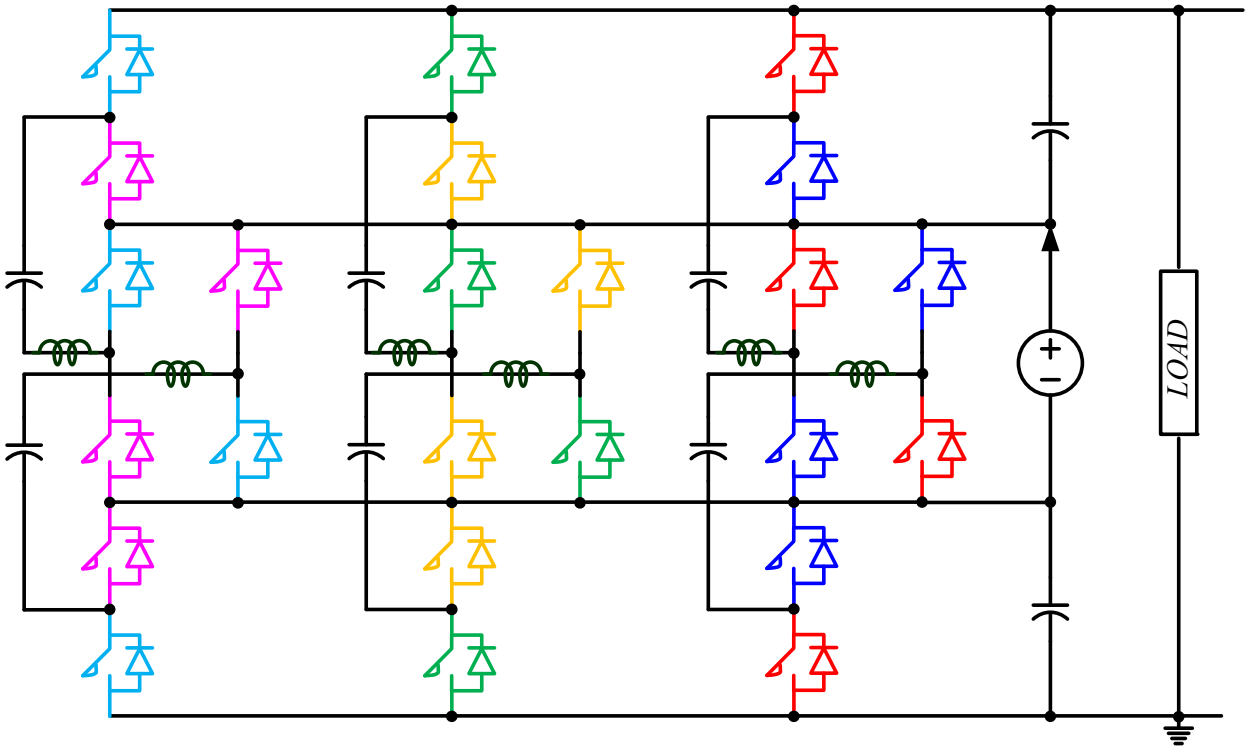


Figure 6.12. 3-phase 3X-ZCS-DW-MMCCC main circuit.

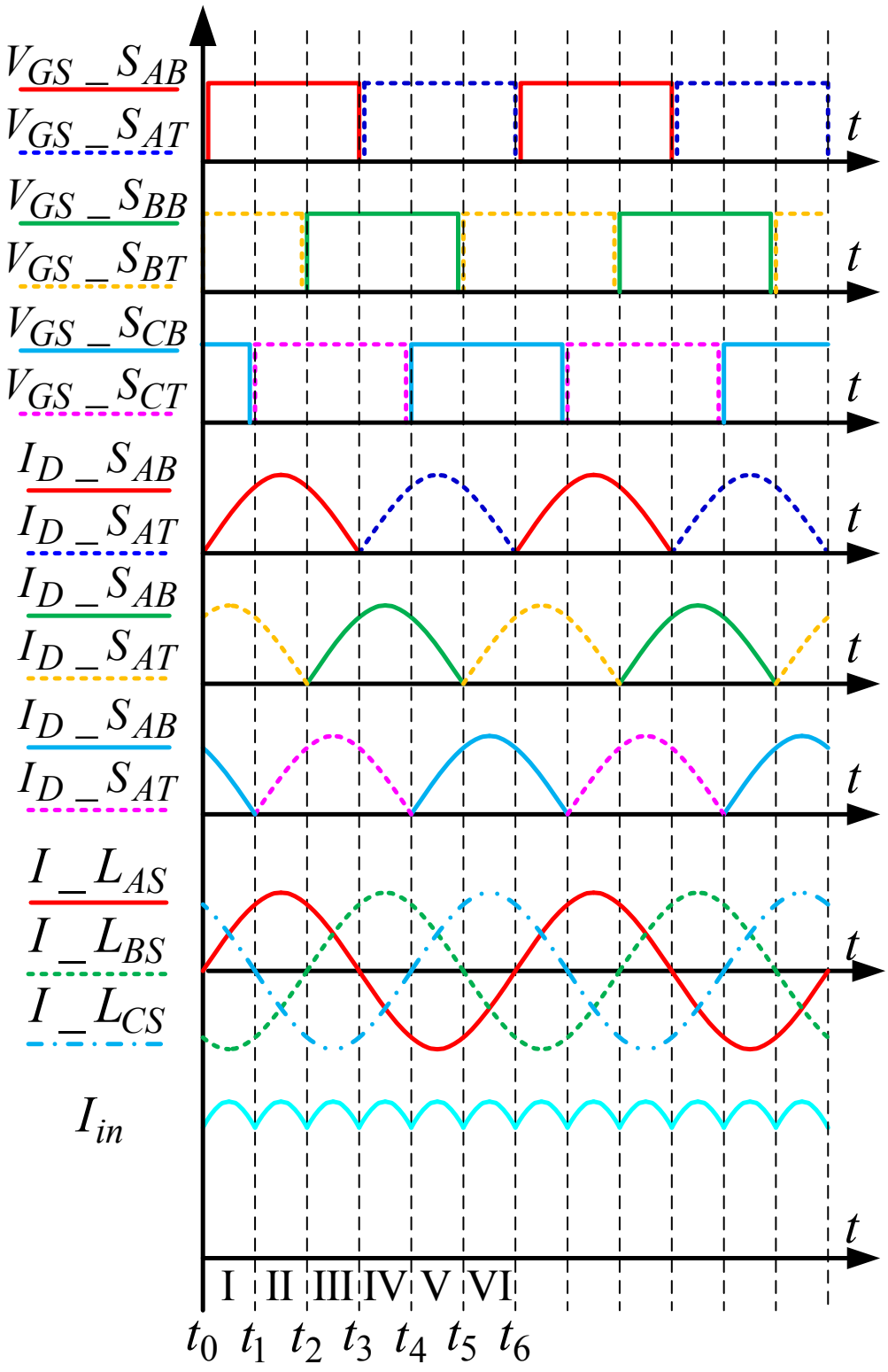


Figure 6.13. Ideal waveforms of 3-phase 3X-ZCS-DW-MMCCC.

6.5 Design Considerations

The design of DW-MMCCC should be divided into two cases: the hard switching case and the soft switching case. By using low switching frequency, high capacitance capacitor and minimized stray inductance in the circuit. The DW-MMCCC can be designed in hard switching case with high efficiency. The switch current of the DW-MMCCC in hard switching case is quasi-square with minimized the conduction loss and gate drive loss. Since the switching frequency of DW-MMCCC in hard switching case is not high, the switching loss is acceptable. The DW-MMCCC can also be designed in soft-switching case with ZCS for all the switches as mentioned previously. The conduction loss of ZCS-DW-MMCCC is about 11% higher than the DW-MMCCC in hard switching case. Since the switching loss can be eliminated in soft-switching case, the switching frequency can be increased, small capacitance multilayer ceramic capacitors can be utilized to resonate with the stray inductance existed in the circuit. The capacitor size in soft-switching case can be reduced significantly. With increased switching frequency, the gate drive loss of soft-switching case would be higher than the hard switching case, but considering the reduced switching loss, the ZCS-DW-MMCCC can be designed with almost the same efficiency and reduced capacitor size. In high power applications, the DW-MMCCC designed with soft-switching is preferred for high efficiency and high power density. In order to utilize the stray inductance to resonate with the capacitor and achieve ZCS for all the switches, the circuit layout must be carefully designed. Some of the stray inductance in the circuit should be minimized, while the stray inductance in other placed can be designed higher. Or even air core inductance can be inserted in some of the places in the circuit, in case the stray inductance is not large enough for resonant. The stray inductance as shown in Figure 6.12 can be considered as a good place to insert air core inductance.

6.6 Simulation and Experiment Results

Figure 6.14 shows the simulation results of a 500 W 14 V input voltage, 42 V output voltage, 3-phase 3X DW-ZCS-MMCCC. It can be derived from the figure that the input current waveform is continuous as expected. And all the switch reach zero current switching. And the current of the stray inductance are all sinusoid.

A 100 W 10 V input 30 V output, 3-phase 3X DW-ZCS-MMCCC has been built, and the experimental waveforms are shown in Figure 6.15 ~ Figure 6.17. The switching devices are the MOSFETs IPB009N03L from infineon. The resonant capacitor is about 75.2 μF using sixteen multilayer ceramic capacitors C5750X7R2A475K from TDK in parallel. The stray inductance is about 200 nH. The switching frequency is about 40 kHz. Figure 6.15 shows the gate drive waveforms of the prototype. Figure 6.15(a) shows the gate drive signals of three phases with 120 degrees phase-shift from each other. Figure 6.15(b) shows the complementary gate drive signal of one-phase. Figure 6.16 shows the switching device S_{AB4} gate drive voltage $V_{GS\_}S_{AB}$, the switching device S_{AB4} drain source voltage $V_{DS\_}S_{AB}$, and the current I_L_{AS} through stray inductance current L_{AS2}. The other switch voltage and stray inductance current are similar to the waveforms as shown in Figure 6.16, so they are not listed here. The stray inductance current is a sinusoid waveform as expected, which means the switch current would be a half sinusoid waveform. All the switching devices achieve zero current switching. There are a little discontinuous during each switching transition of the stray inductance current. This is caused by the deadtime of the switching devices, with proper design and minimized deadtime, this transition discontinuous current can be minimized. Figure 6.17 shows the input voltage and output voltage with the stray inductance current waveforms. The input voltage is 10 V, and the output voltage is 30 V as expected.

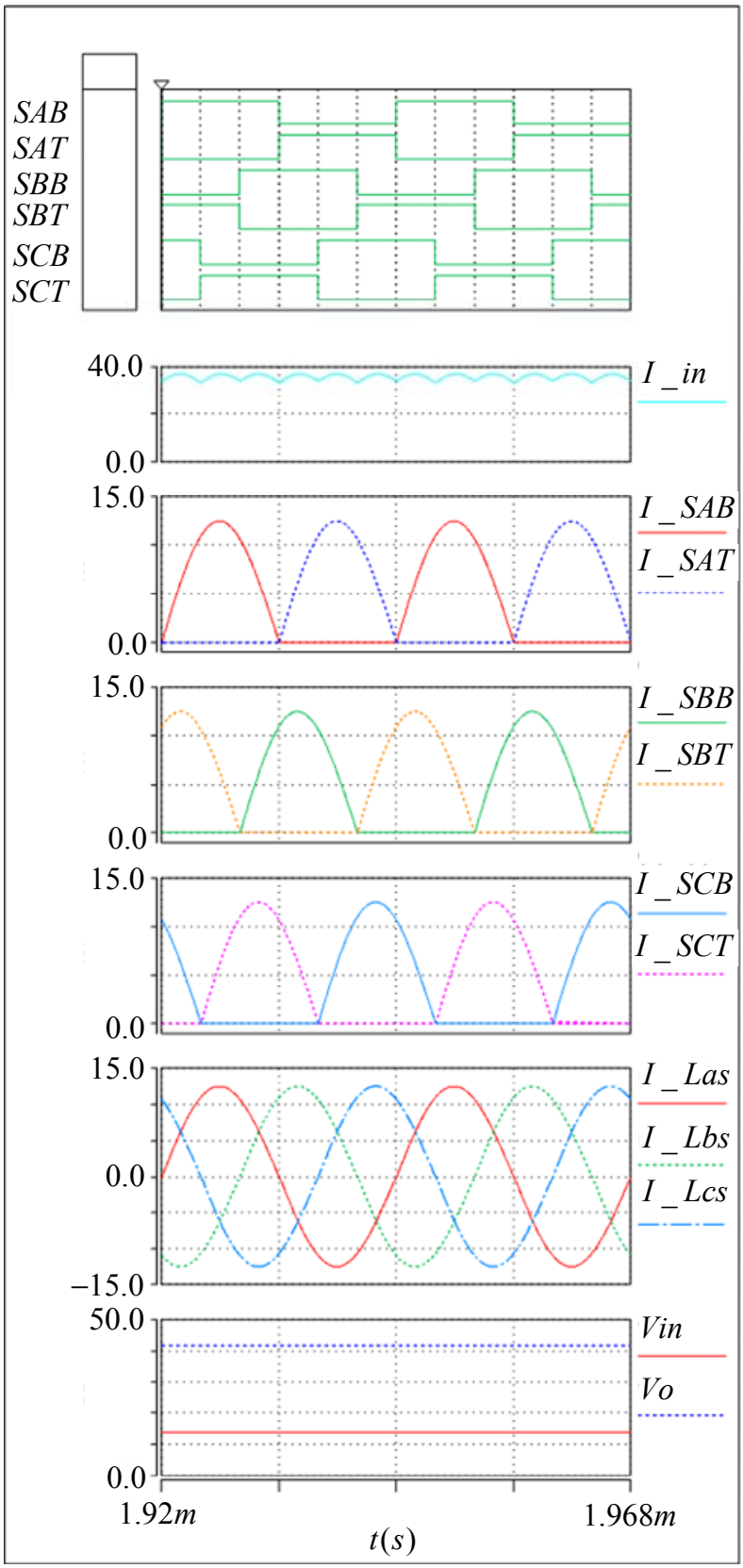
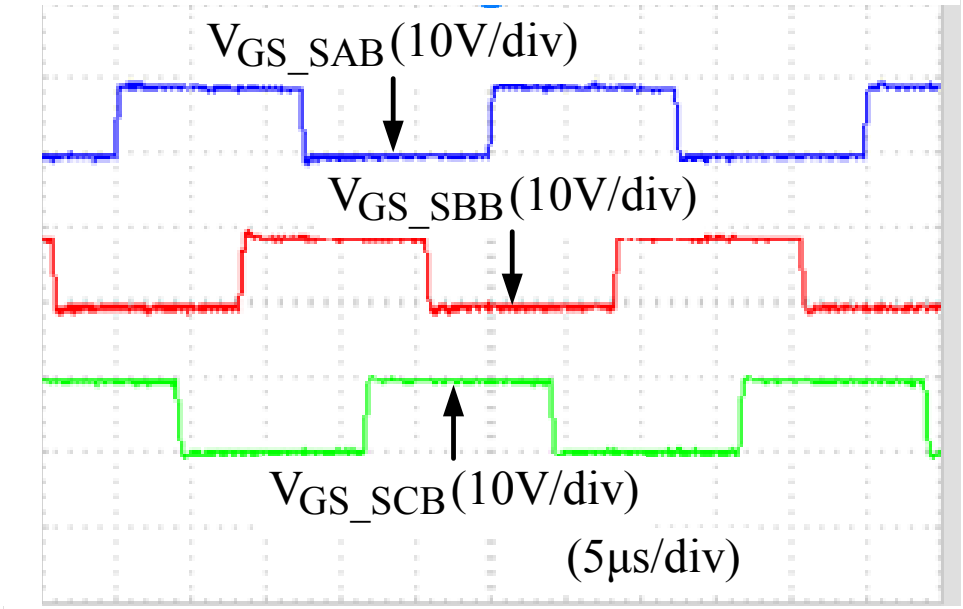
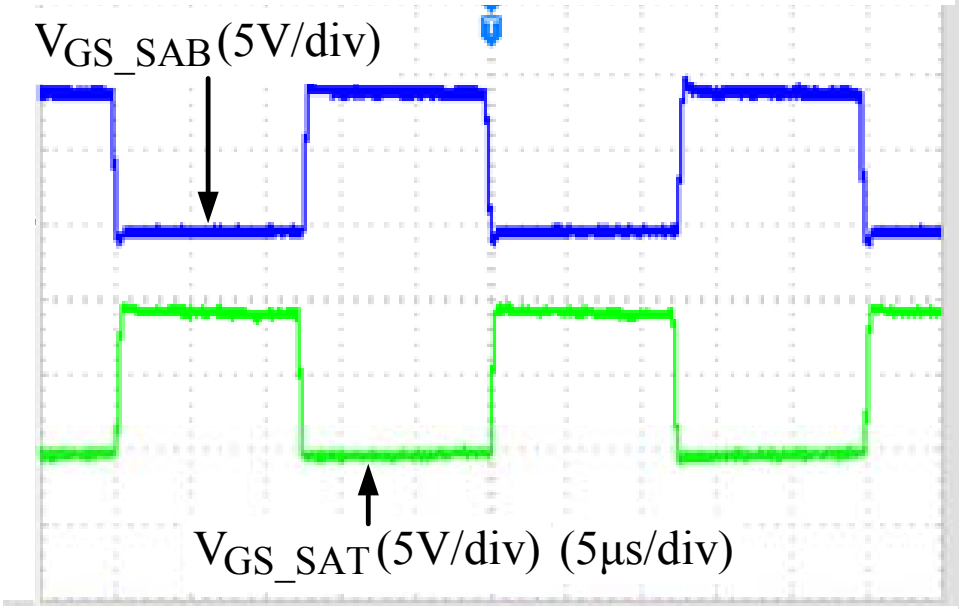


Figure 6.14. Simulation results of 500W 3-Phase 3X-ZCS-DW-MMCCC.





(a) (b)

Figure 6.15. Gate drive waveforms of 500 W 14 V ~ 42 V 3-phase 3X-DW-MMCCC.

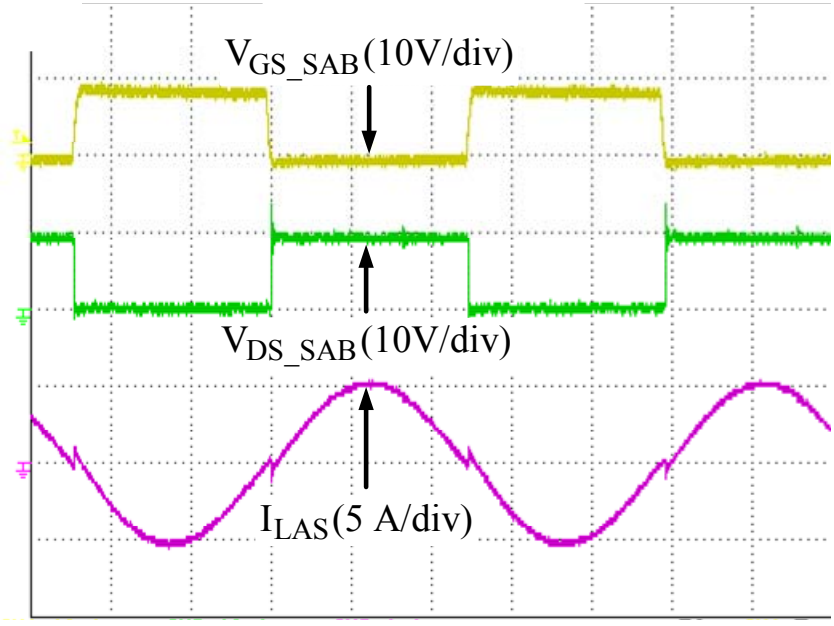


Figure 6.16. Switching device voltage and stray inductance current waveform.

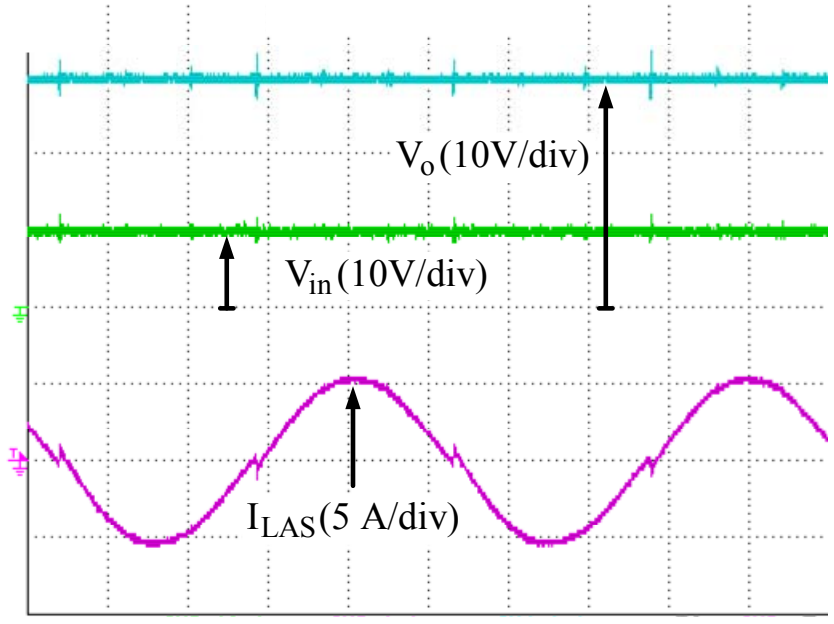


Figure 6.17. Input and output voltage and stray inductance current waveform.

6.7 Conclusion

This chapter presents a DW-MMCCC with zero current switching and interleaving capability. The proposed DW-MMCCC has high voltage gain with low switch voltage stress and low switch current stress features similar to the SW-MMCCC. Compared to traditional SW-MMCCC, the capacitor voltage stress of the proposed DW-MMCCC is reduced by half. The DW-MMCCC input and output does not share the same ground as SW-MMCCC does, which is not an issue for the automotive application. By utilizing the stray inductance properly, the ZCS-DW-MMCCC can be achieved, which means the multilayer ceramic capacitor can be utilized to achieve high efficiency with reduced size. Compared to the traditional 3X multilevel dc-dc converter, the proposed 3-phase 3X-ZCS-DW-MMCCC can also achieve high efficiency, with ten times increased power density. By using the proposed DW-MMCCC, high power, high efficiency, and high power density dc-dc converter can be built.

CHAPTER 7
Zero Voltage Switching Double-Wing Multilevel Modular Switched-Capacitor DC-DC Converter with Voltage Regulation

This chapter presents a phase-shift control method for double-wing multilevel modular switched-capacitor dc-dc converter (DW-MMCCC) to achieve output voltage regulation and zero voltage switching features. By utilizing the circuit stray inductance, and the proposed phase-shift control method, the output voltage of DW-MMCCC can be controlled without sacrificing efficiency significantly. The DW-MMCCCs with odd conversion ratio and even conversion ratio are analyzed separately. Simulation and experiments results are provided to demonstrate the validity of the proposed method. A 500 W prototype is being built and tested...[7]

7.1 Introduction

Since 1970s, switched-capacitor dc-dc converter has been investigated due to its small size, light weight, high efficiency, low EMI and easily integrated features [76, 90, 101, 111, 162, 163]. However, for most of the switched-capacitor dc-dc converters, only fixed voltage gain can be achieved due to the topology structure. The voltage regulation problem of switched-capacitor dc-dc converter becomes a major challenge that limits its application. Many methods have been investigated in the literature to achieve voltage regulation with different circuits [91, 147, 164-173]. The application area of the above mentioned literature is in low power (less than 20W) conversion area, where efficiency can be sacrificed to achieve fine voltage regulation.

[7] This work has been submitted to Applied Power Electronics Conference and Exposition (APEC), 2013

Recently, the multilevel magnetic-less dc-dc converter (switched-capacitor dc-dc converter) has been applied to automotive applications due its small size and high operated temperature features [82, 94-96, 138, 151, 152, 159]. High power (up to 55 kW) and high efficiency (up to 99%) multilevel dc-dc converters have been built and tested. However, these traditional multilevel dc-dc converters may have difficulty to achieve high efficiency with high voltage conversion ratio, and they also cannot achieve fine voltage regulation, only different step voltages can be generated [138, 151, 152]. In order to achieve high conversion ratio with high efficiency, a multilevel modular switched-capacitor dc-dc converter (MMCCC) has been proposed [78-80, 98-100, 130-132, 153]. And by utilizing the stray inductance in the circuit, the zero current switching (ZCS) MMCCC can be achieved with higher efficiency and smaller size [133-135, 154, 161, 174]. A double-wing (DW) MMCCC has been proposed recently with reduced capacitor voltage stress than the traditional MMCCC. By considering the circuit stray inductance, a ZCS-DW-MMCCC can also be achieved with high efficiency and small capacitor size. But the fine voltage regulation is still not achieved for these converters. A switched-capacitor based resonant converter with phase-shift control has been proposed recently [175, 176]. By using the phase-shift control, a fine output voltage regulation with high efficiency can be achieved for the proposed resonant converter.

This chapter presents a phase-shift control method for the DW-MMCCC to achieve output voltage regulation and zero voltage switching. For the traditional control method for DW-MMCCC, the switching devices are controlled complementarily with 50% duty cycle. By using the proposed phase-shift control method, the switching devices are divided into two groups. The devices in each group are controlled complementarily with 50% duty cycle; the phase-shift angle between the two groups can be used to control the output voltage. There are some differences

between the DW-MMCCC with odd conversion ratio and even conversion ratio, so they are analyzed separately using two examples 3X-DW-MMCCC and 4X-DW-MMCCC. The stray inductance in the circuit can be utilized and controlled as a current source to charge the output capacitor. The zero voltage switching (ZVS) of the switches can be achieved by utilizing the energy stored in the stray inductance by selecting proper dead-time and the device output capacitance. The close loop control block diagram with carefully calculated feed-forward is proposed and discussed. The simulation results are provided to demonstrate the validity and features of the proposed circuit. A 500 W prototype is being built, experimental results are provided.

7.2 Proposed Circuit Description and Basic Operation Principles

Figure 7.1 shows the NX-DW-MMCCC with odd conversion ratio, the conversion ratio is up to N where N equals 2n+1 (n is natural number). Figure 7.2 shows the NX-DW-MMCCC with even conversion ratio, the conversion ratio is up to N, where N equals 2n. The parasitic inductance has been draw in the figure. These parasitic inductance can be considered as carefully designed PCB trace or air core inductor. Figure 7.3 shows the 3X-DW-MMCCC main circuit structure. Without using phase-shift control, this circuit can step up or step down three times of the input voltage. By using proposed-phase shift control, this circuit can step down the input voltage to (1/6 ~ 1/2) with high efficiency or step up the input voltage from (2 ~6 times). Since the operation of step down and step up is similar, only the step down case is analyzed without losing generosity. Figure 7.4 shows the ideal waveforms of the 3X-DW-MMCCC with phase-shift control. There are four different modes.

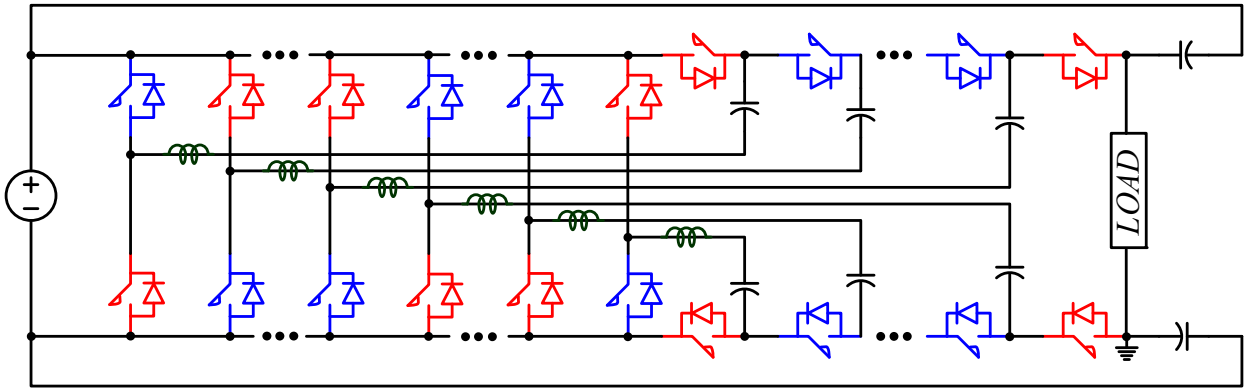


Figure 7.1 NX Double-wing multilevel modular switched-capacitor dc-dc converter with odd conversion ratio

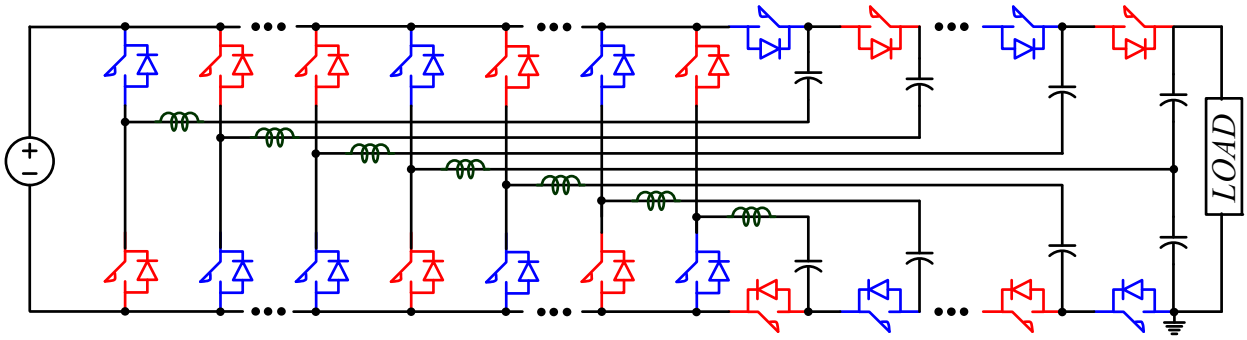


Figure 7.2 NX-Double-wing multilevel modular switched-capacitor dc-dc converter with even conversion ratio

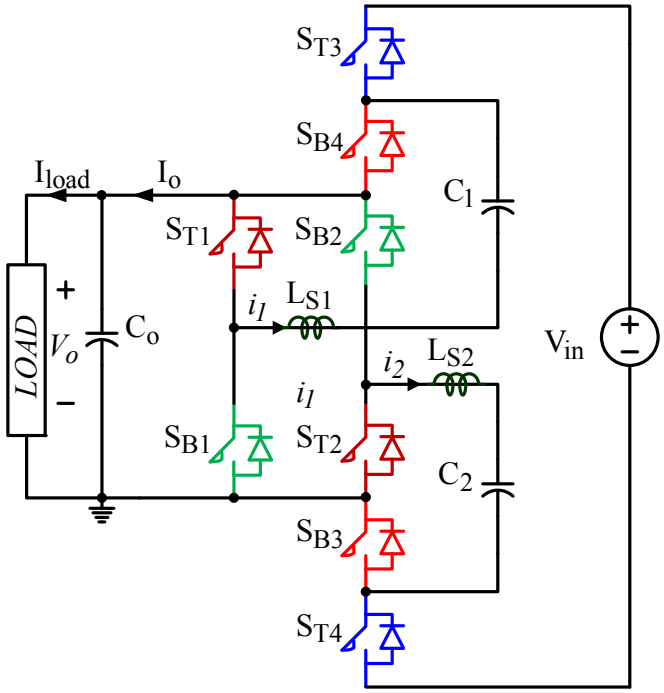


Figure 7.3 3X-DW-MMCCC main circuit structure.

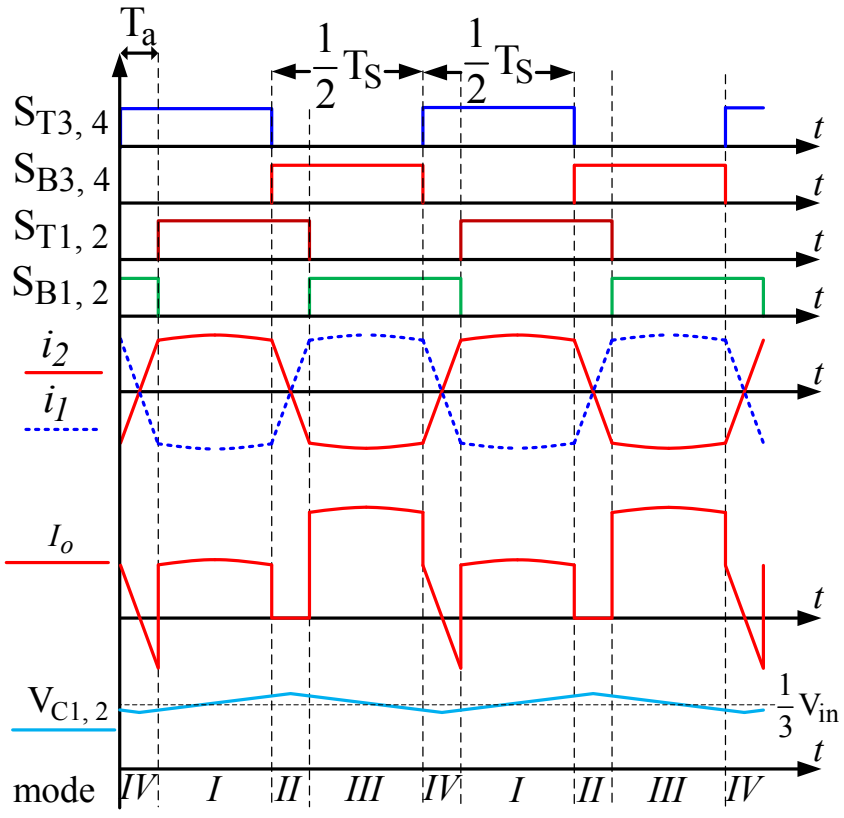
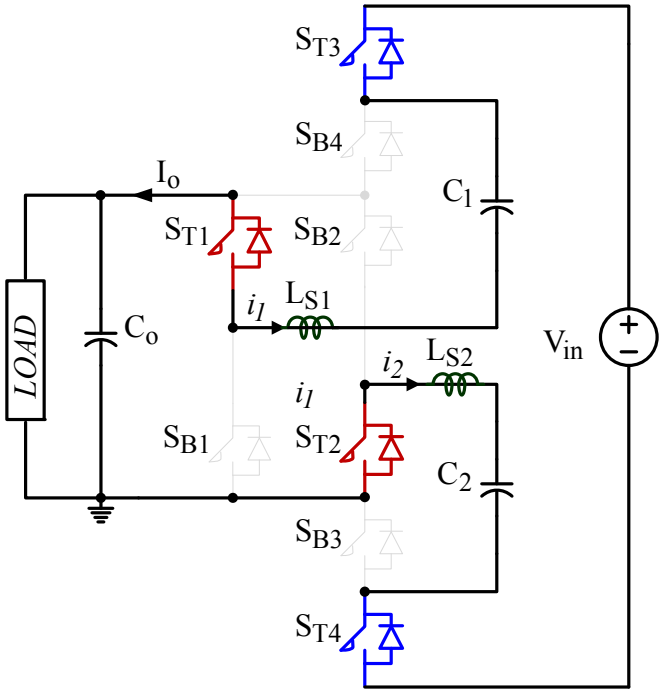
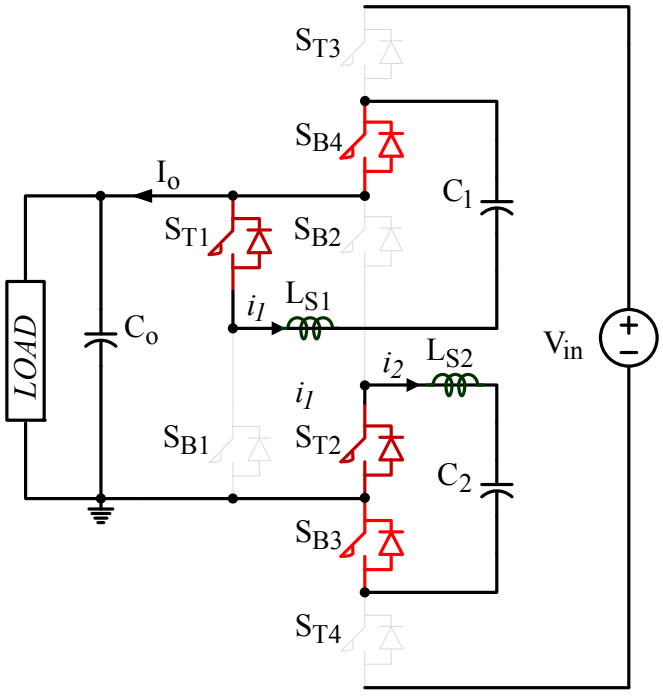


Figure 7.4 Ideal waveforms of 3X-DW-MMCCC with phase-shift control.



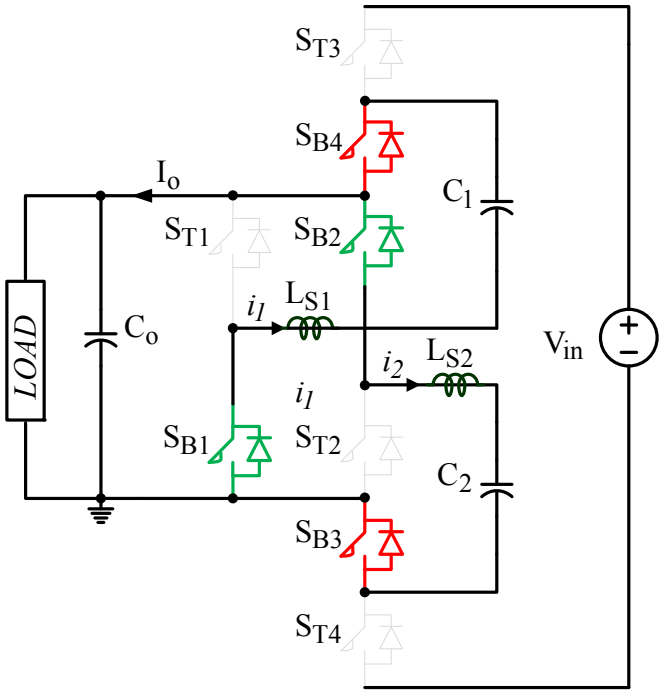
(a)



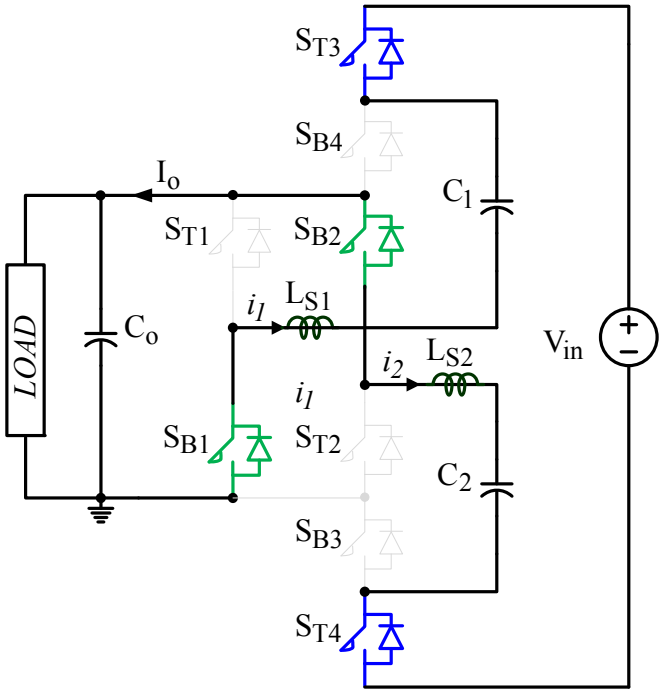
(b)

Figure 7.5 Equivalent circuits in each operation modes of the 3X-DW-MMCCC with phase-shift control.

Figure 7.5 cont'd



(c)



(d)

$S_{T3,4}$, $S_{T1,2}$, $S_{B3,4}$, $S_{B1,2}$ are the gate drive control signals of the switches $S_{T1} \sim S_{T4}$, $S_{B1} \sim S_{B4}$ respectively. From the figure, we can derive that, the control signal of i_1 and i_2 are the current of the stray inductance, the current reference direction is mark in the Figure 7.3. Figure 7.5 shows four different equivalent circuit in each operation modes of 3X-DW-MMCCC with phase-shift control. The mode I as shown in Figure 7.5(a) is the same with one of the traditional operation mode, the energy is transferred from the input to the output through the three capacitors in series. During this mode, all the capacitors are charged by the input voltage source. Figure 7.5(b) is the new operation mode, during this mode, the current circulating in the small loop L_{S1} and C_1 or L_{S2} and C_2. During this mode, the stray inductor current i_1 and i_2 change the direction. Figure 7.5(c) is also the same with one of the traditional operation mode, the energy is transferred from the two capacitors C_1 and C_2 to the load. Figure 7.5(d) is the new operation mode, during this mode, the current circulating in a bigger current loop. And the stray inductor current also change the direction. Figure 7.6 shows the 4X-DW-MMCCC main circuit structure with the conversion ratio equals to four. Although the structure of the even conversion ratio DW-MMCCC is slightly different with the odd conversion ratio DW-MMCCC, the phase-shift control method is the same. All the switching devices connected between the low voltage dc link $S_{T1} \sim S_{T3}$, $S_{B1} \sim S_{B3}$ are in one group name as body switches, all the devices connected between the low voltage dc-link and high voltage dc link S_{T4}, S_{T5}, S_{B4}, S_{B5} are in one group named as wing switches. All the switches in the body switches group or in the wing switches group are controlled complementarily with 50% duty cycle as usual, a phase-shift angle is added between two groups. There are also four different modes in the DW-MMCCC with even conversion ratio, as shown in Figure 7.7. Figure 7.8 shows the ideal waveforms of 4X-DW-MMCCC with phase-shift control. It can be derived from the figure that, the output current

waveforms of the DW-MMCCC with even conversion ratio is more symmetric than the odd conversion ratio DW-MMCCC. And the capacitor voltage or the output voltage ripples of the even conversion ratio DW-MMCCC is smaller than the odd conversion ratio DW-MMCCC due to the self interleaving structure.

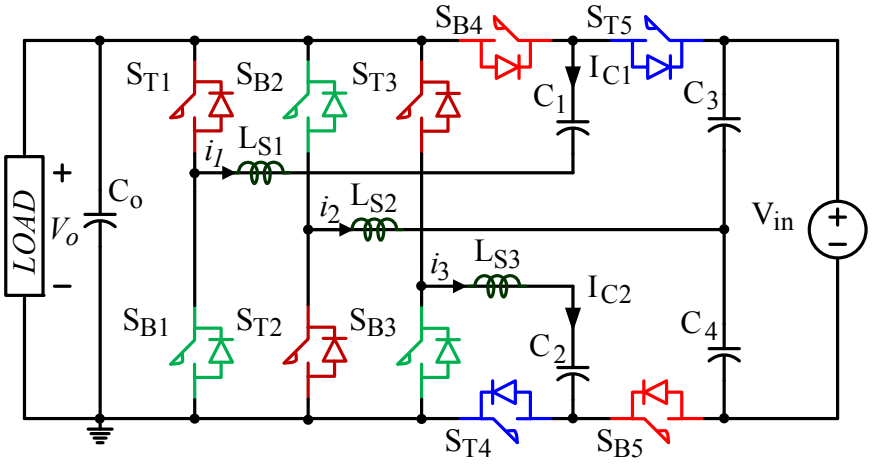
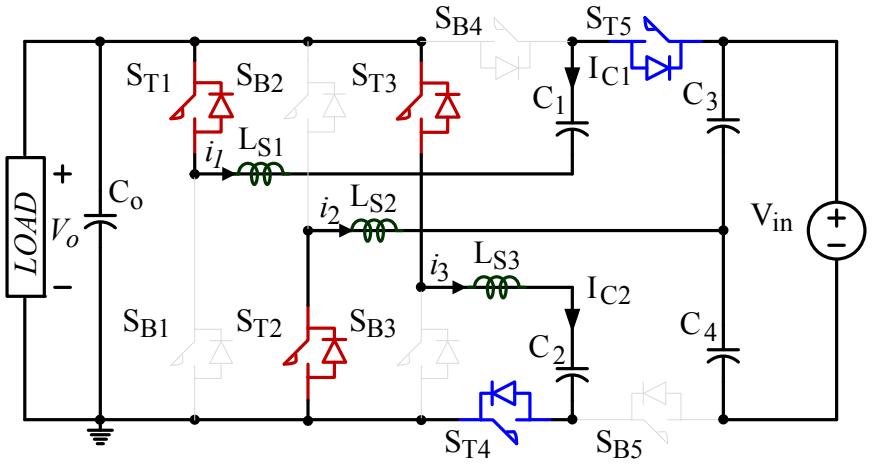


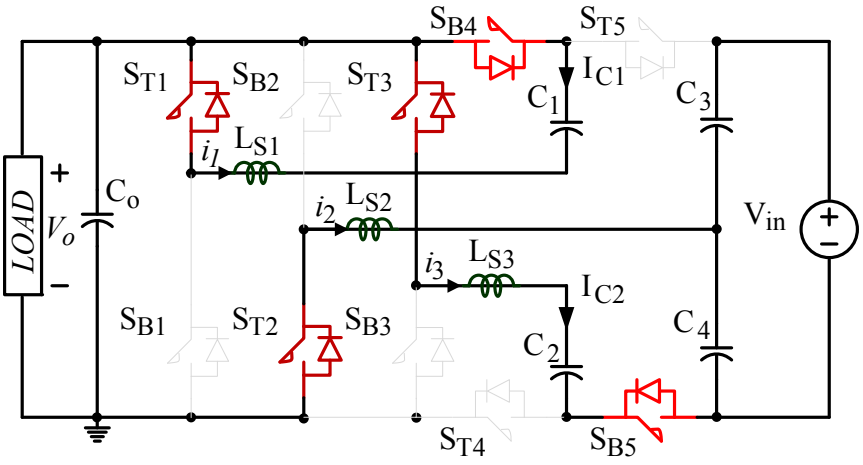
Figure 7.6 4X-DW-MMCCC main circuit structure.



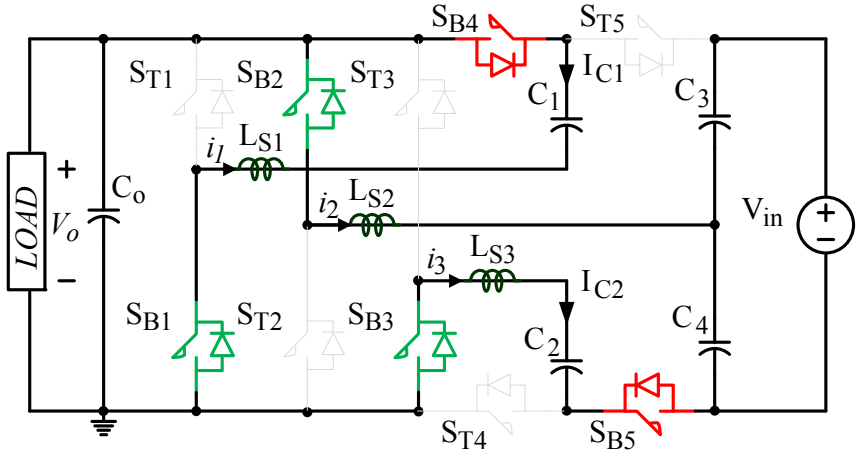
(a)

Figure 7.7 Equivalent circuits in each operation modes of the 4X-DW-MMCCC with phase-shift control.

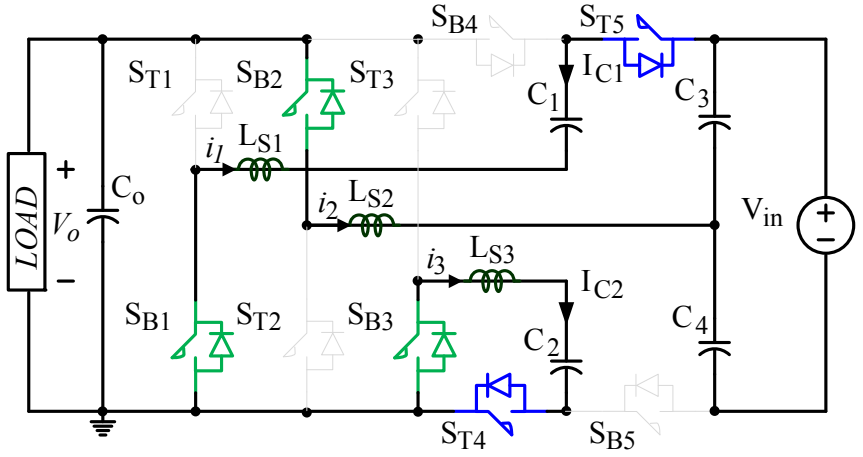
Figure 7.7 cont'd



(b)



(c)



(d)

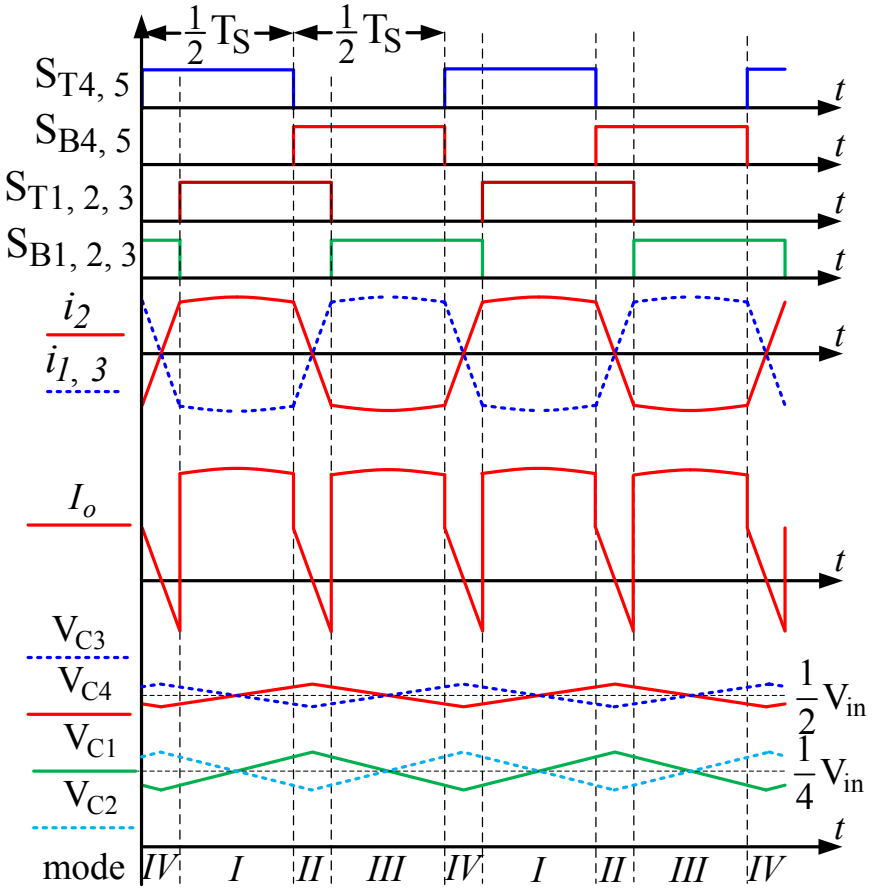


Figure 7.8 Ideal waveforms of 4X-DW-MMCCC with phase-shift control.

However, the multiphase interleaving operation of odd conversion ratio DW-MMCCC can be achieved easily to reduce the input and output current ripple and voltage. The proper circuit can be selected based on the application requirement.

7.3 Soft-switching Operation Principles of the DC-DC Converter Module

By utilizing the energy stored in the stray inductance, the ZVS of all the switches can be achieved. The 3X-DW-MMCCC will be used as an example for analysis without losing generosity. Due to the circuit symmetric features, the ZVS operation principles of the 3X-DW-

MMCCC will only half cycle for analysis. Figure 7.9 shows the idealized voltage and current waveforms with ZVS during a half cycle. The detailed equivalent circuit in each state is shown in Figure 7.10.

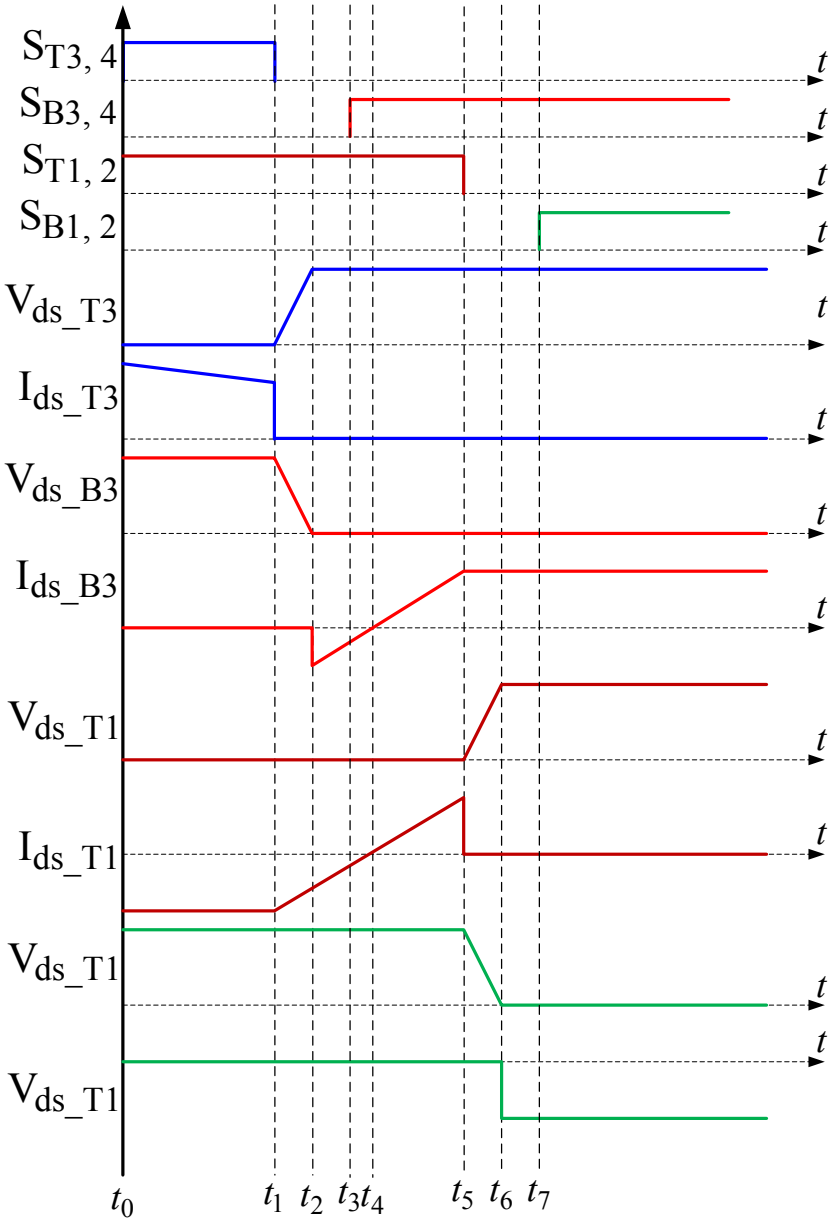
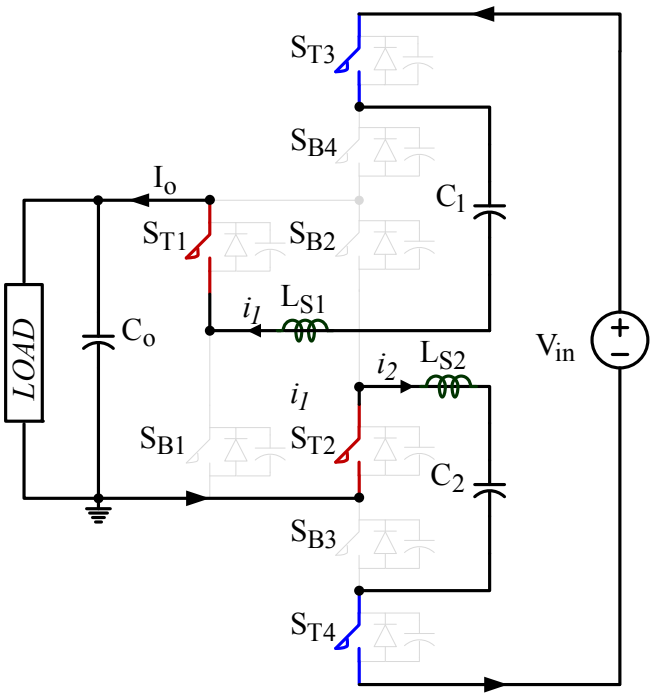
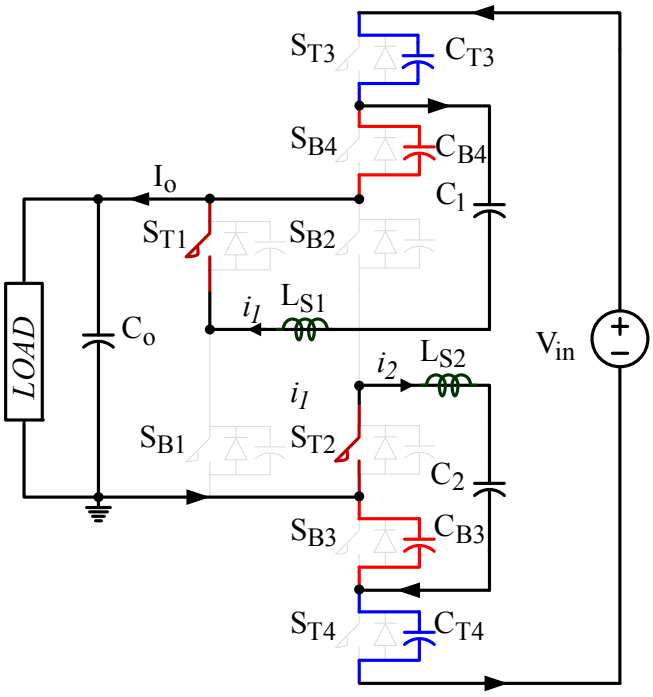


Figure 7.9 Idealized voltage and current waveforms with ZVS.



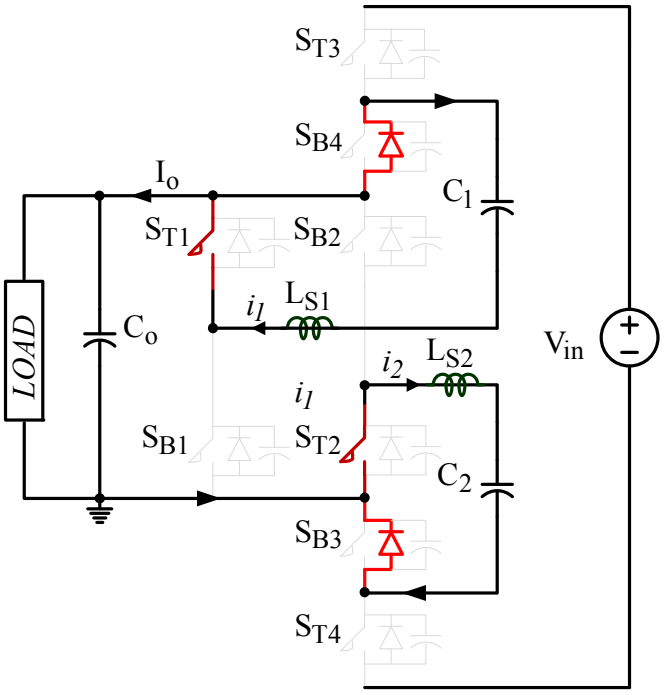
(a)



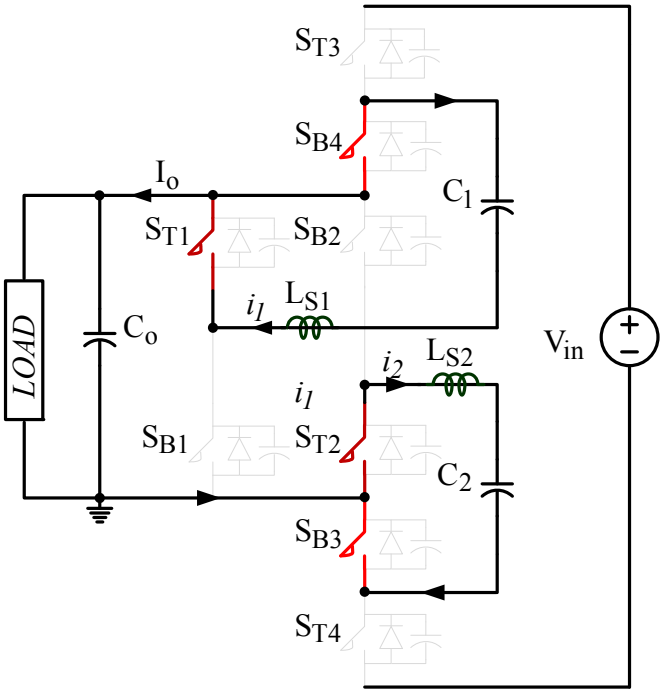
(b)

Figure 7.10 Commutation modes during a half switching cycle. (a) (t0 ~ t1), (b) (t1 ~ t2), (c) (t2 ~ t3), (d) (t3 ~ t4), (e) (t4 ~ t5), (f) (t5 ~ t6), (g) (t6 ~ t7), (h) (t7 ~)

Figure 7.10 cont'd

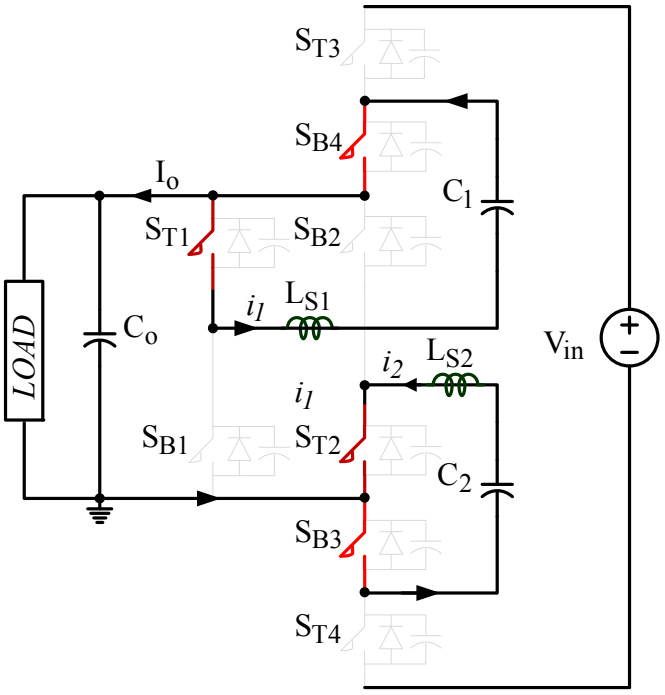


(c)

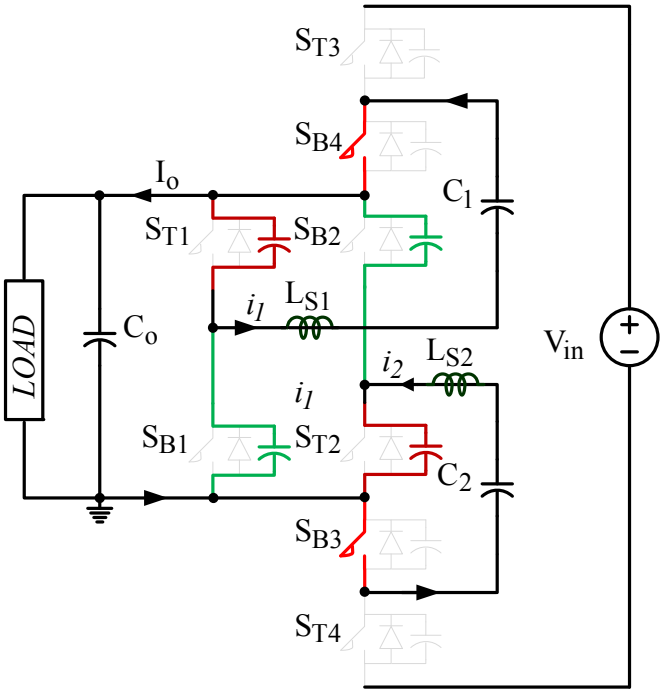


(d)

Figure 7.10 cont'd

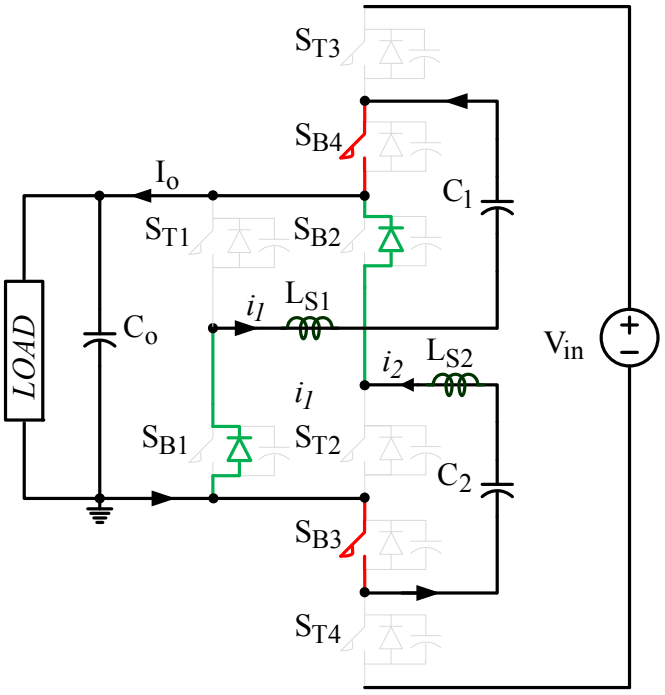


(e)

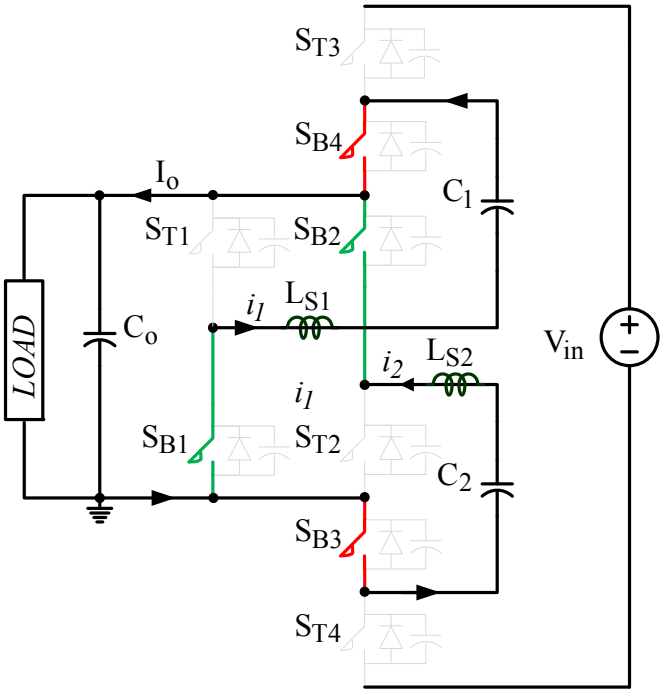


(f)

Figure 7.10 cont'd



(g)



(h)

7.4 Control Strategy

Figure 7.11 shows the system control block diagram. The output voltage and load current are sensed to calculate the feed-forward phase-shift angle. And a PI controller is used to compensate the parameter errors.

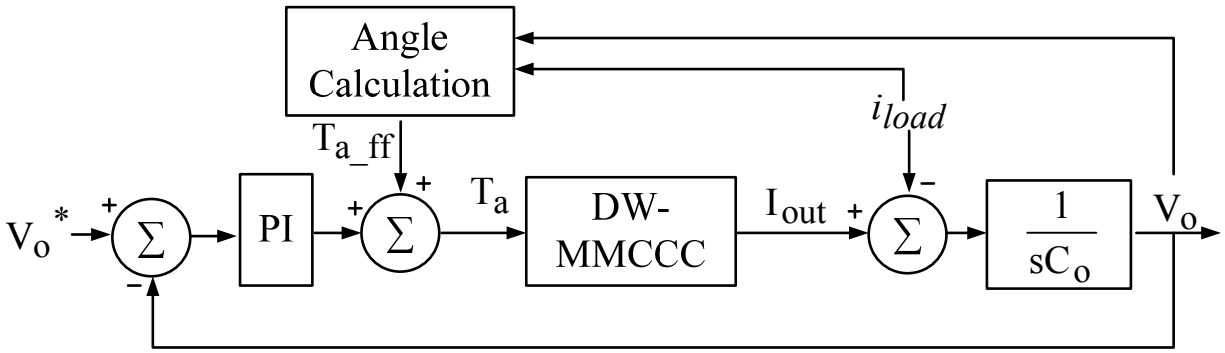


Figure 7.11 Control block diagram of the DW-MMCCC with phase-shift control.

7.5 Simulation Results

Figure 7.12 shows the simulation results of 500 W 3X-DW-MMCCC with 42 V input and three different output voltages. The switching frequency is about 62.5 kHz. The stray inductance is L_{S1} and L_{S2} is about 270 nH. The capacitance of C_1 and C_2 is 100 μF.

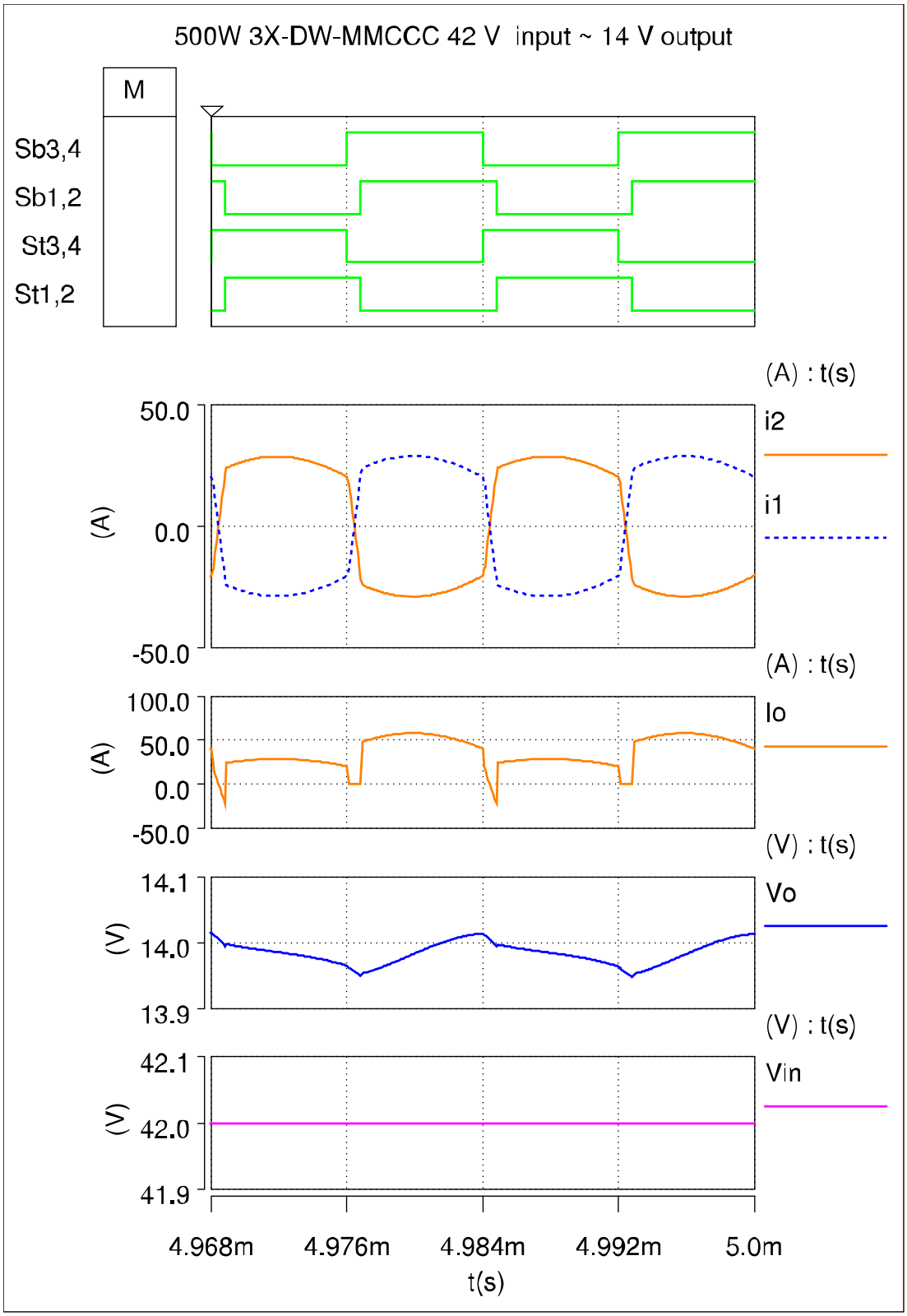
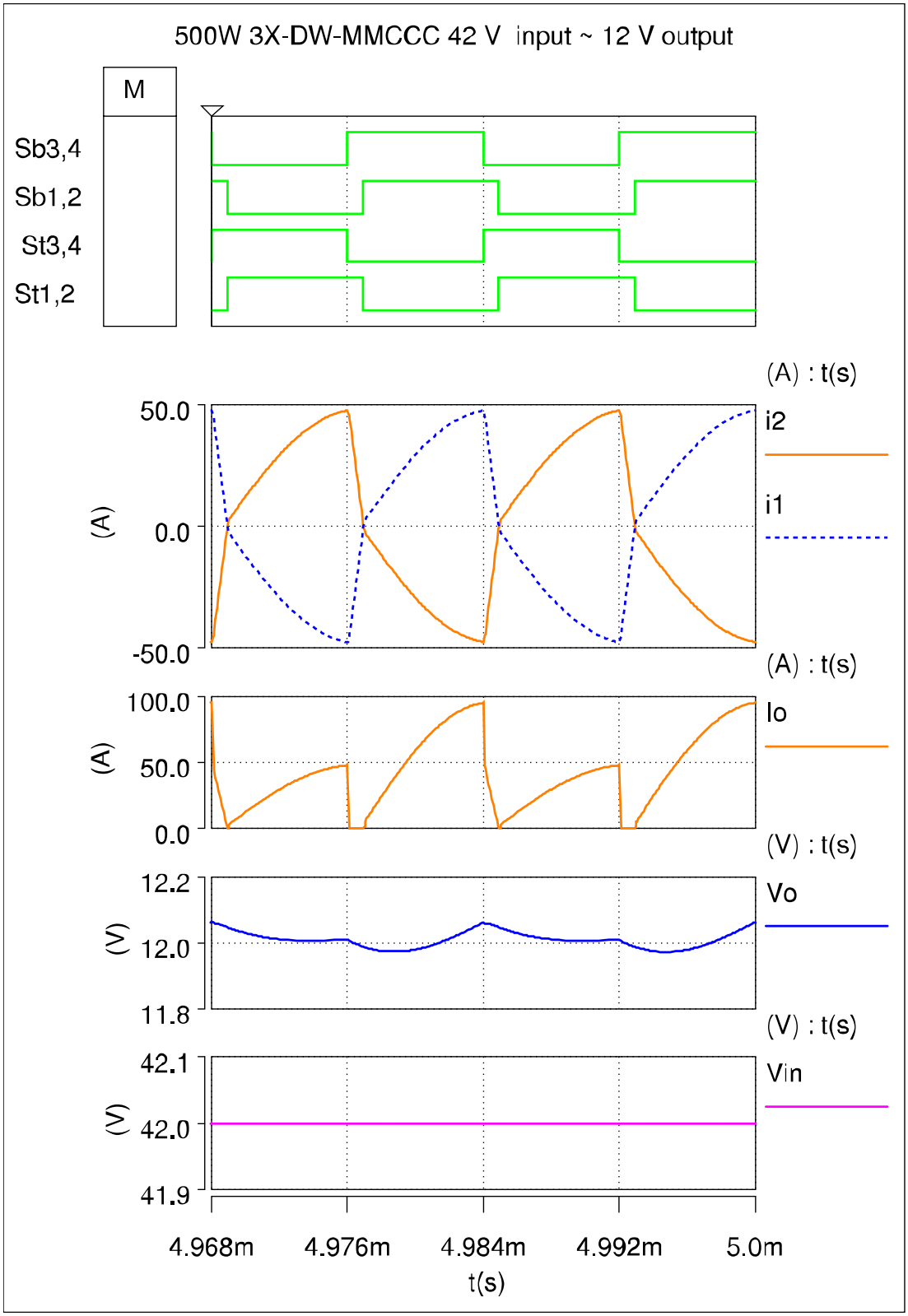


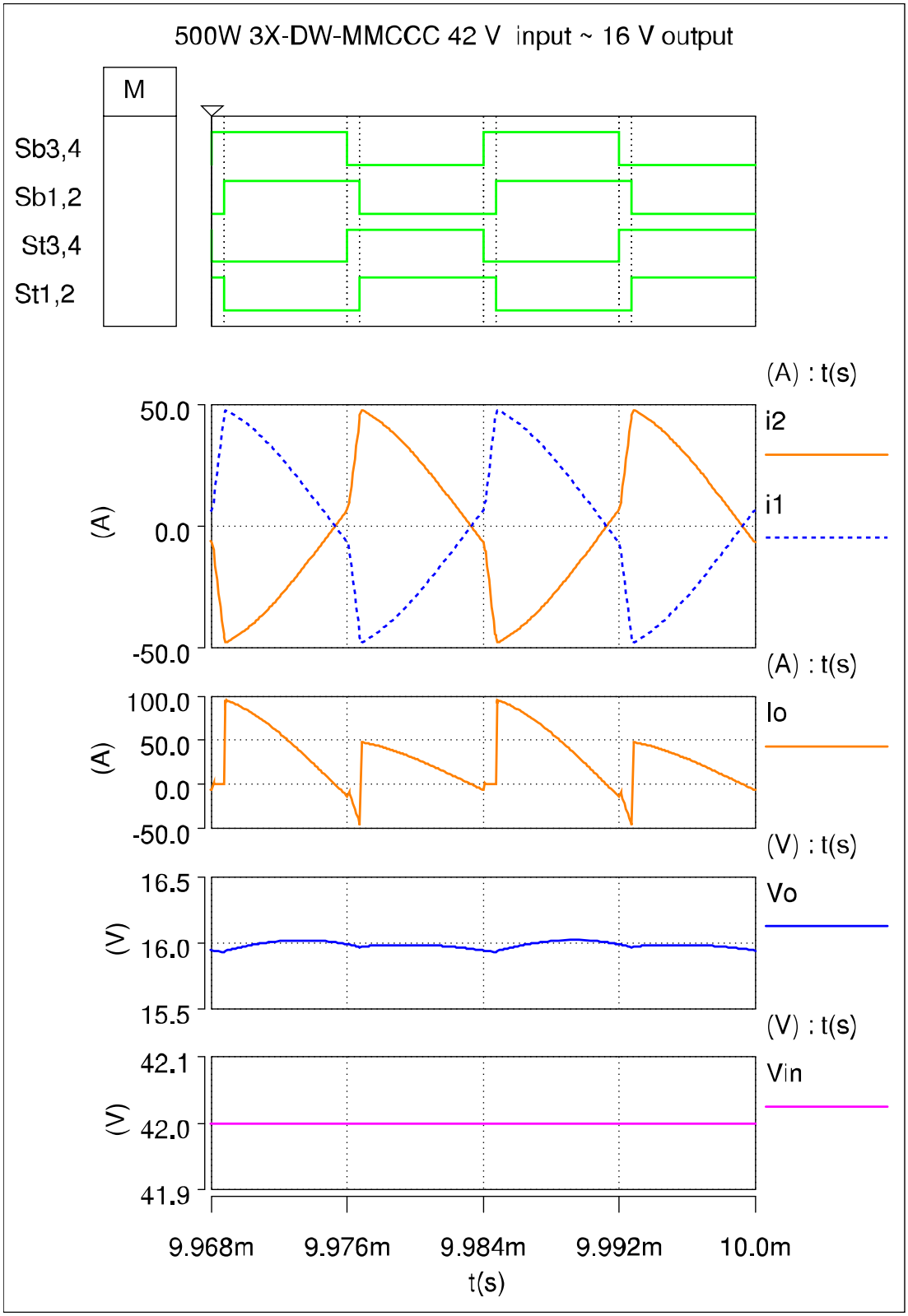
Figure 7.12 (a)Simulation results of 500 W 3X DW-MMCCC with 42 input and three different output voltage. (a) 14 V output. (b) 12 V output (c) 16 V output.

Figure 7.12 cont'd

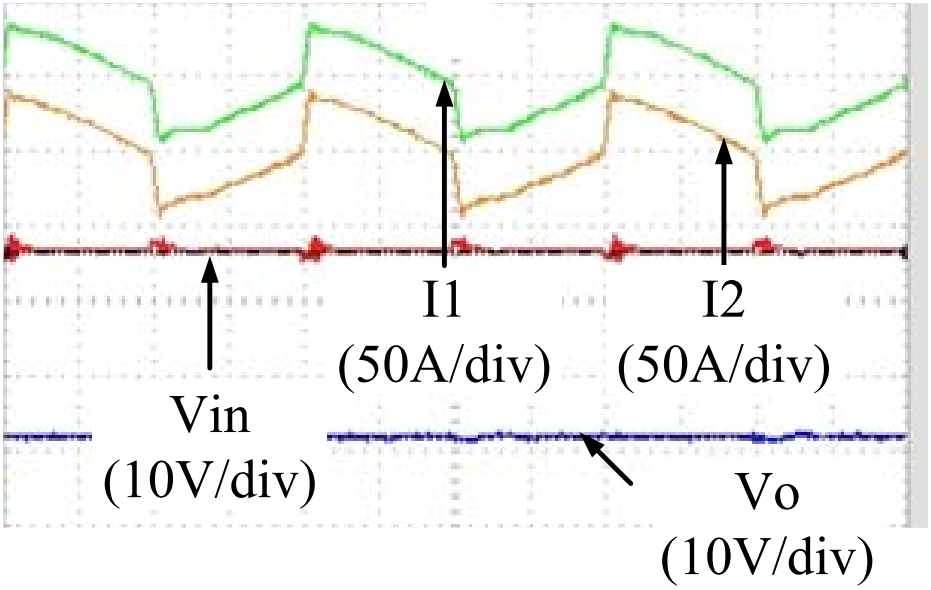


(b)

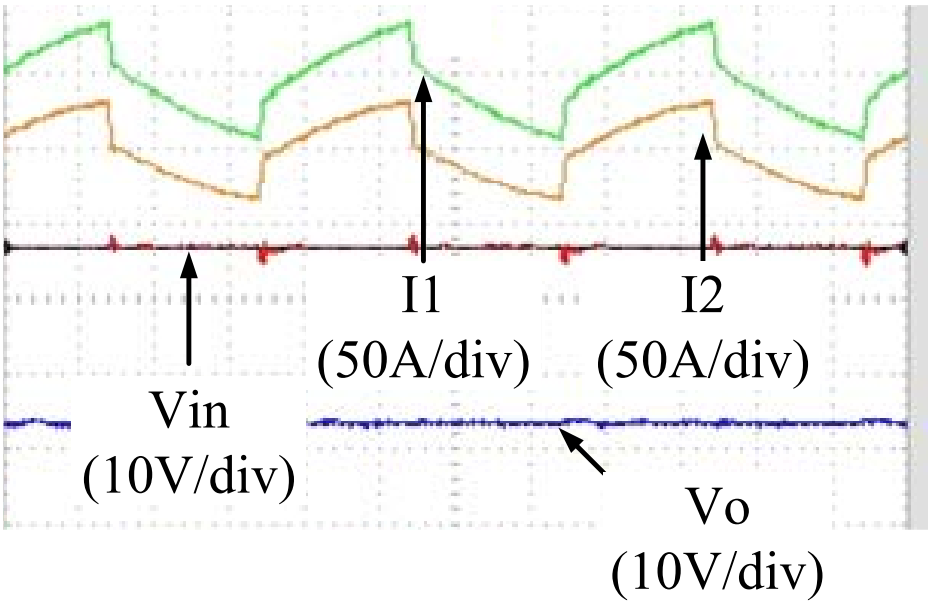
Figure 7.12 cont'd



(c)



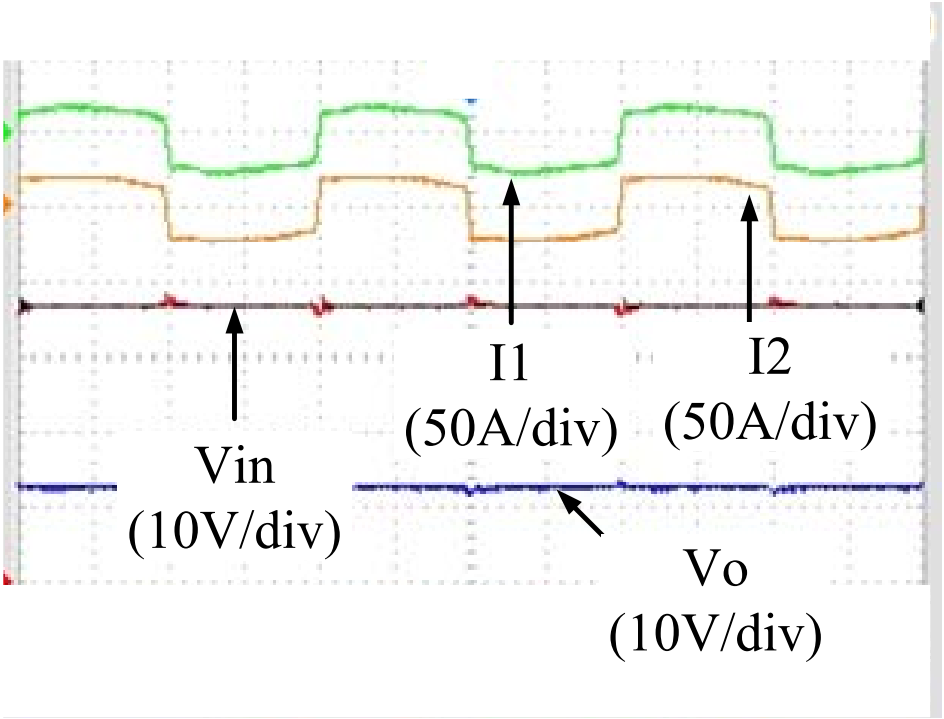
(a)



(b)

Figure 7.13 Experiments results of 500 W 3X DW-MMCCC with 36.8 V input voltage and three different output voltage(a) 12.68 V, (b) 11.6 V (c) 13.4 V.

Figure 7.13 cont'd



(c)

7.6 Conclusion

This chapter presents a phase-shift control method of DW-MMCCC to achieve output voltage fine regulation and zero voltage switching for all the switches. By utilizing the carefully designed stray inductance and controlling the current through it, the output voltage fine regulation can be achieved. Since zero voltage switching can be achieved for all the switches, the switching loss can be eliminated. The converter can be designed to achieve up to 99% efficiency by selecting the proper switching devices and capacitors. By implementing the proposed control method with the traditional step voltage output method, a fine regulation of switched-capacitor dc-dc converter can be achieved with high efficiency in a wide output voltage range. Simulation results are provided to demonstrate the validity of the proposed control method. A 500 W

prototype is being built, experimental results with efficiency curves are provided to illustrate the features of the proposed circuit.

CHAPTER 8
Z-source and Quasi-Z-source DC-DC Converters for DC Motor Drive and Zero Voltage Electronic Load Applications

This chapter presents a group of Z-source and quasi-Z-source dc-dc converter topologies derived from the Z-source and quasi-Z-source inverters. These dc-dc converters own special features, including four quadrant operation and ideal current source characteristics. By only utilizing two active switches and the Z-source network, these converters are able to output positive voltage and negative voltage at the same time by changing duty cycle. Therefore, these converters can provide four quadrant operations for DC motor drive with minimal number of switches. The two active switches of these converters are controlled complementarily. At 0.5 duty cycle, some of the proposed converters can output zero voltage, which means they can draw constant current without any voltage drop like an ideal current source. By using this feature, Z-source dc-dc converter can be used as a zero voltage electronic load for photovoltaic (PV) cell testing. A Z-source dc-dc converter prototype with one MOSFET and a diode has been built to demonstrate the first and forth quadrant operation. A quasi-Z-source dc-dc converter prototype has also been built to demonstrate the ideal current source feature. Experimental results are provided to verify the validity and features of proposed circuits.[8]

8.1 Introduction

[8] This work has been presented in part in *Applied Power Electronics Conference and Exposition, 2009. APEC 2009. Twenty-Fourth Annual IEEE, 2009, pp. 1097-1101.*

Recently, many renewable dc sources (photovoltaic array, fuel cell) have been used for industry applications such as dc motor drives. A four quadrant dc-dc converter is required for the dc motor drive (forward, backward motoring and breaking) [16-18]. Voltage-fed full-bridge dc-dc converters have been used for dc motor drives for many years [18]. For low power dc motor drive, semiconductor switching device cost is the major part of the total cost. By utilizing four active switches, full-bridge dc-dc converters suffer relatively high cost problem. Therefore, to develop a low cost dc-dc converter with fewer switches for dc motor drive becomes a challenge.

At the same time, in the performance test of the renewable energy source such as photovoltaic (PV) arrays, an electronic load is used. In order to test the PV arrays short circuit characteristics, zero voltage operation of the electronic load is required, which is a major challenge for the electronic load design [177-185]. It is difficult for the traditional electronic load to output low voltage near zero due to the transistor power loss and saturation [186]. A zero voltage electronic load (ZVEL) based on Z-source inverter has been proposed recently [187]. It is able to output zero voltage and meets the needs of renewable energy sources testing. But five active switches have to be used.

In order to overcome the problems of voltage-fed and current-fed inverter as well as to achieve buck-boost voltage gain, Z-source inverters (ZSIs) and quasi-Z-source inverters (qZSIs) have been proposed recently [188-192]. ZSIs and qZSIs have been investigated vastly and applied for adjustable speed drive, UPS, fuel cell and photovoltaic applications [193-204]. The control and modulation methods of ZSI are also proposed, compared and investigated thoroughly [125, 205-216]. Utilizing the Z-source network in the dc-dc converter becomes popular recently. Single-phase quasi-Z-source inverter has been applied in the isolated dc-dc converter for distributed power generation applications [217-220]. Two dc-dc converters derived from the Z-

source inverter have been proposed [221, 222]. But detailed device stress analysis, passive component design, and converter voltage gain considering circuit power loss are not covered. Some other dc-dc converters that make use of the Z-source network as a basic cell to achieve four quadrant operation have been proposed [223]. But the derived topologies are not complete, more simply dc-dc converter topologies with four quadrant operation features utilizing Z-source network should also be discussed [224]. Other dc-dc converter topologies using coupled inductor or hybrid Z-network to achieve four quadrant operations have been investigated [189, 225]. But coupled inductors have to be used in these circuits. Therefore, more dc-dc converter utilizing Z-source network with minimum number of passive components should be derived. The detailed design consideration issues of Z-source dc-dc converter including device stress analysis, passive components design, and the converter voltage gain curve in non-ideal case should be discussed.

This chapter presents a family of dc-dc converters derived from the existing voltage-fed/current-fed ZSI/qZSI inverter topologies. The existing Z-source dc-dc converters with four quadrant operation features [221-223] are summarized. More Z-source or quasi-Z-source dc-dc converters with less passive components are proposed in this chapter. These dc-dc converters are able to achieve the four quadrant (bidirectional current flow and bipolar output voltage) operation with minimal number of switching devices and passive components. When the duty cycle changes from 0 to 0.5, these converters can output positive voltage with buck or boost characteristic. When the duty cycle changed from 0.5 to 1, these converters can output negative voltage with buck-boost characteristic. Duty cycle 0.5 is the boundary point of the positive output and negative output. At 0.5 duty cycle some of the converters can output zero voltage while others can output infinity voltage. The converters that can output zero voltage at 0.5 duty cycle can be used as a ZVEL for PV arrays test. A Z-source dc-dc converter prototype with an

active switch and a diode was built to confirm the operation in the first and fourth quadrant. A quasi-Z-source dc-dc converter based ZVEL has also been built. Experiment results are given to demonstrate the specific features of the proposed circuits.

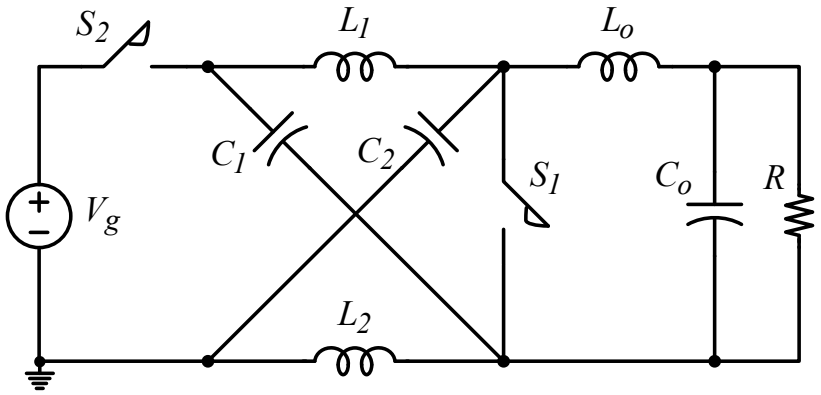
8.2 Topology Derivation and Proposed Circuits

In this section, a systematic way of deriving Z-source dc-dc converters from the voltage-fed/current-fed ZSI or qZSI topologies will be provided. Twelve Z-source/quasi-Z-source dc-dc converter topologies will be derived, some of the derived Z-source dc-dc converter topologies have already been proposed in the literature using other derivation methods [221-223]. However, by using the proposed method in this chapter, more circuits with simpler structures can be derived. The dc-dc converter that can be derived from the voltage-fed/current-fed ZSI topologies will be termed as Z-source dc-dc converter, others that can be derived from the qZSI topologies will be termed as quasi-Z-source dc-dc converter.

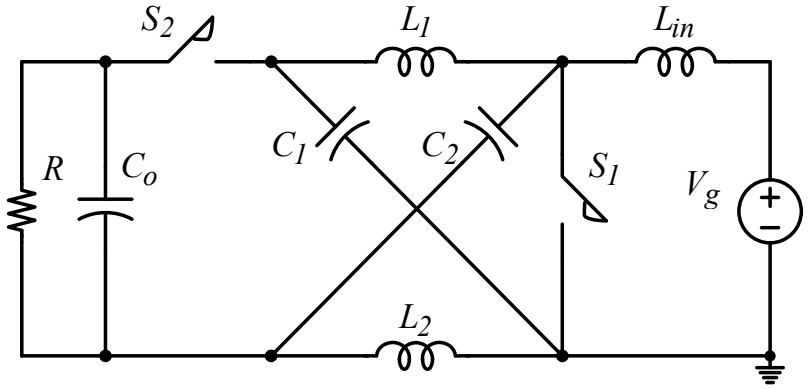
To derive a corresponding dc-dc converter from voltage-fed ZSI/qZSI, the following procedure can be followed: (1) replace the diode with an active switch; (2) replace the inverter bridge with one active switch; (3) add an LC filter in parallel with the switch or add the load directly in parallel with one of the capacitors of the Z-source network. To derive a corresponding dc-dc converter from current-fed ZSI/qZSI, similar procedure can be followed: (1) replace the diode with an active switch; (2) replace the inverter bridge and C filter with one active switch in series with a capacitor. After one circuit is derived by using the aforementioned methods, the input and the output can be swapped to obtain its inverse circuit.

Figure 8.1 shows two Z-source dc-dc converters that can be derived from the traditional voltage-fed and current-fed ZSIs [190-192]. Figure 8.1(a) is derived from the voltage-fed ZSI by replacing the input diode with an ideal switch S2, replacing the inverter bridge with an ideal

switch S1 and a LC filter in parallel with the switch. Figure 8.1(b) can be derived from the current-fed ZSI by replacing the diode with an ideal switch S1, replacing the inverter bridge and the C filter with an ideal switch S2 in series with a capacitor. Figure 8.1(b) can also be derived by swap the input and output of the Figure 8.1(a).



(a)

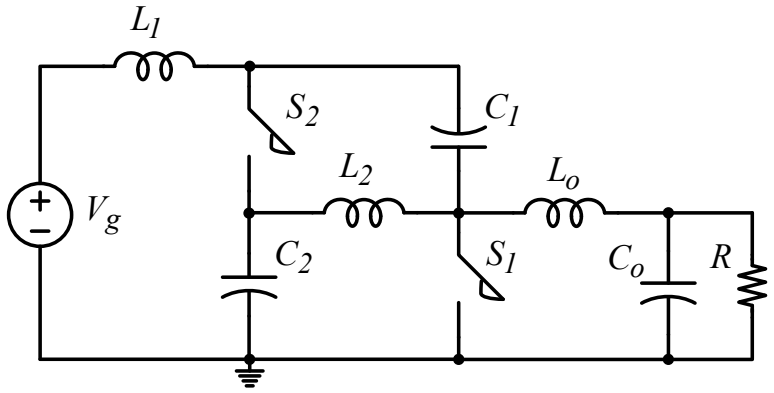


(b)

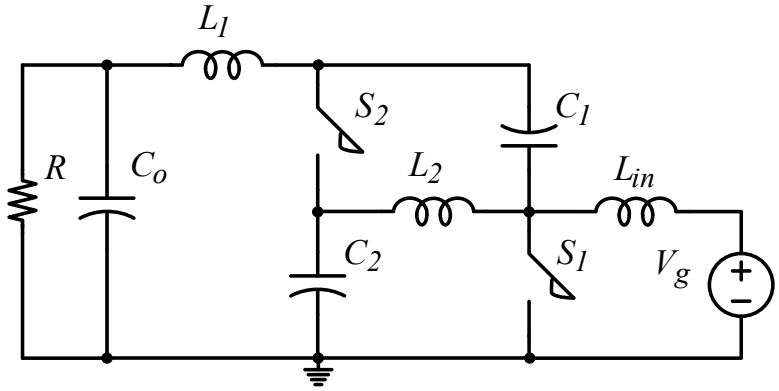
Figure 8.1. (a) Z-source dc-dc converter (a) derived from the voltage-fed ZSI, (b) Z-source dc-dc converter (b) derived from the current-fed ZSI.

Figure 8.2 ~ Figure 8.4 shows the quasi-Z-source dc-dc converters derived from the voltage-fed qZSI. Figure 8.2(a) shows the quasi-Z-source dc-dc converter that can be derived directly from the voltage-fed qZSI with continuous input current. Figure 8.2(b) shows the inverse circuit of Figure 8.2(a) by swapping the input and the output. Figure 8.3(a) shows the quasi-Z-source dc-dc converter derived from the voltage-fed qZSI with continuous input current by adding the

load directly in parallel with the capacitor C2 of Z-source network. Figure 8.3(b) shows the corresponding inverse circuit of Figure 8.3(a). Figure 8.4(a) shows the quasi-Z-source dc-dc converter derived from the voltage-fed qZSI with discontinuous input current. Figure 8.4(b) shows the inverse circuit of Figure 8.4(a).

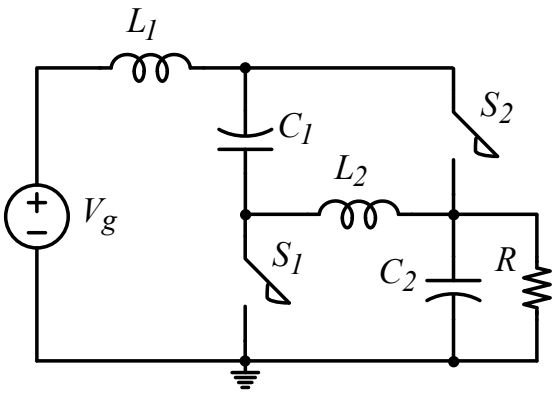


(a)

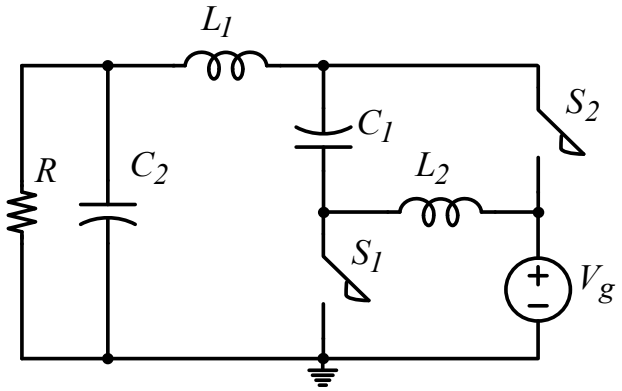


(b)

Figure 8.2. Quasi-Z-source dc-dc converters derived from the voltage-fed qZSI with continuous input current.

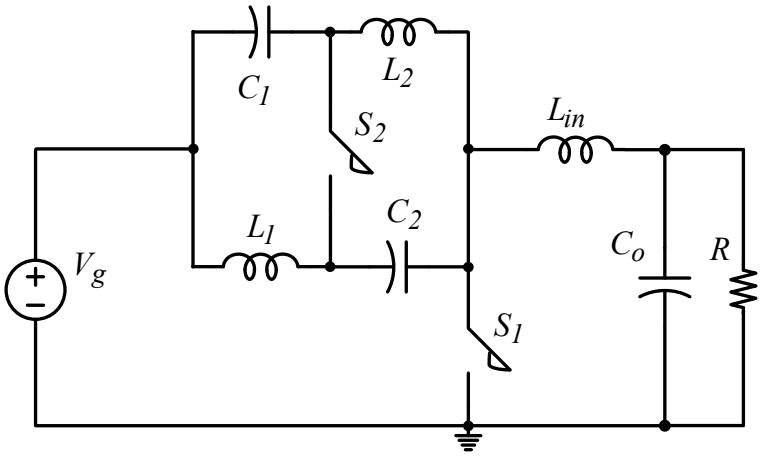


(a)



(b)

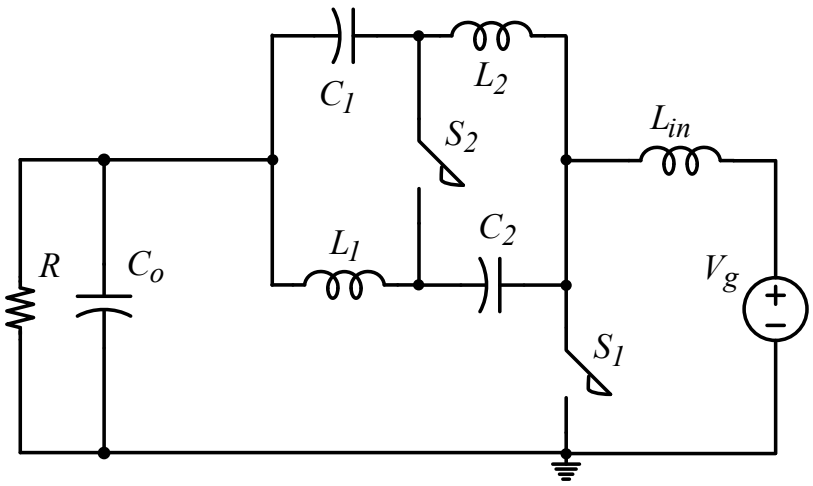
Figure 8.3 Quasi-Z-source dc-dc converters derived from the voltage-fed qZSI with continuous input current.



(a)

Figure 8.4 (a) Quasi-Z-source dc-dc converters derived from the voltage-fed qZSI with discontinuous input current.

Figure 8.4 cont'd

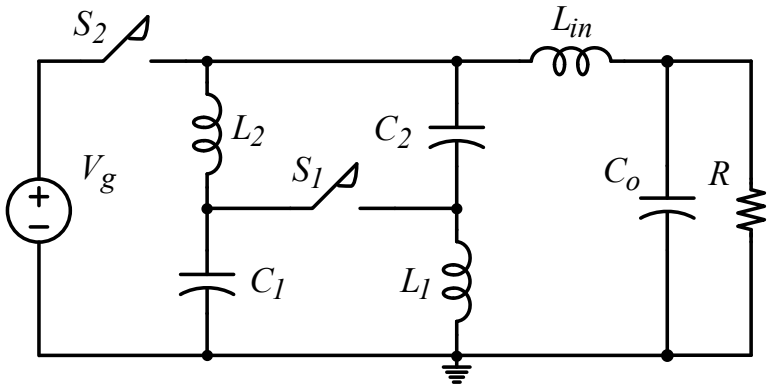


(b)

Figure 8.5 and Figure 8.6 shows the quasi-Z-source dc-dc converters derived from the current-fed qZSI. Figure 8.5(b) shows the quasi-Z-source dc-dc converter that can be derived from the current-fed qZSI with continuous input current. Figure 8.5(a) shows the corresponding inverse circuit of Figure 8.5(b). Figure 8.6(b) shows the Z-source dc-dc converter that can be derived from the current-fed qZSI with discontinuous input current. Figure 8.6(a) shows the corresponding inverse circuit of Figure 8.6(b). Figure 8.6(a) also can be derived from the voltage-fed ZSI by adding load in parallel with the capacitor of Z-source network. Since the circuits in Figure 8.6 can also be derived from the voltage-fed ZSI, it will also be termed as Z-source dc-dc converter.

The Z-source and quasi-Z-source dc-dc converters, as shown in Figure 8.1, Figure 8.4, and Figure 8.5 have been proposed by using other derivation methods [221-223]. By using the proposed systematic deriving method, more circuits, as shown in Figure 8.2, Figure 8.3, and Figure 8.6 can be derived. For the Z-source and quasi-Z-source dc-dc converters in Figure 8.3 and Figure 8.6, the structure are simpler, the number of passive components is reduced. This chapter will concentrate on the Z-source dc-dc converters in Figure 8.3 and Figure 8.6.

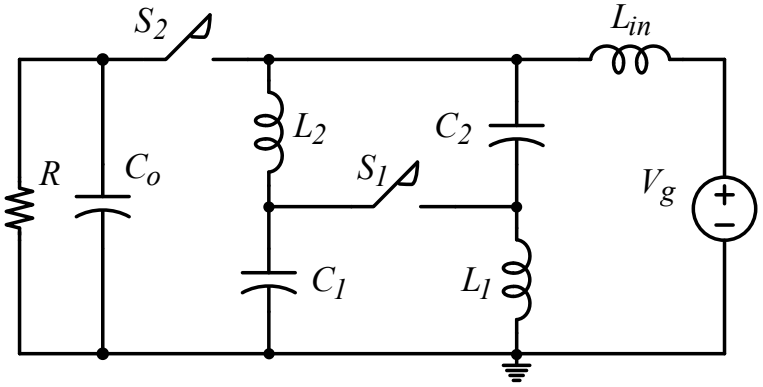
The DC characteristics of the circuits in Figure 8.1(a), Figure 8.2(a), Figure 8.3(a), Figure 8.4(a), Figure 8.5(a), and Figure 8.6(a) are the same including voltage gain and device stress. Define the conduction percentage of switch S1 as the duty cycle. When the duty cycle is changed from 0 to 0.5, the output voltage of these circuits will be changed from the input voltage to positive infinity voltage, which is similar to the boost converter. When the duty cycle is changed from 0.5 to 1, the output voltage of these circuits will be changed from negative infinity to 0, which is similar to the buck-boost converter. Theoretically, when the duty cycle equals to 0.5, these circuits can output positive infinity and negative infinity voltage at the same time. However, due to the circuit power loss, these circuits can only output zero voltage at 0.5 duty cycle. This situation will be discussed in detail section IV. In order to output the positive voltage and negative voltage at the same time, two bi-polar voltage blocking and uni-directional current flowing switching devices, such as Reverse Blocking IGBT (RB-IGBT) have to be used. In section V, more detailed explanation of device selection using device voltage stress and current stress analysis will be provided.



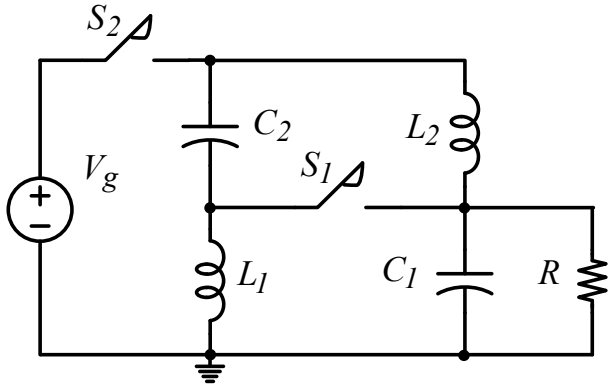
(a)

Figure 8.5. Quasi-Z-source dc-dc converters derived from the current-fed qZSI with continuous input current.

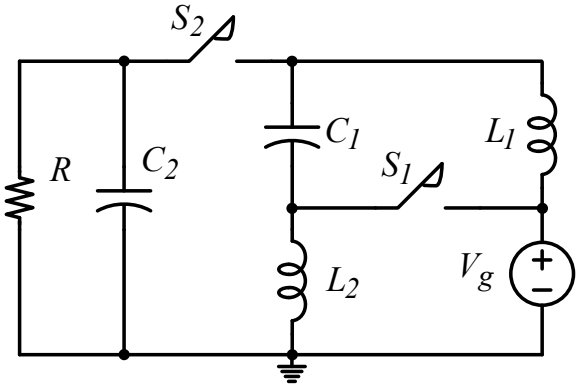
Figure 8.5 cont'd



(b)



(a)



(b)

Figure 8.6. Z-source dc-dc converters derived from the voltage-fed ZSI or current-fed qZSI with discontinuous input current.

The DC characteristics of the circuits in Figure 8.1(b), Figure 8.2(b), Figure 8.3(b), Figure 8.4(b), Figure 8.5(b), and Figure 8.6(b) are the same including voltage gain and device stress. The duty cycle is also defined using the conduction percentage of switch S1. When the duty cycle is changed from 0 to 0.5, the output voltage of these circuits can be changed from the input voltage to zero, which is similar to the buck converter. When the duty cycle is changed from 0.5 to 1, the output voltage of these circuits can be changed from 0 to negative infinity, which is similar to the buck-boost converter. When the duty cycle equals to 0.5, these circuits can output zero voltage. The case of these circuits output zero voltage at 0.5 duty cycle is totally different with the case of above mentioned circuits in Figure 8.1(a)~Figure 8.6(a). These circuits can operate at 0.5 duty cycle without output any power with a little circulating power loss. On the other hand, the aforementioned circuits in Figure 8.1(a)~Figure 8.6(a), can operate at 0.5 duty cycle with all the input power becomes power loss. Different from the circuits in Figure 8.1(a)~Figure 8.6(a), these circuits can utilize two bidirectional current flowing and uni-polar voltage blocking switching devices, such as IGBT and MOSFET to output the positive voltage and negative voltage at the same time. The detailed device stress analysis will also be provided in section V.

8.3 The DC Operation Modes Analysis

As mentioned previously, the converters in Figure 8.1(a)~Figure 8.6(a) have the similar dc characteristics, and the converters in Figure 8.1(b)~Figure 8.6(b) have the similar dc characteristics. In this section, the Z-source dc-dc converter, as shown in Figure 8.6(b) will be used as an example for the dc operation mode analysis. Figure 8.7 shows the Z-source dc-dc converter with all the reference direction marked in the figure for DC operation analysis. The reference direction of the inductor current I1, I2, the switch current I_{S1}, I_{S2} the capacitor voltage

V1, and V_O are marked in the figure. In order to output the positive voltage and the negative voltage at the same time, two active switches (MOSFETs, IGBTs, etc.) with their anti-parallel diodes should be used. If only positive voltage or negative voltage output is needed, only one active switch and a diode are needed for the operation. If zero voltage output is needed, two active switches have to be used at the same time. In the following analysis, these three situations will be discussed separately in terms of duty cycle. Based on the output voltage, the operation mode of this converter can be divided into buck mode, buck-boost mode and zero output voltage mode. In buck mode, the duty cycle is changed from 0 to 0.5; the converter can output positive voltage. During this mode, only one active switch S2 is needed, the switch S1 can be replaced with a diode D1. In buck-boost mode, the duty cycle is changed from 0.5 to 1; the converter can output negative voltage. During this mode, only one active switch S1 is needed, the switch S2 can be replaced with a diode D2. In zero output voltage mode, the duty cycle is equal to 0.5, the converter can output zero voltage. During this mode, two active switches have to be used. Define the conduction time of S1 or D1 as the duty cycle D.

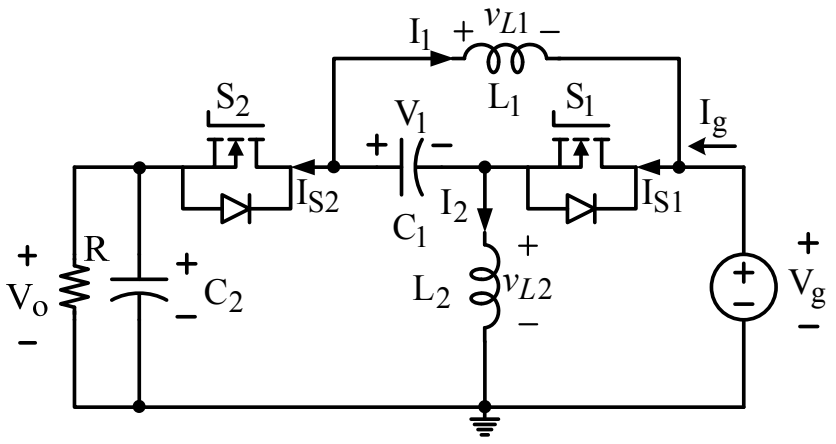
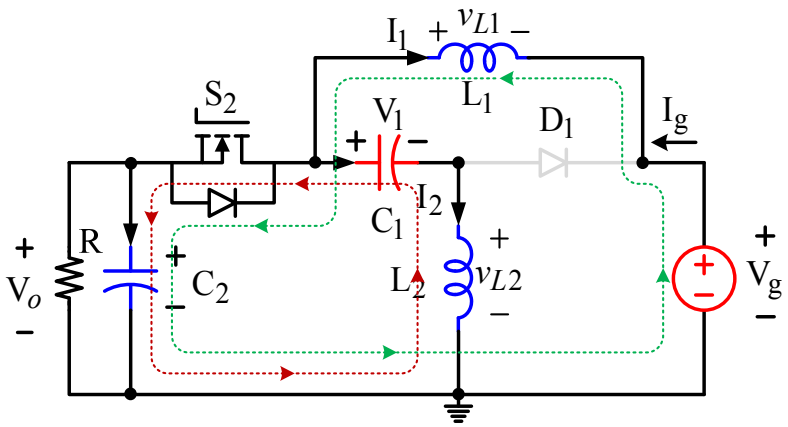


Figure 8.7 Z-source dc-dc converter of Figure 8.6(b) for dc operation analysis. The voltage and current direction marked in the figure is the reference direction. The real voltage and current direction of this converter will varies in different mode.

8.3.1 Buck Mode with Positive Output(0<D<0.5)

When the duty cycle is changed from 0 to 0.5, this Z-source dc-dc converter is similar to a buck converter. The output voltage is positive and the converter voltage gain is smaller than 1. Only one active switch and a diode are needed for the operation. During this duty cycle range, the switch S1 can be considered as the synchronous rectifier, which is similar to the bottom switch of buck converter.

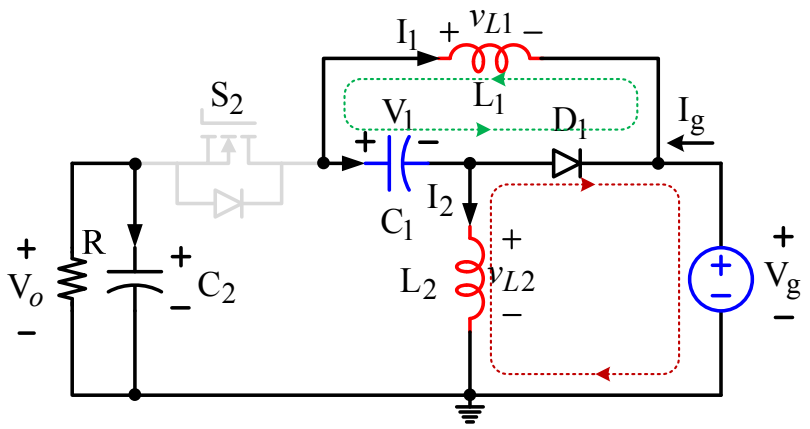
Figure 8.8 shows the two equivalent switching states of the Z-source dc-dc converter in buck mode. Figure 8.8(a) shows the switching state when the switch S2 is on. There are two current loops in this switching state. The real current direction of each loop is marked in the figure with dotted arrow line. During this switching state, the input voltage source Vg charges the inductor L1 and the output capacitor C2; the capacitor C1 charges the inductor L2 and the output capacitor C2. Figure 8.8(b) shows the switching state when the diode D1 is on. There are also two current loops in this switching state. The real current direction is also marked with dotted arrow line in the figure. During this switching state, the diode D1 is conducted for the continuation of inductor current I1 and I2. The capacitor C1 is charged by the inductor L1, and the energy of the inductor L2 flows back to the input voltage source.



(a)

Figure 8.8 Two switching states of Z-source dc-dc converter in buck mode. (a) switch S2 is on; (b) diode D1(S1) is on.

Figure 8.8 cont'd



(b)

Figure 8.9 shows the typical waveforms of Z-source dc-dc converter in buck mode. D1(S1) and S2 show the conduction time of two switches. The inductor current I1 and I2 are negative, because the real inductor current is opposite to the reference inductor current as marked in Figure 8.7. The switch current I_{S1} and I_{S2} are the sum of the inductor current I1 and I2. Since the switch S1 can be replaced by a diode D1 in this mode, the current I_{S1} is negative, which is opposite to the reference current I_{S1} as marked in Figure 8.7. Output voltage is positive and is always smaller than the input voltage.

When the duty cycle is near 0.5, or the inductor current is small, the switch S1 cannot be replaced by the diode for the circuit analysis. Since discontinuous mode may happen if only a diode is used. The discontinuous mode of this converter only using a diode is out of the scope of this chapter, which will not be discussed here. When the duty cycle is near 0.5, two active switches S1 and S2 have to be used for the circuit analysis, which is similar to the zero output voltage mode in part C.

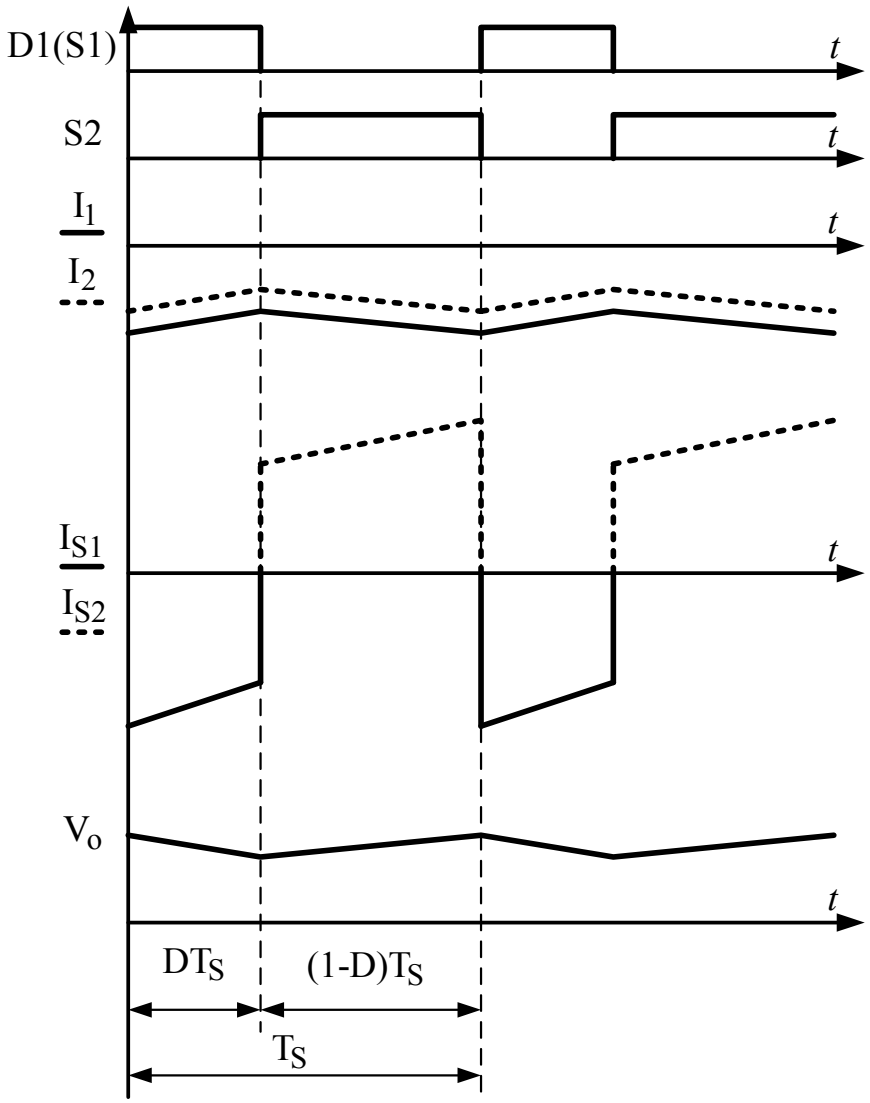
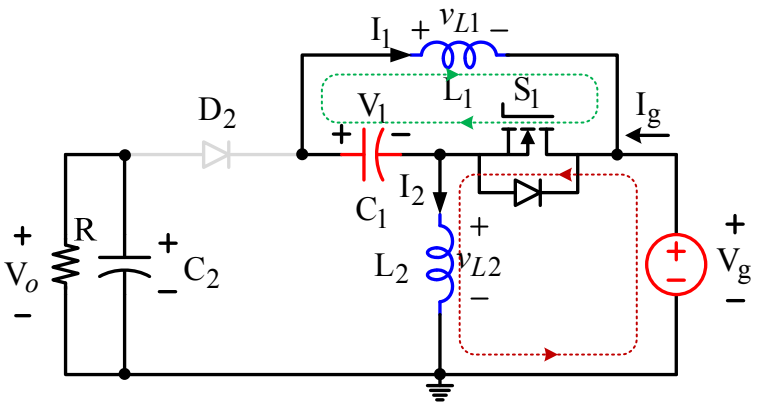


Figure 8.9 Typical waveforms of Z-source dc-dc converter in buck mode (0<D<0.5). The current and voltage reference direction is according to the marked direction in Figure 8.7.

8.3.2 Buck-boost Mode with Negative Output (0.5<D<1)

When the duty cycle is changed from 0.5 to 1, this Z-source dc-dc converter is similar to a buck-boost converter. The output voltage is negative and the converter voltage gain is from zero to negative infinity. Only one active switch and a diode is needed for the operation. During buck-boost mode, the switch S2 can be considered as the synchronous rectifier, which is similar to the output switch of the buck-boost converter.

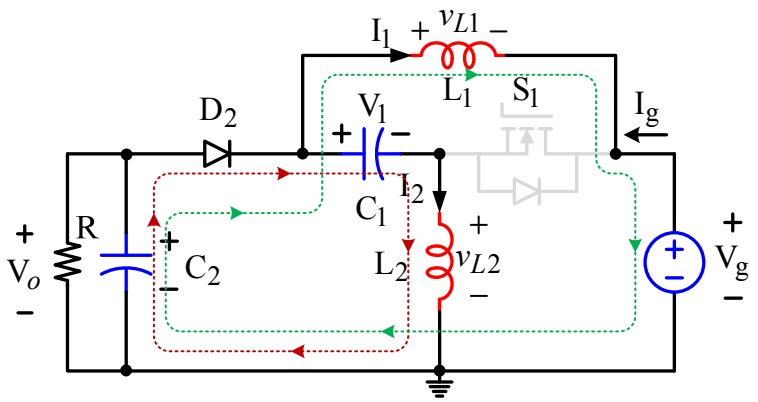
Figure 8.10 shows the two equivalent switching states of the Z-source dc-dc converter in buck-boost mode. Figure 8.10(a) shows the switching state when the switch S1 is on. There are two current loops in this switching state. The real current direction is marked in the figure with dotted arrow line. During this switching state, the input voltage source Vg charges the inductor L2; the capacitor C1 charges the inductor L1. Figure 8.10(b) shows the switching state when the diode D2 is on. There are also two current loops in this switching state. The real current direction is also marked with dotted arrow line in the figure. During this switching state, the diode D2 is conducted for the continuation of inductor current I1 and I2. The capacitor C1 and C2 is charged by the inductor L2, and the capacitor C2 and the input voltage source is charged by the inductor L1.



(a)

Figure 8.10 Two switching states of Z-source dc-dc converter in buck-boost mode. (a) switch S1 is on; (b) diode D2(S2) is on.

Figure 8.10 cont'd



(b)

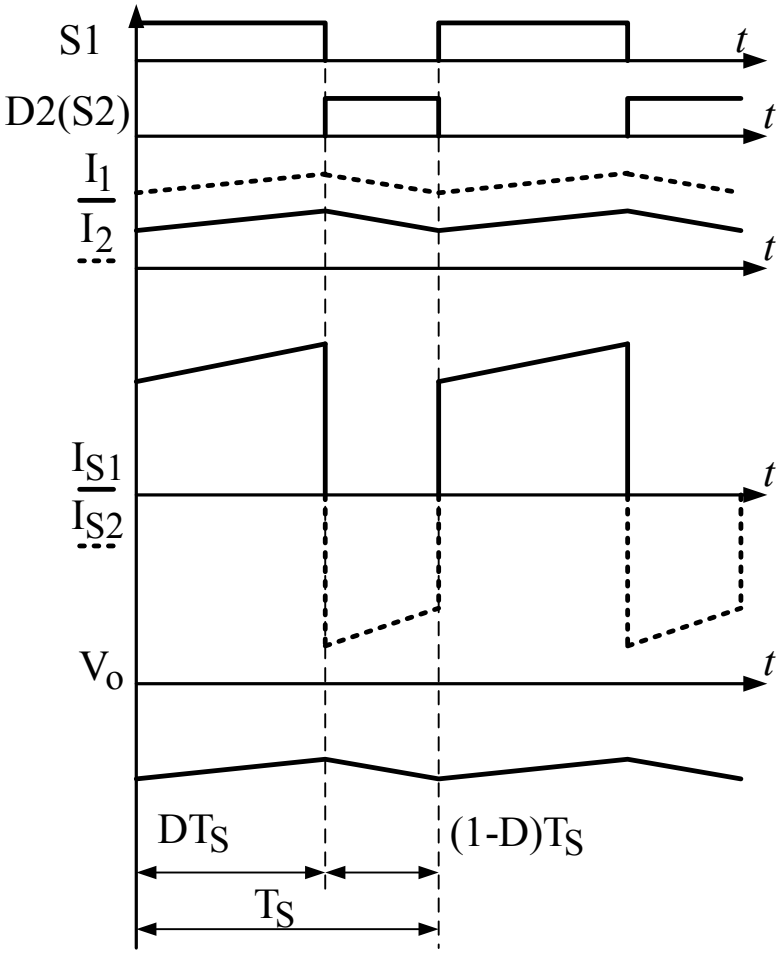


Figure 8.11 Typical waveforms of Z-source dc-dc converter in buck-boost mode (0.5<D<1). The current and voltage reference direction is according to the marked direction in Figure 8.7.

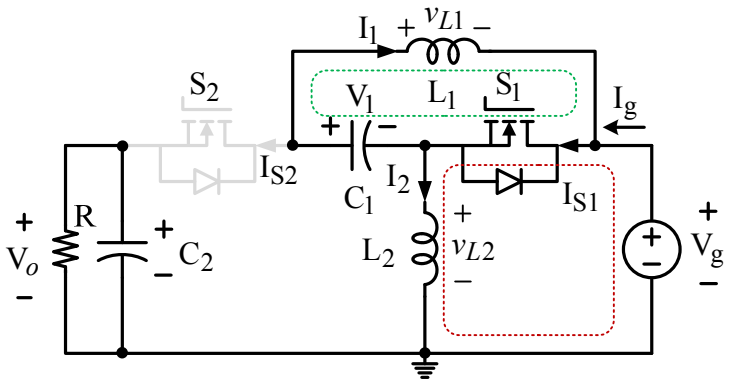
Figure 8.11 shows the typical waveforms of Z-source dc-dc converter in buck-boost mode. S1 and D2(S2) show the conduction time of two switches. The inductor current I1 and I2 are positive, because the real inductor current is the same with the reference inductor current as marked in Figure 8.7. The switch current I_{S1} and I_{S2} are the sum of the inductor current I1 and I2. During the buck-boost mode, S2 can be replaced by a diode D2, so the current I_{S2} is negative, which is the opposite of the reference current I_{S2} as marked in Figure 8.7. Output voltage is negative, and can be changed from zero to negative infinity with the change of duty cycle.

8.3.3 Zero Output Voltage Mode (D=0.5)

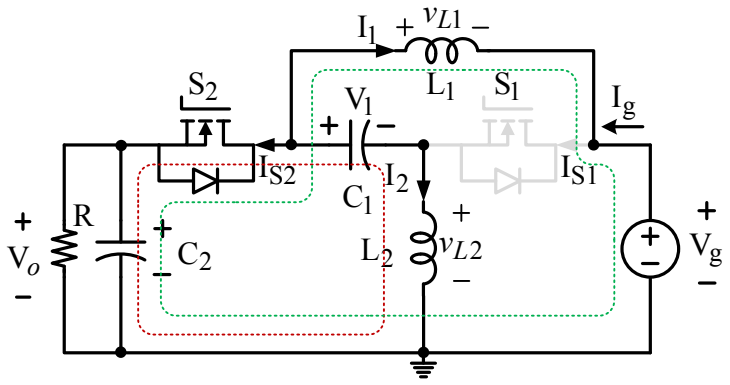
When the duty cycle is equal to 0.5, this Z-source dc-dc converter can output zero voltage. During this mode, the average value of the output capacitor voltage is zero, it still have ac voltage ripples. The average value of the inductor L1 and L2 current is also zero; the inductors still have ripple current. Two active switches with bi-directional current flow capability have to be utilized in this mode, since the ac ripple current of the inductor have to flow from both of the switches. During this mode, only the inductor ac ripple current can cause the power loss of the switches and the inductors. Although the output power is zero during this mode, the standby power loss is not high. The zero output voltage mode of Z-source dc-dc converter is totally different from the traditional buck or boost converter, since the two switches is controlled to output zero voltage. This means these converters can be control as a constant current load with zero dc voltage. By using this feature, the quasi-Z-source dc-dc converter shown in Figure 8.3(b) can be used as the ZVEL, which will be discussed in detail in section VII.

Figure 8.12 shows the two switching states of the zero output voltage mode. Figure 8.12(a) shows the situation when the switch S1 is turned on. There are two current loops in this state. The real current direction of both inductors L1 and L2 will change from negative to positive

corresponding to the reference direction as shown in Figure 8.13. During this switching state, the inductor L1 and L2 will charge the capacitor C1 and the input voltage source. After the inductor current decreases to zero, these two inductors will be charged by the capacitor C1 and the input voltage source. Only circulating current exists in this state. Figure 8.12(b) shows the situation when the switch S2 is turned on. Similarly to the last switching state, there are also two current loops as marked in the figure. And the real current direction of both inductors will change from positive to negative. During this switching state, the energy stored in the inductor L1 and L2 will transfer to the input voltage source or capacitor C1. And then the input voltage source and the capacitor C1 will charge the inductor L1 and L2 in the other direction.



(a)



(b)

Figure 8.12 Two switching states of Z-source dc-dc converter in zero voltage output mode. (a) switch S1 is on; (b) switch S2 is on.

Figure 8.13 shows the typical waveforms of Z-source dc-dc converter in zero output voltage mode. S1 and S2 show the control signal of the two switches. The dc current of inductor I1 and I2 is zero, but the inductors still have ripple current. The switch current I_{S1} and I_{S2} are the sum of the inductor current I1 and I2. And the direction of the switch current will also change during one switching state since only inductor ac current flows through the switches. The dc value of the output voltage is zero. Assume the output capacitor is large enough; the ac ripple of the output capacitor is small. Therefore, the output voltage ac ripple is not marked in the Figure 8.13.

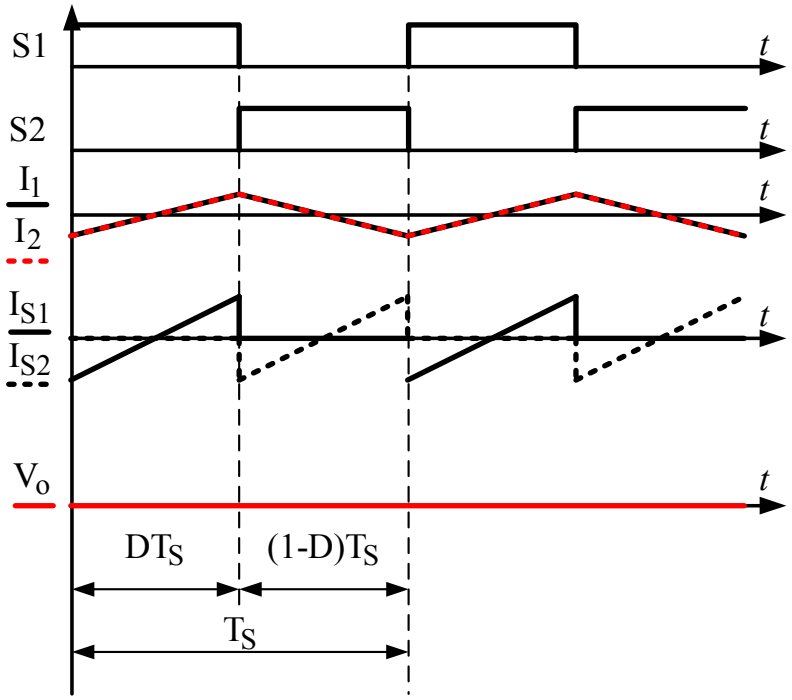


Figure 8.13 Typical waveforms of Z-source dc-dc converter in zero output voltage mode (D=0.5). The current and voltage reference direction is according to the marked direction in Figure 8.7.

The Z-source dc-dc converters in Figure 8.1(b) ~ Figure 8.6(b) have the similar dc operation mode as discussed in this section. The other six Z-source dc-dc converters in Figure 8.1(a) ~ Figure 8.6(a) have three different operation modes: boost mode, buck-boost mode, and prohibited mode. Since these converters are the inverse converters as discussed in this section,

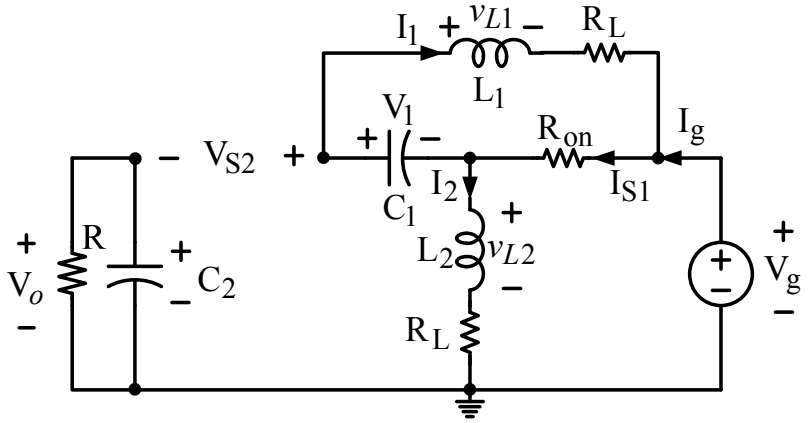
the dc operation can be derived accordingly, which will not be discussed in detail in this chapter. When the duty cycle is equal to 0.5, these converters enter into prohibited mode. In this mode, all the input power becomes power loss of the circuit, which is similar to the boost or buck-boost converter with unity duty cycle. So the 0.5 duty cycle of the Z-source dc-dc converters in Figure 8.1(a) ~ Figure 8.6(a) should be prohibited.

8.4 Converter Voltage Gain Analysis

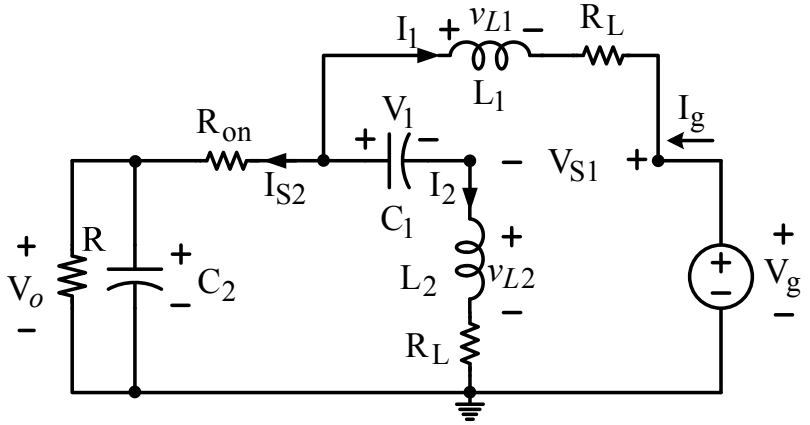
In this section, the Z-source dc-dc converter voltage gain (output voltage over input voltage) in ideal case and non-ideal case considering the circuit power loss will be analyzed. The Z-source dc-dc converters in Figure 8.1(a) ~ Figure 8.6(a) have the same voltage gain, and the Z-source dc-dc converters in Figure 8.1(b) ~ Figure 8.6(b) have the same voltage gain. The Z-source dc-dc converter in Figure 8.6(b) is used as an example for the voltage gain analysis, other converter voltage gain can be derived in a similar manner.

Figure 8.14 shows the two switching states of Z-source dc-dc converter in Figure 8.6(b) considering the inductor power loss and the switch conduction loss. Figure 8.14(a) shows the case when the switch S1 is turned on, Figure 8.14(b) shows the case when the switch S2 is turned on. The reference of voltage polarity and current direction for the following analysis is also marked in the figure. Assume the input voltage is Vg, the voltage across the capacitor C1 is V1, the voltage across C2 is Vo, the current through L1 is I1, the current through L2 is I2. Define the conduction of S1 is duty cycle. R_L is added in series with the inductor to represent the inductor power loss, and R_{on} is added to represent the switch turn on resistance. Assume the R_L of inductor L1 and L2 is the same, and the R_{on} of switch S1 and S2 is the same. Although these resistors cannot represent all the power loss in the circuit, they already can reflect the trend of

voltage gain curve with the increase of power loss. The infinity voltage gain will not exist in the circuit; the peak voltage gain will be limited by the power loss of the circuit.



(a)



(b)

Figure 8.14 Two switching states of Z-source dc-dc converter in Figure 8.6(b) considering the inductor power loss and the switch conduction loss. (a) S1 is on, S2 is off. (b) S2 is on, S1 is off.

According to the inductor voltage-second balance equation on L1 and L2 and the capacitor charge balance equation on C1 and C2, one has

$$\begin{cases} (V_1 - I_1 R_L - (I_1 + I_2) R_{on}) D + \\ (V_o - V_g - I_1 R_L - (I_1 + I_2) R_{on})(1 - D) = 0 \\ (V_g - I_2 R_L - (I_1 + I_2) R_{on}) D + \\ (V_o - V_1 - I_2 R_L - (I_1 + I_2) R_{on})(1 - D) = 0 \\ -I_1 D + I_2 (1 - D) = 0 \\ \left(-\frac{V_o}{R}\right) D + \left(-I_1 - I_2 - \frac{V_o}{R}\right)(1 - D) = 0 \end{cases} \tag{8.1}$$

By solving the equations in (8.1), one can get

$$M(D) = \frac{V_o}{V_g} = \frac{(1 - D)(1 - 2D)}{\frac{R_{on}}{R} + \frac{R_L}{R}\left(1 - 2D + 2D^2\right) + (1 - D)^2} \tag{8.2}$$

Define

$$\frac{R_{on}}{R} = k_1, \ \frac{R_L}{R} = k_2 \tag{8.3}$$

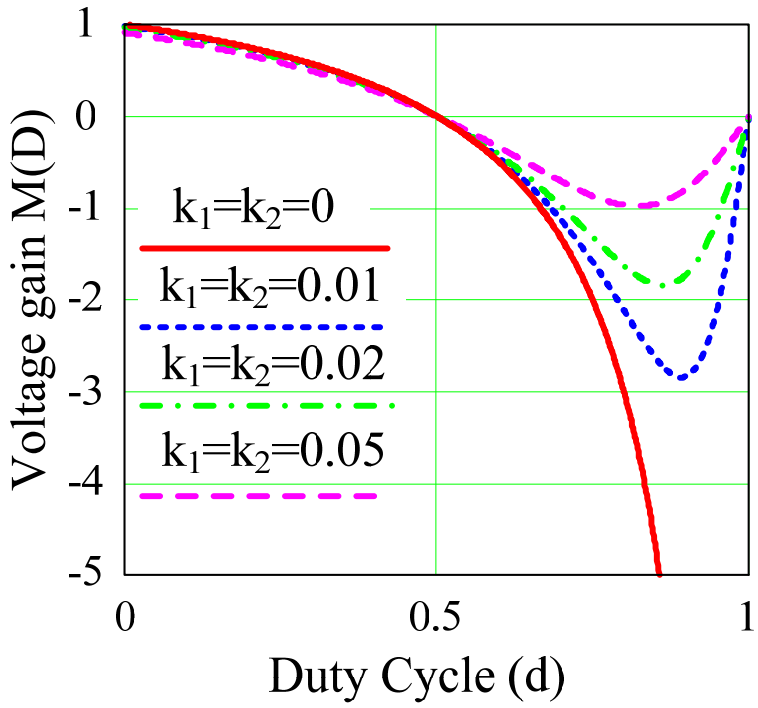
k1 and k2 can be considered as the power loss coefficient. When k1=k2=0, it is the ideal case without any power loss. Figure 8.15(a) shows the Z-source DC-DC converter voltage gain curves as derived in (8.2), considering converter power loss. The peak converter voltage gain will reduce with the increase of k1 and k2. When the duty cycle is equal to 0.5, these converters can output zero voltage. When the duty cycle is one, the converter voltage gain equals to zero instead of negative infinity. The unity duty cycle should be prohibited, since all the input power becomes power loss at this point.

Similarly, the voltage gain curve considering the inductor and the switch power loss of Z-source dc-dc converter in Figure 8.6(a) can also be derived as,

$$M(D) = \frac{V_o}{V_g} = \frac{(1 - D)(1 - 2D)}{k_1 + k_2\left(1 - 2D + 2D^2\right) + (1 - 2D)^2} \tag{8.4}$$

Figure 8.15(b) shows the voltage gain curve of Z-source dc-dc converter in Figure 8.6(a) after considering the power loss. As shown in Figure 8.15(b), in ideal case when k1 = k2 = 0, the

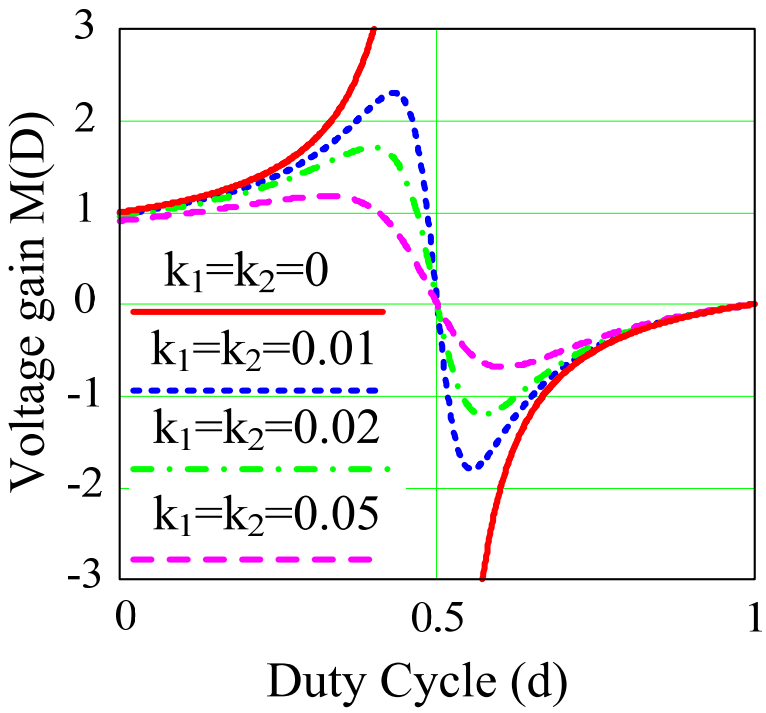
converter voltage gain is discontinuous at the 0.5 duty cycle point. But considering the circuit power loss, which means k1 and k2 are not zero, the converter voltage gain is actually zero at the 0.5 duty cycle. The 0.5 duty cycle should be prohibited for the converter in Figure 8.6(a), since all input power becomes power loss at this point.



(a)

Figure 8.15 Z-source dc-dc converters voltage gain in ideal and non-ideal case considering converter power loss.

Figure 8.15 cont'd



(b)

8.5 Device Stress Analysis and Passive Components Design Guidelines

In this section, the switching device voltage stress and current stress will be analyzed. In order to output positive and negative voltage at the same time, RB-IGBT or IGBT with anti-parallel diode have to be used for different Z-source dc-dc converters. The correct switching device that should be used for each topology will be explained here. Passive component design guidelines will also be provided.

8.5.1 Switching Device Voltage and Current Stress

The Z-source dc-dc converter in Figure 8.6(b) will also be used as an example to analyze device voltage stress. The definition of power device voltage stress polarity is shown in Figure

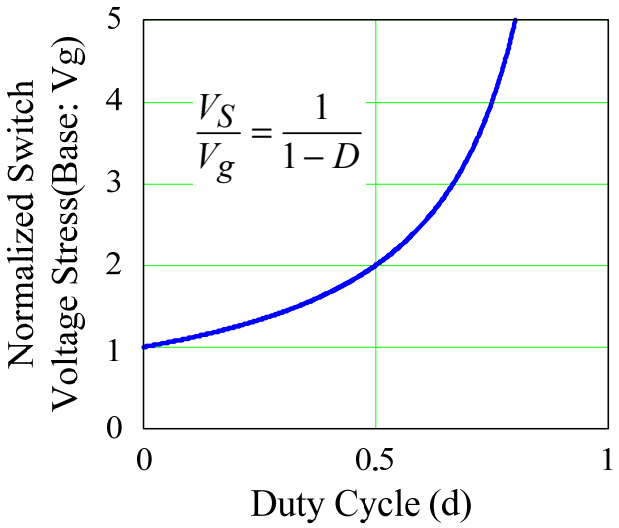
8.14. The device stress analysis can be derived assuming k1 = k2 = 0 without losing generosity, since the device stress polarity is the major concern to select the correct switching device. With different switches are turned on, the voltage V_{S1}, V_{S2} can be derived as,

$$V_{S1} = V_{S2} = V_1 + V_g - V_o = 2V_g - V_o = \frac{V_g}{1-D} \tag{8.5}$$

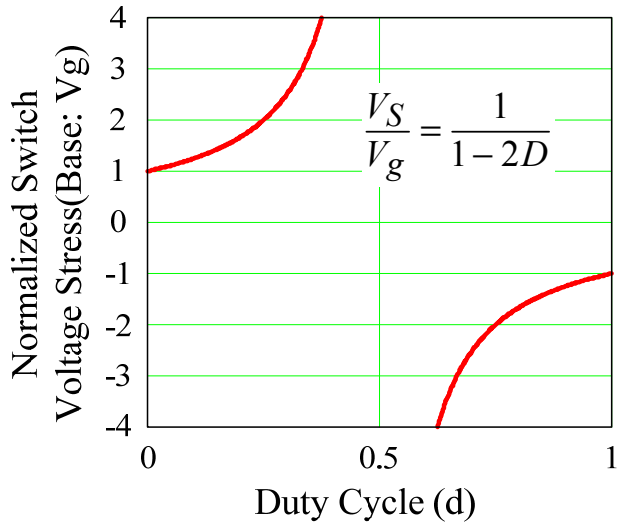
By exchanging the input voltage source and the output capacitor without changing the voltage reference and current direction of Figure 8.14, one can derive the switch voltage stress of Z-source dc-dc converters in Figure 8.6(a) using the following equations,

$$V_{S1} = V_{S2} = 2V_o - V_g = \frac{V_g}{1-2D} \tag{8.6}$$

From (8.5) and (8.6), the device voltage stress of different Z-source converters in terms of duty cycle can be draw in Figure 8.16. Figure 8.16(a) shows the normalized switch voltage stress curve of Z-source dc-dc converter in Figure 8.6(b). The base voltage is input voltage Vg. So the switch voltage stress of the Z-source dc-dc converter shown in Figure 8.6(b) will not change polarity when the duty cycle changes from 0 to 1. Figure 8.16(b) shows the normalized switch voltage stress curve of Z-source dc-dc converter in Figure 8.6(a). The voltage across the switch will change the polarity when the duty cycle is 0.5. In order to operate the duty cycle from 0 to 1, a bi-polar voltage blocking device should be used.



(a)



(b)

Figure 8.16. (a) Normalized switch voltage stress of the converter in Figure 8.6(b). (b)Normalized switch voltage stress of the converter in Figure 8.6(a)

According to the capacitor charging balance of C1and C2 in (8.1) one can derive

$$I_1 = \frac{V_g(2D-1)}{R(1-D)} \tag{8.7}$$

$$I_2 = \frac{V_g D(2D-1)}{R(D-1)^2} \tag{8.8}$$

Figure 8.17 shows the normalized inductor current stress of Z-source dc-dc converter in Figure 8.6(b) with the change of duty cycle. The base current is V_g/R.

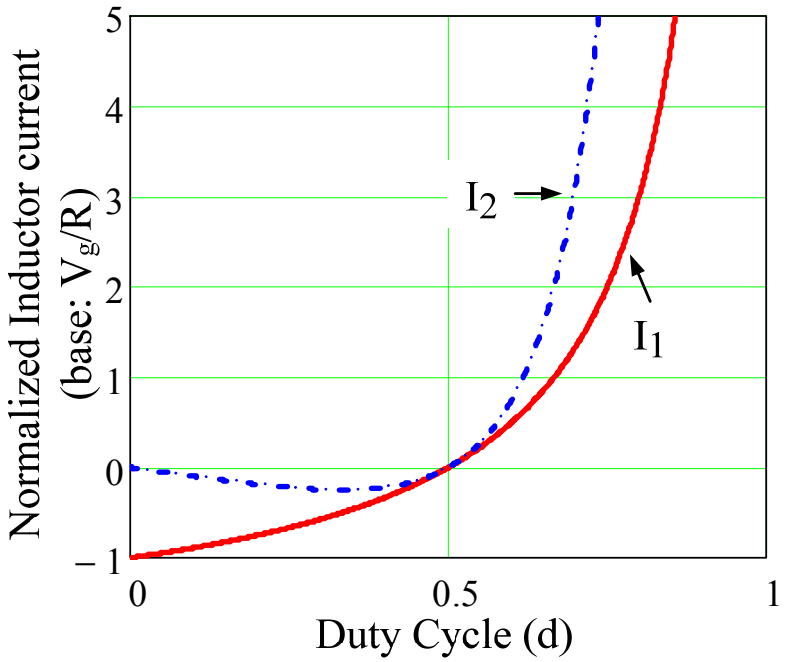


Figure 8.17. Normalized inductor current of Z-source dc-dc converter in Figure 8.6(b).

The current flowing through S1 and S2 is

$$I_{S1} = I_{S2} = I_1 + I_2 \tag{8.9}$$

Plug (8.7) and (8.8) into (8.9), one can get,

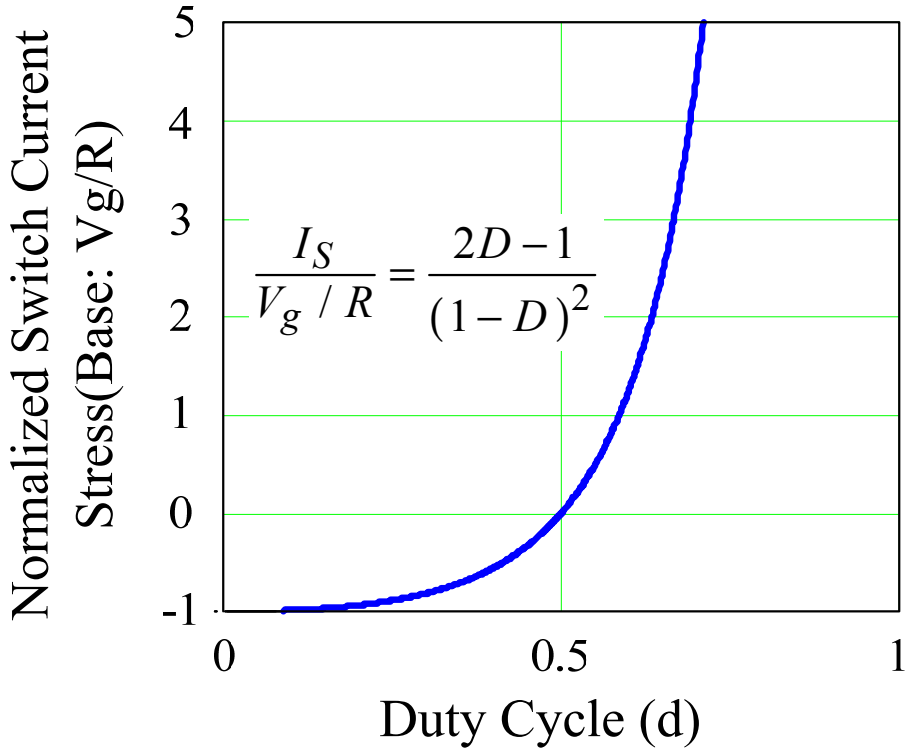
$$I_{S1} = I_{S2} = \frac{V_g(2D-1)}{R(D-1)^2} \tag{8.10}$$

The current stress of switches of Z-source dc-dc converter in Figure 8.6(a) can be derived in a similar manner as follows,

$$I_{S1} = I_{S2} = \frac{V_g(1-D)}{R(2D-1)^2} \tag{8.11}$$

Figure 8.18(a) shows the normalized switch current stress of Z-source dc-dc converters in Figure 8.6(b) with the change of duty cycle. The base current is V_g / R. So, the device current

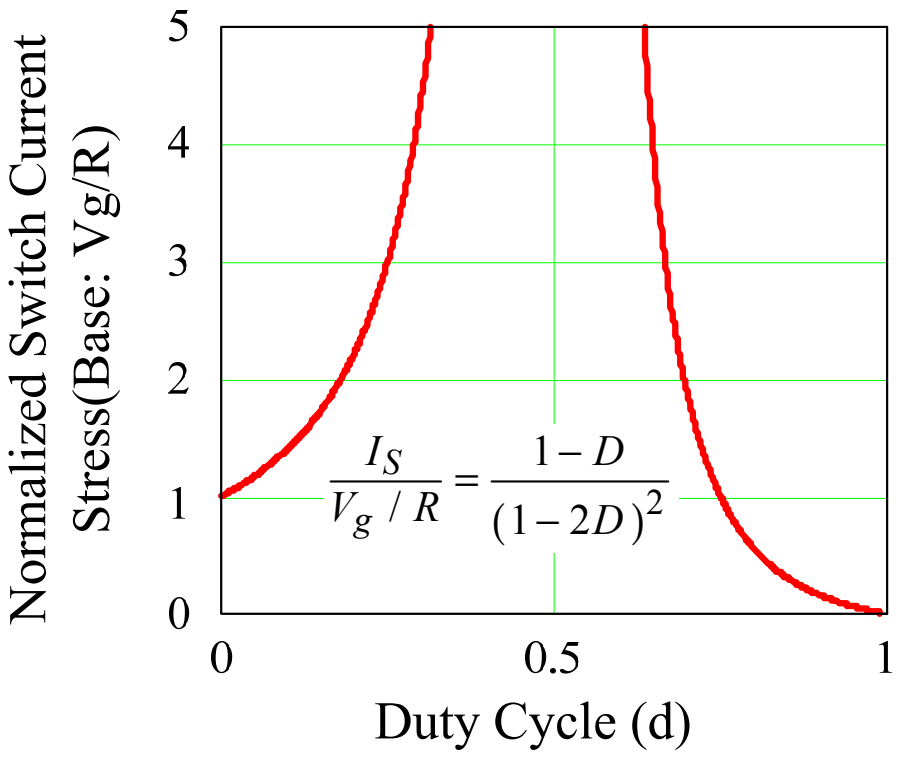
stress of Z-source dc-dc converter in Figure 8.6(b) will change direction when the duty cycle is equal 0.5. This means a bi-directional current flowing device has to be used to operate the duty cycle in the full range. Figure 8.18(b) shows the normalized switch current stress of Z-source dc-dc converter shown in Figure 8.6(a). The current through the switch will change the polarity when the duty cycle changes from 0 to 1.



(a)

Figure 8.18. (a) Normalized switch current stress of the converter in Figure 8.6(b). (b)Normalized switch current stress of the converter in Figure 8.6(a)

Figure 8.18 cont'd



(b)

From the switch voltage stress and current stress analysis as shown in Figure 8.16 and Figure 8.18, the correct device can be chosen to operate at full duty cycle range. For the Z-source dc-dc converter in Figure 8.6(b), a bi-directional current flow and uni-polar voltage blocking device, such as IGBT with anti-parallel diode or MOSFET can be used. The voltage stress of the device is always positive during the full duty cycle range, but the current stress of the device changes from negative to positive. For the Z-source dc-dc converter in Figure 8.6(a), a uni-directional current flow and bi-polar voltage blocking device, such as RB-IGBT or IGBT with a series diode should be used. The current flow through the device is always positive during the full duty cycle range, but the voltage across the device changes polarity. The device stress analysis of other Z-source dc-dc converters can be derived in the similar way.

8.5.2 Passive Components Design Considerations

The Z-source dc-dc converter in Figure 8.6(b) is still used as an example for the passive components design considerations. The voltage ripple of capacitor C1 can be derived as,

$$\Delta V_{C1} = \frac{V_g T_S (1-2D) D}{RC_1 (1-D)} \tag{8.12}$$

The voltage ripple of capacitor C2 can be derived as,

$$\Delta V_{C2} = \frac{V_g T_S (2D-1) D}{RC_2 (1-D)} \tag{8.13}$$

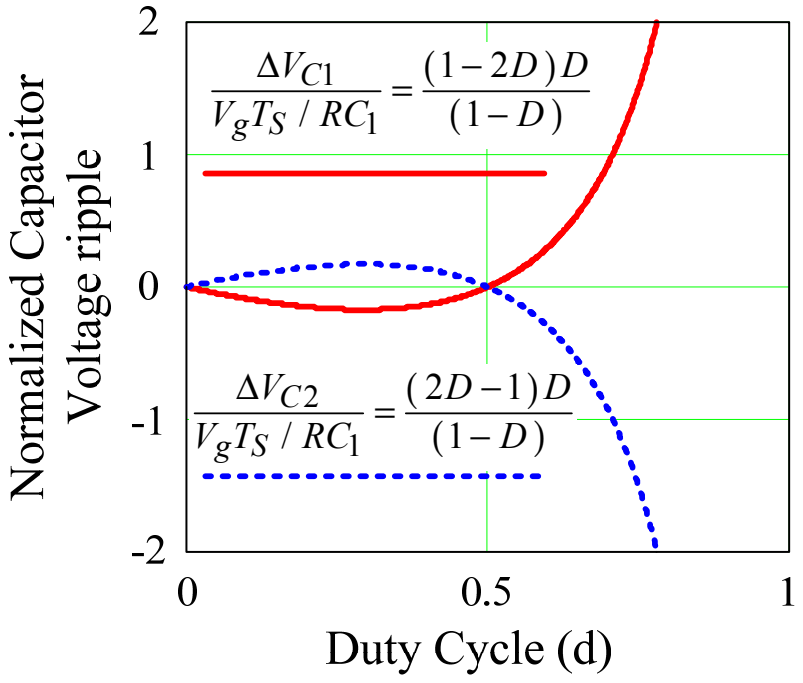
Ts is the switching frequency. The normalized capacitor voltage ripple can be shown in Figure 8.19(a).

The current ripple of inductor L1 and L2 can be derived as,

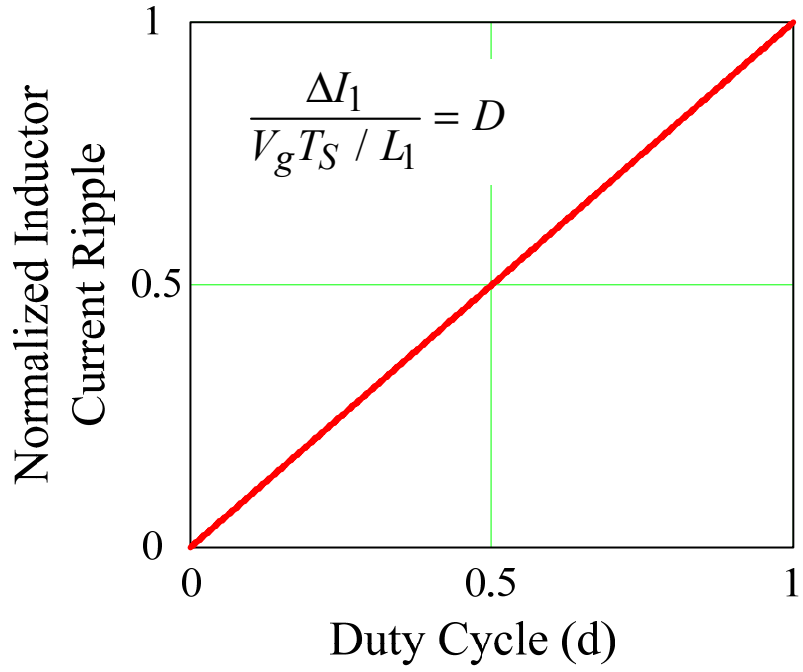
$$\Delta I_1 = \Delta I_2 = \frac{V_g D T_S}{L_1} \tag{8.14}$$

So the inductor current ripple is a linear relationship with the duty cycle which can be shown in Figure 8.19(b).

The capacitance and the inductance value can be designed using (8.12), (8.13), (8.14). When the duty cycle operation range is determined, the capacitance and the inductance value can be chosen considering the peak voltage and current ripple.



(a)



(b)

Figure 8.19. (a) Normalized capacitor voltage ripple of Z-source dc-dc converter in Figure 8.6(b). (b) Normalized inductor current ripple of Z-source dc-dc converter in Figure 8.6(b)

8.6 Proposed Converter Four-quadrant Operation for DC Motor Drive

Figure 8.20 shows typical situation of using four-quadrant dc-dc converter for dc motor drive. The first and third quadrant are the motoring quadrant, the energy is transferred from the input voltage source to the motor. The second and fourth quadrant are the regeneration quadrant, the energy is transferred from motor to the input voltage source. In the first and second quadrant, the equivalent output voltage of the motor is positive. In the third and fourth quadrant, the equivalent output voltage of the motor is negative. In order to drive the dc motor operating at quadrant I and II, a bi-directional dc-dc converter with positive output voltage is required. In order to drive the motor at quadrant III and IV, a bi-directional dc-dc converter with negative output voltage is required. Therefore, a dc-dc converter with bi-directional current and bi-polar output voltage is required for the dc motor four-quadrant operation.

The proposed Z-source dc-dc converters are able output bi-polar voltage and provide bi-directional current at the same time. By using two active switching devices (MOSFET) with its anti-parallel diode, these converters are able to achieve four-quadrant operation. If only the first and the fourth quadrant operation are needed, one active switch and a diode is enough as shown in Figure 8.21. Figure 8.21(a) shows the Z-source dc-dc converter in Figure 8.7(b) operated at the first quadrant. The real voltage and current direction marked in the figure. The dc motor is represented with an ideal voltage source E with internal resistance R. When $0 < D < 0.5$ and the output voltage Vo is positive and larger than the dc motor voltage E, the motor operate at the first quadrant. During this mode, the power is transferred from the input voltage source to the motor. Figure 8.21(b) shows the Z-source dc-dc converter operated at the forth quadrant. In this

quadrant, the output voltage of the dc-dc converter and the motor are both negative. When 0.5 < D < 1 and the output voltage Vo is smaller than the dc motor output voltage E, the motor operated at the fourth quadrant. During this mode, the energy is transferred from the motor to the input voltage source.

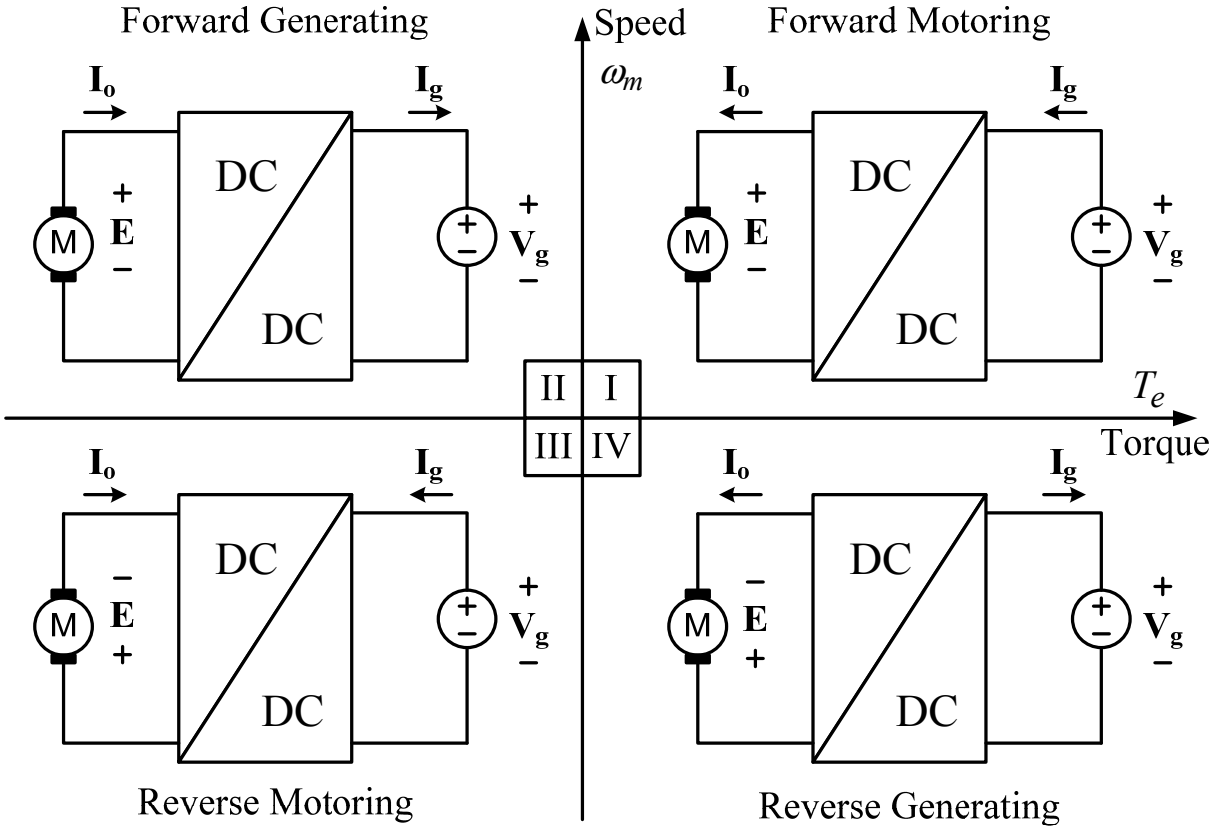
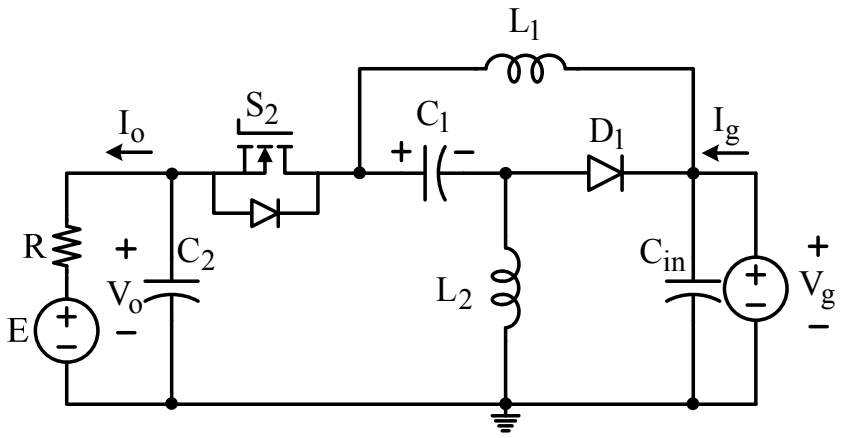
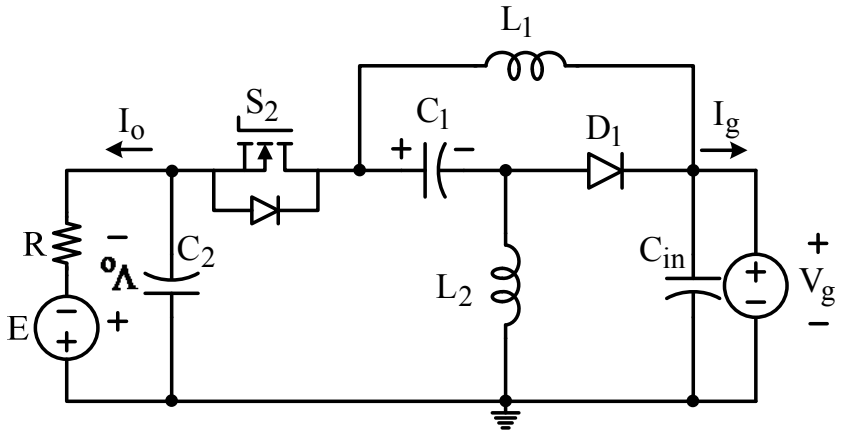


Figure 8.20 Four quadrant operation of DC motor



(a)

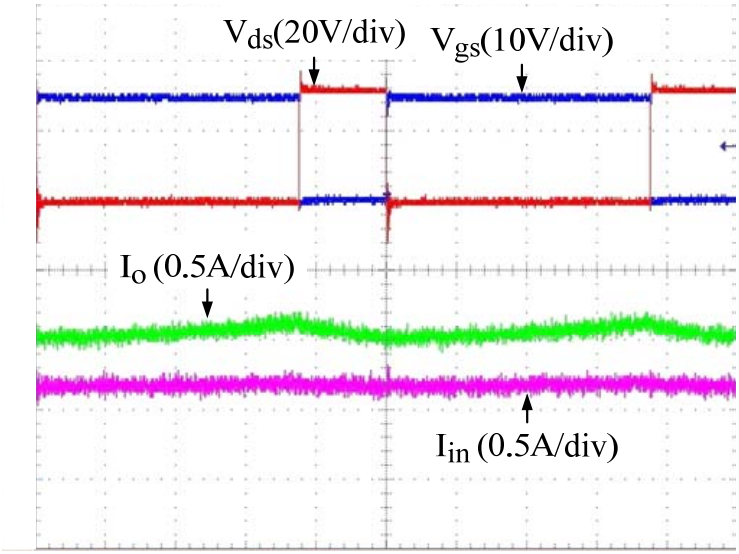


(b)

Figure 8.21 (a)Z-source dc-dc converter in the first quadrant operation mode. (0 < D < 0.5, E<Vo). (b) Z-source dc-dc converter in the fourth quadrant operation mode. (0.5 < D < 1, |E|>|Vo|)

A Z-source dc-dc converter prototype is built to verify the bi-polar output voltage features and its operation at the first and the fourth quadrant. Figure 8.21 shows the circuit topology used in experiment. Only an active switch and a diode are needed for the first and the fourth quadrant operation. The input voltage V_g =24V, the power is 40W, and the switching frequency is 50KHz. E could be a dc motor that is able to operate at positive and negative voltage. Figure 8.22 shows the experimental waveforms of quadrant 1 operation while D<0.5. One should notice that the duty cycle is defined using switch S1 which is already replaced by a diode in the experiment

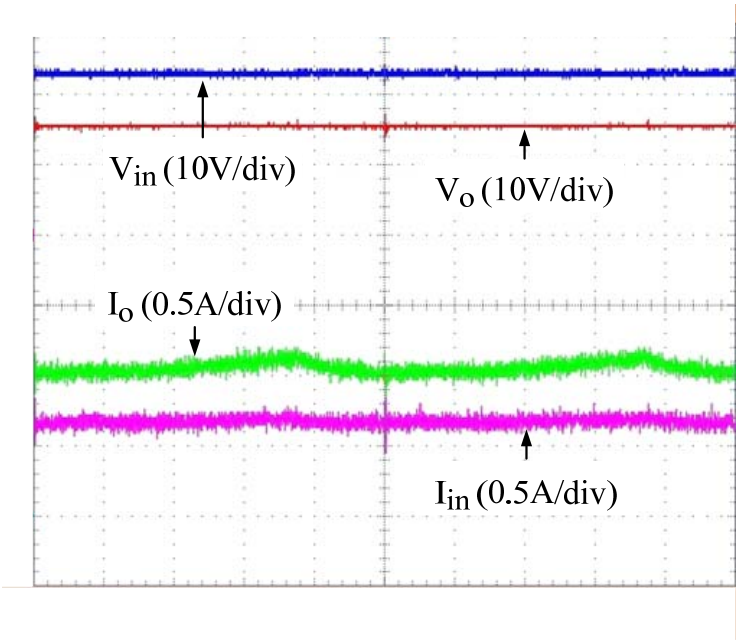
circuit. Vgs is the gate drive signal of switch S2, Vds is the drain source voltage of switch S2. Iin and Io are the input and output current. Vin and Vo are the input and output voltage. The reference direction is marked in Figure 8.21(a). In the quadrant 1 operation, the input voltage and the output voltage are positive, the input current and the output current are also positive. Figure 8.23 shows the experimental waveforms of quadrant 4 while D>0.5. Vgs and Vds are still the gate drive signal and drain source voltage of switch S2. In the quadrant 4 operation, the input voltage is positive, the output voltage is negative, as shown in Figure 8.23(b). The input and output current are both positive since the reference input current direction in Figure 8.21(b) is reversed.



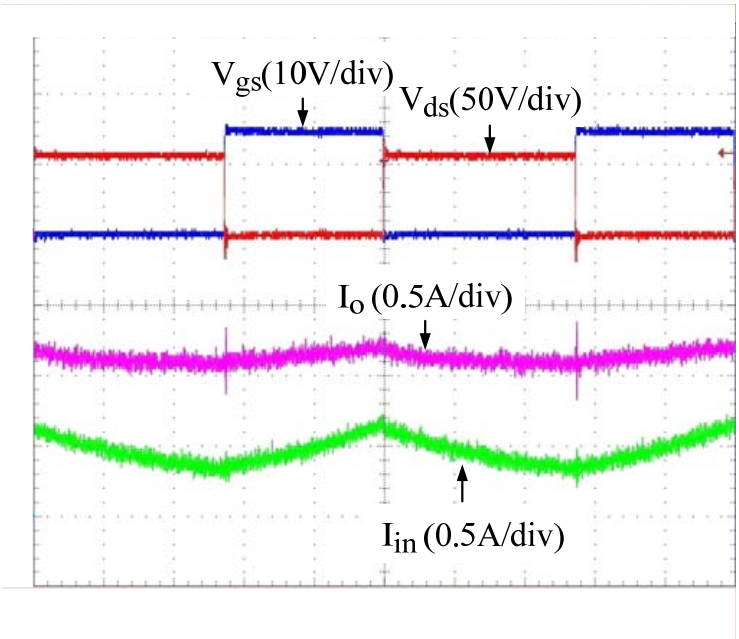
(a)

Figure 8.22. Experiment waveforms of the proposed converter shown in Figure 8.7(b) operated at quadrant 1 (0<D<0.5).

Figure 8.22 cont'd



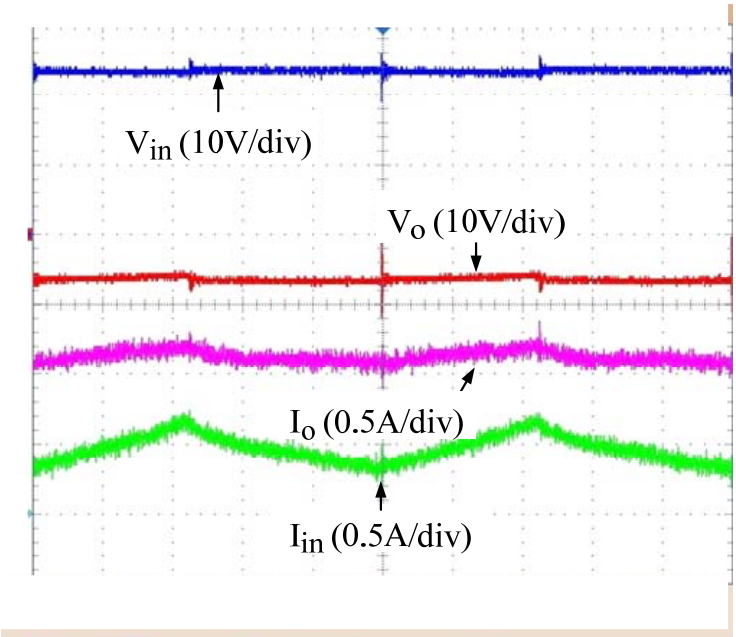
(b)



(a)

Figure 8.23. Experiment waveforms of the proposed converter shown in Figure 8.7(b) operated at quadrant 4 (1>D>0.5).

Figure 8.23 cont'd



(b)

8.7 Quasi-Z-source DC-DC Converter as ZVEL

The proposed quasi-Z-source converter shown in Figure 8.3(b) can behave like an ideal current source. That means they can only draw current from the testing PV panel while keep the voltage across the testing panel be zero. So these circuits can be used as the ZVEL. Figure 8.24 shows the quasi-Z-source converter in Figure 8.3(b) as the ZVEL testing system as an example.

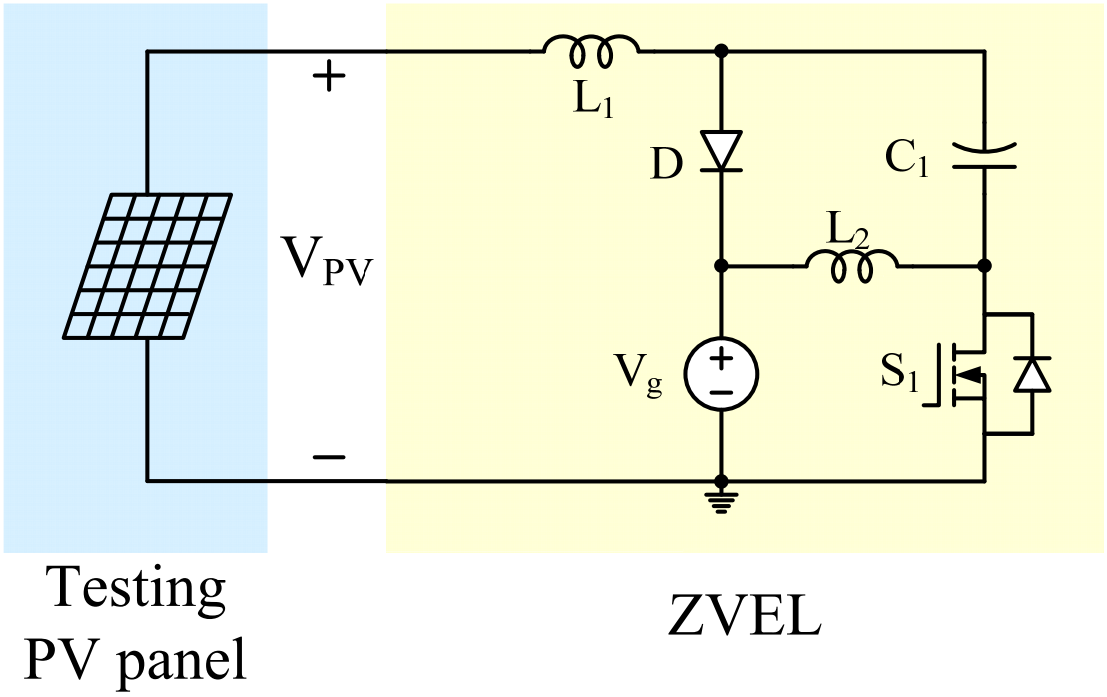


Figure 8.24 ZVEL testing system using quasi-Z-source dc-dc converter.

Figure 8.25 shows the quasi-Z-source dc-dc converter as the ZVEL prototype testing circuit. In order to test the output current capability when testing PV panel voltage is zero, we can use a short circuit to represent it. By considering the internal resistance of the inductor, we can derive the testing current through the PV panel (the inductor L1 current) using inductor voltage-second balance and the capacitor charging balance equations as follows:

$$I_{TEST} = \frac{V_g}{R_L} \cdot \frac{(2D-1)(1-D)}{2D^2 - 2D + 1} \tag{8.15}$$

where Vg is the input voltage and Vg=5 V in the prototype, R_L is the internal resistance of the inductor which is about 25 mΩ. D is the duty cycle defined by the conduction time of S1. C1=470 μF, L1=L2=63 μH.

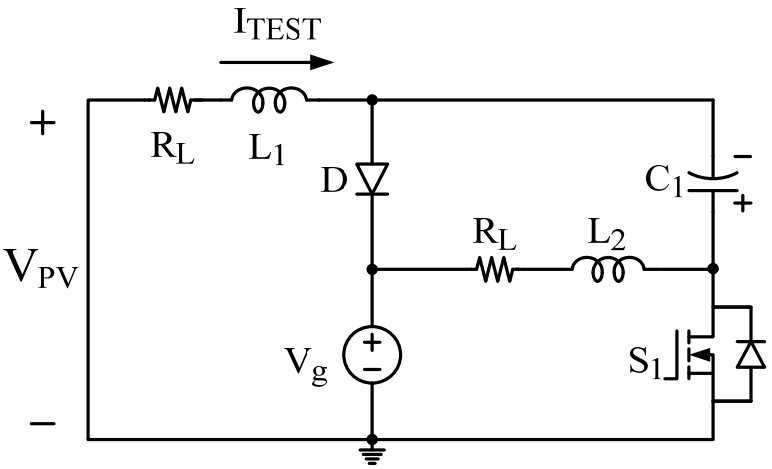


Figure 8.25 quasi-Z-source dc-dc converter as ZVEL experiment verification circuit.

Figure 8.26 shows the relationship between the I_{TEST} and duty cycle using (8.15) when $V_{PV} = 0$. When the duty cycle changes from 0.5 to 1, a positive current can be draws from the testing panel, which can be considered as an ideal current source controlled by the duty cycle.

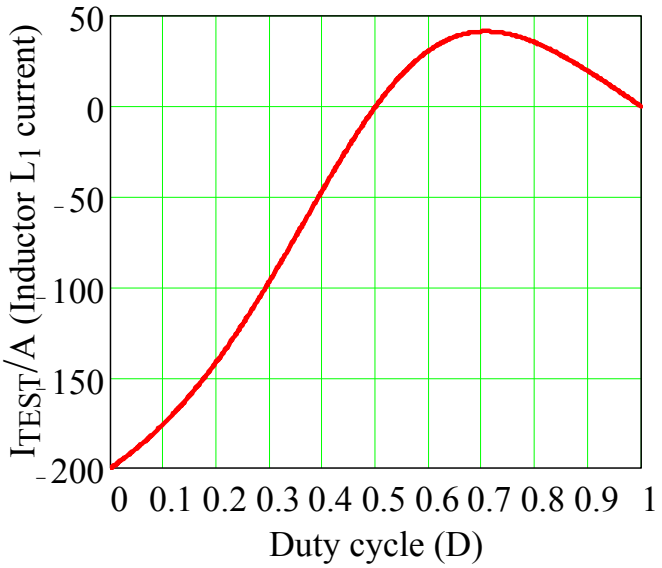
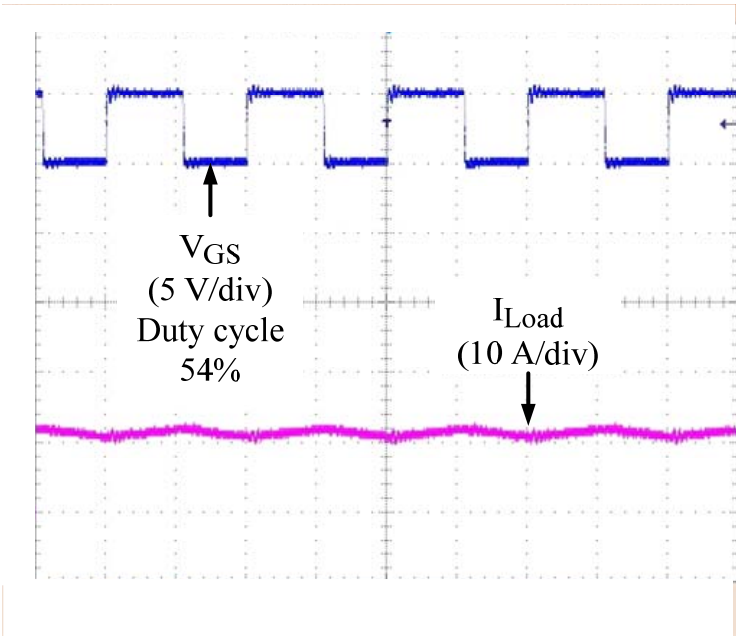


Figure 8.26 Testing current and duty cycle relationship when testing voltage is zero.

Figure 8.27 shows the experiment result of the quasi-Z-source ZVEL prototype experiment results. With the change of duty cycle, different current can be drawn from the testing panel with V_{PV} =0, which shows the ideal current source feature.



(a)

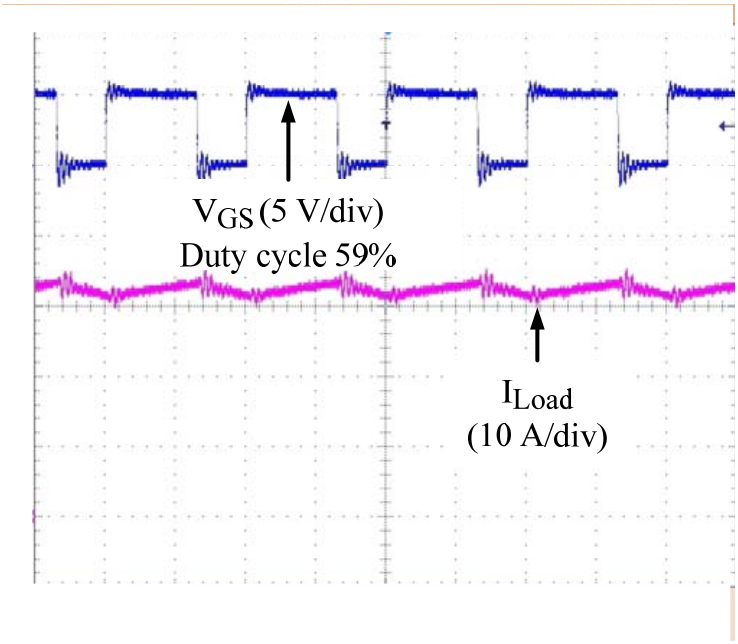


Figure 8.27. Experiment waveforms of the quasi-Z-source dc-dc converter as ZVEL.

8.8 Conclusion

A family of Z-source and quasi-Z-source dc-dc converters with special features has been proposed in this chapter. A systematic topology derivation method is introduced. The proposed

topologies including other existing topologies with similar features are derived and summarized. By only using two active switching devices, the proposed converters can output positive voltage and negative voltage with the change of duty cycle. These converters can provide four-quadrant operation for dc motor drive with minimal number of switching devices and passive components. By providing proper modulation strategy, these converters can also be used as a doubly grounded grid-tied PV inverters or bridge-less PFC [226]. Some of the circuits can output zero voltage when the duty cycle is 0.5, which can be used as a ZVEL for PV arrays testing. Two prototypes have been built and tested to verify the first and forth quadrant operation for dc motor drive and ZVEL feature for PV array test. Experimental results are provided.

CHAPTER 9
Low Cost Semi-Z-source Inverter for Single-Phase Photovoltaic Systems

This chapter presents several non-isolated semi-Z-source inverters for single-phase photovoltaic system with low cost and doubly grounded features. These semi-Z-source inverters employ the Z-source/quasi-Z-source network and only two active switches to achieve the same output voltage as the traditional voltage-fed full-bridge inverter does. The two active switches of the semi-Z-source inverter are controlled complementarily. Different from the traditional single-phase Z-source/quasi-Z-source inverter, shoot-through zero state is not applicable to the semi-Z-source inverter. The input dc source and the output ac voltage of the semi-Z-source inverter share the same ground, thus leading to less leakage ground current advantages over other non-doubly grounded inverters, such as voltage-fed full-bridge inverter. This is a preferred feature for non-isolated grid-connected inverters, especially in photovoltaic application. A revised non-linear sinusoid pulse width modulation method for semi-Z-source inverter is also proposed. By using this method, desired duty cycle can be generated to output the sinusoidal voltage. Other dc-dc converters with similar voltage gain curve, which can also be used as a single-phase inverter are also discussed and summarized. A single-phase semi-Z-source inverter prototype is built; experimental results are provided to verify and demonstrate the special features of the proposed circuit.[9]

9.1 Introduction

[9] This work has been presented in part in *Applied Power Electronics Conference and Exposition, 2011. APEC 2011. Twenty-Sixth Annual IEEE, 2011. And it is* accepted for publication on *IEEE Trans. Power Electron. 2011*

In recent years, due to the energy crisis, renewable energy distributed power generator (DG), such as wind turbine, photovoltaic (PV) cell, fuel cell, and thermoelectric generation (TEG) modules are becoming more and more popular in industrial and residential applications [227]. Many renewable energy DGs such as, PV cell, fuel cell and TEG module can only output dc voltage, so an inverter interface has to be utilized for grid connected applications [228, 229]. Many inverter topologies have been proposed and reviewed recently [230-238].

Based on the galvanic isolation, these inverters can be divided into two categories: isolated inverters and non-isolated inverters. Isolated inverters usually utilize a line frequency or high frequency transformer for electrical isolation. Due to the size, weight and cost considerations, high frequency transformers are inclined to be used for future applications [233]. For the inverter topologies with high frequency transformer, there are several popular approaches. The first approach is the single stage isolated buck-boost inverter or flyback inverter [239-248]. This approach usually utilizes less switching devices, and is able to eliminate electrolytic capacitors by using high voltage low capacitance film or ceramic capacitor for energy storage [233, 240-243]. The second approach is a two stage approach, with an isolated dc-dc converter in the first stage and a full bridge inverter in the second stage [249-257]. A high efficiency high voltage gain dc-dc converter with soft switching can be designed for the first stage [236, 256]. The second full bridge inverter stage can utilize high frequency switches with PWM strategy or line frequency switches just for voltage inversion purposes based on different topologies. The third approach is also a two stage approach with a high frequency dc-ac inverter, a high frequency transformer and an ac-ac converter [236, 258]. Transformer isolated topologies usually have higher voltage gain and safety advantages, but they require more switches with relatively high cost, high complexity and low system efficiency.

In some countries, the galvanic isolation is not a requirement in the low-voltage grid or power levels below 20 kW [259]. This leads to the development of low-cost transformer-less inverter topologies. The transformer-less inverter topologies can be classified into two categories: two stage inverter topologies and single stage inverter topologies [260-275]. The two stage transformer-less inverter topologies are similar in operation to the second approach of the aforementioned transformer isolated topologies. Different from that approach, a non-isolated dc-dc converter is used in the first stage instead. [260-262, 264, 268, 271-273]. In most cases, a full bridge inverter with line frequency switched devices is used in the second stage to reduce the cost and the switching loss. To further simplify the system complexity and to reduce the cost, single stage inverter topologies are investigated. The single stage inverter approach usually consists of two relatively independent dc-dc converters with possible shared passive components and each converter produces a half cycle sinusoid waveform 180° out of phase [236, 263, 265-267, 269, 270, 274]. However, for the transformer-less inverter topologies, if the input dc-source and the grid do not share the same ground, the input dc source, especially for PV cell, may have large leakage current, which will cause safety and EMI problems [232, 259, 276]. In order to solve this problem, either extra switches have to be added to the existing topology which will inevitably increase the cost and system complexity, or doubly grounded topologies have to be used [232, 259, 266, 276-281]. Therefore, for the considerations of safety, cost and system simplicity, the doubly grounded non-isolated inverter topologies are preferred topologies for the renewable DG in grid connected application.

To reduce the cost and to increase the system reliability, Z-source and quasi-Z-source inverter as a single stage transformer-less inverter topology is proposed [190-192]. By utilizing the unique LC network, a shoot-through zero state can be added to replace the traditional zero

state of the inverter and to achieve the output voltage boost function. Many different pulse width modulation strategies have been proposed to control the Z-source inverter or multilevel Z-source inverter based on different methods of placing the shoot-through zero state [205-207, 210-213, 282, 283]. Traditionally, Z-source and quasi-Z-source inverters are applied to the three-phase PV or wind power grid connected generation systems, or three-phase motor drive for HEV application [193, 196, 197, 215, 284-288]. Recently, many Z-source/modified Z-source single-phase inverters have been proposed for PV, motor drive or UPS applications [189, 203, 218, 289-295]. Most of these topologies do not have the aforementioned doubly grounded features except [295]. But [295] only provides the Z-source approach with one cycle control. The control differences of the proposed single phase Z-source inverter with other traditional single-phase Z-source inverter are not discussed. The corresponding quasi-Z-source inverter derived topology is not discussed either.

This chapter presents a family of single-stage non-isolated semi-Z-source inverters that can be used for the aforementioned renewable DG grid-connected application with low cost and doubly grounded features. The proposed circuit can achieve the same output voltage as the traditional voltage fed-full bridge inverter does, with only two active switches. Compared with the traditional single-phase Z-source inverters, the proposed semi-Z-source inverters share the same form of Z-source network. But the Z-source network used in semi-Z-source inverter is in ac side, which is smaller in size than the traditional Z-source network used in dc side. The modulation strategy of the proposed circuit is also different. The traditional Z-source inverters use sinusoidal reference with extra shoot-through reference to output sinusoid voltage and achieve the voltage boost function. However, in order to output sinusoid voltage, the semi-Z-source inverter has to utilize its non-linear voltage gain curve to generate a modified voltage

reference. These differences are the reasons why the author uses the term semi-Z-source inverter to represent the proposed topologies and to distinguish it from the traditional single-phase Z-source inverter. The circuit operation and the modulation strategy of the proposed topology are analyzed in detail and verified by the experimental results.

9.2 Proposed Semi-Z-source/-quasi Z-source Inverters and Topology Derivations

Figure 9.1 and Figure 9.2 show the Z-source and quasi-Z-source dc-dc converters with input and output sharing the same ground [224]. Figure 9.1 shows the Z-source and quasi-Z-source dc-dc converter topologies with discontinuous voltage gain curve, as shown in Figure 9.3(a). Figure 9.2shows the two topologies with continuous voltage gain curve, as shown in Figure 9.3(b). The duty cycle of S1 is defined as D. And the voltage gain equation in terms of D is also shown in Figure 9.3. All of these four topologies can output positive and negative voltage when the duty cycle is changed from 0 to 1. But only the topologies shown in Figure 9.2 can output the positive and negative voltage with continuous voltage gain curve. This means, these two topologies can be used as an inverter by providing proper modulation strategy with the duty cycle D changed from 0 to 2/3. And the output voltage range of the inverter is the same as the full bridge inverter, which is $-V_{in} \sim +V_{in}$. Figure 9.4 shows the proposed single-phase semi-Z-source and semi-quasi-Z-source inverters based on the different impedance network. The semi-Z-source inverter, as shown in Figure 9.4(a) is already discussed in [295]. And this chapter will concentrate on semi-quasi-Z-source inverter and the PWM control strategy. For the proposed semi-Z-source and quasi-Z-source inverter, only two bidirectional current conducting and unidirectional voltage blocking switching devices, such as IGBT and MOSFET are needed for the operation. Because

the voltage gain of the full-bridge inverter is a straight line, the SPWM control strategy can be used to output the sinusoid voltage. The voltage gain of the proposed semi-Z-source inverter is not a straight line as the full-bridge inverter, a modified SPWM strategy has to be used in order to output the sinusoid voltage, which will be discussed in detail in the next two sections.

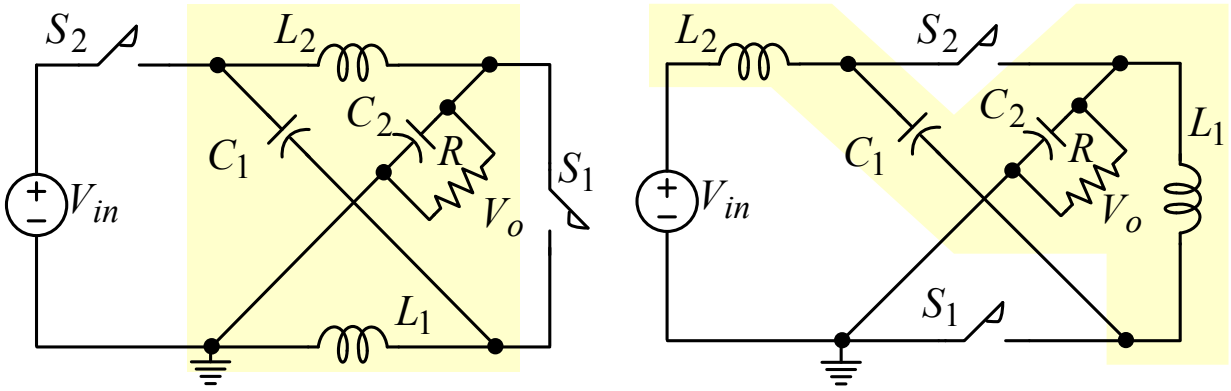


Figure 9.1. Z-source and quasi-Z-source dc-dc converters with discontinuous voltage gain, as shown in Figure 9.3(a).

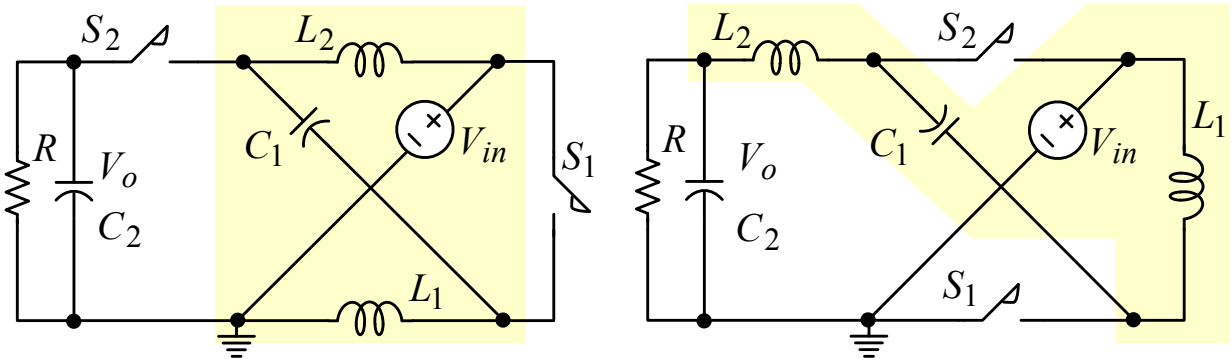


Figure 9.2. Z-source and quasi-Z-source dc-dc converters with continuous voltage gain, as shown in Figure 9.3(b).

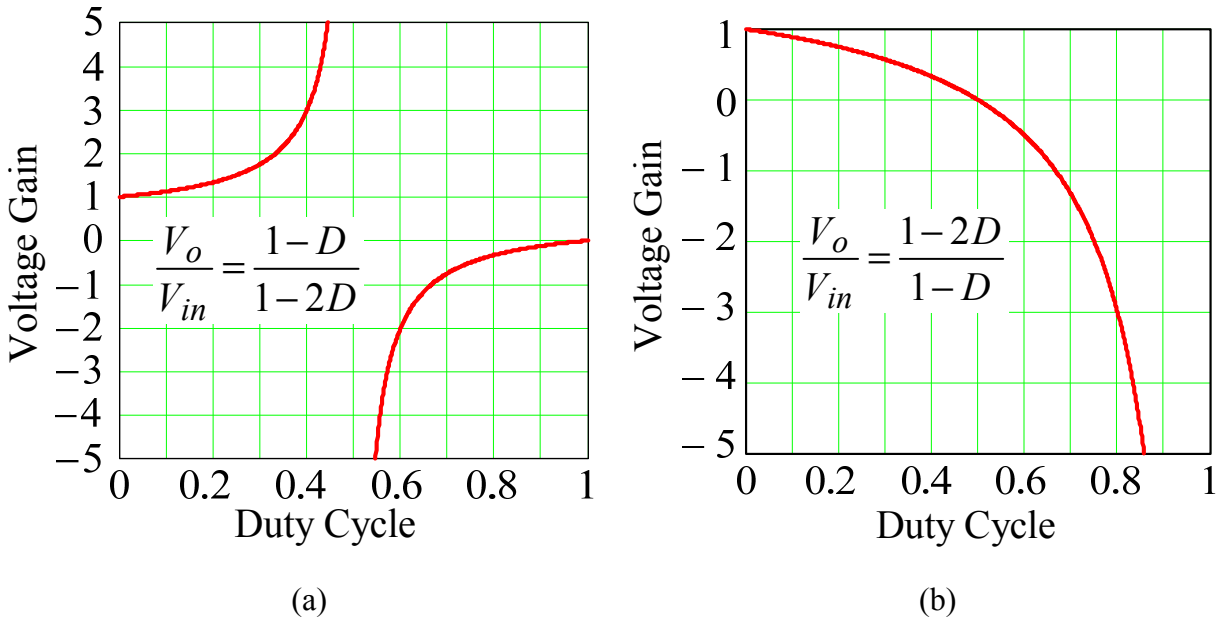


Figure 9.3. Voltage gain curve of Z-source and quasi-Z-source dc-dc converters as shown in Figure 9.1and Figure 9.2.

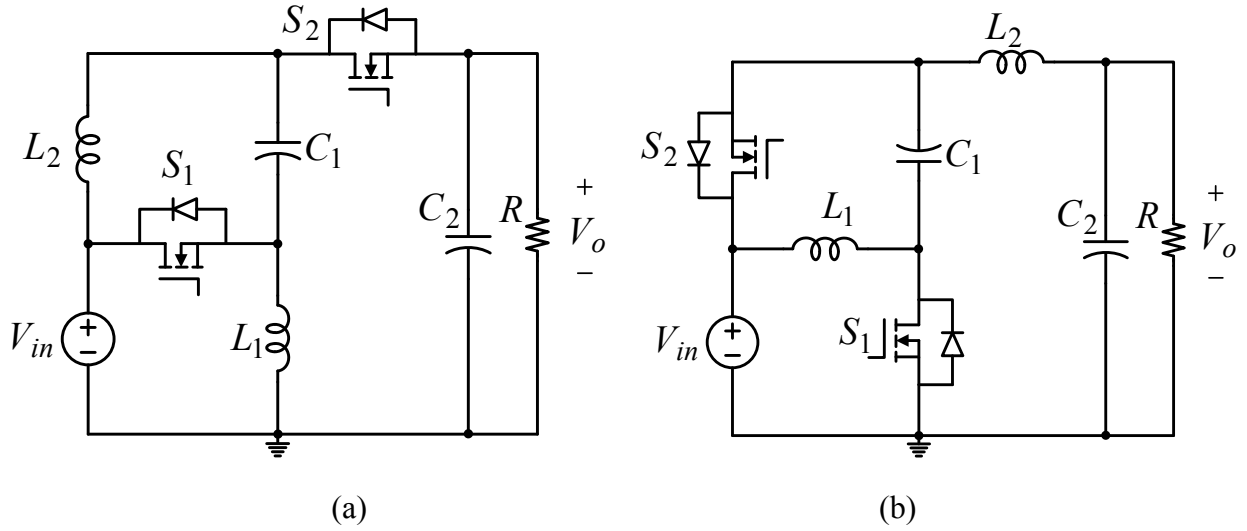


Figure 9.4 Proposed single-phase semi-Z-source inverters, (a) semi-Z-source inverter, (b) semi-quasi-Z-source inverter.

9.3 Operating Principle of Semi-Z-source Inverters

Figure 9.5 shows the voltage gain curve of proposed semi-Z-source inverters. The y axis is the voltage gain of the inverter, and the x axis is the duty cycle of the switch S1. The switch S1 and S2 is conducted in a complementary manner. By operating the switch S1 with duty cycle

changing from 0 to 2/3, the proposed inverters are able to output the same voltage range ($+V_{in}$~$-V_{in}$) as the full bridge inverter, as shown in Figure 9.5 with red solid line. When the duty cycle of S1 changes from (0~0.5), the inverter can output the positive output voltage; and when the duty cycle of S1 changes from (0.5~2/3), the inverter can output the negative output voltage. When the duty cycle is equal to 0.5 the semi-Z-source inverters are able to output zero voltage. Figure 9.6 shows the two states equivalent circuit in one switching period using semi-quasi-Z-source inverter as an example for analysis. Figure 9.6(a) shows the state I when switch S1 is conducted. During this period, the capacitor C1 and the input voltage source charge the two inductors, and the inductor current is increased. Figure 9.6(b) shows the state II when switch S2 is conducted. During this period, the two inductors become the source and the inductor current is decreased. The inductor current reference and the capacitor voltage reference direction are marked in the figure for the following steady state equation derivation. More detailed dc operation modes of this circuit could refer to [224]. According to the inductor voltage second balance and the capacitor charge balance equations, we can have the following steady state equations.

$$\frac{V_o}{V_{in}} = \frac{1-2D}{1-D} \tag{1}$$

$$V_{C1} = \frac{D}{1-D} V_{in} \tag{2}$$

$$I_{L2} = -I_o \tag{3}$$

$$I_{L1} = -\frac{D}{1-D} I_o \tag{4}$$

The output voltage of the inverter can be represented by (5). And the modulation index can be defined as (6); plug (5) and (6) into (1) we can get (7); D'=1-D is the duty cycle of S2 as derived in (8). Because the relationship between the full bridge inverter output and input voltage

is linear in terms of switch duty cycle, the sinusoid output voltage can be achieved by using a sinusoidal changed duty cycle. But the output voltage and the input voltage of the semi-Z-source inverter are not a linear relationship with the switch duty cycle any more. In order to achieve the sinusoid output voltage, the duty cycle cannot be changed in a sinusoid manner. A corresponding nonlinear revised duty cycle has to be used to generate the correct sinusoid output voltage. A new duty cycle reference, as shown in (7) or (8) has to be used. The comparison of the proposed modulation method for semi-Z-source inverters and the traditional single phase Z-source inverter modulation method will be discussed in detail in the next section.

$$V_o = V \sin \omega t \tag{5}$$

$$M = \frac{V}{V_{in}} \tag{6}$$

$$D = \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{7}$$

$$D' = \frac{1}{2 - M \sin \omega t} \tag{8}$$

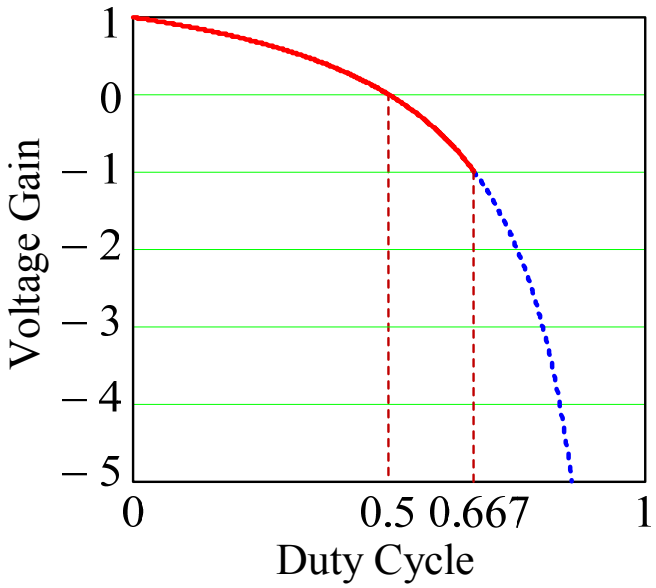


Figure 9.5. Duty cycle operation region of proposed semi-Z-source inverters (solid red line).

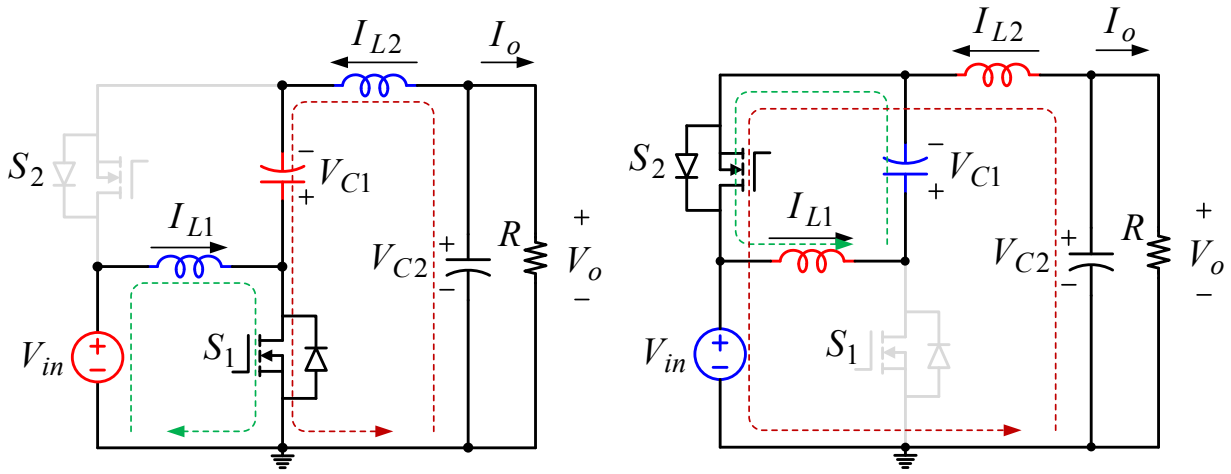
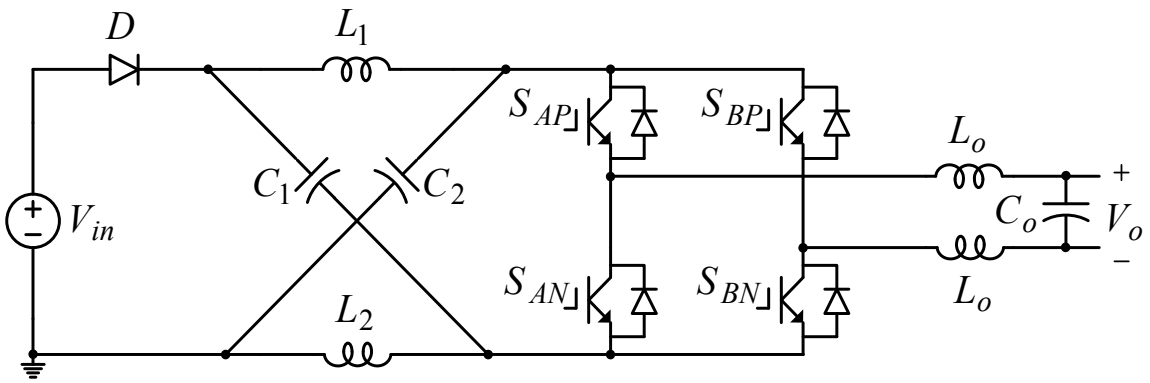


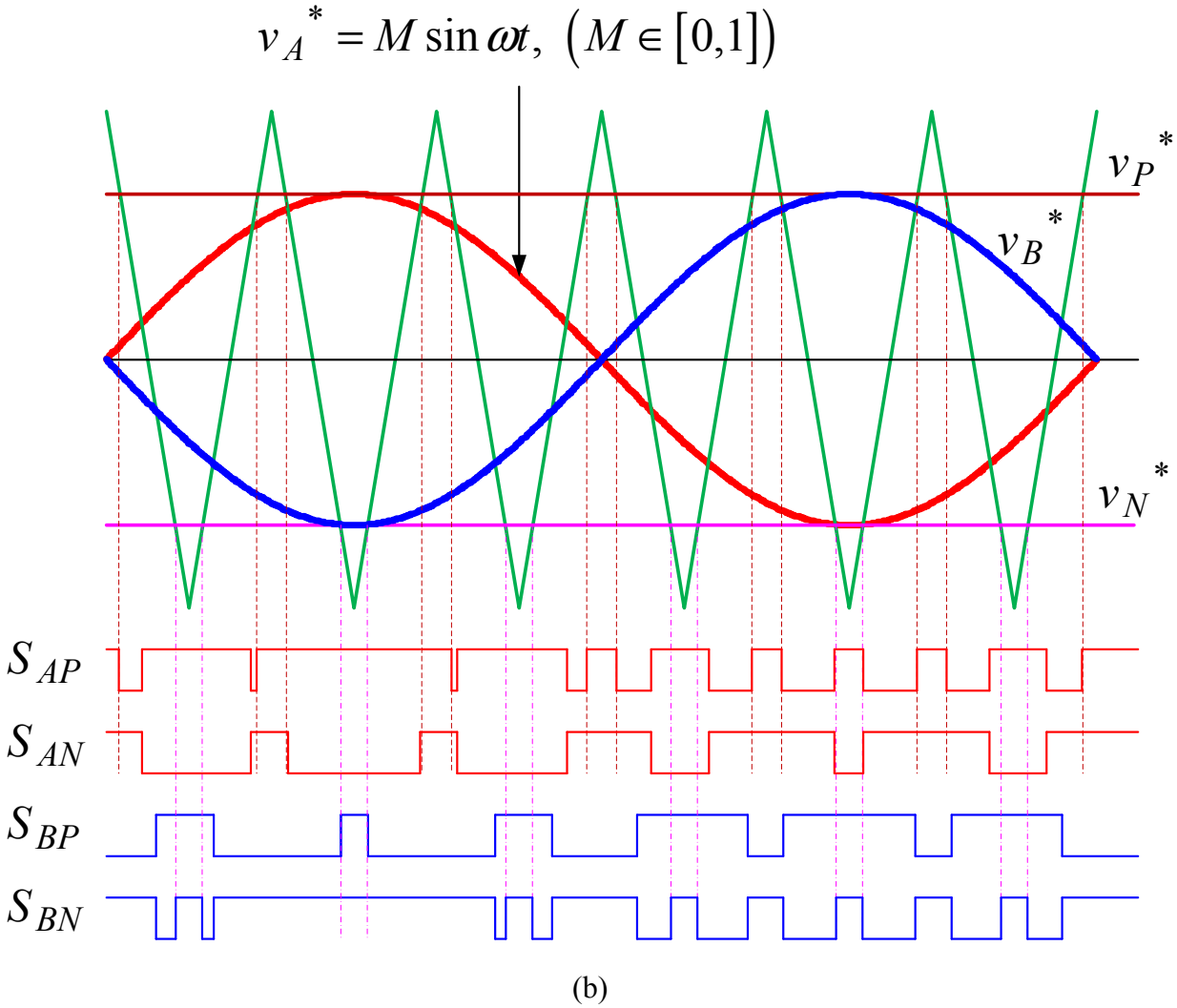
Figure 9.6 Semi-quasi-Z-source operation modes in one switching period. (a) State I S1 is on, (b) State II S2 is on.

9.4 Modulation of Semi-Z-source Inverters

Figure 9.7 shows the traditional single-phase Z-source H-bridge inverter and its modulation method. Simple boost control is used as an example. The correct conduction time of each switch of two phase legs are generalized by two sinusoid voltage references compared with a triangle carrier voltage. The two sinusoid voltage reference v_A^* and v_B^* are 180 degrees phase shift from each other. Two straight lines v_P^* and v_N^* are used to generalize the shoot-through zero state. When the carrier is higher than the upper straight line, phase leg A goes to shoot through state; whereas phase leg B goes to shoot through state when the lower straight line is greater than the carrier [196]. By controlling the shoot through duty cycle, the traditional Z-source inverter can achieve the different voltage gain. Figure 9.8 shows the proposed modified SPWM method of semi-Z-source inverters. Instead of using the sinusoid voltage reference, a modified voltage reference as derived in (8) is used as the reference signal for the conduction of switch S2 in order to output the sinusoid voltage.



(a)



(b)

Figure 9.7 Traditional single-phase Z-source H-bridge inverter and its modulation method

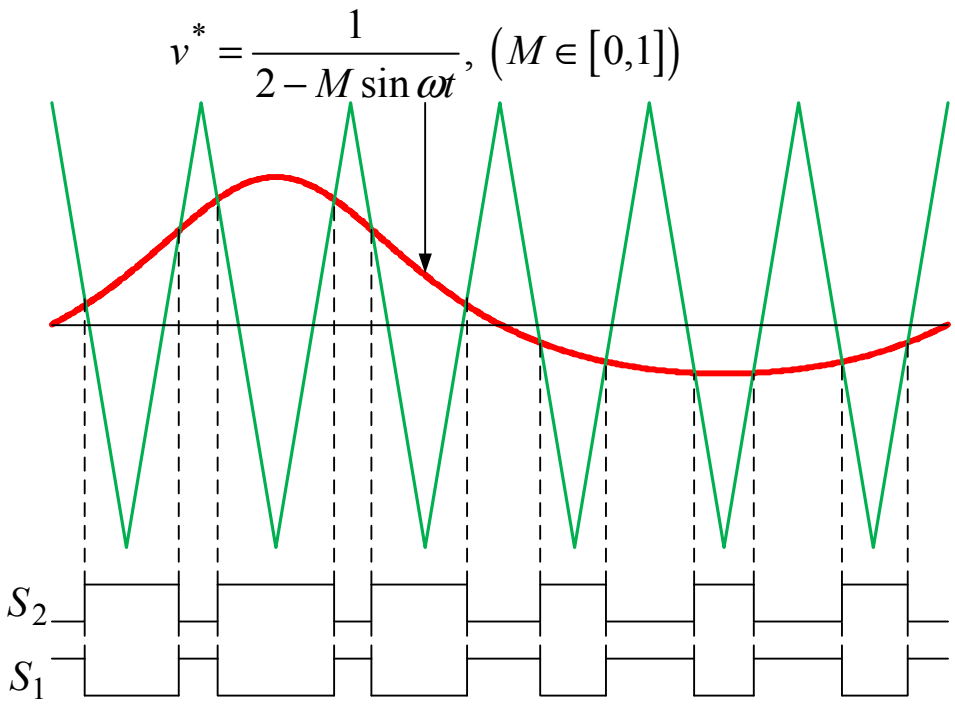


Figure 9.8. Proposed modified SPWM method for semi-Z-source inverters.

When the reference is greater than the carrier the switch S2 is turned on, otherwise S2 is turned off. And the gate signal of S1 is complementary with the switch S2. The modified voltage reference as derived in (7) can be also used directly to generate the gate signal of S1. But in real implantation, the gate signal generation of S2 needs less calculation of DSP, which is usually preferred. So Figure 9.8 uses the generation of gate signal S2 as an example The modulation index of the modified SPWM method is also in the range of 0~1. And Figure 9.8 shows the situation when the modulation index M=2/3 as an example. Figure 9.9 shows the duty cycle operation region with different output voltage when the modulation index is equal to 1. The x axis of Figure 9.9 is the output voltage angle ωt. As shown in (5), with the change of ωt, the sinusoidal output voltage can be achieved. It can be shown from Figure 9.9, in order to output the sinusoid voltage, the duty cycle D is limited in the region (0~2/3). The other region of the duty cycle can also be utilized in other application by using at least two semi-Z-source inverters together, which will be discussed further in section VI.

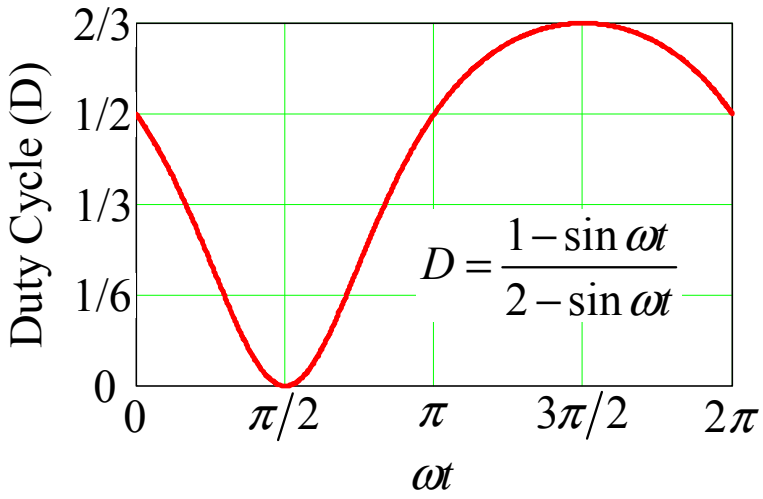


Figure 9.9 The duty cycle operation region of semi-Z-source inverters when the modulation index is equal to 1.

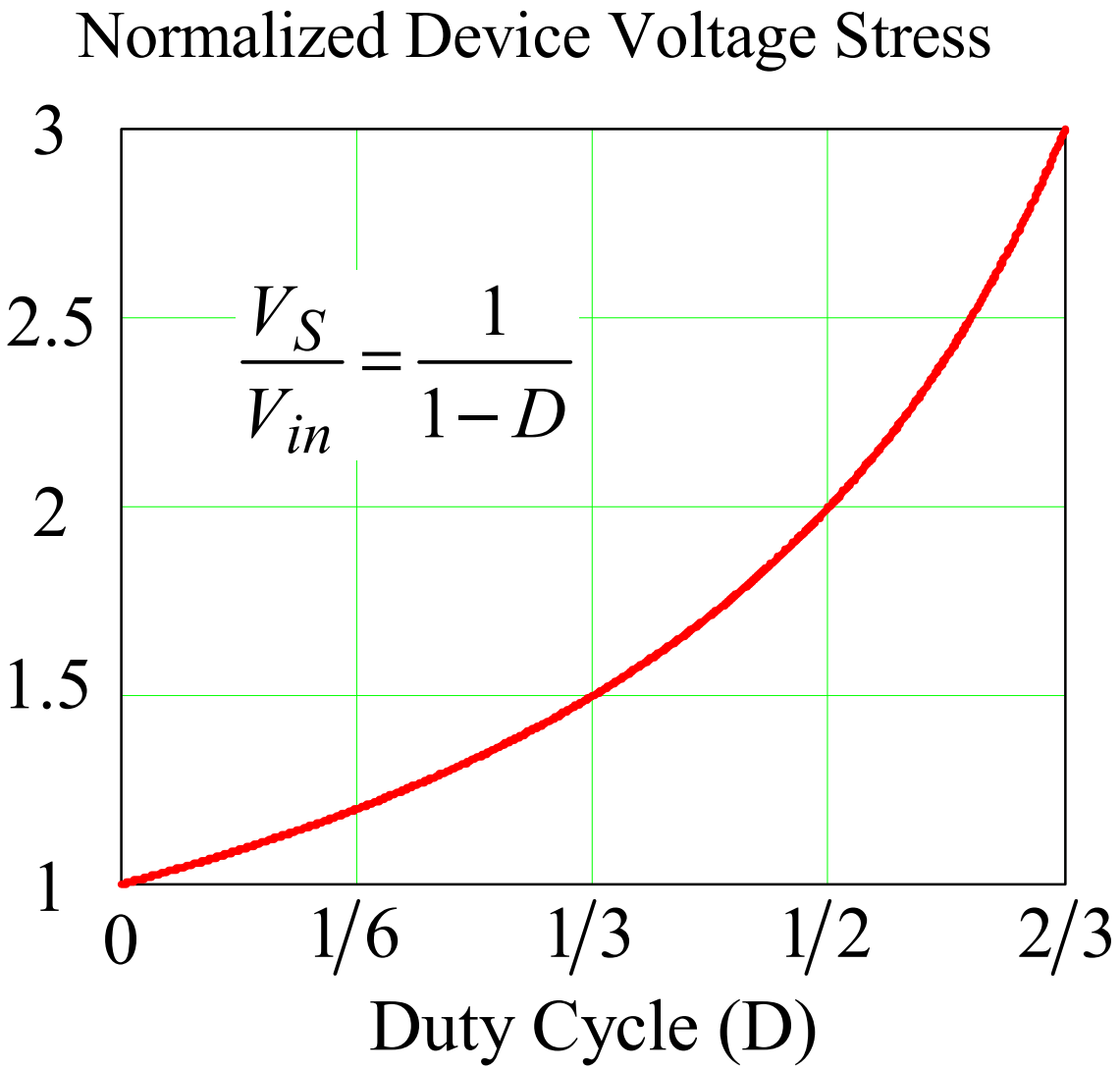
9.5 Device Stress Analysis and Passive Component Design

The semi-quasi-Z-source inverter, as shown in Figure 9.4(b) is used as an example for the device stress analysis and passive component design. The switch voltage stress can be derived as (9). Assume the output current is (10) as an example, which is in phase with the output voltage. The switch current stress can be derived as (11). Figure 9.10 and Figure 9.11 show the normalized device voltage stress and current stress versus duty cycle D, versus modulation index M and output voltage angle ωt. According to (9), (11), Figure 9.10, and Figure 9.11, the peak voltage across the device happens when D=2/3, or M=1, ωt=3π/2, which is $3V_{in}$. And the peak current through the device also happens when D=2/3, or M=1, ωt=3π/2, which is 3I. The voltage stress of the switching device of this inverter is high, but the switching device number is reduced, this inverter is especially suitable for low cost micro-inverter application with high voltage SiC switching devices [296, 297].

$$V_S = V_{in} + V_C = \frac{1}{1-D}V_{in} = (2 - M\sin\omega t)V_{in} \tag{9}$$

$$I_o = I\sin\omega t \tag{10}$$

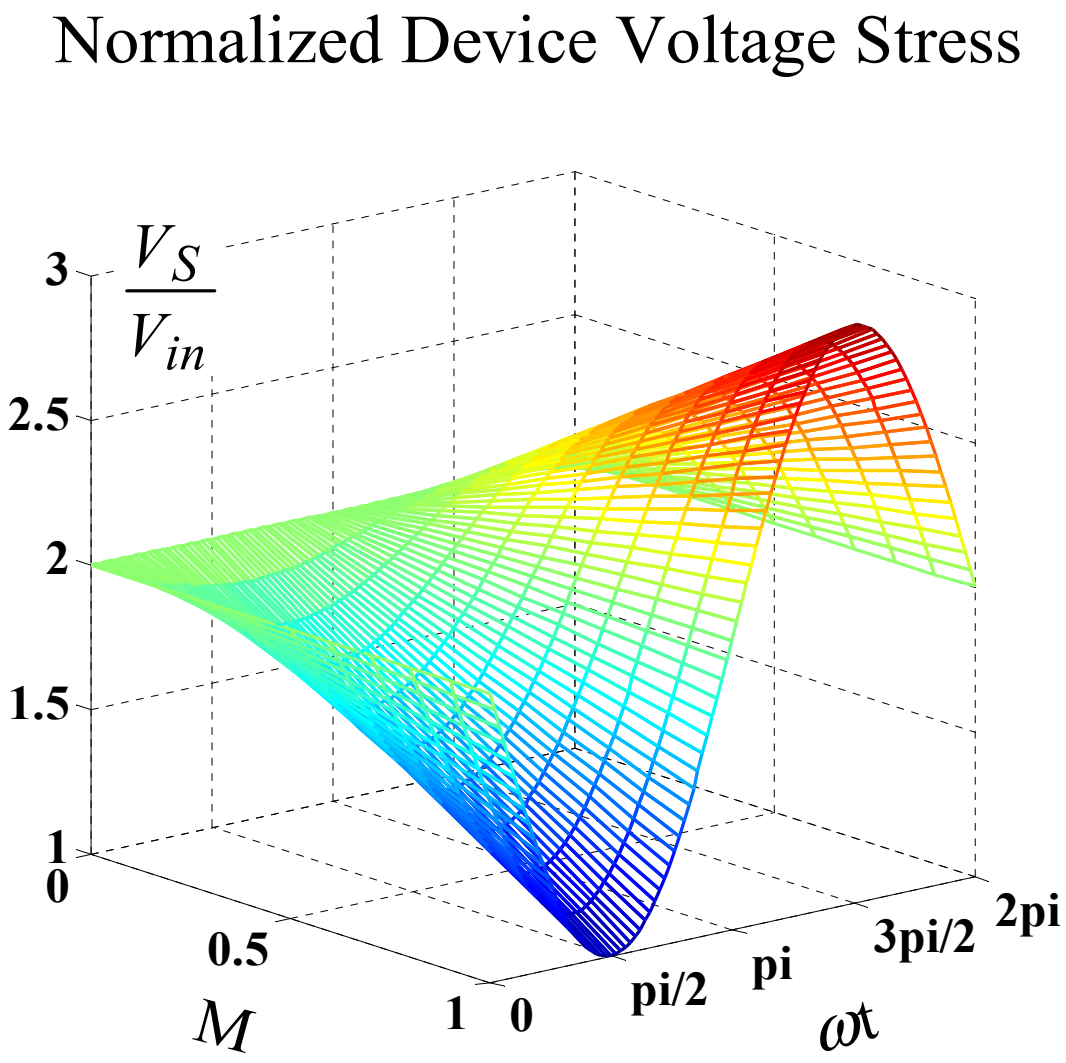
$$I_S = I_{L1} + I_{L2} = \frac{-1}{1-D} I_o = -\left(2\sin\omega t - M\,(\sin\omega t)^2\right) I \tag{11}$$



(a)

Figure 9.10 Normalized device voltage stress. (a) versus D; (b) versus M and ωt.

Figure 9.10 cont'd



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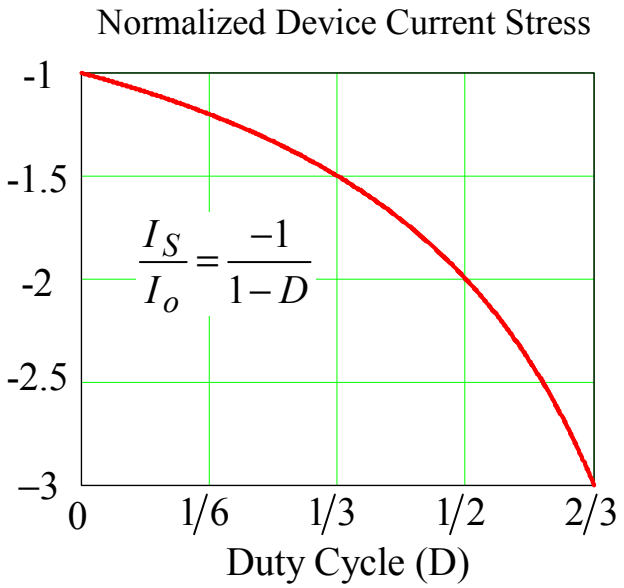

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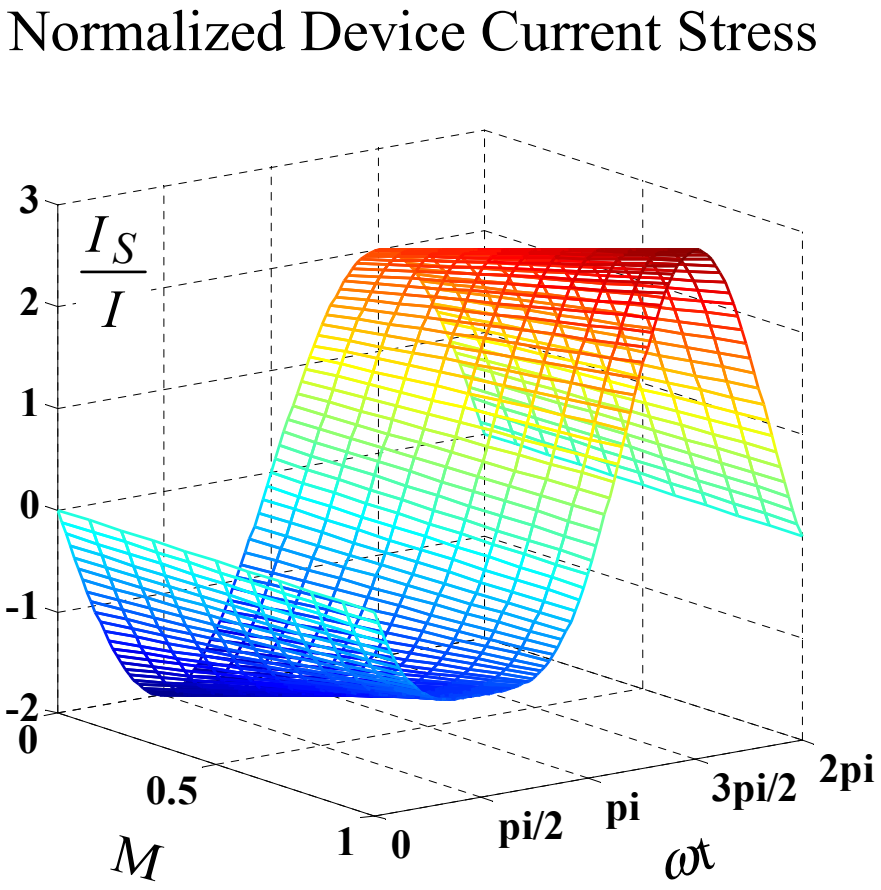


(b)

Figure 9.11 Normalized device current stress. (a) versus D; (b)versus M and ωt.

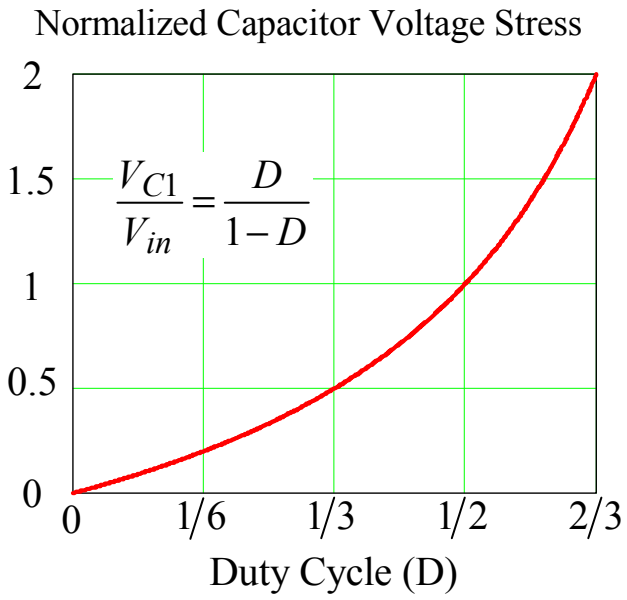
Figure 9.12 shows the normalized capacitor C1 voltage stress in terms of duty cycle, modulation index and output voltage angle. The capacitor C1 peak voltage is $2V_{in}$ according to (2), which happens when the S1 duty cycle D=2/3. The inductor L2 current is derived in (3), and the inductor L1 current can be derived as (13) by plugging (7) into (4). Figure 9.13 shows the normalized inductor L1 current stress in terms of duty cycle, modulation index and output voltage angle. The inductor L1 peak current is 2I, which is two times of the output current peak current. It also happens when the S1 duty cycle D=2/3. The capacitor C1 voltage ripple can be derived as (14). And the inductor current ripple can be derived as (15) assuming L1=L2. Figure 9.14(a) shows the capacitor C1 normalized voltage ripple versus modulation index M and output voltage angle ωt. Figure 9.14(b) shows the inductor L1 normalized current ripple versus modulation index M and output voltage angle ωt. So, the L1 inductance value and C1 capacitance value can be chosen according to the peak ripple requirement as shown in (14),(15), and Figure 9.14.

$$V_{C1} = \frac{D}{1-D} V_{in} = (1 - M \sin \omega t) V_{in} \tag{12}$$

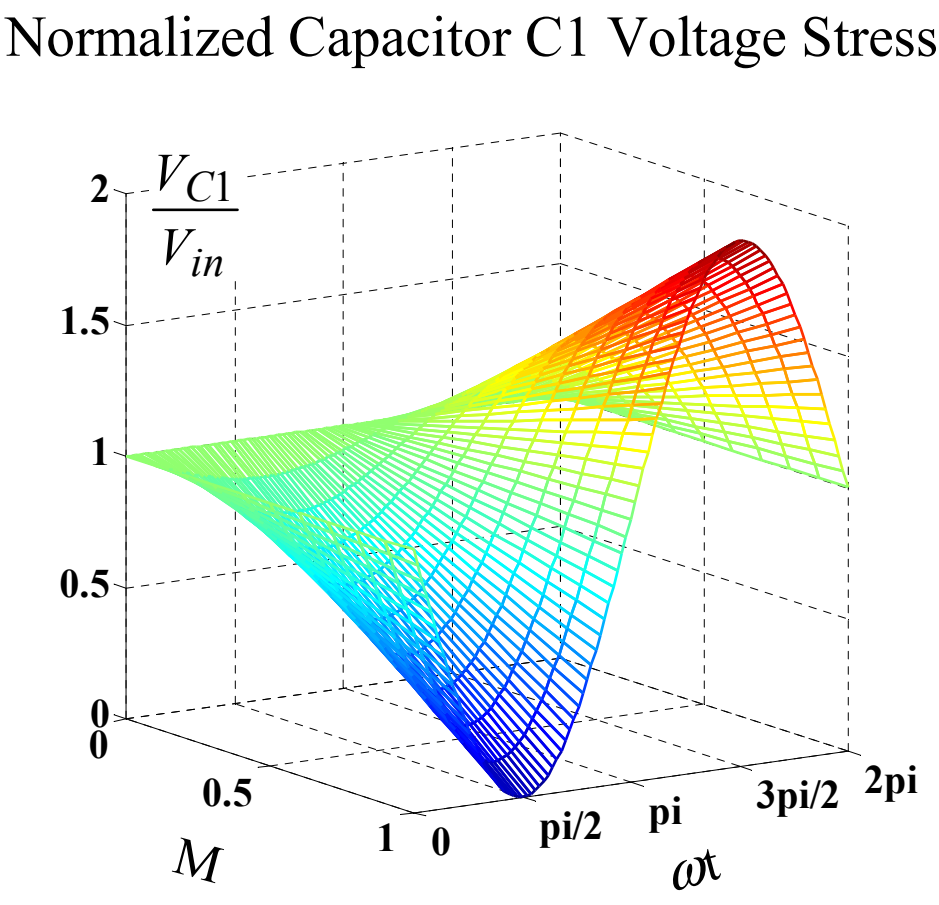
$$I_{L1} = \frac{D}{D-1} I_o = -\left(\sin \omega t - M (\sin \omega t)^2 \right) I \tag{13}$$

$$\Delta V_{C1} = \frac{(1-D) T_s I_{L1}}{C1} = \frac{-\sin \omega t + M (\sin \omega t)^2}{2 - M \sin \omega t} \frac{T_s}{C1} I \tag{14}$$

$$\Delta I_{L1} = \Delta I_{L2} = \frac{V_{in} T_s D}{L_1} = \frac{V_{in} T_s}{L_1} \frac{1 - M \sin \omega t}{2 - M \sin \omega t} \tag{15}$$

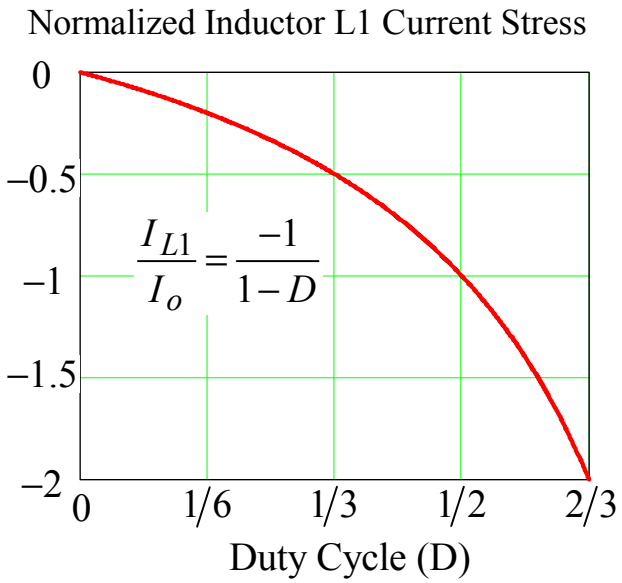


(a)

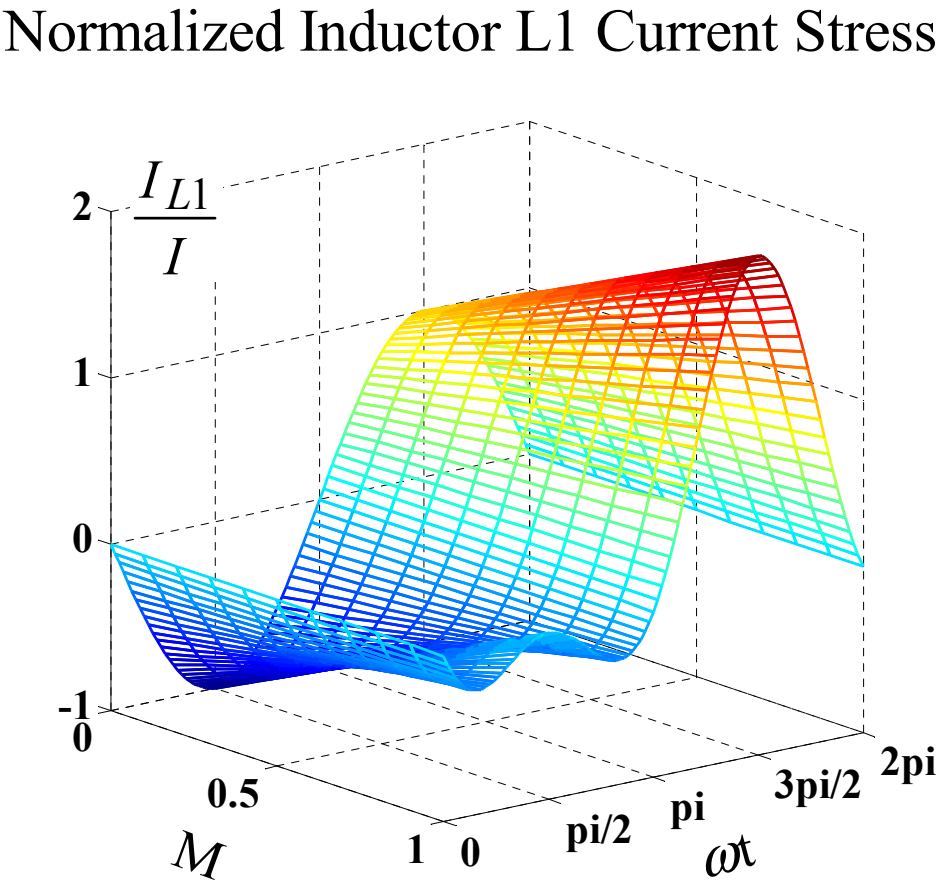


(b)

Figure 9.12 Normalized capacitor C1 voltage stress. (a) versus D; (b) versus M and ωt.

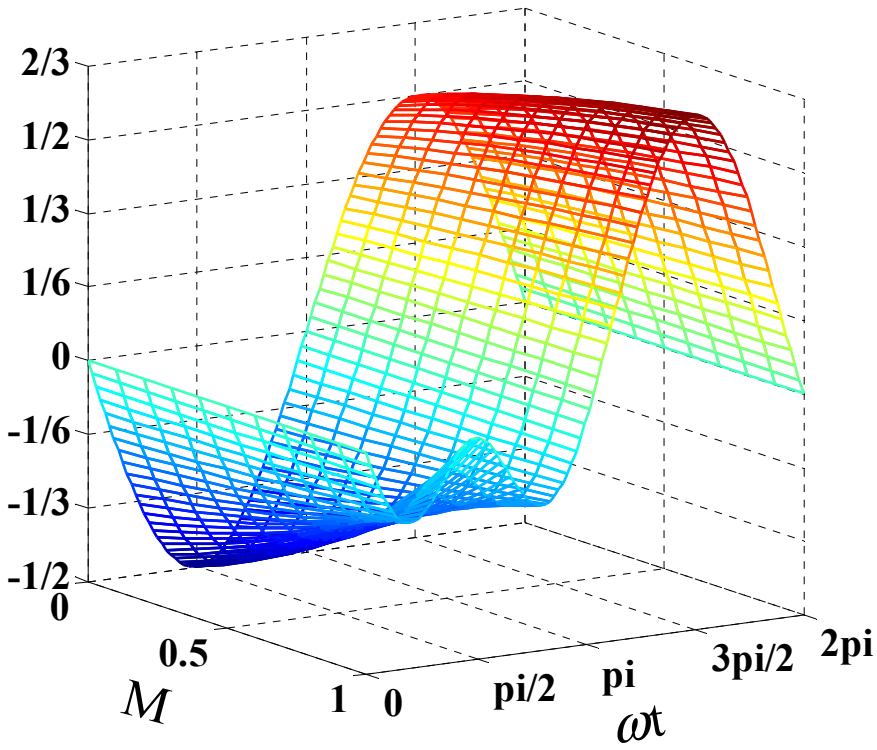


(a)



(b)

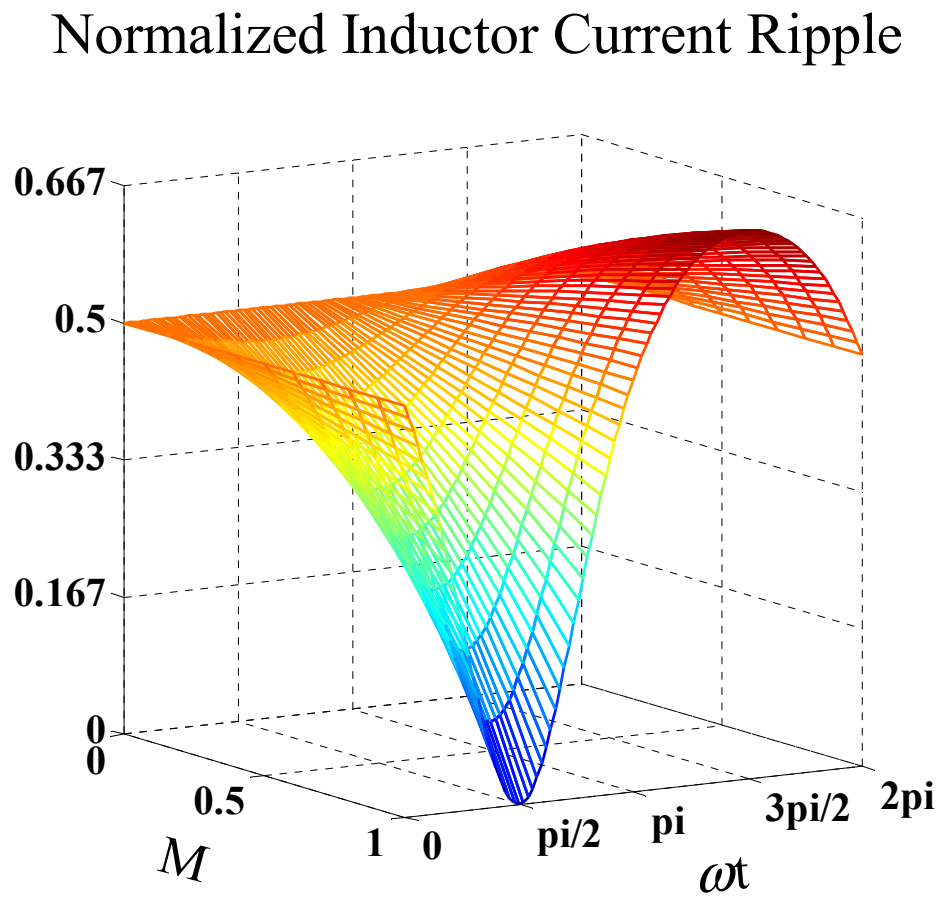
Figure 9.13 Normalized inductor L1 current stress. (a) versus D; (b) versus M and *ωt*.



(a)

Figure 9.14 Normalized capacitor C1 voltage ripple and inductor L1 current ripple versus M and ωt.

Figure 9.14 cont'd



(b)

9.6 Topology Expansion and Discussion

The proposed single-phase semi-Z-source inverter can be expanded to two-phase or three-phase inverter very easily, which are similar to boost or buck-boost inverters. The voltage gain of two-phase or three-phase semi-Z-source inverter can also be increased, because the operation range of the duty cycle can be increased from (0~0.667) to (0~1). Figure 9.15 shows the two-phase semi-quasi-Z-source inverter as an example, which can be also used in the split single-phase application. The corresponding modified reference signal with different voltage gain is shown in Figure 9.16. The output voltage of two-phase semi-quasi-Z-source inverter is twice bigger than the full-bridge inverter with the same input voltage, if the voltage reference is the

same with the single phase version. By changing the voltage reference due to Figure 9.16, the output voltage of two-phase semi-quasi-Z-source inverter can be increased more.

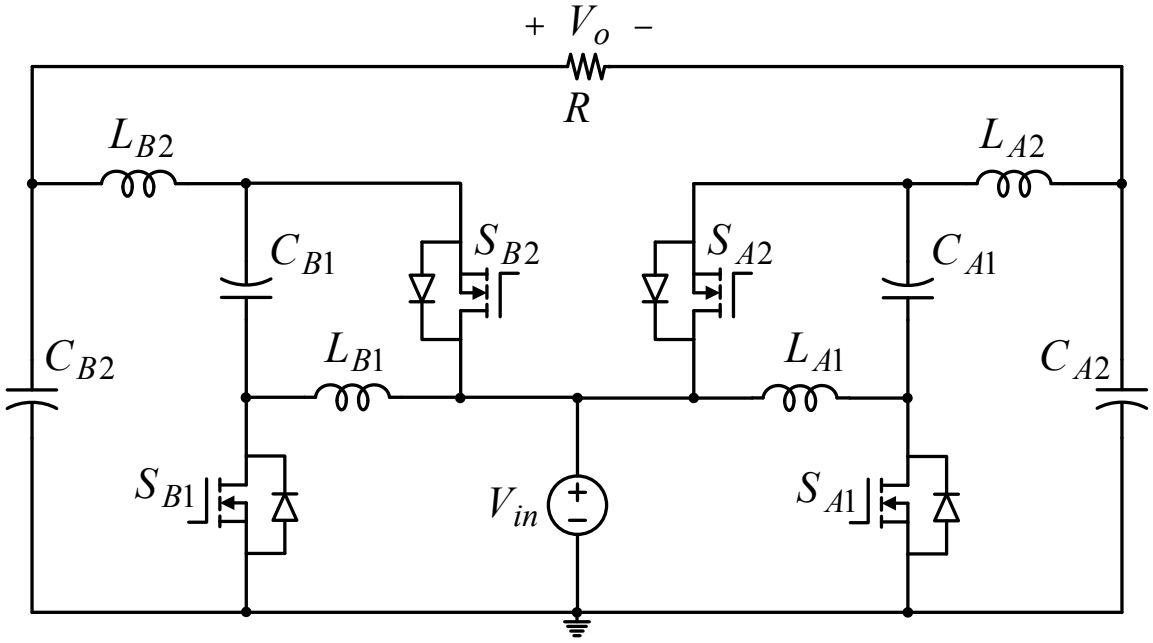


Figure 9.15. Two-phase semi-quasi-Z-source inverter.

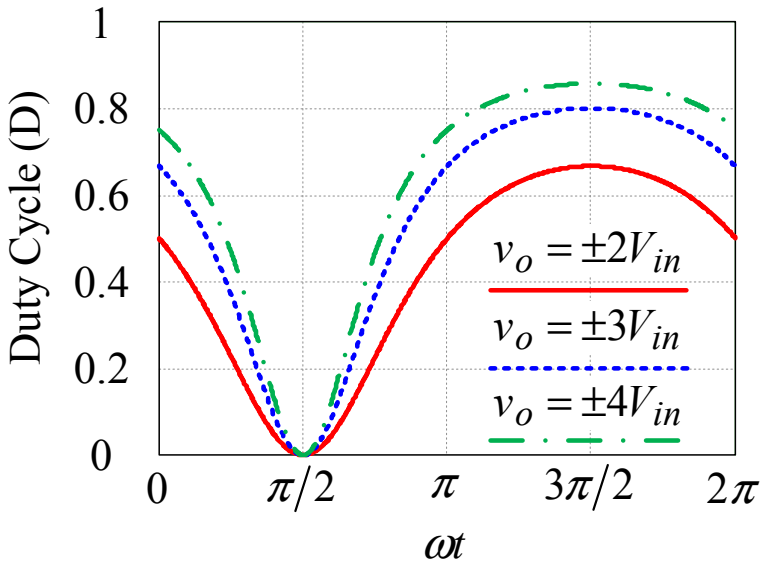
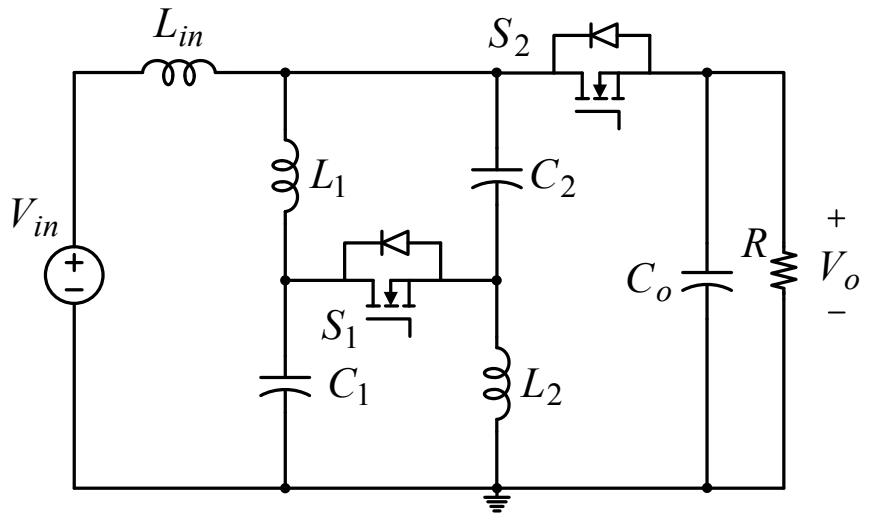


Figure 9.16. The modified reference signal for two-phase semi-quasi-Z-source inverter with higher output voltage.

Actually, many other dc-dc converters with similar voltage gain curves of quasi-Z-source dc-dc converters, as shown in Figure 9.3(b) can also be used as a single-phase inverter with

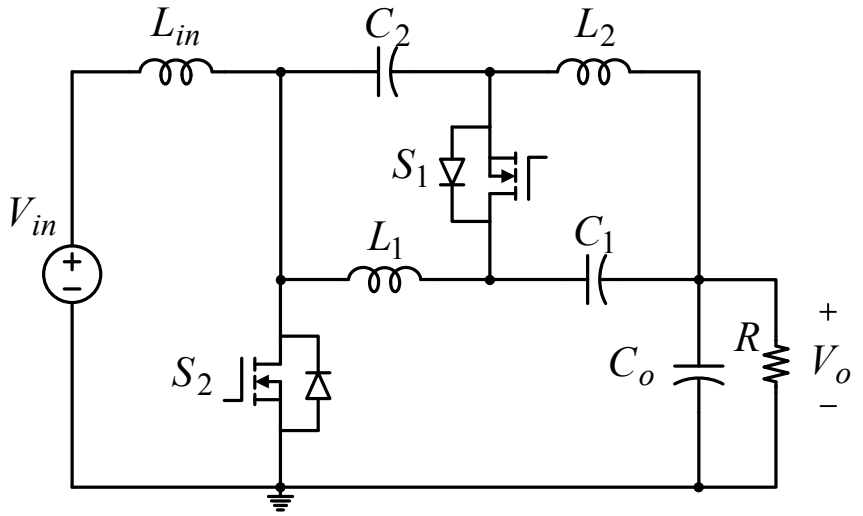
modified SPWM strategy. The current-fed Z-source dc-dc converter mentioned in [189, 295] can be used as a single-phase inverter, which have already been mentioned in above papers. Figure 9.17 shows some other single-phase inverter topologies derived from the current-fed quasi-Z-source inverter topology [190, 191]. These topologies working as a dc-dc converter have already been mentioned in [223]. There are more topologies with the similar voltage gain curves with the proposed single-phase semi-Z-source inverters that can be used as an inverter with similar modified PWM method. Due to the page limit, those topologies are not listed here.



(a)

Figure 9.17 Other single-phase semi-quasi-Z-source inverter topologies derived from the current-fed quasi-Z-source inverter topology.

Figure 9.17 cont'd



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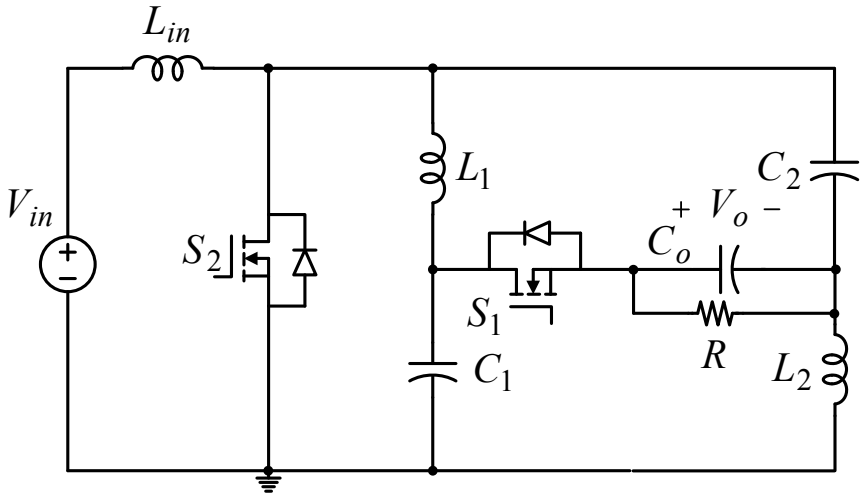


(c)

9.7 Experiment Results

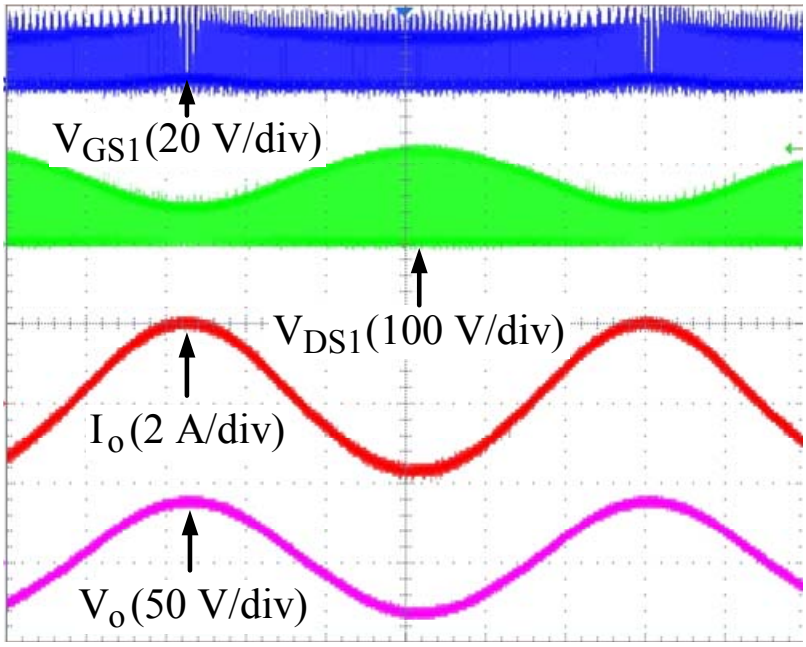
A 40 W semi-quasi-Z-source inverter prototype with 40 V input voltage and 28 V output voltage for operation validation purposes is built. The switching frequency of the prototype is 50 kHz. Because the maximum device stress is 120 V as shown in Figure 9.10, two MOSFETs from ST (STP75NF20) with 200 V voltage rating are selected to be the switching device. The inductor L1 and L2 is designed using (13), (15), Figure 9.13, and Figure 9.14. Because the peak value of

the load current is 2 A for the designed prototype, so the peak value of the inductor L1 current is 4 A according to Figure 9.13, the inductor current ripple of L1 is designed to be 1/3 of the peak current which is about 1.33 A. So the inductance of inductor L1 can be calculated using (15), which is 400 μH. The inductor L2 can be designed using the same design procedure which is also 400 μH. The capacitor C1 can be designed using (12), (14), Figure 9.12 and Figure 9.14. Because the peak voltage stress of capacitor C1 is 80 V according to (12), MLCC capacitor from TDK (C5750X7R2E105K) is selected. The voltage ripple of capacitor C1 is limited to 8.3% of the capacitor voltage, the capacitance can be calculated using (14), which is 4 μF. The output capacitor C2 can be designed using the similar procedure which is also 4 μF.

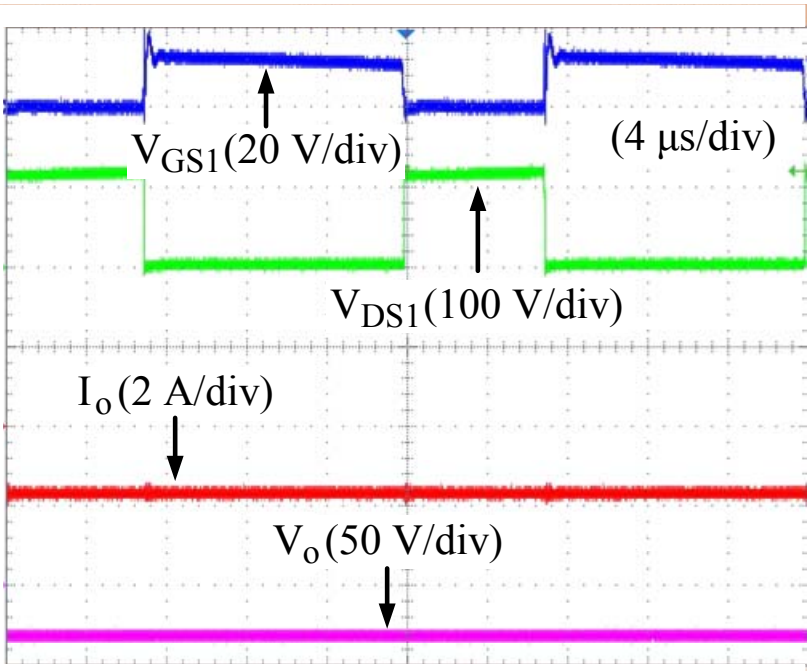
Figure 9.18~Figure 9.21 show the experimental results of a 40 W semi-quasi-Z-source inverter prototype. The input voltage is 40 V, the modulation index is 0.95 and the load resistance is about 19 Ohm. Figure 9.18(a) shows the switch S1 gate to source voltage V_{GS1}, the switch S1 drain to source voltage V_{DS1}, the output voltage V_o and the output current I_o .Figure 9.18(b) shows the zoomed in waveform of Figure 9.18(a). Figure 9.19 shows the capacitor C1 voltage waveform V_{C1}, the inductor L1 current waveform I_{L1}, and the output voltage and current. Figure 9.20(a) shows the two switches drain to source voltage V_{DS1}, V_{DS2} and the output current. Figure 9.20(b) shows the zoomed in waveforms of Figure 9.20(a). Figure 9.21 shows the input voltage V_{in}, capacitor C1 voltage, output current and output voltage waveforms. Figure 9.22 shows the load step change waveform when the load current is changed from half power to full power.

Compared to the traditional single-phase Z-source inverters, as shown in Figure 9.7(a), the proposed semi-Z-source inverter only utilize two switches instead of four switches and one diode. So the total cost of semi-Z-source inverter is reduced. The Z-source network of semi-Z-source

inverter is in ac side, while the traditional single-phase Z-source inverter has Z-source network in dc side. The total size of the Z-source network of semi-Z-source inverter is reduced significantly compared to the traditional single-phase Z-source inverter. Therefore, semi-Z-source inverter is more suitable in single-phase photovoltaic application than the traditional single-phase Z-source inverter.



(a)



(b)

Figure 9.18 Device gate-source voltage, drain-source voltage, output voltage and output current.

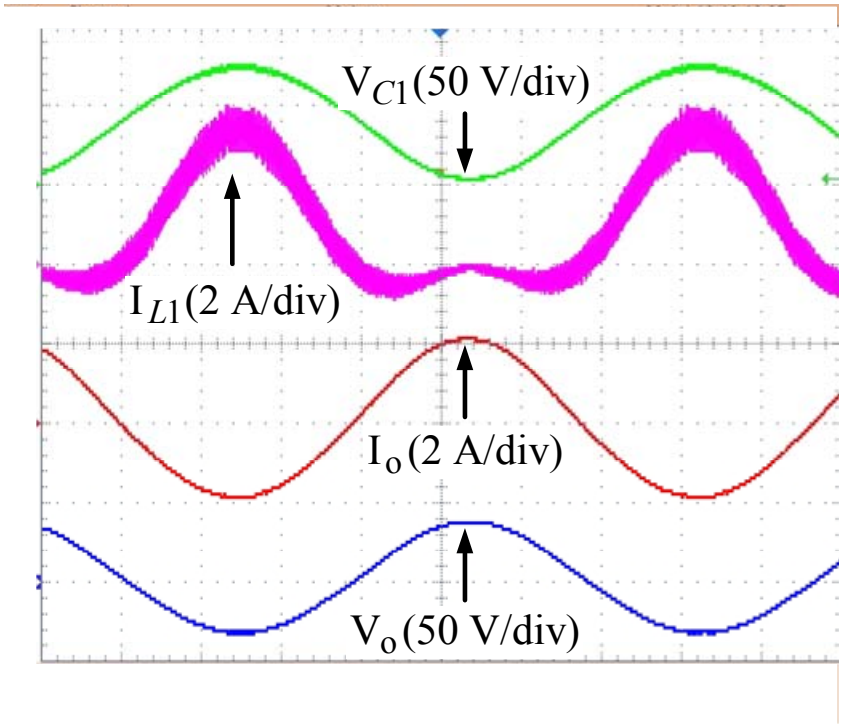
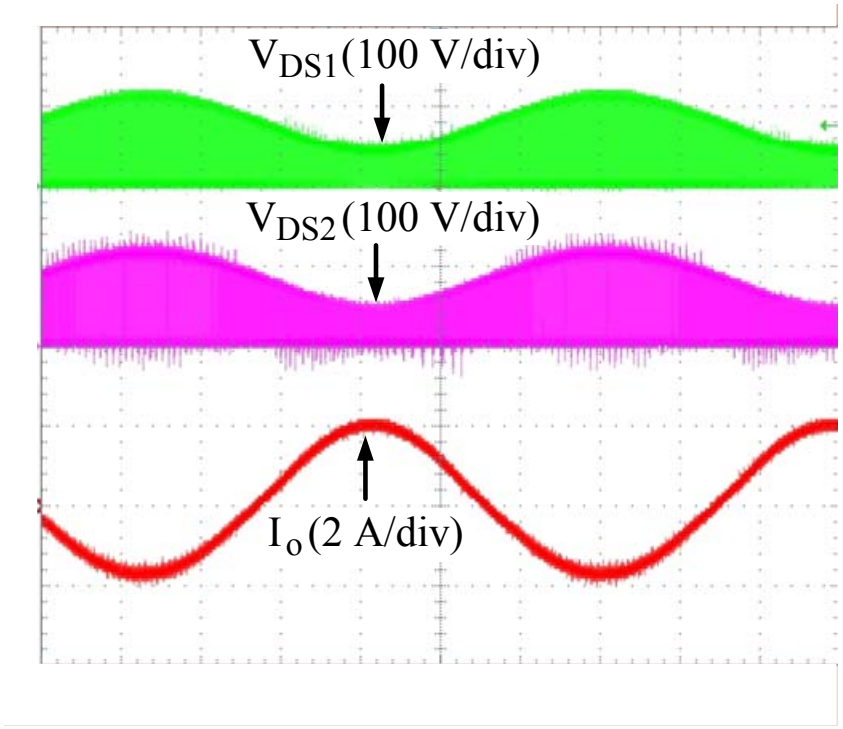


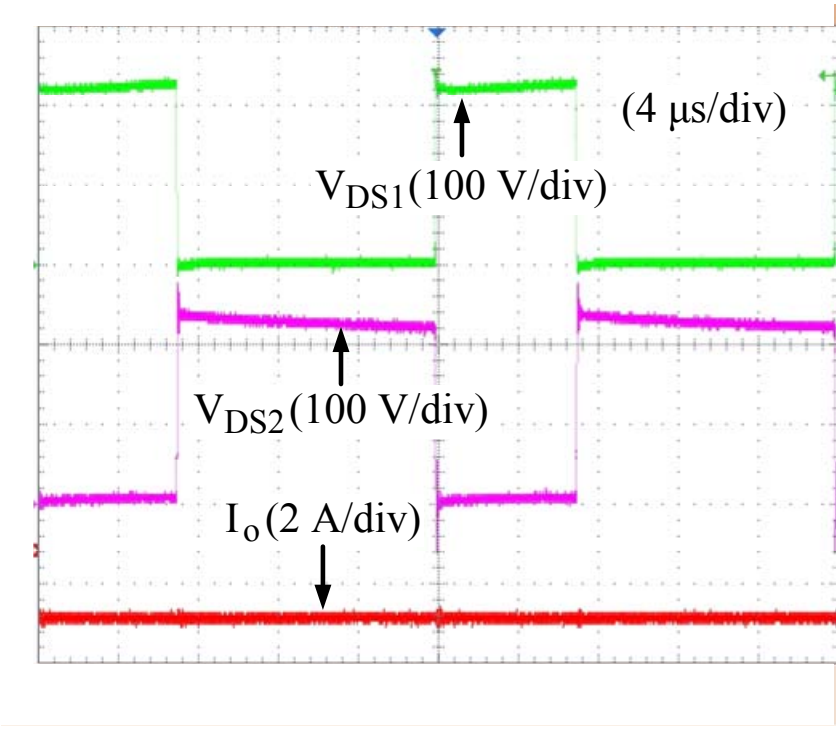
Figure 9.19 Capacitor C1 voltage, inductor L1 current ,output voltage and output current.



(a)

Figure 9.20 Two switching devices drain-source voltage and output current.

Figure 9.20 cont'd



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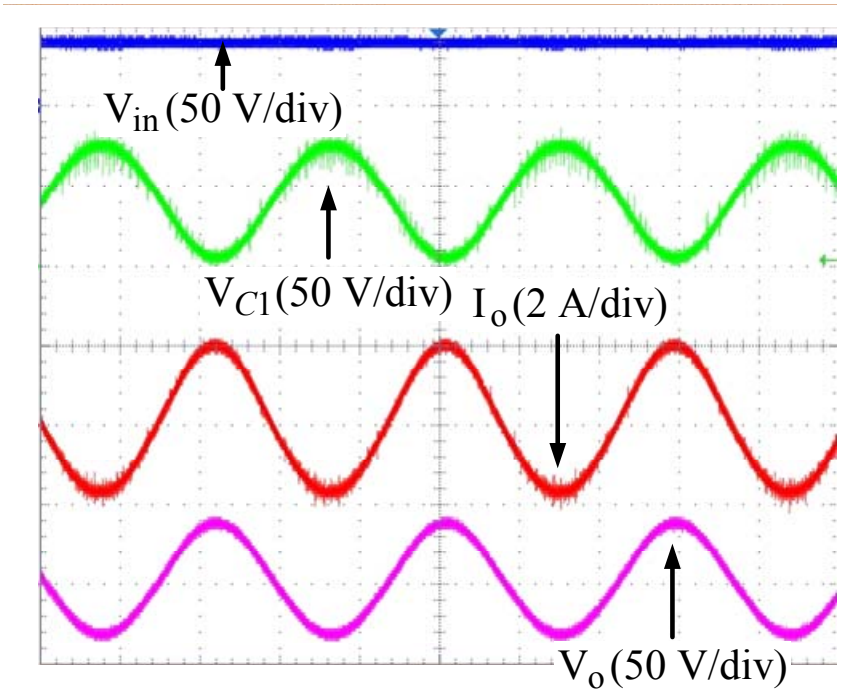


Figure 9.21 Input voltage, capacitor C1 voltage, output voltage and output current.

A 200 W prototype with 160 V input voltage and 110 V output voltage for low voltage grid connection application is built. The design procedure is similar to the aforementioned 40 W prototype. The switching frequency is 20 kHz. The switching devices are STP42N65M5 from ST. The inductance of inductor L1, L2 is about 1.3 mH. The capacitance of capacitor C1 and C2 is 1μF. The measure efficiency curve of this prototype is provided, as shown in Figure 9.23. The efficiency of this prototype is not very high due to the limitation of the lab supply, more efficient design can be made by optimal designed inductor and switching devices.

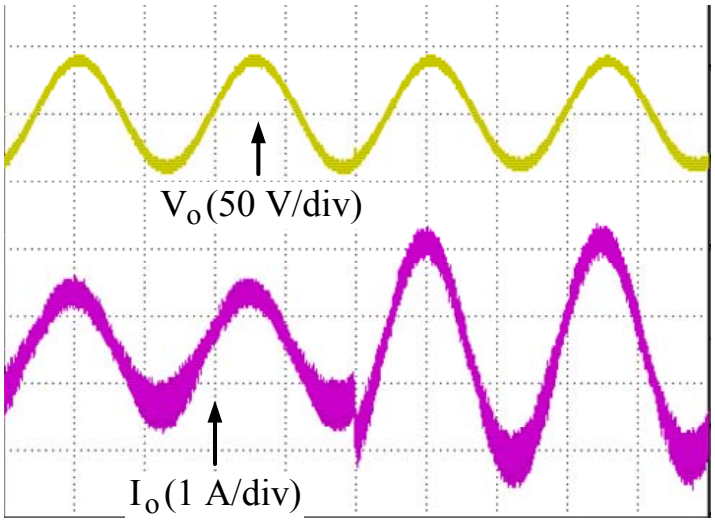


Figure 9.22 Output voltage and current waveform with load step change from half power to full power

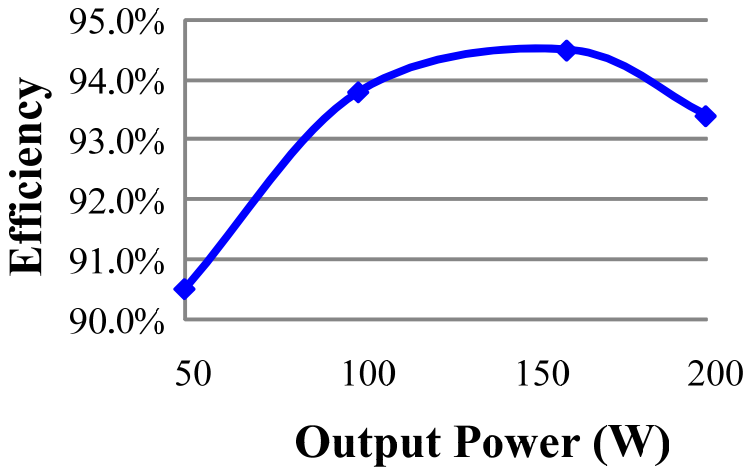


Figure 9.23 Measured efficiency curve.

9.8 Conclusion

In this chaper, several single-stage single-phase non-isolated semi-Z-source inverters are proposed. It is especially suitable for photovoltaic (PV) panel in low voltage grid-connected application as a low cost micro inverter with high voltage SiC switching devices. By employing the Z-source or quasi-Z-source network, the proposed inverters are able to utilize only two active switching devices to achieve the same output voltage as the traditional full bridge inverter does. Different from the traditional single phase Z-source inverter with an extra shoot-through zero state to achieve the boost function, the two switches of the semi-Z-source inverter are controlled complementarily. The input dc source and the output ac voltage share the same ground, which effectively eliminates the leakage current caused by the PV panel. A modified SPWM method is also proposed to solve the non-linear voltage gain problem of the semi-Z-source inverter. The topology expansions are summarized; many other inverter topologies can be derived based on the same idea. A single-phase semi-Z-source inverter prototype has been built and tested to verify the validity of the proposed circuit and to demonstrate the special features. A 200 W

prototype with 110 V output voltage for low voltage grid connection application has also been built, experimental results are provided.

CHAPTER 10
Low Cost Transformer Isolated Boost Half-bridge Micro-inverter for Single-phase Grid-connected Photovoltaic System

This chapter presents a low cost high efficiency transformer isolated micro-inverter for single-phase grid-connected photovoltaic (PV) system. The proposed micro-inverter is composed of two stages, an isolated dc-dc converter stage and an inverter stage with a dc link. A high frequency transformer isolated high voltage gain boost half-bridge dc-dc converter is used at the first stage to achieve maximum power point tracking (MPPT) and to step up the low PV panel voltage to the high voltage dc-link. A pulse width modulated (PWM) full-bridge inverter with LCL filter is used at the second stage to output the synchronized sinusoid current with unity power factor to the grid. By utilizing the transformer leakage inductance, two primary side switches can achieve zero voltage switching (ZVS). A 210 W prototype of the proposed micro-inverter has been built and tested. The efficiency of the proposed boost half-bridge dc-dc converter has been measured according to the PV curve, which is up to 98.2%. Experimental results are provided to demonstrate the validity and features of the proposed circuit.[10]

10.1 Introduction

Recently, because of the energy crisis, the renewable energy sources, such as wind turbine, photovoltaic (PV) panels, etc. become more and more popular in industrial and residential applications. With different radiance and temperature, the dc output voltage and the maximum

[10] This work has been presented in part in *Applied Power Electronics Conference and Exposition, 2012. APEC 2012. Twenty-seventh Annual IEEE, 2012. And it is* submitted to *IEEE Trans. Power Electron.*

output power of the PV panel will change. So, an inverter interface with maximum power point tracking (MPPT) is required for the PV panel to connect to the grid. Different inverter topologies as well as different MPPT techniques will be reviewed as follows.

There are three popular technologies for the PV panels connected to the grid through an inverter: centralized three-phase inverter for matrix connected PV panels, single-phase string inverter for series connected PV panels and modular integrated micro-inverter for a single PV panel [228, 229, 231-237, 298-304]. Due to its low cost and high reliability, modular integrated micro-inverter is preferred for the future application [234, 236]. Based on the galvanic isolation, the PV inverter topologies can be divided into transformer-less topologies and transformer isolated topologies. Since the output voltage of a single PV panel is as low as 20~50 V, a high voltage gain inverter is required for the PV panel to connect to the single-phase grid. Although the transformer-less inverter topologies have low cost and high efficiency features, they usually do not have enough voltage gain to boost the input voltage. Therefore, the transformer isolated inverter topologies with high voltage gain are preferred for a single PV panel grid-connected application.

For the transformer isolated inverter topologies, there are two popular approaches. The first approach utilizes the single stage flyback inverter or isolated buck-boost inverter, which is able to replace the electrolytic capacitor with high voltage low capacitance film capacitor for the energy storage [240-248, 305]. This approach usually uses less switches with low cost, the high frequency transformer is the major design challenge for these topologies to achieve high efficiency. The second approach is a two stage approach with a transformer isolated dc-dc converter as the first stage and a full-bridge inverter as the second stage [249-257, 306]. A high efficiency dc-dc converter with soft switching is usually designed for the first stage [236, 256,

307-311] . A full bridge inverter with PWM or line frequency switches is usually used for the second stage. The dc-dc converter in the first stage is the major design challenge to achieve low cost and high efficiency. A low cost and high efficiency ZVS bidirectional dc-dc converter with boost type half-bridge input side has been proposed for the fuel cell and battery applications [312-315]. Compared to the traditional half-bridge dc-dc converter, this converter have continuous input current and reduced transformer turns ratio features which is especially suitable for the high power step-up applications [316-323].

Due to the non-linear behavior of PV panel, MPPT techniques with proper voltage or current control strategy is required for the PV panel full utilization. Numerous MPPT strategies have been studied in the literature [324-335], such as, perturb and observe (P&O) method, incremental conductance method, ripple correlation method, and reduced current sensor method. Different methods show different tradeoffs of the MPPT steady-state efficiency, transient tracking speed, and control complexity [336]. For the above mentioned two stage PV inverter, the dc-dc converter in the first stage is usually used for the MPPT control.

This chapter presents a boost half-bridge micro-inverter for single-phase photovoltaic system applications with low cost and high efficiency features. The proposed inverter consists two stages, the transformer isolated boost half-bridge dc-dc stage and the full-bridge PWM inverter stage. The two active switches voltage doubler in the secondary side of the traditional bidirectional boost half-bridge dc-dc converter [312] are replaced with two diodes, since only single directional power flow is needed in the proposed micro-inverter system. Only two active switches are utilized in the boost half-bridge dc-dc converter, and no dc current flow into the transformer like the flyback converter. In this case, the transformer size and cost can be reduced correspondingly. The total system cost is reduced, and the efficiency can be improved. The two

switches are controlled complementarily, and the duty cycle is determined by the input voltage generated by MPPT and the desired low dc link voltage. When the transformer leakage inductance is large enough, ZVS of these two active switches can be achieved. A PWM full-bridge inverter is used at the second stage to output the synchronized sinusoid grid current. In the following sections, the circuit description and basic operation principles will be first discussed. Then, the soft-switching operation principle of the boost half-bridge dc-dc converter will be discussed. The system control strategies and design guideline will be provided after that. Simulation and experimental results will be provided to demonstrate the validity and features of the proposed circuit. The efficiency curve of the boost half-bridge dc-dc converter is measured according to the input PV panel power versus voltage curve with peak efficiency up to 98.2%.

10.2 Proposed Circuit Description and Operating Principle

Figure 10.1 shows the proposed boost half-bridge micro-inverter main circuit structure. The proposed circuit is composed of two stages with a high voltage dc-link. A boost half-bridge isolated dc-dc converter is used in the first stage to cover the input voltage range and achieve the MPPT function of PV panel. A full-bridge PWM inverter with a LCL filter is used in the second stage to control the current to the grid. For the first stage, it can be considered as a boost converter with the output capacitor splitted into two capacitors C_1 and C_2. C_{in} and L_{in} represent the input capacitor and inductor of the traditional boost converter respectively. The switch S_1 and S_2 are two MOSFETs and are controlled in a complementary manner, and the duty cycle is determined by the low dc-link voltage V_{LV} and the input voltage V_{in}. By controlling the input voltage, the MPPT of the PV panel can be achieved. The low dc-link voltage V_{LV} has to be set higher than the maximum output voltage of PV panel to ensure the

boost operation of the circuit. The transformer T primary side is connected between the center tapes of the switches S_1 and S_2, the capacitor C_1 and C_2. The voltage-second of this transformer is always zero during one switching period, no dc-current will flowing into this transformer. A voltage doubler composed of two diodes D_1 and D_2 and two capacitors C_3 and C_4 is connected on the secondary side of the transformer. The high voltage dc-link voltage V_{HV} is the sum of the voltage of C_3 and C_4. The transformer turns ratio (1:n) is the voltage ratio of the low dc-link voltage and the high dc-link voltage, which is $V_{LV} : V_{HV}$. The secondary stage full bridge inverter is composed of four MOSFETs (S_{AP}, S_{AN}, S_{BP}, S_{BN}) with SPWM control strategy. Grid current I_g is controlled as a sinusoid waveform with unity power factor through third order LCL filter ($L_1 \sim L_4$, and C_o). The inductors L_1 and L_2 are coupled together; the inductors L_3 and L_4 are also wound in one core with differential mode coupling method as shown in Figure 10.1

Since the output voltage of a single PV panel with 72~80 cells is about 31 ~ 62 V, which is much lower than the single phase grid voltage, a high voltage gain step-up dc-dc converter is required. Due to the high voltage gain and residential application safety requirement, the isolated dc-dc converter using a high-frequency transformer is one of the solutions. For the isolated dc-dc converters, several topologies candidates including flyback, forward, half-bridge and full-bridge can be considered. Although flyback converter has only one active switch with relatively low cost, the flyback transformer and preferred discontinuous operation may increase the converter power loss. The forward converter only utilizes a half wave rectifier with reduced the output voltage, is more suitable for step-down application.

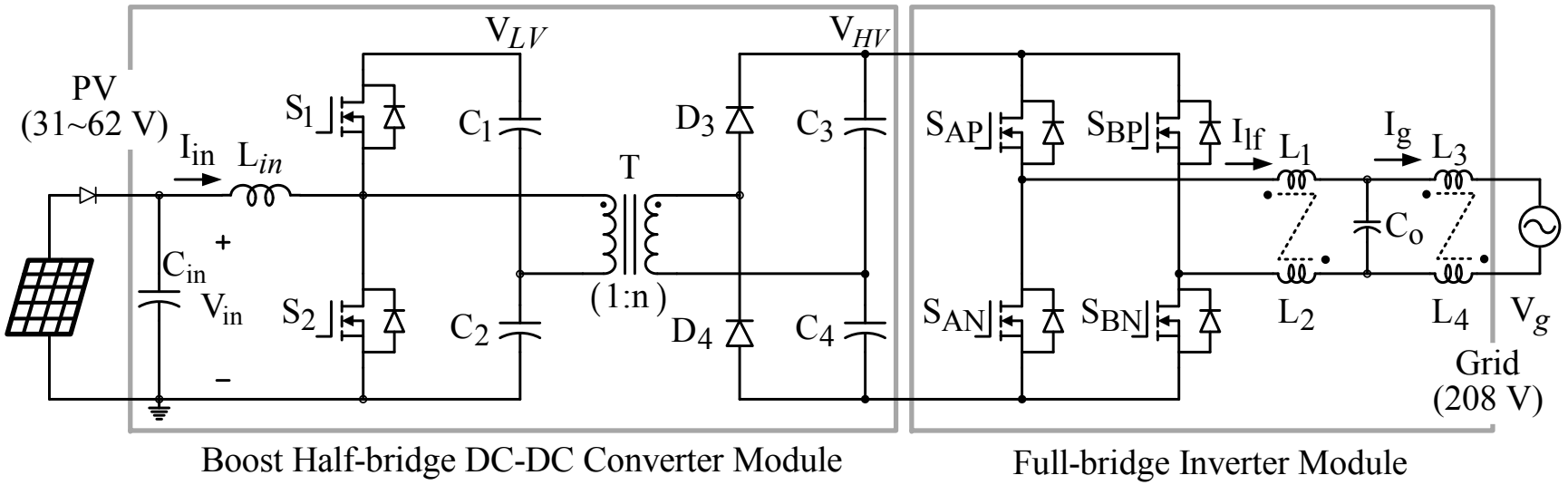


Figure 10.1 Proposed boost half-bridge micro-inverter main circuit structure.

The full-bridge converter utilizes four active switches, which is more suitable for high power (> 1 kW) application. In the low power (around 200 W) micro-inverter application, the full-bridge dc-dc converter solution may increase the total system cost. Traditional half-bridge dc-dc converter can be considered as a buck converter in the primary side, and the transformer primary side voltage is only one half of the input voltage, which makes it more suitable for the voltage step-down application. At the same time, the sever voltage overshoot across the secondary side diode also limits the application of full-bridge and half-bridge with high output voltage. Generally speaking, the dc-dc converter topologies with a voltage fed primary side are more suitable for the voltage step-down application with high input voltage and low output voltage such as communication power supply. The dual structure of the above voltage-fed dc-dc converter is the current fed dc-dc converter with inductors or boost type input structure are more suitable for the voltage step-up applications [255, 337]. However, the dual circuit of the traditional voltage-fed half-bridge dc-dc converter or double-L dc-dc converter suffer server voltage overshoot problem across the primary side switches. Complicated clamping circuits are required to limit the primary switch voltage overshoot, which increase the total cost and reduce the system reliability [255]. The proposed boost half-bridge dc-dc converter has capacitors across the both primary side active switches and the secondary diodes, which can eliminate the voltage spike across the switches by proper circuit layout. Different from the traditional voltage-fed symmetrical half-bridge dc-dc converter with duty cycle control, the two switches of the proposed boost half-bridge converter is controlled complimentarily. The transformer is fully utilized at both switching periods to transfer the energy. If the leakage inductance of the transformer is designed small enough; the leakage inductance current is almost square waveform with minimum rms value. In this way, the copper loss of the transformer and the switching

device conduction loss can be minimized. In the meanwhile, if the leakage inductance of the transformer is designed relatively large, the energy stored in the leakage inductance can also be used to achieve the zero voltage switching of the primary side devices. The proper design and selection of the transformer leakage inductance should be a trade off with different application.

Figure 10.2 shows the primary referrer equivalent circuit of the boost half-bridge dc-dc converter. The transformer is replaced by its equivalent circuit with two leakage inductance L_1 and L_2 a magnetizing inductance L_m. The leakage inductance is used to transfer the energy from the primary side to the secondary side. Different from the bidirectional boost half-bridge dc-dc converter using the phase shift of the primary side switch and the secondary switch, the secondary diode of the proposed topology will conduct automatically when the transformer primary side voltage V_{trP} is higher than the secondary side voltage V_{trS}. The energy can only transferred from the primary side to the secondary side, so the referred voltage of the secondary side V_3 and V_4, will always smaller than V_1 and V_2. C_{S1} and C_{S2} are the parasitic capacitance of MOSFETs S_1 and S_2.

Figure 10.3 shows the idealized voltage and current waveforms of the transformer, when the transformer leakage inductance is relatively large (>1 uH) and the capacitance of capacitor $C_1 \sim C_4$ is large enough. If the transformer leakage inductance is extremely small (≈ 10 nH), or the capacitance of the capacitor $C_1 \sim C_4$ is too small, the transformer current will become quasi-square waveform or resonant waveform, which is out of the scope of this chapter. Assume one switching period is 2π, the conduction time of switch S_1 and S_2 is 2πD and 2π(1-D) respectively. The sum of the leakage inductance L_1 and L_2 is L_S.

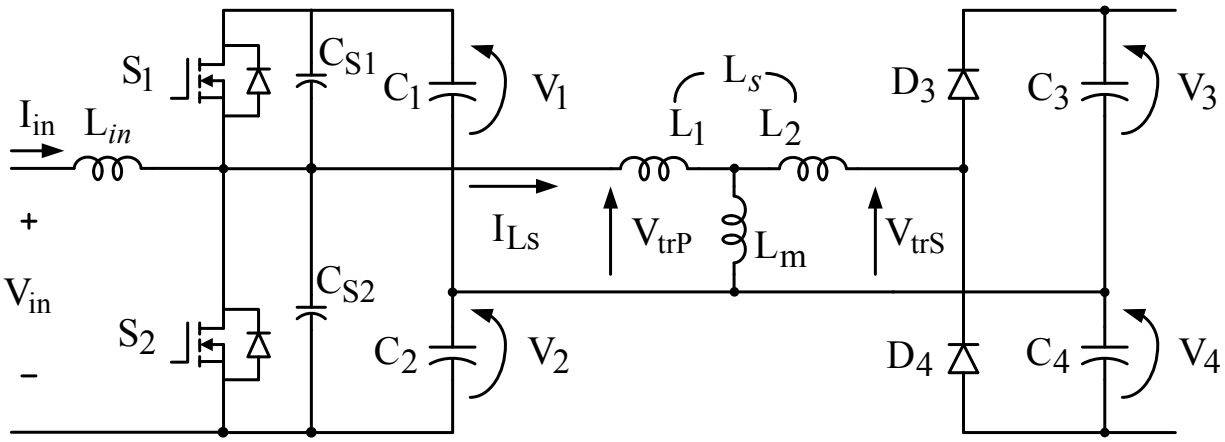


Figure 10.2. Primary referred equivalent circuit of the dc-dc converter

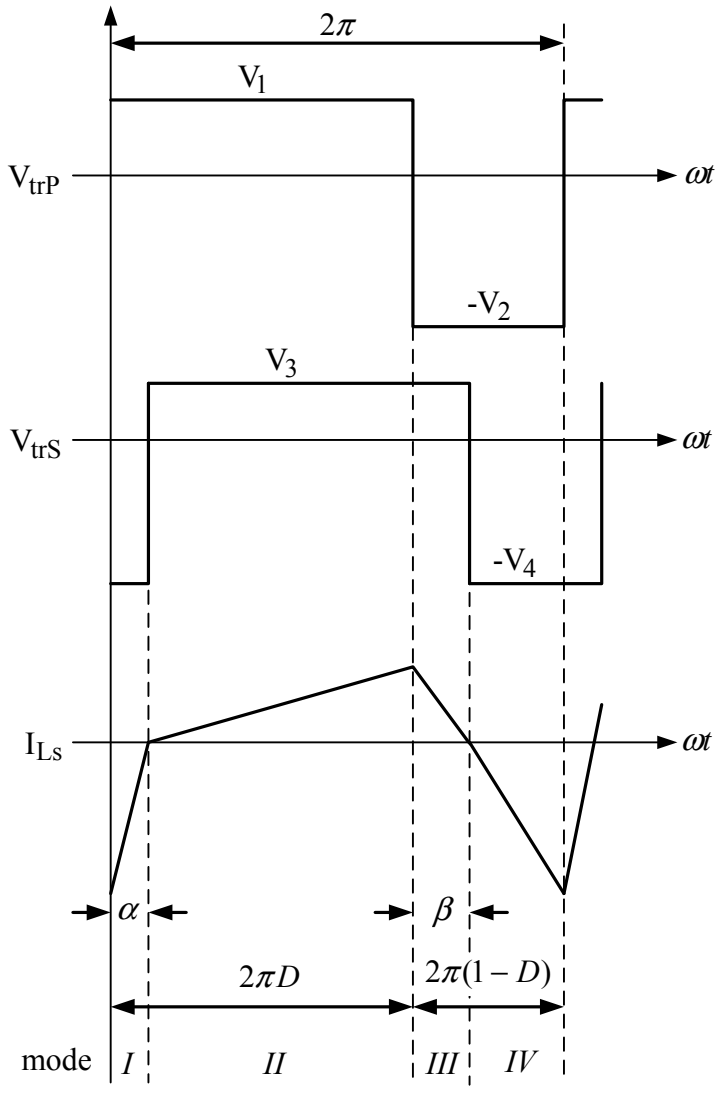


Figure 10.3. Idealized voltage and current waveform of transformer.

During one switching period, there are four operation modes. The switching frequency is ω.

In mode I, (0<θ<α) the transformer current can be calculated as,

$$I_{Ls}(\theta) = \frac{V_1 + V_4}{\omega L_s}\theta + I_{Ls}(0) \tag{1}$$

In mode II (α<θ<2πD), the transformer current is,

$$I_{Ls}(\theta) = \frac{V_1 - V_3}{\omega L_s} + I_{Ls}(\alpha) \tag{2}$$

In mode III (2πD<θ<2πD+β), the transformer current is,

$$I_{Ls}(\theta) = \frac{-V_2 - V_3}{\omega L_s}\theta + I_{Ls}(2\pi D) \tag{3}$$

In mode IV (2πD+β<θ<2π), the transformer current is,

$$I_{Ls}(\theta) = \frac{-V_2 + V_4}{\omega L_s}(\theta - 2\pi D - \beta) + I_{Ls}(2\pi D + \beta) \tag{4}$$

According to the boundary conditions of transformer current,

$$\begin{aligned} &I_{Ls}(\alpha) = I_{Ls}(2\pi D + \beta) = 0, \\ &I_{Ls}(0) = I_{Ls0}, I_{Ls}(2\pi D) = I_{Ls2\pi D} \end{aligned} \tag{5}$$

And according to the transformer primary side and secondary side voltage-secondary balance, one can derive,

$$V_1 D = V_2(1 - D) \tag{6}$$

$$V_3(2\pi D + \beta - \alpha) = V_4(2\pi - 2\pi D + \alpha - \beta) \tag{7}$$

Since for this topology, the transformer current is also pure ac during one switching period, one can get,

$$I_{Ls2\pi D}(2\pi D + \beta - \alpha) = -I_{Ls0}(2\pi - 2\pi D + \alpha - \beta) \tag{8}$$

From the representation of the transformer current $I_{Ls}(\theta)$, and the transformer primary side voltage $V_{trP}(\theta)$, which can be derived very easily from the figure, and assume the input power is equal to the output power, the output power can be derived as,

$$P_O = \frac{1}{2\pi}\int_0^{2\pi} I_{Ls}(\theta) V_{tr}(\theta)\, d\theta \tag{9}$$

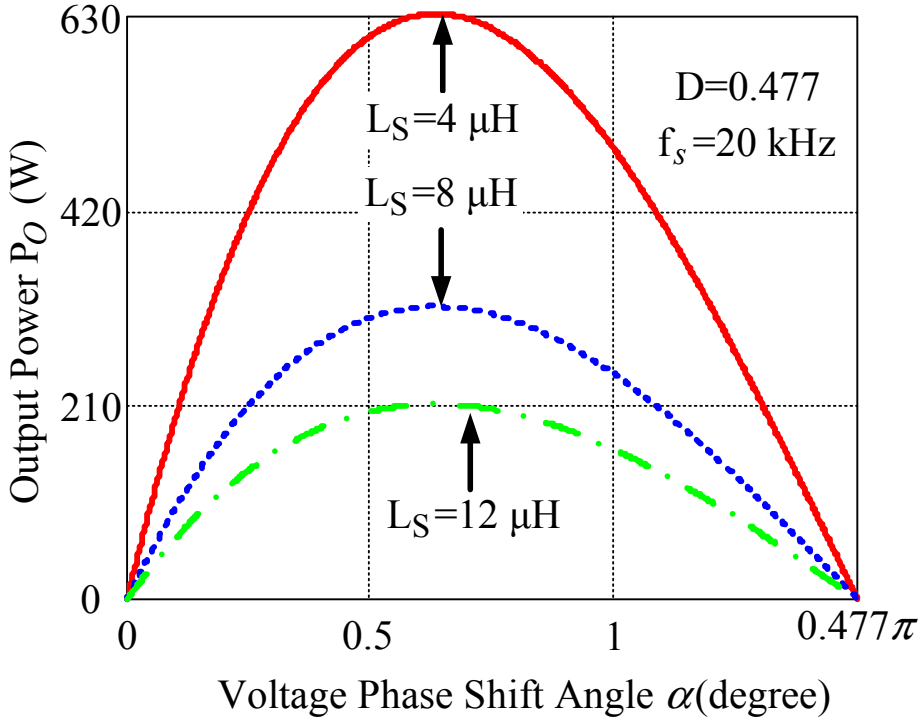
which is equal to

$$P_O = \frac{{V_{LV}}^2 \cdot D \cdot \alpha (1-D)^2 (\alpha - 2\pi D)(\pi D - \alpha)}{L_s \cdot \omega\left(2\pi D^2 - 2\alpha D + \alpha\right)\left(\alpha - 2\pi D - 2\alpha D + 2\pi D^2\right)} \tag{10}$$

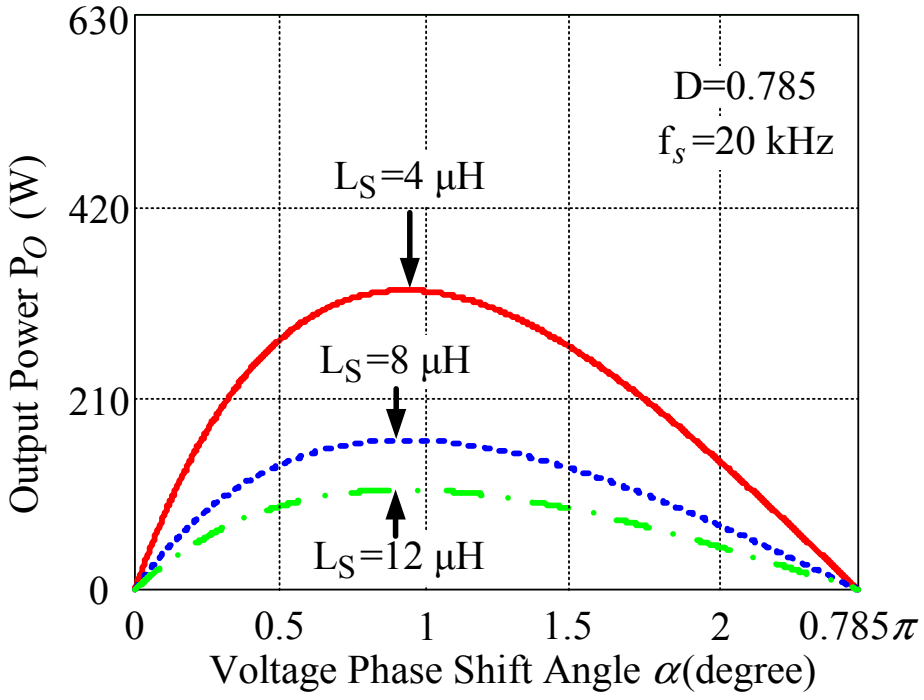
According to (10), the output power is a function of duty cycle, voltage phase shift angle, leakage inductance value, and the switching frequency, assuming the low dc-link voltage is constant. Since the transformer primary side can be considered as a boost converter, with the change of the input voltage, the low dc-link voltage can controlled with a constant value. Figure 10.4 (a)~(d) shows the output power P_O versus voltage phase shift angle α with different leakage inductance, duty cycle and switching frequency using our 210 W design as an example. The input voltage range of the PV panel to achieve MPPT is 31 V ~ 51 V, and the low voltage dc-link is set to be 65 V. With the change of input voltage, the duty cycle will change from 0.477 to 0.785. Figure 10.4(a) shows the case when the duty cycle is 0.477 or input voltage is 31 V and the switching frequency is 20 kHz with the different leakage inductance. It can be derived from the figure that with the increase of leakage inductance, the power transfer capability is reduced. So in order to ensure the output voltage is larger than the desired value, a maximum leakage inductance value should be determined. Figure 10.4(b) shows the case when the input voltage is 51 V or the duty cycle is 0.785 with 20 kHz switching frequency. The maximum leakage inductance limitation can also be derived from the figure with fixed power transfer capability. At the same time, the maximum leakage inductance value has to be reduced at this duty cycle.

Figure 10.4(c) shows the case when the leakage inductance is 6 μH and switching frequency is 20 kHz with different duty cycles. It can be proved that when the duty cycle is 0.5, the power transfer capability is highest with determined leakage inductance and switching frequency. The proof will not be provided here due to the page limitation. And when the duty cycle is other values, the maximum power transfer capability is reduce accordingly. So leakage inductance has to be designed smaller than the worst case duty cycle value with the minimum power transfer capability. In our design duty cycle 0.785 with 51 V input voltage is the worst case.

Figure 10.4(d) shows the case when the leakage inductance is 6 μH, the duty cycle is 0.5 with different switching frequencies. With the increase of switching frequency, the power transfer capability is also reduced. Therefore, the proper switching frequency has to be selected according to the power level and the leakage inductance value. In our design, the switching frequency is selected to be 20 kHz, to ensure the non-audible noise and maximum power transfer capability.



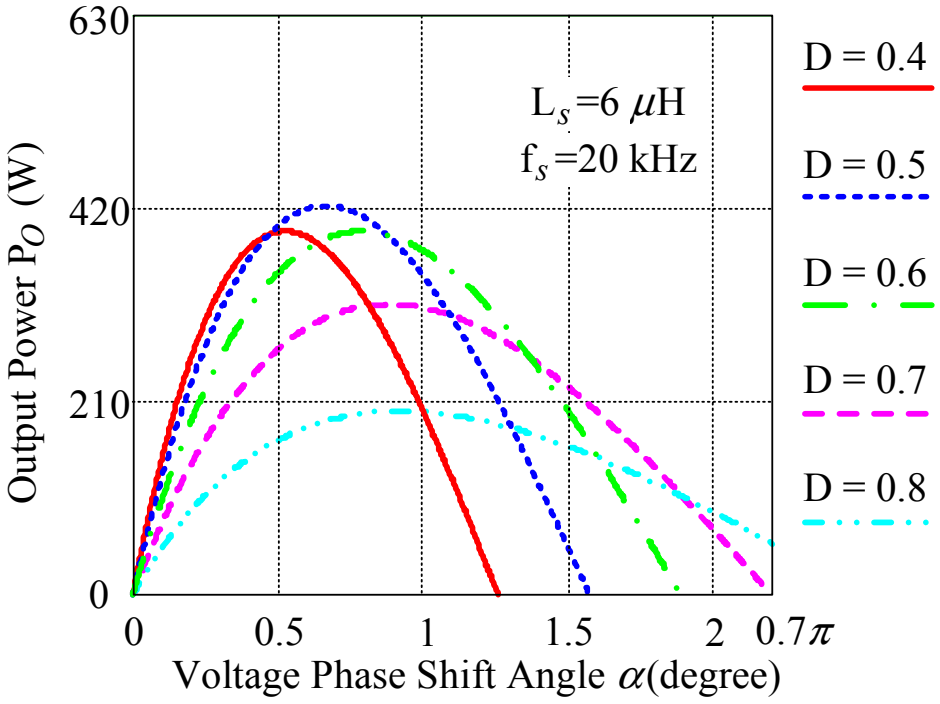
(a)



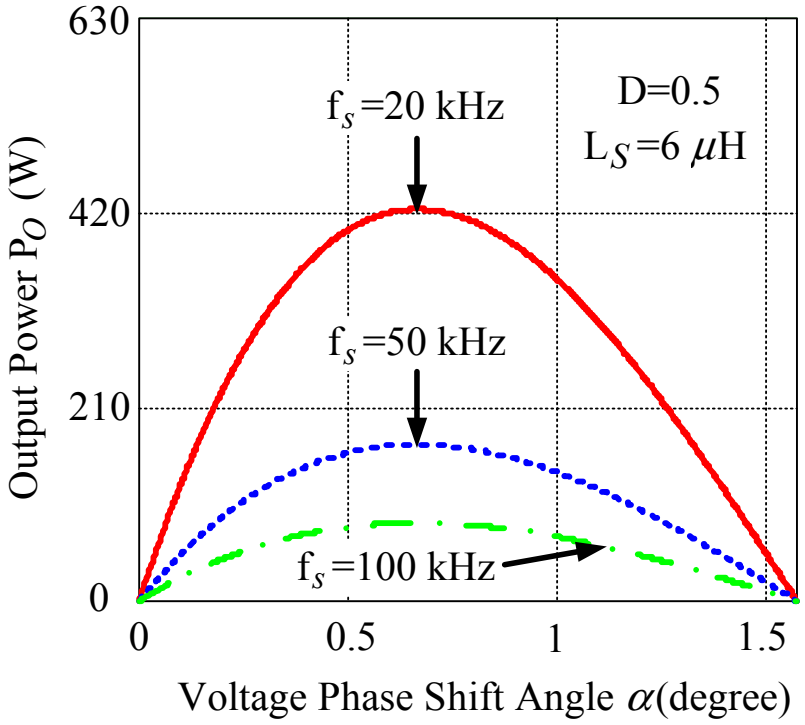
(b)

Figure 10.4 Output power P_o versus phase shift angle α with different the leakage inductance L_S, duty cycle D, and switching frequency f_s.

Figure 10.4 cont'd



(c)



(d)

10.3 Soft-switching Operation Principles of the DC-DC Converter Module

When the leakage inductance is large enough to store the energy to discharge the energy of the device parasitic capacitor, the ZVS of the first stage boost half-bridge dc-dc converter can be achieved with the proper selection of deadtime. In this section, the ZVS operation of the first stage boost half-bridge dc-dc converter will be analyzed and discussed. In order to simplify the circuit analysis, the primary referred equivalent circuit is drawn in Figure 10.2 is used for analysis, where the transformer is replaced with a leakage inductance and a magnetizing inductance. Figure 10.5 shows the commutation steps in one switching cycle. Figure 10.6 shows the idealized waveforms and switching time in one switching cycle.

- ($t_1 \sim t_2$): The circuit is in steady state, the switch S_1 is conducted, the diode D_3 is conducted, the energy is transferred from the primary side to the secondary side, as shown in Figure 10.5(a).
- ($t_2 \sim t_3$): At t_2, the switch S_1 is turned off, the leakage inductance begin to resonant with the switch parasitic output capacitor C_{S1} and C_{S2}, since these two capacitors can be selected big enough to make the charge of the capacitor C_{S1} long enough than the switch S_1 turn off time, the zero voltage turn off of the switch S_1 can be achieved. The leakage inductor continues to discharge the capacitor C_{S2} until the voltage across this capacitor drop to zero, as shown in Figure 10.5(b).
- ($t_3 \sim t_4$): At t_3, the capacitor C_{S2} voltage drop to zero, and the parasitic diode D_2 of switch S_2 is conducted naturally as shown in Figure 10.5(c).
- ($t_4 \sim t_5$): At t_4 switch S_2 can be turned on at zero voltage, since the body diode has already

conducted. The secondary diode current begin to change from D_3 to D_4, as shown in Figure 10.5(d).

- ($t_5 \sim t_6$): At t_5 diode D_3 is turned off completely, and diode D_4 begin to conduct, the circuit enter into another steady state as shown in Figure 10.5(e). During this period, the energy is transferred from the primary side to the secondary.
- ($t_6 \sim t_7$): At t_6 the switch S_2 is turned off, the output capacitor C_{S1} of the switch S_1 begin to discharge while the output capacitor C_{S2} of the switch S_2 begin to charged by the input current and the transformer current I_{Ls}. The switch S_2 is turned off at zero voltage as shown in Figure 10.5(f).
- ($t_7 \sim t_8$): At t_7 the capacitor C_{S1} voltage is discharged to zero, the parasitic diode D_1 of the switch S_1 is turned on naturally.
- ($t_8 \sim t_9$) At t_8 the top switch S_1 can be turned on with zero voltage switching since the diode D_1 has already conducted. From t_9 the next switching cycle begins, which is the same as the time t_1.

If the parasitic capacitance of the MOSFETs S_1 and S_2 is not big enough, a relatively large capacitor has to be added in parallel with the switch to ensure the zero voltage turn off. The zero voltage turn on of the bottom switch S_2 is determined by the current in the leakage inductance, when the load is light or the leakage inductance is not big enough, zero voltage turn on cannot be achieved. Since the energy stored in the leakage inductance should be larger than the energy stored in the capacitor C_{S2}. And the capacitor C_{S1} is discharged by the input current and the transformer leakage inductance current at the same time. So the zero voltage turn on of the top

switch S_1 can be achieved easier than the bottom switch S_2. With light load or small leakage inductance, the ZVS of these two switches cannot be achieved.

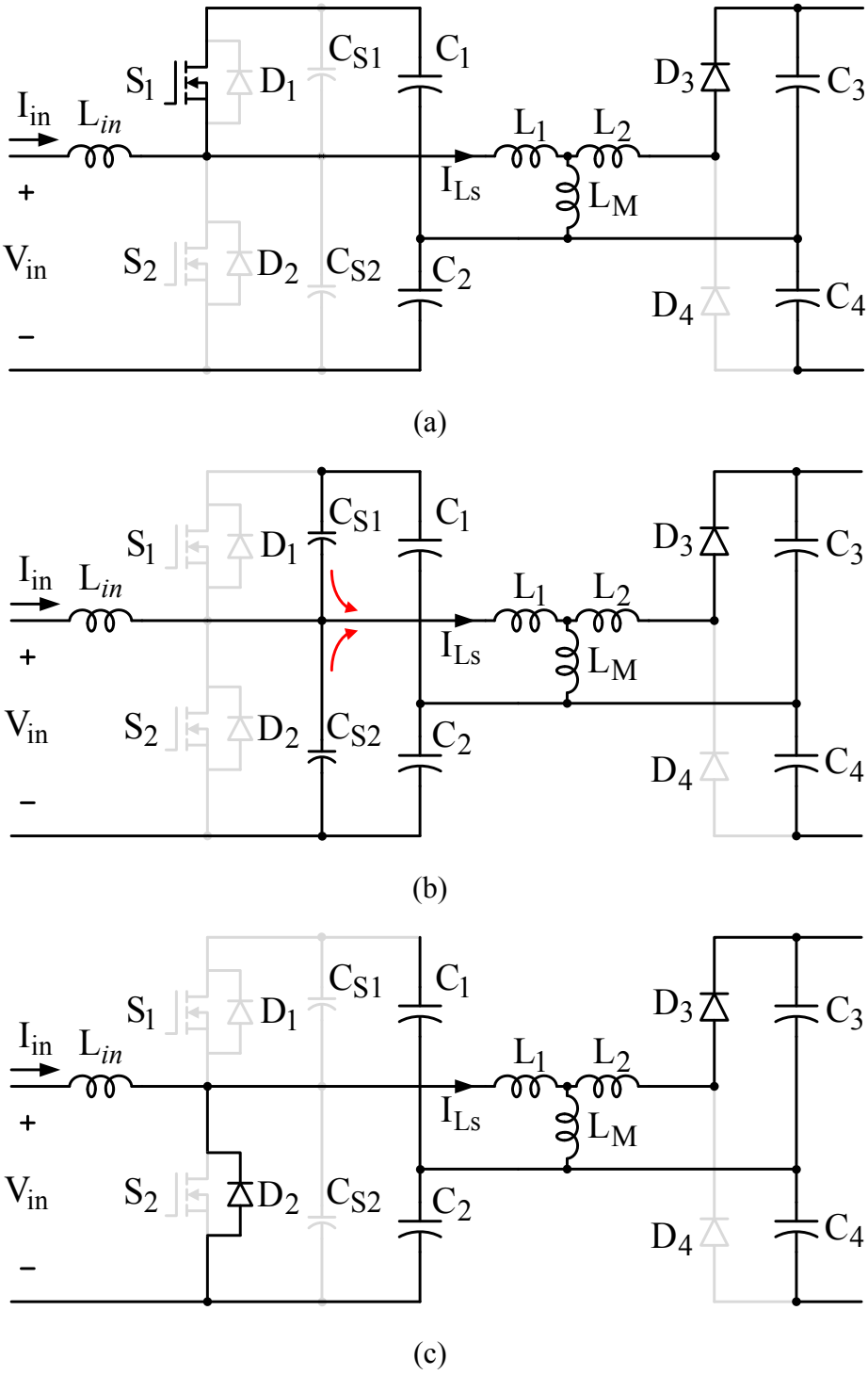
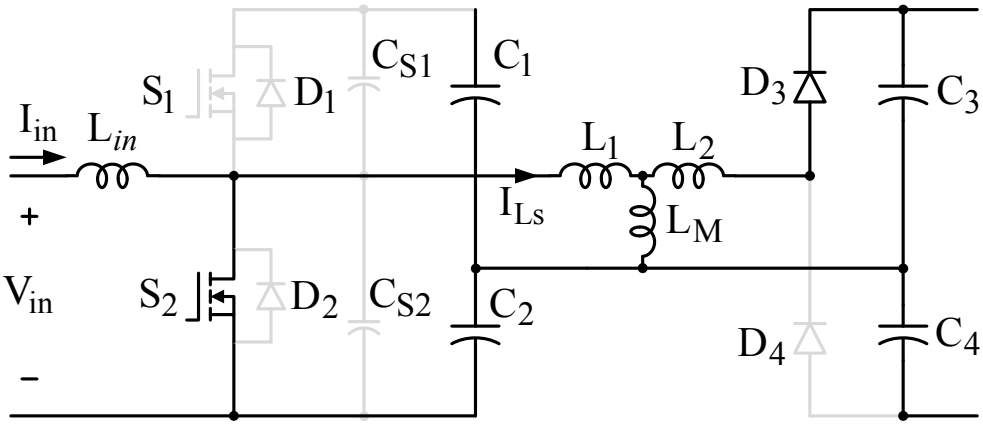
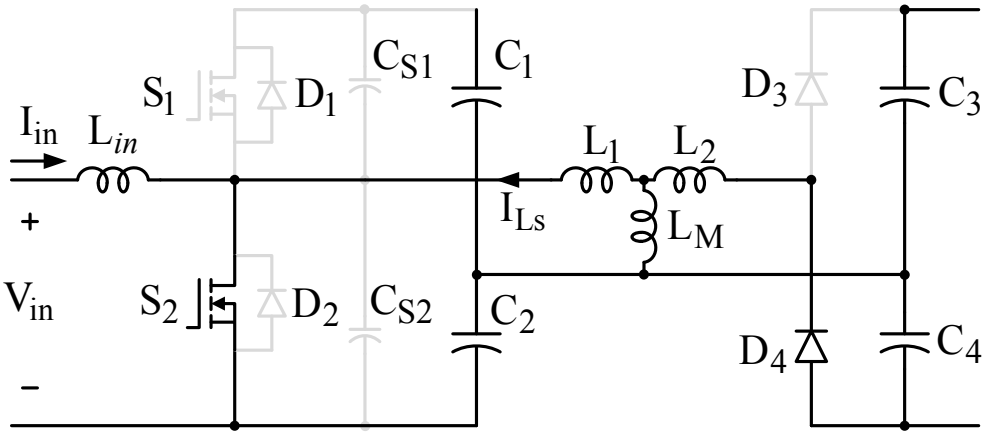


Figure 10.5 Commutation step diagrams during a switching cycle.

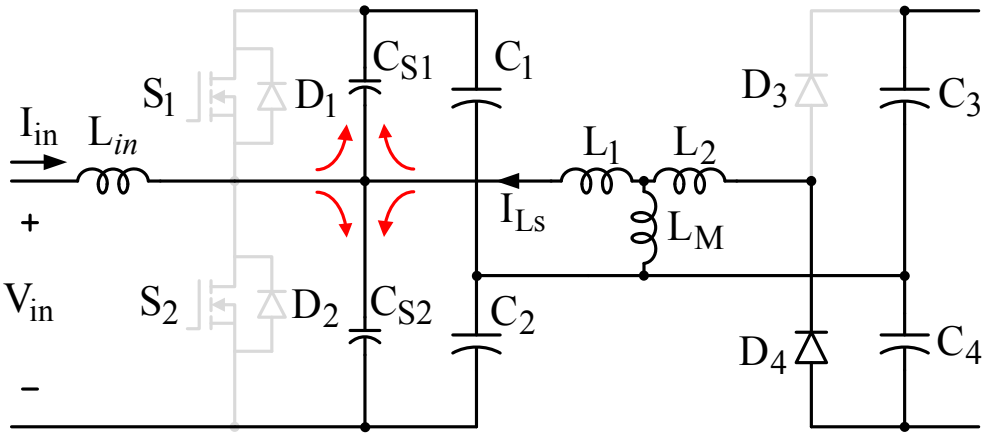
Figure 10.5 cont'd



(d)

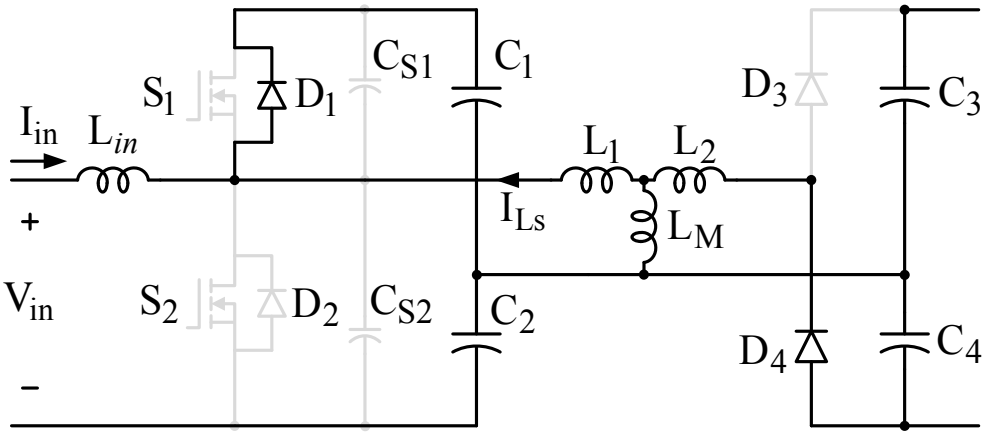


(e)

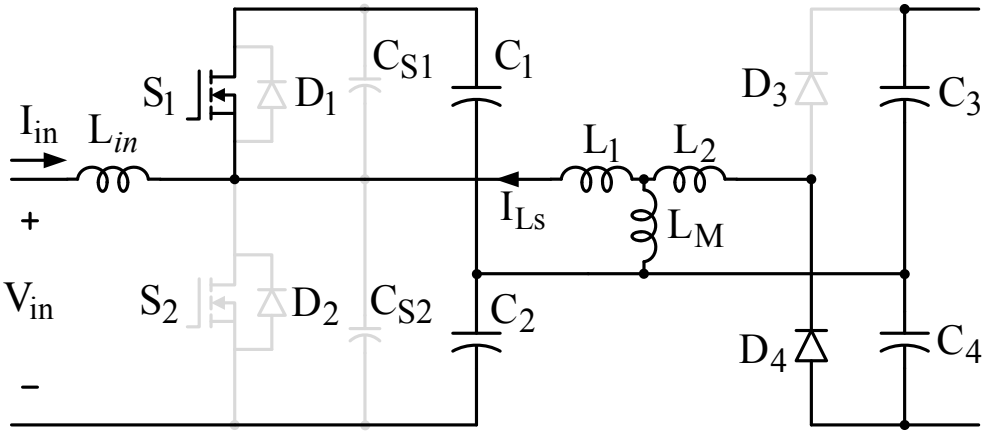


(f)

Figure 10.5 cont'd



(g)



(h)

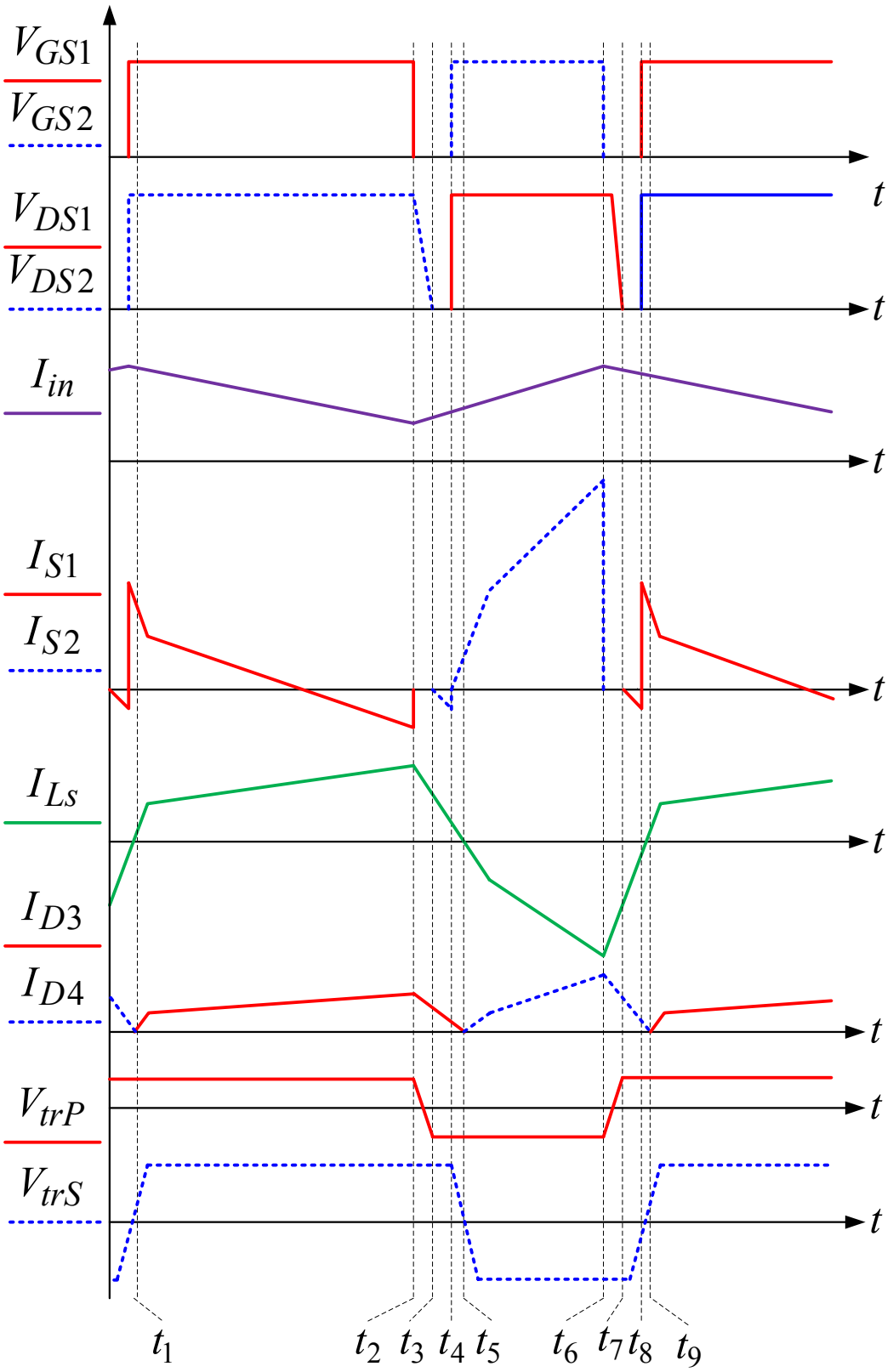


Figure 10.6. Waveforms and switching timing one switching cycle.

10.4 Control Strategy

Figure 10.8 shows the system control block diagram. Four voltage sensors and two current sensors are used. The input voltage V_{PV} , primary side low dc-link voltage V_{LV} , secondary side high dc-link voltage V_{HV} , and the grid voltage v_{grid} are sensed. The input current I_{PV} and the inverter output current i_{inv} are sensed. The MPPT is realized by the dc-dc converter by controlling the input dc voltage. The perturb and observe (P&O) MPPT algorithm is used to track the irradiation of PV panel. The low dc link voltage is controlled by the inverter output current. The inverter grid voltage is sensed to calculate the inverter current reference and the feed-forward for the inverter current controller. A repetitive current controller is used to generate the synchronized low THD sinusoid inverter current.

10.5 Prototype and Experimental Results

A 210 W micro-inverter prototype is built and tested. The system specification is provided in Table 10.1. The transformer leakage inductance is about 2 μH. The PV panel used for the prototype test is HIT210 from Sanyo.

Table 10.1 System specification

PV output voltage	31 V~ 51 V
Peak PV power	230 W
Norminal power	210 W
Input Inductance L_{in}	200 uH
Low DC link voltage	65 V
DC-DC switching frequency	21.6 kHz
Transformer Turns Ratio	1 : 6
High DC link voltage	370 V
Filter inductance $L_1 \sim L_4$	4.25 mH
Fillter capacitance C_o	330 nF
Output voltage	179 V ~ 232 V
Output current	1 A
Inverter switching frequency	10.8 kHz

Figure 10.7 shows output inductor L_1 and L_2 current ripple distribution with the change of duty cycle and modulation index, this can be used for the inductor core loss estimation for the inductor design and optimization.

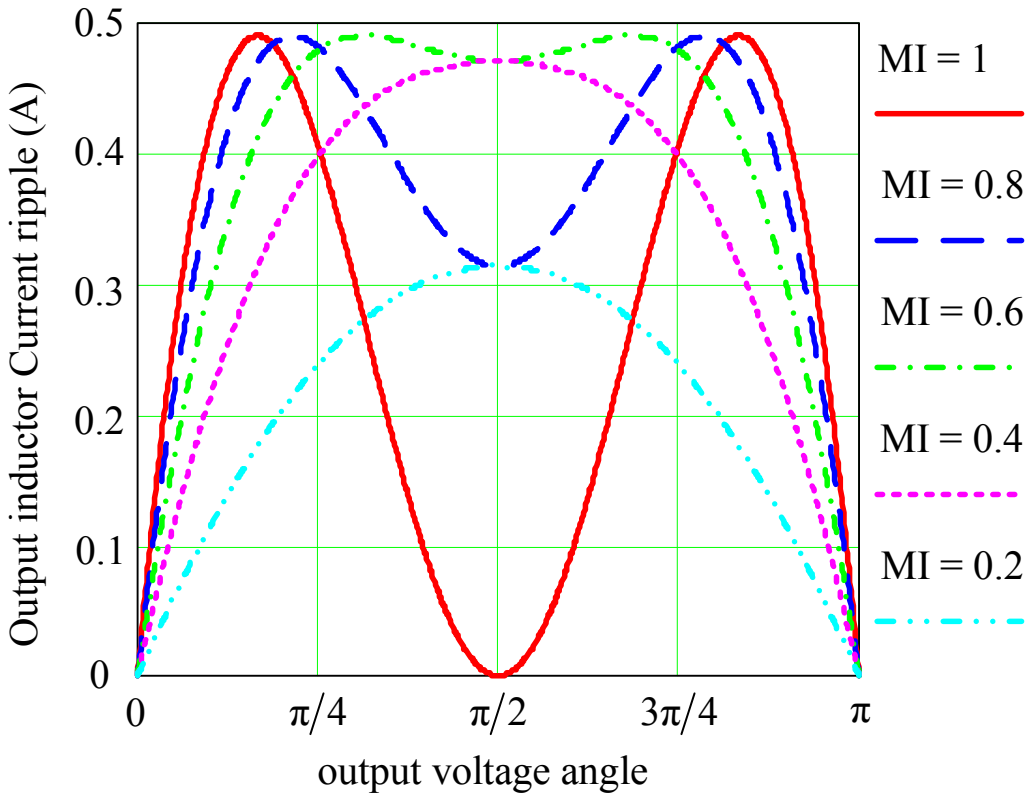


Figure 10.7 Output inductor current ripple with the change of output voltage angle with different modulation index.

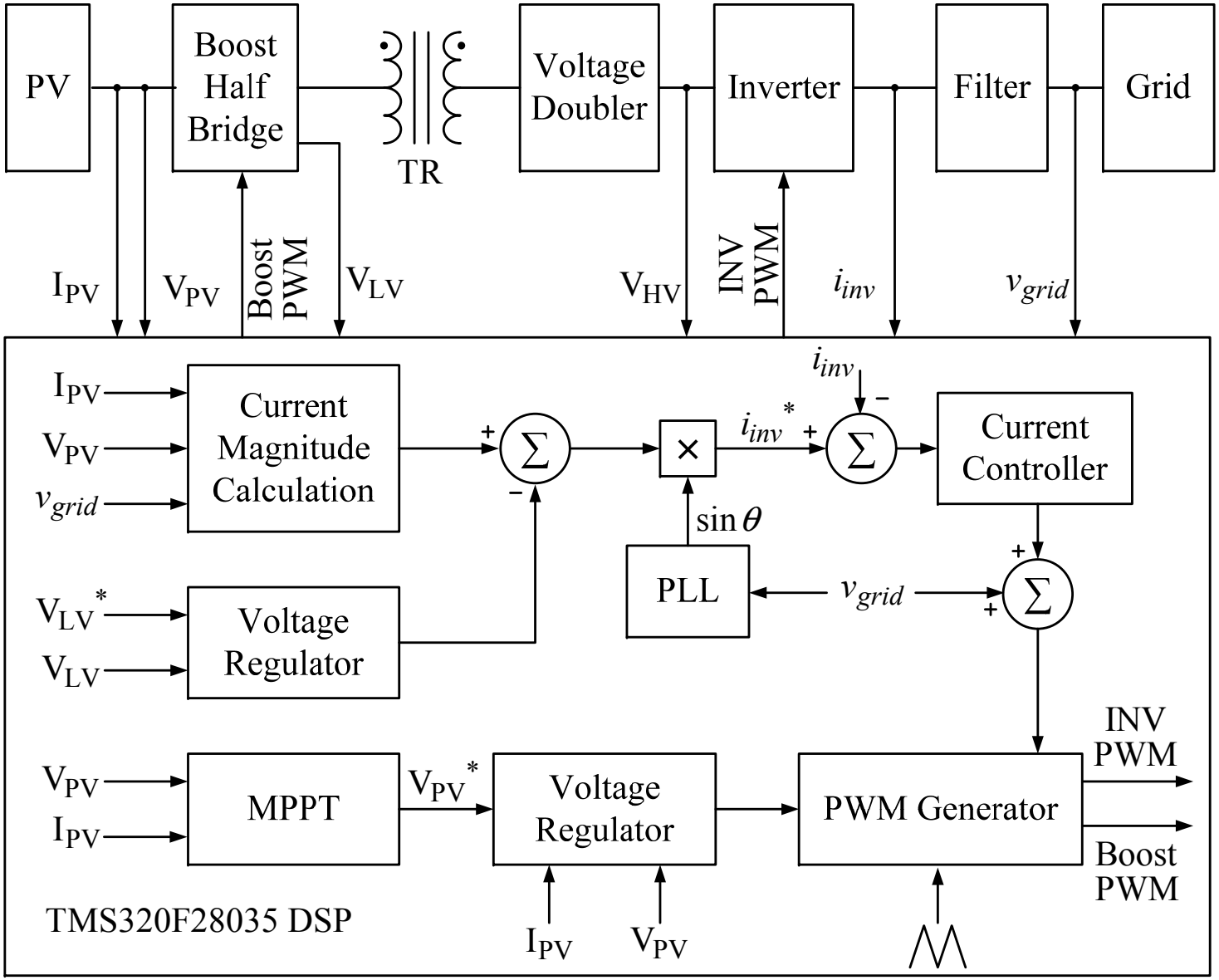


Figure 10.8. System control block diagram.

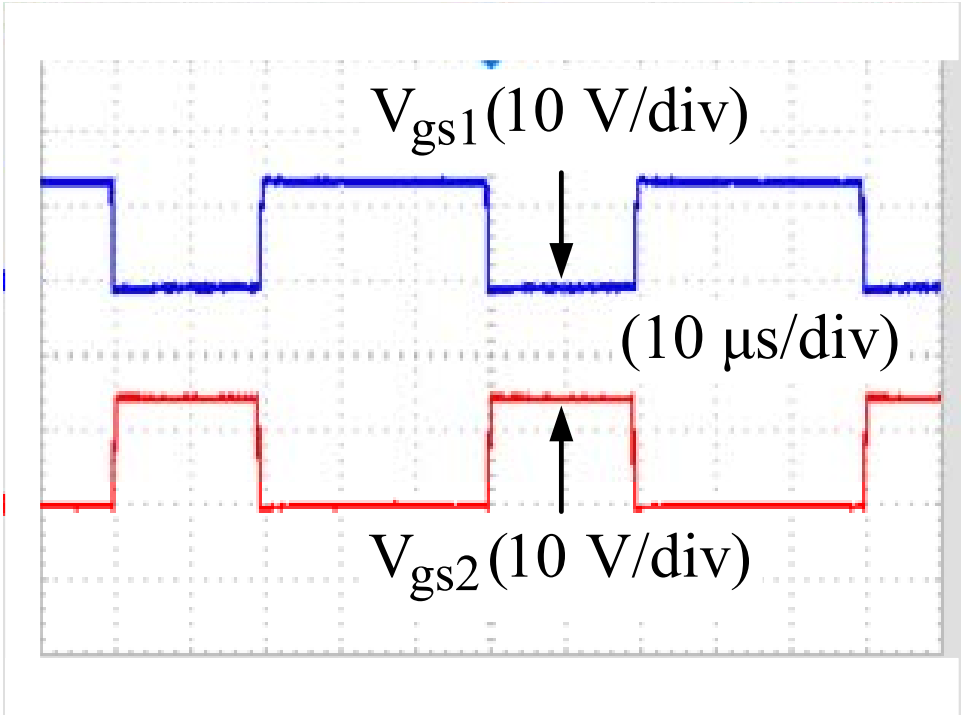
Figure 10.9 ~ Figure 10.11 shows the experimental results and the measured dc-dc converter at maximum power point with about 40 V input voltage. These tests results show the most frequent operation point to verify the proposed circuit basic function and operation. Figure 10.9(a) shows the complementary control signals of switch S_1 and S_2. Figure 10.9(b) shows the switch S_2 gate-source voltage V_{gs2}, drain-source voltage V_{ds2} and the transformer current I_{Ls}. Figure 10.9(c) shows the zoomed in waveform of Figure 10.9(b), the zero voltage turn on is achieved. Figure 10.10(a) shows the transformer primary and secondary side voltage and the transformer current. Figure 10.10(b) shows the high voltage side voltage doubler diode voltage with transformer current. Figure 10.10(c) shows the low dc-link and high dc-link voltage and the transformer current, the ratio is the same as the transformer turns ratio, which is about six. Figure 10.11 shows the input voltage, input current, output voltage and output current of the proposed micro-inverter.

Figure 10.12 shows the input and output waveforms of the micro-inverter system with MPPT under different solar irradiance, when the solar irradiance is suddenly increased from partial shading to the full irradiance. According to the datasheet of the PV panel HIT210 from Sanyo, the peak irradiance during the experiment is about 880 W / m^2 at about 50 ºC.

Figure 10.13(a) shows the measured efficiency of the boost half-bridge dc-dc converter according to the PV panel output power. The PV panel is controlled by the dc-dc converter from the constant current region to the constant voltage region, the output voltage is from 30 V to 50 V. By measuring the efficiency of the PV panel from 30 V to 50 V, the close loop control of the boost dc-dc converter is verified which is robust enough to operate the PV panel from constant current region to the constant voltage region. Figure 10.13(b) shows the measured PV panel output power versus output voltage which is consistent to the PV panel datasheet. Figure 10.14

shows the measured efficiency of the boost half-bridge dc-dc converter and the total micro-inverter system including dc-dc converter, dc-ac inverter, LCL filter. The measurement points are according to the California Energy Commission (CEC) weighted efficiency measurement method published on its GoSolar website. Three different PV panel output voltages, which includes the constant current, maximum power point and constant voltage region, are used for the operation validation and efficiency measurement. Figure 10.14(a) shows the efficiency measurement curves of boost half-bridge dc-dc converter. Figure 10.14(b) shows the efficiency measurement curves of the total inverter system.

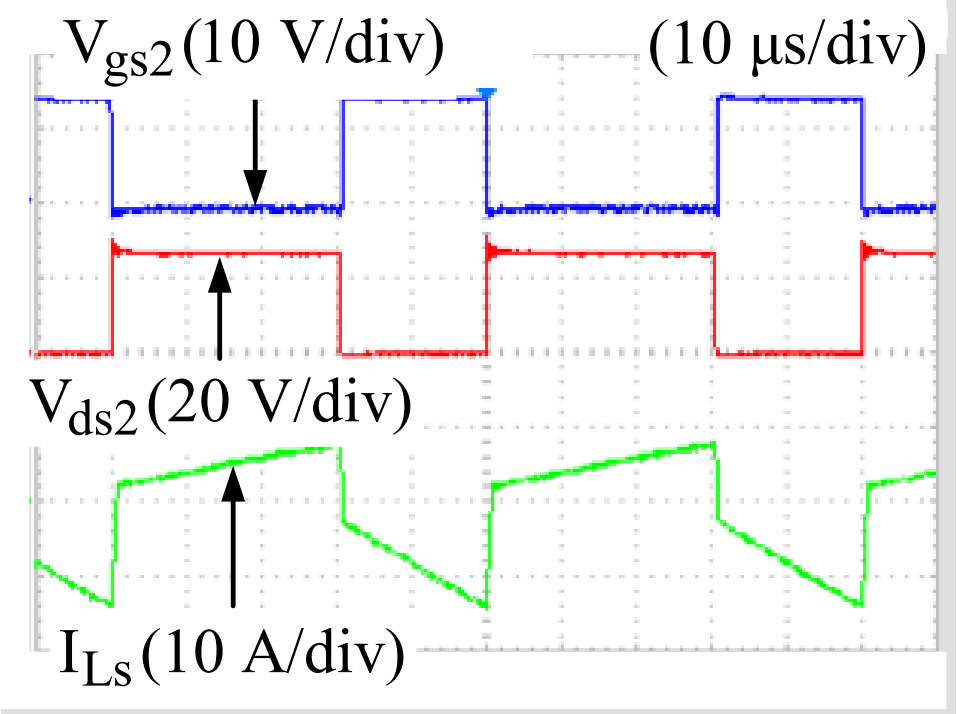
Figure 10.15 shows the prototype of the proposed micro-inverter. The total inverter size is about 20cm×80 cm×5cm, the picture of the prototype is taken by spreading the controller board and the main power board on the same surface.



(a)

Figure 10.9 (a) complimentary gate drive voltage of the primary two switches. (b) S2 gate-source and drain-source voltage with transformer current. (c) Zoomed in switch S2 ZVS turn on.

Figure 10.9 cont'd



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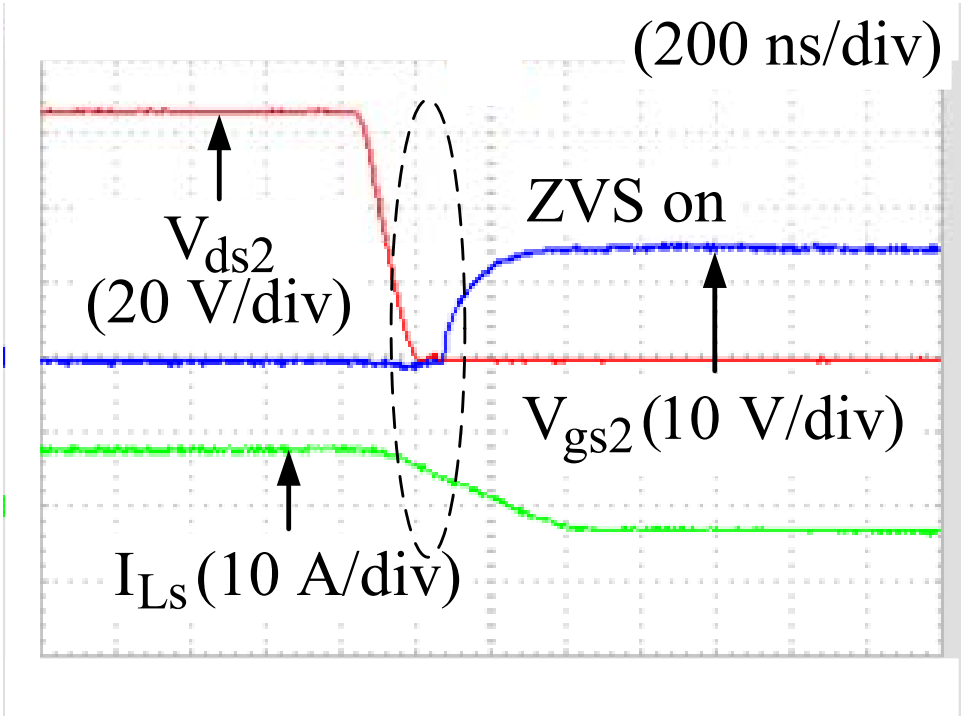

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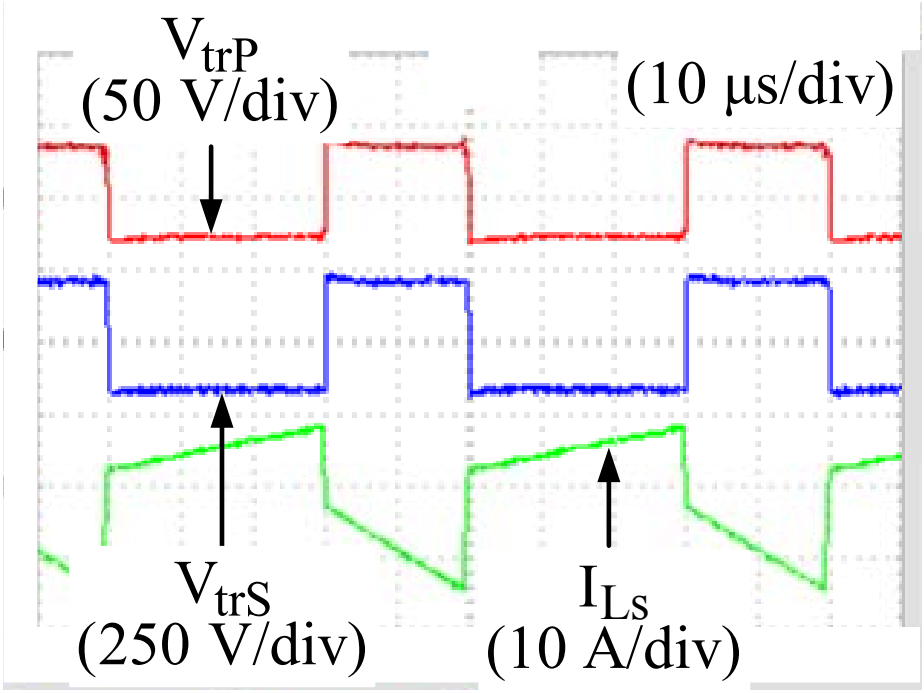
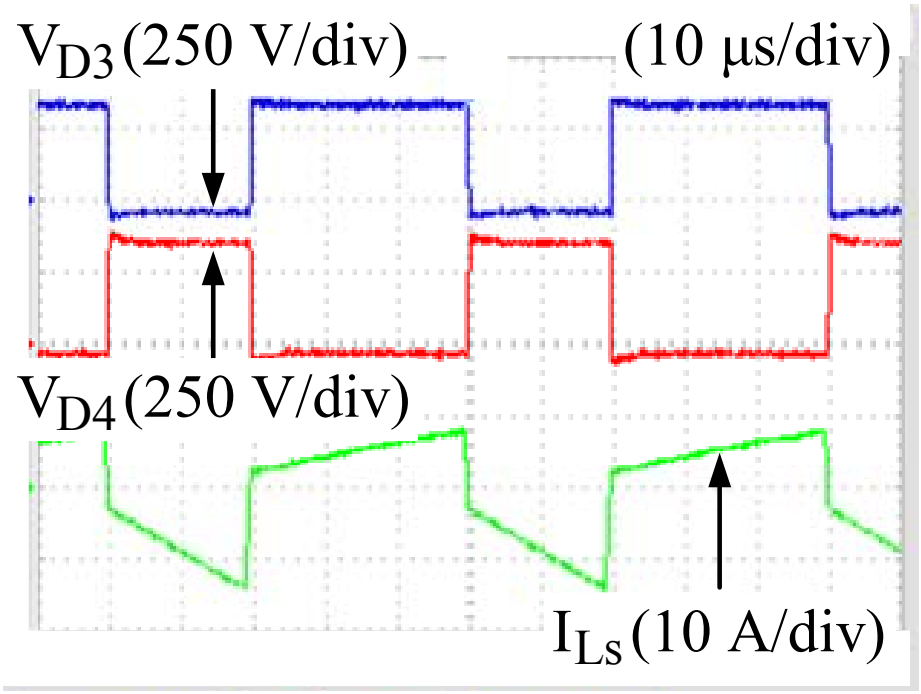


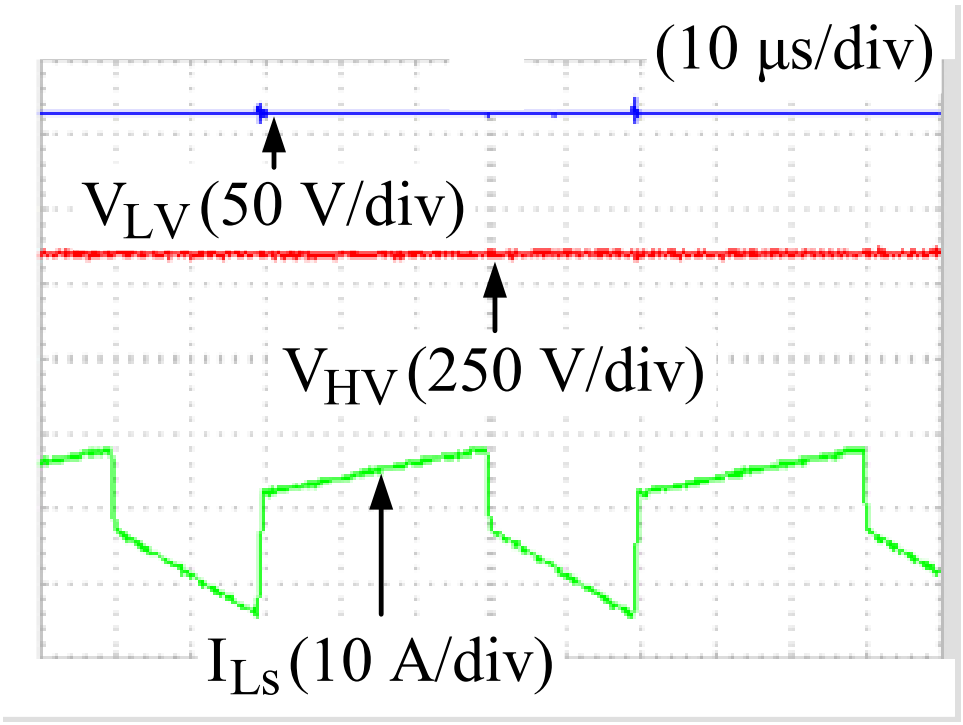
(a)



(b)

Figure 10.10 (a) Transformer input voltage, output voltage and current waveforms. (b) secondary side diode voltage and transformer current waveforms. (c) Low dc-link voltage, high dc-link voltage and transformer current.

Figure 10.10 cont'd



(c)

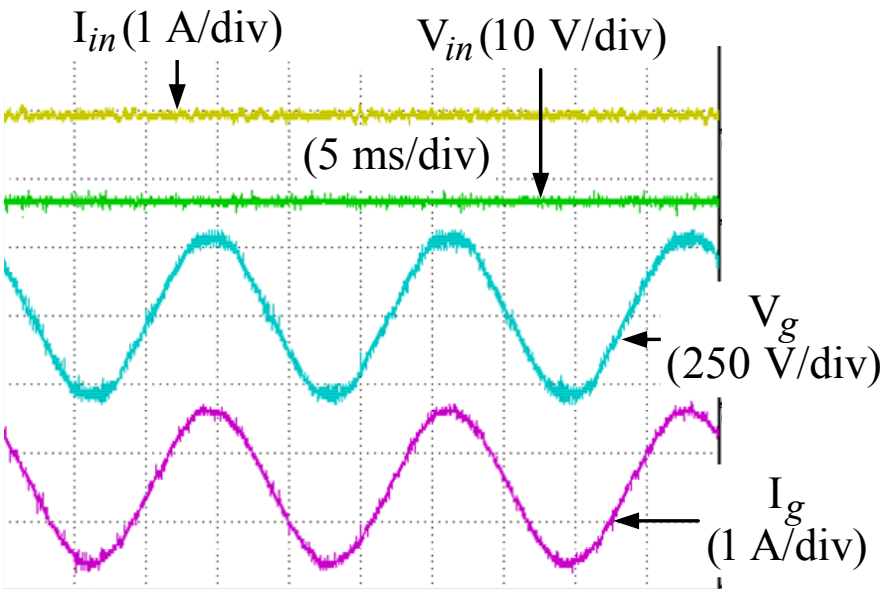


Figure 10.11 Input voltage, current, and the output voltage, current waveforms.

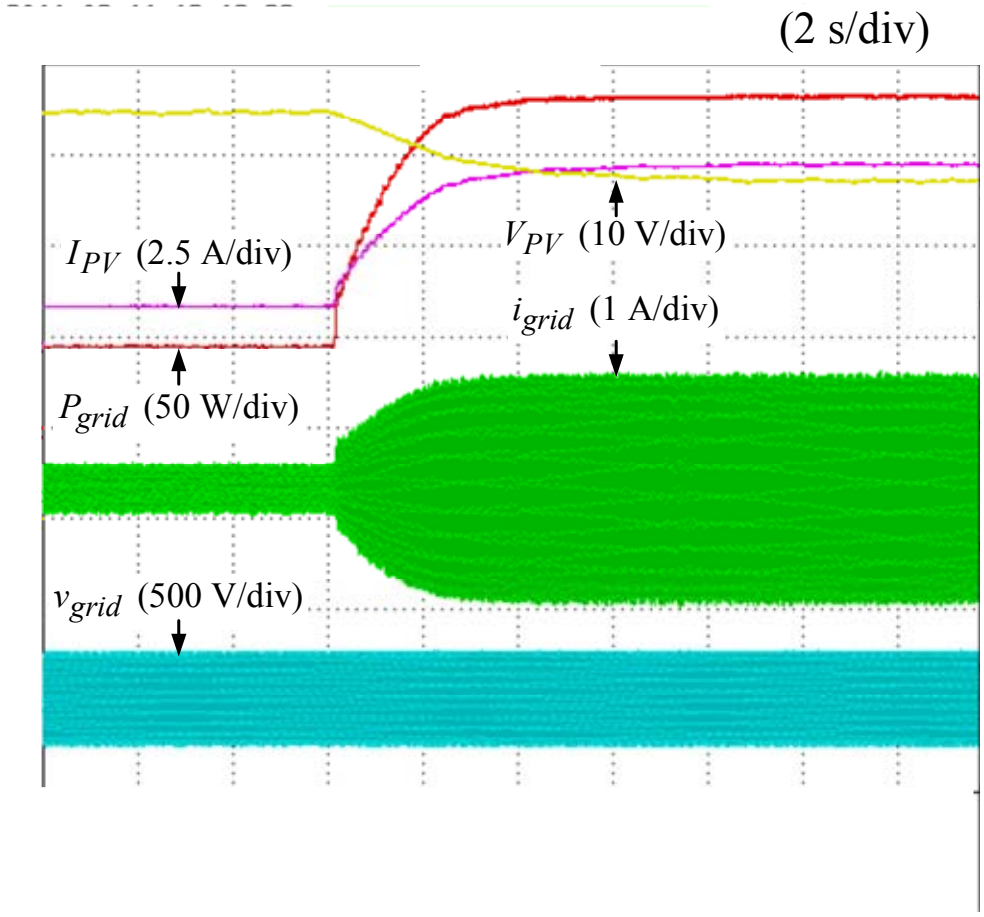


Figure 10.12 Input and output waveforms with MPPT of the PV micro-inverter system under solar irradiance change (from partial shading to 880 W / m^2 at 50 ºC).

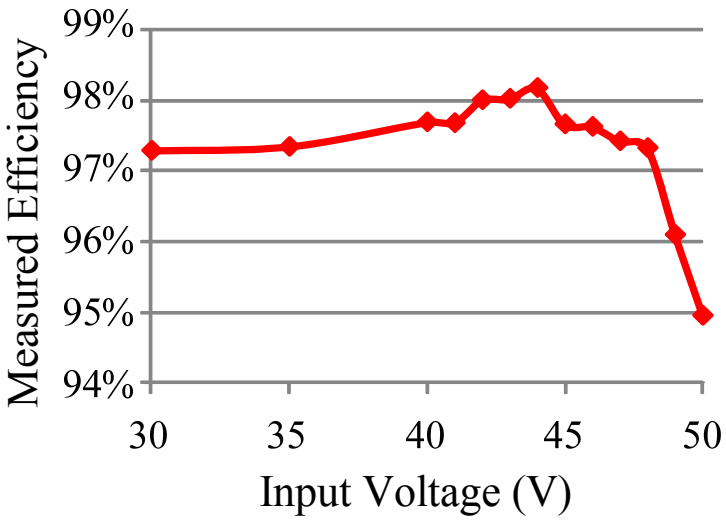
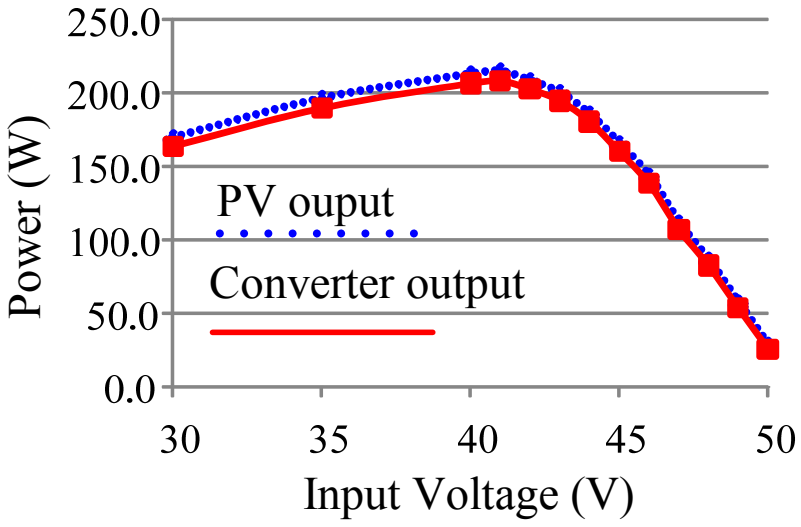


Figure 10.13 (a) Measured efficiency of the dc-dc converter according to the PV curve (b) PV panel output power versus voltage

Figure 10.13 cont'd



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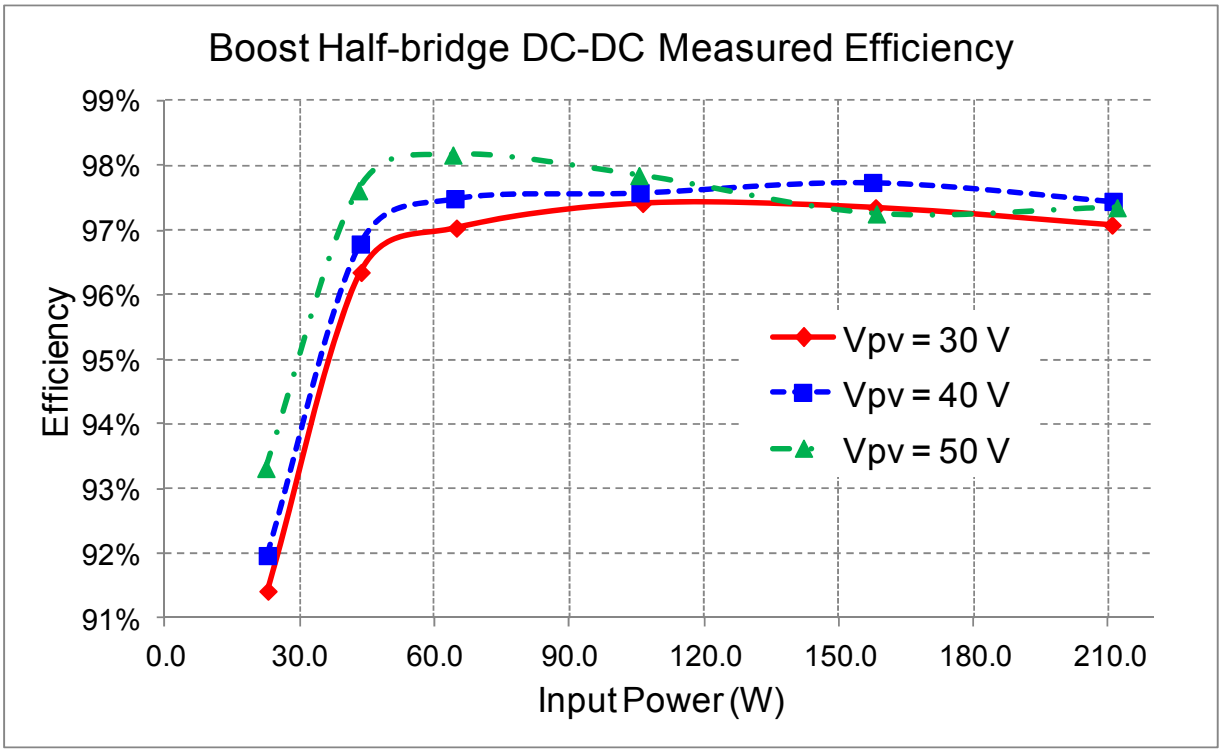
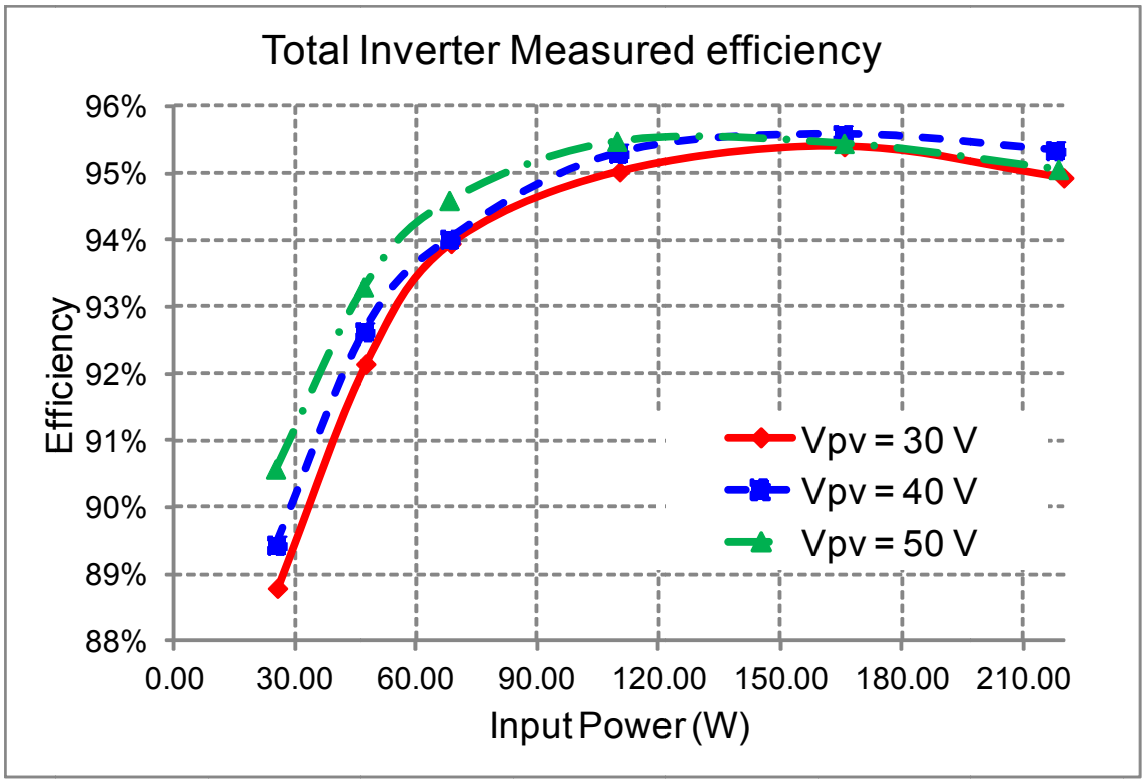


(a)

Figure 10.14 Measured efficiency at three different PV panel voltage (constant current region@30 V, maximum power point@40 V, constant voltage region@50 V) (a) Boost half-bridge dc-dc converter efficiency (b) Total micro-inverter system efficiency.

Figure 10.14 cont'd



(b)

Figure 10.15 Prototype picture of the proposed micro-inverter.

10.6 Conclusion

This chapter presents a transformer isolated boost half-bridge micro-inverter for the single-phase photovoltaic grid connected system. A low cost and high efficiency boost half-bridge dc-dc converter is proposed and analyzed. By using this topology with capacitors across all the active switches and diode, the voltage overshoot problem can be eliminated. The transformer is utilized fully to transfer energy with pure ac current, which can be designed with high efficiency. By utilizing the transformer leakage inductance, the ZVS of the primary switches can be achieved. Due to practical application requirement, this circuit can also be designed to operate at hard switching with high efficiency. The total system control strategy with MPPT and inverter current control is briefly discussed. A 210 W prototype using the proposed circuit is built, experimental results are provided to demonstrate the validity and features of the proposed circuit. The efficiency curve of the dc-dc converter according to the real PV panel output is also measured; up to 98.2% efficiency has been shown.

CHAPTER 11
Conclusion and Future works

11.1 Contributions

This work has the following contributions:

- Electrical characteristics of TEG modules in steady state and high frequency are proposed and modeled. The problems related to dc-dc converter design of TEG modules in automotive application are addressed. The problems of traditional step-up dc-dc converters and switched-capacitor dc-dc converters are summarized.
- A quasi-resonant soft switching strategy of utilizing the distributed stray inductance in the circuit for the switched-capacitor dc-dc converter is proposed. By using the proposed soft switching strategy, the high voltage and current spike of traditional switched-capacitor dc-dc converter are reduced. The huge di/dt and dv/dt in the switching transition and EMI noise are restricted. The huge capacitor bank to reduce the voltage ripple and achieve high efficiency is eliminated.
- A ZCS multi-level modular switched-capacitor dc-dc converter as the high input current, high voltage gain interface circuit for TEG in automotive application is proposed. This new converter includes the advantages of both zero current switching and multi-level modular switched-capacitor dc-dc converter. Also this new converter does not employ extra devices to achieve ZCS which increase the circuit reliability.
- A family of ZCS switched-capacitor dc-dc converter for the automotive application is proposed and analyzed. By using the proposed ZCS switched-capacitor dc-dc converter, very high power density dc-dc converter operating at high temperature could be made.

- A family of multiphase ZCS switched-capacitor dc-dc converter with interleaving capability is proposed in order to reduce the input capacitor current stress by reducing the input current ripple using interleaving strategy. By interleaving the improved ZCS switched-capacitor dc-dc converter, a family of ZCS switched-capacitor with continuous input current is achieved. Much higher power density with higher input current rating switched-capacitor dc-dc converters could be made.
- The Optimal design method for MMSCC has been proposed and proved. The MMSCC can be designed in both over-damped case and under-damped case to achieve high efficiency. However, to design the MMSCC in over-damped case to achieve high efficiency, a huge capacitor bank has to be utilized, which will increase the converter size. Design the MMSCC in under-damped case, low capacitance MLCC capacitor can be used, ZCS for all the switches can be achieved. Small size and high efficiency features can be achieved at the same time.
- In order to reduce the capacitor voltage stress of MMSCC, a DW-MMSCC have been proposed by reducing the capacitor voltage stress by half without losing any features of MMSCC. ZCS can also be achieved for all the devices. By using DW-MMSCC, higher power density and efficiency switched-capacitor dc-dc converter can be built.
- The zero voltage switching of DW-MMSCC has been proposed by using phase-shift switching strategy. The voltage regulation of DW-MMSCC can also been achieved by using the proposed control method.
- A family of Z-source dc-dc converters have been proposed and analyzed. By utilizing two active switching devices, Z-source dc-dc converter can output positive voltage and negative

voltage at the same time. It can be used for low cost dc motor drive and zero voltage electronic load.

- A semi-Z-source dc-ac single phase inverter is proposed. By using proper modulation strategy in Z-source dc-dc converter, the semi-Z-source dc-ac inverter can be achieved. The input dc voltage and output ac voltage share the same ground, the high frequency ground current caused by parasitic capacitance of PV panel can be eliminated.
- A low cost boost-half-bridge micro-inverter has been proposed for transformer isolated approach PV panel in grid-connected application. High efficiency and low cost target have been achieved.

11.2 Recommendations for Future Works

- The optimal design considerations of DW-MMCCC can be investigated.
- The switched-capacitor dc-dc converter using stray inductance for output voltage regulation can be investigated.
- The model and control of semi-Z-source inverter can be derived for grid connected applications.
- The integrated version of switched-capacitor dc-dc converter working at higher switching frequency around (200 kHz~500 kHz) with ZCS by utilizing the stray inductance could also be investigated.

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