GROUND FAULT DETECTION FOR FLEXIBLE HIGH VOLTAGE POWER SYSTEMS

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ABSTRACT

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Hybrid Electric Vehicles (HEV) in the consumer and commercial vehicle sectors have seen tremendous technological advancement in the last decade. The commercial vehicle industry in particular has benefited significantly from the hybridization of the propulsion system, and unlike the automotive segment, serves a wide variety of functions. This diversity in vehicle applications drives the necessity for high voltage power systems to be flexible in nature, allowing them to adapt to different vehicle architectures while performing the intended function. As a result, diagnostic modules within the high voltage power system, such as ground fault detection circuits, are being required to operate robustly in a high voltage power system that is exposed to electrical noise and significant variation in common mode impedance characteristics.

This paper explores four different ground fault detection methodologies that exist today in the industry, and evaluates their performance in a flexible high voltage power system. A thorough comparison of these technologies is performed based on results from seven distinct test cases, followed by a recommendation for the ideal ground fault detection system.

To my parents, Haragopal and Vijaya Lakshmi Mathsyaraja

Whom I love and respect unconditionally

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CHAPTER 1

1 Introduction

Hybrid Electric Vehicles (HEV) in the consumer and commercial vehicle sectors have seen tremendous technological advancement in the last decade. In the wake of depleting fuel reserves, increasing fuel costs, and stringent emissions restrictions by governments worldwide, many vehicle manufacturers and OEM suppliers are working to reduce cost and increase reliability of all the components that form a hybrid vehicle, which uses two or more energy sources for propulsion (typically gasoline/ diesel, and battery supplied electrical energy).

Depending on the manufacturer and the application type, a HEV can be constructed and configured in a variety of ways. In a typical vehicle, a High Voltage battery pack usually in the range of a 100 to 1000 Volts DC, is used to power an inverter that converts DC power to three phase AC power to drive a traction motor. The High Voltage battery pack is also commonly used to power other electrical auxiliary devices, such as a DC-DC converter for stepping down voltage to the vehicle's low voltage (12-14V) power net, or an auxiliary inverter unit for converting High Voltage DC to 120VAC. The power is often transmitted over High Voltage lines that could be accessible to the user, and are generally shielded to shunt electrical noise to the chassis of the vehicle.

The integrity of this high voltage system is critical to the reliability and safety of the vehicle. Typically, the vehicle chassis will be electrically isolated from the terminals

or conductors of the high voltage system. Under normal conditions, leakage currents in the order of micro amps exist between the conductors of the high voltage bus and the frame of the vehicle. However, as these complex systems are housed in locations that may observe exposure to harsh environments with rapidly changing temperature conditions, as well as severe vibration, there exists a potential for gradual or relatively instantaneous isolation breakdown; depending on the failure mode. This condition is hazardous to users and personnel of the vehicle, and sometimes the vehicle itself.

This phenomenon of isolation breakdown is intrinsic to the nature of machines and electronics, and has been acknowledged by the industry for many decades. Several methodologies have been invented to identify ground faults within power systems and react to prevent potential failures or hazards, such as Ground Fault Circuit Interrupters (GFCIs). Especially in the last 5 years, many ground fault detection systems have been created specifically for hybrid electric vehicle power systems, as this technology continues to advance and penetrate the market. Yet, in spite of all the development that has occurred in this field, few systems exist that are generic in nature but sufficiently robust to be able to accurately identify low impedance to ground conditions on flexible power systems, where the components that make up the system are interchangeable and hence may vary significantly in design. This is particularly true for the commercial hybrid vehicle market, which has many differences in comparison to the passenger vehicle market.

Whereas passenger hybrid vehicles are designed for the single purpose of transportation of people, with mostly similar duty cycles and environments, commercial

hybrid vehicles vary tremendously in the utility of the vehicle, and in the environments within which they operate. In addition, mass production quantities of passenger hybrid vehicles are far higher in comparison to those of commercial hybrid vehicles. With applications ranging from city delivery, utility, telecommunications, and mining, to refuse, goods transportation, mass public transit systems, and many more – the hybrid power systems that have to be integrated into these vehicles will significantly differ in topology and design. It has therefore become critical to design hybrid power systems that maintain a standard framework but at the same time offer the ability to be modified as per the requirements of the application; thence the introduction of flexible hybrid power systems, and the need for a ground fault detection system that will function effectively irrespective of the devices that are connected to the High Voltage Bus.

The first part of this thesis will focus on the details of hybrid vehicular ground faults, discussing their root causes and effects. The second part, which contributes to the primary intent of this thesis, will dive into an analysis of the various technologies that exist today for achieving ground fault detection, and demonstrate that a ground fault detection method for flexible hybrid power systems can be developed based on these existing technologies. Close attention will be paid to the various attributes and characteristics of these concepts, and eventually their strengths and weaknesses. As a result of this analysis, a few recommendations for future work will be presented that will lay the groundwork for the development of a potentially powerful and versatile diagnostic system.

CHAPTER 2

2 Failure Modes & Root Causes

Isolation breakdown between High Voltage conductors and the chassis of the vehicle can occur in several locations within the system, and may have been caused by one or more of a wide range of fault conditions. In a Hybrid Electric Vehicle, a ground fault can occur primarily between the High Voltage DC (HVDC) bus and chassis, or the High Voltage AC (HVAC) bus and chassis. The following sections will describe the different modes of failure, as well as potential root causes of the fault.

2.1 Resistive Leak Fault on HVDC Bus

Figure 1 illustrates a typical construction of the HV power system on a HEV. As can be seen, there are several locations on the HVDC power path that can leak to chassis.

2.1.1 Wire Chafing

Technological advancement of vehicles for increased safety, fuel efficiency, on board diagnostics & prognostics, and artificial intelligence has resulted in significant electrification of the vehicle system. This electrification has been predominantly low voltage in nature, but with the advent of hybrid electric vehicles, high voltage power systems including the power lines and connectors have been introduced to the environment. Although these HV lines are usually very well insulated and routed, proximity to the vehicle chassis and potential abrasive surfaces is inevitable due to the space and weight constraints on vehicles. Mechanical vibration of these cables causes

gradual wear and tear due to friction with surfaces in close proximity, eventually leading to insulation failure and a subsequent ground fault. Many industry reports, such as the one created by the NASA Research Center for Wiring Fault Detection, endorse that wire chafing is the root cause of ~30% of all wiring faults that occur in aircraft [1].

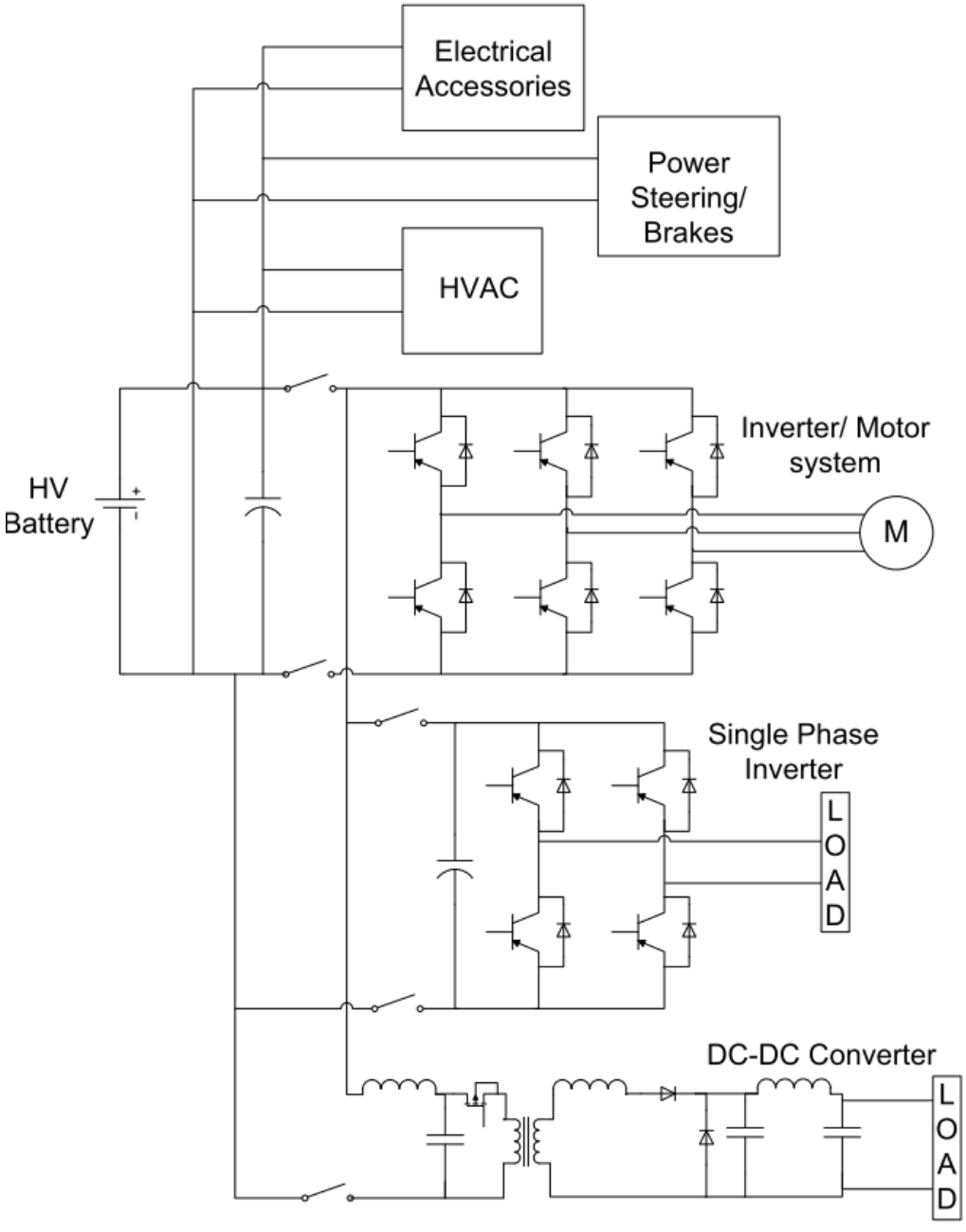

Figure 1: Typical HV Power System on a Hybrid Electric Vehicle

2.1.2 Aging of Components

Due to the nature of plastic composite material used as insulation for vehicle wiring, embrittlement and eventual cracking of wire insulation is a common phenomenon. Cracked insulation reduces electrical isolation between a high voltage conductor and the vehicle chassis, and hence can increase leakage current. Studies have shown that electrical stress conditions, chemical structures, and operating environments (both mechanical and thermal) lead to the aging and subsequent dielectric breakdown of polymeric insulation [2].

2.1.3 Contaminant Intrusion

Sealing of electronic components in medium and heavy duty commercial hybrid vehicles is a critical component towards system reliability, and is most often a challenge because of the harsh environments that these vehicles are exposed to. The following conditions could lead to the intrusion of contaminants into the HV system, eventually leading to current leak paths to the chassis:

- Constant heating and cooling of components resulting in condensation, and subsequent moisture intrusion
- Heavy rains or snow accumulation resulting in water entering improperly sealed components, or those with porous metal enclosures
- Broken, defective, or improperly sealed high voltage power connectors resulting in water intrusion

- Infiltration of salt, dirt, and other debris into high voltage components or battery system

- Leakage of electrolyte from high voltage battery cells to the case of the battery which is grounded to the vehicle's chassis [3] [4]

2.1.4 Manufacturing Defect

As power electronics systems become more complex in design due to the integration of several power conversion modules into one chassis, manufacturability becomes a challenge. This coupled with the fact that market demand for these components is still relatively very low, most of the production is done manually. This increases opportunity for build error, and eventual defects in parts which, depending on the nature of the defect, might not surface until the component has been installed in the vehicle and operated for several duty cycles. Some good examples of defects that could cause ground faults are:

- Wrong or defective components being installed in power system components. E.g. a shorted Y-capacitor installed in an inverter

- Foreign conductive material intrusion into the component during manufacturing. E.g. extra screws, wires, components etc.

2.1.5 Maintenance worker incident

A majority of the tools (screw drivers, wrenches etc.) used during maintenance and service are conductive in nature, and tight spaces in power systems enclosures could cause the service personnel to short a high voltage cable or bus bar to the chassis of the

vehicle. If a pre-existing ground fault is present in the system (from either positive or negative conductor to chassis), and the service personnel creates a fault between the other conductor and chassis, an arc condition could exist and potentially harm the individual, in addition to damaging the tool.

2.2 Alien Component Introduced to System

High Voltage battery power on hybrid electric vehicles although traditionally was used to drive a traction motor for propulsion, increased vehicle electrification has resulted in the batteries being a source of power for several other components such as power steering systems, air conditioning systems, 120V auxiliary power generators, HV battery chargers etc. Currently, few industry standards exist that regulate the design of these devices; which means that such commodity high voltage components could potentially be used in a flexible power system, and cause a ground fault.

2.2.1 Excessive filtering to ground

Electromagnetic Interference (EMI) has become a great concern in power electronics applications, especially in Hybrid Electric Vehicles, and the problem seems to be increasing as the industry is moving rapidly towards higher power density components for smaller package sizes. Although certain design procedures can be used to reduce component sizes (such as higher switching frequencies), these same procedures worsen the EMI phenomenon. In order to reduce EMI within a system, engineers use various filtering techniques in a power device. The size of these filters is related to the desired degree of attenuation of harmonics of the current noise [5].

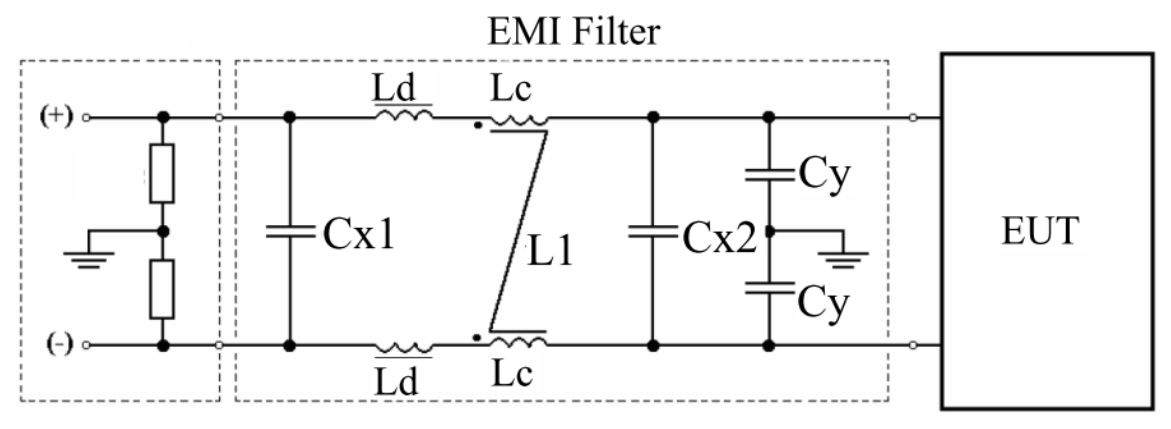

Figure 2: Differential Mode and Common Mode filters [5]

Figure 2 illustrates a typical EMI filter in a power converter system, where C_Y and L_C are inductive and capacitive elements used to suppress Common Mode (CM) noise, and L_D and C_X are used to suppress Differential Mode (DM) noise. CM noise occurs on all power supply lines with respect to the reference ground plane and it is essentially caused by insulation leakage, electromagnetic coupling and secondary effects due to parasitic components. DM noise is always present between the two power supply lines and it is mainly caused by pulsating currents and device turn-on and turn-off transients [5].

Although CM noise filter elements reduce system EMI, they contribute significantly to AC leakage current within the system. In a modular HEV where there exist more than five power converter devices, each with its own EMI filter, the compounding effect of the filter components could lead to leakage currents that have hazardous effects.

2.2.2 Auxiliary Loads with Pre-existing Faults

Many power electronics devices, especially in hybrid vehicle applications, are designed to have isolation between the High Voltage DC input stage and the output AC or DC stage. This is most commonly achieved through galvanic isolation methods, such as transformers. However, galvanic isolation is not a mandate in the industry, and there are power electronics manufacturers that do not design isolation into inverter devices in order to save on size and cost. A typical example of this is a non-isolated Auxiliary Power Generator (APG) device that converts 300-400 VDC to 120VAC at 60Hz for accessory usage in Utility truck HEVs or heavy duty line hauler truck HEVs[6]. The lack of isolation causes the high voltage bus to be physically connected to any device that the user plugs into the system, such as hand tool battery chargers, halogen lamps, fans, air compressors, microwave ovens, air conditioners etc. The system therefore is vulnerable to leakage current to chassis ground through these devices if a fault exists within them.

2.3 Leak Fault on the HVAC Bus

Depending on the topology of the power converter, isolation breakdown between the output High Voltage AC lines to chassis could lead to excess flow of leakage current to ground. The root causes of an AC side resistive fault are similar to those outlined in Section 2.1. Furthermore, excessive filtering on the common mode AC bus could also add to ground leak current. However, since there are power semiconductor devices (IGBTs, MOSFETs etc.) in the current path between the AC load and the HVDC energy source, the profile or footprint of this leakage current will be distinctly unique when

compared to DC side leakage current. Characterization of such a fault therefore has to be done differently.

2.3.1 Motor winding insulation fault

Ground faults are more prevalent in motors than other power systems devices, because of the violent manner and frequency with which they are started. The number one contributor to motor winding insulation failure is thermal stress, which can be a result of heat loss in the windings, high ambient temperature conditions, or friction of insulation caused by severe vibration profiles [7]. Such a ground fault could cause additional thermal stress due to the fault current, voltage stress to the inverter, higher electrical noise emissions, increased motor torque ripple etc.

Ground current also flows through the leakage capacitance and inductance intrinsic to the machine windings. When an induction or Permanent Magnet Synchronous Machine is driven by a PWM inverter, as shown in Figure 3, the triangular carrier frequency is often set beyond the audible frequency range (over 15 kHz) in order to suppress acoustic noise. In this case, the output voltage potential of the inverter steps up and down at a very high frequency according to the switching of the transistors or FET's and the charging current flows into the leakage capacitance formed between the windings and the iron core of the motor. This current flows through the capacitance to the ground and then returns to the inverter along a miscellaneous path. The leakage current consists of usually spike wise pulses which correspond to the switching instants of the transistors, and the RMS value of the current is roughly proportional to the square root of the number

of the pulses or to the switching frequency. Since the core of the machine is grounded to the chassis of the vehicle, this leakage current could be a shock hazard for personnel [8].

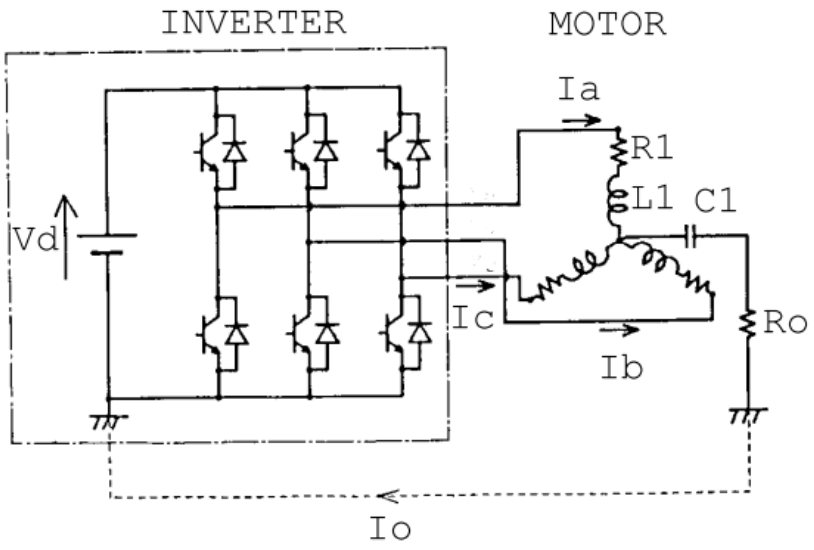

Figure 3: Equivalent circuit of traction inverter and induction motor in HEV [8]

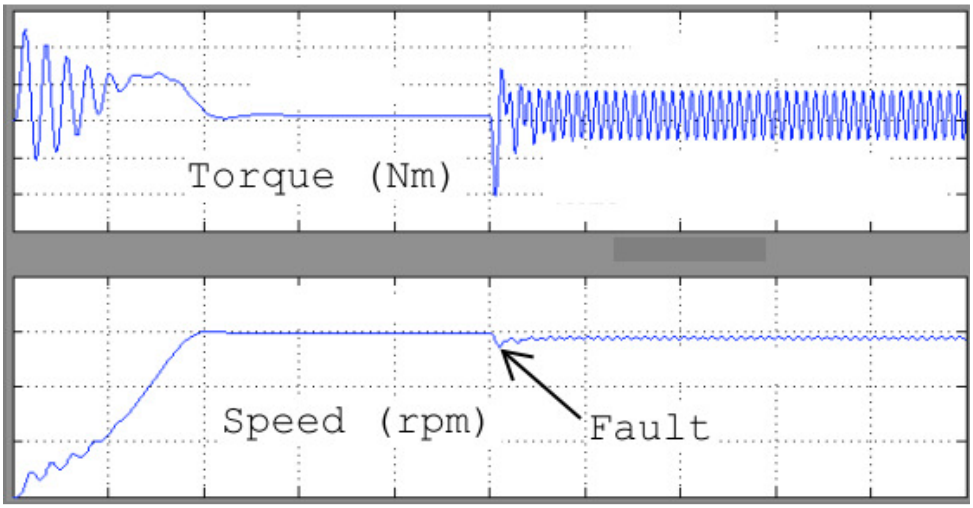

Figure 4: Speed and Torque during phase to ground fault [7]

CHAPTER 3

3 Effects of Ground Faults

In the previous chapter, various failure modes and root causes related to ground faults in HEVs were discussed. Any degree of reduction in the overall impedance of the High Voltage power system with respect to the original system design could result in various unwanted system behaviors or conditions.

3.1 Interference with other Circuits

Several circuits exist within subsystems of the HEV that are designed for device control, data acquisition, prognostics, diagnostics, and protection from conducted and radiated emissions. Some of these circuits use voltage and current measurements of the high voltage bus with respect to chassis in order to operate effectively. A ground fault between a high voltage conductor and vehicle chassis could result in the malfunction of these electronic circuits, often resulting in unwanted shut down of the hybrid system, increased vehicle downtime, and potential warranty costs to be incurred by the manufacturer.

3.2 Potential Shock Hazards (AC and DC current)

By far the most critical reason ground fault protection is an absolute necessity in power electronic systems is the potential risk a ground fault poses to the safety of people. Traditional electrical components on a vehicle operate on 12VDC, which is too low a voltage to cause harmful currents to flow through the human body. However, most hybrid

vehicles today run on voltages ranging from 300 V to 1000 V; shock currents at these voltages could be lethal.

For this reason, all hybrid vehicles with high voltage energy sources have floating grounds, which essentially means that the High Voltage bus is completely isolated from the low voltage bus.

A floating system ensures two layers of protection from a shock hazard, since both the positive and the negative conductors are isolated from the user. This ensures that a dual point failure has to occur to cause a shock, and thus is mandated as a design practice for all high voltage systems. In the case that a low impedance path exists between a high voltage rail (positive or negative) and chassis as shown in Figure 7 on Page 18, however, a single point failure is sufficient to cause a shock. It is therefore very critical to have a system that monitors and reacts to a leakage condition within the hybrid vehicle.

Many international organizations have released literature and standards on the effects of electrical shock on human physiology, and have mandated certain safety design practices to regulate the quality of products being released in the market.

Figure 5 below describes the various effects of increasing current (at 60Hz) on the human physiology. As can be seen, non-hazardous leakage current is considered to be any amount below the let-go current threshold. Hence, most ground fault circuit interrupting devices are designed to open the circuit below this threshold.

Shock current @ 60 Hz (1 – 3 sec)	Physiological Effect
0.2 mA – 7 mA	Threshold of Perception
8 mA – 90 mA	Let-go current
> 15 mA	Respiratory paralysis, fatigue, pain
> 70 mA – 5 A	Ventricular fibrillation
> 1 A	Sustained myocardial contraction, burns, injury

Figure 5: Physiological effects of electricity [9]

In Figure 5, threshold or estimated mean values are given for each effect in a 70 kg human for a 1 to 3 s exposure to 60 Hz current applied via copper wires grasped by the hands [9].

UL 2231-2 – "Personnel Protection Systems for Electric Vehicle Supply Circuits," is a standard authored by the Underwriter's laboratory and has a very robust test methodology for determining the effectiveness of ground isolation within a system, as well as that of circuit interrupting devices designed to protect personnel in the case of a ground fault [10].

In summary, this standard introduces a distinct means to measure leakage current through a human body model, and quantify the impact the shock current has on the human physiology. By placing the measuring instrument circuit (Figure 6) as a load across the terminals of a power system that the user could potentially get access to in a fault condition, one can measure the Measurement Indication Unit (MIU) which correlates to a normalized current parameter (across various frequencies). MIUs are

related to the physiological effects when electric current flows through the human body. At low frequencies, the number of MIUs that is obtained by dividing the output voltage, in mill volts, by 500 ohms, equals the current, in milliamperes, through the measuring instrument. At high frequency, the meter indication of MIUs is less than the number of milliamperes through the measuring instrument. For example, at 100 KHz, 0.5 MIU-RR occurs when the actual current through the measuring instrument is 70 mA. At any frequency, the acceptability of the leakage current can be determined by comparing the number of MIU's to the MIU limit, which is shown in Table 1.

This measurement methodology forms the basis for designing and testing ground fault detection circuits in HEVs.

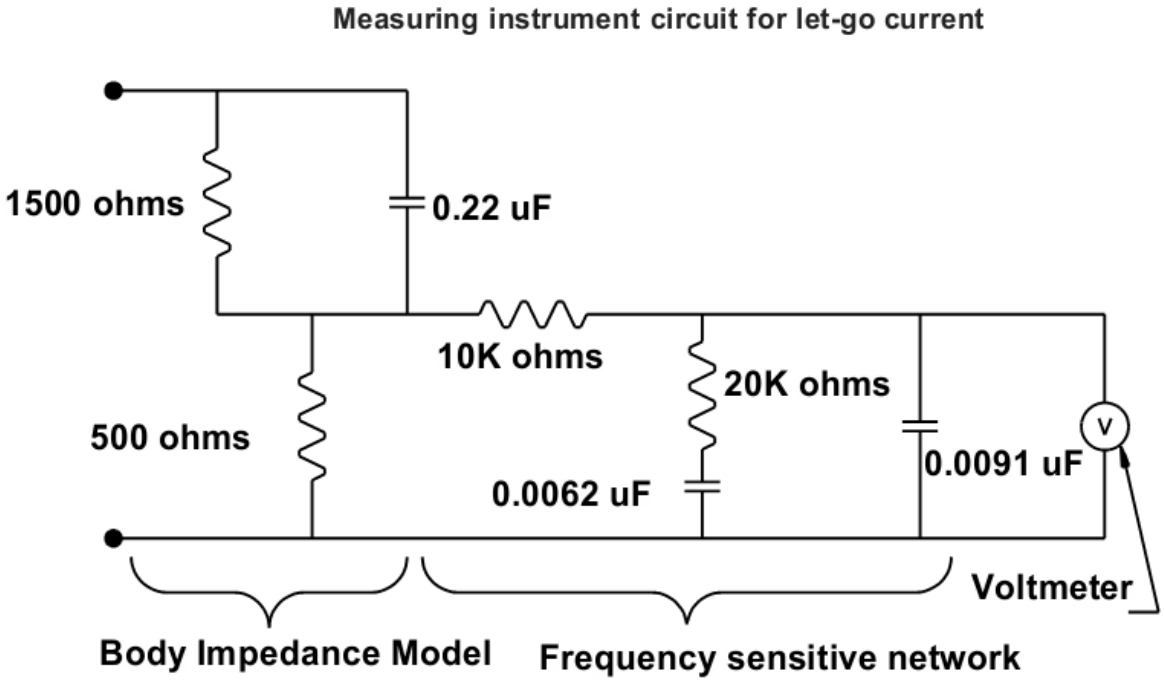

Figure 6: Equivalent Human Body Circuit Model [10]

Table 1: Required trip threshold for charger circuit interrupting devices [10]

Type of source for fault-current	**Ground fault threshold – I (rms mA) or (MIU)**
60 Hz	5 ± 1
DC	30
DC+AC	5 minimum
AC > 60 Hz	5 × FF but not greater than 70
Multiple frequencies	5 × FF but not greater than 70
FF – is the Frequency Factor from Figure 21.2 on Page 30 of [10]	

3.3 Damage of Auxiliary Filter Circuits

Although isolating the high voltage bus from the chassis of the vehicle adds several layers of safety from an electrical shock, it makes it difficult to shunt electrical noise (generated by power electronics circuits) to the vehicle chassis. This noise can be electromagnetically coupled into other subsystems in the vehicle, and cause interference with their operation. It is therefore common practice to design EMI filters into power electronics components to reduce the conducted and emitted noise footprint of the component. These filters are usually made up of small y-capacitors or common mode chokes (inductors). This addition of discrete components not only adds cost and complexity to the device, but also leaves them susceptible to damage in the case of a high voltage short circuit to the chassis.

Consider a common mode EMI filter as shown in Figure 7, where the filter impedance is balanced between High Voltage positive and chassis, and High Voltage

negative and chassis. In an ideal state, the voltage potential across C_1 and C_2 would be equal, i.e. half of the source DC voltage.

$$C_1 = C_2 = {}^1/_2\, VDC$$

Y-capacitors are generally rated for the full DC voltage, with some additional voltage for margin. This ensures longevity of capacitor life and protects against damage during fault conditions. For example, in the case of a DC side ground fault as illustrated in Figure 7 below, the Y-capacitor C_2 would not see more than 400V, assuming that the DC voltage source is rated for a maximum of 350V. However, in the case that the traction motor of the HEV has a back EMF characteristic of above 600V at high speeds, there could be potential overvoltage (and eventual damage) of the capacitors.

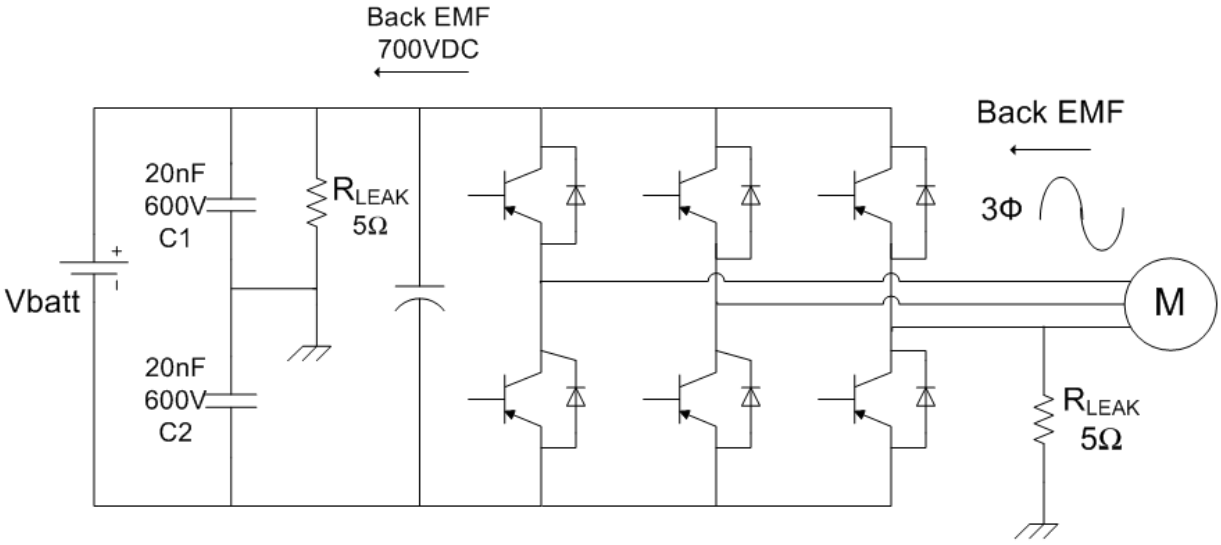

Figure 7: Effect of back EMF on EMI filter

In the case of an AC side ground fault, high frequency current ripple of significant magnitude could result in excessive heating of the Y-capacitors, eventually causing accelerated aging and damage [11].

CHAPTER 4

4 Survey and Analysis of Existing Technologies

Although ground fault detection units and circuit interrupters for power systems in residential and industrial applications have been available for many decades now, distinct differences in vehicle applications have created the need to develop unique diagnostic circuits for HEVs. There have been many inventions of such diagnostic systems for vehicles in the past 5 years. This chapter will discuss in detail the operation of these systems, and how they may be implemented in a flexible high voltage system.

4.1 Definition of Flexible HEV Architecture

As mentioned earlier in the introduction, the commercial hybrid electric vehicle space varies significantly from that of the automotive HEV industry. Due to the plethora of applications, and relatively low production quantities for these applications, many companies are opting to design flexible HEV systems that provide the Original Equipment Manufacturer (OEM) with a base propulsion system (a HV energy source, inverter, and motor) that has provisions for connectivity to other auxiliary devices that serve key functions in the vehicle. This allows OEMs to install components that are pertinent to the utility of the HEV, and also offers them the flexibility to source components from a multitude of suppliers that may manufacture components that achieve the same function but are designed differently. The ultimate goal is to develop a system that is modular in terms of the devices that can plug into it and scalable in terms of power

throughput, while being adaptable to any base vehicle; all at a reasonable cost [9]. In order to do this, the architecture of the base propulsion system should have a robust electrical and mechanical interface, with in-built software to control and monitor auxiliary devices. This software embedded in the system controller should also be capable of detecting ground faults accurately (both DC and AC side), irrespective of the components that are plugged into the system.

Figure 8 illustrates this type of architecture:

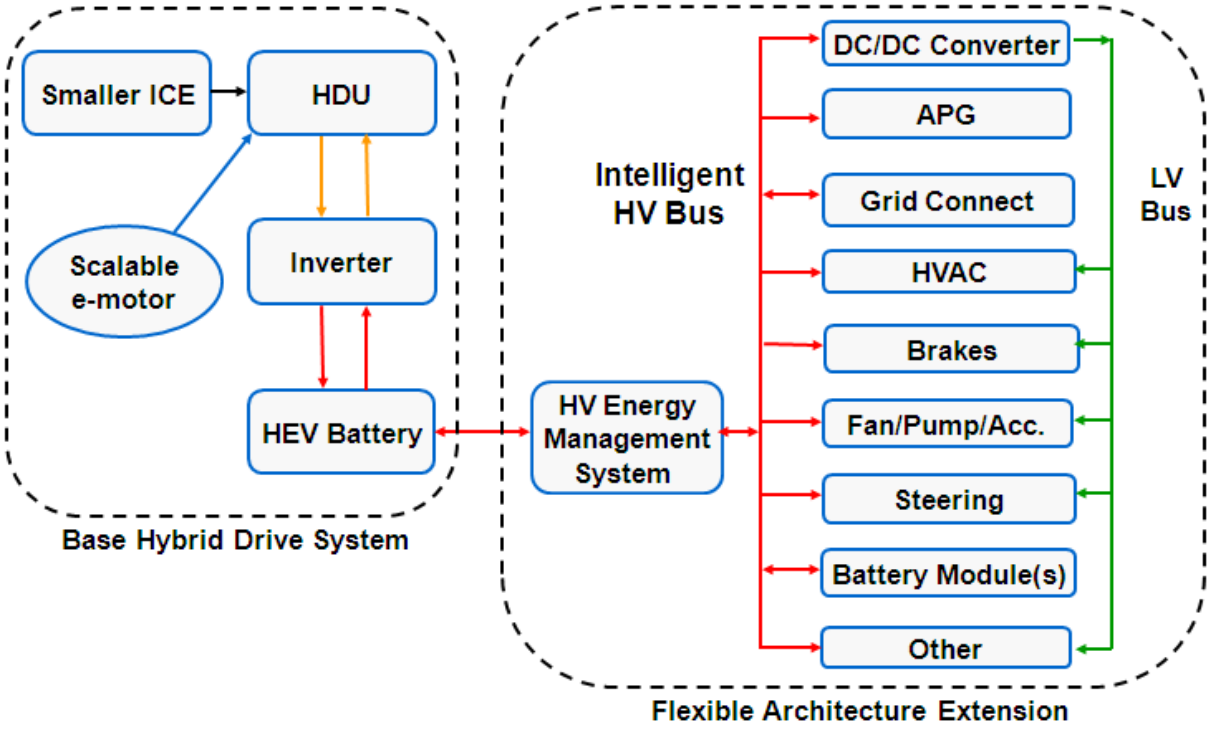

Figure 8: Flexible Hybrid Electric Vehicle architecture [12]

As vehicle electrification is growing at a rapid pace, there are many more components that can be designed for and connected to a high voltage power net within a HEV. This change in design philosophy also lends towards progress in the Electric Vehicle (EV) industry, where an ICE (Internal Combustion Engine) and 12V battery

source are not needed, since all components are powered by a High Voltage battery source. Some examples of devices that can be connected to the baseline drive system are DC-DC converters, Auxiliary Power Generators (APG) for 120V power, Power Grid Connect interfaces, Heating Ventilation and Air Conditioning (HVAC) systems, brakes, power steering systems, and many other electrical accessories.

The HV Energy Management System would house the ground fault detection technology, which would ideally monitor for faults in the entire system. The next section discusses the various technologies that exist in the industry today, and evaluates whether they would be a robust solution for a flexible architecture as described above.

4.2 Nissan Motor – Ground Fault Detector for Vehicle

4.2.1 Technology Overview

Inventors Tsuyoshi Morita and Shinsuke Nakazawa from Nissan Motor Co. developed an adaptation of the popular signal injection method for detecting ground faults in an electric vehicle (or HEV). This ground fault detector system interfaces with the High Voltage Bus of the vehicle, as well as the low voltage system, via a controller [13].

The system described in the invention is designed to perform three operations:

1. Detect the presence of a ground fault within the system
2. Identify the location of the ground fault within the system
3. Identify the cause of the ground fault

The method allows for perpetual monitoring of the HV bus for ground faults, even during the operation of the vehicle. The following diagram may be used to illustrate the invention:

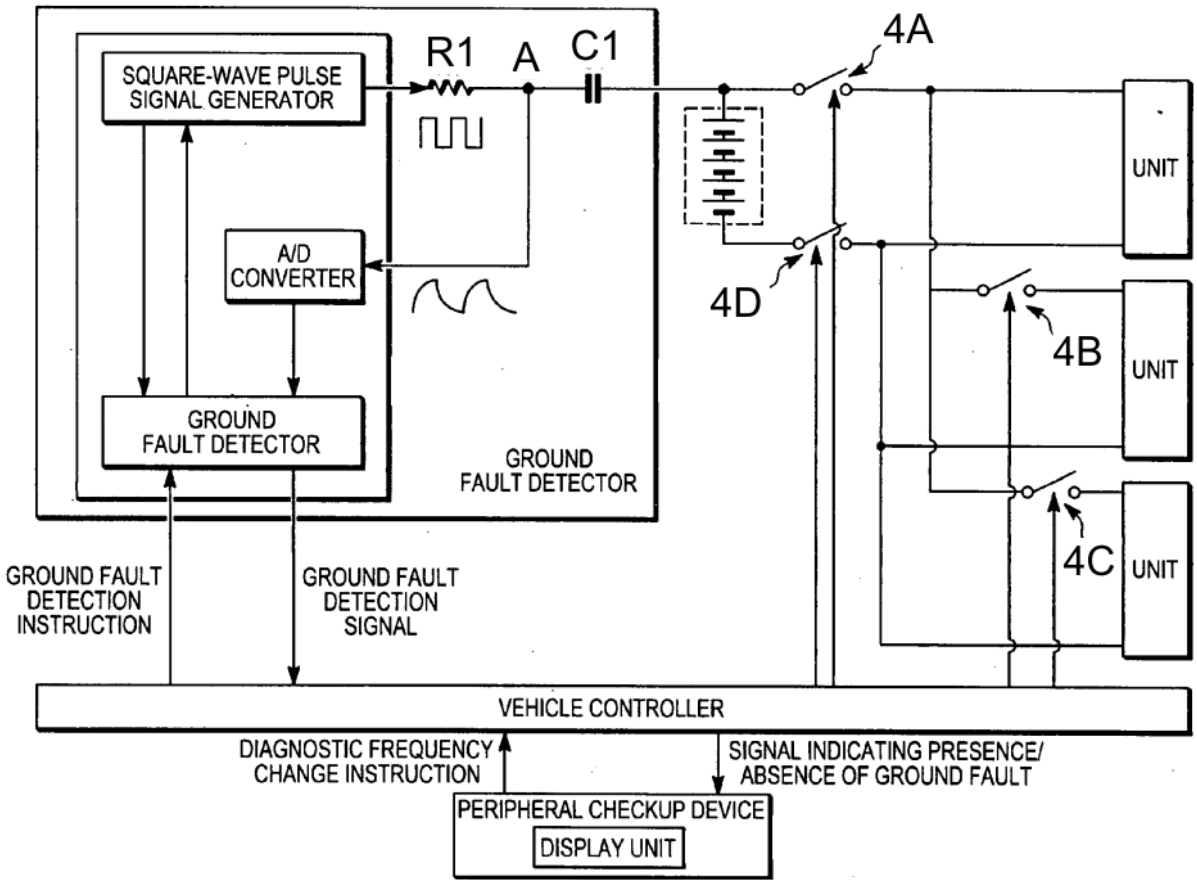

Figure 9: Schematic overview of method 1 [13]

As can be seen from Figure 9, a square wave signal generator is used to output a square pulse of amplitude V_S (e.g. 5V) and frequency f_1 (e.g. 10Hz). The output of the generator is capacitively coupled to the high voltage positive (+) rail through capacitor C_1. Per the patent, the signal frequency of the square pulse should be significantly less than the switching frequency (usually 20 kHz to 3MHz) of power electronics components on the HV bus in order to prevent the high frequency noise from interfering with the leak detection circuit's ability to operate effectively.

The ground fault detector then measures the voltage (V_{DET}) at point A in the circuit, to determine the attenuation in the signal based on common mode impedance in the HV bus. This equivalent common mode impedance (Z_{EQ_P}) between the high voltage positive rail and chassis, and (Z_{EQ_N}) between the high voltage negative rail and chassis is a combination of all the resistive, capacitive, and inductive elements in the common mode bus. For simplicity, only resistive and capacitive elements will be considered in this analysis.

As described in the previous section, consider an HEV system with a HV battery source (V_{BATT}) and several fixed and variable power electronics components connected to this source (Units 1, 2, 3, 4 etc). Each component has inherent impedance between the high voltage rails and chassis ($Z_{1\_P}, Z_{1\_N}, Z_{2\_P}, Z_{2\_N}$ etc) where:

$$Z_{1\_P} = \frac{1}{\left(\frac{1}{R_{1\_P}}\right) + j\left(2\,\pi f\, C_{1\_P}\right)}$$

And

$$Z_{1\_N} = \frac{1}{\left(\frac{1}{R_{1\_N}}\right) + j\left(2\,\pi f\, C_{1\_N}\right)}$$

Therefore,

$$Z_{EQ\_P} = \frac{1}{\left(\frac{1}{Z_{1\_P}}\right) + \left(\frac{1}{Z_{2\_P}}\right) + \left(\frac{1}{Z_{3\_P}}\right) + \left(\frac{1}{Z_{4\_P}}\right)}$$

And

$$Z_{EQ\_N} = \frac{1}{\left(\frac{1}{Z_{1\_N}}\right) + \left(\frac{1}{Z_{2\_N}}\right) + \left(\frac{1}{Z_{3\_N}}\right) + \left(\frac{1}{Z_{4\_N}}\right)}$$

There also potentially exists a resistive fault element R_{L_P} or R_{L_N} between the high voltage rails and chassis (ground), and R_{L_AC} between the non-isolated switched AC line of an inverter device (e.g. single phase auxiliary inverter) and the chassis.

Ideally, Z_{EQ_P} and Z_{EQ_N} are relatively large for DC and low frequency AC. Hence, the attenuation in signal V_S (measured as V_{DET}) could be relatively small in a faultless system. The amplitude of V_{DET} is as follows:

$$V_{DET} = V_S \cdot \frac{Z_{EQ\_P} - jXC_1}{Z_{EQ\_P} - jXC_1 + R_1}$$

The reactance of C_1 is an order of magnitude smaller than R_1 at 10 Hz. Hence, in the case that a resistive fault R_{L_P} or R_{L_N} (e.g. 5 Ω) exists, Z_{EQ_P} or Z_{EQ_N} becomes significantly small as well, resulting in large attenuation of the 5V signal V_S. Based on this principle, an appropriate threshold impedance Z_{TH} may be chosen as a lower limit for the common mode impedance Z_{EQ_P} or Z_{EQ_N}, and the corresponding threshold voltage V_{TH} can be derived to be used as a metric for diagnosing ground faults.

This summarizes the ground fault detection methodology of the invention. The authors also discuss a simple means for detecting the location of the fault, by first detecting its presence in the system, and then isolating the fault to individual components by controlling switch circuits 4A, 4B, 4C, and 4D independently at different times.

Finally, the invention also discloses a method to determine the nature of the fault within the system by varying the oscillating frequency of signal V_S. The controller generating the square pulse first changes the frequency to f_2, which is lower (e.g. 5Hz) than the original frequency f_1. In the case of a resistive fault, the impedance $Z_{EQ\_P} - jXC_1$ or $Z_{EQ\_N} - jXC_1$ changes by the same factor as the frequency, i.e.:

$$Z_{EQ(f2)} - jXC_{1(f2)} = (Z_{EQ(f1)} - jXC_{1(f1)}) \cdot \frac{f_2}{f_1}$$

However, in the case of a capacitive fault or a fault of dielectric nature, the impedance $Z_{EQ} - jXC_1$ at frequency f_2 will be higher than that of a resistive fault at frequency f_2, since the reactance of capacitive elements is nonlinear with respect to time, as shown in Figure 10 below:

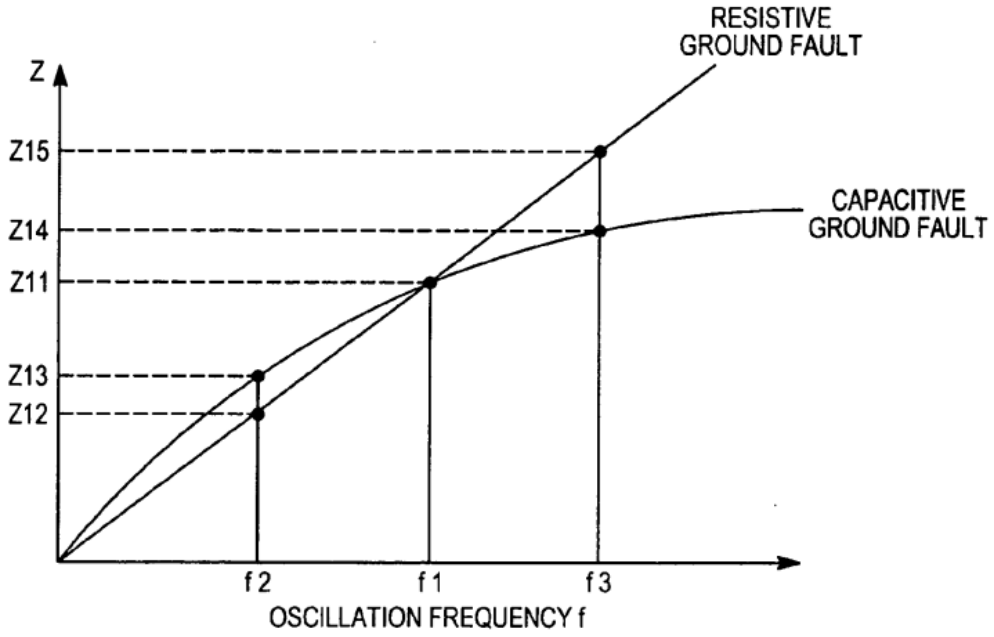

Figure 10: Change in impedance for capacitive vs. resistive ground faults [13]

At the decreased frequency, the threshold amplitude V_{TH} (or fault judgment value) for fault detection is set such that it is higher than the signal amplitude for a resistive fault, but lower than that for a capacitive fault (see Figure 11 for illustration). Hence, based on the attenuation factor of the detection voltage V_{DET} after the frequency is decreased, the diagnosis could determine whether the existing ground fault is resistive or capacitive in nature.

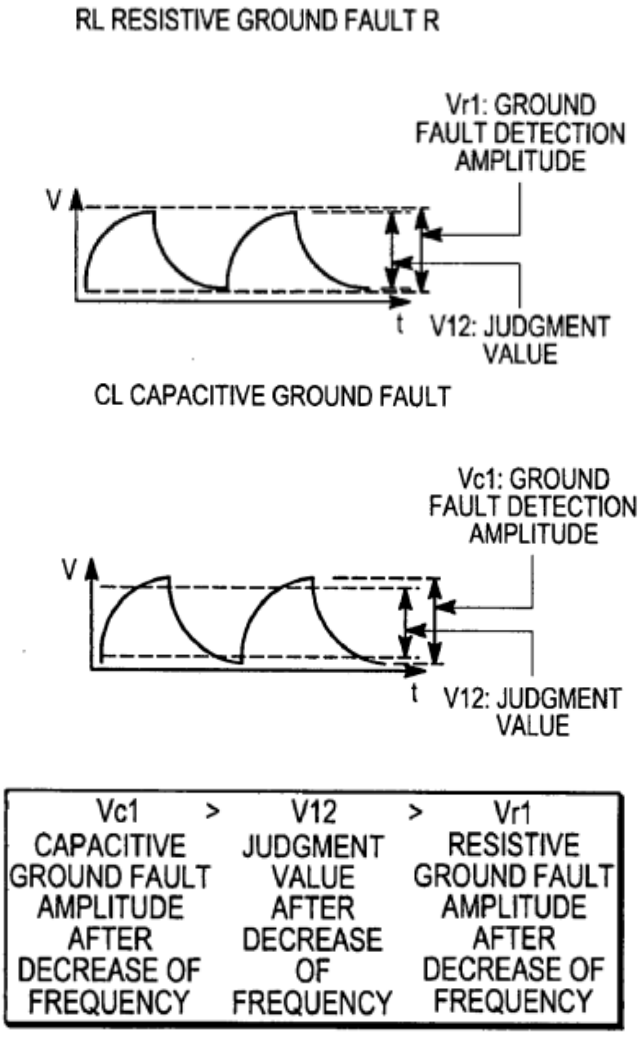

Figure 11: Response of circuit after decrease in frequency [13]

Similarly, the original frequency can be increased to f_3 (e.g. 20 Hz) to identify the nature of the fault. At the increased frequency, the threshold amplitude V_{TH} for fault

detection is set such that it is lower than the signal amplitude for a resistive fault, but higher than that for a capacitive fault (see Figure 12 for illustration).

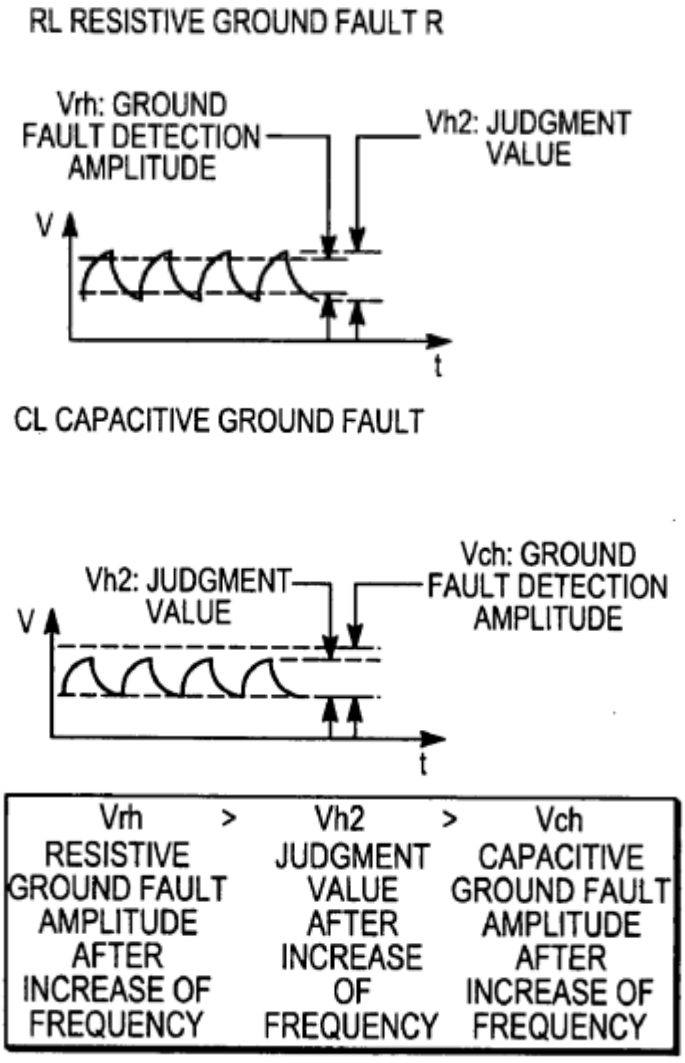

Figure 12: Response of circuit after increase in frequency [13]

4.2.2 Simulation and Analysis

The method proposed by the inventors is a technique that has been in use in other industries, such as Uninterruptible Power Supplies, for many years prior to the invention [3]. In order to analyze the viability and effectiveness of the method, this paper will test

the proposed ground fault detection circuit in seven different test scenarios that may exist within a HEV system.

Figure 13 on Page 31 is a circuit model designed using the Allegro Design Entry CIS application to replicate the above ground fault detection system, along with common mode impedances of power electronics components in the system.

As can be seen from the circuit, values for R_1 (54 kΩ) and C_1 (2.65uF) have been chosen arbitrarily based on the following criteria:

$$f_1 = 10Hz$$

$$V_S = 5V$$

$$V_{TH} = 3.45V$$

$$V_{BATT} = 600V$$

$$I_{TH}(\text{threshold leakage current to trip ground fault}) = 5mA$$

$$Z_{TH}(\text{threshold impedance to trip ground fault}) = \frac{V_{BATT}}{I_{TH}} = 120k\Omega$$

$$R_1 = 54k\Omega$$

We know that attenuation of V_S will be 31% at the threshold impedance, i.e.:

$$\frac{\sqrt{Xc_1^2 + Z_{TH}^2}}{\sqrt{Xc_1^2 + Z_{TH}^2} + R_1} = \frac{3.45V}{5V}$$

$$Xc_1 = \frac{1}{2\,\pi\, f_1 C_1}$$

Using the above equations and known values, we solve for X_{C1}= 6005Ω

Therefore, $C_1 = 2.65uF$

R_2 and C_2 in the circuit are an added filter that would typically serve to eliminate high frequency noise that is superimposed onto V_{DET} because of semiconductor switching (this filter is not specified in the invention disclosure).

The cutoff frequency (f_C) of the added filter is ~16Hz, so that the 10Hz component of V_S is not attenuated significantly.

$$f_C = \frac{1}{R_2 \cdot 2\pi \cdot C_2} = \frac{1}{100 \cdot 10^3 \cdot 2\pi \cdot 0.1 \cdot 10^{-3}} = 15.9\ Hz$$

We can calculate the new threshold voltage for ground fault detection using the known time constant R_2C_2 of the filter:

$$V_{TH\_NEW} = V_{TH} \cdot \frac{X_{C2}}{\sqrt{X_{C2}^2 + R_2^2}}$$

$$X_{C2} = \left(\frac{1}{2\,\pi 10 \cdot 0.1uF}\right) = 159.2k\Omega$$

$$V_{TH\_NEW} = 3.45 \times \frac{159.2 \times 10^3}{\sqrt{(159.2 \times 10^3)^2 + (100 \times 10^3)^2}} = 2.92V$$

Hence, if V_{DIODE} is being used as the measurement signal, the threshold for ground fault detection would be 2.92V.

A diode D_1 with a breakdown voltage of 5V has also been added to the leak detection circuit to prevent high voltage transients from damaging the controller input.

A High Voltage battery source, traction inverter, auxiliary single phase inverter, DCDC converter, and one auxiliary load have been modeled in the simulation circuit. Switches S1 through S10 are used to connect or disconnect the various power electronics components to or from the HV battery source.

TEST CASE 1

For the first test case, the ground fault detection circuit is connected only to the HV battery and the traction inverter. Also, there are no low impedance paths between the high voltage rails and chassis ground. This test case is to evaluate the ideal response of the ground fault detection system during a no-fault condition, and verify that a false fault would not be set.

Hence, all switches in the system are open, and the only impedance to ground in addition to the capacitor C_1 is the common mode impedance of the traction inverter:

$$Z_{1\_P} = \frac{R_{1\_P} \cdot C_{1\_P}^2}{R_{1\_P}^2 + C_{1\_P}^2} - j \cdot \left(\frac{R_{1\_P}^2 \cdot C_{1\_P}}{R_{1\_P}^2 + C_{1\_P}^2} \right)$$

Based on Figure 14, as expected, there is a small amount of attenuation in the signal, and $V_{DET(pp)} = 4.39V$. Since the threshold voltage is 3.45 V, no fault is triggered.

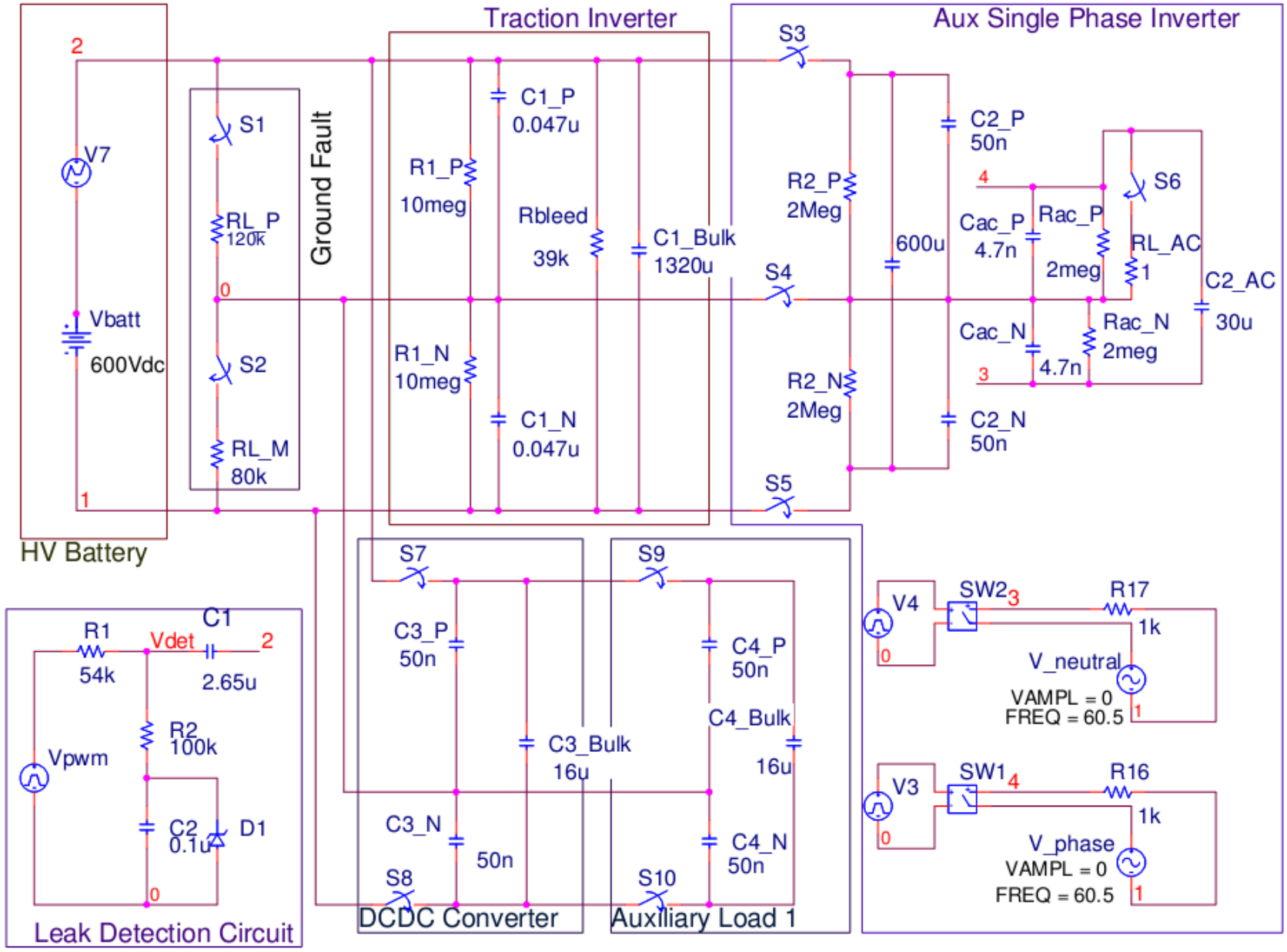

Figure 13: High voltage power system circuit model

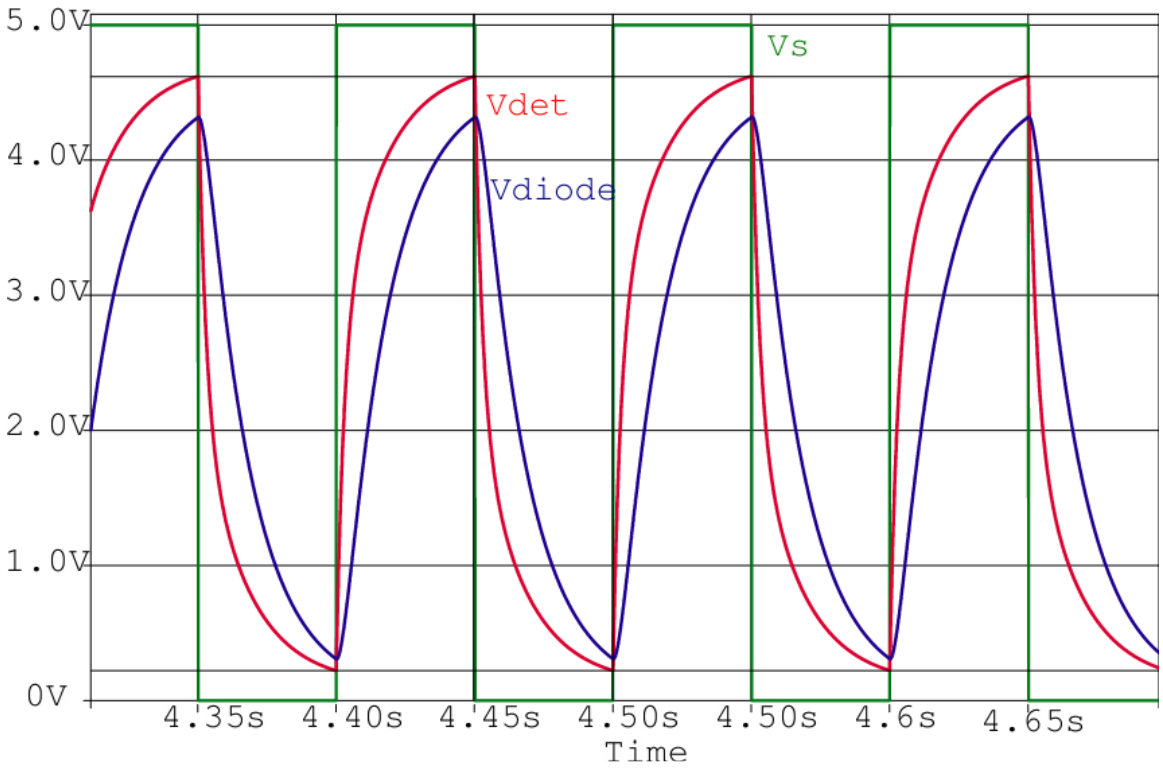

Figure 14: Simulation results for test case 1 of method 1

(For interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis)

TEST CASE 2

For the second test case, switches S3, S4, and S5 will be closed in order to connect the Auxiliary Single Phase Inverter. Since the inverter is not galvanically isolated, the input HVDC bus and output AC bus are physically connected through the switching IGBTs. Hence, high frequency common mode noise due to IGBT switching, as well as 120Hz ripple voltage (two times the fundamental output frequency of inverter) will be superimposed onto the signal V_{DET}. This test case is simulated to understand the susceptibility of the circuit to ripple voltage and switching noise. The results are shown in Figure 15.

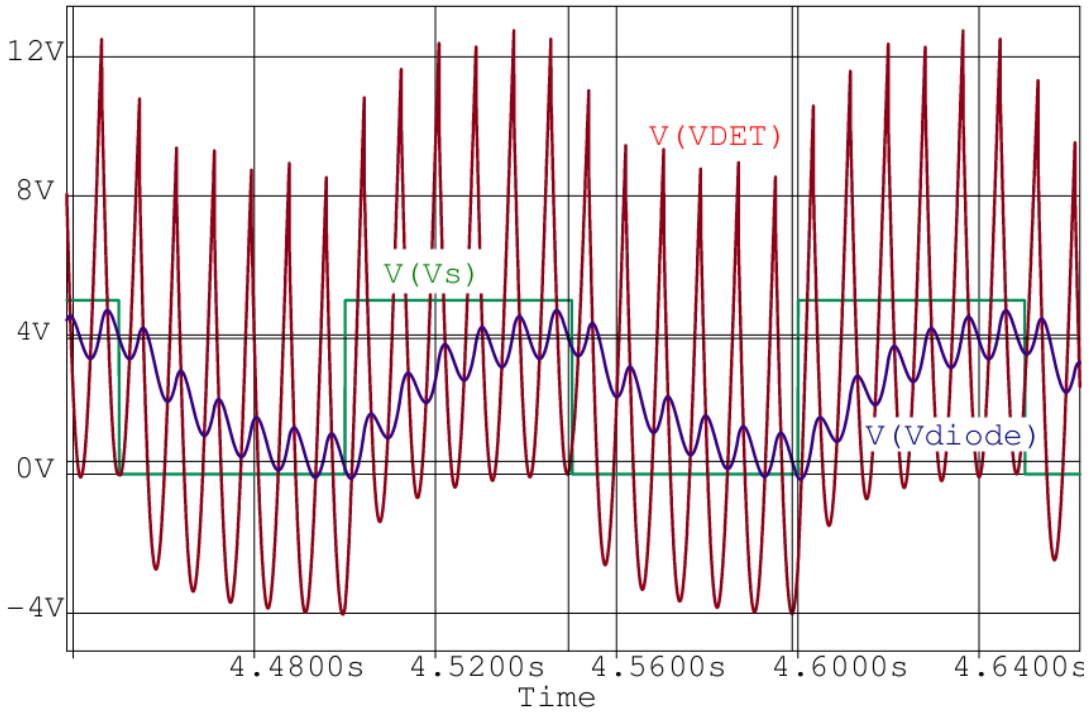

Figure 15: Simulation results for test case 2 of method 1

$$V_{DET(PP)} = 16.9V$$

$$V_{DIODE(PP)} = 4.92V$$

There are two components that contribute to the overall 120Hz waveform being superimposed onto V_{DET}:

1) The DCR (Direct Current Resistance) of the HV Battery system as well as inherent series impedance of the transmission path from the battery to the inverter causes a voltage ripple on the HVDC link when the single phase inverter load is drawing 120Hz current.

2) In a non-isolated inverter system, the ratio of DC side impedance between high voltage and ground to the overall impedance of the system (AC and DC side) will determine the amplitude of the AC voltage that will be superimposed onto the DC bus. Figure 17 describes this.

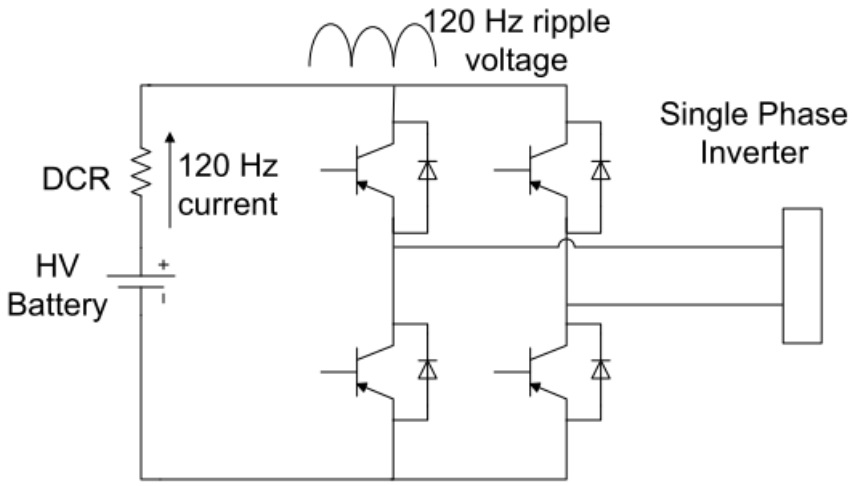

Figure 16: DC ripple current in a non-insulated single phase inverter system

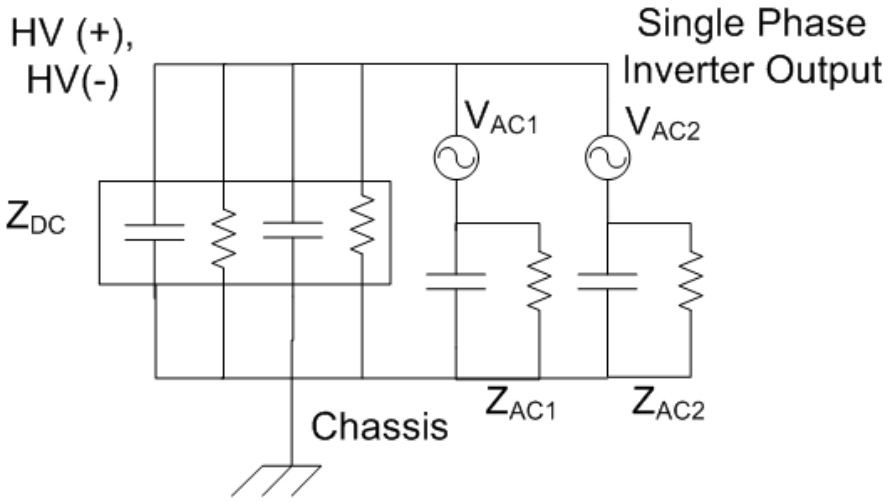

Figure 17: Equivalent circuit of AC and DC common mode bus

$$V_{RIPPLE} = V_{AC1} \cdot \left(\frac{Z_{DC}}{Z_{DC} + Z_{AC1}}\right) + V_{AC1} \cdot \left(\frac{Z_{DC}}{Z_{DC} + Z_{AC2}}\right)$$

V_{RIPPLE} is the ripple voltage on the high voltage bus

V_{AC1} and V_{AC2} are common mode output voltages of the inverter

Z_{DC} is the common mode impedance between HV + and chassis, and HV – and chassis

Z_{AC} is the common mode impedance between inverter output line 1 and chassis, and line 2 and chassis

The red line in Figure 15 represents V_{DET}, and has a peak-to-peak amplitude of 16.9V. For most microcontrollers, the analog or digital inputs are limited to 5V; hence, this would be too high a voltage to accurately measure. This is where the second filter (R_2, C_2) and the zener diode (D_1) come into play. V_{DIODE} is shown in blue in Figure 15, and is representative of the filtered version of V_{DET}.

The peak-to-peak value of V_{DIODE} is 4.92V, which would clearly not trip a leak fault (the threshold for V_{DIODE} being 2.92V). This is an important characteristic to note, since the 120Hz ripple on the signal adds to the complexity of signal processing of the measured signal, since there is poor fidelity in the raw waveform. Depending on the architecture of the system, this could be a significant issue. Although the most effective manner for processing V_{DET} would be to sample at a very high frequency (e.g. 1kHz) and then calculate a moving average of the data points to calculate the RMS voltage of the signal, the new RMS value might still misrepresent the true condition of the system. On the other hand, if the peak-to-peak voltage was to be used for ground fault analysis, the data would be highly unreliable due to the added noise on the signal (as illustrated in this test case).

TEST CASE 3

In this test case, the response of the ground fault detection circuit during an actual fault on the DC side is analyzed. Switch S1 between High Voltage Positive and chassis is

closed at time $t = 0\,sec$. All other switches in the system are open, and the leakage resistance R_{L_P} is set to 120kΩ. Hence, the only common impedance in the HV positive to chassis ground system would be that of the leakage resistance R_{L_P} in parallel with C_{1_P} and R_{1_P} (in the traction inverter). This test case is to validate that the circuit can successfully detect a fault in a true leakage condition. The result of the simulation is shown in Figure 18 below.

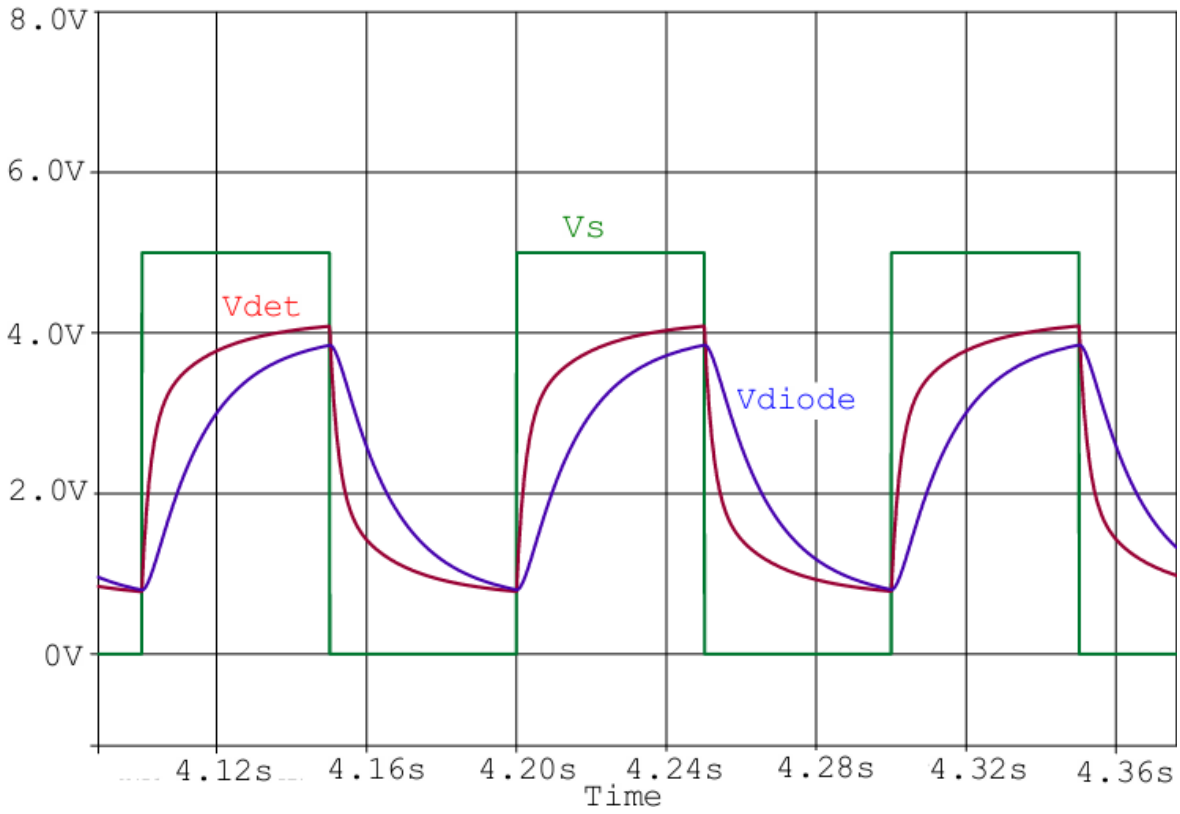

Figure 18: Simulation results for test case 3 of method 1

$$V_{DET(PP)} = 3.38V$$

$$V_{DIODE(PP)} = 3.05V$$

As expected, V_{DET} is less than the threshold voltage $V_{TH} = 3.45V$; this value would trigger a ground fault and allow the system controller to take necessary actions. The ground fault detection method described works well for purely resistive faults.

TEST CASE 4

In this test case, not only is SW1 closed to create a leakage resistance path to ground from the HV positive rail, but also switches SW3, SW4, and SW5 in order to connect the Single Phase Inverter. In test case 2, it was demonstrated that the diagnosis of a ground fault could become complex depending on the robustness of the Digital Signal Processing (DSP) within the microcontroller. It is important to understand if a true ground fault can be detected in the case of ripple voltage being superimposed on the measured signal V_{DET}. The results are shown in Figure 19 on Page 38.

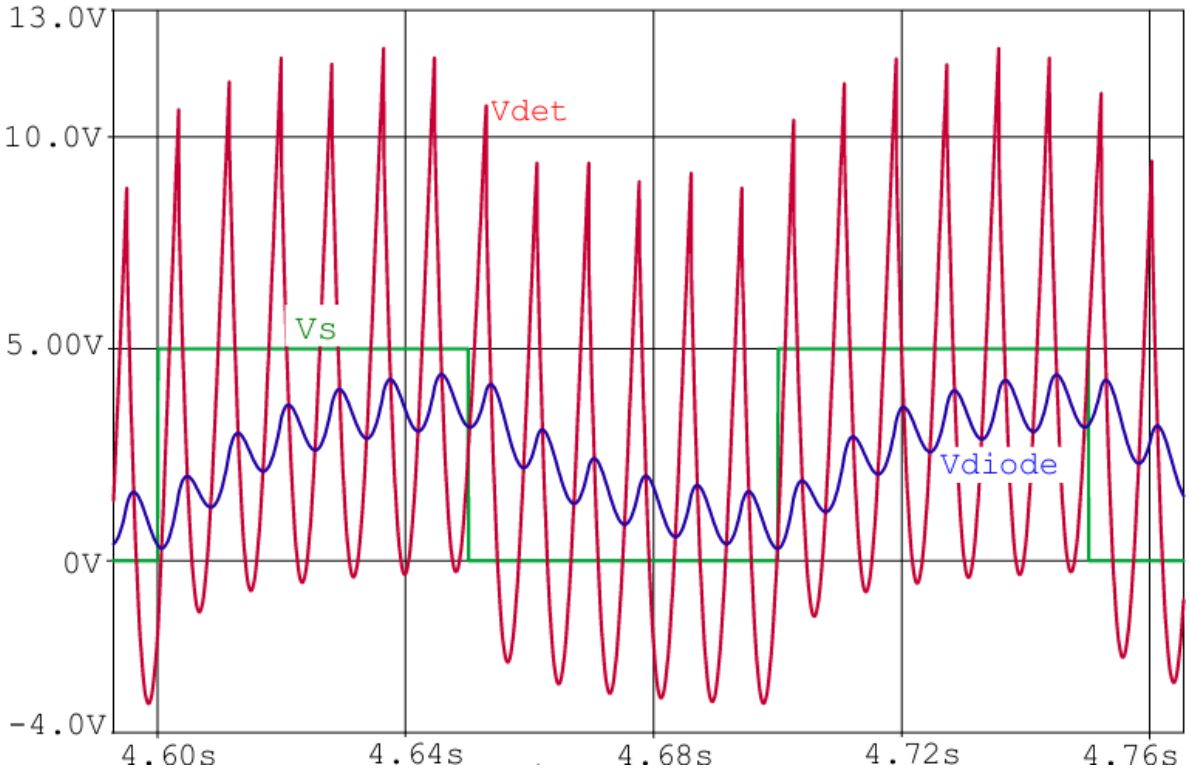

Figure 19: Simulation results for test case 4 of method 1

$$V_{DET(PP)} = 15.55V$$

$$V_{DIODE(PP)} = 4.16V$$

$$V_{DIODE(RMS)} = 2.62V$$

It is apparent that the amplitude of the filtered signal V_{DIODE} (peak to peak) is less than it was in test case 2; however, if the peak to peak voltage was used as a parameter for ground fault diagnosis, the system proposed in this invention would not be able to correctly detect that a ground fault exists, since $V_{DIODE} = 4.16V > V_{TH\_NEW} = 2.92V$.

If the RMS voltage was to be used, the system would potentially be able to detect the fault. As iterated earlier, the effectiveness of the proposed method is reduced in a system with low frequency ripple on the common mode bus.

TEST CASE 5

In this test case, the impact of excessive DC side Y-capacitance on the ground fault detection circuit is analyzed by closing SW3, SW4, SW5, SW7, SW8, SW9, and SW10. Although the single phase inverter is now connected, the device is assumed to not be converting power (hence, no 120Hz ripple).

Although Y-capacitance can be a leak path for AC current to flow from the HV rails to chassis ground, very little AC voltage potential exists on the DC side common mode bus. Therefore, Y-capacitance in the system does not contribute significantly to AC leak currents, and is an open circuit for DC leak currents. Hence, it should not be considered when diagnosing DC ground faults.

One might argue that during single phase inverter operation, low frequency ripple voltage (e.g.120 Hz) on the common mode bus may reach significant amplitudes that could result in unacceptably high AC leak currents flowing through the Y-capacitors to chassis, which could be a shock hazard. Although this is true, there are several design methods that can be implemented to reduce this AC voltage. Moreover, the scope of this invention is to detect resistive faults to ground, and not capacitive faults.

The Single phase inverter, DC-DC Converter, and Auxiliary Load in the test circuit each add 50nF of Y-capacitance to the system. Although 50nF is an arbitrary value, it is not uncommon for manufacturers of High Voltage DC systems to sometimes exceed the maximum allowable Y-capacitance design value for 60 Hz, 120Vrms AC systems (where 60Hz leak current is considered to be worst case as described in Chapter 3). This maximum value may be calculated as follows [14]:

$$C_{Y\_MAX} < \left(\frac{I_{CM\_MAX}}{2\,\pi V_{AC} f}\right)$$

$$C_{Y\_MAX} < \left(\frac{3.5\ \cdot 10^{-3}}{2\,\pi \cdot \left(120\,\sqrt{2}\right) \cdot 60}\right) = 54.7nF$$

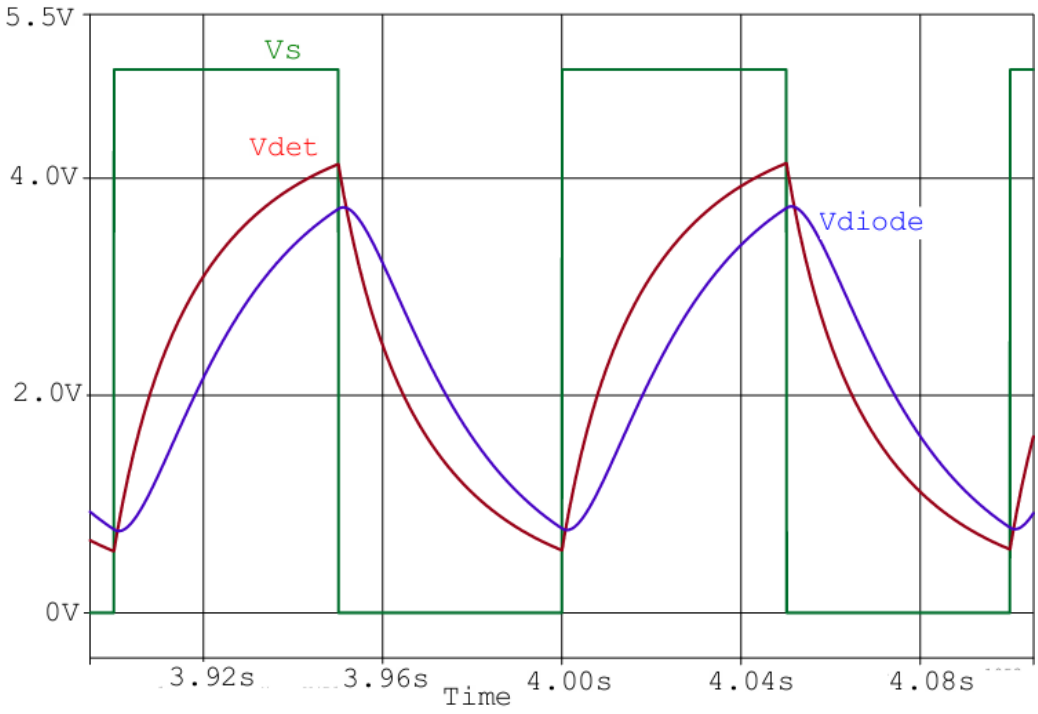

Figure 20: Simulation results for test case 5 of method 1

$$V_{DET(PP)} = 3.58V$$

$$V_{DIODE(PP)} = 12.99V$$

It is evident from the simulation results in Figure 20 that the added capacitance on the common mode bus alter the filter characteristics of the ground fault detection system, hence attenuating the source signal V_S significantly, resulting in $V_{DET(pp)}$ being very close to the threshold voltage V_{TH} of 3.45V. Given this response, a resistive leak path (between HV rail and chassis) larger than the threshold resistance 120kΩ could potentially trigger a ground fault. Depending on the system's reaction to a fault, a false

ground fault diagnosis such as this could result in unwanted shut down of the hybrid system, increased vehicle downtime, and potential warranty costs to be incurred by the manufacturer.

TEST CASE 6

This test case evaluates the response of the ground fault detection system to an AC side leak fault. To achieve this, Switch SW6 in the test circuit is closed to inject a 120kΩ resistive path between the Line 1 output of the Single Phase Inverter and the chassis ground. The simulation results are shown in Figure 21.

Ideally, the ground fault detection system should be able to distinguish between a fault on the DC side and AC side of the HEV power system. In the case of the cited invention, significant ripple voltage on the detected signal V_{DET} increases the complexity of accurately diagnosing a leak fault, since $V_{DIODE(pp)}$ is much higher than the threshold voltage V_{TH_NEW} of 2.92V. Averaging methods implemented in system software might not be a viable option either, due to the magnitude of ripple.

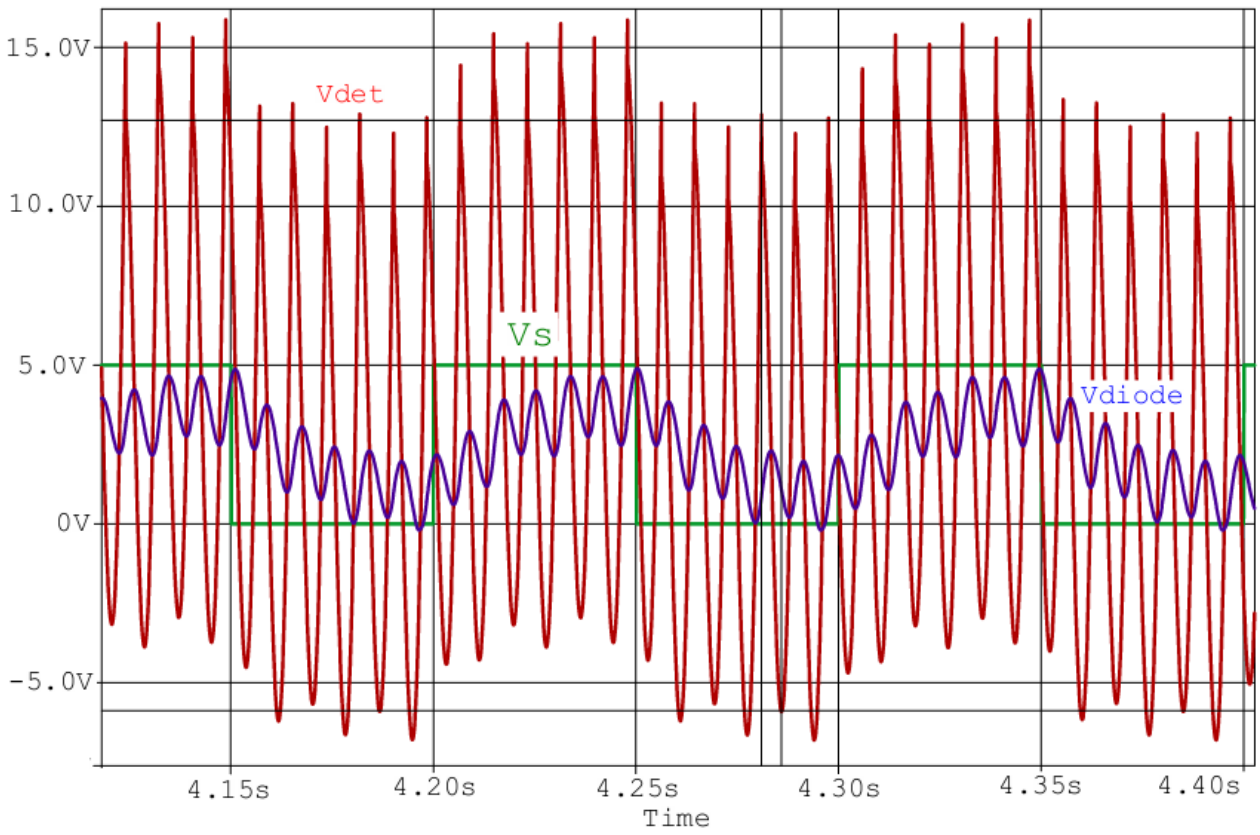

Figure 21: Simulation results for test case 6(a) of method 1

$$V_{DET(PP)} = 18.6V$$

$$V_{DIODE(PP)} = 4.95V$$

In the case of an AC leak fault of very low resistance (e.g. 1Ω), the measured signals V_{DET} and V_{DIODE} would be unreliable diagnostic inputs since the full magnitude of AC voltage will be superimposed onto the common mode bus, as calculated below:

$$V_{RIPPLE} = V_{AC1} \cdot \left(\frac{Z_{DC}}{Z_{DC} + Z_{AC}}\right) = 120 \cdot \sqrt{2} \cdot \left(\frac{Z_{DC}}{Z_{DC} + 1}\right) \approx 120\sqrt{2} \approx 170V$$

Where $Z_{DC} >> 1$

The results of the simulation are shown in Figure 22.

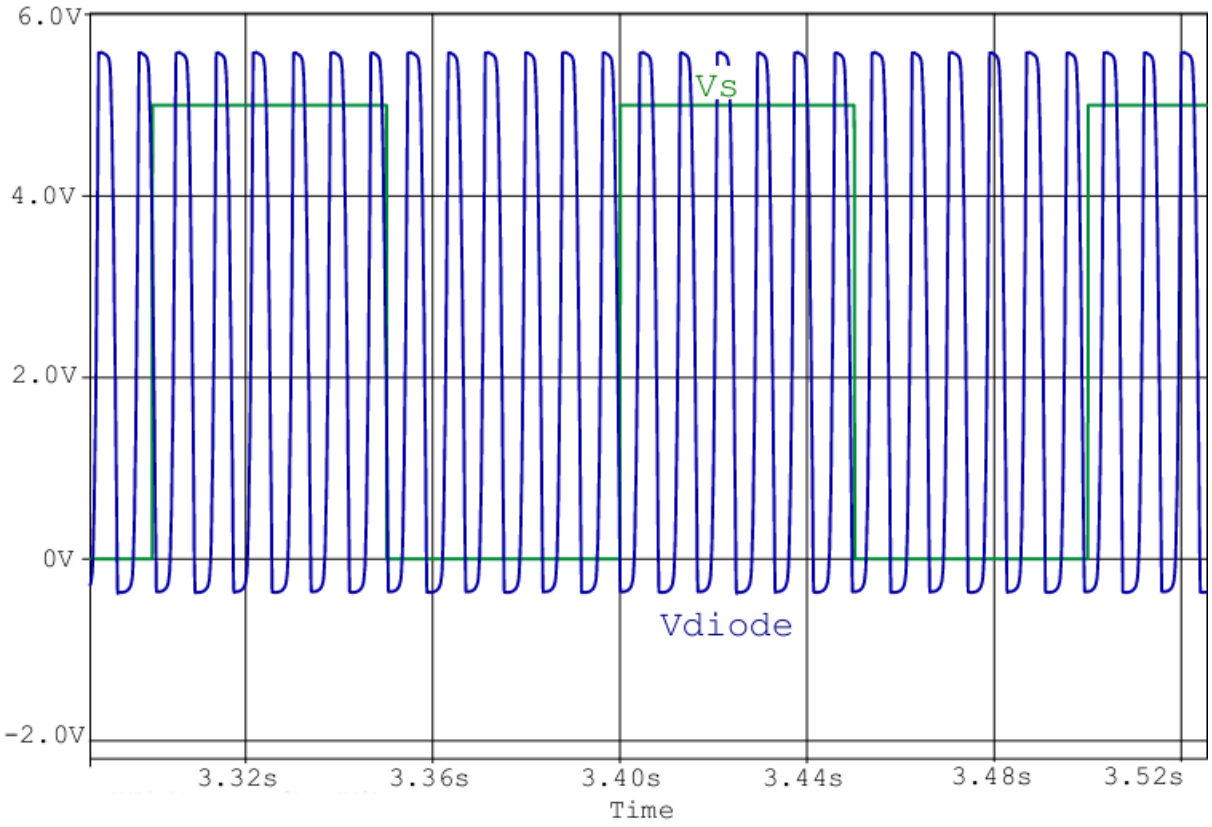

Figure 22: Simulation results for test case 6(b) of method 1

TEST CASE 7

Although there are hybrid vehicle or electric vehicle architectures that operate on a regulated High Voltage bus, many HEV platforms use a variable High Voltage battery source to function. As a result, most power electronic components, such as a Voltage Source Inverter (VSI) with input bulk capacitance, are designed to operate with an input DC source that has a dynamic voltage profile [15]. The steady state voltage of a high energy/ high power battery typically used in a HEV (e.g. 500V lithium ion battery pack) gradually changes based on the state of charge of the pack. However, due to high power pulses in the drive cycle of the vehicle, there are several instances of voltage excursions in the High Voltage bus. This is a direct result of the voltage drop across the Direct Current Resistances (DCR) of cells in the high voltage battery pack, during high current

pulses [16]. In a typical commercial vehicle application, there could exist current pulses nearing 100A for a period of 5-10 seconds. Assuming an arbitrary DCR of $5m\Omega$ per cell in a Li-ion battery pack with 150 cells in series, this would mean voltage excursions of $\Delta V = I \cdot DCR = 100A \cdot 0.005m\Omega \cdot 150 = 75V$ for 5-10 seconds [17].

This test case simulates a power discharge cycle of the High Voltage DC battery by superimposing a random negative voltage waveform on the DC bus, as shown in Figure 23 below, to determine the impact on the measured signal V_{DET}.

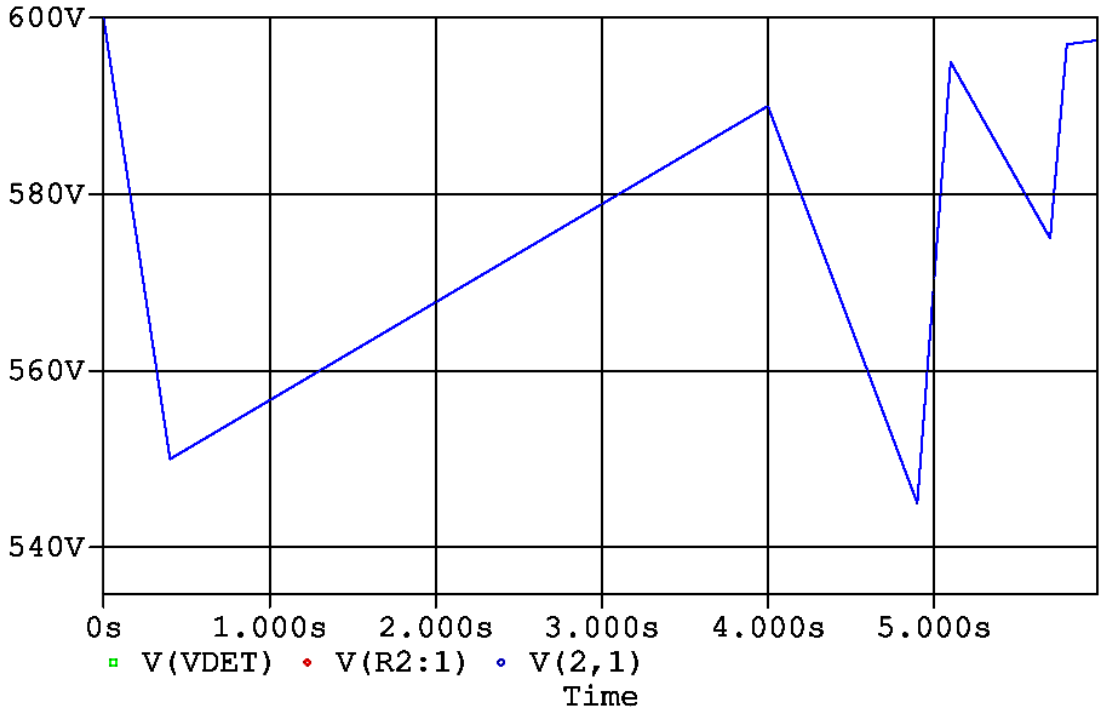

Figure 23: Variation in the HV DC bus voltage during discharge cycle

These transients on the differential HVDC bus are also observed on the common mode bus by virtue of the impedances between the HVDC positive and negative rails and chassis ground. The frequencies of the transients are low enough to pass through unfiltered to the leak detection circuit, resulting in erratic behavior of the signal V_{DET}, as

shown in Figure 24 below. Once again, there is very low fidelity in the signal response data, and diagnostics for ground faults become highly unreliable.

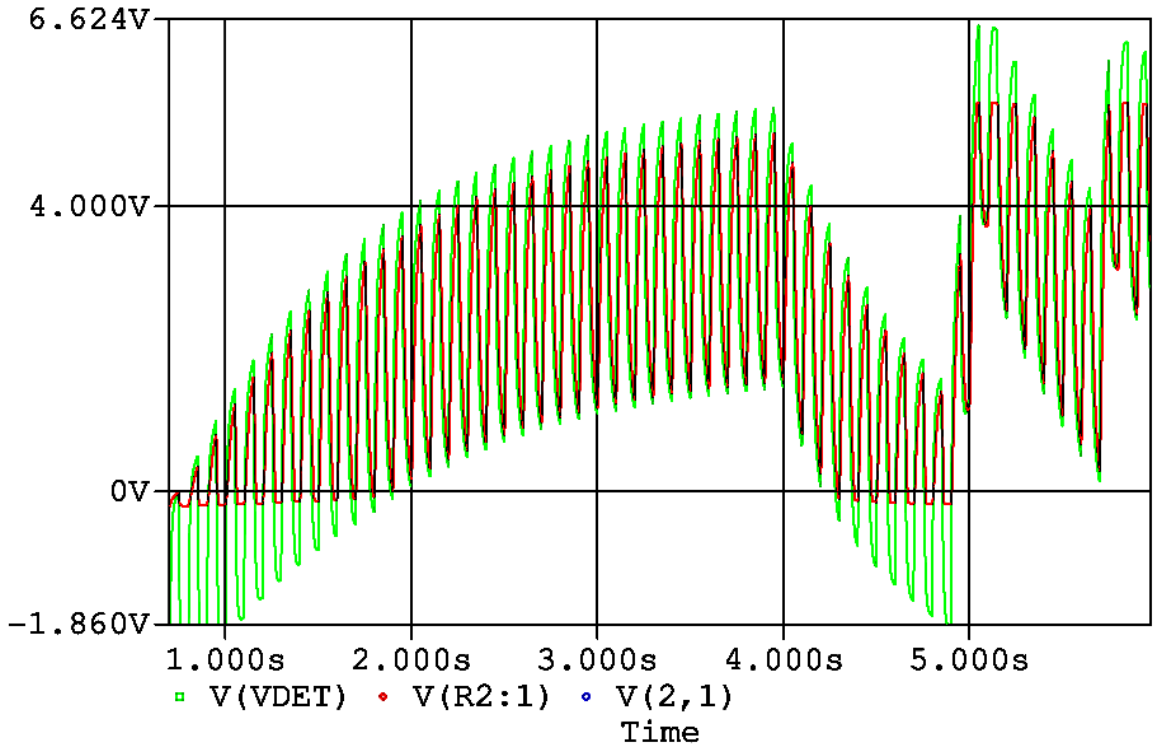

Figure 24: Simulation results for test case 7 of method 1

In conclusion, the method described in this section for ground fault detection is fairly reliable in systems without large magnitudes of Y-capacitance, and those that have isolated power electronics components. In general, however, it is not a suitable method for a flexible hybrid power system as described in Chapter 4.1 for reasons outlined throughout the analysis section.

4.3 Maxim Integrated Products – Fault Detecting Method for Detecting Leak Paths between Power Sources and Chassis

4.3.1 Technology Overview

Inventors Mark Plagens and Brian Fritz from Maxim Integrated Products, Texas developed a method to detect a resistive ground fault condition between a DC power system and the chassis of an EV or HEV. The aforementioned invention was developed to address the need for a reliable detection methodology that would not be susceptible to large amounts of noise created by parasitic or inherent capacitance in the common mode HV bus, or a failed component within the detection circuit itself [18].

The following Figure 25 graphically illustrates the invention:

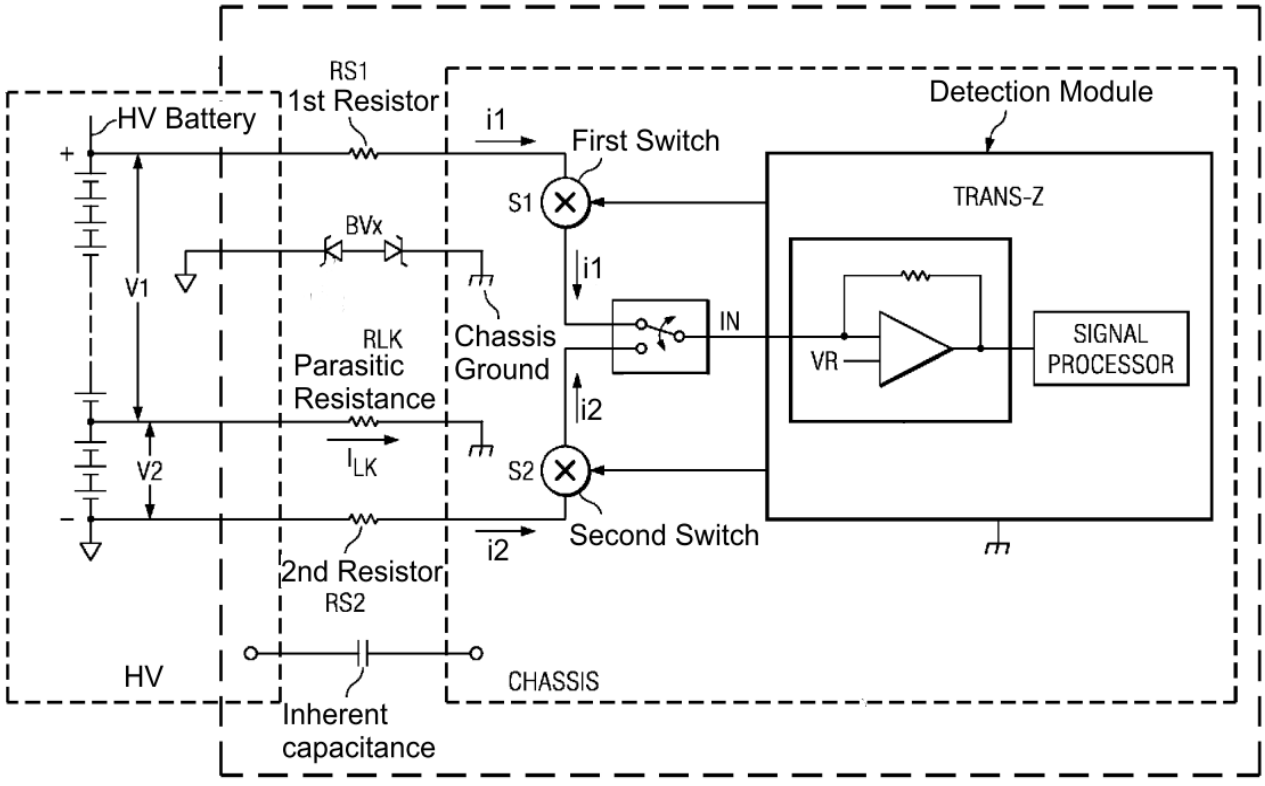

Figure 25: Schematic overview of method 2 [18]

The system described above is designed to detect the total parasitic resistance R_{LK} that exists between the High Voltage bus and chassis ground. A 1st resistor R_{S1} is connected on one end to the positive node of the High Voltage system, and to a switch S1 on the other. The switch S1 when closed allows current to flow from the positive high voltage rail to the chassis. This current I_1 is measured by a current sensor device and then sent to a microcontroller for processing. A 2nd resistor R_{S2} is connected to the High Voltage negative rail on one end and to a switch SW2 on the other. Current I_2 flows from the negative rail of the bus to the chassis ground through SW2 when it is closed, and this current is sensed and processed by the microcontroller in the system.

There also exists inherent capacitance within the system that could be a result of close proximity of high voltage conductors to the chassis of the vehicle. In addition, there are many power electronics components with Y-capacitors for EMI filtering, which could add to the inherent common mode capacitance in the system. The fault detection system functions as described below:

Switch SW1 is first closed at time T_0, causing current I_1 to flow through the resistor R_{S1} and switch SW1 until the inherent capacitance C_N (e.g. 1nF) is charged. As C_N is charged, the value of I_1 declines, ideally approaching zero in a no fault condition due to the large value of the R_{S1} (e.g. 1 MΩ) and the parasitic leakage resistance in the system. At time T_2, switch SW1 is opened and switch SW2 is closed. As a result, inherent capacitance C_N discharges through SW2 and 2nd resistor R_{S2} (e.g. 1 MΩ), and

this current I_2 eventually approaches zero. This behavior is illustrated in Figure 26, and is representative of an ideal system with very large parasitic resistance.

In the case of a true leak fault, when SW1 is closed, current I_1 does not decline because of leakage current flowing through parasitic resistance (e.g. $I_{LK} = 10mA$ through the parasitic resistance R_{LK}). At time T_2, when SW1 is opened and SW2 closed, current I_2 flows through the resistor R_{S2} but again does not decline due to the leakage current across parasitic resistance R_{LK}. The footprint of I_1 and I_2 in this case is shown in Figure 27.

In the case where the parasitic resistance R_{LK} is not very low, but is approaching the threshold of 120kΩ (e.g. 300kΩ), current I_1 declines rapidly but does not approach zero due to the leakage across R_{LK}. This behavior is illustrated in the Figure 28.

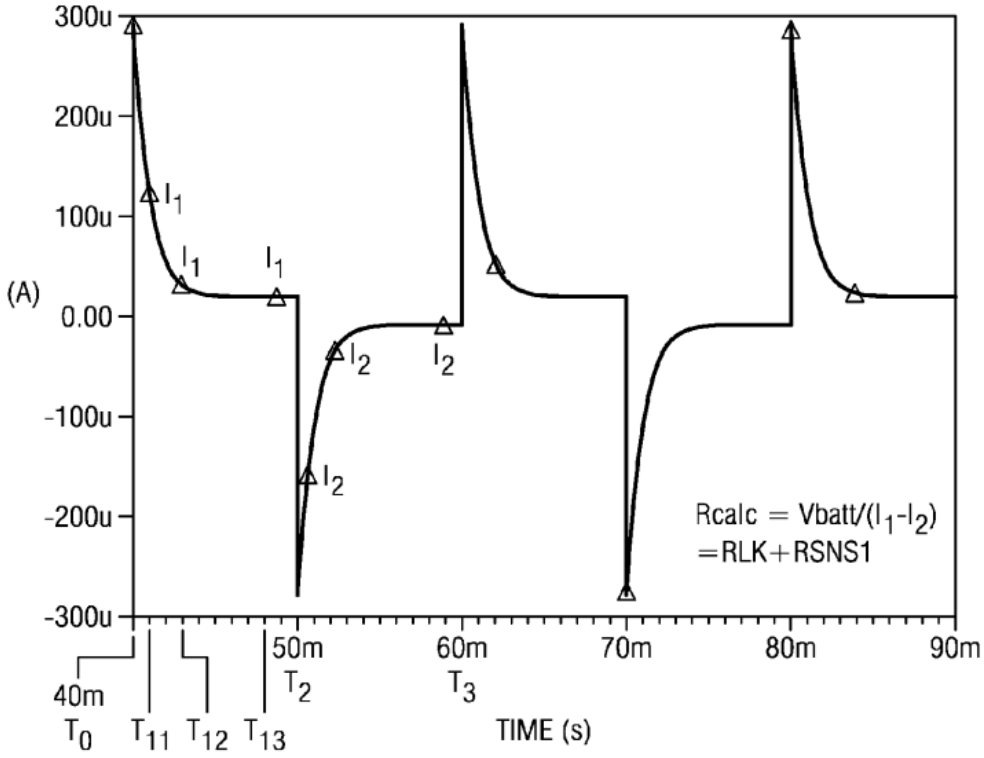

Figure 26: Response of I_1 and I_2 in a no fault condition [18]

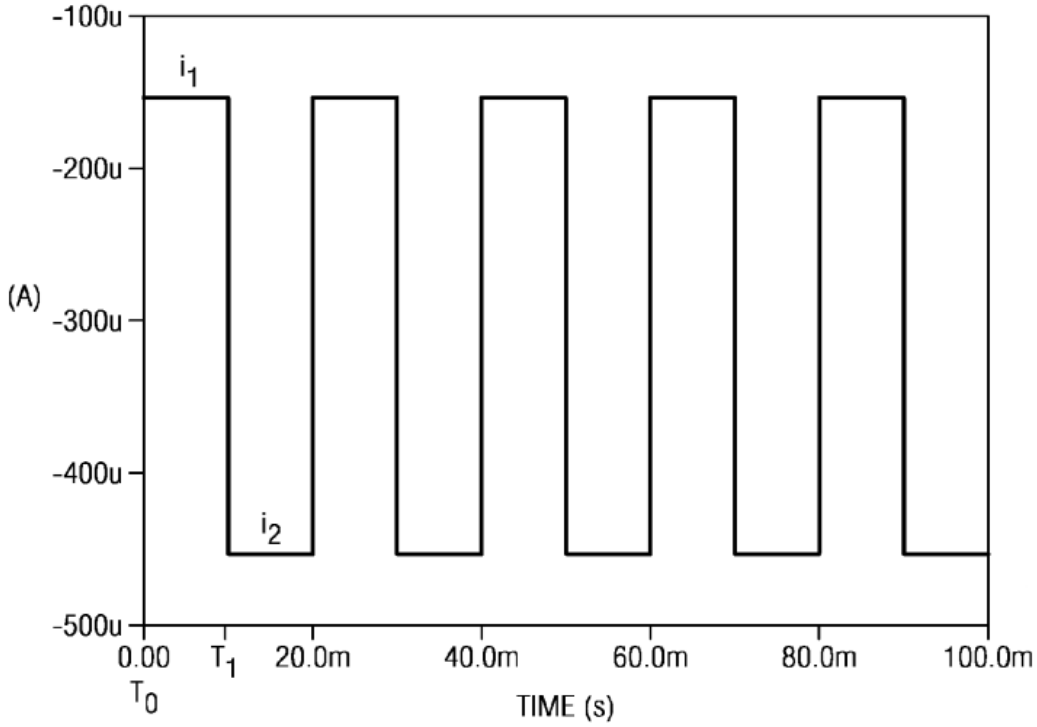

Figure 27: Response of I_1 and I_2 in a true fault condition [18]

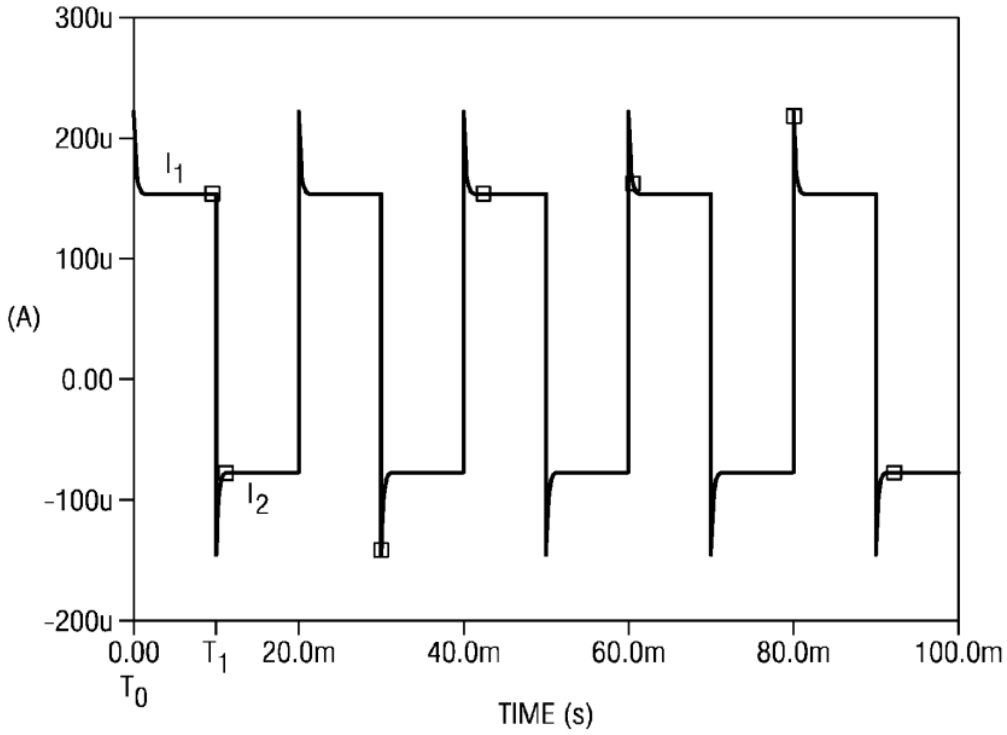

Figure 28: Response of I_1 and I_2 in a low impedance condition [18]

Similarly, in the case of a damaged component in the test circuit, such as an open resistor R_{S1}, no current I_1 will flow through the switch SW1 since the circuit is open. Therefore, the signature of current waveforms I_1 or I_2 are sufficiently unique to diagnose that the detection system has failed. This is one positive aspect of the described invention, where every perturbation in the hybrid power system results in a response with a unique signature that can be processed for reliable diagnostics. This can be achieved by increasing the sampling rate of the current waveform, programming the microcontroller to be able to identify its signature footprint, and then correlating the footprint to a certain operating condition of the system. The patent for the invention provides more detail on the mechanics of this function, which is not within the scope of this paper.

As the microcontroller acquires measurement data for I_1 and I_2, It processes the information to calculate the leakage current I_{LK} in the system, using the following equations:

When SW1 is closed (and SW2 is open):

$$I_1 = \frac{V_P - V_G}{R_{S1} + R_{LK}}$$

Where V_P is the voltage potential at the HV positive node and V_G is chassis ground potential

When SW2 is closed (and SW1 is open):

$$I_2 = \frac{V_N - V_G}{R_{S1} + R_{LK}}$$

Where V_N is the voltage potential at the HV negative

Combining the currents and setting $R_{S1} = R_{S2}$:

$$(I_1 - I_2) = \frac{(V_P - V_G) + (V_N + V_G)}{R_{S1} + R_{LK}} = \frac{V_{BATT}}{R_{S1} + R_{LK}}$$

Since I_1, I_2, V_{BATT}, and R_{S1} are known values, R_{LK} may be calculated as follows:

$$R_{LK} = \left(\frac{V_{BATT}}{I_1 - I_2}\right) - R_{S1}$$

Leading to calculation of leakage current:

$$I_{LK} = \frac{V_{BATT}}{R_{LK}}$$

For accurate calculations of the leakage current, it is critical to use steady state values of I_1 and I_2 (i.e. the set of data points in the tail end of the switch ON phase). The derived value of I_{LK} may then be compared to a threshold leakage current value (e.g. 5mA) to diagnose a ground fault.

4.3.2 Simulation and Analysis

In order to perform a simulation of the fault detection system, the same HV system circuit model shown in Figure 13 of Section 4.2.2 was used, with modifications made to the leak detection circuit (as shown in Figure 29).

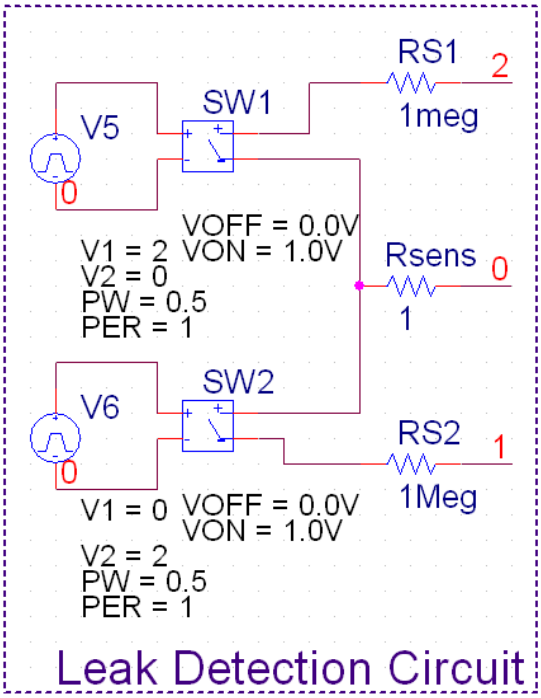

Figure 29: Method 2 leak detection circuit model

The following values were selected for the key parameters of the circuit (next page):

$$R_{S1} = 1M\Omega$$

$$R_{S2} = 1M\Omega$$

$$F_{sw1} = 1\,Hz \text{ (Switching Frequency of SW1)}$$

$$D_{sw1} = 50\% \text{ (ON-OFF Duty Cycle of SW1)}$$

$$F_{sw2} = 1\,Hz \text{ (Switching Frequency of SW2)}$$

$$D_{sw2} = 50\% \text{ (ON-OFF Duty Cycle of SW2)}$$

The switching frequencies of SW1 and SW2 are arbitrarily calculated based on the known fixed inherent capacitance C_N of the system. Using a conservative design approach, the C_N of the system would be the highest when all components are connected to the High Voltage Bus. Assuming 100nF of Y-capacitance each (sum of capacitance from HV positive to chassis and HV negative to chassis) for the Traction Inverter, DC-DC Converter, Auxiliary Load, and Single Phase Inverter, this would amount to:

$$C_N = 100nF \cdot 4 = 400nF$$

The time constant of the circuit switched by SW1 and SW2 would then be (in a no fault condition of $R_{LK} = 1.5M\Omega$):

$$\tau = R_{EQ}C_N = \left(\frac{R_{S1} \cdot R_{LK}}{R_{S1} + R_{LK}}\right) \cdot C_N = \left(\frac{1.5 \cdot 10^{12}}{2.5 \cdot 10^{6}}\right) \cdot 400 \cdot 10^{-9} = 240msec$$

Hence, a switch ON time of 500msec (50% Duty Cycle of 1Hz switching frequency) would result in C_N charging to $1 - e\text{^}(-0.5/0.24) \approx 0.875 \approx 87.5\%$ of the maximum voltage. This allows currents I_1 and I_2 to settle within 13% of their steady

state values, which means that under any condition, the system could have at most 13% error in calculating the actual leakage current in the system (as described in section 4.3.1).

TEST CASE 1

As described in section 4.2.2, this test case is designed to evaluate the response of the ground fault detection system in an ideal, no fault state. The conditions and constraints for the test are the same as in section 4.2.2. The results are plotted in Figure 30 below.

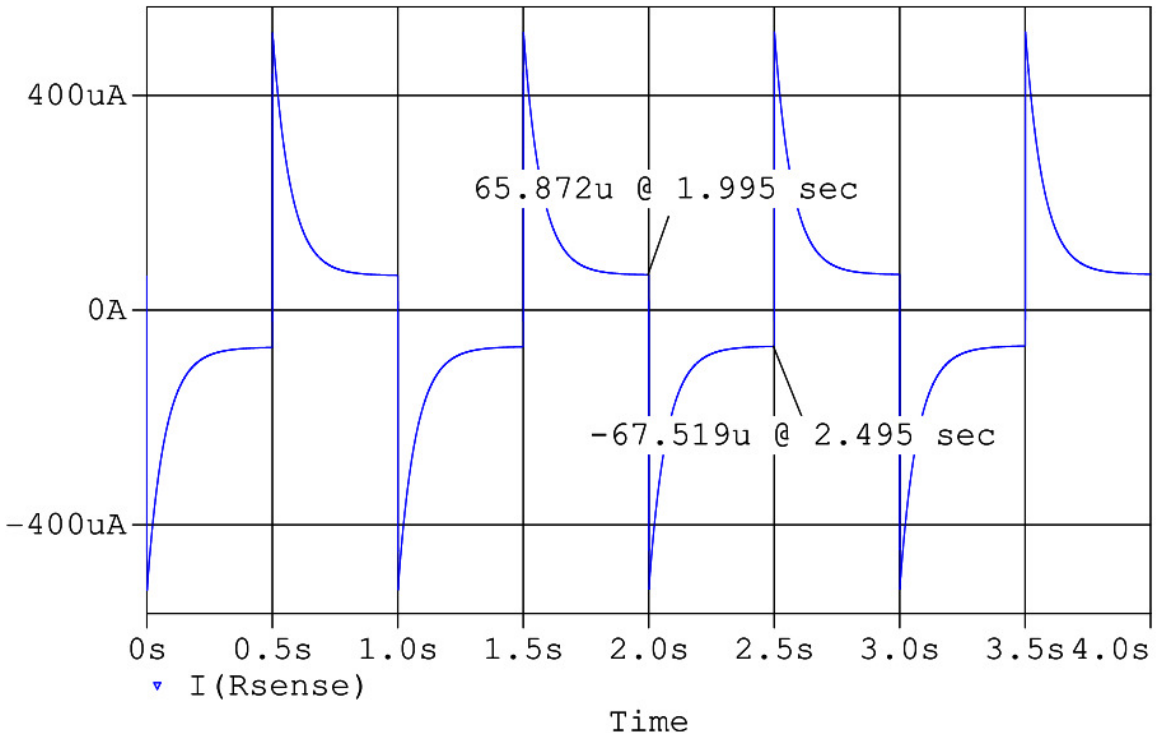

Figure 30: Simulation results for test case 1 of method 2

As expected, the current I_1 is highest at t = 0.5 sec, when the switch S1 is first closed. As the capacitance C_N charges, the current gradually declines to a steady state value at t = 1 sec. Subsequently, the reverse happens to I_2 as the inherent capacitance C_N

initially discharges, and then eventually settles to a steady state value at t = 1.5 sec. The leakage current can therefore be calculated as:

$$R_{LK} = \frac{V_{BATT}}{I_1 - I_2} - R_{S1} = \left(\frac{600}{(65.872 + 67.519)\ \cdot 10^{-6}}\right) - 1\ \cdot 10^{6} \approx 3.5M\Omega$$

$$I_{LK} = \frac{V_{BATT}}{R_{LK}} = \frac{600}{3.5\ \cdot 10^{6}} = 171.14\mu A$$

Evidently, this is not greater than the leakage current threshold $I_{TH} = 5mA$, therefore a ground fault will not be set.

TEST CASE 2

The second test case is to evaluate the response of the circuit when a non-isolated single phase inverter is connected to the HV battery. The conditions and constraints are similar to those described in section 4.2.2. Unlike what was observed for the detection methodology described in the previous section, there is little impact on the current waveforms I_1 and I_2 that are used as inputs for diagnosis. This is illustrated Figure 32.

The leakage current in this case is 1.22mA, because of the resistors between high voltage rails and chassis inside the inverter. Furthermore, the peak to peak amplitude of the current ripple is 8.37uA (as shown in Figure 32), which is insignificant. The circuit therefore is robust to low frequency voltage ripple on the common mode bus.

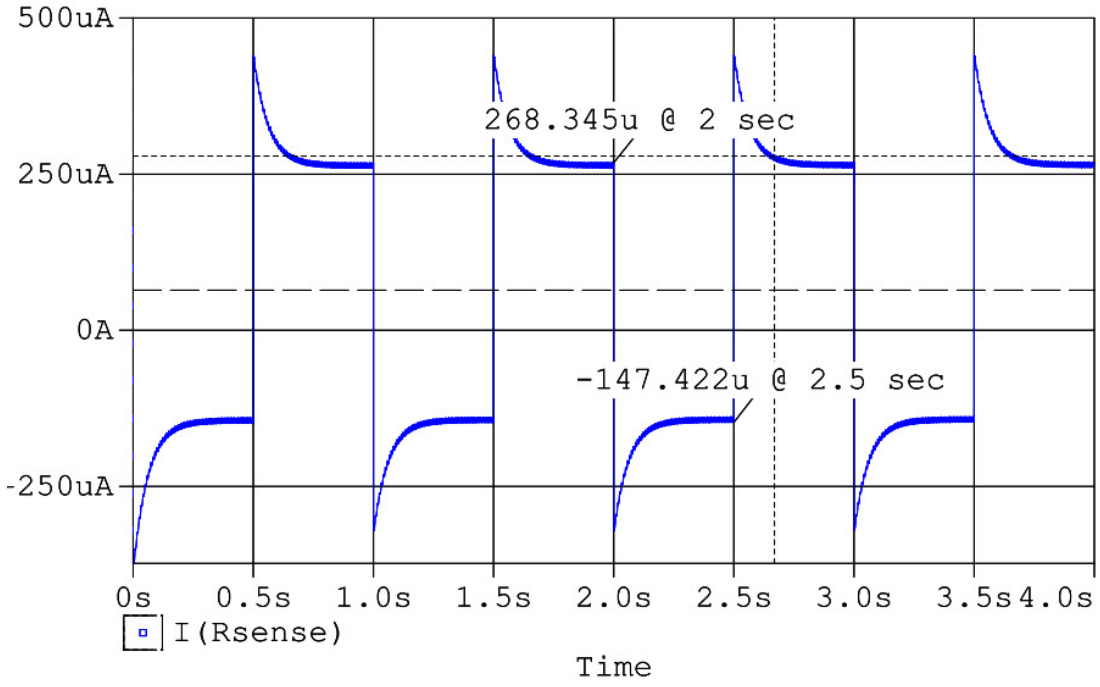

Figure 31: Simulation results for test case 2 of method 2

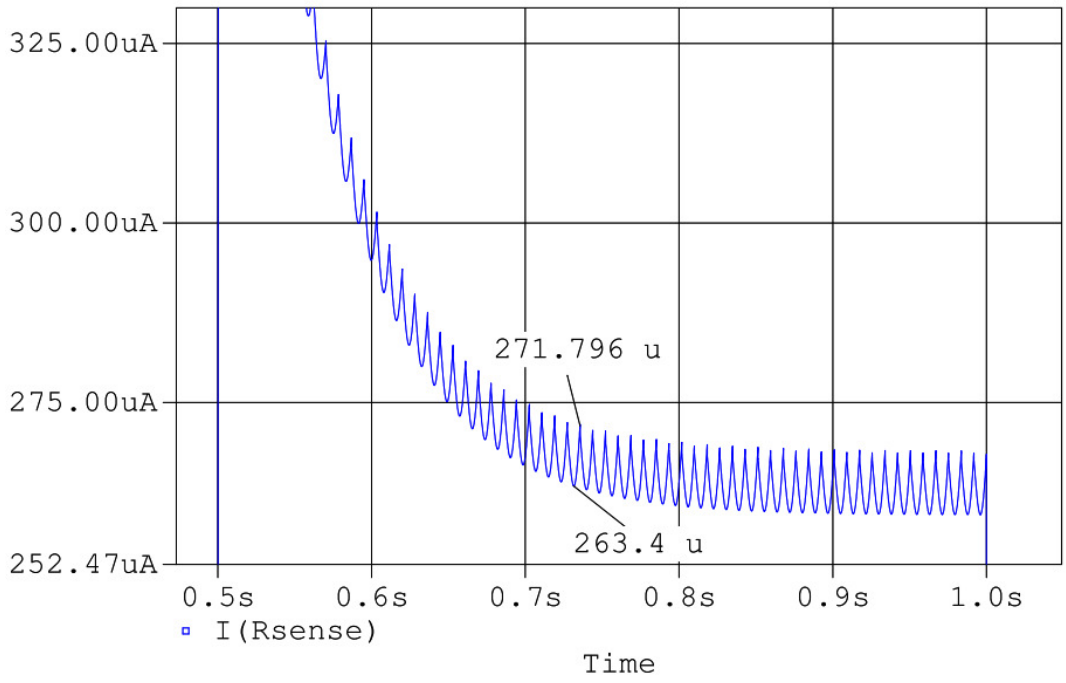

Figure 32: Zoomed simulation results for test case 2 of method 2

TEST CASE 3

This test case is to evaluate the response of the circuit in a true fault condition. The conditions and constraints of this test case are similar to those in test Case 4 of section 4.2.2. A 120kΩ leak fault is induced between the high voltage positive rail and chassis, while the single phase inverter is connected to the system. The results are shown in Figure 33.

The leakage current is calculated to be 5.70mA based on the simulation, which is an accurate representation of the true leakage current.

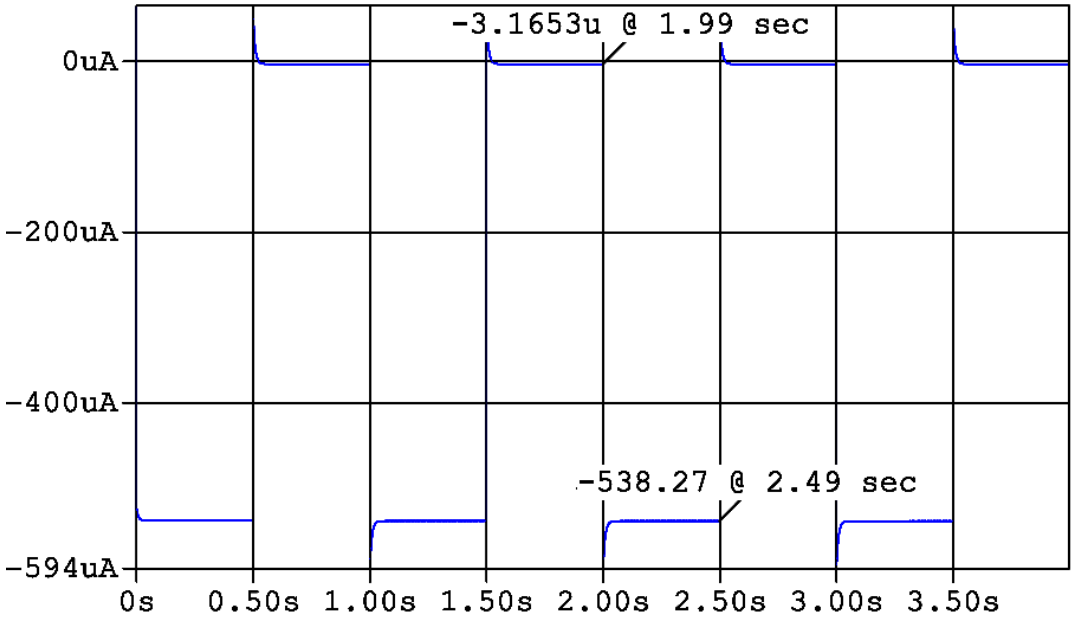

Figure 33: Simulation results for test case 3 of method 2

TEST CASE 4

This test case is synonymous to test case 5 in section 4.2.2, where the response of the leak detection circuit to added Y-capacitance the common mode bus is evaluated.

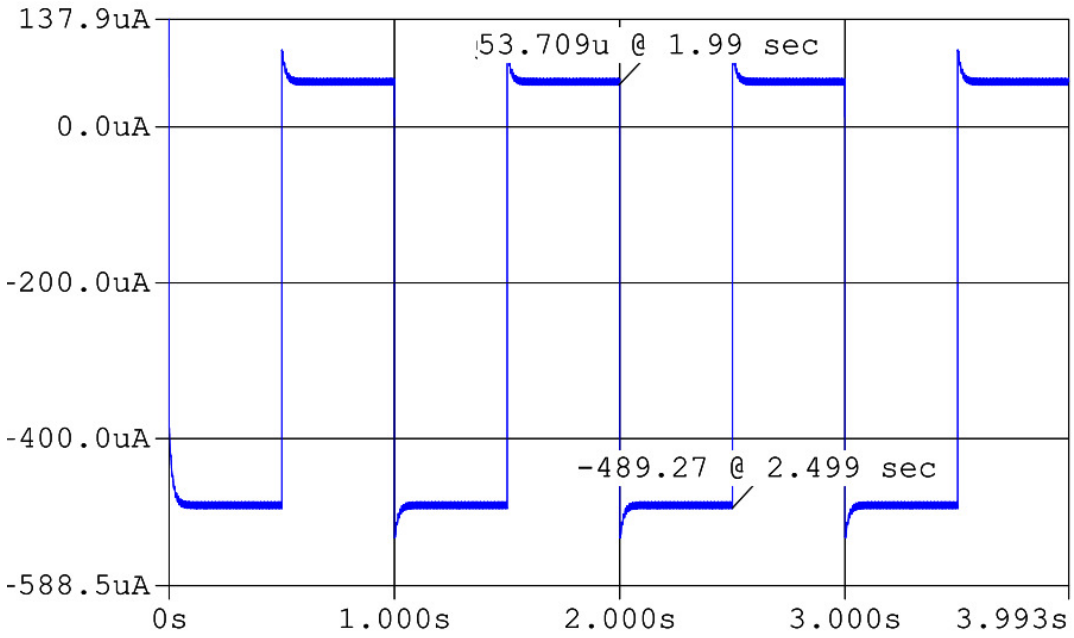

Figure 34: Simulation results for test case 4 of method 2

With a switching period of 500 msec, there is sufficient time for current I_1 and I_2 to settle to a steady state current, in spite of 150nF of added capacitance C_N. The calculated leakage current is 338.95uA, which once again is a fair representation of the DC leak current from HV rail to ground.

TEST CASE 5

The conditions and constraints of this test case are similar to those of test case 6 in section 4.2.2. The purpose of this simulation is to evaluate the response of the leak detection system to an AC ground fault of 1Ω (short circuit). The results are shown in the Figure 35 below.

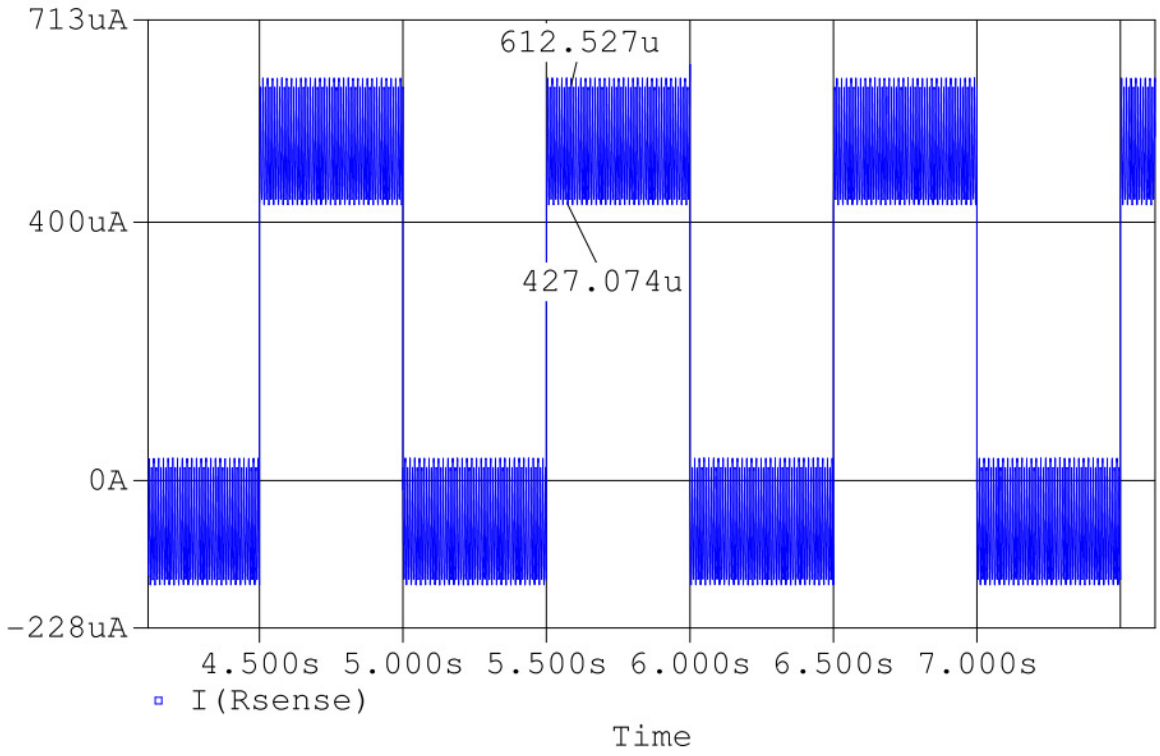

Figure 35: Simulation results for test case 5 of method 2

There is a distinct signature to the footprint of the waveform in an AC leak fault condition. As expected, a significant portion of the AC output of the single phase inverter (@ 120Hz) is superimposed onto the common mode DC bus, causing AC leak currents to flow through the capacitance CN. The amplitude of the AC leak current can be calculated by measuring the peak and trough of the 120Hz component of the waveform, Therefore, if the sampling frequency of the waveform was increased (e.g. 1000Hz), it would be possible to identify the frequency and amplitude of the AC leak current, and diagnose an AC leak fault within the system.

TEST CASE 6

The conditions and constraints of this test case are similar to those of test case 7 in section 4.2.2. The purpose of this simulation is to evaluate the impact of voltage swings in the DC bus on the current waveforms I_1 and I_2. The results are shown in Figure 36.

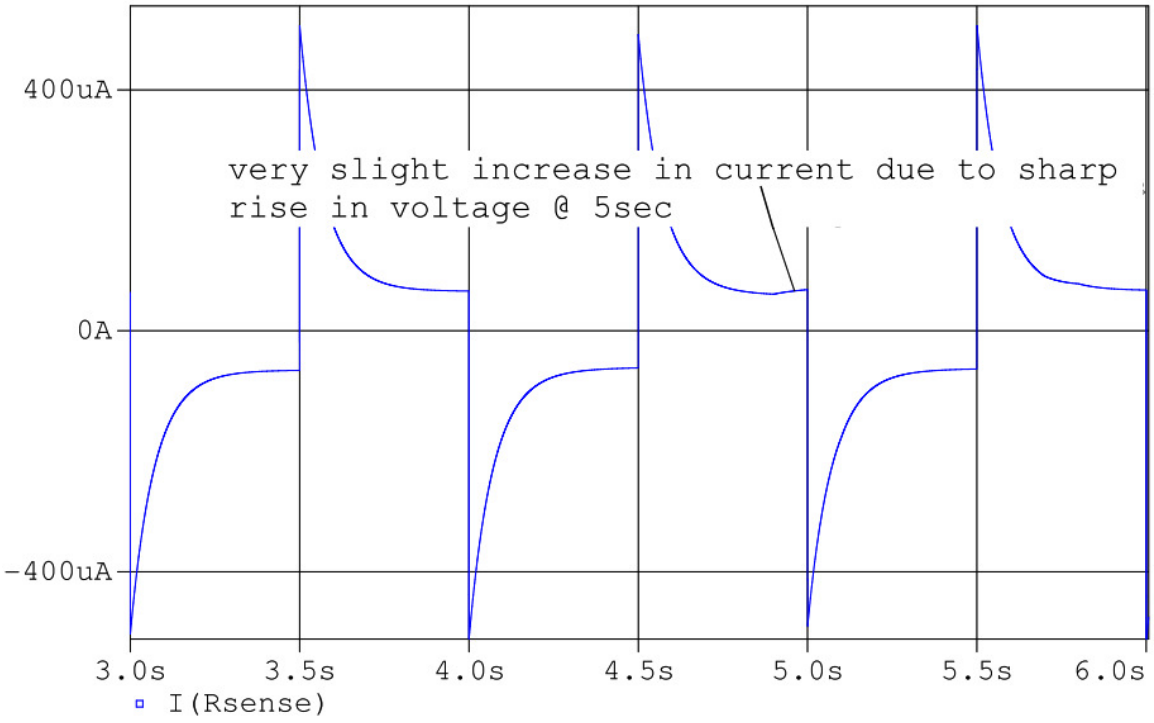

Figure 36: Simulation results for test case 6 of method 2

As expected, the currents I_1 and I_2 are slightly skewed due to the swing in voltage. However, this does not affect the calculation of leakage current I_{LK} because the value of V_{BATT} also changes dynamically with I_1 and I_2. As a result, voltage swings in the DC bus will not impact the reliability of the ground fault detection system.

4.4 Lear Corporation – Ground Fault Detection System for Vehicles with High Voltage Power Net

4.4.1 Technology Overview

Inventors Miguel Angel Acena and Jordi Escoda from Lear Corporation, Michigan developed a method to detect loss of electrical isolation in a vehicle that uses a HV power net [19]. This is achieved by charging HV capacitors, then connecting them at different times between the HV positive and negative rails and the vehicle chassis, and measuring the remaining charge after a fixed period of time. The amount of energy lost in the capacitors reflects the level of isolation of the floating HV power system to chassis ground. If the discharge is low (shallow), the equivalent resistance to ground is high and the isolation can be characterized as proper. If the discharge is above some nominal level, the equivalent resistance is lower and isolation can be characterized as improper [19]. Once again, the primary purpose of the proposed methodology is to detect resistive leak faults in the system, in both energized and non-energized states. There are minor variations in the implementation of the fault detection system for a vehicle in the off-state (when the HV batteries are disconnected) in comparison to a system for a vehicle in the on-state (HV batteries are connected). However, the design principle behind both systems is the same, and for the purpose of evaluating this method, we will analyze the fault detection method designed for an energized system.

Figure 37 below shows an illustration of the Ground Fault Detection System (GFDS).

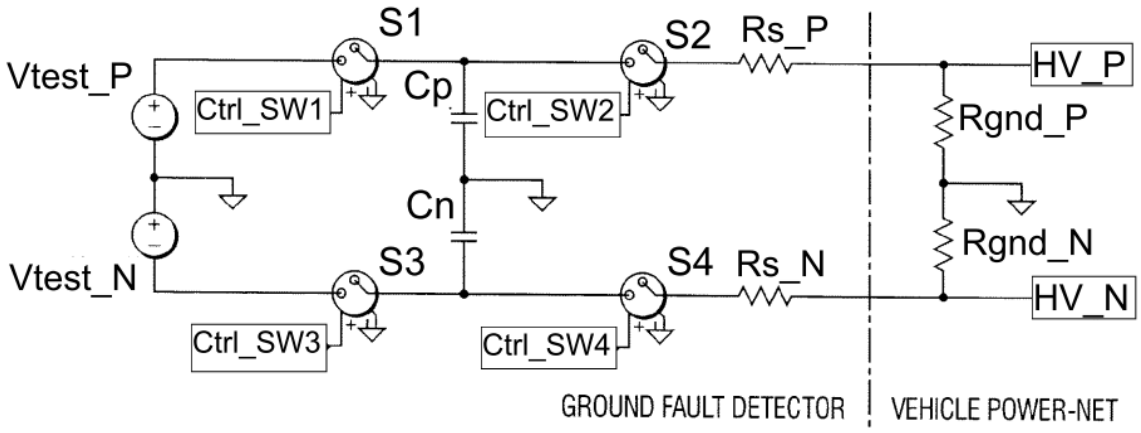

Figure 37: Schematic overview of method 3 [19]

From Figure 37, HV_P and HV_N are the High Voltage Positive and High Voltage Negative power nets respectively. This typically represents the High Voltage bus of the hybrid vehicle, which contains the HV battery pack and the power electronics components of the system. V_{TEST_P} and V_{TEST_P} are two sources that are separate from the HV battery, and are used to charge the capacitors C_P and C_N through switches S1 and S3 respectively. Switches S2 and S4 are used to connect each of C_P and C_N to the HV vehicle power lines (HV_P and HV_N) for a fixed time. R_{GND_P} and R_{GND_N} are the inherent resistances of the high voltage system to chassis ground, and resistors R_{S_P} and R_{S_N} are intended to limit the discharge current from the capacitors C_P and C_N in the case of a very low value of R_{GND_P} or R_{GND_N} (e.g. a short circuit) [19].

The aforementioned HV battery can be represented as an ideal voltage source plus a low equivalent series resistor (R_{S_BATT}). By applying Thevenin's theorem to the vehicle power net at HV_P and HV_N with respect to chassis ground, the circuits in Figure

38 arise. Assuming R_{S_BATT} is negligible in comparison to R_{GND_N} and R_{GND_P}, the following equations may be derived:

$$R_{P\_EQ} = \frac{R_{GND\_N} \cdot R_{GND\_P}}{R_{GND\_N} + R_{GND\_P}}$$

$$V_{P\_EQ} = V_{BATT} \cdot \frac{R_{GND\_P}}{R_{GND\_N} + R_{GND\_P}}$$

$$R_{N\_EQ} = \frac{R_{GND\_N} \cdot R_{GND\_P}}{R_{GND\_N} + R_{GND\_P}}$$

$$V_{N\_EQ} = V_{BATT} \cdot \frac{R_{GND\_N}}{R_{GND\_N} + R_{GND\_P}}$$

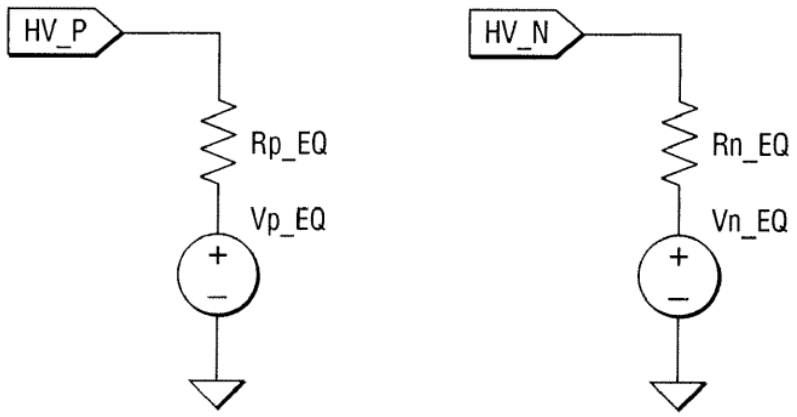

Figure 38: Equivalent circuit of common mode bus [19]

The operation of the GFDS can be described by observing the timing of the four switches S1, S2, S3, and S4. Assuming all switches are initially in the open state, switch S1 is closed at time t_1 to allow C_P to be charged up to V_{TEST_P}. Before t_2, the capacitor is completely charged (i.e.$V_{CP} = V_{TEST\_P}$) and then S1 opens. At t_3, S2 is closed and kept in that state up to t_4. During this interval ($t_{SW2} = t_4 - t_3$) the capacitor C_P is

discharged through a resistance that equals the sum of R_{S_P} and R_{P_EQ}. After the discharging process, at time t_{CP}, the resulting voltage across the capacitor C_P (i.e. V_{CP}) can be approximated by the following equation:

$$V_{CP(t=t_{CP})} = \left(V_{TEST\_P} - V_{P\_EQ}\right) \cdot e^{-\frac{t_{SW2}}{C_P \cdot \left(R_{S\_P} + R_{GND\_EQ}\right)}} + V_{P\_EQ}$$

This voltage V_{CP} (at time t_{CP}) reflects the level of isolation that exists between HV_P and chassis ground (i.e. R_{GND_EQ}) since it is related to R_{GND_EQ} as shown in the equation above.

A similar process can be followed using the switches S3 and S4 in order to arrive at the following equation for the voltage across the capacitor C_N (i.e. V_{CN}) after it goes through the discharging process:

$$V_{CN(t=t_{CN})} = \left(V_{TEST\_N} - V_{N\_EQ}\right) \cdot e^{-\frac{t_{SW4}}{C_N \cdot \left(R_{S\_N} + R_{GND\_EQ}\right)}} + V_{N\_EQ}$$

From the equation above, it is evident that both V_{TEST_P} and V_{TEST_N} must be greater than V_{BATT}. This guarantees that the capacitors C_P and C_N are charged up to a voltage higher than V_{BATT}, ensuring that there is charge available for the HV power net for any value of R_{GND_EQ}. This can be achieved in several ways, and the patent discloses one method which uses a flyback converter to step up the vehicle's 12V battery voltage to the desired V_{TEST_P} and V_{TEST_N}.

Figure 39 graphically illustrates the sequencing of the switches. The measured values of V_{CP} at time t_{CP} and V_{CN} at time t_{CN} can then be used to calculate R_{GND_EQ}, and subsequently compare the result to a threshold value R_{TH} (e.g. 120kΩ) to determine whether a fault condition exists or not.

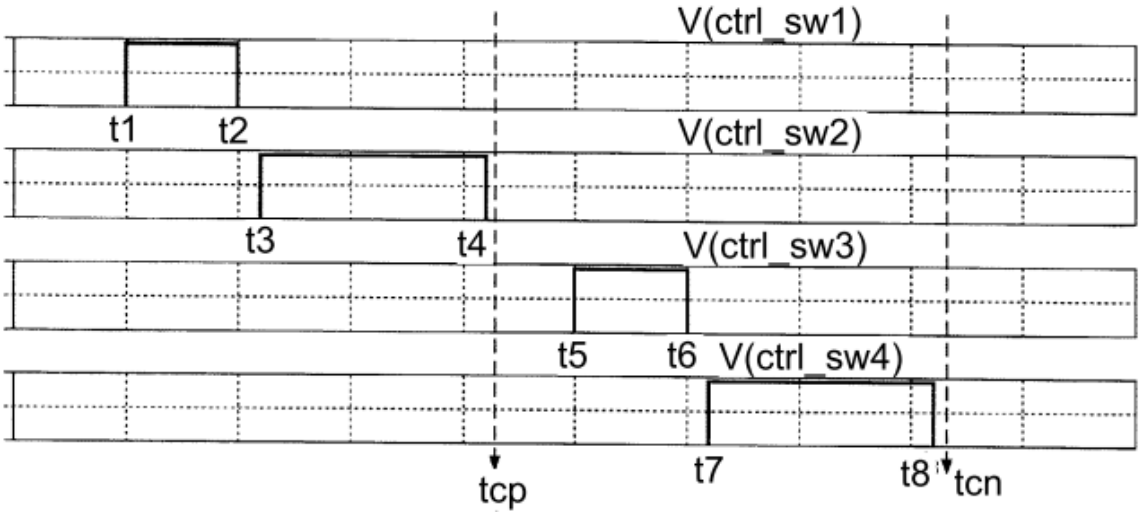

Figure 39: Sequence of switch operation for method 3 [19]

4.4.2 Simulation & Analysis

In order to perform a simulation of the GFDS, the same HV system circuit model shown in Figure 13 of Section 4.2.2 was used, with modifications made to the leak detection circuit (as shown in Figure 40).

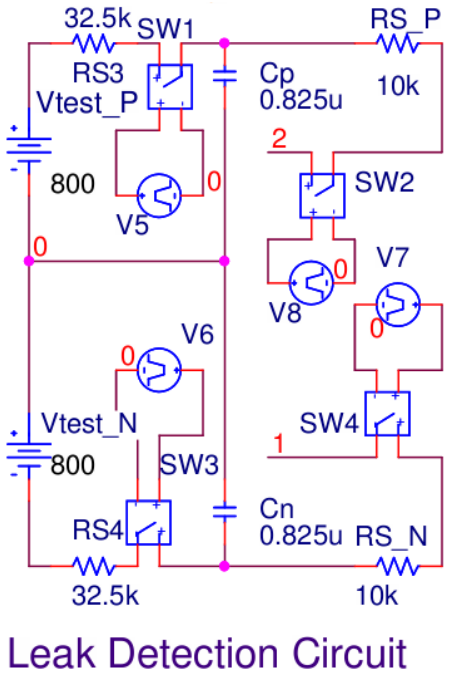

Figure 40: Leak detection circuit model for method 3

Assuming that the maximum differential voltage of the HV bus (V_{BATT}) is 600V, V_{TEST_P} and V_{TEST_N} have been arbitrarily chosen to be 800V, which is higher than V_{BATT}. The choice of parameters C_P, C_N, R_{SN}, R_{SN}, R_{S3}, and R_{S4} is dependant on the switching times t_1 through t_8. Time $t_{SW1} = t_2 - t_1$ is the length of time that switch SW1 is ON and C_P is charging, and $t_{SW2} = t_4 - t_3$ is the length of time that switch SW2 is ON and C_P is discharging. Considering 120kΩ to be the threshold for low ground resistance (R_{GND_EQ}), the level of discharge of capacitor C_P to be 90% of its original voltage, and t_{SW2} to be 245 msec (leaving 5 msec as dead time between t_{SW2} and t_{SW3}), the value of C_P can be calculated as follows:

$$V_{CP(t=t_{CP})} = V_{TEST\_P} \cdot e^{-\frac{t_{SW2}}{C_P \cdot (R_{S\_P} + R_{GND\_EQ})}}$$

Where:

$$V_{CP} = 10\% \, of \, V_{TEST\_P} = 80V$$

$$t_{sw2} = 245 \, msec$$

$$R_{S\_P} = 10k\Omega$$

$$R_{GND\_EQ} = 120 \, k\Omega$$

Therefore, $C_P \approx 825\mu F$

A similar set of calculations can be performed for selecting C_N.

Now, using an arbitrarily low value for $t_{SW1} = 99 \, msec$ (leaving 1 msec as deadtime between t_{SW1} and t_{SW2}), and assuming a level of charge of 98% for C_P, R_{S3} may be calculated as follows:

$$V_{CP(t=t_2)} = V_{TEST\_P} \cdot (1 - e^{-\frac{t_{SW1}}{C_P \cdot R_{S3}}})$$

Where:

$$V_{CP} = 98\% \, of \, 800V \approx 780V$$

$$t_{SW1} = 99 \, msec$$

$$C_P = 825uF$$

Therefore, $R_{S3} \approx 32.5k\Omega$

Since $t_{SW1} = t_{SW3} = 99\,msec$, and $t_{SW2} = t_{SW4} = 245\,msec$, the total period for leak detection in this case is ~700 msec. This is shown in Figure 41.

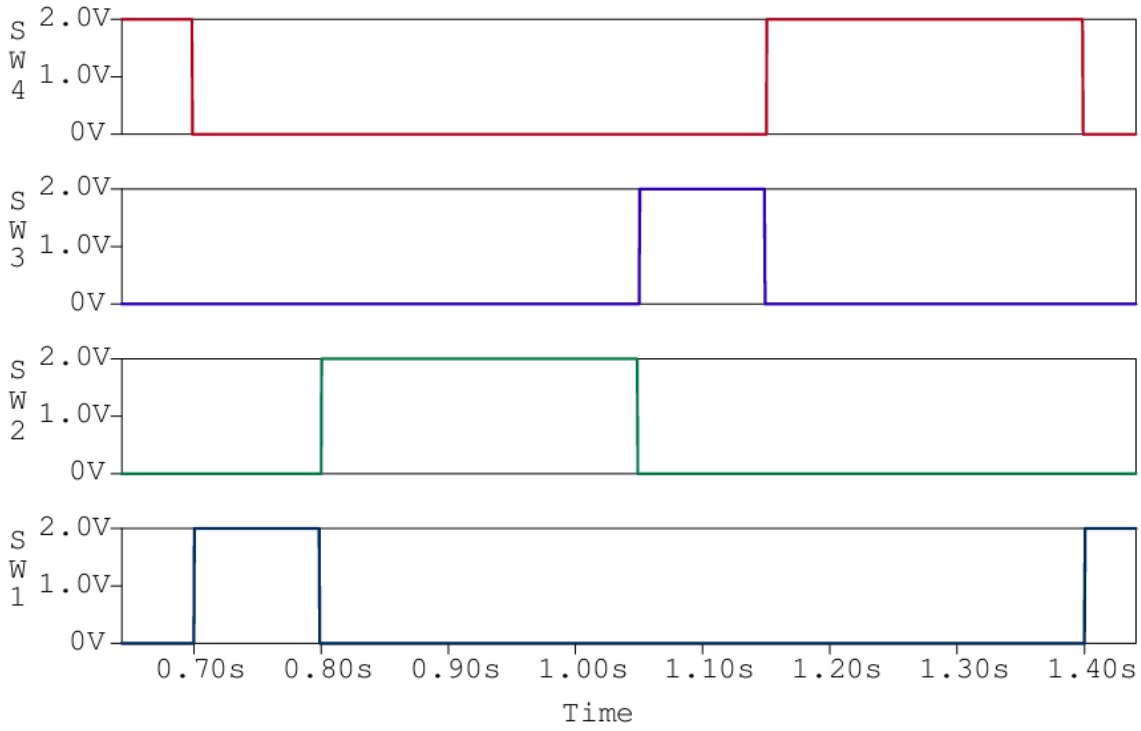

Figure 41: Sequencing of switches for simulation

For simplification of the analysis process, only the response characteristic of V_{CP} will be evaluated throughout this section. Since all the data required for calculation of the common mode resistance (R_{GND_EQ}) can be gleaned from phase 2 of the diagnostic cycle (i.e. t_{SW2}), emphasis will be placed on evaluating the circuit's response during this phase.

TEST CASE 1

As described in section 4.2.2, this test case is designed to evaluate the response of the ground fault detection system in an ideal, no fault state. The conditions and

constraints for the test are the same as in section 4.2.2. The results are plotted in Figure 42.

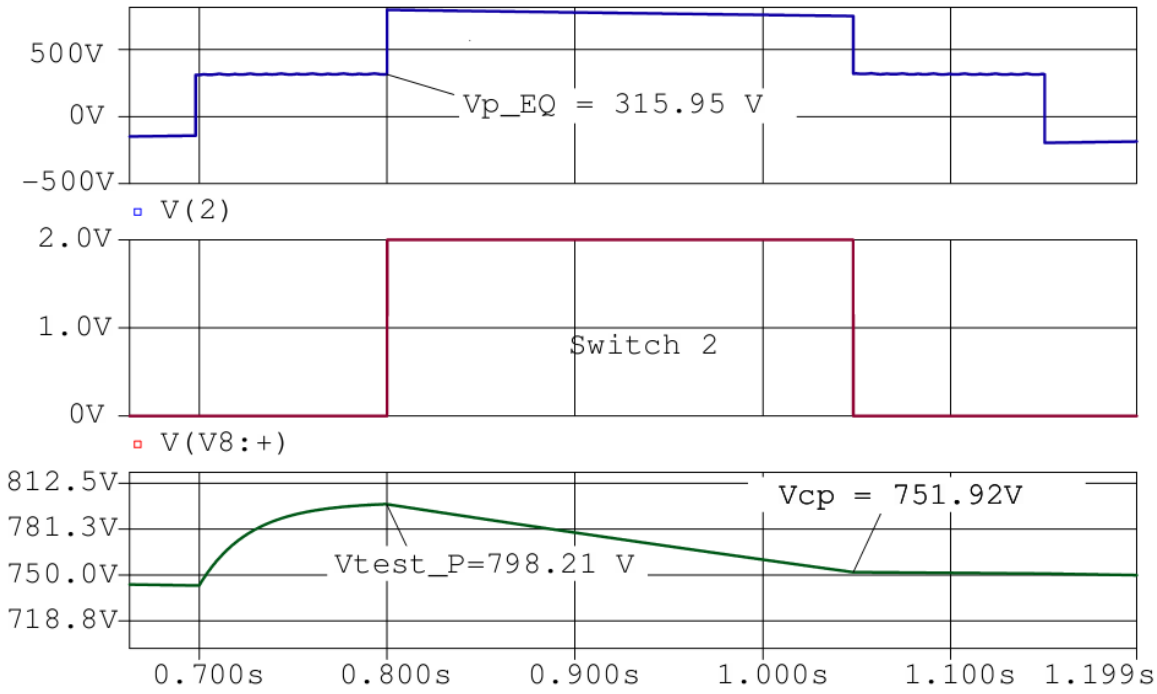

Figure 42: Simulation results for test case 1 of method 3

As is evident in Figure 42, the bottom graph represents the voltage V_{CP}, the middle graph represents the state of SW2 (2V being ON, and 0V being OFF), and the top graph represents the voltage V_{PEQ} (i.e. HV_P with respect to chassis ground). Since isolation between the high voltage bus and chassis ground is high, the discharge of capacitor C_P is shallow, and the equivalent ground resistance can be calculated as follows:

$$V_{CP}(t = t_{CP}) = \left(V_{TEST\_P} - V_{P\_EQ}\right) \times e^{-\frac{t_{SW2}}{C_P\left(R_{S\_P}+R_{GND\_EQ}\right)}} + V_{P\_EQ}$$

Therefore,

$$R_{GND\_EQ} = \frac{t_{sw2}}{ln\left(\frac{V_{TEST\_P} - V_{P\_EQ}}{V_{CP} - V_{P\_EQ}}\right) C_P} - R_{S\_P}$$

$$R_{GND\_EQ} = \frac{0.245}{ln\left(\frac{798.21 - 315.95}{751.92 - 315.95}\right) \times 0.825 \times 10^{-6}} - (10 \cdot 10^3)$$

$$R_{GND\_EQ} \approx 2.96M\Omega$$

Since the threshold to set a ground fault is R_{TH} = 120kΩ, no fault is set in this case.

TEST CASE 2

The second test case is to evaluate the response of the circuit when a non-isolated single phase inverter is connected to the HV battery. The conditions and constraints are similar to those described in section 4.2.2, with the exception that the DC-DC Converter and Auxiliary Load 1 are also connected (thereby adding 100nF each of common mode capacitance between HV_P and ground, and HV_N and ground). The added 120Hz ripple from the single phase inverter has a negligible impact on the voltage waveform V_{CP}, as shown in Figure 43. The level of discharge is higher than it was in test case 1 due to the added common mode capacitance, as well as the 2MΩ resistors in the inverter.

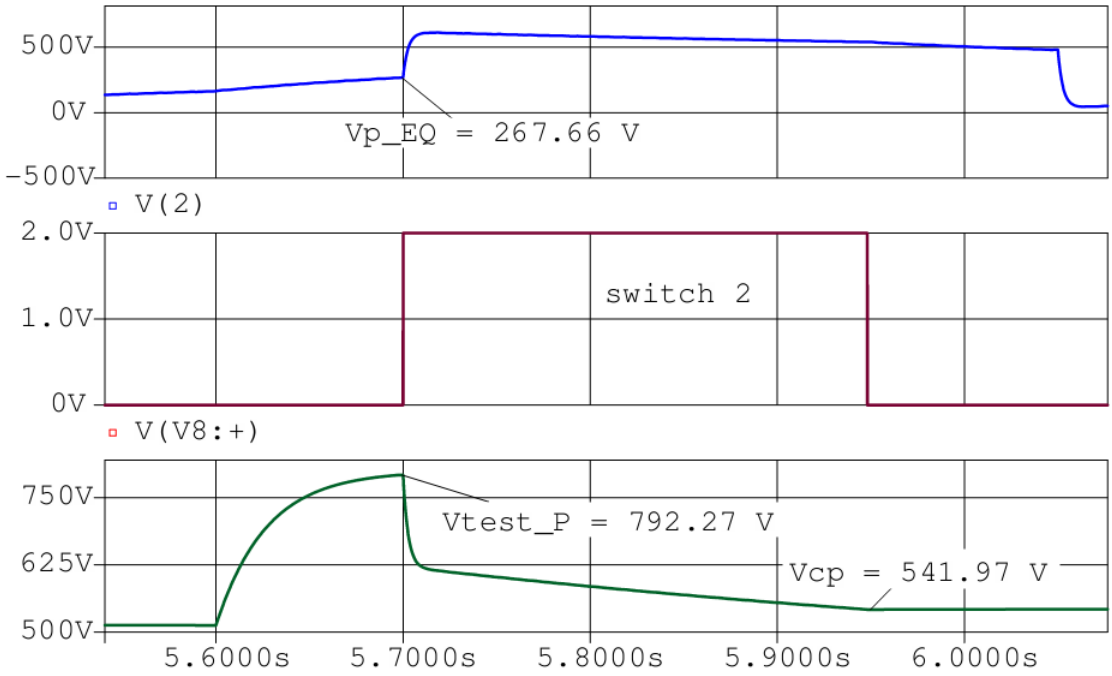

Figure 43: Simulation results for test case 2 of method 3

By substituting the measured values into the equation for R_{GND_EQ}, we obtain 460kΩ. The actual resistance to ground is fairly higher than 460kΩ (i.e. ~1.75MΩ), but due to the presence of Y-caps in the DC-DC converter and Auxiliary load there is additional energy drawn from C_P to charge the Y-caps that were originally at V_{P_EQ} = 267.66V. This condition is representative of test case 5 of section 4.2.2, and could potentially reduce the reliability of this GFDS. Since the diagnostic algorithm does not consider Y-capacitance, a drop in voltage V_{CP} due to this capacitance is interpreted as reduced isolation between HV power net and chassis ground.

TEST CASE 3

This test case is to evaluate the response of the circuit in a true fault condition. The conditions and constraints of this test case are similar to those in Test Case 3 of section 4.2.2. The results of the simulation are shown in Figure 44.

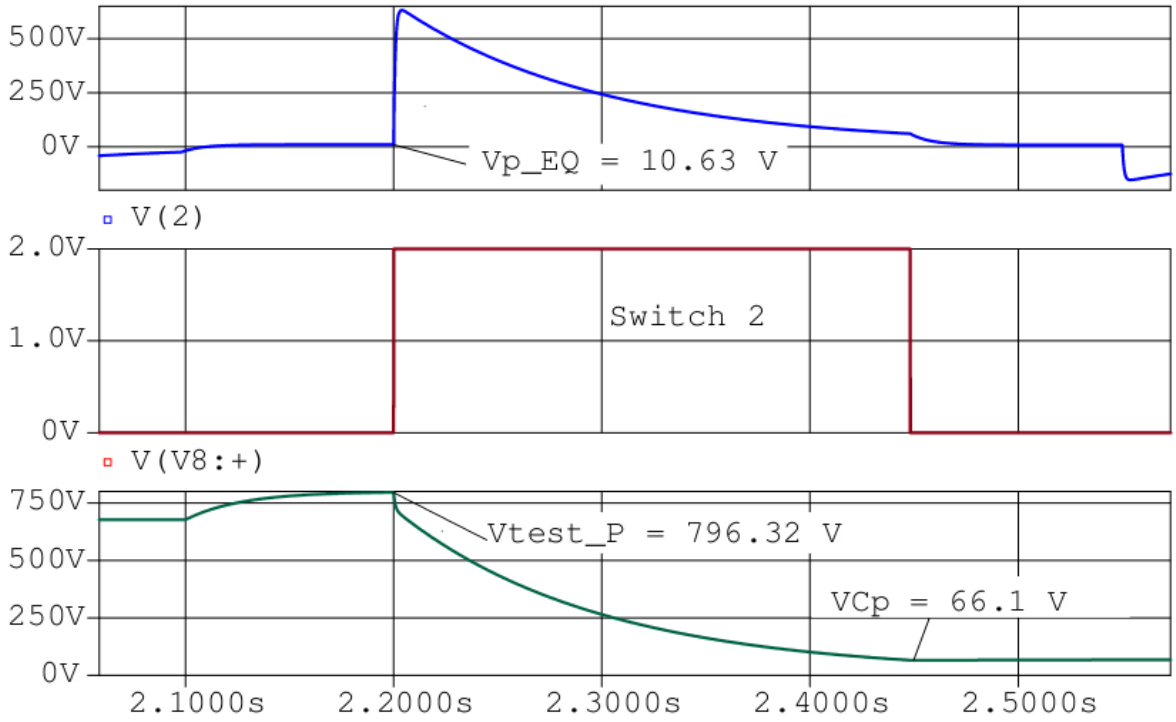

Figure 44: Simulation results for test case 3 of method 3

The depth of discharge of C_P is significant in this particular case, as expected. Also, V_{P_EQ} almost approaches 0V, which is indicative that there is a huge imbalance in the common mode impedance and voltage on the HV power net. Using the measured values to calculate R_{GND_EQ} we obtain ~ 112.5kΩ, which is consistent with the true leakage condition in the system.

TEST CASE 4

The conditions and constraints of this test case are similar to those of test case 6 in section 4.2.2. The purpose of this simulation is to evaluate the response of the leak detection system to an AC ground fault of 1Ω (short circuit). The results are shown in Figure 45 below.

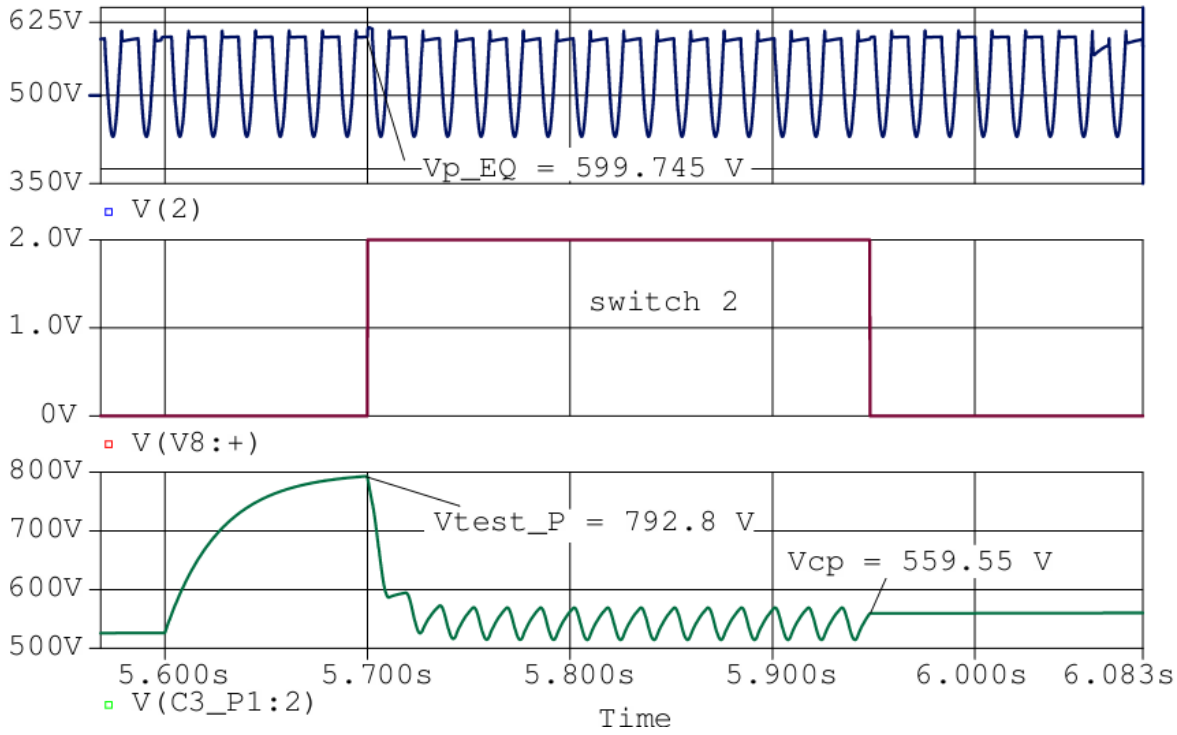

Figure 45: Simulation results for test case 4 of method 3

Due to the existence of a short circuit path between one of the AC output lines and chassis ground, there is a significant amount of AC voltage that is super imposed onto the common mode DC bus; as explained in section 4.2.2. This can be seen in the top graph of Figure 45. The superimposition of AC voltage onto the common mode DC bus results in measurement signals V_{CP} and V_{PEQ} being noisy and hence reduce fidelity in the measured data. The reliability of the diagnostic circuit is therefore significantly minimized in AC fault conditions.

A good example of this can be seen in the simulation above, where substitution of the measured values into the equation for R_{GND_EQ} will result in a non-real value, due to V_{P_EQ} being higher than V_{CP}.

TEST CASE 5

The conditions and constraints of this test case are similar to those of test case 7 in section 4.2.2. The purpose of this simulation is to evaluate the impact of voltage swings in the DC bus on the current waveforms I_1 and I_2. The results are shown in Figure 46 below.

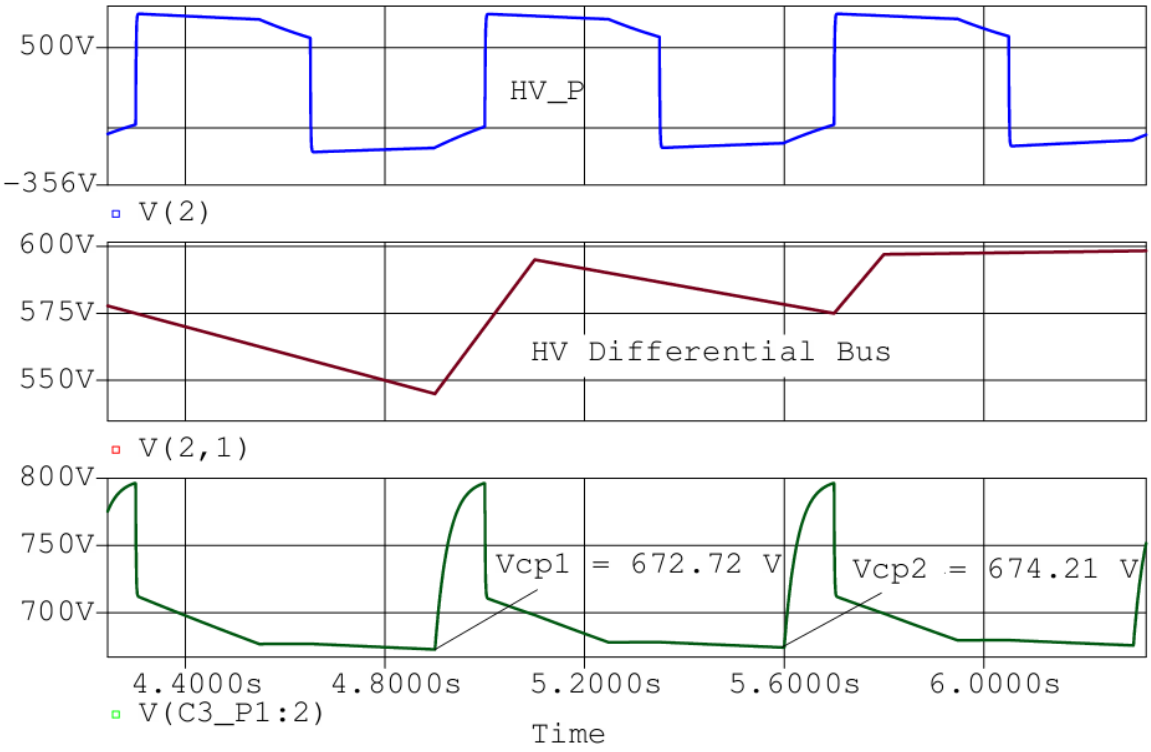

Figure 46: Simulation results for test case 5 of method 3

Variation in the differential bus voltage does not significantly impact the common mode bus voltages, as evidenced by the graphs shown in Figure 46. A 30V swing in the high voltage bus (from t = 5 to t = 5.6) causes a negligible change in V_{CP} (< 2V).

In summary, the GFDS discussed in this section performs the intended function in systems that have fixed components whose ideal common mode impedance is known. Further, distinction between a discharge caused by resistive elements vs. capacitive

elements is not possible, hence skewing the data used for diagnostics and affecting the reliability of fault detection.

Introducing a high voltage power supply on the common mode bus that has an output voltage higher than V_{BATT} may be detrimental to Y-caps within peripheral devices connected to the HV bus (as described in section 3.3). Finally, the low frequency high voltage waveform imposed on the common mode bus may also interfere with or affect circuitry in peripheral devices that are connected to the HV bus. This waveform is shown in Figure 47 below.

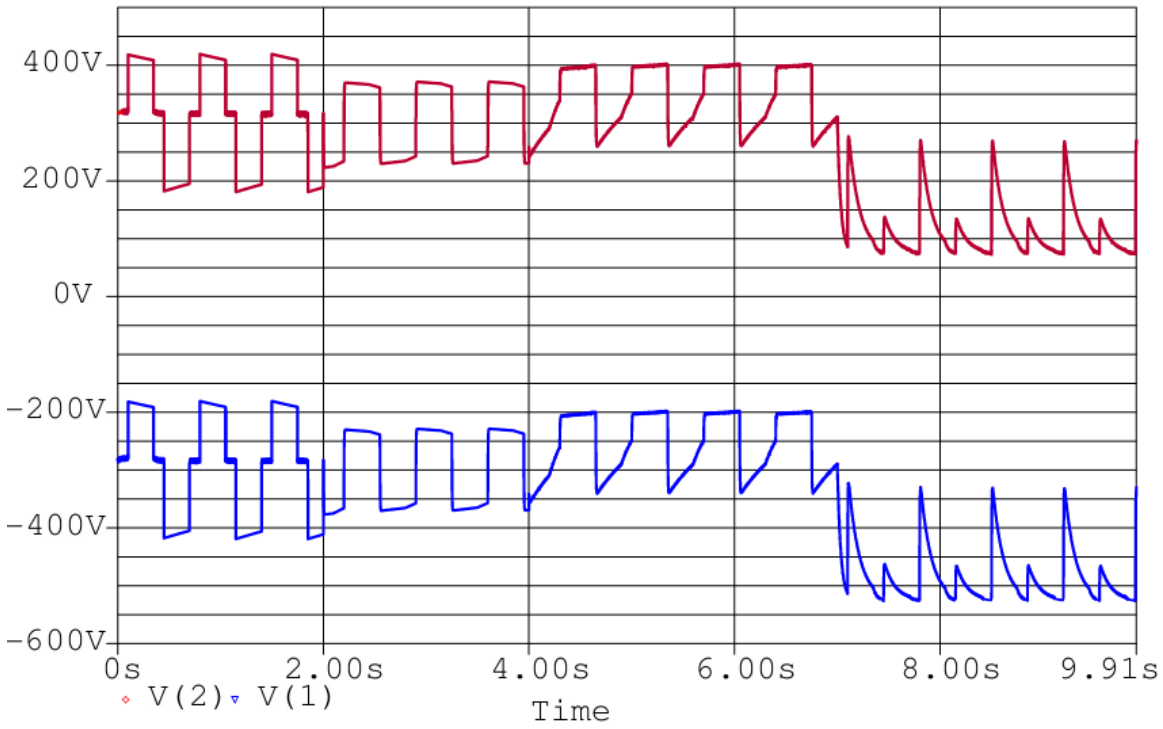

Figure 47: Common mode bus voltage as a result of method 3

4.5 Caterpillar Inc – Systems and Methods for Electrical Leakage Detection

4.5.1 Technology Overview

Inventors Robert Wayne Lindsey and Jennifer Leah Lindsey from Caterpillar Inc, Peoria, IL improved upon a popular impedance measurement technique referred to as the Wheatstone bridge, which although is effective in determining low impedances to ground in the HV power system, becomes unreliable in the case of a balanced leak fault [20]. The relevance of this invention may be understood by briefly examining the principle behind the Wheatstone bridge, and its limitations. Masaki Yogou from Sanyo Electric Co., Japan illustrates the implementation of the Wheatstone bridge principle to detect electrical leakage in a power supply as shown in Figure 48 [21].

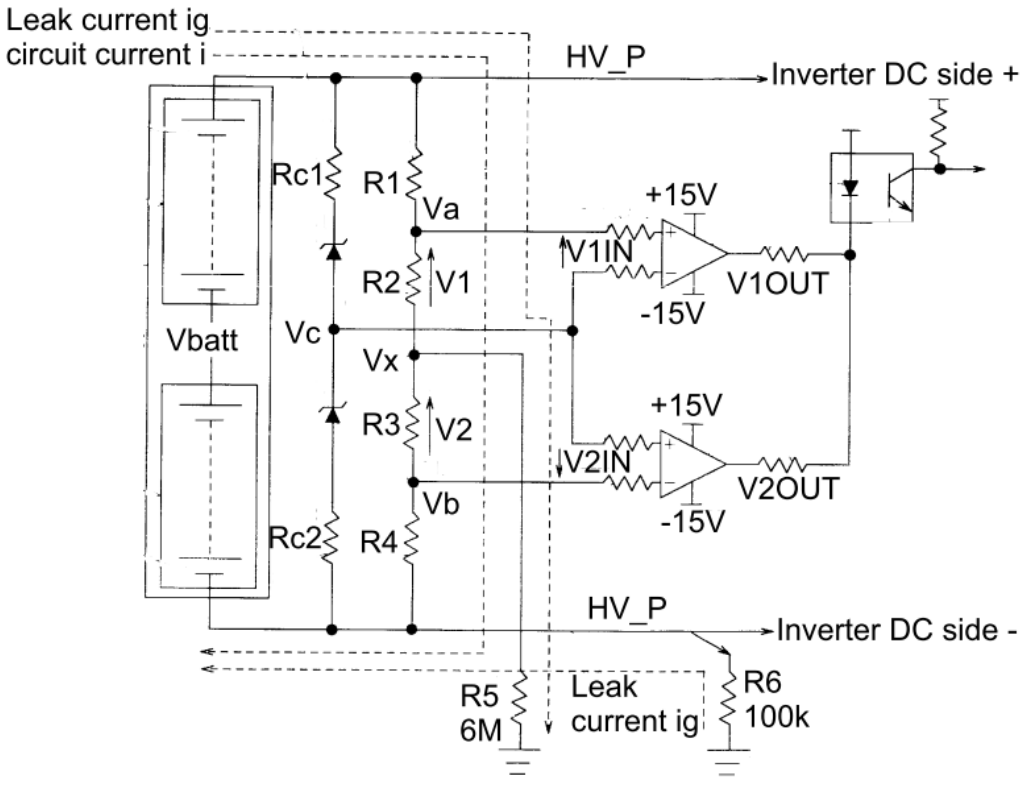

Figure 48: schematic overview of typical Wheatstone bridge method [21]

In the figure, a High Voltage battery is connected to an inverter across the positive and negative terminals. A separate GFDC unit comprising R_{C1}, R_{C2}, R_1, R_2, R_3, R_4, R_5, two op-amps, and an LED is also connected to the HV bus. R_{C1} and R_{C2} are voltage dividing resistors of equal magnitude that are connected to a common reference V_C. R_1 and R_4 are protection resistors of high value (e.g. 1MΩ), which are connected in series to R_2 and R_3 respectively. R_2 and R_3 are detection resistors of lower value (22kΩ) that are connected to chassis ground through an isolation resistor R_5 (e.g. 6MΩ). Resistors R_4 and R_3, and R_1 and R_2 have common references V_B and V_A respectively. By measuring Voltages V_{1IN} (i.e. $V_A - V_C$) and V_{2IN} (i.e. $V_B - V_C$), and comparing the measurements to a threshold voltage V_{TH}, a ground fault may be diagnosed.

Under ideal conditions, the isolation between HV_P or HV_N and chassis ground (i.e. R_6) is significantly high (multiples of MΩ - e.g. 10MΩ). In this case, the currents i and i_G (as shown in Figure 49) may be calculated as follows:

$$V_X = V_{BATT}\left(\frac{\frac{(R_3+R_4)(R_5+R_6)}{R_3+R_4+R_5+R_6}}{\left(R_1+R_2+\frac{(R_3+R_4)(R_5+R_6)}{R_3+R_4+R_5+R_6}\right)}\right)$$

Where

$$R_1 = R_4 = 1M\Omega$$

$$R_2 = R_3 = 22k\Omega$$

$$R_5 = 6M\Omega$$

$$R_6 = 10M\Omega$$

Therefore, $V_X = 290.72\ V$

$$\mathrm{V_C} = \mathrm{V_{BATT}}\left(\frac{\mathrm{R_{C2}}}{\mathrm{R_{C1}} + \mathrm{R_{C2}}}\right) = 600\left(\frac{56\mathrm{k\Omega}}{56\mathrm{k\Omega} + 56\mathrm{k\Omega}}\right) = 300\mathrm{V}$$

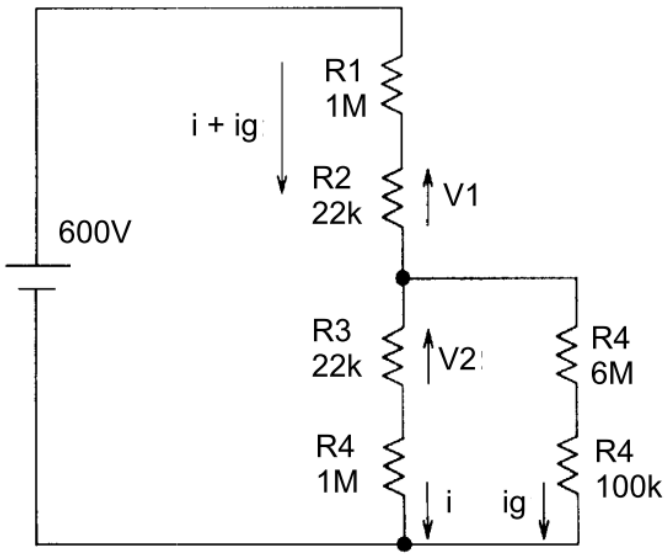

Figure 49: Partial equivalent circuit of Wheatstone bridge [21]

Now,

$$i = \frac{V_X}{R_3 + R_4} = 290.14\mu A$$

$$i_G = \frac{V_X}{R_5 + R_6} = 18.17\mu A$$

Hence,

$$V_1 = (i + i_G) \cdot R_2 = 6.78V$$

$$V_2 = i \cdot R_3 = 6.38V$$

$$V_{1IN} = V_A - V_C = (V_X + V_1) - V_C = 290.72 + 6.78 - 300 = -2.5V$$

$$V_{2IN} = V_B - V_C = (V_X - V_2) - V_C = 290.72 - 6.38 - 300 = -15.66V$$

Similarly, In the case of a true leak condition where $R_6 = 100k\Omega$, V_{1IN} is calculated to be -16.24V and V_{2IN} to be -29.16V. In the case where the fault occurs between HV_P and chassis ground, the same result as described above is obtained. Hence, the threshold for a ground fault may be selected as $V_{1IN} < -16V$ or $V_{2IN} > 16V$.

One challenge with using such a method for ground fault detection is that a compromise of isolation on BOTH the positive conductor to chassis and negative conductor to chassis can skew the values of V_{1IN} and V_{2IN} such that they will NOT trigger a fault. This is shown in section 4.5.2.

As mentioned earlier, the method developed by Robert and Jennifer Lindsey operates on similar principles, but is modified to allow detection of balanced leak faults.

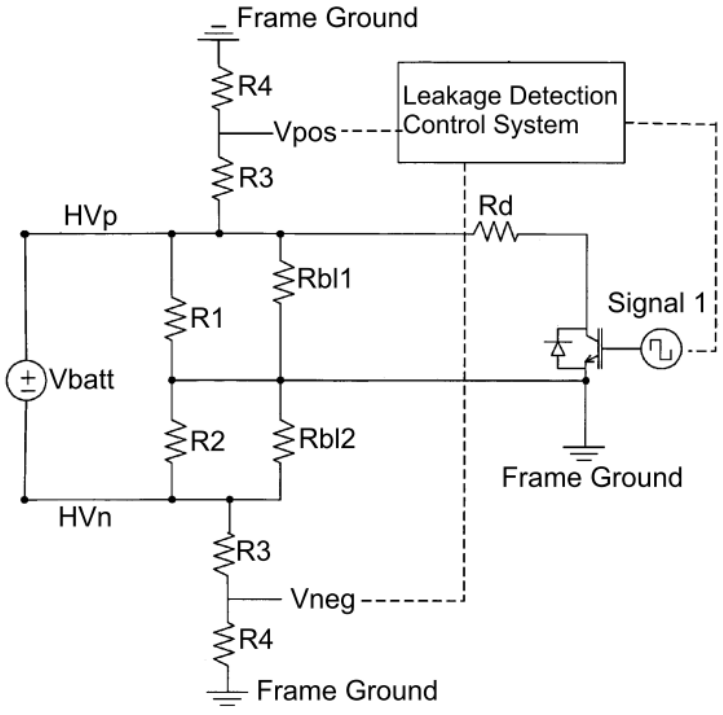

Figure 50: Schematic overview of method 4 [20]

Figure 50 shows the architecture of the GFDC [20]. In the figure, R_1 and R_2 are two resistors of equal resistance providing means to balance and reference the high voltage buses HV_P and HV_N equally to chassis (or frame) ground (synonymous to R_{C1} and R_{C2} described earlier in the section). R_3 and R_4 form a voltage divider that is used to measure V_{POS} and V_{NEG} in reference to chassis ground. The inherent leakage resistance between HV+ and chassis, and HV– and chassis is shown as R_{BL1} and R_{BL2} respectively. When R_{BL1} and R_{BL2} are equal in magnitude, the system is considered to be in a balanced condition. Conversely, when R_{BL1} does not equal R_{BL2}, the system is considered to be in an unbalanced condition, and the voltage across HV_P and ground does not equal the voltage across HV_N and ground. Therefore, the Imbalance of the system may be defined by the following equations:

$$V_{BATT} = HV_P - HV_N$$

$$Imbalance = 1 - \left(\frac{HV_N}{\frac{V_{BATT}}{2}} \right)$$

Since V_{POS} and V_{NEG} refer to the voltage measurements across resistors R_4, and can be represented in terms of HV_P and HV_N, the expression for voltage imbalance may be rewritten as:

$$HV_P = V_{POS} \cdot \frac{R_3 + R_4}{R_4}$$

$$HV_N = V_{NEG} \cdot \frac{R_3 + R_4}{R_4}$$

Therefore,

$$Imbalance = 1 - \left| \frac{\frac{V_{NEG}}{V_{POS} - V_{NEG}}}{2} \right|$$

For unbalanced fault conditions, the measured values of V_{POS} and V_{NEG} may be used to calculate the degree of imbalance, and subsequently the magnitude of leakage resistance. Assuming a ground fault between high voltage positive and chassis ground (i.e. R_{BL1} is a low value), V_{POS} and V_{NEG} maybe used to calculate R_{BL1}.

$$V_{POS} = (V_{POS} - V_{NEG}) \cdot \left(\frac{R_{EQ\_P}}{R_{EQ\_P} + R_{EQ\_N}} \right)$$

Where

$$R_P = \frac{R_1 \cdot (R_3 + R_4)}{R_1 + R_3 + R_4}$$

$$R_{EQ\_P} = \frac{R_{BL1} \cdot R_P}{R_{BL1} + R_P}$$

Now, assuming R_{BL2} is very high (e.g. 10MΩ)

$$R_{EQ\_N} = \frac{R_{BL2} \cdot R_P}{R_{BL2} + R_P} \approx R_P$$

Therefore,

$$R_{BL1} = -R_P \cdot \left(\frac{V_{POS}}{V_{POS} + V_{NEG}} \right)$$

However, in a balanced fault condition, V_{POS} and V_{NEG} may show that the circuit is balanced and the true leakage resistance may not be accurately calculated. In order to detect the leakage resistance in a balanced fault condition, leakage detection resistor R_D may be switched into the circuit, as shown in Figure 50. For this purpose, any transistor switch may be used, controlled by a signal issued by the microcontroller. When the switch is ON, resistor R_D provides an additional current path from HV_P to chassis ground, thus changing the equivalent resistance R_{EQ_P} between high voltage positive rail and chassis, and subsequently generate an offset voltage to unbalance the system.

$$R_{EQ\_Pnew} = \frac{R_{EQ\_P} \cdot R_D}{R_{EQ\_P} + R_D}$$

Furthermore, the resistance of the parallel configuration of R_2, $(R_3 + R_4)$, and R_{BL2} (i.e. R_{EQ_Nnew}) also equals that of R_{EQ_Pnew} because R_{BL1} equals to R_{BL2}, and R_1 equals R_2. Therefore, when R_D is switched into the system, the voltage distribution across HV_P and ground, and HV_N and ground can be expressed as follows:

$$R_{EQ\_Pnew} = R_{EQ\_Nnew} = R_{EQ\_new}$$

$$R_{EQ\_P} = R_{EQ\_N} = R_{EQ}$$

$$\frac{V_{POS}}{V_{NEG}} = \frac{R_{EQ\_new}}{R_{EQ}}$$

Hence,

$$R_{EQ} = R_D \cdot \left| \frac{V_{NEG} - V_{POS}}{V_{POS}} \right|$$

In this manner, by switching R_D into the system, R_{EQ} may be calculated followed by R_{BL1} and R_{BL2}.

4.5.2 Simulation and Analysis

Although the mechanism used to calculate the leakage resistance in a balanced fault condition is a unique modification to the original method, it uses the same Wheatstone bridge principle. Hence, for simplicity of analysis, only the original method discussed for detecting ground faults in an unbalanced condition will be simulated to verify reliable operation under various test cases. This is also done in order to be consistent with the test conditions used for analysis of other design methodologies. Figure 51 below shows the circuit model used for simulation.

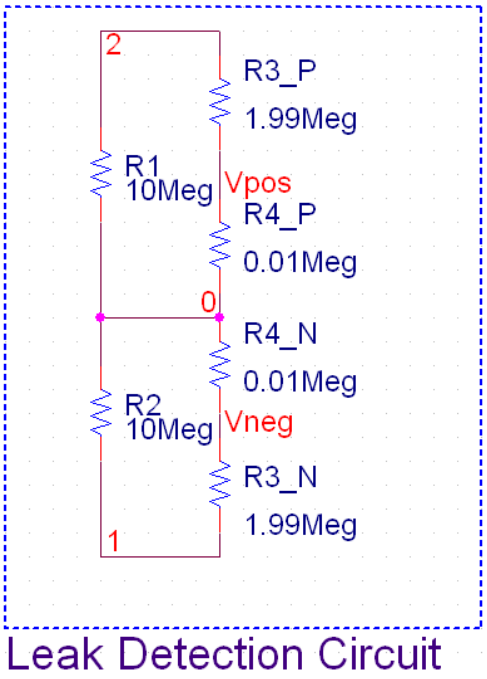

Figure 51: Leak detection circuit model for method 4

As mentioned, the resistor R_D and the transistor switch have not been modeled. In addition, although the invention disclosure uses a value of 8kΩ for the voltage divider resistors R_1 and R_2, 10MΩ has been used for the simulation to in order to maintain large isolation between the high voltage rails and chassis. The detection resistors R_{4_P} and R_{4_N} are 10kΩ each in order to reduce the measured common mode voltage by a factor of 200 so that it may be used as a voltage input for a microcontroller channel that is limited to 5V.

TEST CASE 1

This test case is designed to evaluate the response of the ground fault detection system in an ideal, no fault state. The conditions and constraints for the test are the same as in section 4.2.2. The results are plotted in Figure 52.

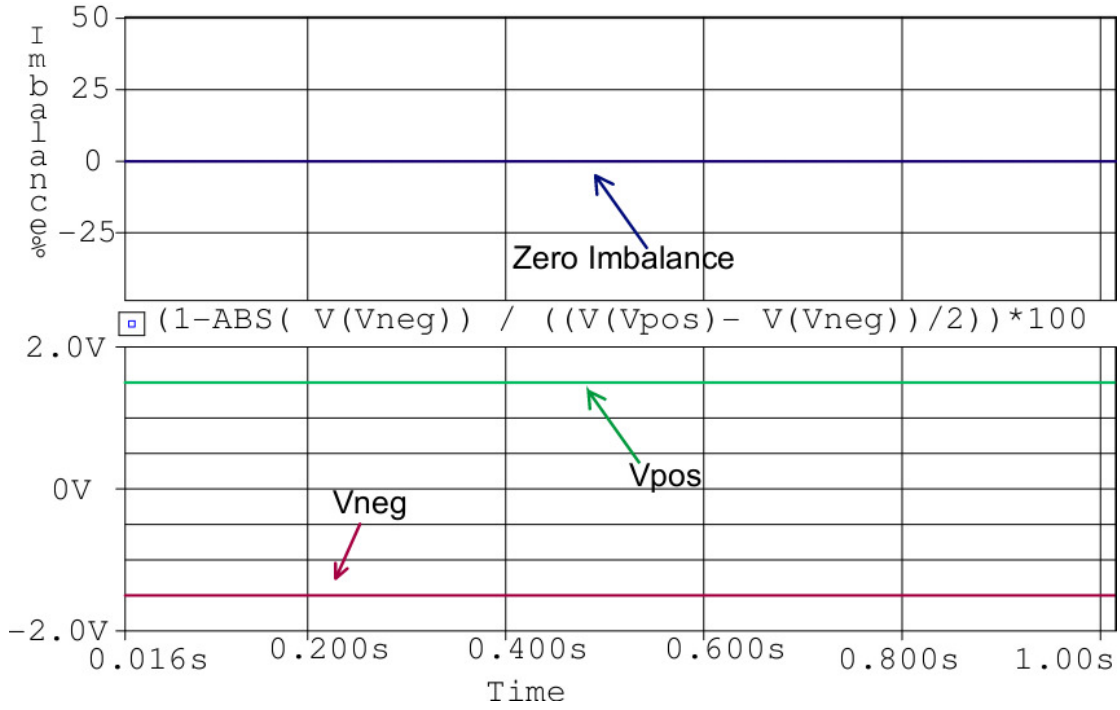

Figure 52: Simulation results for test case 1 of method 4

As expected for a no-fault balanced system, the following measurements were realized:

$$V_{POS} = V_{BATT} \cdot \left(\frac{R_{EQ\_P}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

$$V_{NEG} = -V_{BATT} \cdot \left(\frac{R_{EQ\_N}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

$$R_{EQ\_P} = R_{EQ\_N}$$

$$V_{POS} = -V_{NEG} = 600 \cdot \left(\frac{1}{2}\right) \cdot \left(\frac{0.01 \cdot 10^6}{1.99 \cdot 10^6}\right) = 1.5V$$

$$\%\ Imbalance\ =\ 1 - \left| \frac{\frac{V_{NEG}}{V_{POS} - V_{NEG}}}{2} \right| \cdot 100$$

$$\%\ Imbalance\ =\ 1 - \left| \frac{\frac{-1.5}{1.5 - (-1.5)}}{2} \right| \cdot 100 \approx 0\%$$

In this case, since the imbalance in the circuit is zero, R_D could be switched into the circuit to test for the leakage resistance in the common mode bus and verify that the isolation is indeed high.

TEST CASE 2

The second test case is to evaluate the response of the circuit when a non-isolated single phase inverter is connected to the HV battery. The conditions and constraints are similar to those described in section 4.2.2. The added 120Hz ripple from the single phase

inverter has a negligible impact on the voltage waveforms V_{POS} and V_{NEG}, as shown in Figure 53.

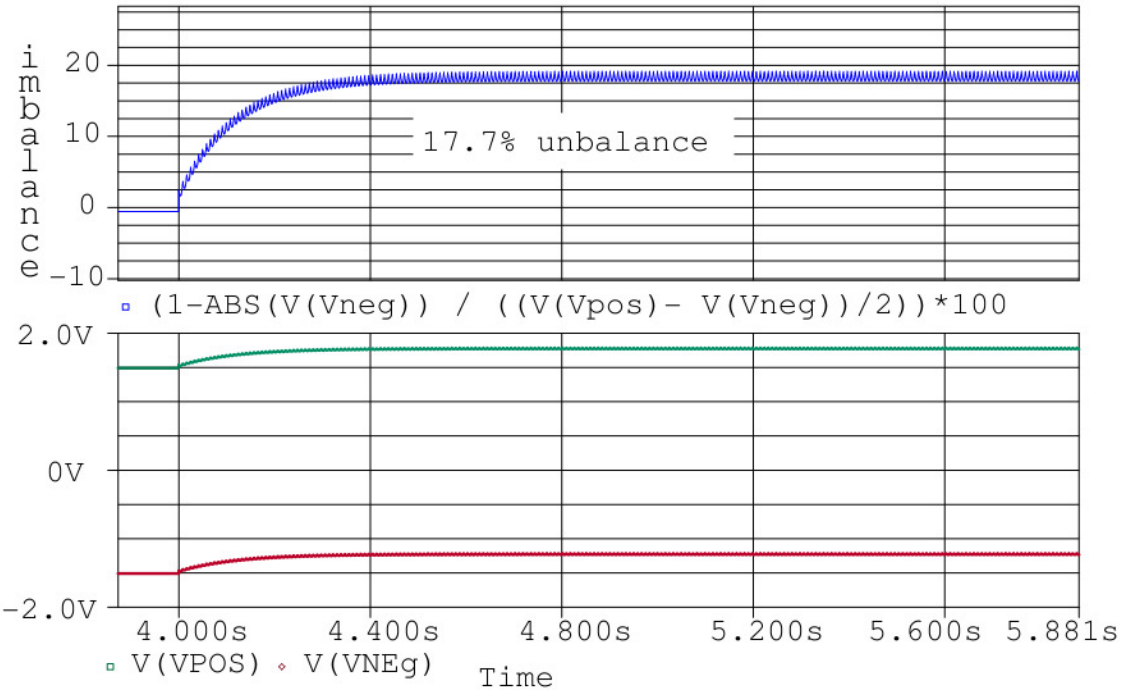

Figure 53: Simulation results for test case 2 of method 4

120Hz ripple is noticeable in the calculated waveform for system imbalance, but does not have any consequential impact on fault diagnostics. A positive imbalance of ~18% shows us that there is lower isolation resistance between HV_N and chassis. Since this imbalance is inherent to the setup of the circuit model for the single phase inverter, it is expected.

TEST CASE 3

This test case is to evaluate the response of the circuit in a true fault condition. The conditions and constraints of this test case are similar to those in Test Case 3 of section 4.2.2. The results of the simulation are shown in Figure 54.

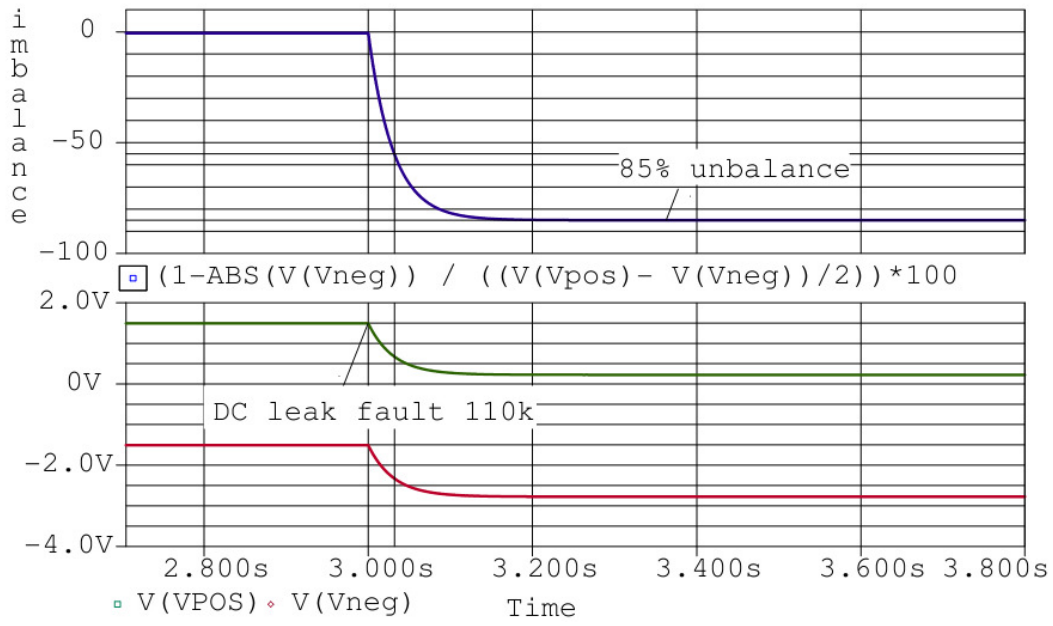

Figure 54: Simulation results for test case 3 of method 4

When the 110kΩ resistor is induced between high voltage positive and chassis at t = 3.0 s, both V_{POS} and V_{NEG} drop by 1.275 V. Hence, the imbalance in the network is 85%, and since 120kΩ is the threshold leakage resistance R_{TH} for the circuit, 80% (with a 5% margin) may be used as the imbalance threshold for detecting a ground fault (i.e. Imbalance > 80% will trigger a leak fault). However, this threshold is relevant only for a system with the conditions similar to those that were used for this simulation, i.e. only the traction inverter is connected to the HV bus and nothing else. If other known components were introduced to the system that would imbalance the system further, the threshold would need to change. This is discussed further in test case 7.

TEST CASE 4

This test case is synonymous to Test Case 5 in section 4.2.2, where the response of the leak detection circuit to added Y-capacitance on the common mode bus is evaluated. The results are shown in Figure 55.

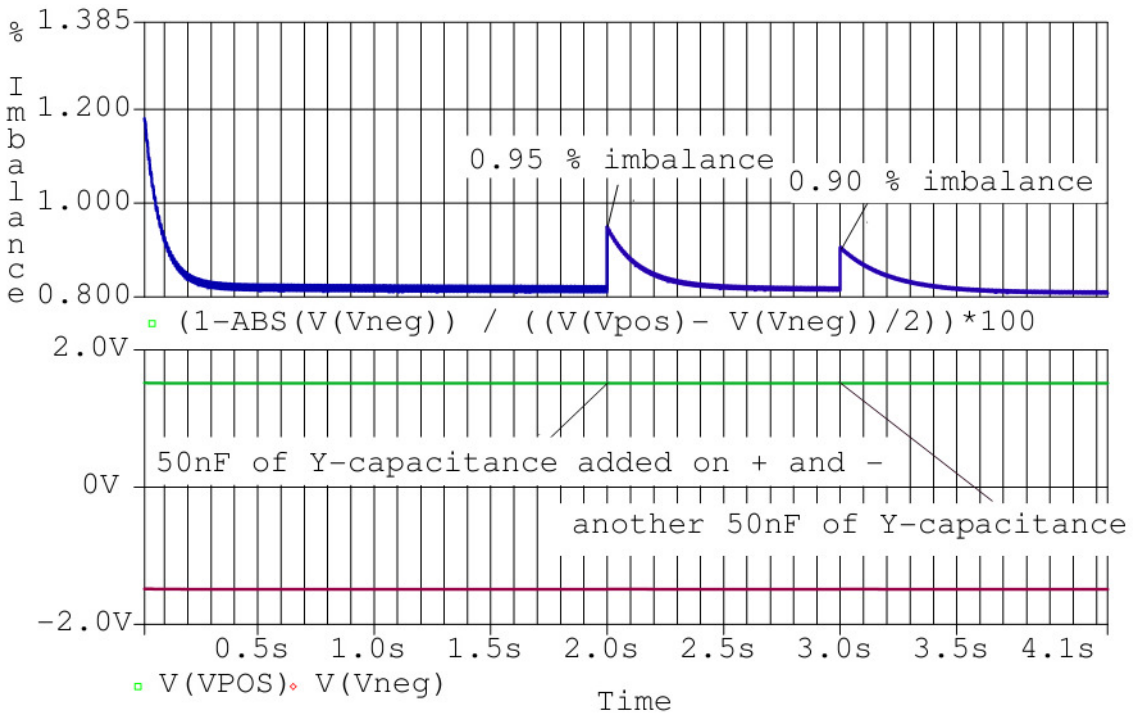

Figure 55: Simulation results for test case 4 of method 4

The addition of 50nF of capacitance to the common mode bus at time $t = 2.0\,sec$ when switches S7 and S8 are closed does not have a significant impact on the voltages V_{POS} and V_{NEG} since the overall common mode impedance only changes momentarily as the capacitors charge up. A similar response is observed again at $t = 3.0\,sec$ when an additional 50nF of capacitance is added to the common mode bus, before the system eventually reaches steady state at $t \approx 4\,sec$. The level of voltage imbalance and time taken for the voltage to stabilize is dependant on the magnitude of Y-capacitance in the system.

TEST CASE 5

The conditions and constraints of this test case are similar to those of test case 6 in section 4.2.2. The purpose of this simulation is to evaluate the response of the leak

detection system to an AC ground fault of 1Ω (short circuit). The results are shown in Figure 56 below.

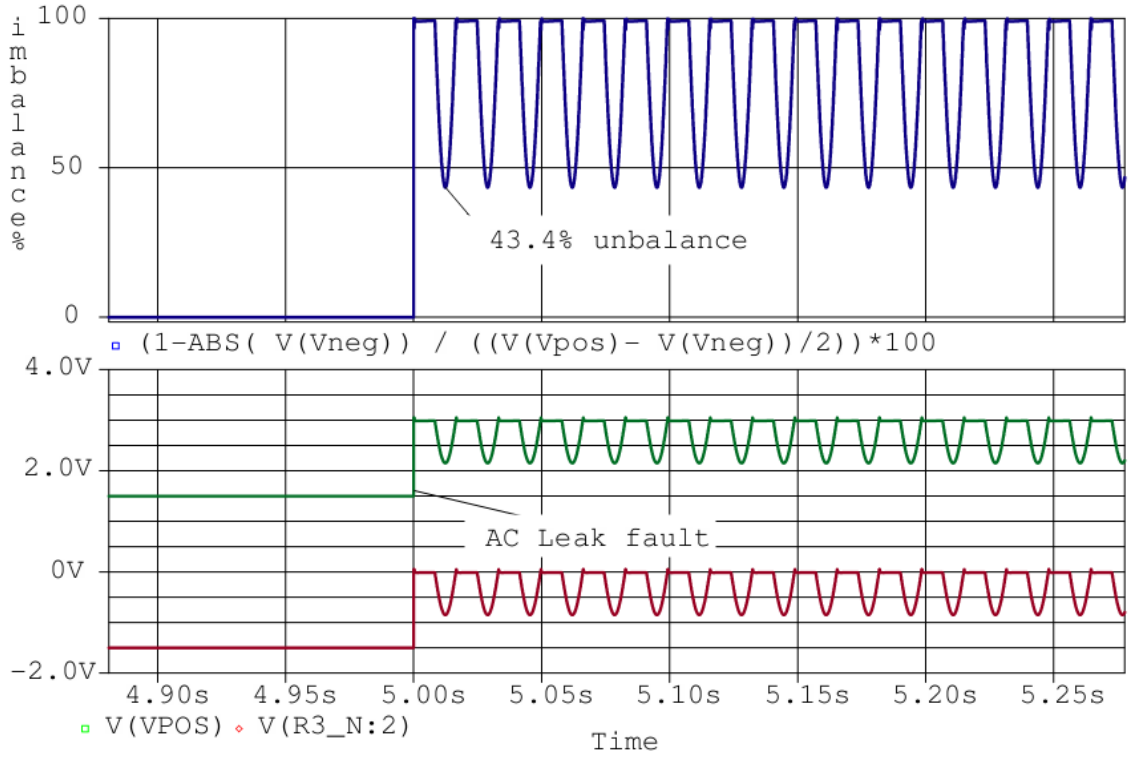

Figure 56: Simulation results for test case 5 of method 4

As described in section 4.2.2, an AC leak fault within the HEV system causes a large amplitude of ripple voltage to be superimposed on the DC side common mode bus, typically at a frequency that is two times the fundamental frequency of the output of a single phase inverter, and six times that of a three phase inverter (e.g. traction inverter). This causes the voltages V_{POS} and V_{NEG} to oscillate at the same frequency, as illustrated in the bottom graph of Figure 56. Consequently, the imbalance of the system also varies at the same frequency. Depending on the sampling frequency of the voltage monitoring device in the GFDS, certain algorithms may be implemented to identify an AC leak fault in the system.

TEST CASE 6

The conditions and constraints of this test case are similar to those of test case 7 in section 4.2.2. The purpose of this simulation is to evaluate the impact of voltage swings in the DC bus on the voltage waveforms V_{POS} and V_{NEG}. The results are shown in Figure 57 below.

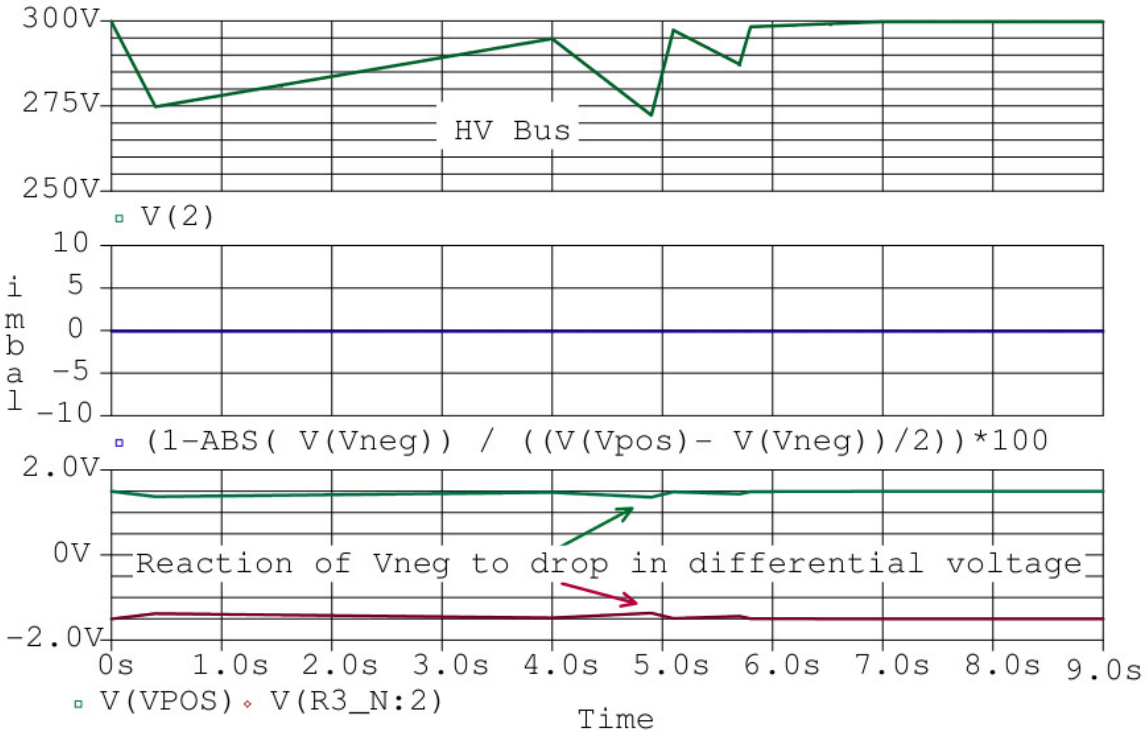

Figure 57: Simulation results for test case 6 of method 4

Although variations in the differential voltage of the HV bus will impact the voltages V_{POS} and V_{NEG}, the percentage of voltage imbalance will not change because both positive and negative common mode voltages will increase or decrease by the same factor. This may be explained mathematically as follows:

Recall that V_{POS} and V_{NEG} are defined as:

$$V_{POS} = V_{BATT} \cdot \left(\frac{R_{EQ\_P}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

$$V_{NEG} = -V_{BATT} \cdot \left(\frac{R_{EQ\_N}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

Then, the change in these voltages i.e. ΔV_{POS} and ΔV_{NEG} is given by:

$$\Delta V_{POS} = \Delta V_{BATT} \cdot \left(\frac{R_{EQ\_P}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

$$\Delta V_{NEG} = -\Delta V_{BATT} \cdot \left(\frac{R_{EQ\_N}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)$$

Therefore, assuming that the resistances of the circuit do not change,

$$\frac{\Delta V_{POS}}{\Delta V_{NEG}} = \frac{V_{POS}}{V_{NEG}} = -\frac{\left(\frac{R_{EQ\_P}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)}{\left(\frac{R_{EQ\_N}}{R_{EQ\_P} + R_{EQ\_N}} \cdot \frac{R_4}{R_4 + R_3} \right)}$$

For a balanced circuit,

$$\frac{\Delta V_{POS}}{\Delta V_{NEG}} = \frac{V_{POS}}{V_{NEG}} = -1$$

Hence, $\Delta V_{POS} = \Delta V_{NEG}$.

TEST CASE 7

A unique test case was developed for this particular GFDS to evaluate its effectiveness in detecting a fault in a "partially unbalanced" system. Two distinct fault conditions (balanced and unbalanced) were discussed and methods to detect leakage

resistance under these conditions were proposed. However, a required condition for effectively calculating R_{BL1} or R_{BL2} in an unbalanced fault state was that at least one of these parameters is known (i.e. no isolation breakdown between positive or negative rail and chassis).

Revisiting test case 3, if a 120kΩ fault was introduced between HV_P and chassis ground at t = 3 sec, an imbalance of 85% would occur, and a leak fault would be triggered. If a similar fault was introduced between HV_N and chassis ground at t = 5 sec, a balanced fault condition would exist, and R_D could be switched into the circuit to determine R_{EQ} and eventually R_{BL1} (=R_{BL2}).

Instead, if the equivalent resistance between HV_N and chassis was partially reduced to $R_{EQN} = 1M\Omega$ at t = 5 sec, an unbalanced fault condition would continue to exist but the percentage imbalance would be different. Such an occurrence could be caused by, for example, connecting an additional component to the flexible HEV bus that has reduced isolation to ground. A simulation of this case is shown in Figure 58 on Page 93.

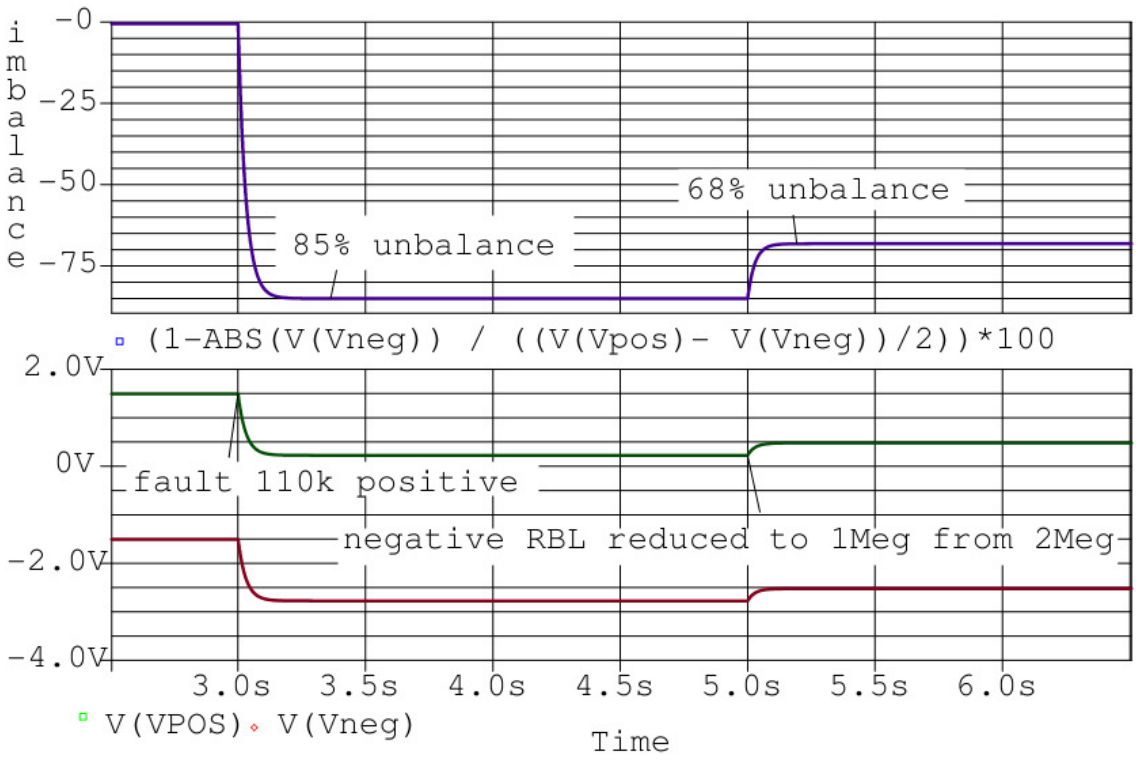

Figure 58: Simulation results for test case 7 of method 4

By reducing R_{EQ_N} from 2MΩ to 1MΩ, the percentage imbalance in the circuit decreased from 85% to 68%, in spite of the leakage resistance between HV_P and chassis being only 120kΩ. In this case, a leak fault would not be set, rendering both methods only partially effective in detecting ground faults.

In summary, the GFDS discussed in this section is pretty robust in detecting unbalanced and balanced leak faults; where an unbalanced leak fault is defined as isolation breakdown between either positive rail and chassis, or negative rail and chassis, but not both. However, this GFDS is not capable of accurately detecting low isolation in the case of a partially unbalanced fault, as described in test case 7. Also, it has been shown that ripple voltage or noise on the common mode bus can skew measurements of V_{POS} and V_{NEG}. Finally, although it is important to keep the value of R_D low (e.g.

10kΩ) in order to accurately detect low isolation resistance in a balanced fault condition, this component creates an additional leakage path to chassis by significantly reducing the common mode equivalent impedance in the system during the transistor switch ON period.

One recommendation for improving the GFDS would be to add switches SW1 and SW2 between R_{3_P} and R_{4_P}, and R_{3_N} and R_{4_N} respectively. Similar to the GFDS analyzed in section 4.3, switches SW1 and SW2 would be controlled independently and switched at alternate times so that both switches are never ON at the same time. One embodiment of this is shown in Figure 59 below.

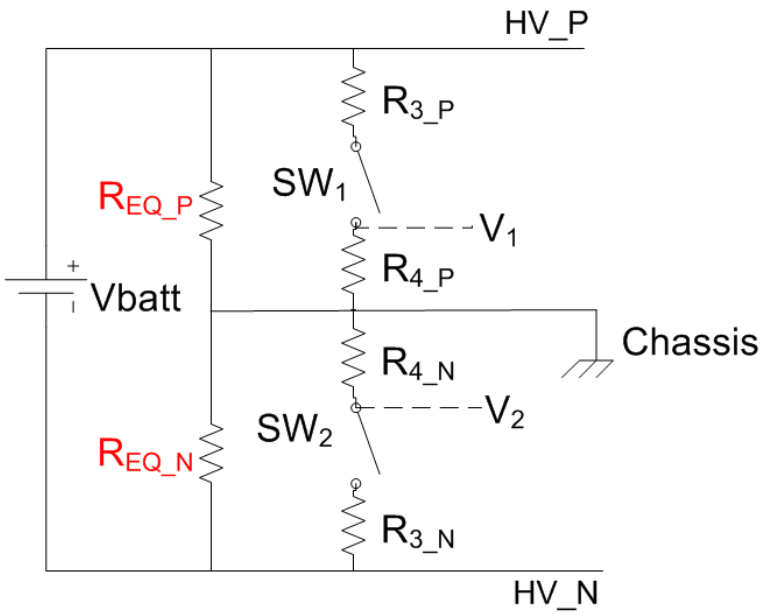

Figure 59: Circuit improvement for method 4

R_{EQ_P} and R_{EQ_N} are the equivalent resistances between high voltage positive or negative with respect to ground, and HV_P and HV_N represent high voltage positive and negative bus voltages respectively. Also, balancing resistors R_1 and R_2 may be

eliminated since they do not contribute to the calculation of R_{EQ_P} and R_{EQ_N} as described below.

Assuming $R_{3\_P} = R_{3\_N} = R_3 = 1.99M\Omega$, and $R_{4\_P} = R_{4\_N} = R_4 = 0.01M\Omega$, when SW1 is first turned ON,

$$V_1 = HV_P \cdot \left(\frac{R_4}{R_3 + R_4}\right)$$

$$HV_P = V_{BATT} \cdot \frac{\frac{R_{EQ\_P} \cdot (R_3 + R_4)}{R_{EQ\_P} + R_3 + R_4}}{R_{EQ\_N} + \left(\frac{R_{EQ\_P} \cdot (R_3 + R_4)}{R_{EQ\_P} + R_3 + R_4}\right)}$$

Therefore,

$$V_1 = \frac{V_{BATT} \cdot R_4 \cdot R_{EQ\_P}}{R_{EQ\_P} \cdot R_{EQ\_N} + (R_3 + R_4) \cdot R_{EQ\_P} + (R_3 + R_4) \cdot R_{EQ\_N}}$$

Similarly, when SW1 is OFF and SW2 is ON,

$$V_2 = HV_N \cdot \left(\frac{R_4}{R_3 + R_4}\right)$$

$$HV_N = V_{BATT} \cdot \frac{\frac{R_{EQ\_N} \cdot (R_3 + R_4)}{R_{EQ\_N} + R_3 + R_4}}{R_{EQ\_P} + \left(\frac{R_{EQ\_N} \cdot (R_3 + R_4)}{R_{EQ\_N} + R_3 + R_4}\right)}$$

$$V_2 = \frac{V_{BATT} \cdot R_4 \cdot R_{EQ\_N}}{R_{EQ\_P} \cdot R_{EQ\_N} + (R_3 + R_4) \cdot R_{EQ\_P} + (R_3 + R_4) \cdot R_{EQ\_N}}$$

Now, solving the expressions for V_1 and V_2 for R_{EQ_P}, we get

$$R_{EQ\_P} = -\frac{(R_3 + R_4) \cdot R_{EQ\_N} \cdot V_1}{R_3 \cdot V_1 + R_4 \cdot (V_1 - V_{BATT}) + R_{EQ\_N} \cdot V_1}$$

And,

$$R_{EQ\_P} = -\frac{\left(R_3 \cdot V_2 + R_4 \cdot (V_2 - V_{BATT})\right) \cdot R_{EQ\_N}}{\left(R_3 + R_4 + R_{EQ\_N}\right) \cdot V_2}$$

Finally, equating these two expressions for R_{EQ_P}, and solving for R_{EQ_N}, we get

$$R_{EQ\_N} = -\frac{\left(R_3 \cdot (V_1 + V_2) + R_4 \cdot (V_1 + V_2 - V_{BATT})\right)}{V_1}$$

This process may be repeated for R_{EQ_P} to arrive at

$$R_{EQ\_P} = -\frac{\left(R_3 \cdot (V_1 + V_2) + R_4 \cdot (V_1 + V_2 - V_{BATT})\right)}{V_2}$$

The performance of this modified GFDS would be very similar to that of section 4.3 due to similarity in the operation principle.

CHAPTER 5

5 Comparison of Technologies

Although a small selection of existing technologies have been reviewed, it is important to understand that there are many other variations of ground fault detection systems designed for a plethora of industries and applications. Ultimately, all ground fault detection systems are developed to identify the impedance between a high voltage conductor and ground, and this can fundamentally be achieved in a finite number of ways.

The four methods that were evaluated in chapter 4 had some fundamental differences in method of operation and thus were chosen to be reviewed. In order to benchmark these methodologies against an ideal GFDS, a popular engineering method known as Pugh analysis will be used that helps determine which potential solutions are better than others, based on pre-defined criteria. It is a scoring matrix used for concept selection, in which options are assigned scores relative to criteria. The best approach is selected based on the consolidated scores [22].

5.1 Criteria for Analysis and Weighting Factor

In order to proceed with the analysis, it is critical to identify important characteristics of a GFDS that is to be implemented in a Flexible Hybrid Power System. These characteristics may be used as criteria for comparison.

5.1.1 Detection time

The response time of a diagnostic circuit and its embedded software to a true ground fault condition is a critical parameter to be considered when designing the GFDS. UL specification 2231-2 states that a ground fault circuit interrupting device shall open a circuit in no more than $T = \left(20/I\right)^{1.43}$, where T is time in seconds, and I is the fault trip current in mA (e.g. 5mA) [10]. Keeping in mind that this specification written for electric charging systems in vehicles is very conservative, and that T = 7.25 sec is a requirement for AC faults (for which limits are more stringent), it is perhaps acceptable for trip times to be higher. Moreover, most standards such as UL 2231 are developed for Ground Fault Interrupters which are meant to be reactive, instead of Vehicle Ground fault Detection Systems which are meant to be proactive. As explained in section 3.2.2, loss of isolation between a high voltage conductor and chassis ground only creates a shock hazard, but does not cause a shock. We may still use T = 7.25 sec for defining various ratings that a GFDS can be classified under.

Table 2: Definition of ratings for criteria 1

Rating	Description
0	System cannot reliably diagnose a leak fault in less than 7.25 sec, and cannot be designed to perform continuous monitoring of the power system. This may be because of limitations inherent to the design, or incompatibility with the HEV power system
1	system can be designed to have a reliable detection time of less than 7.25 sec, but cannot perform continuous monitoring of the power system

2	system can perform continuous monitoring of the high voltage system for leak faults, but cannot be designed to establish a true fault within 7.25 sec of leakage occurrence
3	system can perform continuous monitoring of isolation faults and diagnose a leak fault within 7.25 sec of occurrence

The weighting factor for this criterion may arbitrarily be selected as 4 (from a scale of 1 to 5), since fast detection time is critical to rapid mitigation of the negative effects of leak faults as described in chapter 3.

5.1.2 Type of Fault

Although the GFDS is connected to the HVDC bus, it is expected to diagnose leak faults that may exist anywhere in the power system, including those between AC lines (that are not isolated from DC) and chassis ground. The weighting factor for this criterion may arbitrarily be selected as 2 (from a scale of 1 to 5), since additional GFDSs for AC leak faults may be implemented in the system if the GFDS being rated is not capable of detecting both AC and DC faults.

Table 3: Definition of ratings for criteria 2

Rating	Description
1	System can detect DC faults only
2	System can detect both DC and AC faults

5.1.3 Mode of Detection

A flexible HEV power system can have a very complex architecture depending on the nature of components connected to the HV bus. Hence, HV bus characteristics such as current, voltage, and impedance may be very dynamic, creating the need for a GFDS that can function reliably in all states of operation. These states include:

- HEV Off mode – The hybrid power system is powered down
- HEV Standby/ Stationary mode – The High Voltage system is live, but the vehicle is not in motion, and all power electronic loads are disconnected. This can also be considered electrical steady state.
- HEV ON/ drive mode – The HV system is live, and devices such as the traction inverter, DC-DC Converter, single phase inverter etc. are in conditioning power.

Hence, the ratings for this criterion may be defined as shown in Table 4. The weighting factor for this criterion may arbitrarily be selected as 4 (from a scale of 1 to 5), since it is critical that the system functions in all modes of operation of the HEV.

Table 4: Definition of ratings for criteria 3

Rating	Description
0	System can only perform diagnostics during the HEV OFF state
1	System can perform diagnostics when the high voltage system is live, but only in an electrically steady state when the HEV is stationary and no power electronic loads are being powered.
2	System can perform reliable diagnostics in any state of operation

5.1.4 Flexibility of Design

One of the most critical factors in developing a GFDS for a HEV with flexible architecture (as described in section 4.1) is the ability of the system to adapt to changes in the high voltage bus configuration, either intrinsically or through non-intrusive system calibration that can be performed without impacting the design life cycle of the HEV system or subsystem. Typically, if a GFDS requires a hardware design change in order to function effectively in a new high voltage bus configuration/ application, it would not be suitable for use in a flexible high voltage system. However, if all that was required was a software calibration or a patch downloadable to the hybrid system controller through a vehicle diagnostic tool, then adaptation becomes seamless. This will be discussed in detail in section 5.2.

The ratings for this criterion may therefore be defined as shown in Table 5. The weighting factor would be 5 (from a scale of 1 to 5) because of the significance of this feature in a flexible power system.

Table 5: Definition of ratings for criteria 4

Rating	Description
0	System requires a hardware change to be compatible with a high voltage bus configuration that varies from the original configuration it was designed for
2	System contains software that can be calibrated or modified to adapt to a new high voltage bus configuration

5.1.5 Susceptibility to common noise sources

System monitoring devices and controllers in a HEV system are constantly exposed to electromagnetic interference (EMI). Common mode conducted noise on the high voltage bus and ripple current produced by the mutual interaction of power converters with the battery can be of significant interference for voltage and current monitoring circuits [23]. The fundamental frequency of this common mode voltage may be as low as 60 Hz, but it can reach 120 kHz with considerable amplitudes as shown in Figure 60. Other sources of interference can be electronic devices or controllers resident on the common mode bus that employ current switching techniques to perform their function (such as secondary isolation monitoring circuits). The interference caused by noise sources in the HEV system could result in the GFDS not setting a leak fault when it actually exists (Type I error), or conversely setting a leak fault when it actually does not exist (Type II error). Both of these are undesired effects, for reasons described in section 3.1.

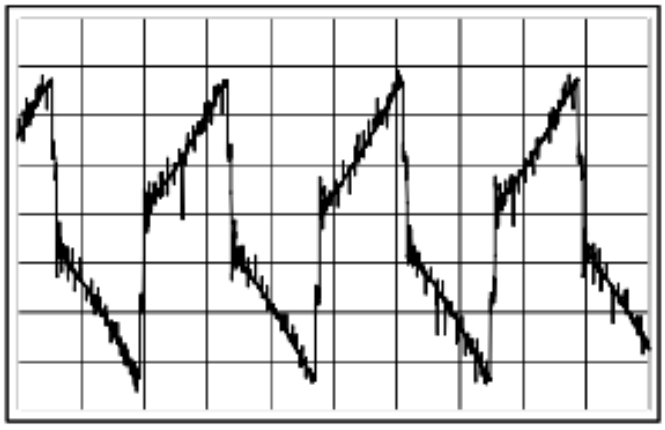

Figure 60: High frequency Common mode noise in PWM inverter (100V/div) [23]

Therefore, it is important to select a GFDS methodology that is fairly immune to conducted and radiated emissions in the hybrid system. At the same time, it is also

preferable that the GFDS does not become a source for conducted emissions that could interfere with the operation of other monitoring circuits in the system. Hence, the ratings for this criterion may be defined as shown in Table 6, and the weighting factor may arbitrarily be selected as 4 (from a scale of 1 to 5), since immunity to noise relates directly to the functionality of the GFDS.

Table 6: Definition of ratings for criteria 5

Rating	Description
0	System is susceptible to interference, resulting in a Type I error or Type II error or both
1	System is fairly immune to common mode noise, or is capable of identifying an input signal of low fidelity and reporting a fault. However, system can be a source for conducted emissions
1.5	System is fairly immune to common mode noise, or is capable of identifying a diagnostic input signal of low fidelity and reporting a fault. System does not generate noise.

5.1.6 Cost & Complexity

One observation that can be made about the systems evaluated in chapter 4 is that most of the systems require few components to functionally operate. A majority of the components being used are discrete resistors, capacitors, and switches. Almost all the systems include a processor or microcontroller that has intelligence to performance diagnostics based on inputs from digital sensors in the circuit. Some systems utilize additional power supplies in order to fundamentally perform leakage detection. With a

variety of architectures, an important criterion for consideration is the actual cost and overall reliability of the system.

In general, the cost and reliability of a system improves as the complexity and number of components within the system is reduced. Using GFDS 2 (the system described in section 4.3) as a benchmark, the ratings for this criterion may be defined as shown in Table 7. The weighting factor may be arbitrarily selected as 1 (from a scale of 1 to 5), since this criteria is not necessarily correlated to the functional robustness of the GFDS. NOTE: The rating selection for this criterion is highly simplified, and is arbitrary at best.

Table 7: Definition of ratings for criteria 6

Rating	Description
0	System design is more complex than GFDS 2
1	System design is similar in complexity to GFDS 2
2	System design is less complex than GFDS 2

5.2 System Benchmarking

The next step after defining criteria for analysis is to rate each system against this set of criteria.

CRITERIA 1: DETECTION TIME

Method 1: Nissan Motor Design

As mentioned in section 4.2, this GFDS was designed to perform continuous monitoring of the high voltage system for ground faults. Assuming a very low sampling

frequency of $f = 10\ Hz$ for the amplitude of V_{DET}, and conservatively using $N = 70$ as the number of consecutive counts of V_{DET} being below the leak threshold V_{TH} in order to trigger a leak fault, $T = \left({}^{1}/_{f}\right) \cdot N = 7\ sec$ the minimum time required for the system to reliably detect a leak fault. In this case, method 1 would receive a rating of 3.

Usually, 1 or 2 data points are not sufficient for an accurate diagnosis of the state of the system, because of potential noise in the signal that could skew data measurements. Although one exemplary implementation of the method was used to rate the system, it is not implied that the system cannot be optimized to perform leakage detection in a shorter period of time.

Method 2: Maxim Inc. Design

Similar to method 1, using a sampling frequency of $f = 1\ Hz$ for I_1 and I_2, and $N = 7$ as the number of consecutive counts of leakage current I_{LK} being greater than the threshold current I_{TH} in order to trigger a leak fault, $T = 7\ sec$ is the minimum time required for the system to reliably detect a leak fault. In this case, method 2 would receive a rating of 3.

Method 3: Lear Corp Design

Using the model developed in section 4.4, the period to calculate one data point of R_{GND_EQ} is t=700msec. Assuming N=10 as the number of consecutive counts of leakage current R_{GND_EQ} being less than the threshold leakage resistance R_{TH} in order to trigger a leak fault, T= 7 sec is the minimum time required for the system to reliably detect a

leak fault. Also, this design can be implemented for continuous monitoring of the system for faults. Hence, method 2 would receive a rating of 3.

Method 4: Caterpillar Inc Design

Although this method described in section 4.5 may be used for continuous monitoring of the system, if resistor R_D (e.g. 10kΩ) was to be switched into the system to calculate R_{BL} in a balanced fault condition, leakage detection would be less frequent. Increasing the value of R_D would also increase the time to detect a leak fault because of increased settling time for common mode voltage due to the presence of Y-capacitors. Hence, this system would receive a rating of 1.

CRITERIA 2: TYPE OF FAULT

Method 1: Nissan Motor Design

Based on the evaluation of this method, unless a major re-design of the GFDS was performed, it would only be capable of detecting DC faults i.e. rating 1.

Method 2: Maxim Inc. Design

As mentioned in section 4.3, an increase in sampling frequency of the GFDS and modification to the diagnostic algorithm, method 2 would be capable of effective fault detection on both AC and DC buses, i.e. rating 2.

Method 3: Lear Corp Design

As explained in section 4.4, this method would only be capable of detecting DC ground faults, i.e. rating 1.

Method 4: Caterpillar Inc Design

Similar to method 1, if the sampling frequency of V_{POS} and V_{NEG} was sufficiently increased, the GFDS could potentially detect both AC and DC faults, i.e. rating 2.

CRITERIA 3: MODE OF DETECTION

Method 1: Nissan Motor Design

Since this GFDS is susceptible to ripple voltage in the common mode bus, as well as Y-capacitance in the high voltage system, it may only perform reliable diagnostics when the system is in standby/steady state. Hence, it would be given a rating of 1.

Method 2: Maxim Inc. Design

This GFDS is fairly robust in any state of operation, therefore it would receive a rating of 2.

Method 3: Lear Corp Design

As explained in section 4.4.2, added Y-capacitance in the system could affect the effectiveness of GFDS by causing it to set a leak fault when the leakage resistance is not actually below 120kΩ. Hence, the GFDS may only perform reliable diagnostics in standby mode (when all components are disconnected from the battery), resulting in rating of 1.

Method 4: Caterpillar Inc Design

This GFDS is fairly robust in any state of operation, therefore it would receive a rating of 2.

CRITERIA 4: FLEXIBILITY OF DESIGN

Method 1: Nissan Motor Design

When implemented in a HEV with a Y-capacitance footprint that is different from what the GFDS was originally designed for, a hardware change would be necessary to maintain diagnostic effectiveness. As explained in section 4.2.2, due to the principle of operation of this GFDS, reducing V_{TH} or adding software filters will not be of any benefit. Hence, the rating for the system would be 0.

Method 2: Maxim Inc. Design

Since this GFDS is fairly immune to common mode ripple voltage, and can perform diagnostics reliably irrespective of the Y-capacitance in the system, a simple software change for f_{SW1} and f_{SW2} should be sufficient to allow implementation in a HEV with a different architecture. Hence, this method would receive a rating of 2.

Method 3: Lear Corp Design

Similar to method 1, the reliability of this GFDS would vary depending on the architecture of the HEV system, and there are no software changes that can be made to allow this GFDS to adapt to a different HEV system than it was designed for. Hence, this method would receive a rating of 0.

Method 4: Caterpillar Inc Design

Similar to method 2, This GFDS is fairly adaptable to any HEV system architecture with little to no software changes. Hence, this method would receive a rating of 2.

CRITERIA 5: SUSCEPTIBILITY TO COMMON NOISE SOURCES

Method 1: Nissan Motor Design

This GFDS is most definitely susceptible to noise, as discussed in section 4.2.2. Hence, it would receive a rating of 0.

Method 2: Maxim Inc. Design

Even though this GFDS is fairly immune to noise on the common mode bus, software algorithms may be implemented to allow the system to identify low fidelity measurements (large high frequency noise) and trigger a fault. However, since the method of operation is based on forcing a voltage imbalance in the system (when SW1 and SW2 are switched), it could be a source of interference for other monitoring devices in the system. Hence, this system would receive a rating of 1.

Method 3: Lear Corp Design

Similar to method 2, even though the system is fairly immune to common mode noise, it causes significant shifts of voltage in the common mode bus (since V_{TEST_P} and V_{TEST_N} are > V_{BATT}), potentially interfering with the operation of other circuits in the system. Hence, this system would receive a rating of 1.

Method 4: Caterpillar Inc Design

Once again, although the system is fairly immune to common mode noise, due to the GFDS's inability to detect a DC ground fault that is "partially unbalanced" as described in 4.5.2 (resulting in a Type I error), this system would receive a rating of 1.

CRITERIA 6: COST & COMPLEXITY

Method 1: Nissan Motor Design

Since the only components needed for this GFDS are capacitors, resistors, diodes, and a few op-amps, the design complexity is comparable to GFDS 2, i.e. rating would be 1.

Method 2: Maxim Inc. Design

The rating of this system would be 1 by default.

Method 3: Lear Corp Design

Because this GFDS requires the use of 2 boost converters, the complexity and cost of the system increases dramatically. It would receive a rating of 0.

Method 4: Caterpillar Inc Design

This detection method is fairly simple to implement, and is comparable in complexity to GFDS 2. Therefore, the rating would be 1.

5.3 Pugh Analysis

Using the methods for leak detection, criteria for analysis, weighting factors for individual criterion, and assigned rating per criterion for each method, the Pugh Matrix in Table 8 is developed.

Table 8: Pugh Matrix

		Ground Fault detection Technology			
Critical Criteria	**Weight**	**Method 1**	**Method 2**	**Method 3**	**Method 4**
Detection Time	4	3	3	3	1
Type of Fault	2	1	2	1	2
Mode of Detection	4	1	2	1	2
Flexibility of Design	5	0	1	0	1
Susceptibility to Noise	4	0	1	1	1
Complexity & Cost	1	1	1	0	1
	Total	19	34	22	26

Based on the Pugh matrix, it is evident that method 2 described in section 4.3 is the best solution for a GFDS in a flexible HEV architecture.

CHAPTER 6

6 Conclusion

As Hybrid Electric Vehicles penetrate the commercial vehicle industry at an extremely rapid pace, it has become important for manufacturers to develop flexible power system architectures that adapt to a multitude of vehicular applications. Equally important is the need for the hardware of subsystems and components of the flexible power systems to be designed for compatibility with alien devices and loads that may be connected to the power system. Four Ground Fault Detection Systems developed for electric vehicles have been analyzed for theory of operation, and tested for functional effectiveness using circuit modeling and simulation techniques.

Some of the major challenges that are faced by engineers designing GFDSs for flexible HEVs are varying magnitudes of Y-capacitance in power electronics components, and the unknown nature of frequency, phase, and amplitude of the voltage ripple generated by them. Not only were the theories of operation verified, but specific test cases were designed to evaluate the performance of the following four methods of isolation detection against these issues:

- Method 1: Determining the leakage resistance between high voltage conductors and chassis ground by injecting a square wave pulse into the common mode bus through a capacitively coupled path, and measuring the level of attenuation.

- Method 2: Alternately switching a known resistance into the positive and negative common mode buses and measuring the leakage current through the resistance to

calculate the total equivalent leakage resistance between high voltage and chassis ground.

- Method 3: Charging a fixed capacitance to a known high voltage, and subsequently discharging the energy into the common mode bus through a fixed resistance in order to measure the time constant of the circuit and eventually the equivalent leakage resistance.

- Method 4: Measuring the percentage of voltage imbalance between the high voltage positive bus and chassis, and high voltage negative bus and chassis, and subsequently comparing the measurement to a threshold value to detect isolation breakdown.

Finally, a Pugh analysis was done to determine the most suitable method amongst by comparing them against six criteria: detection time, type of fault detection, mode of detection, flexibility of design, susceptibility to noise, and design complexity. Method 2 was determined to be the most robust solution due to the flexibility in design and the immunity to noise, and this process successfully demonstrated that existing fault detection theories could be used for implementation in flexible high voltage power systems.

A plethora of detection strategies and methodologies exist in the industry today with consistent incremental benefits being gained for every new invention. This has been confirmed through a literature search on GFDSs for HEVs. However, a significant portion of these methodologies share the same fundamental operating principles as revealed in this study. Although most of the techniques have been presented in this paper,

there are methods that have not been researched, such as differential monitoring of float current using split core transformers or half effect sensors. This could be a potential area for future research work.

It has also been demonstrated that AC fault detection using hardware for DC GFDSs can be achieved by modifying the leakage detection algorithm. There are several papers and invention disclosures that propose potential methods for this purpose. Finally, future work could also analyze techniques for GFDS self diagnostics (to prevent type I and type II errors), methods to increase detection time, and algorithms to identify the source of the ground fault.

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