A NEURAL RECORDING FRONT END FOR MULTI-CHANNEL WIRELESS IMPLANTABLE APPLICATIONS

By

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ABSTRACT

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By recording neurons' activities simultaneously, awake animal behaviors can be predicted in real time, brain–machine interfaces controlling the machine by thought can be set up, and treatments for neurological disorders can be explored. Existing commercial neural recording equipment are bench-top systems that are bulky, high cost, consume high power, and require wire bundles tethering the neural recording probes to skull-mounted connector. To overcome these disadvantages, a miniature wireless implanted multi-channel integrated neural recording micro-system with low power and low noise is needed. This thesis work addresses the challenges to developing an analog front end for wireless implanted multi-channel neural recording systems, which include ultra low noise, extremely low power, high power supply rejection radio, low area occupation, sufficient data conversion speed and optimizing design tradeoff between all these requirements. Two versions of a neural amplifier were built. Following optimization guidelines in this thesis, noise efficiency and a new figure of merit for neural amplifiers were effectively improved. A successive approximation (SAR) ADC tailored to wireless implantable neural recording systems was also designed. The new SARADC is able to process 32 neural spikes recording channels in a multiplexing manner with low power consumption and low area occupation. The results of this research lay a solid foundation for future realization of high sensitivity wireless implantable neural recording system

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Haitao Li

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

1 Introduction

1.1 Motivation and application

There is a great demand for technologies that enable neuroscientists and clinicians to observe the activity of brains neurons simultaneously [1]. By recording this activity, one can predict behavior of awaking animal in real time [2-4]. Hand or limb movements are recorded together with the corresponding neural signals. This information can be used to drive a robotic arm or a cursor on a screen [5]. In this way, brain–machine interfaces which control the machine by thought can be set up if the activity of multiple neurons can be observed [6]. According to the survey by Christopher & Dana Reeve Foundation, there are 5.6 million paralyzed patients in USA, among which nearly 1.3 million have a spinal cord injury. They will be free from wheelchair or crutch with technology advancement in brain–machine interfaces. Multi-channel neural recording system can result in increased prosthetic control and lifetime [7].

A miniature implanted multi-channel integrated neural system is also very important for treatment of neurological disorders [8]. These neural diseases includes epilepsy and Parkinson's disease [9]. Among 50 million epilepsy patients in the world, thirty percent of them cannot be efficiently controlled by the current technology [10]. Globally, about 6.3 million people are suffering Parkinson's disease, among which 1 to 1.5 million are Americans, but there is no cure for this disease now. Neural stimulation can effectively eliminate the tremors of Parkinson's disease [8].

The commercial neural recording equipments are bench-top ones, which are bulky,

high cost and consume high power [9]. Moreover, there are no commercial wireless implantable neural recording products. Currently, the data is collected outside body through bundles of wires tethering the neural recording probes to skull-mounted connector. These bulky connection wires and connector lead to tissue infection, external noise and interfering signals coupling. To overcome these disadvantages, a miniature wireless implanted multi-channel integrated neural recording micro-system with low power and lower noise is necessary to be studied.

1.2 Challenges and objectives

A typical neural system is shown in Figure 1.1. The neural probes capture the neural signal from neurons. Recording interface performs noise and offset rejection, signal amplifying and digitizing. The digitized signal is then processed by digital block and transmitted to computer for further data analysis. The wireless module also receives commands from computer for signal processing. This module also receives the stimulation signals from computer and transfers them to stimulation interface for neural stimulation. This thesis will work on the recording front end, including neural amplifier and ADC.

1.2.1 Challenges

For neural signal recording application, the input signal is very weak, typically between 50 μV and 1 mV [11]. Extremely low noise is needed for the interface circuit. As the first stage of neural interface, the noise of recording front end is extremely important to the system performance. Practically, the input-referred noise of neural recording front end should be below the background noise of the recording site which is from 5 μV to 10

μV [12]. A large ripple also exists on the wireless power line. Therefore, the system should have a good power supply rejection radio. The chip needs also to consume small area to be implantable.

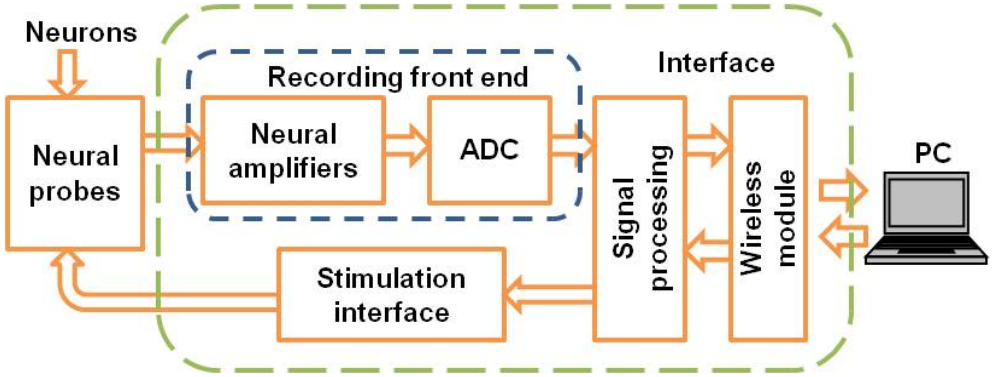


Figure 1.1. Simplified block diagram for implanted multi-channel neural system. For Interpretation of the references to color in this and all other figures, the reader is referred to the electronic version of this thesis.

The power of the circuit can increase the temperature of the surrounding tissues. For neural detection, temperature should rise less than 2 ºC to avoid damage to surrounding neurons [13]. For a multi-channel neural recording system implanted within the skull, the channel's number is on the order from 100 to 1000 [5]. Therefore, such a high density interface array is very sensitive to the power limitation. Plus, ultra-low power operation can preserve long-battery life and maximize the time between recharges [13]. As a critical part of the neural interface, the recording front end should consume low power. At the same time, there is tradeoff between low power and low noise for circuit design. How to achieve an optimized design is one of the challenges for implanted multi-channel neural recording system design.

ADC design in the neural recording front end is also very important to the neural interface. For a multi-channel recording, sharing an ADC among several channels is

necessary for low power requirement. The total number of circuit components decreases in this way. For such an ADC arrangement, a high speed ADC is required to ensure enough recording bandwidth. Also, there is a tradeoff between low power and high speed design for ADC. This tradeoff is another challenge for recording front end of implanted neural recording system.

The Other requirements for implanted multi-channel neural recording system includes: good linearity of neural amplifier to reject signal distortion and low chip area to be suitable for implantation. There is also a tradeoff between these factors.

To sum up, the challenges of front end of wireless implanted multi-channel neural recording system interface circuit are:

(1) Extremely low noise performance should be achieved to detect low amplitude neural spike;
(2) Extremely low power should be achieved to avoid damage to human issues;
(3) High power supply rejection radio to be immune to the large wireless power ripple;
(4) Tradeoff between noise, power, power supply rejection radio, linearity and chip area should be considered when designing neural amplifiers;
(5) Tradeoff between speed, power, accuracy and chip area should be considered when designing neural ADC.

1.2.2 Objectives

This research is to build up a practical neural front end circuit for implanted neural recording system. The front end includes a neural amplifier and an ADC. The neural

amplifier should reject the noise and dc offset and amplify the neural signals. Technologies for low noise, low power and small chip area need to be studied. The neural ADC should be shared by multi-channels. The total power dissipation of neural recording front end should be less than 5mW and the lower, the better.

1.3 Thesis organization

This chapter serves as an introduction and motivation for the neural recording interface in this thesis. Challenges and objective is also presented in this chapter. The rest of the chapters are organized in the following way:

- Chapter 2 introduces the background knowledge of neural signals and neural electrodes array, and takes a review of the neural interface circuits. The information on different neural signals is stated. After that, the approaches and design results from different group will be presented and discussed in this chapter. Finally, our approaches will be described.
- Chapter 3 discusses the neural amplifier design. Specification of neural amplifier is given upon the calculation and background knowledge of neural signals. The design results of the primary version are described. Based on these test result, an optimized design is given.
- Chapter 4 states ADC design. Different ADC structures are compared for the best choice. After that, ADC arrangement with multi-channels is analyzed. Finally, the design results are shown in this chapter.
- Chapter 5 gives a summary of the work in this thesis. Conclusion and the suggestion of future work are provided.

2 Background knowledge and literatures review

2.1 Background knowledge of neural signals

2.1.1 Neurons

The neuron is one special type of cell which is electrically excitable to transmit and process information by electrical and chemical signal. There are over 10 billion neurons in human brain [14]. A typical neuron includes a cell body (soma), dendrites, and an axon, as shown in Figure 2.1. Dendrites can be a lot of branches, hundreds of micrometers long, while axon can be one meter long for humans. Ion channel is formed in the neuron cell membranes with ions such as sodium, potassium, chloride, and calcium. Voltage gradients are maintained by the ion channel.

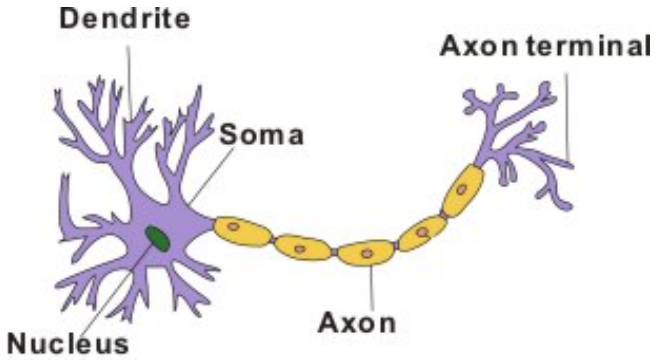


Figure 2.1. Neuron cell's structure [15].

2.1.2 Neural recording methods

Generally, there are two ways to measure the neural signals: one is non-invasive method and the other is invasive method. The non-invasive neural recording methods are Electroencephalography (EEG), Magnetoencephalography (MEG), functional Magnetic Resonance Imaging (fMRI) and Positron Emission Tomography (PET).

EEG records the electrical field changes of neurons by placing electrodes on the scalp. It has high time resolution, on the order of milliseconds, to detect very small events, enabling it to be the primary monitoring technique for most neurophysiological processes. However, the most importance limitation of this technology is the poor spatial resolution.

MEG is generated by the same neurophysiologic process with EEG. The difference is that MEG detects the magnetic field changes. Compared with EEG, MEG has better spatial resolution but less information.

fMRI and PET monitor the neural activity through blood flow and metabolic in the cortical tissues. These two technologies have better spatial resolution than EEG. The limitations are that they have poor time resolution and the recording subject cannot move freely.

The invasive neural recording methods record the neuron activity directly from the cortex under the skull. They can provide high spatial and time resolution at the same time. This is very important for understanding of intracranial connectivity and neural activity. These methods include Electrocorticography (ECoG) and Intracranial EEG.

ECoG places the microelectrode on the surface of cortex, and intracranial EEG places microelectrode into the cortex. As a result, ECoG cannot record neural signal of individual neuron cell while intracranial EEG can. Intracranial EEG allows extremely high spatial and temporal resolution enabling to decode neural signals and control artificial limbs [16].

2.1.3 Characteristics of neural signals

The neural signals recorded by microelectrodes array can be divided into two categories: action potential and local field potential (LFP). For these two kinds of neural signals, the characteristics are different on signal bandwidth, amplitude and function.

Action potential is a series of pulse generated by the large voltage change on ion channels. The action potential pass through axon very quickly and active nearby neurons. This neuron activity is called “neuron firing”. Action potentials in neurons are also named as "spikes". There are two ways to record action potentials: intracellularly recording and extracellularly recording [17]. For the case of intracellularly recording, a sharp electrode in inserted into the cell. A 40mV action potential can be detected in this way. For extracellularly recording by placing electrode adjacent to the neurons, the neural spikes’ amplitude is from 10μV to 500μV with a bandwidth from 300Hz to 7kHz.

A LFP is a kind of electrophysiological signal, dominated by the electrical current flowing from all nearby dendritic synaptic activity within a volume of tissue [18]. LFP can be recorded with a low impedance extracellular microelectrode, placed far from individual local neurons to prevent any particular cell from dominating the electrophysiological signal. LFP’s amplitude is from 0.1mV to 50mV and may contain frequency content below 1 Hz [1] and is cut at around 300 Hz [18]. Spike activity and LFP activity are coherent [19]. Because the spikes are the primary signal of interest, it is important to remove LFP while detecting neural spikes.

2.2 Literature review for neural recording system

2.2.1 Neural spikes recording micro-electrodes array

Neural electrodes array is used for multi-channel neural signal simultaneous recording. Two microelectrode arrays are widely used in the academic groups. One is from University of Michigan, and the other is from University of Utah.

Both 2-D array and 3-D array exist for microelectrodes array from University of Michigan. There are two kind of 2-D microelectrodes arrays in [20]. The first one is an eight-site neural array for both recording and stimulation. The site is 165μm^2, located at the tip of the shank, which is 5mm in length, and approximately 15μm thick. The center to center distance between sites is 20-40μm. The second one is a thirty-two channel neural array with integrated amplification and time-division multiplexing circuitry. The on-probe circuit can provide 40dB gain and limit the signal band at 9.9kHz. A Michigan probe is expected to displace (or destroy) approximately 50 neurons and 400 000 synapses [13]. The limitation of 2-D electrodes array is that it cannot record the activities of a large region of cortex. To solve this problem, University of Michigan also built 3-D Microelectrodes array [21]. It is an 8×16 shank eight-probe array formed by 2-D Michigan Probe. A lot of system is already developed based on micro-electrodes array from University of Michigan [22-27].

The picture of microelectrodes array from University of Utah can be found in [28]. Utah Electrode Array is a 10×10 platinum-tipped silicon 3-D electrodes array with a size of 4×4×1.5 mm^3. The inter-electrode space is 0.4mm. The needle is 80μm wide at the

base. An average of 58.6% of the microelectrodes in the array functions properly. The average signal-noise ratio is 5.5:1. Some groups are using Utah Electrode Array for research [29, 30].

To make the specification of the neural interface circuit, it is necessary to study the neural electrodes characteristics. An equivalent circuit of neural electrode is shown in Figure 2.2. C_e is the total electrode capacitance. R_t represents the effects of charge transfer, which involves the transfer of electrons mediated by oxidation and reduction reactions at the electrodes under equilibrium conditions. R_s is spreading resistance due to electrolyte resistance and is affected by the electrode geometry. Smaller electrodes normally have higher impedance [17]. The impedance of neural electrodes ranges from 80kΩ [28] to 4MΩ [31] for 1kHz frequency.

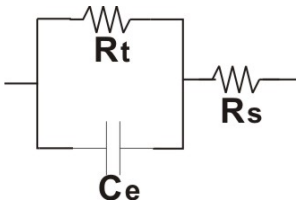


Figure 2.2. Circuit model of the electrode [32, 33].

The requirement of neural recording system is set by the electrode thermal noise. By Nyquist's formula, the electrode thermal noise is expressed as:

$$V_{RMS} = \sqrt{4k_B TR\Delta f} \tag{2.1}$$

where k_B is Boltzmann's constant, T is the temperature, R is the electrode resistance, and

Δf is the bandwidth. Set R=1MΩ, T=300K, Δf=7kHz, then the thermal noise is 11 μV_{rms}. Taking the background spikes noise into consideration, the total noise of the neural input signal for the sensor is less than $30\mu V_{rms.}$ Therefore, the electronic noise of neural interface circuit should be less than $30\mu V_{rms}$. In the work in this thesis, the value is set at $10\mu V_{rms}$ to get better performance.

In vivo application, motion artifacts should be considered. Electrodes contacting with electrolyte may have different potentials [34]. Motion artifacts results from the fact that if the distance of two electrodes in an electrolyte changes, the potential difference will also changes [35]. Therefore, a DC offset is available between recording electrodes and the reference electrodes and will vary with different arrangement of these two kinds of electrodes. This DC offset can be from several hundred mV [17] to 1V [1]. It needs to be removed by the interface circuit.

To sum up, the neural interface circuit is required to filter LFP and DC offset and amplifies the neural spikes. Low noise performance is needed to detect the weak neural input and $10\mu V_{rms}$ is set as the design goal. Low power is needed to avoid the surrounding neural issue damage and 5mW is set as the design goal.

2.2.2 Neural recording front-end circuits

One important research group studying on neural recording detection is from University of Michigan. In 1992, J. Ji described an implantable neural recording interface [36]. The preamplifier is with a diode-capacitor filter to provide low cut-off

frequency. The on-probe circuit can offer 300× ac gain over the bandwidth from 15Hz to 7kHz. The input equivalent noise is 15 μV_{rms}. However, one major issue is the gain variability from probe to probe and even from channel to channel. The gain cannot also keep stability upon the time and light effect. To overcome these problems, P. Mohseni presented new preamplifier structure utilizing the dc baseline stabilization scheme in 2004 [37]. The closed loop formed by resistance feedback provides 39.3dB ac gain. The input equivalent noise is 7.8μV_{rms}. However, the power dissipation is as large as 114.8μW and the noise efficiency factor is as large as 19.4. In 2005, R. H. Olsson III used diode connected sub-threshold NMOS transistors to set low cut-off frequency [20]. The on-probe amplifier has a gain of 38.9dB, and an input referred noise of 9.2μV_{rms}. The power dissipation decreases to 68μW. The same amplifier is utilized in a neural recording system [22]. The input referred noise is 12.6 μV_{rms}. A 5-bit successive approximation (SAR) ADC is built with sampling frequency at 160ksamples/s. The entire system consumes 5.4 mW of power interfacing 256 sites. In [38], the same amplifier is further optimized with input referred noise at 4.8μV_{rms} and power at 50μW. In [39], a 8-bit SAR ADC with different structure from that in [22] is given with sampling frequency at 20kSampling/s and power at 680 nW. This group has not start to design the wireless implants yet.

Another important group is from University of Utah. In 2003, R. R. Harrison proposed a neural preamplifier for neural recording application [1]. This design turns to be a very popular design for neural interface. MOS-Bipolar pseudo-resistor

elements are used to reduce distortion for large output signals and act as a high pass filter together with the feedback capacitor. Current-mirror structure is utilized for operational transconductance amplifier (OTA). The input-referred noise is 2.2 μV_{rms}, the dissipated power is 80μW, the bandwidth is from 0.025Hz to 7.2kHz, the noise efficiency factor (NEF) is 4.0, the total harmonic distortion (THD) is 1.0% for 16.7mV input, the gain is 40dB, and the occupied area is 0.16mm^2. In 2006, this amplifier is utilized in a 100-electrode neural recording system INI1 and INI2 [40]. A successive-approximation (SAR) ADC converts the analog signal into digital signal. The sampling rate is 15kSamples/s and the accuracy is 10 bit. The chip consumes 13.5mW of power. In 2008, INI5 fixed all design errors [41]. The input referred noise is 5μV_{rms}. The chip consumes 8mW from an unregulated AC coil voltage. Absolute threshold are used for spikes detection in this group to decrease the data density.

One group from University of California at Santa Cruz is studying on neural interface circuit. In 2006, a recording system with off-chip ADC was reported [42]. An improved current-mirror structure OTA is used to improved noise performance and increase open-loop gain. SAR ADC is adopted because it is more widely used in multiplexed data acquisition systems compared with sigma-delta ADC. For the OTA, the simulation result shows that the input referred noise is 8.5 μV_{rms} and the power is 18 μW. The number of ADC per channel is also discussed at the end of the paper but not in details. In 2008, the same group published a paper on design optimization for neural recording system. The optimal transconductance and gain of pre-amplifier for their

application is are mathematically derived and an optimal number of channels per ADC for 128 channels recording is selected to achieve power-area product [43]. The input referred noise is 5.5μV_{rms}, the bandwidth is 10.9kHz, and the consumed power is 5.5mW for 128 recording channels. For the setting-up test in this paper, the extracellular electrode is from FHC, Brunswick, ME. In 2009, an improved version of neural recording interface was reported combined with wireless transmission module and spike feature extraction module [44]. An ADC is shared by 16 amplifiers through time-multiplexing. The resolution of the ADC can be adjusted from 6 bits to 9 bits. There are 128 channels in total. The input referred noise is 4.9 μV_{rms}. The total chip power dissipation is 6mW.

Another neural interface research group is from University of Toronto. In 2007, a 16×16 neural recording array is reported [45]. The preamplifier is similar to the structure in [1]. The input referred noise is 13μV_{rms}. The power dissipation is 6mW. No ADC is integrated in this system. In 2009, a 16×16 channels neural recording system interfacing with Utah electrode array was reported from this group [29]. Telescope OTA structure is used for neural amplifier. The input referred noise decreases to 7μV_{rms}, and the power dissipation decreases to 5.04mW. No ADC is integrated in this micro-system. In 2010, a neural recording and stimulation interface was built for 128 channels. This version is full differential structure to suppress common mode noise and interference. An 8-bit SAR ADC is built in this micro-system. The total power dissipation is 9.33mW. The wireless module to transfer power and data has not been set up yet.

A research group at Massachusetts Institute of Technology (MIT) reported a neural amplifier in 2007 [5]. The OTA is an improved version of conventional folded-cascode topology. A source-degenerated current sources structure can optimize noise performance. The test result shows that the input referred noise is 3.06 μV_{rms}, the bandwidth is from 45Hz to 5.32kHz, the NEF is 2.67, and the consumed power is 7.56 μW. In 2008, a wireless neural interface with the amplifier was reported [46]. An analog decoding architecture is used instead of ADC. Not completed test result is given in this paper.

There are other neural interface research groups from Ecole Polytechnique de Montreal [47-49], Israel Institute of Technology [50], University of Leuven [51], Johns Hopkins University [52], University of California at Los Angeles [53], Swiss Federal Institute of Technology [54], etc..

2.3 Neural recording system for wireless implants

According to the literature review, a lot of research groups are working on neural interface. However, some research groups' work is not wireless implantable system; some other research groups are still working on wireless implantable system. Nobody has achieved the wireless implantable design goal yet. A wireless and implantable neural recording system is really important to neural recording because it can 1) avoid the infection caused by transcutaneous connector; 2) avoid external noise and interference coupling to the connection wire; 3) avoid the bulky connector and external electronics and enable free movement of target animals [40].

This thesis contributes to a wireless and implantable neural recording system. Some critical modules of neural recording system will be built.

2.3.1 Our approach

Our system aims to build a neural recording system for wireless implants. It supports high capacity, real time bi-directional communication. The system consists of two modules: the Wireless Neural Recorder (WNR) and the Extra-cranial Neural Relay (XNR). The WNR is fixed on the surface of cortex under the skull. The analog front end interfaces with the implanted micro-electrodes array directly, detecting the neural spikes and filtering the noise. The neural signal processor (NSP) on the WNR compresses the neural data from analog front end. The Wireless power and data transceiver receives the power wirelessly and transmit the neural data to XNR out of the skull. The XNR provides power to the WNR through inductive coupling, relaying neural data to the external processing unit (EPU) and sending configuration commands to the WNR. User can control the entire system and process the data by a graphical user interface (GUI) on the EPU. The diagram of our neural recording system is illustrated in Figure 2.3.

This thesis's goal is to build the analog front end of neural recording system for wireless implants. It contents of two parts: recording channel and analog-to-digital converter. In each recording channel, there is one pre-amplifier, band pass filter and variable gain amplifier (VGA). The pre-amplifier is to amplify the neural spikes. The band pass filter is to filter the noise. The VGA is to provide additional gain to neural spikes. The diagram of the analog front end is shown in Figure 2.4.

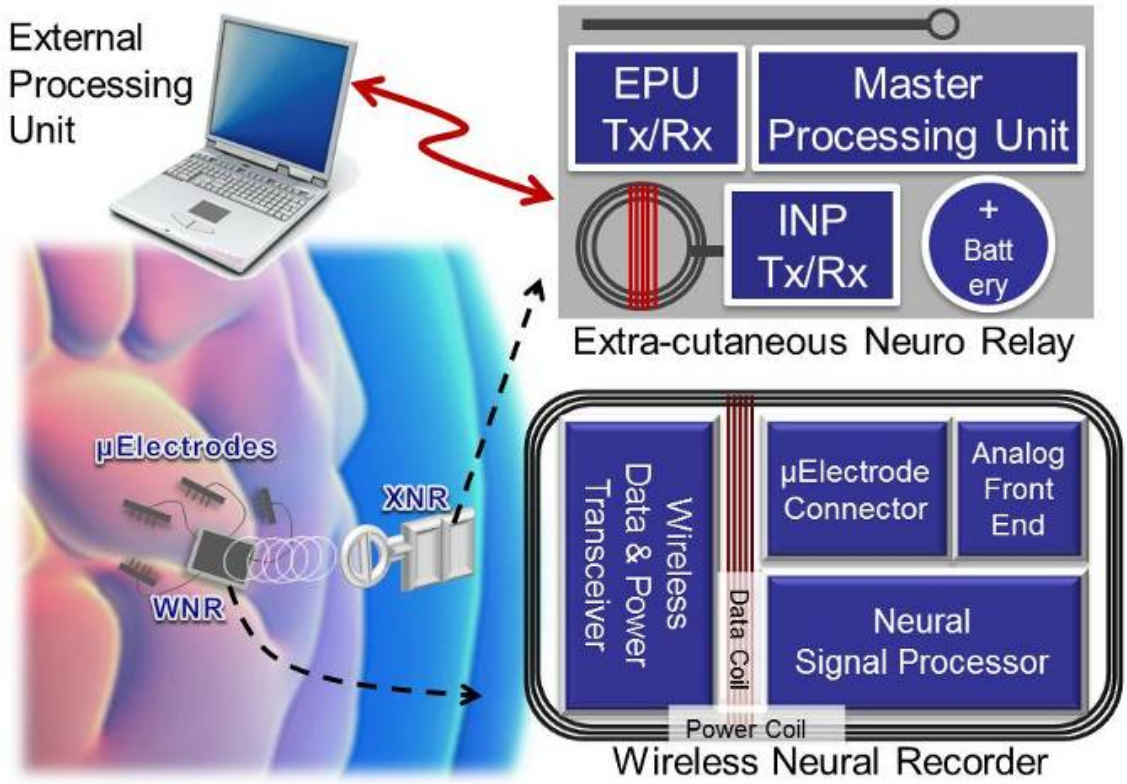


Figure 2.3. System diagram of neural recording system for wireless implants [55].

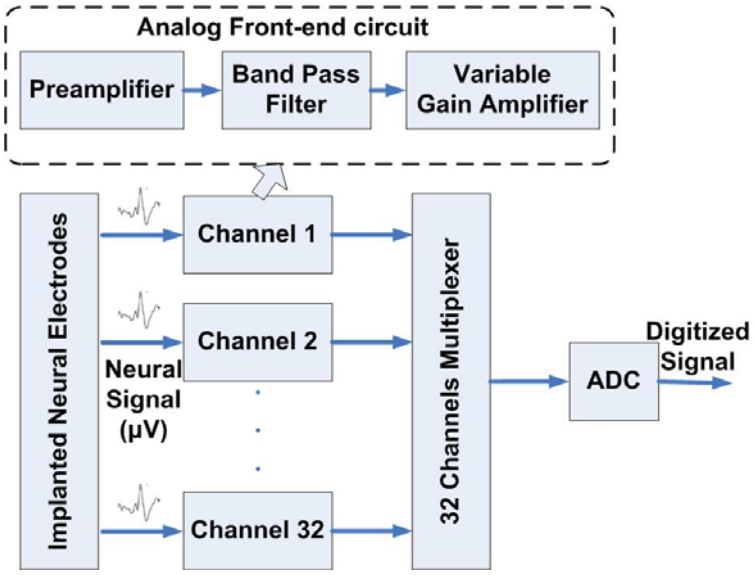


Figure 2.4. Diagram of analog front end. 32 recording channels are taken as an example.

3 Neural amplifier design for wireless recording implants

In this chapter, the design of neural amplifiers is introduced for wireless recording implants. This application requires a neural amplifier which could provide low noise, low power and good noise rejection from power line. The performance tradeoff of analog design makes such an amplifier hard to be achieved. To find out the proper structure, design rules and design experience of neural amplifier, a neural amplifier was fabricated and tested.

3.1 Comparison between a full-differential and a single-ended structure

Firstly, a single-end structure and a full-differential structure were compared to meet the design requirement. For multi-channel application, the power dissipation, noise and area are import factors. Here common-mode rejection ratio (CMRR) is used to compared the noise performance. Power supply rejection ratio (PSRR) would not be compared because there is no significant difference on this factor between a single-end structure and a full-differential structure. From the design experience and knowledge of analog integrated circuit design, the power, area and noise performance between these two structures are listed in Table 3.1. The single-end structure has better performance on power dissipation and area occupation, and full differential structure has better performance on the rejection of common mode noise. Even though the single-end structure cannot provide CMRR as good as full-differential structure, it provides sufficient CMRR for neural recording with two differential inputs. Therefore, single-ended structure was adopted in this work.

Table 3.1. Comparison between single-ended and full-differential structures.

Performance	Single end	Full differential
Power dissipation	good	fair
Area occupation	good	fair
CMRR	fair	Good

3.2 Neural amplifier requirement and specification

The main duty of a neural amplifier is to provide gain over the bandwidth of neural action potentials and also reject the signal out of the bandwidth. As discussed in chp2. Neural action potentials typically have amplitude from 10μV to 500μV with a bandwidth from 300Hz to 7kHz. The neural amplifier should also reject low frequency interference, including DC offset, typically around 1V, and local field potentials (LFP), typically 0.1mV to 50mV below 300Hz.

Typically, neural amplifier consists of two stages, as shown in Figure 3.1. The first stage is pre-amplifier, providing gain and filtering function as the direct interface between the neural recording micro-electrodes and neural recording interface circuit. The second stage is gain amplifier, providing addition gain.

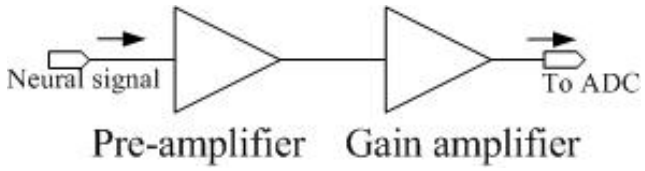


Figure 3.1. Typical structure of neural amplifier. The pre-amplifier is the more important than the gain amplifier.

3.3 Noise specification of neural amplifier

To analyze the affect of the two stages of neural amplifier to noise performance, a noise model of multi-stage system is shown in Figure 3.2. V_{in} and V_{out} are the input and

output signal, respectively. V_{ni} (i=1,2…) is the noise at the input of the i_{th} stage. A_i is the gain of the i_{th} stage.

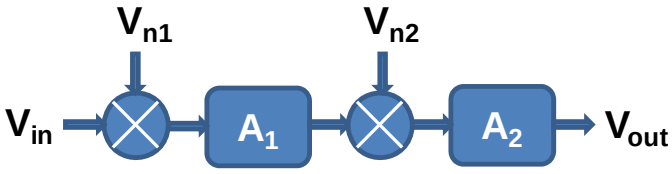


Figure 3.2. Noise model of a two-stage neural amplifier.

Define V_{inref} as the input referred noise, and then it is given by

$$V_{inref} = V_{n1} + V_{n2}/A_1 \tag{3.1}$$

(3.1) shows that the noise at the first stage makes the major contribution for the noise performance in a multi-stage system and the noise from the following stage is decreased by a factor of A_1, which is the gain of the first stage. As discussed in Chapter 2, the input referred should be less than 30 μV_{rms} in theory. To leave enough design margin, the design goal of input referred noise for the pre-amplifier was set at 10μV_{rms} in this work. The gain amplifier can use the same OTA.

3.3.1 The open loop gain of OTA

The open loop gain of operational transconductance amplifier (OTA) affects closed loop gain accuracy of neural amplifier. In Figure 3.4, a is the open loop gain, and β is the feedback factor. Define T as the loop gain, then

$$T = a\beta \tag{3.2}$$

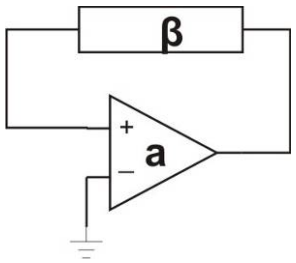


Figure 3.3. Schematic of amplifier for OTA's open loop gain analysis.

Define that the closed loop gain of the circuit in Figure 3.3 is A, then

$$A = \frac{a}{1 + a\beta} = \frac{1}{\frac{1}{a} + \beta} \tag{3.3}$$

If $T=a\beta \rightarrow \infty$, then the idea value of A

$$A_{ideal} = \frac{1}{\beta} \tag{3.4}$$

However, T cannot be infinite in reality. Substituting (3.4) into (3.3), we get

$$A = A_{ideal} \times \frac{1}{1 + 1/T} \tag{3.5}$$

Define gain error as G_e, then

$$G_e(\%) = 100\frac{A - A_{ideal}}{A_{ideal}} \approx -\frac{100}{T} = -\frac{100}{a\beta} \tag{3.6}$$

Therefore, for a fixed β, a large a provides a small gain error. For neural signal detection application, the closed loop gain of neural amplifier can be from 100 to 1000. Here we take A=100 for calculation (β=0.01). To achieve a gain error less than 1%, the

open loop gain *a* should be larger than 80dB. Therefore, the open loop gain of the OTA in neural amplifier should be larger than 80dB.

3.3.2 The power signal rejection radio of OTA

Because the front-end interface circuit is implanted powered wirelessly, the ripple on the power line may be large and affect the noise performance of the neural amplifier. Therefore, the power signal rejection radio (PSRR) performance is very important for wireless implanted neural recording system.

The PSRR is defined as

$$PSRR = \frac{A_v(V_{dd} = 0)}{A_{dd}(V_{in} = 0)} \tag{3.7}$$

in which A_v is the open loop gain (differential gain) of OTA, A_{dd} is the gain from power ripple to OTA output, V_{dd} is the power ripple, V_{in} is the differential input.

The typical value of power ripple from the wireless supported power module on chip can be larger than 10mV (personal discussion with Professor Ghovanloo from Georgia Tech Institute), even if the wireless power receiver is followed by a regulator. For example, a PSRR over 80dB is necessary to ensure 10-bit accuracy for a 10mV ripple, assuming a 10μV input.

3.3.3 Other specifications and requirements of neural amplifier

High CMRR can reject common mode noise sources including the interference from 50/60 Hz power line noise. CMRR is set larger than 80dB for the OTA. The phase margin

of the OTA is set larger than a typical value of 60° to ensure neural amplifier stability. The bandwidth of the pre-amplifier is set from 300Hz to 7kHz to amplify neural spikes and reject DC offset and LFP. The power of neural amplifier is set to less than 100 μW to ensure that the whole system power dissipation is less than 10mW to avoid tissue damage in 32 channels. A closed loop gain of 40dB is set for the first stage of neural amplifier. An additional stage follows this stage to provide additional 20dB gain. The reason that 60dB gain is not set for the first stage is to relax the design difficulty for the OTA. If 60dB is set for neural amplifier, open loop gain of OTA should increase to maintain the same gain error, and output range should also increase to maintain linearity. All these factors increase the design difficulty.

3.4 Design of neural amplifier

3.4.1 Feedback structure design of pre-amplifier

The feedback path of the pre-amplifier is to provide gain and filter function together with OTA. Figure 3.4 illustrates the archetypal differential configuration for neural amplifiers. The two different structures are commonly employed for the feedback path, defined as style I and style II in Figure 3.4. For both of these structures, the feedback path with C_f realizes a high-pass filter. The style I feedback path [20] is realized with two subthreshold-biased transistors, and style II [56] is realized with two diode-connected transistors. To compare these two structures, both were implemented in a 0.5μm CMOS test chip. To accommodate the n-well technology, the substrate of the feedback path transistors was connected to the common mode voltage, V_{cm}, for style I. The purpose using capacitors instead of resistors for closed loop gain is to improve system matching,

and increase the noise performance. Both of these two feedback structures are fabricated to compare the performance for future optimization design.

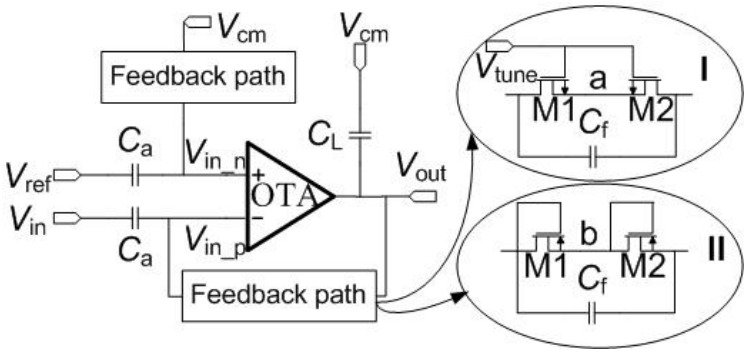


Figure 3.4. Pre-amplifier with two optional feedback paths.

3.4.2 The design of gain amplifier

The structure of gain amplifier is shown in Figure 3.5. There are two options of structures. One is the inverting structure, and the other is non-inverting structure. In this work the non-inverting structure is used to avoid the capacitance load effect to the first stage of neural amplifier. Sub-threshold self-biased transistors same in the first stage is used here to remove dc offset. The gain of this stage is express as $(C_f+C)/C$. The capacitor with value of "C" can also be substituted by a capacitors array for variable gain application.

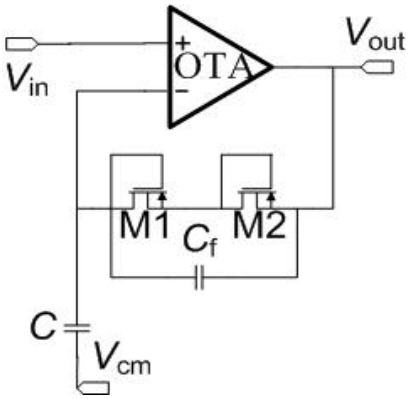


Figure 3.5. The structure of gain amplifier.

3.4.3 Schematic design of OTA

As shown in Figure 3.4 and Figure 3.5, OTA is a key component of both pre-amplifier and gain amplifier. It was found in Section 3.2 that the OTA of pre-amplifier is extremely important for system performance. The OTA of this stage can be shared by the gain amplifier.

The OTA schematic is shown in Figure 3.6. It is a two–stage structure with miller compensation capacitance between the first stage and the second stage. The input transistors are biased in sub-threshold region to minimize the power consumption and improve noise performance. Large area PMOS transistors are used as input transistors to minimize the 1/*f* noise. The base and source of input transistors are shorted to improve CMRR and transistor matching. For the load and current mirror transistors, the over driving voltage is set at 0.5~0.6 V to minimize their contributions to input referred noise. These transistors also use large L value to improve current mirror matching.

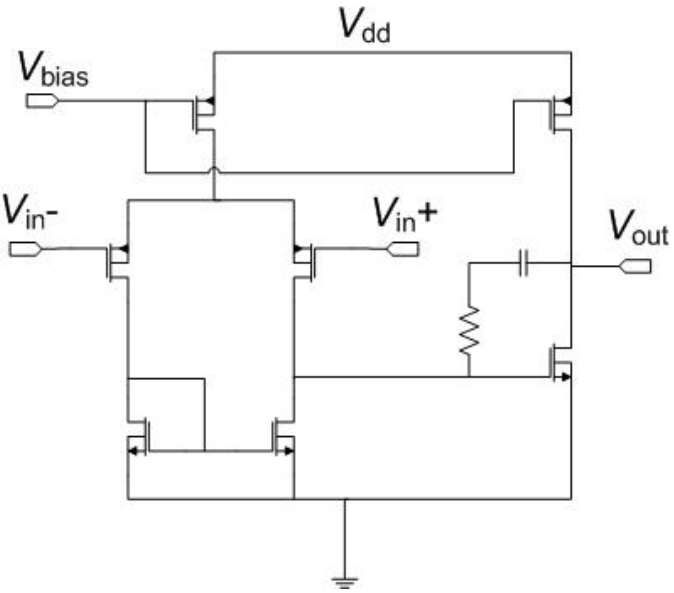


Figure 3.6. The schematic of OTA. Both pre-amplifier and gain amplifier use this OTA

structure.

3.4.4 Neural amplifier layout design

For amplifier layout design, the device matching is important to improve CMRR and decrease offset. One important layout matching method for the OTA is common-centroid layout design. For transistor matching, all the symmetrical transistors should be divided into fingered structures and placed in a common-centroid way. Figure 3.7 shows a common-centroid layout placement for two input transistors of OTA: M1 and M2. M1 and M2 are divided into two same parts, respectively and each part is with fingered structure.

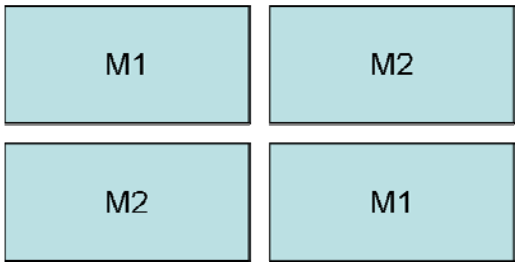


Figure 3.7. Common-centroid layout design.

Another way to improve transistor matching is to place the symmetric transistors in the same orientation to avoid the effect of implantation angle in the fabrication process. Transistor mismatching can be further decreased by placing dummy transistor along the transistors. Increasing the size of transistor can also decrease device mismatching.

For those transistors forming current mirror structure, all the transistors should be divided into fingered structures and placed alternatively to improve matching. One placement way can be ABABA, where A and B represent one finger of the transistors.

For capacitor mismatching, increasing capacitance can improve the matching accuracy.

Common-centroid layout placement is used for capacitor design as shown in Figure 3.8. C1 and C2 are divided into two parts and placed in a common-centroid way. Dummy capacitors can also be used to further improve capacitor matching.

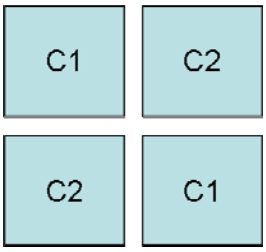


Figure 3.8. common-centroid layout design for capacitors.

Each OTA is surrounded by the guard ring to isolate the noise affect from other modules. There are two kinds of guard ring: one is hard guard ring, and the other is soft guard ring. In order to achieve the best noise protection, hard guard ring is used for amplifier isolation. The guard ring structure is shown in Figure 3.9, which includes two parts: the inside one is connected to the substrate and the outside one is connected to the N-well. In this way, the OTA is protected from all the noise outside of the N-well.

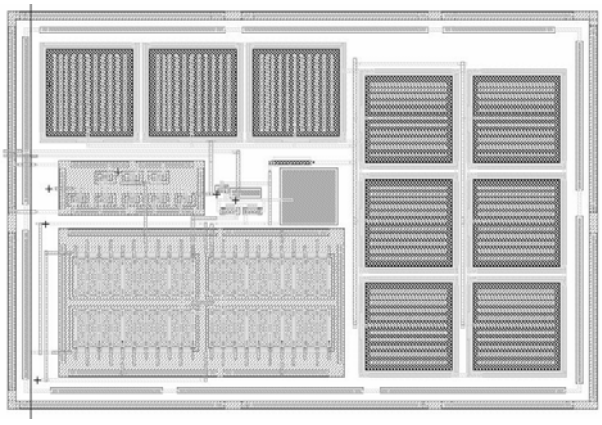


Figure 3.9. Guard ring surrounding the OTA.

The input wire from the sensor to interface circuit is very sensitive to noise. This

wire should be short and narrow to decrease the parasitic capacitor and shielded to achieve the best noise performance. For 3-metal, N-well process, the wire can be protected in the way in Figure 3.10. M1 in the center is well protected by the surrounding grounded metal and N-well from noise affect.

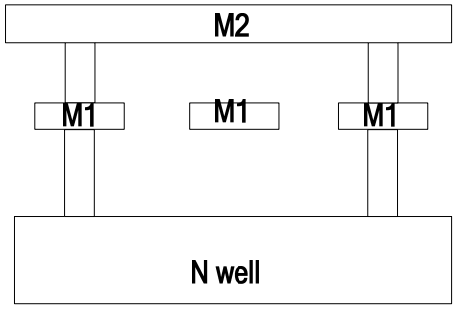


Figure 3.10. Wiring shielding structure. M1 is metal 1 layer, and M2 is metal 2 layer.

Electrostatic discharging (ESD) circuit should be built with pad to avoid device breakdown. The MOSFET gate has an extremely high resistance and low capacitor. As a result, the electrostatic charge on the gate may bring high voltage and cause transistor breakdown. ESD circuit is shown in Figure 3.11. Suppose the voltage across a forward biased diode is 0.7V. When V_{in} is larger is V_{dd}+0.7V, the diode D1 will be on and force V_{in} to be less than V_{dd}+0.7V. When V_{in} is less then GND-0.7V, the diode D2 will be on and force V_{in} to be larger than GND-0.7V. In this way, the range of V_{in} is fixed from GND-0.7V to V_{dd}+0.7V.

Layout design reliability should be taken into consideration. Before routing, simulation should be run for the maximum current of each wire. The minimum wire path width and the number of via across the wire should be calculated according to this peak

current. One single via is not suggested to be used because the fabrication result may not be good. Use a wide wire for the power wire. For those extremely wide wires, wire holes maybe needed to decrease the stress effect. 45 degree routing should be used if the wire routing direction needs to be changed to reject noise accumulation at the corner.

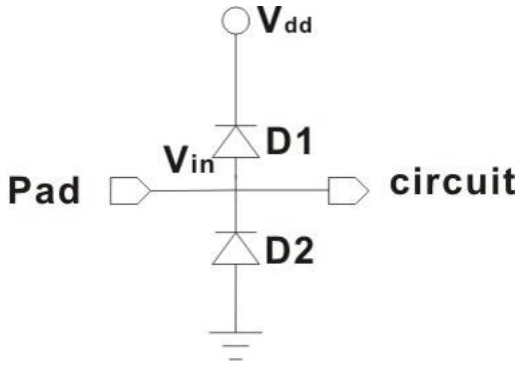


Figure 3.11. ESD protection circuit.

The long wire routing switched the metal layers through the M1M2 via for every 300 μm to avoid stress effects. The stress effect may break the wire routing. For those wire connecting to a transistor's gate, the wire routing was also switched to different meal layer after a short routing to avoid antenna effect. The antenna effect may break the MOFET gate by static charge on the gate.

Voltage attenuation was taken into consideration. The voltage attenuation happens when the wire resistant is so large to course large voltage dropping on the wire. This effect can be weaken by placing power wires with wide path in the periphery of the chip, and placing enough via holes on the guard rings and the active regions of transistors to decrease parasitic resistance.

3.4.5 Post-layout simulation results of neural amplifier

Post-layout simulations were run with Cadence Spectre tool for neural amplifier designs. Two feedback structures shown in Figure 3.4 are used as preamplifier. All the neural amplifiers used the same OTA structure in Figure 3.6.

To get the open loop gain, phase margin and unity bandwidth of OTA, post-layout simulation were run for open loop configured OTA and the results are shown in Figure 3.12. The gain is 86.7dB, unity gain bandwidth is 708 kHz, and the phase margin is 54°. The results show that the OTA has sufficient gain and bandwidth for neural amplifier and is stable with sufficient phase margin.

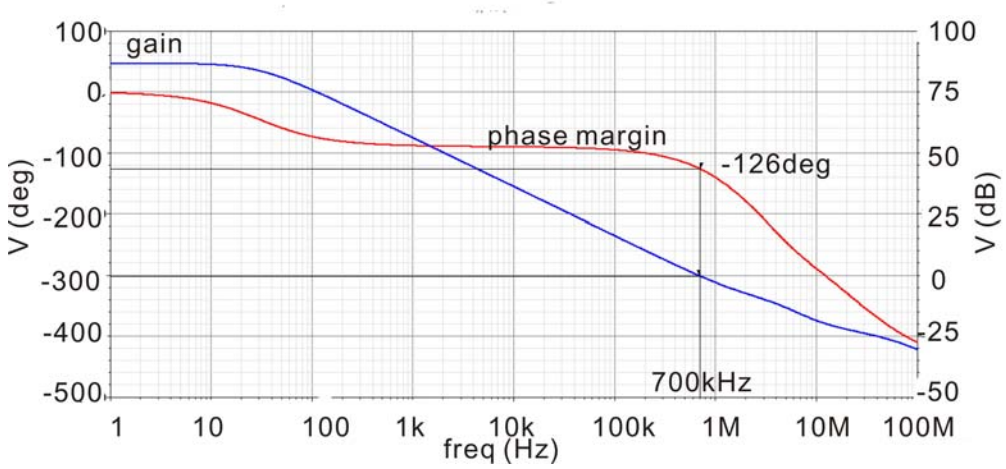
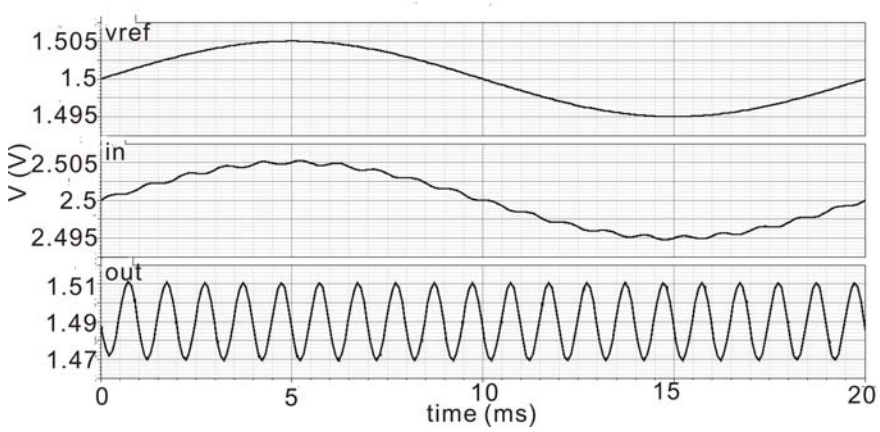


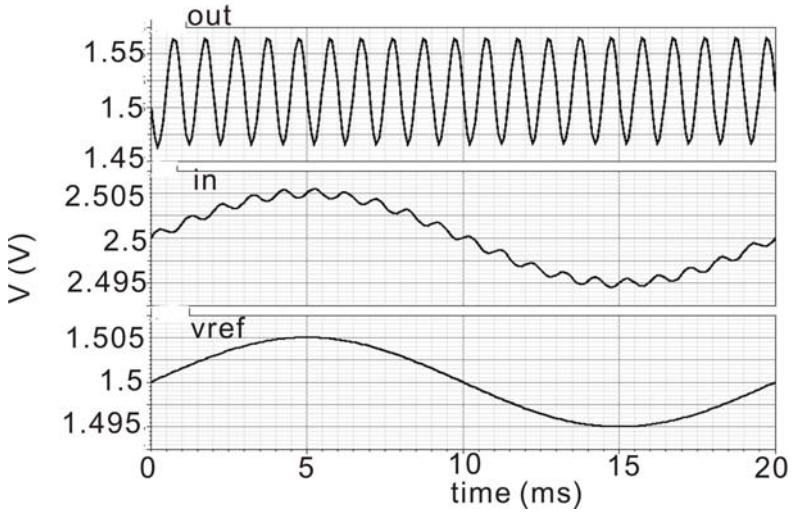
Figure 3.12. Post-layout simulation result of OTA open loop characteristics.

To verify the function of preamplifier, transient analysis was run for neural amplifiers with two different feedback structures in Figure 3.4. The simulated signal V_{ref} on the reference node is a 10mV, 50Hz sine wave, as LFP. The input signal V_{in} on the input node is a 500 μV, 1 kHz sine wave with dc offset of 1V, modulated with the

reference signal. The simulation results are shown in Figure 3.13. On the out node, the LFP and dc offset are removed, showing that the preamplifiers function well.



(a)



(b)

Figure 3.13. Transient analysis of pre-amplifiers with (a) feedback structure I and (b) feedback structure II.

A summary of OTA, pre-amplifier and gain stage amplifier simulation results are shown in Table 3.2.The results are suitable for neural recording application. The PSRR of the gain stage amplifier is a little bit lower than 80 dB, which should be improved in next

generation.

Table 3.2. Post-layout simulation results of neural amplifier.

	OTA	**Pre-amplifier with feedback structure II**	**Pre-amplifier with feedback structure I**	**Gain stage amplifier**
Supply (V)	3	3	3	3
Power (μW)	47.4	47.4	47.4	47.4
Input referred noise (μVrms)	9.25	9.2	9.2	-
Gain (dB)	86.7	38.66	40	21
Bandwidth (kHz)	708	225~6.68	263.8~5.7	-
Phase Margin (°)	54	-	-	-
THD(5mV input)		1%	3.47%	0.3%
CMRR @ 60Hz (dB)	82	80	80	-
PSRR @1kHz (dB)	88	88	88	44
input/output range (V)	0.5 ~ 2.54	-	-	-
Area (mm^2)	0.04	0.07	0.07	0.05

3.5 Test results of neural amplifier

3.5.1 Test set up for neural amplifier

The chip was fabricated in the ON Semiconductor 0.5μm CMOS process. A printed circuit board (PCB) for neural amplifier need be built to evaluate the performance. The power supply, common mode voltage, tuned voltage and biased current supply are on the board. Several operation amplifiers on board are used to test neural amplifier performance.

A 9V battery is used to general low noise power. A low noise power regular MIC5219 is used to convert 9V to 3 V for the chip. There are two way to generate current on the PCB. One way is to connect a variable resistor with power supply directly to

supply tuned current. The other way is to use chip LM334 which is a variable current generator. Low noise amplifiers MC34072 were used to generate modulated sine wave used as the neural amplifier test input. The test board is shown in Figure 3.14. The board is place in a Faraday cage to block the environment noise especially the 50/60Hz noise.

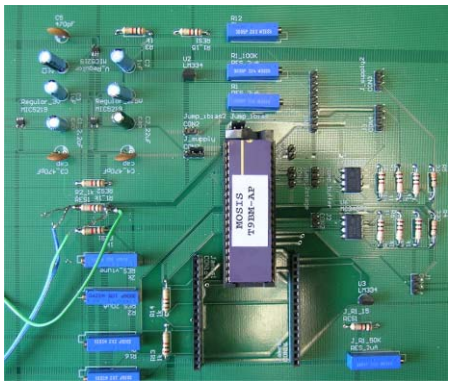


Figure 3.14. PCB for neural amplifier test. The size of the board is 6 inches by 7 inches.

3.5.2 Test results of neural amplifier

The neural amplifier noise performance was tested. The instrument noise was calibrated before the chip test. The instrument noise was measured by short the inputs with ground. When measuring the noise with oscilloscope, the RMS noise got by dividing noise amplitude V_{pp} by a factor of 6, supposing the noise distribution is Gauss distribution. The rms noise of true RMS multimeter was easily got by directly reading the instrument output value. The multimeter is FLUKE 79 III true RMS multimeter. The inherent noise of true RMS multimeter is 20 μV_{rms}. The oscilloscope is Agilent 54624A oscilloscope. Note that the function of "BW limit" should be switched on to decrease the noise effect for oscilloscope. The inherent noise of oscilloscope is 833 μV_{rms}.

To measure the noise performance of the circuit, two inputs of neural amplifier were

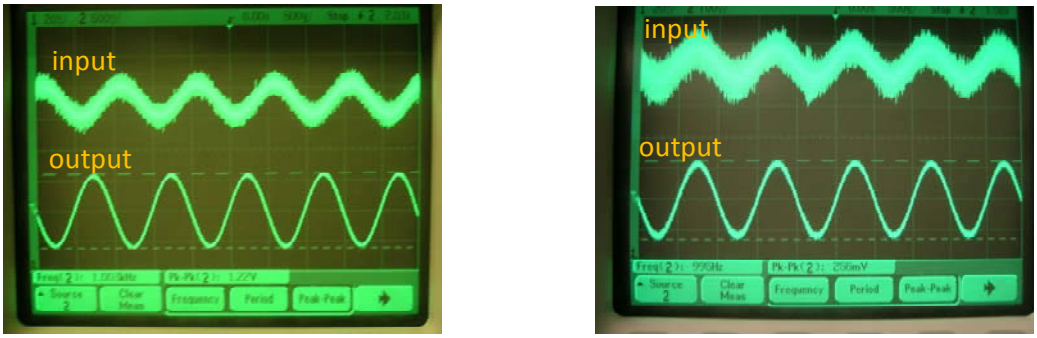
shorted to ac ground, and measure the neural amplifier output with multimeter. The output value is the sum of circuit noise and multimeter inherent noise that was previously measured and can be subtracted.

A simple way is used to measure the CMRR of neural amplifier. The two inputs of neural amplifier are connected together for test input. The input is a sine wave generated by signal generator with an amplitude $V_{pp\_cmrr\_in}$ and dc offset at common mode voltage. Oscilloscope is connected to the neural amplifier output to measure sine wave amplitude $V_{pp\_cmrr\_out}$. The common mode gain A_{cm} can be obtained by $V_{pp\_cmrr\_out}/ V_{pp\_cmrr\_in}$. The CMRR can be calculated by A_{cm}/A_v, in which A_v is the differential gain of neural amplifier.

When measuring PSRR, the two inputs of neural amplifier are connected together to common mode voltage. The power supply for the chip is coupled with a sine wave, whose amplitude $V_{pp\_psrr\_in}$ is around several hundred mV. Oscilloscope is connected to the neural amplifier output to measure sine wave amplitude $V_{pp\_psrr\_out}$. The gain A_{dd} from power line to amplifier output can be calculated by $V_{pp\_psrr\_out}/ V_{pp\_psrr\_in}$. At last PSRR can be got from A_{dd}/A_v.

The signal generator is Tabor Electronics 50Ms/s waveform generator. The minimum sine amplitude output is 20mV, which is used as the artificial neural input. At first, the gain of neural amplifiers is tested, and the test result is shown in Figure 3.15.

The input is a sine wave with frequency of 1kHz and amplitude of 20mV. High frequency ripple can be found on the input wave, which is high frequency noise. For the first stage, the output amplitude is 1.22V. Therefore, the gain of the first stage is 35.6 dB. For the second stage, the output amplitude is 239mV. Therefore, the gain of the second stage is 21dB. For the gain of the first stage, there is a large distortion between the simulation value and test value. The reason is that a buffer is not placed after the neural amplifier. As a result, the pad capacitance provides additional load to the neural amplifier, and leads the decrease of bandwidth. Figure 3.16 shows the test result for input with a dc offset. The result shows that the dc offset is removed by the first stage neural amplifier.



(a) (b)

Figure 3.15. Gain test results of the gain of neural amplifier. (a) The test result for the first stage of neural amplifier. (b) The test result of the second stage of neural amplifier.

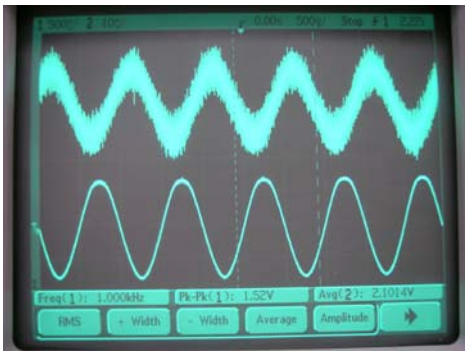


Figure 3.16. Test result of first stage of neural amplifier. The input is 1kHz, 20mV amplitude of sine wave with dc offset of 0.6V.

The test results of neural amplifier are summarized in Table 3.3. All the factors other than the bandwidth meet the design specification. An on-chip buffer can increase the bandwidth and meet the design specification.

Table 3.3. Summary of neural amplifier test results.

Performance	Test results	Design goal
Closed gain of pre-amplifer (dB)	39@500Hz 37.5@1kHz	40
Closed gain of gain stage (dB)	20	20
Input referred noise (μV_{rms})	13	10
Low-cutoff freq. (Hz)	30Hz~300Hz	300
High-cutoff freq. (Hz)	1.4k@Ibias=2μAbias 3.1k@Ibias=4μAbias	7k
PSRR@1kHz (dB)	>72	80
CMRR@60Hz (dB)	>73	80

3.6 Conclusion

In this chapter, the design of neural amplifier suitable for wireless implantable systems was presented. First, single-end and full differential structures were compared and the single-end structure was chosen. Analysis of neural amplifier was given on noise, open loop gain, bandwidth, CMRR, PSRR, etc. to set the specification of neural amplifier. Two versions of neural amplifier were built with two kinds of feedback structures to find out the best structure. The neural amplifier performance is close to the design target. The neural amplifier need also be optimized for higher recording-channel density.

4 Optimized design of pre-amplifier for wireless recording implants

In the future application, higher neural recording channel density is required, for example, more than 100 channels to capture more information of cortex activities. There is neural amplifier in each channel. Therefore, the power of each amplifier is important for the whole system and need to be minimized. This requirement raises a stricter requirement to neural amplifier. In this chapter, a comprehensive analysis was given to provide neural amplifier design guidelines. Following these guidelines, an optimized design of pre-amplifier was built to further decrease the power, area and noise.

4.1 Neural Amplifier Feedback Structures

The best feedback structure of pre-amplifier needs to be found for wireless implanted neural recording system. Two commonly feedback styles of pre-amplifier exist on the neural amplifier test chip. The performance of these two structures is summarized in Table 4.1. Style I was shown to be capable of an adjustable low-cutoff frequency, from less than 1Hz to several hundred Hz by changing the voltage V_{tune}. In contrast, style II only provides a fixed low-cutoff frequency, less than 10Hz even with large size M1 and M2 in feedback path. For neural spikes detection, style II would require an additional filter, e.g., a g_{m}-C filter or a simpler structure [5], to provide a higher low-cutoff frequency, which would occupy more chip area and weaken the total harmonic distortion (THD).

Table 4.1. Performance comparison of pre-amplifier with different feedback structures.

Performance	**Feedback path styles**		
	Style I	***Style II***	***Style II + filter***
Simulated THD	0.9%	0.37%	0.8%
Low cut-off freq.	Adjustable	Fixed	Adjustable
Offset at ouput	Yes	None	None
Area	Small	Small	Medium

Style I produces an offset at V_{out} that is proportional to the input amplitude and can be several mV for neural spikes with amplitude over 300μV. This offset voltage in style I is due to the gate voltage of M1 and M2 being fixed by V_{tune} (0.6V larger than V_{cm}), as shown in Figure 4.1. When V_{in_p} is equal to V_{cm}, V_{out} is pushed to a voltage higher than V_{cm} to ensure M1 and M2 are on and operated in the subthreshold region. This offset also weakens the THD in style I. In style II, the feedback transistors act as pseudoresistor elements [56]. The MOSFETs and parasitic bipolar transistors in these elements act as converse polarity diodes connected in parallel so the output node will never be pushed to an offset above V_{cm}.

Style II without an additional filter the best choice for low frequency neural signals (e.g., LFP) because it has better THD and no offset. However, for recording neural spikes (300Hz to 7kHz), style II requires a filter to raise the low cut-off frequency, which will weaken the THD and increase power consumption. To compare style I and style II accurately, an additional filter was simulated with style II to match the bandwidth of style I. Table I shows that the THD of style I is similar to style II with a filter. The output offset

is not critical because it can be removed by the following variable gain stage. Thus, style I was determined to be better for recording neural spikes because it requires lower power and less chip area.

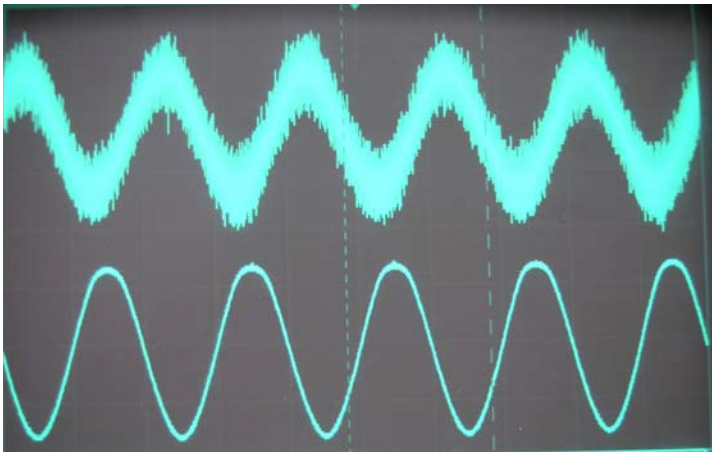


Figure 4.1. Feedback structure test chip results for style I. The input is 1kHz, 20mVpp sine wave and the output is 1.52Vpp sine wave with 0.6V dc offset.

4.2 Pre-Amplifier OTA Structures

There are different OTA structures with different performance. For strictly optimization, the most suitable OTA structure needs to be found out. Optimization of OTA structure can significantly improve all the performance of the system including noise, power, area, etc.. Many different OTA structures have been reported for pre-amplifiers in neural spikes detection, including 2-stage amplifier [20], current mirror [56], folded-cascode amplifier [5] and telescopic amplifier [29]. To determine the optimal OTA structure for pre-amplifiers, this section provides an analysis of OTA performance relative to requirements of wireless implanted neural recording applications.

4.2.1 OTA phase margin and bandwidth

In all the published papers on pre-amplifier of neural recording systems, the OTA

phase margin (PM) is set at a value larger than 50. However, higher closed loop gain inherently provides a larger loop PM [57]. For a pre-amplifier with a large closed loop gain of 40dB, the requirement for the OTA PM at 0dB can be greatly relaxed. To illustrate this principle, suppose that the OTA is a two-pole system with poles at f_{d} and f_{nd}. The loop gain T can thus be expressed as

$$T = \beta(f)A_{\mathrm{o}}(f) = \frac{\beta A_{\mathrm{o}}}{(1 + jf / f_1)(1 + jf / f_2)} \tag{4.8}$$

which results in the gain and phase response illustrated in Figure 4.2. For two possible closed loop gains, A_{c1} and A_{c2}, the loop PM and loop gain T, which is the difference between A_{o} and A_{cx}, are shown. Here, PM_1 and PM_2 are larger than 45º even though PM_0 is almost 0º. Note that PM_1 is larger than PM_2 because of the smaller T_1. Thus, because the closed loop gain can be as large as 40 dB, the PM of the neural amplifier OTA can be very small. The permits OTA design to tradeoff PM for other performance parameters. Thus considering the desired high-cutoff frequency at 7kHz, bandwidth and phase margin are not critical OTA parameters for neural amplifiers. However, because frequency characteristics can vary slightly from theoretical models, and because the neural amplifier filter feedback loop will introduce a new pole, it is important to test stability of the closed loop system before accepting the OTA PM.

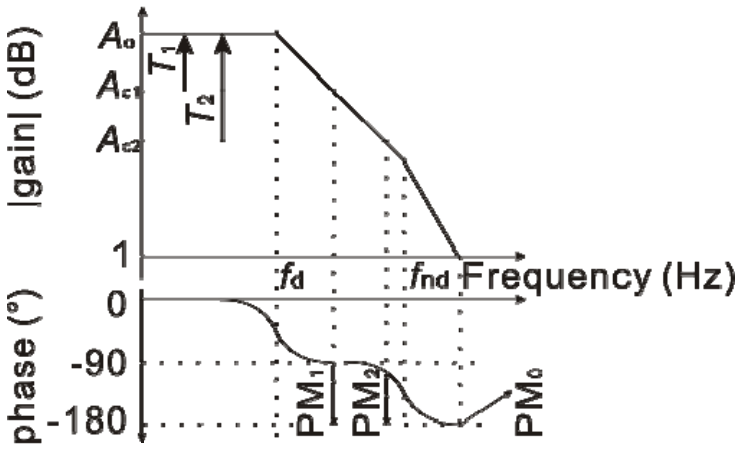


Figure 4.2. Bode plots of gain for two-pole system. PM0 is OTA's phase margin at 0dB and closed to 0 º, whereas PM1,2 is loop phase margin, larger than 45º.

4.2.2 OTA structure analysis

There are a lot of performance factor of OTA. The key performance factors of OTA for wireless implantable application need to be found out. For implantable pre-amplifiers, the the OTA should consume minimal power to avoid damage to human tissue and permit maximum channel density. It should have extremely low noise for high SNR. A very high open loop gain is preferable to minimize the gain error for a large closed loop gain, and high CMRR is needed to reject common mode noise including common mode neural signals and interference from 50/60 Hz power line noise. For implants with wirelessly transmitted power, a high PSRR is needed to reject the large ripple on the power line, which can be larger than 10mV even if the wireless power receiver is followed by a regulator. For example, a PSRR over 80dB is necessary to ensure 10-bit accuracy for a 10mV ripple, assuming a 10μV input. The bandwidth requirement is not strict because the high cut-off frequency is less than 10kHz and the phase margin does not need to be large. The input and output range does not need to be large; for example, for a closed loop gain of 40dB, the output amplitude for a 10μV to 500μV input is only 0.1mV to

50mV.

To sum up, the OTA key performance factors for wireless implantable multichannel neural recording application are power, area, CMRR, PSRR, noise. etc. A generalized comparison of key neural amplifier performance parameters is given in Table 4.2 for the four common OTA structures. It was determined that the telescopic OTA has the best performance for the combination of parameters that are most important for pre-amplifiers.

Table 4.2. Performance comparison of OTA structures.

Performance	**OTA structures**			
	Two stage	***Current mirror***	***Folded cascade***	***Telescopic***
Gain	Good	Poor	good	good
Noise	Good	Poor	fair	good
Power	Poor	Poor	fair	good
Bandwidth	Fair	Good	poor	poor
I/O range	Good	Good	fair	poor
PSRR	Poor	Poor	good	good

It should be noted that a typical neural system also includes a variable gain amplifier (VGA) that follows the pre-amplifier. For this VGA stage, power, output range, CMRR and PSRR are the most important parameters. Table 4.2 indicates that a folded-cascode OTA is best for this stage.

4.2.3 Capacitance optimization for pre-amplifier

The preferred feedback path structure and OTA have been defined for use in a neural spike recording amplifier. To complete the design, values must be assigned to C_a and C_f. This is not a trivial process because these values have a significant impact on noise and

layout area as described in the optimization analysis of this section.

Three primary noise sources must be considered for a neural system: neural signal noise, electrode noise, and electronic noise. For spike recording with a typical microelectrode array, the first two sources can be estimated as 5~10μV_{rms} [58] and 12.6μV_{rms} [43], respectively. The electronic noise should be kept below the total input noise from the neural electrode, which is around 20μV_{rms}. The main source of electronic noise is the pre-amplifier because contributions from following stages will be divided by the high gain of the pre-amplifier stage and can thus be ignored.

The noise model of a pre-amplifier is shown in Figure 4.3. The input referred noise V_{ieq} for OTAs in Table I can be expressed as

$$V_{ieq}^{\ 2} = \frac{\left(C_f + C_a + C_p + C_g\right)^2}{C_a^{\ 2}} \times \frac{16kT}{3g_m} \tag{4.9}$$

where C_g is MOSFET gate capacitance at the OTA input and C_p is the wiring parasitic capacitance that is negligible compared with C_a. Considering the relationship between C_g and g_m, the theory of capacitive noise matching [57] says that V_{ieq} is minimized when C_g = (C_a+C_f). However, in a practical design this minimum can not be achieved without excessive power consumption and chip area.

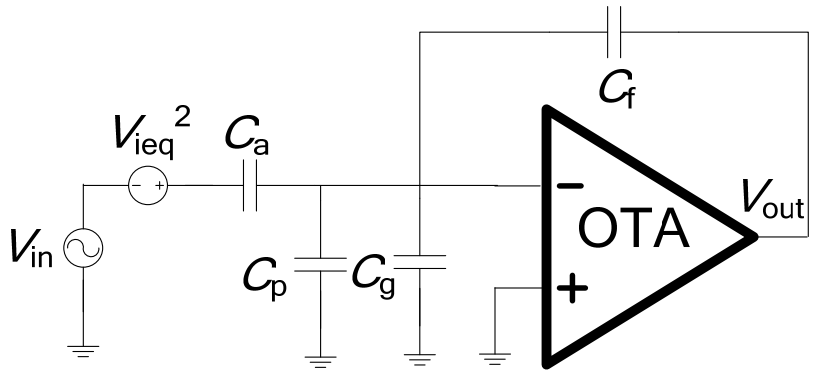


Figure 4.3. Noise model for pre-amplifier.

Consider the standard model for C_g given by

$$C_g = \frac{2}{3} C_{ox} W L_{eff} (1+\gamma) = \frac{C_f + C_a}{N} \tag{4.10}$$

where C_{ox} is the gate oxide capacitance per unit area, γ is a factor relating gate-source and gate-drain capacitances, W and L_{eff} represent the effective gate size, and $N = (C_a+C_f)/C_g$ is a ratio useful in considering capacitive noise matching. C_g is determined by the OTA input transistor size. For neural amplifiers, the sum of C_a and C_f is generally a large value, such that $N \geq 1$. A plot of input referred noise vs. input transistor size [57] shows that smaller N results in better input referred noise when $N \geq 1$. For a fixed input transistor size, i.e. for a fixed C_g, C_f and C_a should kept small to decrease N and thereby improve noise performance. At the same time, this helps to minimize the chip area of the pre-amplifier.

4.3 Optimized pre-amplifier design for wireless implantable multi-channel neural recording application

The analysis above can be summarized by the following design guidelines to improve the performance of pre-amplifier for multi-channel neural spikes recording implants.

1. Style I feedback structure should be used to decrease chip area and power consumption.
2. The open loop phase margin of OTA can be set well below 45º to further improve OTA performance.
3. A telescopic OTA provides a good tradeoff between noise, power and PSRR.
4. The capacitance in the feedback structure should be minimized to improve noise performance and decrease area.

Following the above guidelines, a pre-amplifier was designed in 0.5μm CMOS. C_f was chosen to be 100fF to meet the feedback capacitance guideline with a value large enough to overcome stray parasitic capacitance [20]. The closed loop gain of the pre-amplifier A_c was set at 100, which is the most common value found in neural amplifiers. To match these values, C_a was set to 10pF.

Noise efficiency factor (NEF) is commonly used to qualify the tradeoff between noise, bandwidth and power in neural amplifiers [5, 29, 56, 59]. To set OTA parameters during design, simulations were performed to minimize NEF. Several different bias currents were considered, and 1 μA was found to provide the best NEF. Different input

transistor sizes were also tested, and the final size was set to 165µm by 4.5µm because further increase of size beyond this yielded limited improvement in noise performance. PM optimization was found to enable improvements in open loop gain, noise, power performance, CMRR and PSRR. The final pre-amplifier layout is shown in Figure 4.4 and described by the post-layout simulation parameters in Table 4.3.

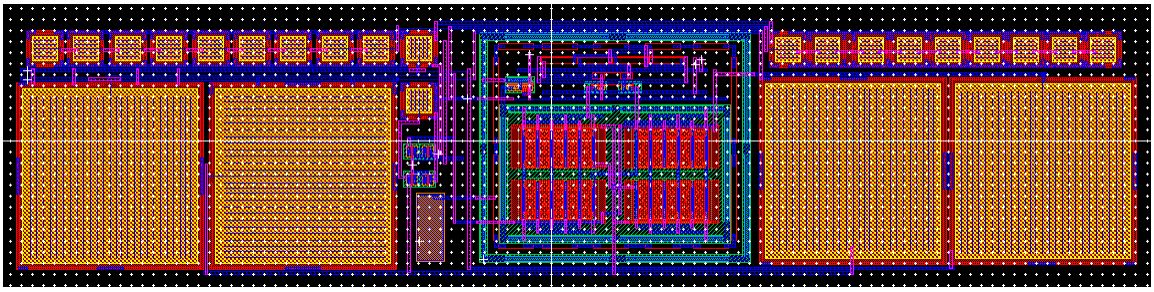


Figure 4.4. Layout of pre-amplifier optimized for our application. The area is 507µm×114µm.

Table 4.3. Post-layout simulation results of pre-amplifiers.

Parameters	**Performance**
N	6.67
Open loop PM of OTA (º)	5
Input referred noise (μV_{rms})	5.38
Bandwidth (Hz)	331-7.1k
CMRR (1-7kHz) (dB)	>43
PSRR (1-7kHz) (dB)	>81
OTA Bias current (µA) @3V	1
Close loop gain (dB)	40
C_L (F)	1.8p
Area (mm^2)	0.058

Layout area of a neural amplifier is important to maximizing the channel density of a multi-channel neural recording system. Supply voltage is also important to evaluate the system power consumption. To incorporate chip area and supply voltage into the performance comparison, a new figure of merit (FoM) is introduced.. The new FoM is

expressed as

$$FoM = NEF^2 \cdot area \cdot V_{\sup ply} = K \cdot V_{ieq}{}^2 \cdot P / BW \cdot area \qquad (3.11)$$

where V_{supply} is the supply voltage, P is the power, BW is the bandwidth, and K is a constant. Lower values of FoM represent a better performance. Table 4.4 shows a comparison of NEF and FoM between reported pre-amplifiers. The design reported in this paper consumes the lowest power, has the lowest (best) NEF and the lowest (best) FoM. Reported NEF and FoM values, normalized to the results of this work, are plotted in Figure 4.5 for easy comparison. Figure 4.5 shows that [5] has the closest NEF but has an FoM that is three times larger. [29] has the closest FoM but its NEF is 83% larger, and the process is more advanced. This comparison shows that the optimization guidelines developed in this thesis enable significant performance improvements in amplifier for wireless neural recordings.

The stability of the pre-amplifiers was verified by applying a 10mV pulse on the input. Figure 4.6 (a) shows there is no oscillation. Initially the output is discharged to zero and then charged to 1.5V by the feedback path. Figure 4.6 (b) shows the transient analysis with artificial neural signal for the amplifier with bias current of 1μA. The input is a signal with amplitude of 200μV and frequency of 1kHz modulated by LFP with amplitude of 10mV, frequency of 50Hz and 1V dc offset. At the output node, LFP and input dc offset is removed while the neural signal of frequency of 1kHz is amplified by 40dB.

Table 4.4. Comparison of pre-amplifier characteristics.

	Process	**Power**	**Gain**	**Area**	**NEF**	**FoM**
[56]	1.5µm	40µW	40dB	0.16mm^2	4	2.56
[5]	0.5µm	7.7µW	40dB	0.16mm^2	2.67	1.14
[29]	0.35µm	4.2µW	34dB	0.02mm^2	4.6	0.42
[59]	0.18µm	7.9µW	39.4dB	0.063mm^2	3.35	0.71
This work	0.5µm	3µW	40dB	0.058mm^2	**2.51**	**0.37**

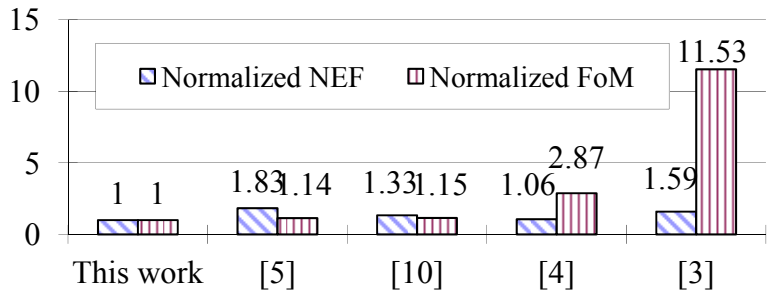


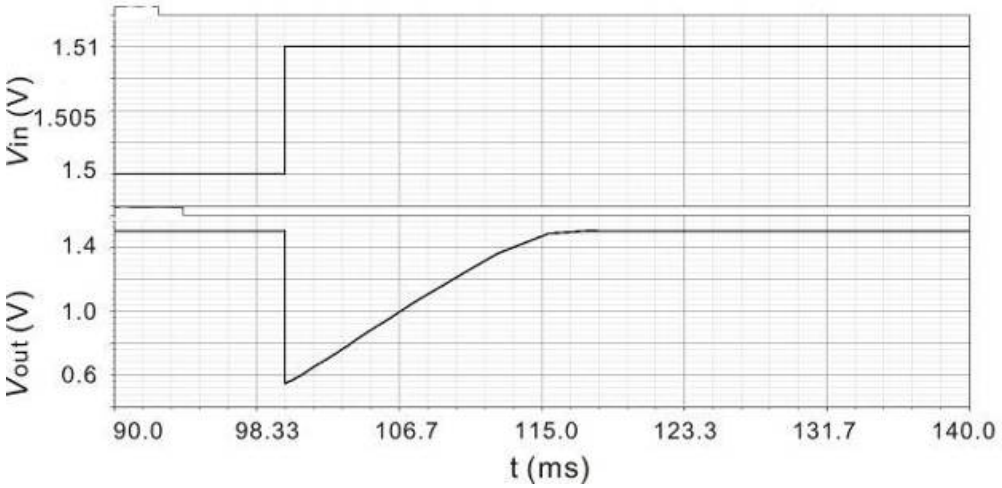
Figure 4.5. Normalized NEF and FoM comparison.

4.4 Conclusion

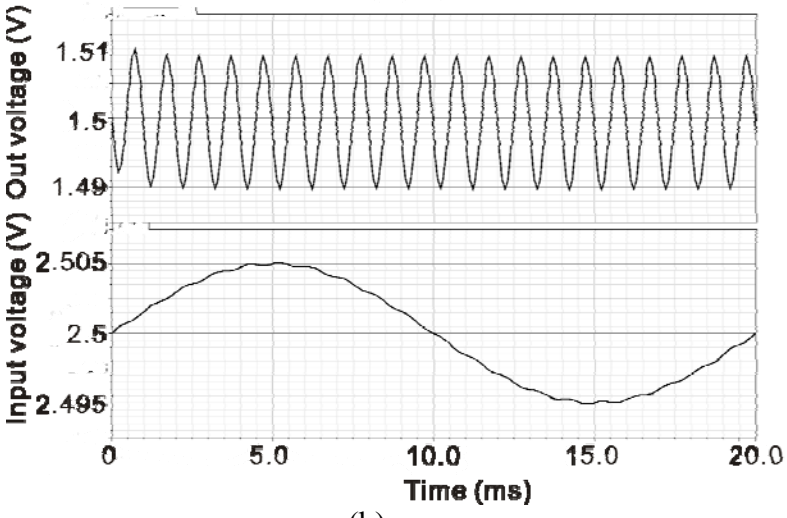
As a key component in the recording channel of wireless implanted neural recording system, the pre-amplifier is extremely important for the system performance. An optimized pre-amplifier was designed to improve the recording-channel density. Two feedback structures of pre-amplifier were compared. Analysis shows that the V_{tune} bias feedback structures is more suitable for neural spikes detection.

Analysis was given for bandwidth, phase margin, CMRR, PSRR, and noise to

determine the OTA structure of pre-amplifier. The telescope OTA was found to be the best structure. OTA performance was found to be optimized with relaxed open loop phase margin requirements. Capacitive noise matching technology was incorporated for noise and area optimization of neural amplifiers. Following the optimization guidelines in this paper, NEF and an FoM for neural amplifiers were effectively improved.



(a)



(b)

Figure 4.6. Transient analysis for neural amplifiers. The input pulse in (a) is 10 mV to test the stabilization. The artificial neural signal input in (b) is 1kHz, 200μVpp signal modulated by 50Hz, 10mV signal with 1V dc offset.

5 Analog-to-digital converter design for implanted neural recording interface

The neural front end includes two main blocks as stated in Section 2.3.1. One is neural amplifiers and the other one is an analog-to-digital converter (ADC). An ADC is needed to convert the analog signal into digital signal for further digital signal processing. This chapter shows the ADC design.

5.1 Analog-to-digital converter specifications and architecture

This thesis work focuses on systems that are wireless and implantable, and the power and area constraints inherent to such systems. The key performance factors of ADC in such systems are resolution, power, sampling frequency and area.

The resolution of the ADC indicates the number of discrete values it can produce over the range of analog values. It can be set by analyzing to dynamic signal-to-noise ratio (DSNR). DSNR for neural interface is defined as the ratio of the maximum input power to the input noise power. For example, the noise from a typical neural probe is 30 μV_{rms}, and the largest spike amplitude is smaller 1mV. Therefore, the DSNR is 31dB. Divided by 6, it is equivalent to 6 bit ADC. To provide a margin of error in ADC design margin, the design specification for ADC accuracy was set to 8 bits. Higher accuracy is unnecessary and undesirable because it would increase the power and area consumed by the ADC.

The sampling frequency of ADC is also named sampling rate. It is defined as the rate at which new digital values are sampled from the analog signal. For our application,

it depends on how many channels sharing one ADC. The purpose to share one ADC among multi channels is that the overall power and chip area of the analog front end can be decreased. At the same time, such a configuration requires an ADC with higher sampling frequency. The bandwidth of the neural spikes is 7kHz. To satisfy the Nyquist sampling frequency theorem, the sampling frequency per channel should be larger than 14kHz. There are 32 channels in our application. Therefore, if one ADC is shared by all these channels, the sampling frequency should be larger than 448kHz. To ensure sufficient design margin, the sampling frequency was set to 700kHz.

The chip area is largely occupied by capacitor area especially for those ADC structure with capacitance array. For example, for a successive approximation (SAR) ADC, the area increases exponentially with respect to the resolution [43]. In a wireless implantable multi-channel neural recording system, the total power budget of front end is 5mW, and the less, the better. Based on the design experience, the power of the ADC is set at 300μW.

To sum up, an 8-bit ADC with sampling frequency of 700kHz and 300μW is needed for our application. There are several ADC structures suitable for this application, such as oversampling ADC, algorithmic ADC and SAR ADC. SAR ADC can provide required accuracy and bandwidth [60] low power and small area [61]. Therefore, SAR architecture was selected as ADC.

5.2 Principle of SAR ADC

The SAR ADC architecture is shown in Figure 5.1. The main blocks include digital

logic controller, comparator, capacitor array DAC, and switch array. The operation starts by sampling the analog input signal and storing it as V_h by capacitor array. After that, the successive approximation starts. It requires N clock cycles to complete an N-bit conversion. At every clock cycle, the digital logic controller's 8-bit output changes according to the comparator's output. The switch array changes the corresponding switches' status, resulting in the change of V_h. The new V_h changes the comparator's output for the next clock cycle. This process goes again and V_h is successively approaching to $V_{cm.}$ At the end of N clock cycle, the digital logic controller's 8-bit output is also the ADC output.

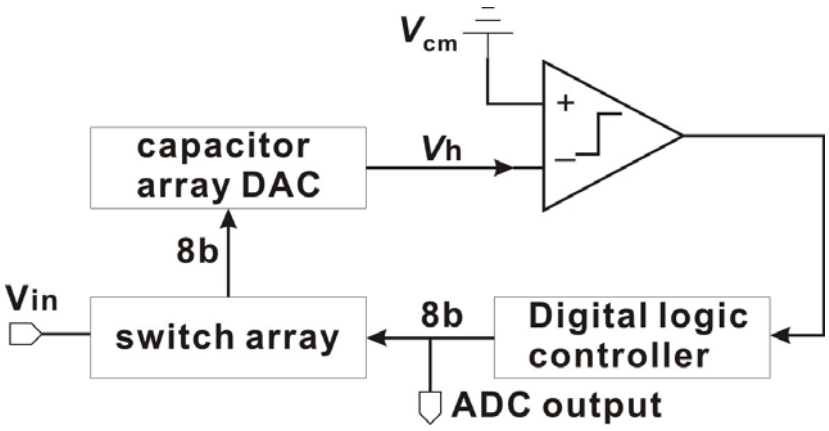


Figure 5.1. SAR ADC block diagram.

The algorithm for SAR ADC is illustrated in Figure 5.2. i stands for clock cycle in successive approximation. Based on the value of V_h, b_i of digital logic controller is set to 0 or 1. The action of switch array results in the change of V_h. If b_i=1, then $V_h \rightarrow V_h+V_{ref}/2^{i+1}$. Otherwise, $V_h \rightarrow V_h-V_{ref}/2^{i+1}$. As i increase, ΔV_h become less and less. At

last, $\Delta V_h = V_{ref}/2^N$, which is the least significant bit (LSB) of SAR ADC.

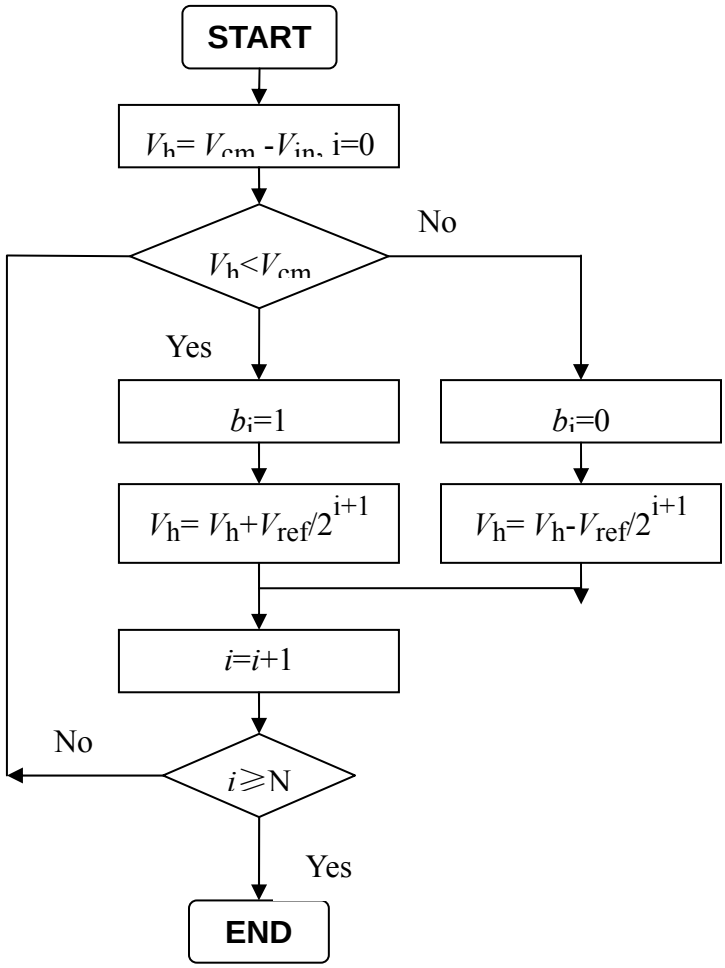


Figure 5.2. Data flow graph for successive approximation.

The operation phases for SAR ADC include sampling phase, hold phase, and bit cycling phase. In sampling phase, the input analog signal is sampled. Switches positions in sampling phase is shown in Figure 5.3. The total capacitance C_T is $2^{N+1}C$. In the sampling phase, $V_h = V_{cm}$ and V_{in} is sampled by the capacitor array. Now the total charge Q on the node of "V_h" is

$$Q = C_T(V_{cm} - V_{in}) \tag{4.1}$$

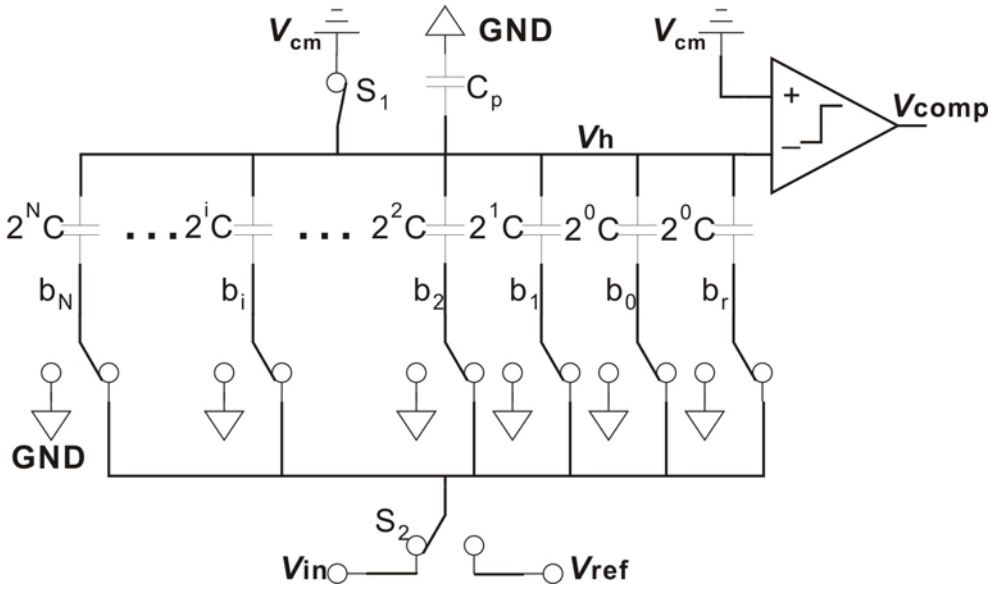


Figure 5.3. Switches' positions of SAR ADC in the sampling phase.

In hold phase, the sampled input in sampling phase is stored. Figure 5.4 shows the switches' positions in the holding phase. C_p is the parasitic capacitance on the node of "V_h". Now each plate of all the capacitors is set to GND. Now the Q is

$$Q = (C_T + C_p)(V_h - 0) \tag{4.2}$$

The total charge on node V_h is the same as in the sampling phase. Therefore, Setting (4.1) equal to (4.2) and solving for V_h, we get

$$V_h = \frac{C_T}{C_T + C_p}(V_{cm} - V_{in}) \tag{4.3}$$

In the bit cycling phase, the digital output of the SARADC approaches the input value, and in the last phase the error between the input and output is the smallest. Figure 5.5 shows the switches' positions in the bit cycling phase. Initially, b_N is set to 1, and one plate of the left capacitor is connected to V_{ref}. The total charge on the node of V_h is

$$Q = \frac{1}{2} C_T (V_h - V_{ref}) + (\frac{1}{2} C_T + C_p)(V_h - 0) \tag{4.4}$$

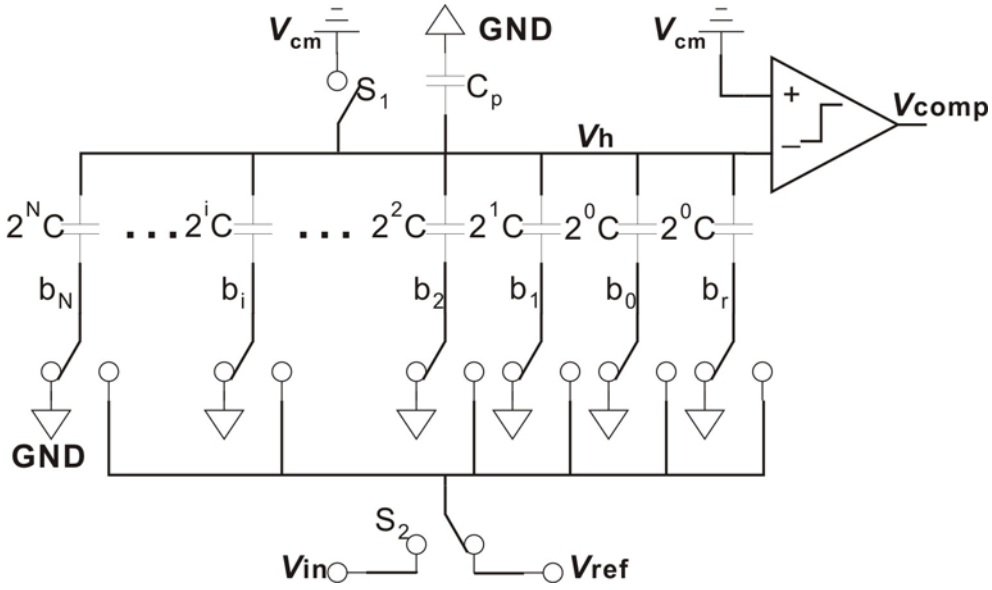


Figure 5.4. Switch positions of SAR ADC in the holding phase.

The total charge on node V_h is the same as in the sampling phase. Therefore, Setting (4.1) equal to (4.2) and solving for V_h, we get

$$V_h = \frac{C_T}{C_T + C_p}(V_{cm} - V_{in}) \tag{4.5}$$

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$$Q = \frac{1}{2} C_T (V_h - V_{ref}) + (\frac{1}{2} C_T + C_p)(V_h - 0) \tag{4.6}$$

Setting (4.1) equal to (4.4) and solving for V_h, we get

$$V_h = \frac{C_t}{C_t + C_p}(V_{cm} - V_{in}) + \frac{1}{2} V_{ref} \frac{C_t}{C_t + C_p} \tag{4.7}$$

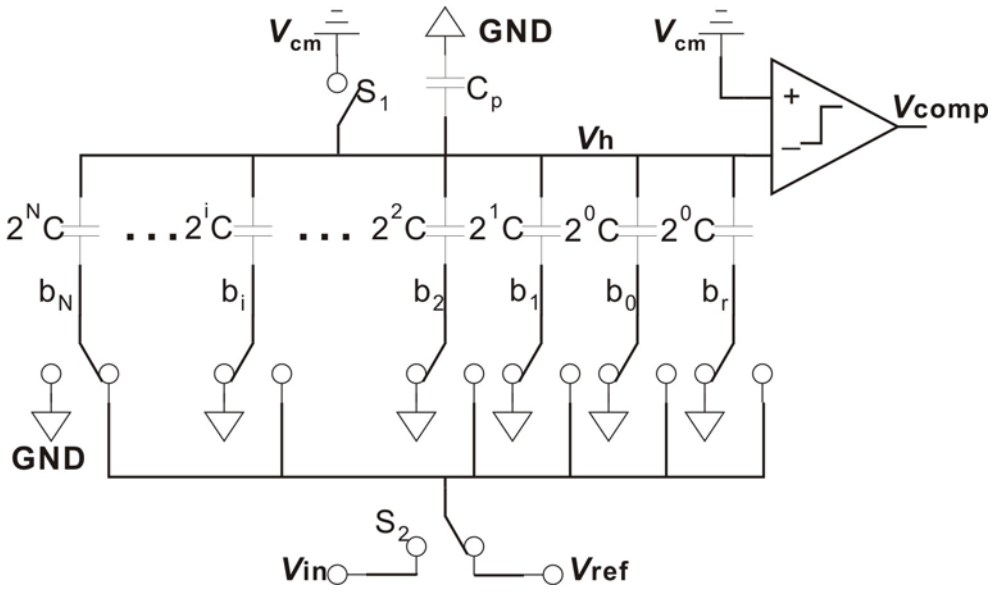


Figure 5.5. Switches' positions of SAR ADC in the bit-cycling phase.

Next, V_h is then compared with V_{cm} by comparator, which performs

$$V_{cm} - V_h = \frac{C_t}{C_t + C_p}(V_{in} - \frac{1}{2}V_{ref} + \frac{C_p}{C_t}V_{cm}) \tag{4.8}$$

If the output of comparator V_{comp} is equal to1,then b_N is set to 1. Otherwise, b_N is set to 0.

The bit cycling phase includes 8 clock periods. The 8-bit digital command code D7-D0 is shown in Table 5.1, at each clock period.

(4.6) shows an SAR ADC output offset

$$Offset = \frac{C_p}{C_t}V_{cm} \tag{4.9}$$

Table 5.1. Digital command codes for SARADC

Cycles	Digital command code								V_{comp}
0	1	0	0	0	0	0	0	0	D7
1	D7	1	0	0	0	0	0	0	D6
2	D7	D6	1	0	0	0	0	0	D5
3	D7	D6	D5	1	0	0	0	0	D4
4	D7	D6	D5	D4	1	0	0	0	D3
5	D7	D6	D5	D4	D3	1	0	0	D2
6	D7	D6	D5	D4	D3	D2	1	0	D1
7	D7	D6	D5	D4	D3	D2	D1	1	D0
Final codes	D7	D6	D5	D4	D3	D2	D1	D0	-

Output offset needs to be decreased for large dynamic range and output accuracy. To decrease the ADC output offset, C_p/C_t should be minimized. Increasing unit capacitance

C of capacitor array can also decrease the offset error because C_T is larger. Larger *C* can also decrease kT/C switch noise.

5.3 Design of main blocks of SAR ADC

5.3.1 Capacitor array design

The capacitor array functions as a DAC to convert 8-bit digital signal into analog signal. For the design of capacitor array, there is a tradeoff between chip, area, sampling frequency and noise. A large total capacitance increases the chip area, decreases the maximum sampling frequency, but also decreases the *k*T/C noise. For this design, the noise requirement is not critical because the only 8-bit is required. The chip area and sampling frequency should be given be priority consideration. The total capacitance is 2^8C here, where C is the unite capacitance and was set at 20fF.

5.3.2 Comparator design

A high performance comparator consists of three stages: a pre-amplification stage, a positive feedback stage and an output buffer stage. The schematic of comparator is shown in

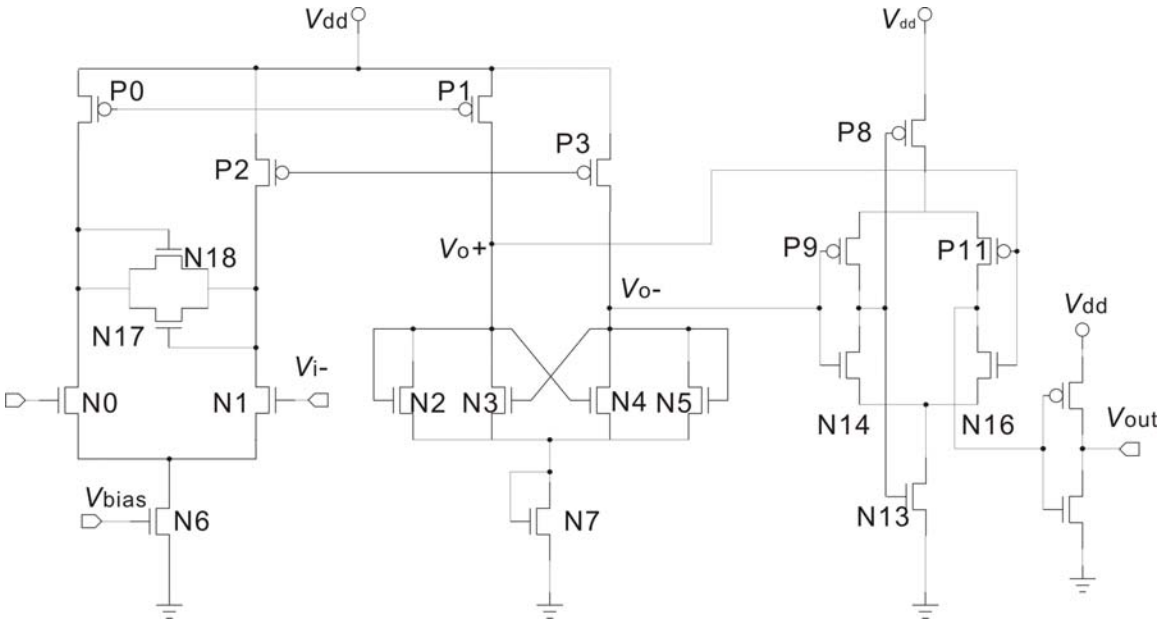


Figure 5.6. The pre-amplification stage is formed by $N_{1,2}$, $N_{17,18}$, and P_0-P_3. This stage amplifies the input signal to improve the comparator sensitivity and also isolates the input stage from kickback noise from the following stages of comparator. The positive feedback stage uses latch to compare the two input signals and store the result. The output buffer stage provides large load drive capacity with large size transistors. The main purpose of the output buffer is to convert the latch output into real digital signal range from 0V to 3V. Large size P10 and N15 is used to improve the driving capacity.

A design tradeoff exists between the pre-amplification gain, resolution, power consumption and speed. The gain of the pre-amplification stage is

$$A_{i-v} = \frac{I_{o+} - I_{o-}}{V_{i+} - V_{i-}} = Rg_{m1} = R\sqrt{K(W/L)_{1,2} I_{ss}} \quad (4.10)$$

where g_{m1} is the transconductance of $N_{1,2}$, R is the W/L ratio between $P_{1,3}$ and $P_{0,2}$, I_{ss} is

the tail current of input pair, and $(W/L)_{1,2}$ is the W/L ratio of $N_{1,2}$. Increasing R, $(W/L)_{1,2}$ and tail current can improve the gain of the first stage. Large tail current increases the power consumption; large $(W/L)_{1,2}$ decreases speed. Note that the length of $N_{1,2}$ should be small to reject the channel length modulation effect which may give rise to an unwanted offset voltage.

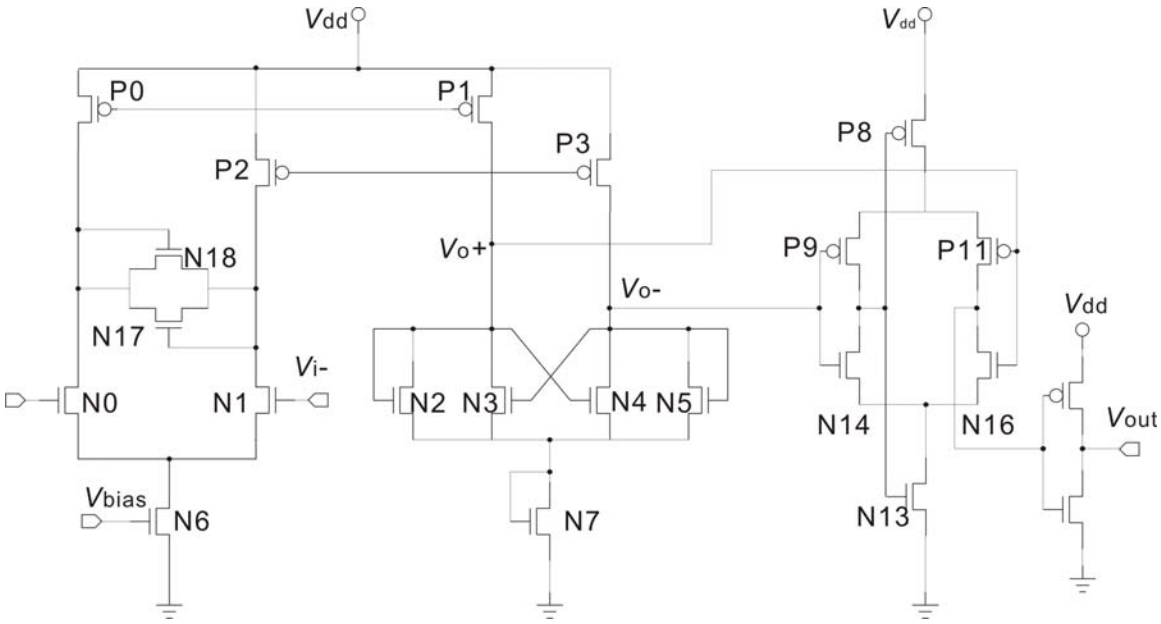
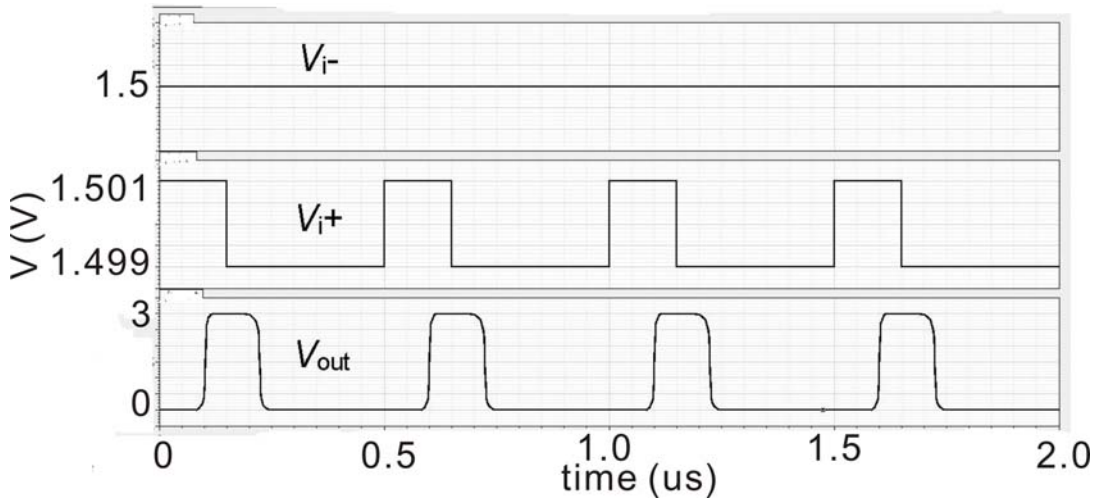


Figure 5.6. High speed latched comparator schematic for SAR ADC.

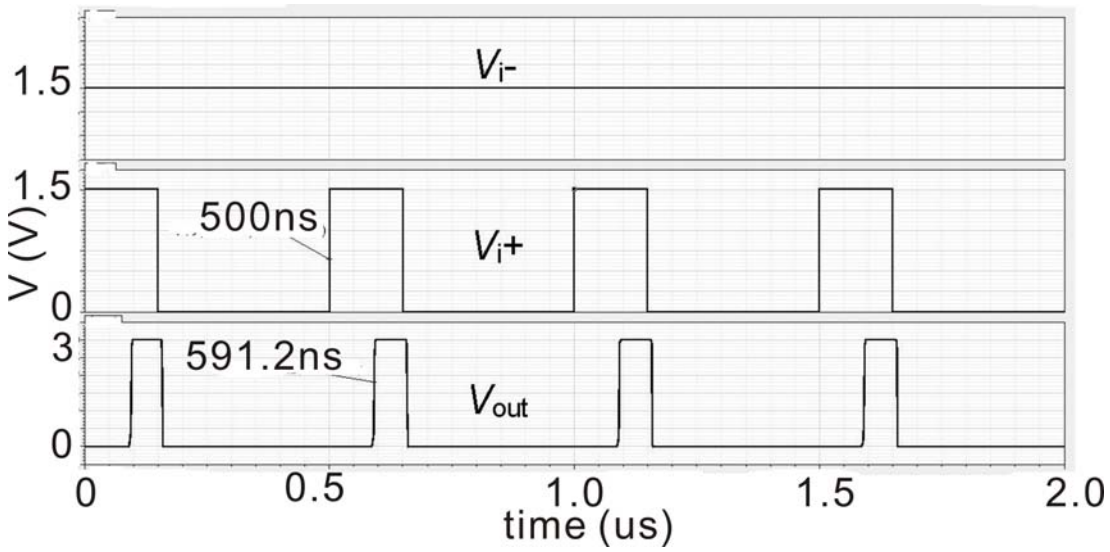
A clamped configuration is used to increase the operation speed of comparator by N_{17} and N_{18}. These two diode-connected transistors ensure that the difference of the voltage on the drain ends of N_0 an N_1 is always less than V_{thn}. In this way, the

comparator speed increases. For example, without N_{17} and N_{18}, if a pulse from 0V to 1.51V is applied to the input node V_i+, N_1 and $P_{0,1}$ is off at the beginning and on at the end. The node 9 needs to be discharged from V_{dd}-V_{thp} to V_{cm}- V_{thn}+V_{sat1} with a range of 1.7V. With N_{17} and N_{18}, the discharge range on node 9 is less than 0.7V.

To set the comparator resolution specification, note that the comparator should resolve the input signal down to 0.5LSB, where for 8-bit ADC, the LSB is $V_{ref}/2^8$. In this design V_{ref}= V_{dd}=3V, 0.5LSB=0.006V. The resolution of comparator should therefore be less than 6 mV. Figure 5.7. (a) shows the comparator output when a pulse with amplitude from 1.499V to 1.501V was applied on Vi+. The accuracy of the comparator achieves 2mV, meeting the design requirement.



(a)



(b)

Figure 5.7. Transient simulation analysis of the comparator (a) for resolution and (b) for delay. The input in (a) is a pulse with amplitude from 1.499V to 1.5001V. The input in (b) is a pulse with amplitude from 0V to 1.5005V pulse.

To find out the maximum speed of comparator, the comparator delay was simulated. A pulse with amplitude from 0V to 1.5V was applied on *V*i+ and the comparator output is shown in Figure 5.7. (b). The delay of comparator is 91ns for a 0V to 1.505V pulse. With this comparator, 1M Sampling/s speed can be achieved for 8-bit application.

The offset of the comparator was simulated by applying a dc sweep potential on the node of *V*i+. The comparator output response is shown in Figure 5.8. Figure 5.7. The plot shows that the comparator offset is 0.2mV.

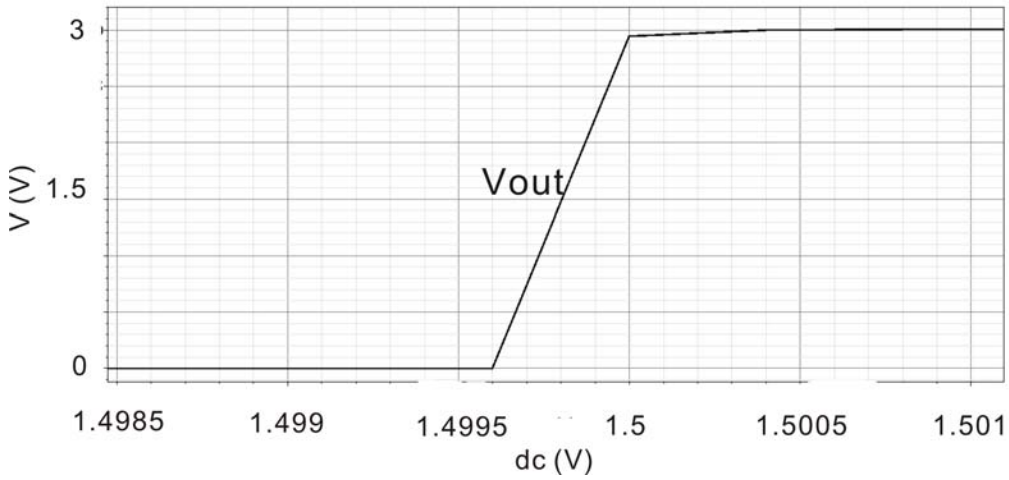


Figure 5.8. DC analysis for comparator dc offset.

5.3.3 Digital logic controller design

The digital logic controller is a key component to finish successive approximation. It provides capacitor array DAC input. This component includes two parts: shift register and conversion register. The SAR digital logic module shown in Figure 5.9 was implemented with a structure similar those previously reported [17, 61, 62].

The upper part is a shift register formed with nine D flip-flops. The bottom part is the conversion register that is formed by nine D flip-flop and outputs digital control command D7~D0 based on the comparator output COMP. Reset signal RST resets the shift register into 10000000. At every following clock rising edge, 1 shifts 1 bit towards lower bit, and comparator output COMP is stored in conversion register. Table 5.2 shows the conversion steps of SAR logic module when the final output is 10011001.

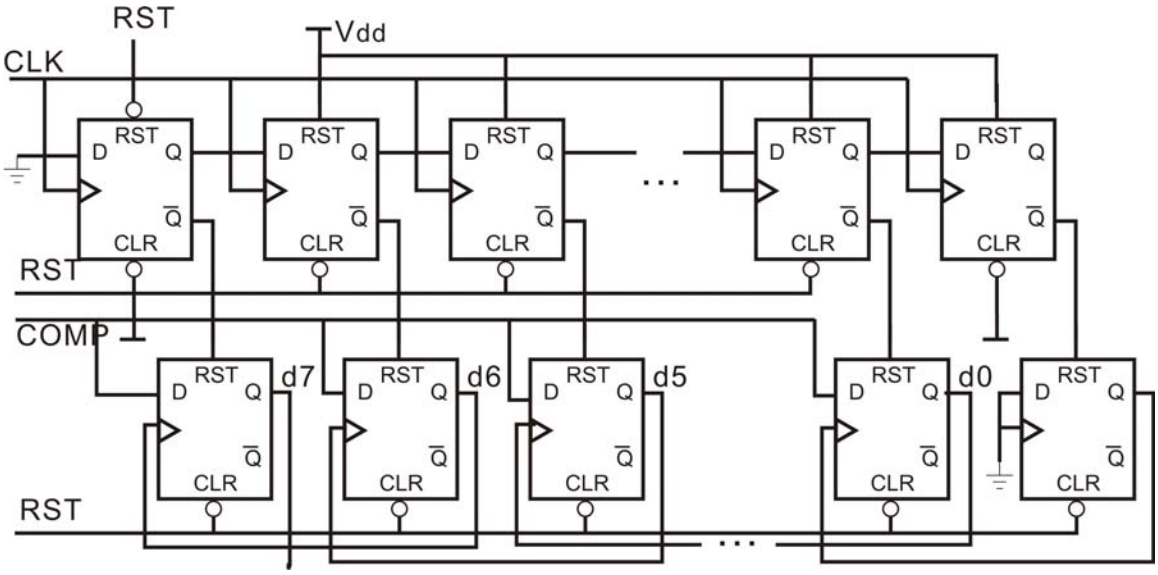


Figure 5.9. Digital logic module of SAR ADC.

Table 5.2. Register actions for 8-bit SARADC.

Conversion steps	Shift register								Conversion register								COMP
0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
1	0	1	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0	1	0	1	0	0	0	0	0	0
3	0	0	0	1	0	0	0	0	1	0	0	1	0	0	0	0	1
4	0	0	0	0	1	0	0	0	1	0	0	1	1	0	0	0	1
5	0	0	0	0	0	1	0	0	1	0	0	1	1	1	0	0	0
6	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	0	0
7	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
Final codes	-	-	-	-	-	-	-	-	**1**	**0**	**0**	**1**	**1**	**0**	**0**	**1**	-

The digital controller block function is verified by applying a artificial COMP input. The simulation result is shown in Figure 5.10. D7-D0 is the digital output of conversion register. The key is to check whether the COMP value at the rising edge of CLK has been stored by conversion register. The simulation result shows that at 0.466ms, all the expected COMP values were stored by digital logic controller. Therefore, the digital controller block functions very well.

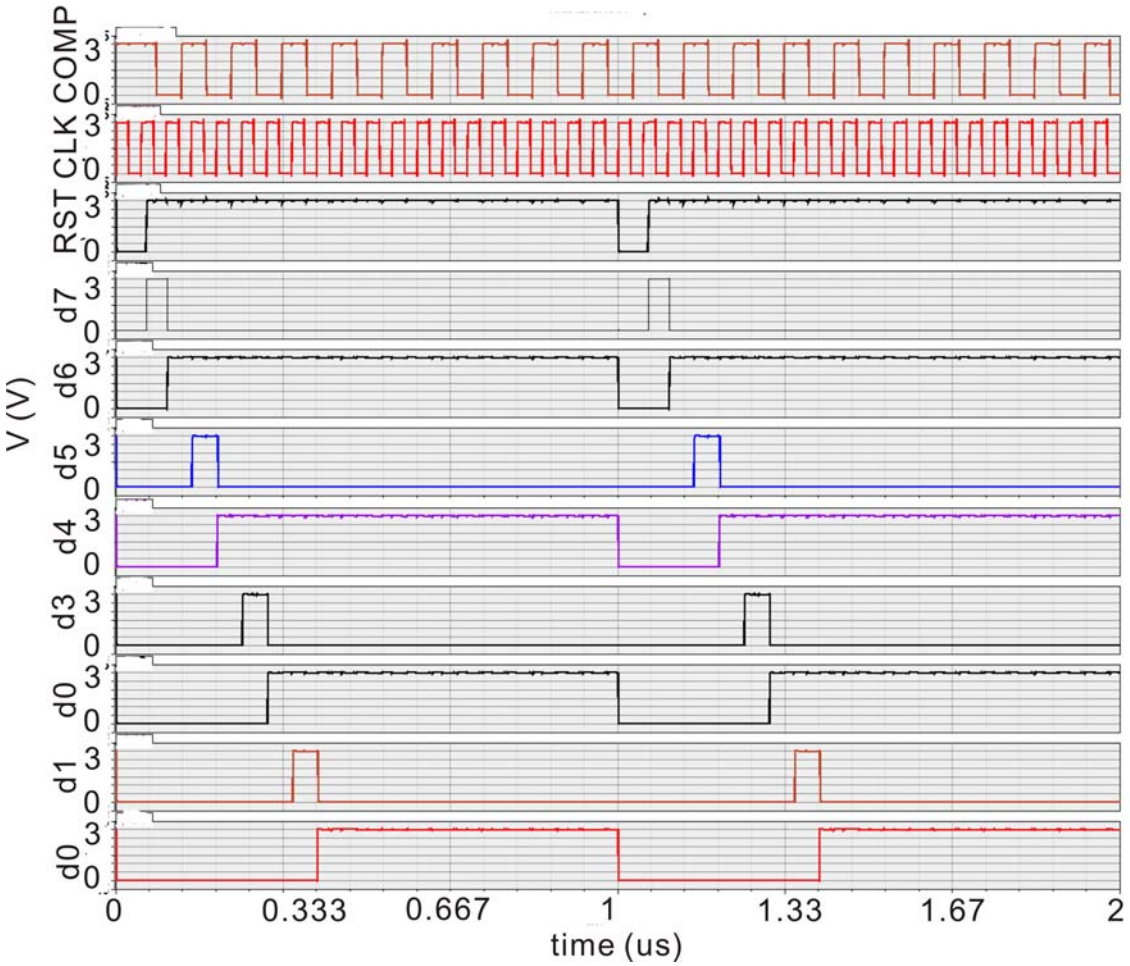


Figure 5.10. Simulation results of digital controller block.

5.3.4 Switches design

Two kinds of switches are needed in SAR ADC design. As shown in Figure 5.3, one is bank of two-way selection switches including b7~b0, br, S2, and the other is an one-way switch S1. The two-way selection switch was realized with two transmission gates. These gates have large size to decrease the equivalent resistance and increase capacitor array charge speed. To design switch S1, the signal range needs to be discussed. For an analog input ranging from 0V-3V, V_h ranges from -1.5V to 3V. Therefore, PMOS transistor was used as switch S1. The size of PMOS was minimized to reject switch noise.

A dummy transistor was used for S1 to decrease the charge injection noise.

5.3.5 Layout design of SAR ADC

The ADC linearity is sensitive to the ratio accuracy of capacitor array, which can be improved with good capacitive matching. Common-centroid layout design was used for capacitor array layout design. The least small capacitor is C, and the largest capacitor is $128C$. The capacitance larger than C was divided into two equal parts and place symmetrically. Dummy capacitors were used around the array outside to further improve the capacitor matching. The upper plates of the capacitor array were connected to the node V_h to decrease parasitic capacitance. In this way, the ADC offset and noise were decreased. The layout of digital logic controller block was generated by Encounter Digital Implementation System from Cadence. The final layout of SAR ADC is shown in Figure 5.11. The core area is 0.23 mm^2. The digital logic controller, the capacitor array and switch array occupy a large area together.

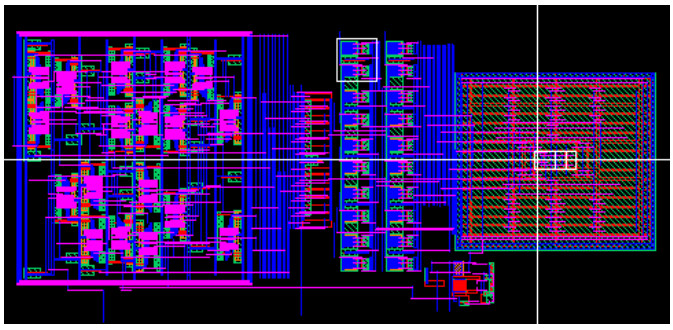


Figure 5.11. Layout of SARADC.

5.4 SARADC design results

To simulate the ADC output error, different DC voltages were applied on node V_{in}.

Figure 5.12 shows the simulation result when V_{in}=1.8V as an example. For V_{in}=1.8V, the ADC output error is 7mV, equal to 0.6LSB. ADC output errors for all DC input are listed in Table 5.3. The output shows that the SAR ADC functions well. The largest output error 0.8LSB occurs when the input is 0.9V and 2.4V.

The performance summary of SAR ADC is shown in Table 5.4. The sampling rate is larger than 714kS/s. The total power consumption is 242μW and only 7.56μW is consumed per recording channel. All these parameters meet the design goals.

Table 5.3. ADC output code and error.

Analog input	**ADC output**	**ADC output error**	
0V	0000’0000	0mV	0LSB
0.3V	0001’1001	-7mV	-0.6LSB
0.6V	0011’0011	-2.3mV	-0.2LSB
0.9V	0100’1100	-9.4mV	-0.8LSB
1.2V	0110’0110	-4.7mV	-0.4LSB
1.5V	1000’0000	0mV	0LSB
1.8V	1001’1001	-7mV	-0.6LSB
2.1V	1011’0011	-2.3mV	-0.2LSB
2.4V	1100’1100	-9.4mV	-0.8LSB
2.7V	1110’0110	-4.7mV	-0.4LSB
2.99V	1111’1111	-1.2mV	-0.1LSB

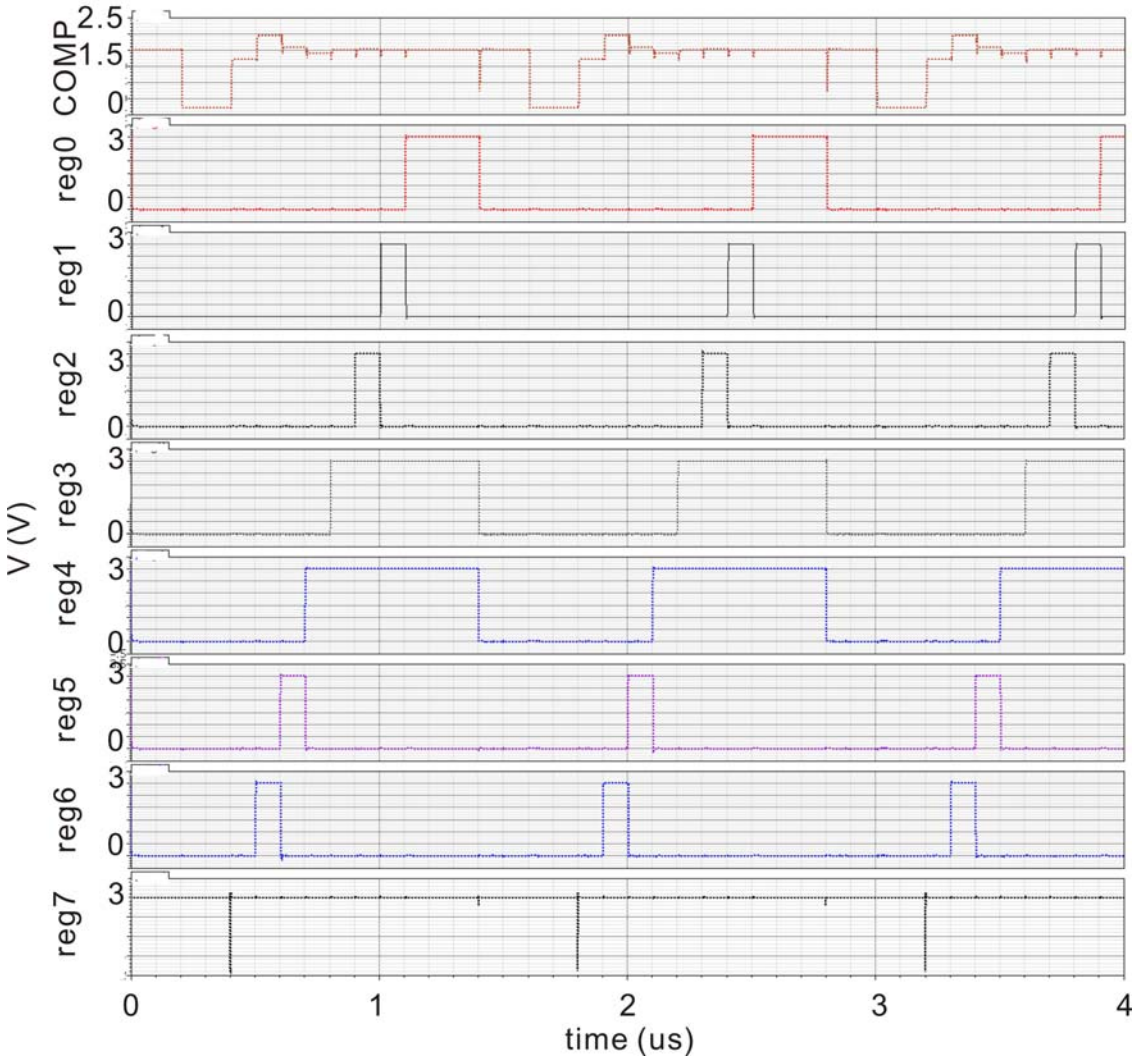


Figure 5.12. Simulation results of SAR ADC output. V_{in}=1.8V. Output=10011001=1.7930V.

Table 5.4. Performance summary of SAR ADC.

Parameter	**Value**
Input range	0V to 2.99V
Sampling rate	714kS per second
Accuracy	8bits
Area	0.23mm^2
Total power	242μW
Channels	32
Power per channel	7.56μW per channel

5.5 Conclusion

This chapter described an SAR ADC design for wireless implantable neural recording system. The SAR ADC is composed of comparator, digital controller block module, capacitor array and switch array. The principal of SARADC was introduced. The design details of these blocks were discussed. Simulation was run for ADC performance. The design results show the performance of SARADC meets the system requirement.

6 Conclusion and future work

6.1 Conclusion and contribution of this work

This thesis developed a neural front end circuit for wireless implants. The front end circuit includes two parts: neural amplifier for neural spikes detection and SAR ADC for data conversion. Two versions of neural amplifier were design. The second version was designed based on the test results of the first version and comprehensive analysis of neural amplifier. The single-end neural amplifier with telescope OTA and voltage-tuned feedback structure was found to be suitable for spikes detection. Phase margin of OTA can be optimized to improve other performance factors. Capacitive noise matching was considered to set the capacitance of neural amplifier. Different ADCs were compared and SAR ADC was found to be suitable for spikes detection. An 8-bit SAR ADC was developed with a sampling rate of 714kS/s and power consumption of 7.56μW/channel. The main contributions:

1. A new figure of merit was introduced to evaluate the neural amplifier performance. In contrast to traditional neural amplifier metrics, this figure of merit takes the chip area and power into consideration to provide a better all-round performance evaluation for wireless implants.

2. A comprehensive neural amplifier optimization approach incorporating relaxed phase margin and capacitive noise matching was introduced and utilized for the first time to optimize amplifier performance for wireless implants. Amplifier architectures and feedback structures were analyzed to identify the best choice for implantable neural recording applications. Bandwidth and phase margin requirements were analyzed to

identify an optimization path through relaxing phase margin requirements. To optimize the noise performance and circuit area, noise capacitive matching was applied to optimize the size of neural amplifier capacitors. Following the optimization guidelines identified in this paper, noise efficiency and the new figure of merit for neural amplifiers were effectively improved.

3. An SARADC tailored to wireless implantable neural recording systems was designed. It is able to process 32 neural spikes recording channels in a multiplexing manner with low power consumption and low area occupation.

6.2 Future work

The work in this thesis provides a solid basis for realizing a wireless implantable neural recording system. Further work is needed for system integration.

1. Test the whole neural front end with real neural spikes. Do the animal experiment with implanted neural probes to test the neural front end performance.
2. Design the spike detection circuit to decrease the data density in order to save the transmission and data processing power; optimize the SAR ADC with capacitive split-array structure to decrease the chip area for higher recording-channel density.
3. Combine the neural recording front-end circuit in this thesis with digital processing block and wireless power and data transmission module to form a complete wireless implantable neural recording system.

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